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Communication System Lab

Title of the Experiment: Frequency Modulation and Demodulation

Experiment No: 3

AIM

1. To generate frequency modulated signal using 555 timer IC.
2. To calculate frequency deviation and modulation index of the generated FM signal.
3. To demodulate the FM modulated signal using 565 Phase Locked Loop (PLL).

APPARATUS REQUIRED

1. NE 555 and LM 565 IC (Both 1 pcs).
2. Resistors and capacitors as per shown in the circuit diagram.
3. Function generator
4. Digital Storage Oscilloscope

Theoretical Background

Part I: Frequency Modulated Signal

In angle modulated signal the spectral components of the modulated waveform depend on the amplitude as well as the frequency of the spectral components in the baseband signal. The modulation system is not linear and hence superposition principle does not hold true. In these systems if the frequency of the carrier is dependent on the amplitude of the baseband signal and the amplitude of the carrier signal remains constant. This type of the signal is called as frequency modulated signal which offers a high signal to noise ratio although its coverage area is limited as compared to amplitude modulated signal.

Part II: Introduction to NE-555

555 timer is a generic IC which is widely used for generating accurate time delay or oscillation in analog integrated circuits. A single 555 timer can provide time delay ranging from few microseconds to as longs as several hours which enables its usage for clock generation purpose.

The 555 timer can be used with power supply in the range of +5 V to +18 V with maximum drive load upto 200 mA. The beauty of this timer IC lies in its compatibility with both TTL and CMOS logic circuits. Due to the wide range of power supply, 555 timer is versatile and easy to use in various applications which includes oscillator, pulse generator, ramp and square wave generator, mono-shot multivibrator etc. The function block diagram of 555 timer is shown in Fig. 3(a) and complete circuit diagram is shown in Fig. 3(b).

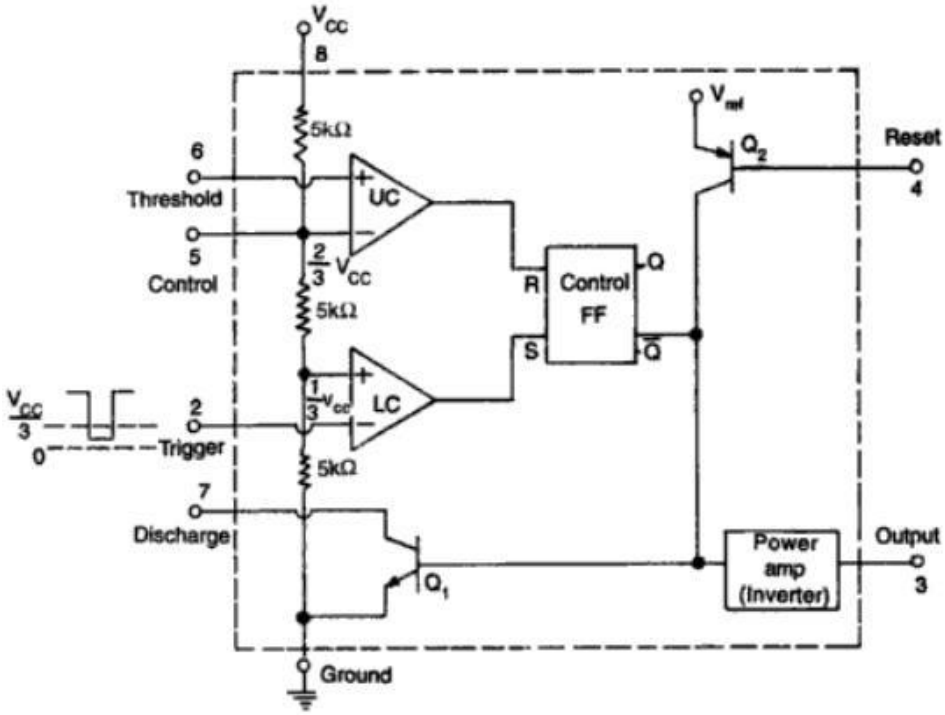
Part III: Operation of NE-555

Refer to Fig. 3(a). The three 5 kΩ internal resistors act as voltage divider providing bias voltage of 2/3 V_{CC} to the Upper comparator (UC) and 1/3 V_{CC} to the lower comparator (LC) where is V_{CC} is the supply voltage. These two voltages fix the necessary comparator threshold voltage which further aids determining the timing interval. **However it is possible to vary time electronically too by introducing modulation voltage to the control voltage input terminal (Pin 5). In applications where the no such modulation input is required Pin 5 should connected to ground terminal via a 0.01 µF capacitor to by-pass noise or ripple voltage from the power supply to avoid any undesired oscillation.**

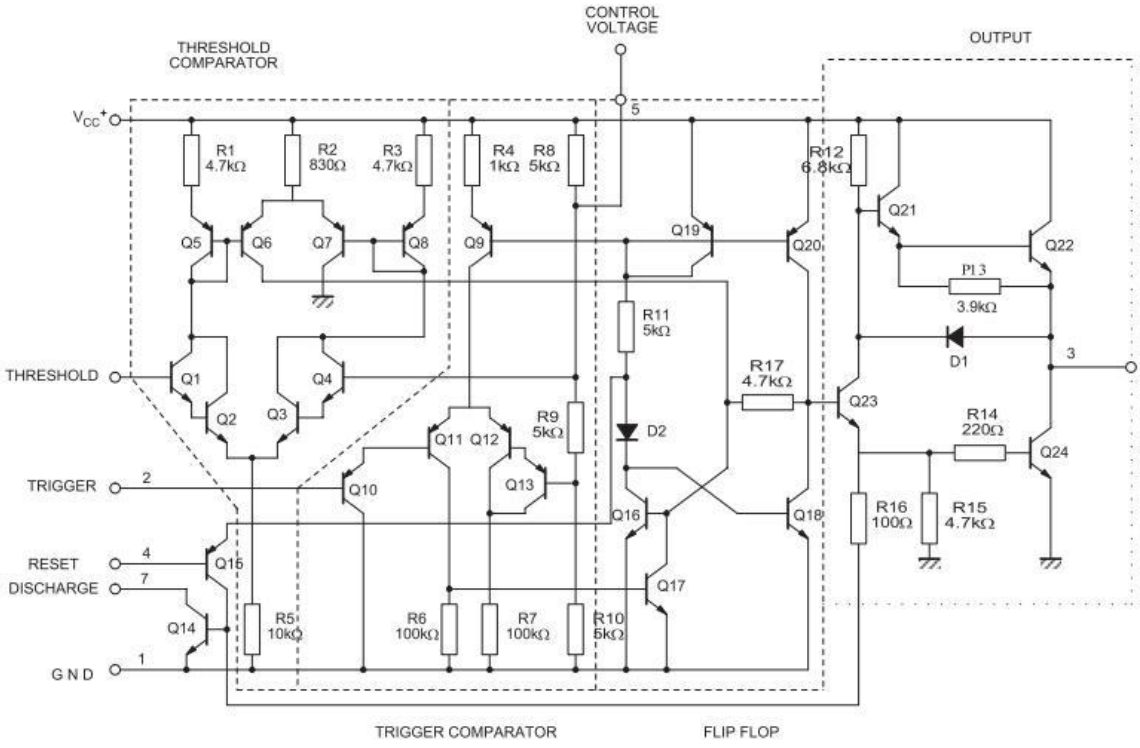
In the standby or stable state, the output $\overline{Q}$ of the control flip-flop (F/F) is HIGH. This make the output LOW as the power amplifier is basically an inverter. A negative going trigger pulse is applied to PIN 2 and should have its DC level greater than the threshold level of the lower comparator i.e. 1/3 V_{CC}. At the negative going edge of the trigger, as the trigger passes

through $V_{CC}/3$, the output of the lower comparator goes HIGH and sets F/F (Q = 1). During each positive excursion, when the threshold voltage at PIN 6 passes through 2/3 V_{CC}, the output of the upper comparator goes HIGH and resets the F/F (Q = 0).

The reset input (PIN 4) provides a mechanism to reset the F/F in a manner which overrides the effect of any instruction coming to F/F from lower comparator. This overriding reset is very much effective when the reset input is less than 0.4 V. When reset is not used it is returned to V_{CC}. The transistor Q_2 serves as a buffer to isolate the reset input from the F/F and transistor Q_1. The transistor Q_2 is driven by an internal reference voltage V_{ref} obtained from supply voltage V_{CC}.



(a)



(b)

Fig. 3: (a) Functional block diagram of NE-555 timer; (b) complete internal circuit diagram of NE-555 timer. Note the presence of three 5 kΩ resistor as potential divider circuits which is reason for the name 555.

Part IV: Operation of NE-555 as Astable Multivibrator

As shown in Figure 4, adding a second resistor, R_B, and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multi-vibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B. This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \times V_{CC}$) and the trigger-voltage level ($\approx 0.33 \times V_{CC}$).

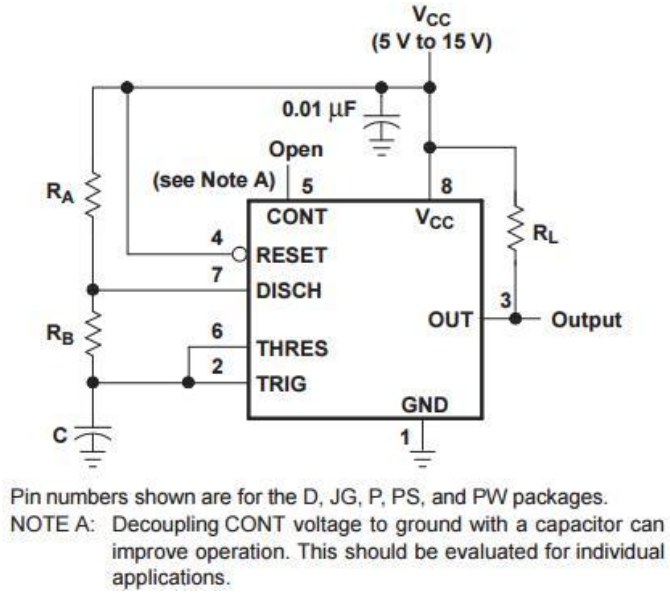


Fig 4: Circuit of astable multivibrator.

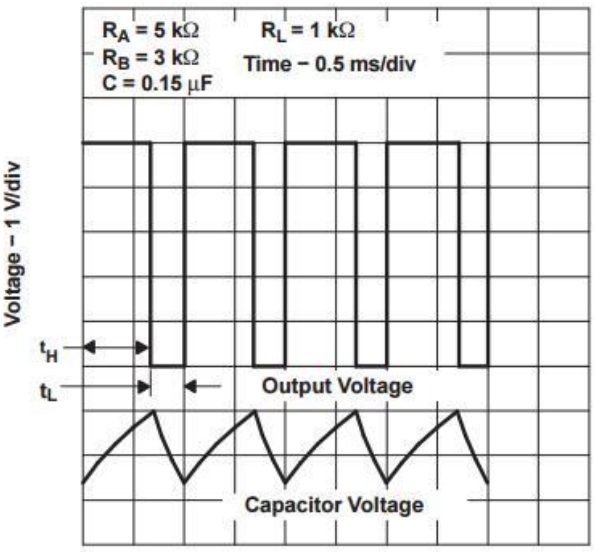


Fig. 5: Output waveforms during astable operation.

Fig. 5 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L can be calculated as follows:

$$\begin{cases} t_H = 0.693(R_A + R_B)C \\ t_L = 0.693R_B C \end{cases}$$

Other useful relations in this mode are,

Time Period: $t = 0.693(R_A + 2R_B)C$

Frequency: $f = \dfrac{1.44}{(R_A + 2R_B)C}$

Output waveform duty cycle: $D = 1 - \dfrac{R_B}{R_A + R_R}$

Part V: Operation of NE-555 as FM Generator

The 555 is wired as a normal astable multivibrator with constant on-off time period (**Refer Fig. 6**). The only difference in this modulator circuit is that the pin number 5 is not connected to the positive via a capacitor, but it is used to receive the modulating signal. The pin number 4, which is the reset pin, is connected to the V_{CC}. The pin 2 which is the trigger pin and the pin 6 which is the threshold pin is shorted together and a capacitor is connected across this point and the ground. This capacitor charges towards V_{CC} through the diode 'D' and the resistor 'R1' and discharges from the pin 7 through the resistor 'R2'. The charging time depends on the value of the capacitor and the value of the resistor 'R1' and the discharging time depends on the value of the capacitor and the value of the resistor 'R2'. The on-off time period of the output pulse depends on the charging and the discharging time of the capacitor. Since in this circuit the R1 and R2 has the same value the charging and discharging time is same and also the on-off time period of the output pulse are same.

As the amplitude variations occurs in the baseband signal, the frequency generated by the 555 (carrier) changes and hence a frequency modulated wave is obtained at the output of the 555 IC (**Refer Fig. 6**). As the amplitude increase the frequency decreases and vice versa. For large amplitude signals the frequency variation will be large and for small amplitude signals the frequency variations will be small.

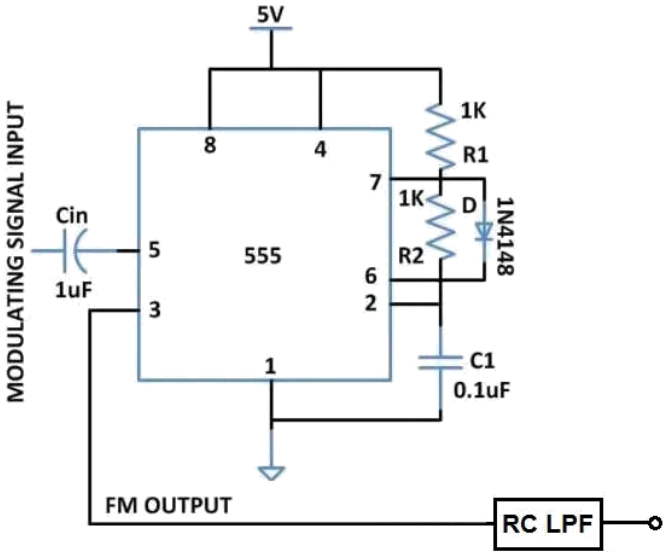


Fig. 6: Experimental setup for generating FM signal. **Use R_1 and R_2 and C by your own calculation to achieve the free running signal frequency in the range of ~ 100 KHz. This is required in order to successfully demodulate using PLL IC. Use design formulas as described earlier in astable multivibrator section.**

Part VI: Demodulation using LM-565 PLL IC

The LM565 and LM565C are general purpose phase locked loops containing a stable, highly linear voltage controlled oscillator for low distortion FM demodulation, and a double balanced phase detector with good carrier suppression. The VCO frequency is set with an external resistor and capacitor, and a tuning range of 10:1 can be obtained with the same capacitor.

The major design parameters of PLL circuit are listed below.

Free running frequency: $f_0 \cong \frac{0.3}{R_0 C_0}$; Hold in range of the PLL is $f_H \cong \pm \frac{8 f_0}{V_C}$

where, V_C is total supply voltage to the circuit and R_0 (Pin 8) and C_0 are timing resistor and capacitor (Pin 9).

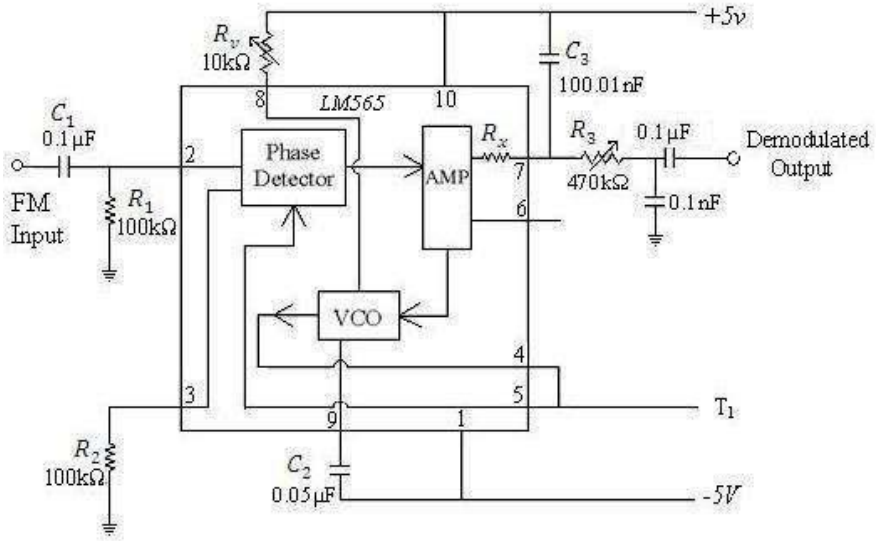


Fig. 7: LM 565 PLL used as FM demodulator circuit.

Operation of PLL Demodulator Circuit

The input FM signal (V_i) is applied to the PIN 2 through a coupling capacitor C_C. A part of this signal is also applied to the PIN 3 through the potential divider network, consisting of R_2, R_3 and R_4. The DC power supply is also provided to PIN 2 and PIN 3 through R_1 from $+V_{CC}$ supply. The capacitor C_2 is used to filter out an AC ripple if present in the DC supply. The demodulated FM signal is nothing but the control signal which is available at PIN 7. Thus the signal available at PIN 7 is the original baseband signal. Check this signal with the original baseband signal used in the FM modulator part. **Note that the free running frequency of the PLL should be near to the carrier frequency in the FM modulator part. It should also be noted that for successful demodulation of FM signal PLL should be in locked state. One can adjust the free running frequency of PLL IC by adjusting R_0 and C_0 as described earlier.**

RESULTS

Table 1: Calculation of frequency deviation of FM modulated signal.

Serial Number	Message signal frequency (Hz)	Message Signal Amplitude (V)	Modulated Signal Amplitude (V)	Frequency Deviation (Hz)	Modulation Index
1					
2					
3					
4					
5					

Trace: Trace the output waveform at (a) Pin 3 of 555 timer
(b) After LPF section of PIN-3 of 555 timer
(c) Demodulated output.

REFERENCES

1. B. P. Lathi and Zhi Ding, Modern Digital and Analog Communication Systems, Fourth Edition, Oxford University Press.
2. H. Taub and D. Schilling, *Principles of Communication Systems*, 2nd Edition, TMH.
3. Datasheet of NE-555.
4. Datasheet of LM-565.