Common source Characteristic

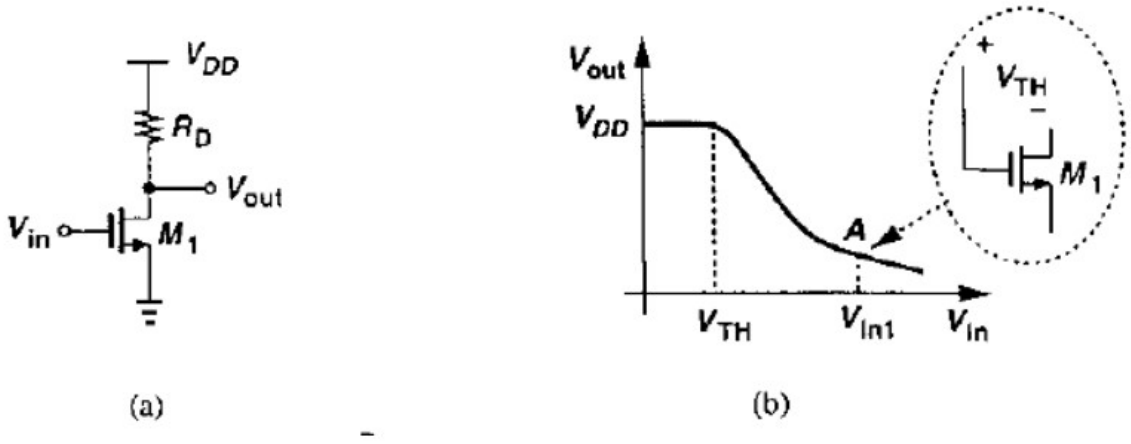
AIM :

To design and plot characteristic of common source amplifier with resistive load , Nmos load and Pmos load

THEORY:

Mosfet is the voltage controlled current source which convert change in its gate source voltage to small signal drain current which can pass through resistor to generate an output voltage

Figure below shows such operation



The input impedence of the circuit is very high at low frequencies.

If the input voltage increases from zero, M1 is off and Vout = Vdd as shown in figure (b). As Vin approaches Vth, M1 begins to turn on, drawing current from Rd and lowering Vout. If Vdd is not excessively low, M1 turns on in saturation and we have

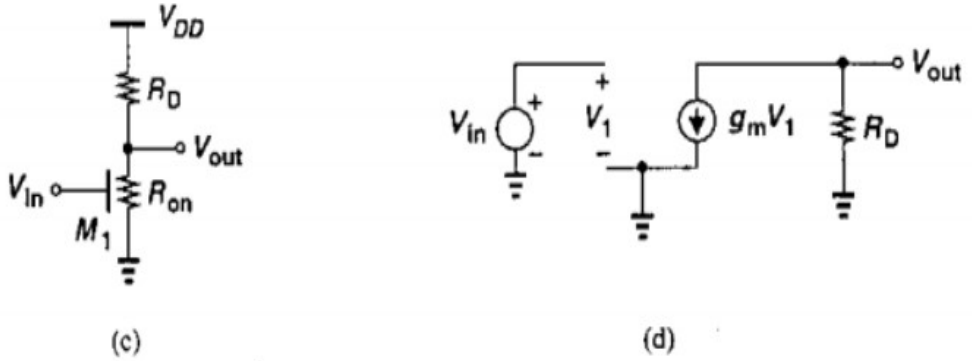
$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{0X} \frac{W}{L} (V_{in} - V_{TH})^2$$

where channel length modulation is neglected. With furthur increase in Vin, Vout drops more and the transistor continues to operate in saturation until Vin exceeds Vout by Vth. At this point,

$$V_{in1} - V_{TH} = V_{DD} - R_D \frac{1}{2} \mu_n C_{0X} \frac{W}{L} (V_{in1} - V_{TH})^2$$

from which Vin1 - Vth and hence Vout can be calculated. For Vin > Vin1, M1 is in the triode region:

$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [2(V_{in} - V_{TH}) V_{out} - V_{out}^2]$$



If Vin is high enough to drive M1 into deep triode region , vout << 2(vin-vth) , and from the equivalent circuit

$$V_{out} = V_{DD} \frac{R_{on}}{R_{on} + R_D} = \frac{V_{DD}}{1 + \mu_x C_{ox} \frac{W}{L} R_D (V_{in} - V_{TH})}$$

Since the transconductance drops in the triode region we usually ensure that Vout > vin – vth and hence the circuit operates to the left point of A and from the input output characteristic and viewing the slope as small signal gain

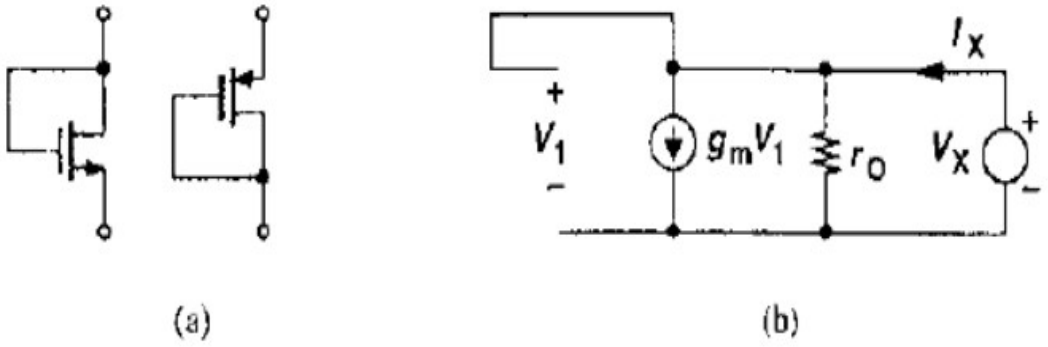
$$A_v = \frac{\partial V_{out}}{\partial V_{in}} = -R_D \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH}) = -g_m R_D$$

Even though the gain is derived but the equation predicts certain effects as gm varies itself with the input signal and gain of the circuit changes subsequently with the signal swing , the dependance of gain on the signal leads to various non linearity which is an undesirable effect.

Common source stage with diode connected load

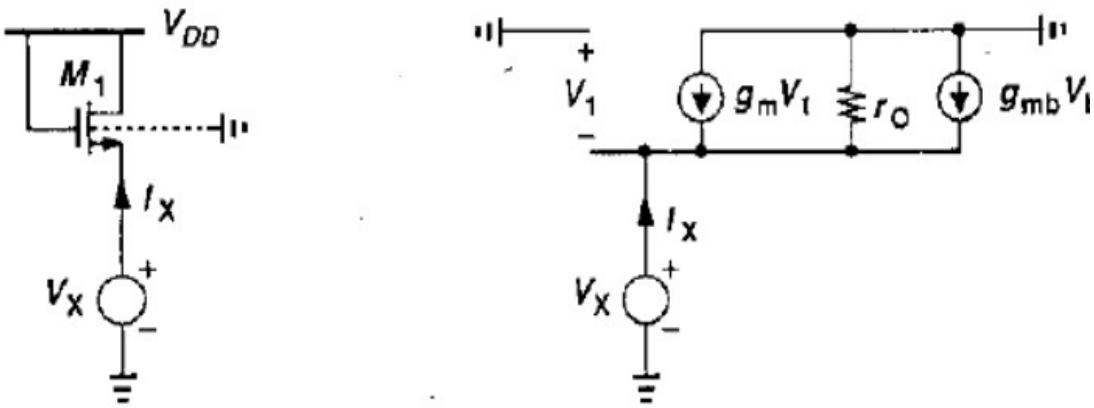
In some CMOS technology it is difficult to fabricate resistor with specific values consequently it is desirable to replace resistor with MOS transistor

A MOSFET can operate as a small signal resistor if its gate and drain are shorted which is called diode connected load in a small signal behavior it acts as a 2 terminal resistor , in this configuration transistor always operates in the saturation region because gate and drain are in same potential



(a) (b)

Using the small signal equivalent to obtain the Impedence of the device



(a) (b)

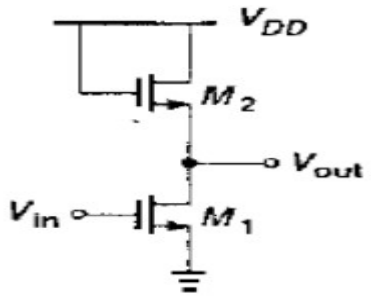
Impedence looking from the source terminal is

$$\frac{V_x}{I_x} = \frac{1}{g_m + g_{mb} + r_0^{-}1}$$

$$= \frac{1}{g_m + g_{mb}} || r_0$$

$$\approx \frac{1}{g_m + g_{mb}}$$

Now applying this diode connected load configuration in the common source stage as a load an calculating the small signal gain



For negligible channel length modulation the voltage gain can be calculated as considering MOS transistor to behave as a two terminal resistor and acting as a load to the common source stage

$$A_v = -g_{m1}\frac{1}{g_{m2}+g_{mb2}}$$

$$= -\frac{g_{m1}}{(g_{m2})(1+\eta)}$$

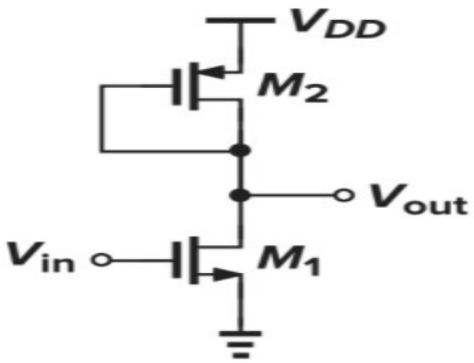
$$\text{where } \eta = \frac{g_{mb2}}{g_{m2}}$$

Now expressing gm1 and gm2 in terms of device dimension and bias current we have

$$A_p = -\sqrt{\frac{(\frac{W}{L})_1}{(\frac{W}{L})_2}}\frac{1}{(1+\eta)}$$

Now this gain equation is independent of bias current and voltage which is non linearity in resistive connected load

The diode connected load can be PMOS load as well



Where voltage gain is calculated as

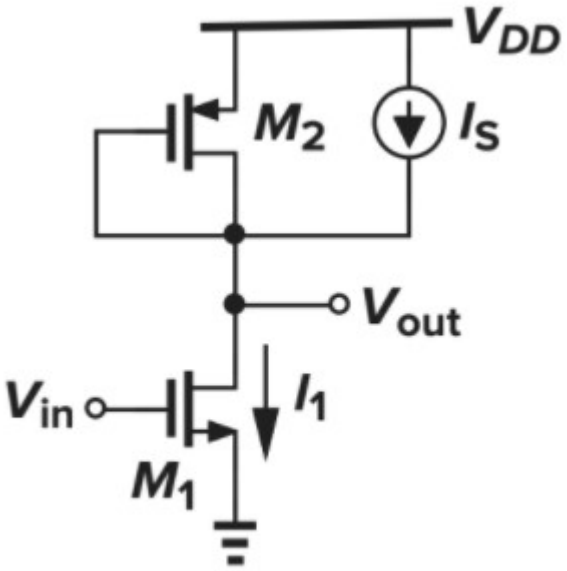
Id1 = |Id2|

$$\mu_n \left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH1})^2 = \mu_p \left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH2})^2$$

So voltage gain is

$$\frac{|V_{GS2} - V_{TH2}|}{V_{GS1} - V_{TH1}} = A_v$$

We can further increase the gain of the NMOS Load and PMOS Load configuration using the DC current source across the load like

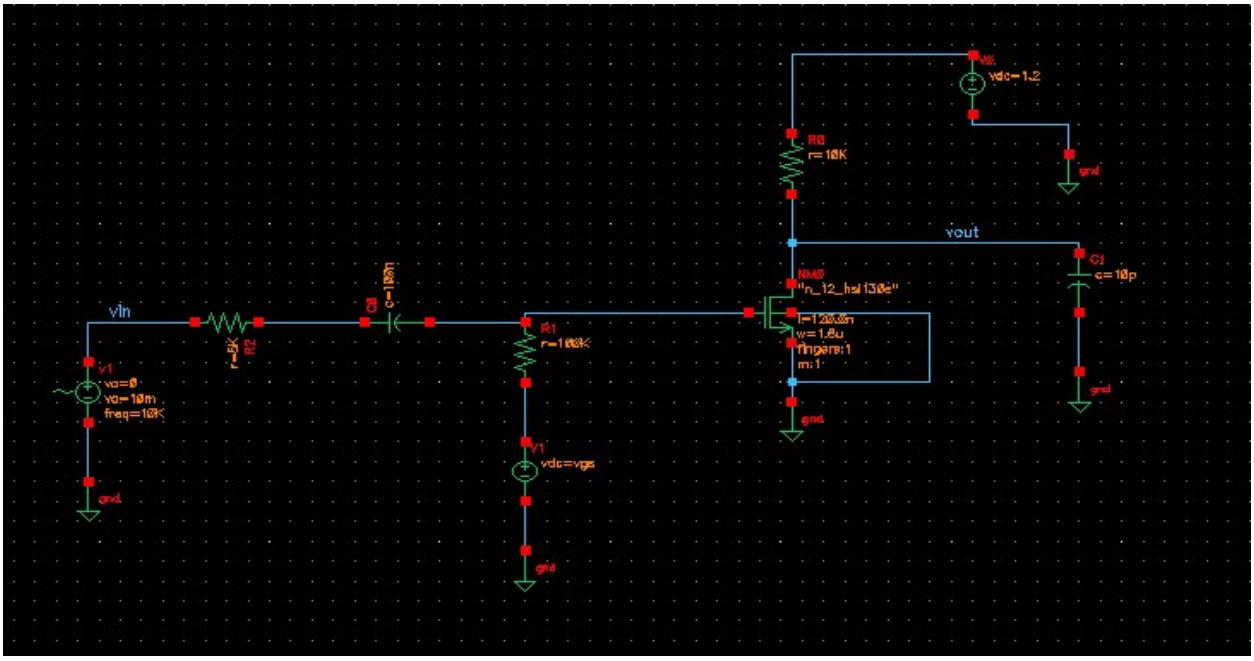


Design Procedure:

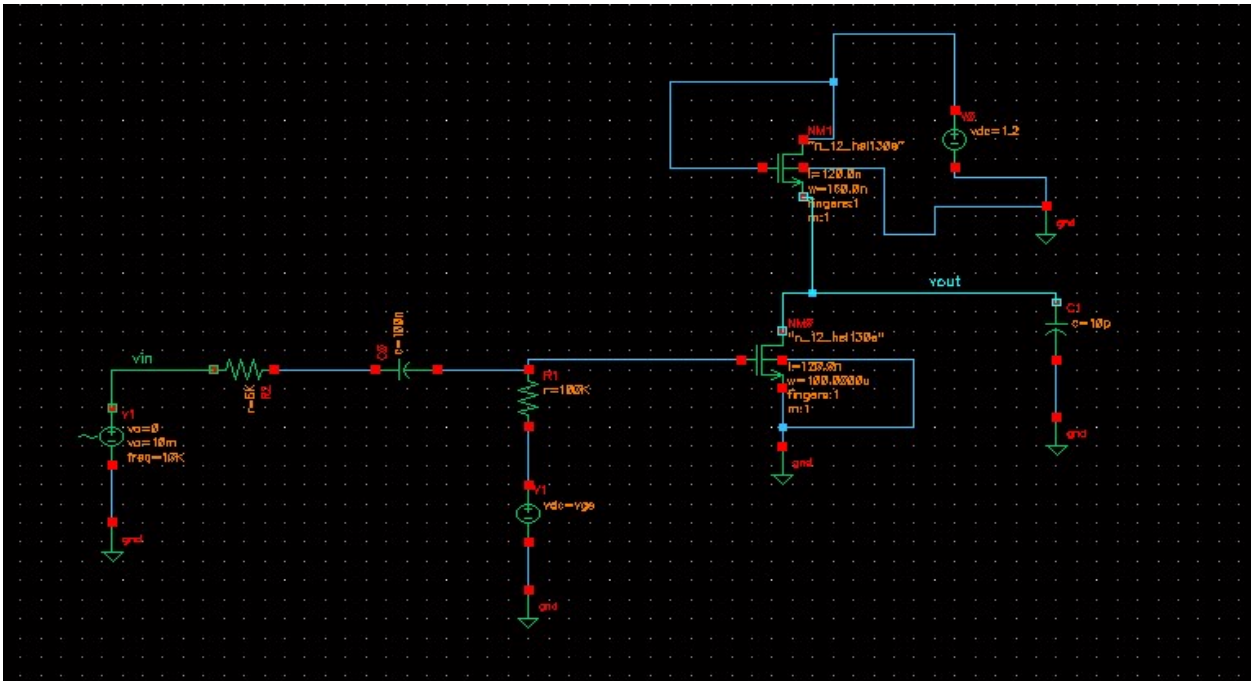
1. First we have created a new library of our own with which we want to create an Common source amplifier
2. After that we created a cell view of an CS in the schematic
3. After creating the given schematic we first do DC analysis to fix the bias voltage that is Vgs which is to be fixed at vdd/2
4. After fixing bias voltage AC analysis is performed to find gain and Bandwidth
5. Then Transient analysis for viewing output of the amplifier
6. Same steps are repeated for NMOS and PMOS load

Circuit Schematic:

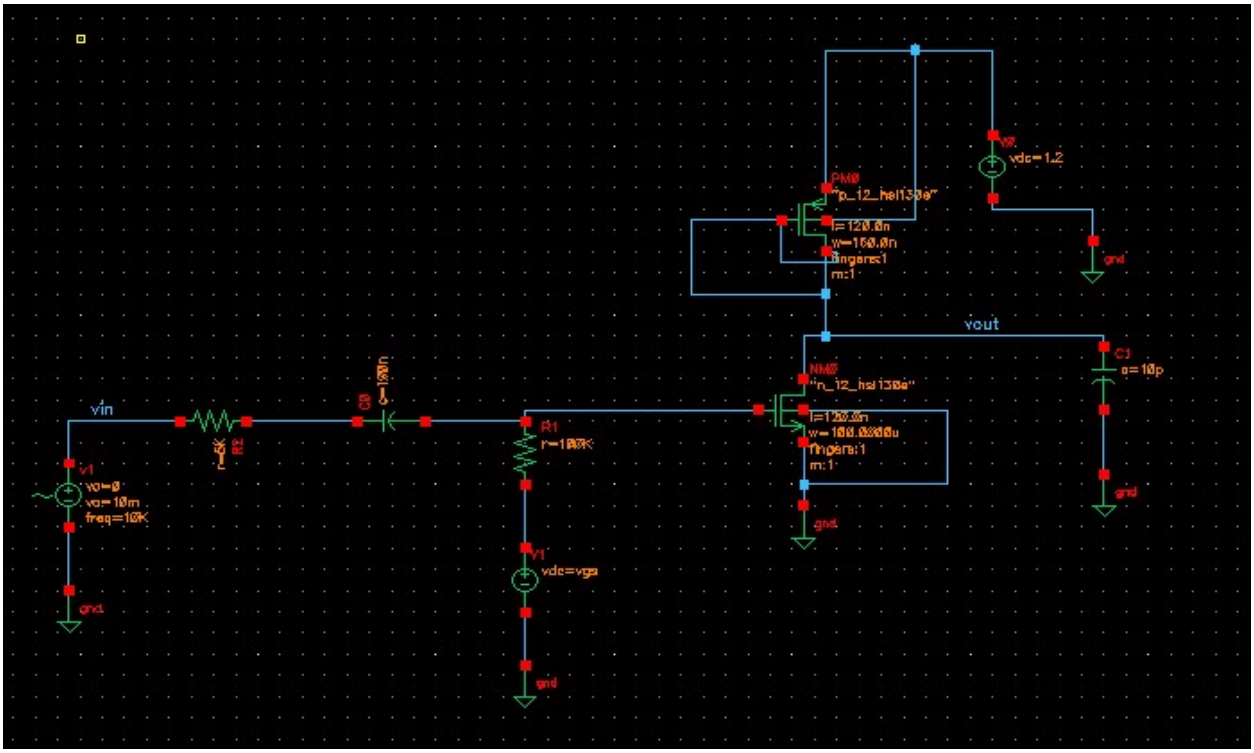
Resistive Load



Nmos diode connected load



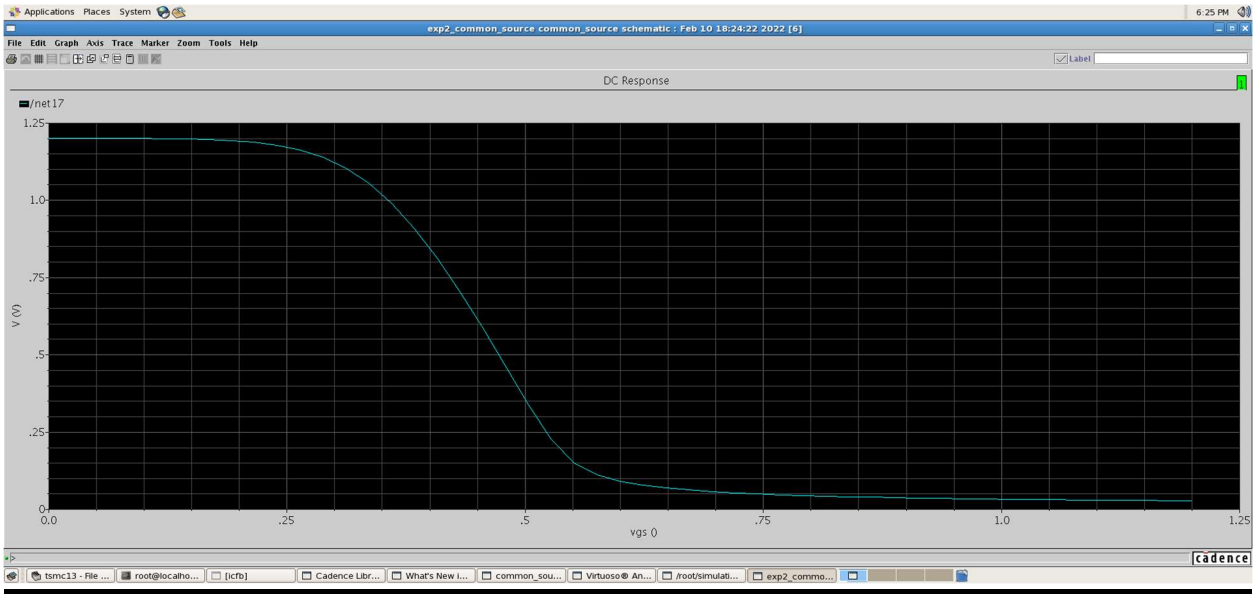
Pmos diode connected load



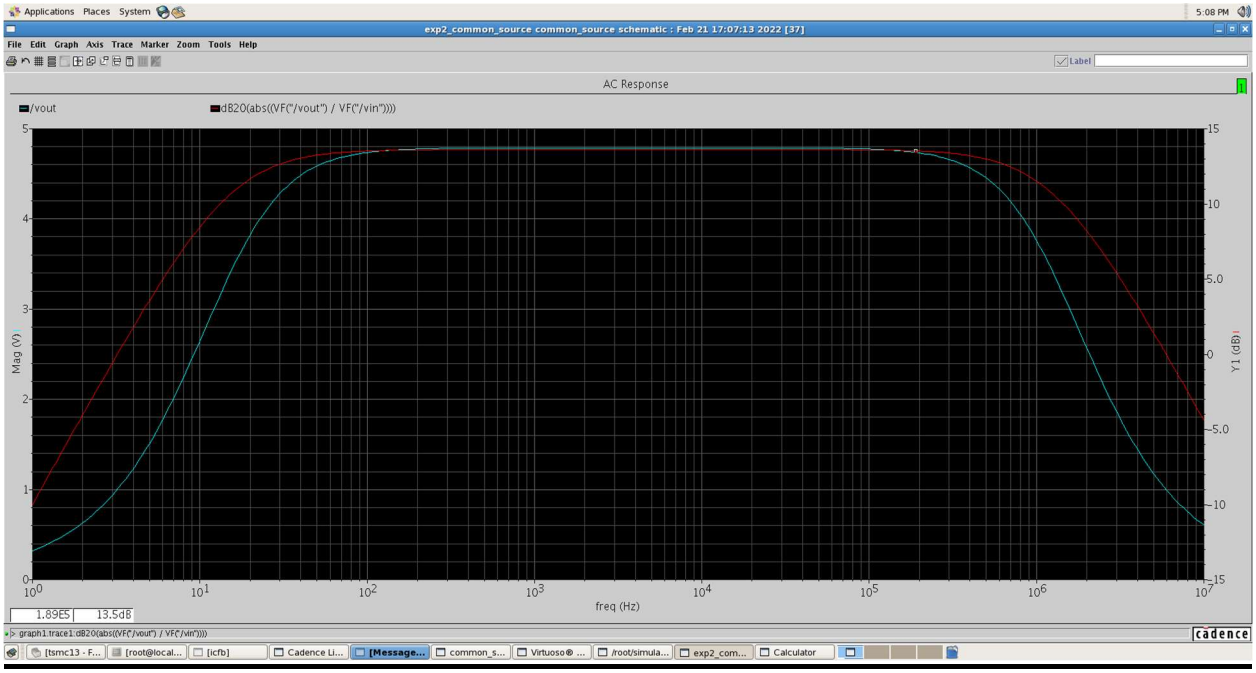
Result of Simulation

Resistive load

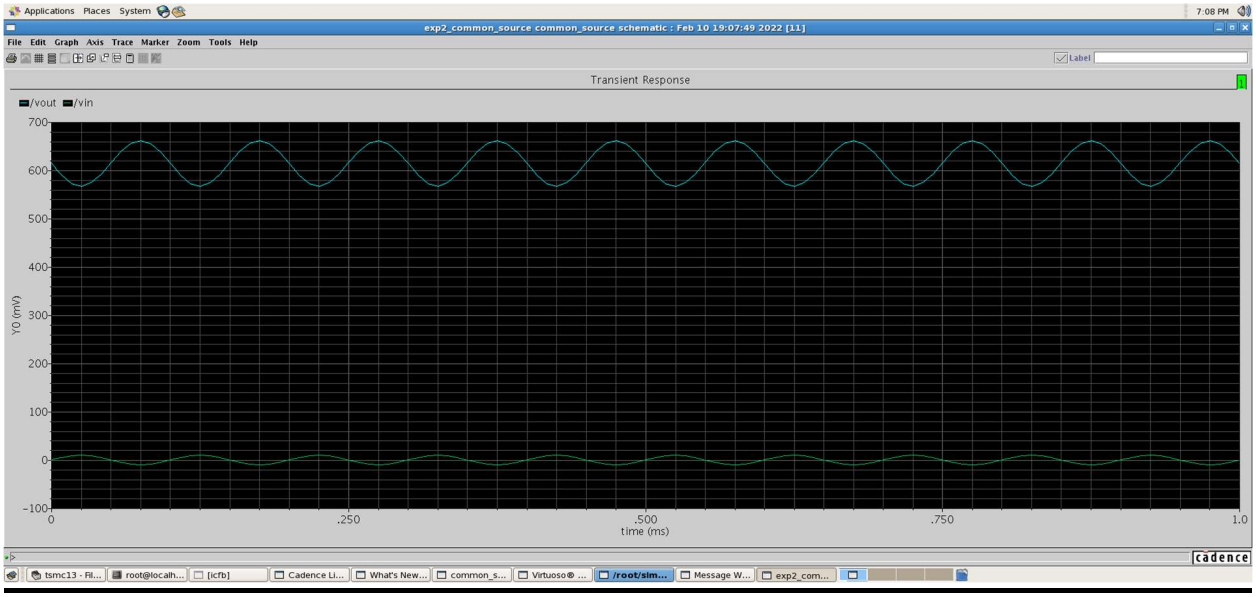
DC analysis



Ac analysis

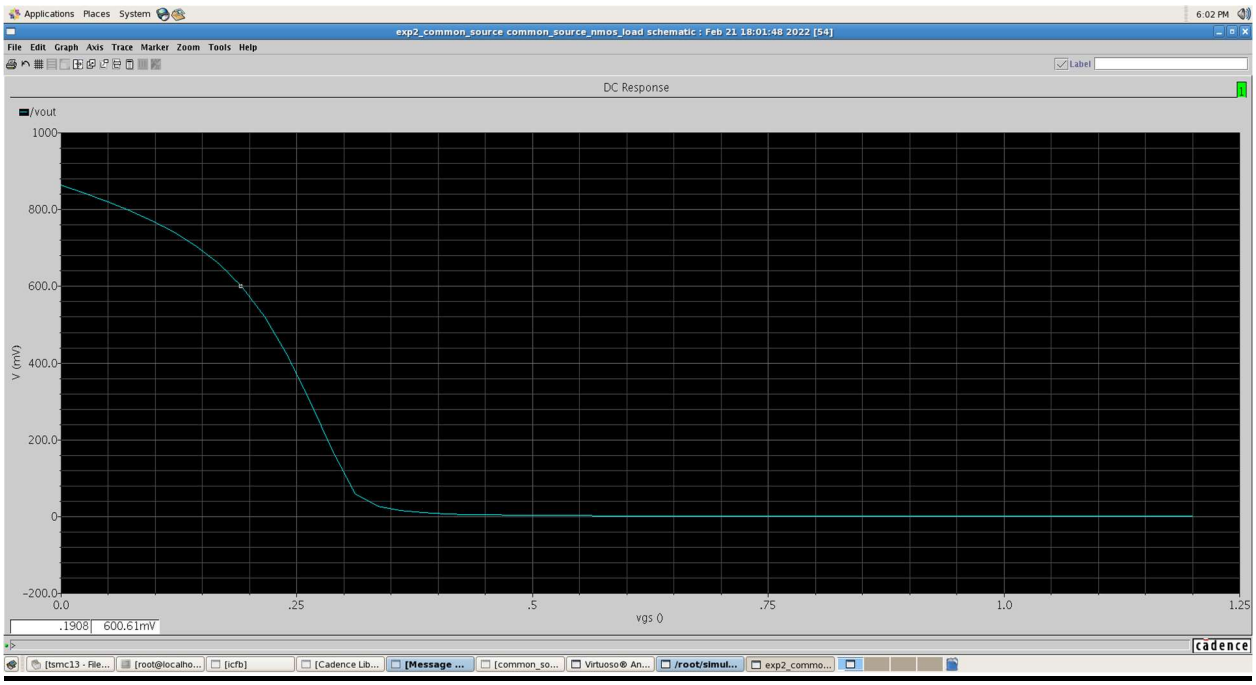


Transient analysis

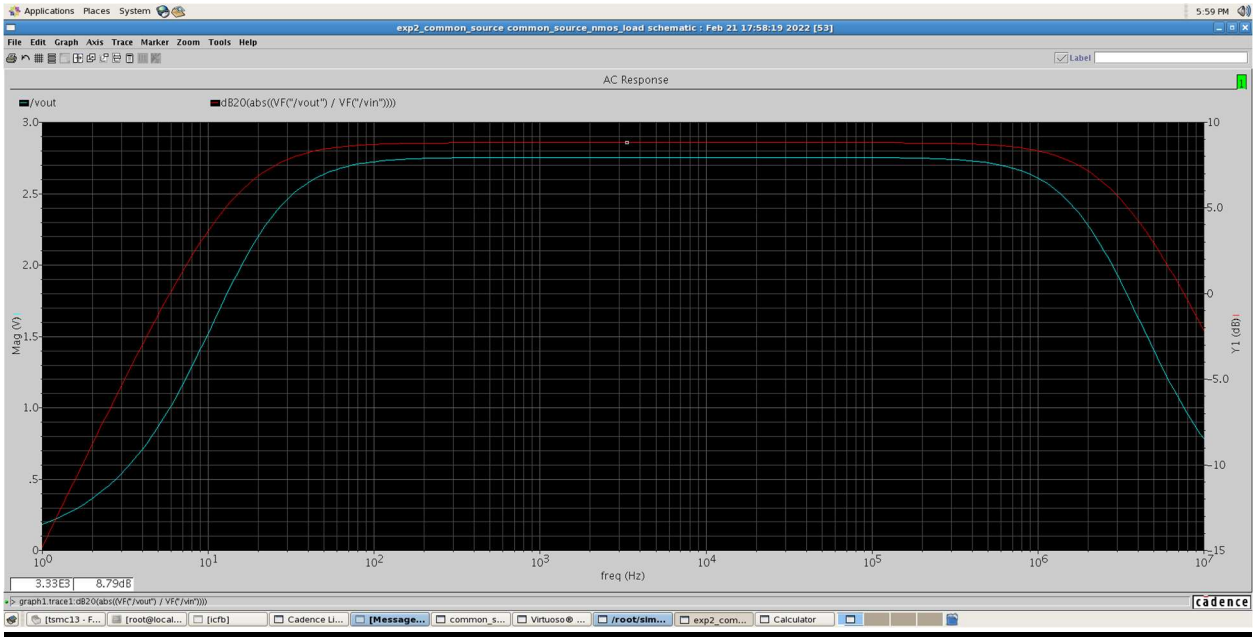


Nmos Diode connected load

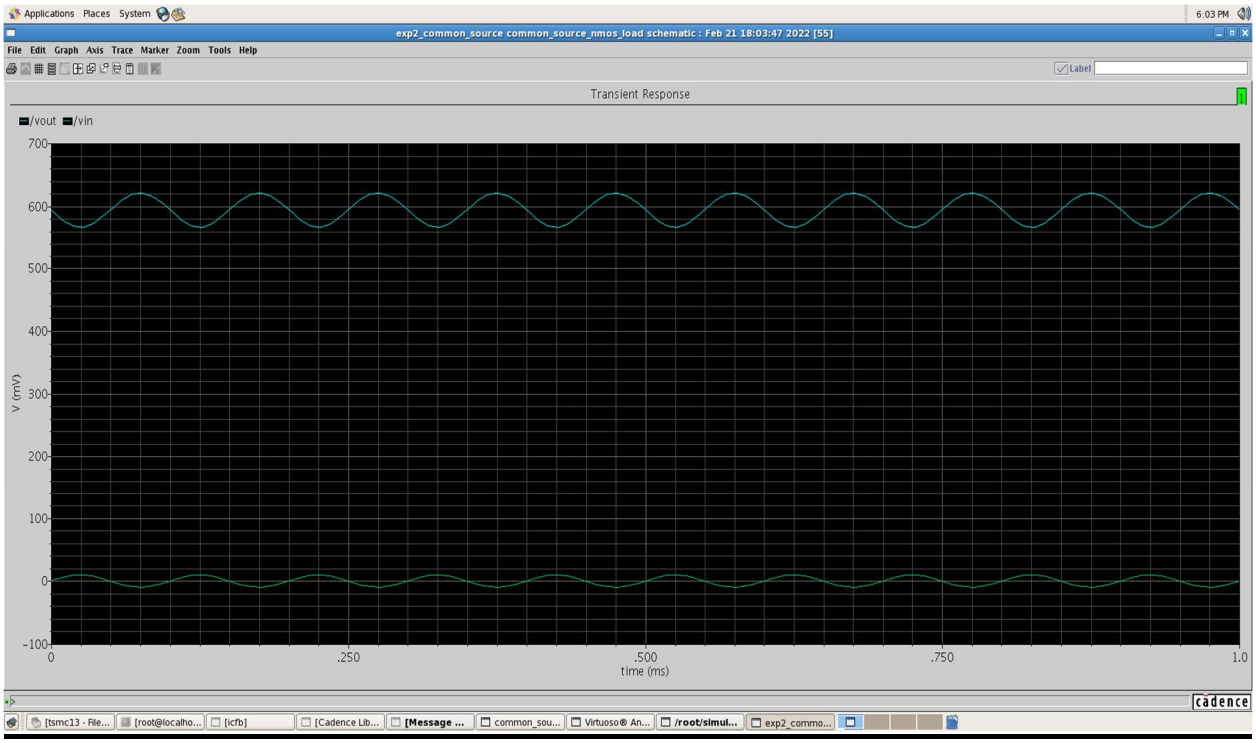
Dc analysis



AC analysis

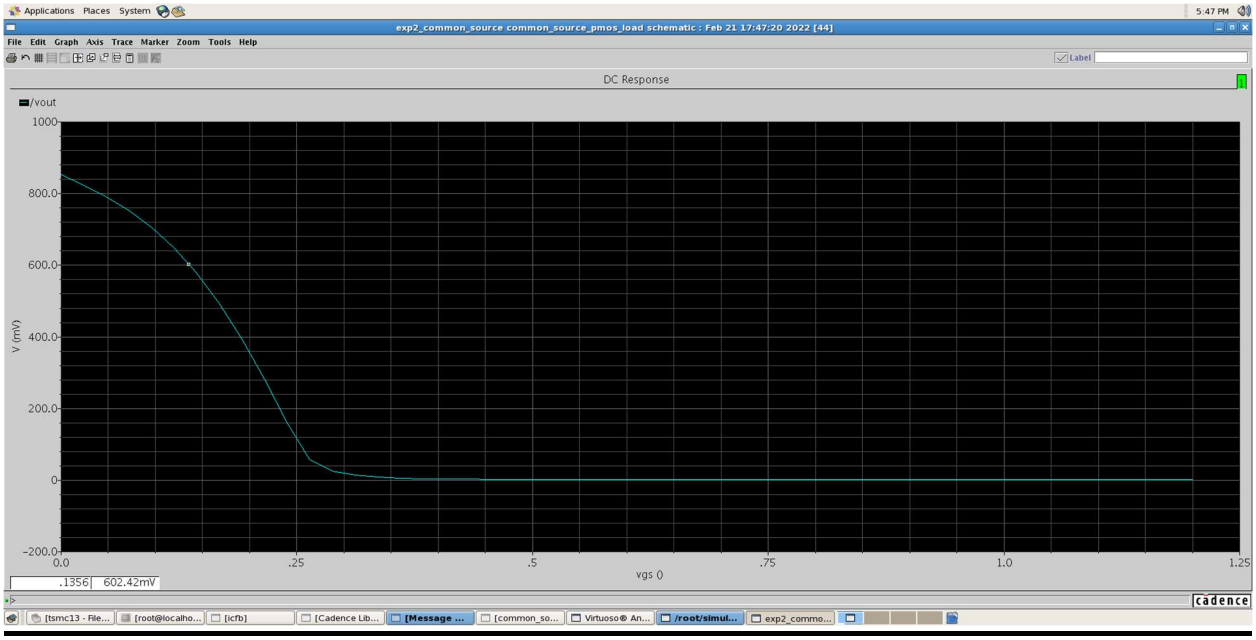


Transient analysis

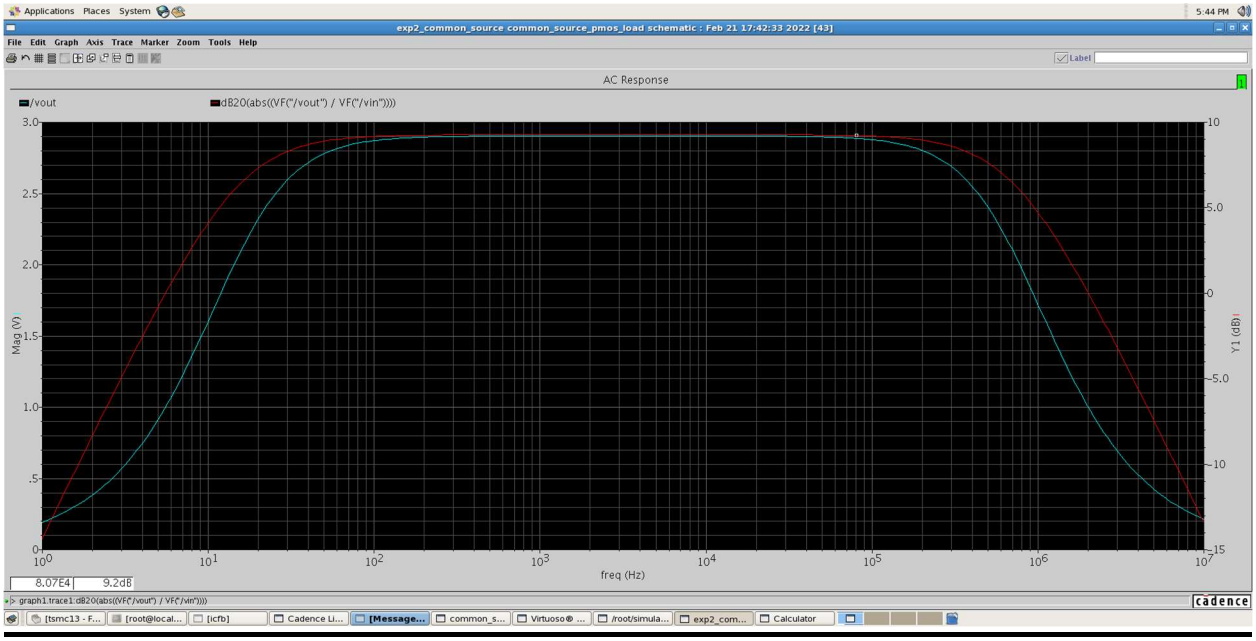


Pmos Diode Connected load

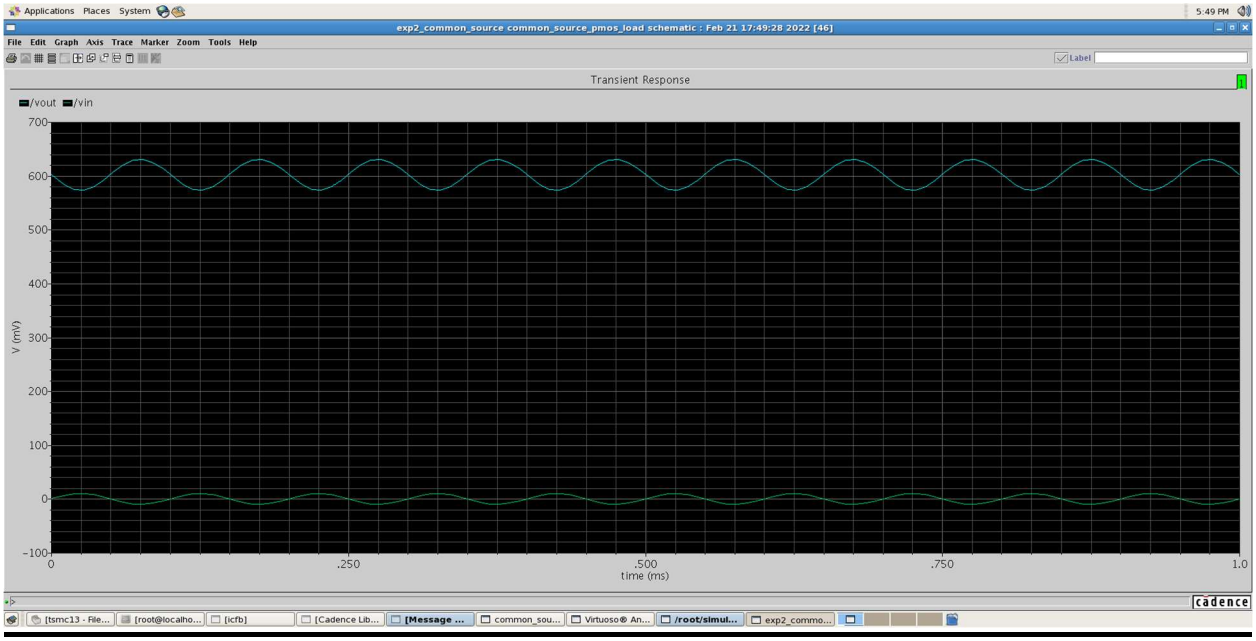
DC analysis



AC analysis



Transient analysis



Calculation

Given Id = 60 ua

Vdd = 1.2v

Vds = 0.6v

And Av = 5

From the circuit

Rd = vdd-vds / Id

Rd = 10K

And Av = 5

|gmRD| = 5

Gm = 500us

Now calculating **W** from the Gm equation in the saturation region

Which comes is **1.6u** taking length as 120nm

And Vgs can be calculated from the equation

Vgs = 2Id/gm + vthn

Vgs = 460mv

Inference

1. Resistive load gain comes dependent on the input parameter so non ideality came which is undesirable
2. Using NMOS and PMOS load gain become independent of input parameter which is desirable and non ideality is reduced
3. Pmos load is better as compared to nmos load because body effect is not there in pmos load which is decreasing the gain