Aman Butoliya

DSP Algorithm Acceleration Engineer

SIMD Optimization | Memory Hierarchy | Vision and Perception

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Professional Summary

Embedded DSP systems engineer with 2.5 years of industry experience accelerating vision and perception algorithms on constrained DSP architectures. Specialized in translating OpenCV and PCL style C++ logic into deterministic C implementations, SIMD optimized kernel design, and frame level DMA orchestration under tight on-chip DSP memory limits. Experienced in performance bottleneck analysis, regression testing, and customer facing issue resolution. Familiar with system safety methodologies and standards such as ISO 26262, contributing to reliable and safety-compliant solutions.

Education

Indian Institute of Technology, Bombay, M. Tech in Electrical Engineering — Aug 2020 – May 2023

- **Coursework: DSP**, **Image Processing**, **Computer Vision**, and Machine Learning | **CGPA - 8.7**

Industry Experience

Design Engineer II, Cadence Design Systems – Pune, India — July 2023 – Present

- **Stereo Rectification**
  - Implemented a Levenberg–Marquardt based stereo rectification pipeline on DSPs, enforcing deterministic numeric behavior and a unique minimal-rotation solution suitable for production stereo workloads
  - Optimized compute-intensive stages using SIMD intrinsics, achieving approximately 150× cycle reduction
  - Orchestrated frame-level execution using ping-pong DMA (Direct Memory Access) buffering to overlap compute and data movement, sustaining high throughput under tight on-chip DSP memory limits
- **Radar SLAM – Inlier-Only ICP**
  - Designed and implemented an Inlier-Only ICP based radar SLAM pipeline in C to improve pose estimation robustness for sparse radar point clouds with high outlier rates encountered in real deployments
  - Improved convergence by introducing dynamic inlier–outlier classification within the ICP loop, outperforming standard ICP on real-world radar datasets across diverse operating conditions
  - Optimized DSP execution by mapping core ICP stages to tile-level kernels and orchestrating frame-level execution using ping-pong DMA buffering under strict on-chip memory limits
- **Image Stitching**
  - Accelerated bundle adjustment and brightness adjustment in a panoramic image stitching pipeline using SIMD optimization and ping-pong-pang DMA buffering to overlap multi-stage compute and data movement
  - Ensured deterministic output by maintaining bit-exact floating-point and fixed-point implementations to match SIMD behavior across planar, cylindrical, and spherical modes for stable regression and reproducible validation
  - Achieved scalable performance, processing up to 20 images per panorama with 38M–247M cycle execution
- **Production Ownership**
  - Supported customer-reported failures by debugging real-world datasets, resolved QA-identified issues, and established Jenkins-based regression to preserve correctness and performance across release cycles

Publications

New Features for the Detection of Fetal QRS Complexes in Non-Invasive Fetal ECG — Dec 2023
ieeexplore.ieee.org/document/10340399

Deep Learning with Sparse Representations for Biomedical Signals — July 2023
ieeexplore.ieee.org/document/10167363

LEADERSHIP AND AWARDS

- Contributed in the development of course material and lab manual for the UG and PG **SrijaTI TI-DSP** lab courses
- Bagged second runner up position at institute level in entrepreneurship competition - **Hult Prize IITB**

Technologies

Languages: Embedded C, C++, Python for tooling
Processors Programmed: Tensillica's V230, V240, V331, V341, VP6 (**SIMD**, VLIW, Vectorization)
Expertise: SIMD vectorization, IVP intrinsics, DMA orchestration, performance profiling, deterministic numeric behavior