1.   The subnet mask for a particular network is 255.255.31.0 Which of the
     following pairs of IP addresses could belong to this network?
     a   172.57.88.62 and 172.56.87.23
     b   10.35.28.2 and 10.35.29.4
     c   191.203.31.87 and 191.234.31.88
     d   128.8.129.43 and 128.8.161.55

2.   In networking, UTP stands for
     a   Unshielded T-connector port
     b   Unshielded twisted pair
     c   Unshielded terminating pair
     d   Universal transmission process

3.   The address resolution protocol (ARP) is used for
     a   Finding the IP address from the DNS
     b   Finding the IP address of the default gateway
     c   Finding the IP address that corresponds to a MAC address
     d   Finding the MAC address that corresponds to an IP address

4.   Which of the following is a MAC address?
     a   192.166.200.50
     b   00056A:01A5CCA7FF60
     c   568, Airport Road
     d   01:A5:BB:A7:FF:60

5.   What is the primary purpose of a VLAN?
     a   Demonstrating the proper layout for a network
     b   Simulating a network
     c   To create a virtual private network
     d   Segmenting a network inside a switch or device

6.   SHA-1 is a
     a   Encryption algorithm
     b   Decryption algorithm
     c   Key exchange algorithm
     d   Message digest function.

7.   Advanced Encryption Standard (AES) is based on
     a   Asymmetric key algorithm
     b   Symmetric key algorithm
     c   Public key algorithm
     d   Key exchange

8. The primary purpose of an operating system is
   a To make the most efficient use of the computer hardware
   b To allow people to use the computer
   c To keep systems programmers employed
   d To make computers easier to use

9. Which is the correct definition of a valid process transition in an operating system?
   a Wake up: ready → running
   b Dispatch: ready → running
   c Block: ready → running
   d Timer runout: → ready → blocked

10. The correct matching for the following pairs is
    (A) Disk check   (1) Round robin
    (B) Batch processing   (2) Scan
    (C) Time sharing   (3) LIFO
    (D) Stack operation   (4) FIFO

	A	B	C	D
a	3	4	2	1
b	4	3	2	1
c	3	4	1	2
d	2	4	1	3

11. A page fault
    a Occurs when a program accesses an available page of memory
    b Is an error in a specific page
    c Is a reference to a page belonging to another program
    d Occurs when a program accesses a page not currently in memory

12. Using larger block size in a fixed block size file system leads to
    a Better disk throughput but poorer disk space utilization
    b Better disk throughput and better disk space utilization
    c Poorer disk throughput but better disk space utilization
    d Poorer disk throughput and poorer disk space utilization

13. Which of the following statements about synchronous and asynchronous I/O is NOT true?
   a An ISR is invoked on completion of I/O in synchronous I/O but not in asynchronous I/O
   b In both synchronous and asynchronous I/O an ISR (Interrupt Service Routine)is invoked after completion of the I/O
   c A process making a synchronous I/O call waits until I/O is complete, but a process making an asynchronous I/O call does not wait for completion of the I/O
   d In the case of synchronous I/O, the process waiting for the completion of I/O is woken up by the ISR that is invoked after the completion of I/O

14. Consider three CPU-intensive processes, which require 10,20 and 30 time units and arrive at times 0,2, and 6, respectively. How many context switches are needed if the operating system implements a shortest remaining time first scheduling algorithm? Do not count the context switches at time zero and at the end
   a 1
   b 2
   c 3
   d 4

15. The performance of Round Robin algorithm depends heavily on
   a Size of the process
   b The I/O bursts of the process
   c The CPU bursts of the process
   d The size of the time quantum

16. Consider a system having "n" resources of same type. These resources are shared by 3 processes A, B, C. These have peak demands of 3, 4 and 6 respectively. For what value of "n" deadlock won't occur
   a 15
   b 9
   c 10
   d 13

17. Consider a set of 5 processes whose arrival time, CPU time needed and the priority are given below

Process Priority	Arrival Time (in ms)	CPU Time Needed (in ms)	Priority
P1	0	10	5
P2	0	5	2
P3	2	3	1
P4	5	20	4
P5	10	2	3

(Smaller the number, higher the priority.)
If the CPU scheduling policy is priority scheduling without pre-emption, the average waiting time will be
a   12.8 ms
b   11.8 ms
c   10.8 ms
d   09.8 ms

18. The range of integers that can be represented by an n-bit 2's complement number system is
a -2^{n-1} to $(2^{n-1}-1)$
b $-(2^{n-1}-1)$ to $(2^{n-1}-1)$
c -2^{n-1} to 2^{n-1}
d $-(2^{n-1}+1)$ to $(2^{n-1}-1)$

19. The switching expression corresponding to $f(A,B,C,D)=\sum(1,4,5,9,11,12)$ is
a   BC'D'+A'C'D+AB'D
b   ABC'+ACD+B'C'D
c   ACD'+A'BC'+AC'D'
d   A'BD+ACD'+BCD'

20. Consider the following boolean function of four variables
$f(w, x, y. z)=\sum(1,3,4,6,9,11,12,14)$, The function is
a   Independent of one variable
b   Independent of two variables
c   Independent of three variables
d   Dependent on all the variables

21. In which addressing mode, the effectives address of the operand is generated by adding a constant value to the content of a register?
a   Absolute mode
b   Indirect mode
c   Immediate mode
d   Index mode

22. A certain microprocessor requires 4.5 microseconds to respond to an interrupt. Assuming that the three interrupts I_1, I_2 and I_3 require the following execution time after the interrupt is recognized :
(i) I_1 requires 25 micro seconds
(ii) I_2 requires 35 microseconds
(iii) I_3 requires 20 microseconds
I_1 has the highest priority and I_3 has the lowest. What is the possible range of time for I_3 to be executed assuming that it may or may not occur simultaneously with other interrupts?
a   24.5 microseconds to 39.5 microseconds
b   24.5 microseconds to 93.5 microseconds
c   4.5 microseconds to 24.5 microseconds
d   29.5 microseconds to 93.5 microseconds

23. The process of organizing the memory into two banks to allow 8- and 16-bit data operation is called
a   Bank switching
b   Indexed mapping
c   Two-way memory interleaving
d   Memory segmentation

24. Suppose the numbers 7, 5, 1, 8, 3, 6, 0, 9, 4, 2 are inserted in that order into an initially empty binary search tree. The binary search tree uses the usual ordering on natural numbers. What is the inorder traversal sequence of the resultant tree?
a   7 5 1 0 3 2 4 6 8 9
b   0 2 4 3 1 6 5 9 8 7
c   0 1 2 3 4 5 6 7 8 9
d   9 8 6 4 2 3 0 1 5 7

25. A data structure is required for storing a set of integers such that each of the following operations can be done in (log n) time, where n is the number of elements in the set.
1. Deletion of the smallest element.
2. Insertion of an element if it is not already present in the set.
Which of the following data structures can be used for this purpose?
a   A heap can be used but not a balanced binary search tree
b   A balanced binary search tree can be used but not a heap
c   Both balanced binary search tree and heap can be used
d   Neither balanced binary search tree nor heap can be used

26. The following numbers are inserted into an empty binary search tree in the given order: 10, 1, 3, 5, 15, 12, 16. What is the height of the binary search tree (the height is the maximum distance of a leaf node from the root)?
   a   2
   b.   3
   c   4
   d   6

27. Assume that the operators +, -, x are left associative and ^ is right associative. The order of precedence (from highest to lowest) is ^, x,+, -. The postfix expression corresponding to the infix expression a + b x c – d ^ e ^ f is
   a   abc x + def ^ ^ -
   b   abc x + de ^ f ^
   c   ab + c x d – e ^ f ^
   d   - + a x bc ^ ^ def

28. The infix expression A + (B – C) * D is correctly represented in prefix notation as
   a   A + B – C * D
   b   + A * – BCD
   c   ABC – D * +
   d   A + BC – D *

29. A one dimensional array A has indices 1…. 75. Each element is a string and takes up three memory words. The array is stored at location 1120 decimal. The starting address of A [49] is
   a   1267
   b   1164
   c   1264
   d   1169

30. The five items: A, B, C, D, and E are pushed in a stack, one after the other starting from A. The stack is popped four times and each element is inserted in a queue. Then two elements are deleted from the queue and pushed back on the stack. Now one item is popped from the stack. The popped item is
   a   A
   b   B
   c   C
   d   D

31. A full binary tree with n leaves contains
    a   n nodes
    b $\log_2 n$ nodes
    c   2n-1
    d 2^n nodes

32. The expression 1 * 2 ^ 3 * 4 ^ 5 * 6 will be evaluated as
    a 32^{30}
    b 162^{30}
    c   49152
    d   173458

33. The feature in object-oriented programming that allows the same operation to be carried out differently, depending on the object, is
    a   Inheritance
    b   Polymorphism
    c   Overfunctioning
    d   overriding

34. The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields: a micro-operation field of 13 bits, a next address field (X), and a MUX select field (Y). There are 8 status bits in the inputs of the MUX. How many bits are there in the X and Y fields, and what is the size of the control memory in number of words?
    a   10, 3, 1024
    b   8, 5, 256
    c   5, 8, 2048
    d   10, 3, 512

35. A CPU has 24-bit instructions. A program starts at address 300 (in decimal). Which one of the following is a legal program counter (all values in decimal)?
    a   400
    b   500
    c   600
    d   700

36. Consider a disk pack with 16 surfaces, 128 tracks per surface and 256 sectors per track. 512 bytes of data are stores in a bit serial manner in a sector. The capacity of the disk pack and the number of bits required to specify a particular sector in the disk are respectively
   a   256 Mbyte, 19 bits
   b   256 Mbyte, 28 bits
   c   512 Mbyte, 20 bits
   d   64 Gbyte, 28 bits

37. Consider a pipelined processor with the following four stages
   IF: Instruction Fetch
   ID: Instruction Decode and Operand Fetch
   EX: Execute   WB: Write Back
   The IF, ID and WB stages take one clock cycle each to complete the operation. The ADD and SUB instructions need 1 clock cycle and the MUL instruction need 3 clock cycles in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions?

                           ADD R2, R1, R0   R2←R1+R0
                           MUL R4, R3, R2   R4←R3*R2
                           SUB R6, R5, R4   R6←R5-R4
   a   7
   b   8
   c   10
   d   14

38. The use of multiple register windows with overlap causes a reduction in the number of memory accesses for
   1.Function locals and parameters
   2.Register saves and restores
   3.Instruction fetches
   a   1 only
   b   2 only
   c   3 only
   d   1,2 and 3

39. A processor that has carry, overflow and sign flag bits as part of its program status word (PSW)performs addition of the following two 2's complement numbers 01001101 and 11101001. After the execution of this addition operation, the status of the carry, overflow and sign flags, respectively will be
   a   1,1,0
   b   1,0,0
   c   0,1,0
   d   1,0,1

40. The two numbers given below are multiplied using the Booth's algorithm.
Multiplicand : 0101 1010 1110 1110
Multiplier   : 0111 0111 1011 1101
How many additions/Subtractions are required for the multiplication of the above two numbers?
   a   6
   b   8
   c   10
   d   12

41. The addition of 4-bit, two's complement, binary numbers 1101 and 0100 results in
   a   0001 and an overflow
   b   1001 and no overflow
   c   0001 and no overflow
   d   1001 and an overflow

42. Which of the flowing statements about relative addressing mode is FALSE?
   a   It enables reduced instruction size
   b   It allows indexing of array element with same instruction
   c   It enables easy relocation of data
   d   It enables faster address calculation than absolute addressing

43. Substitution of values for names (whose values are constants) is done in
   a   Local optimization
   b   Loop optimization
   c   Constant folding
   d   Strength reduction

44. A root α of equation f(x)=0 can be computed to any degree of accuracy if a 'good' initial approximation x_0 is chosen for which
   a $f(x_0)>0$
   b $f(x_0) f''(x_0)>0$
   c $f(x)_0 f''(x_0)<0$
   d $f''(x_0)>0$

45. Which of the following statement is correct
   a $\Delta(u_k v_k) = u_k \Delta v_k + v_k \Delta u_k$
   b $\Delta(u_k v_k) = u_{k+1}\Delta v_k + V_{k+1} \Delta u_k$
   c $\Delta(u_k v_k) = v_{k+1}\Delta u_k + u_k \Delta v_k$
   d $\Delta(u_k v_k) = u_{k+1}\Delta v_k + v_k \Delta u_k$

46. The shift operator E is defined as
    E $[f(x_i)] = f(x_i+h)$ and $E^{-1}[f(x_i)] = f(x_i-h)$
    Then Δ (forward difference) in terms of E is
    a   E - 1
    b   E
    c $1-E^{-1}$
    d   1-E

47. The formula
    $$\int_{x0}^{xn} y(n)\, dx \simeq h/2\, (y_0 + 2y_1 + \ldots + 2y_{n-1} + y_n)$$
    $$- h/12\, (\nabla y_n - \Delta y_0) - h/24\, (\nabla^2 y_n + \Delta^2 y_0)$$
    $$-19h/720\, (\nabla^3 y_n - \Delta^3 y_0) \ldots\ldots \text{ is called}$$
    a   Simpson rule
    b   Trapezoidal rule
    c   Romberg's rule
    d   Gregory's formula

48. The cubic polynomial y(x) which takes the following values:
    y(0)=1, y(1)=0, y(2)=1 and y(3)=10 is,
    a $x^3 + 2x^2 + 1$
    b $x^3 + 3x^2 - 1$
    c $x^3 + 1$
    d $x^3 - 2x^2 + 1$

49. x = a cos(t), y = b sin(t) is the parametric form of
    a   Ellipse
    b   Hyperbola
    c   Circle
    d   Parabola

50. The value of x at which y is minimum for $y = x^2 - 3x + 1$ is
    a   -3/2
    b   3/2
    c   0
    d   -5/4

51. The formula
    $$P_k = y_0 + k\nabla y_0 + \frac{k(k+1)}{2}\nabla^2 y_0 + \ldots\ldots + \frac{k\ldots(k+n-1)}{n!}$$
    $\nabla^n y_0$ is
    a   Newton's backward formula
    b   Gauss forward formula
    c   Gauss backward formula
    d   Stirling's formula

52. If G is a graph with e edges and n vertices the sum of the degrees of all vertices in G is
   a   e
   b   e/2
   c e^2
   d   2 e

53. Let G be an arbitrary graph with n nodes and k components. If a vertex is removed from G, the number of components in the resultant graph must necessarily lie between.
   a   k and n
   b   k-1 and k+1
   c   k-1 and n-1
   d   k+1 and n-k

54. A graph in which all nodes are of equal degree, is known as
   a   Multigraph
   b   Non regular graph
   c   Regular graph
   d   Complete graph

55. If in a graph G there is one and only one path between every pair of vertices then G is a
   a   Path
   b   Walk
   c   Tree
   d   Circuit.

56. A simple graph (a graph without parallel edge or loops) with n vertices and k components can have at most
   a   n edges
   b   (n-k) edges
   c   (n-k) (n-k+1) edges
   d   (n-k) (n-k+1)/2 edges.

57. Consider the polynomial $p(x) = a_0 + a_1 x + a_2 x^2 + a_3 x^3$, where $a_i \neq 0$, $\forall\, i$. The minimum number of multiplications needed to evaluate p on an input x is
   a   3
   b   4
   c   6
   d   9

58. Consider the following code written in a pass-by-reference language like FORTRAN.

```
Subroutine swap (ix,iy)
             It = ix
L1:          ix = iy
L2:          iy = it
        end
        ia = 3
        ib = 8
        call swap (ia,ib +5)
        print*, ia,ib
        end
```

   S1: The compiler will generate code to allocate a temporary nameless cell, initialize it to 13, and pass the address of the cell to swap
   S2: On execution the code will generate a runtime error on line L1
   S3: On execution the code will generate a runtime error on line L2
   S4: The program will print 13 and 8
   S5: The program will print 13 and -2
        Exactly the following set of statement(s) is correct:
        a   S1 and S2
        b   S1 and S4
        c   S3
        d   S1 and S5

59. A square matrix A is called orthogonal if A'A=
        a   I
        b   A
        c   -A
        d   -I

60. If two adjacent rows of a determinant are interchanged, the value of the determinant
        a   becomes zero
        b   remains unaltered
        c   becomes infinite
        d   becomes negative of its original value.

61. If $\begin{vmatrix} 3 & 3 \\ x & 5 \end{vmatrix}$ =3. then the value of x is
        a   2
        b   3
        c   4
        d   5.

62. If A,B,C, are any three matrices , then A'+B'+C' is equal to
  a   a null matrix
  b   A+B+C
  c   (A+B+C)'
  d   -(A+B+C)

63.
$$\begin{vmatrix} 265 & 240 & 219 \\ 240 & 225 & 198 \\ 219 & 198 & 181 \end{vmatrix} =$$
  a   779
  b   679
  c   0
  d   256

64. Let f(x) be the continuous probability density function of a random variable x. The probability that a $<x \le$ b, is
  a   f(b - a)
  b   f(b) - f(a)
  c $\int_{a}^{b} f(x)dx$

  d $\int_{a}^{b} xf(x)dx$

65. If the mean of a normal frequency distribution of 1000 items is 25 and its standard deviation is 2.5, then its maximum ordinate is
  a $\dfrac{1000}{\sqrt{2\pi}} e^{-25}$
  b $\dfrac{1000}{\sqrt{2\pi}}$
  c $\dfrac{1000}{\sqrt{2\pi}} e^{-2.5}$
  d $\dfrac{400}{\sqrt{2\pi}}$

66. If the pdf of a Poisson distribution is given by
$f(x) = \dfrac{e^{-2} 2^{x}}{x!}$, then its mean is
  a 2^{x}
  b   2
  c   -2
  d   1

67. Activities which ensure that the software that has been built, is traceable to customer requirement is covered as part of
    a Verification
    b Validation
    c Maintenance
    d Modeling

68. A Testing method, which is normally used as the acceptance test for a software system, is
    a Regression Testing
    b Integration Testing
    c Unit Testing
    d System Testing

69. The 'command' used to change contents of one database using the contents of another database by linking them on a common key field is called
    a Replace
    b Join
    c Change
    d Update

70. A locked database file can be
    a Accessed by only one user
    b Modified by users with the correct password
    c Used to hide sensitive information
    d Updated by more than one user

71. Which of the following contains complete record of all activity that affected the contents of a database during a certain period of time?
    a Transaction log
    b Query language
    c Report writer
    d Data manipulation language

72. Purpose of 'Foreign Key' in a table is to ensure
    a Null Integrity
    b Referential Integrity
    c Domain Integrity
    d Null & Domain Integrity

73. Which of the following scenarios may lead to an irrecoverable error in a database system?
   a A transaction writes a data item after it is read by an uncommitted transaction
   b A transaction reads a data item after it is read by an uncommitted transaction
   c A transaction reads a data item after it is written by a committed transaction
   d A transaction reads a data item after it is written by an uncommitted transaction

74. Use of IPSEC in tunnel mode results in
   a IP packet with same header
   b IP packet with new header
   c IP packet without header
   d No changes in IP packet

75. Special software to create a job queue is called a
   a Driver
   b Spooler
   c Interpreter
   d Linkage editor

76. Process is
   a A program in high level language kept on disk
   b Contents of main memory
   c A program in execution
   d A job in secondary memory

77. When a process is rolled back as a result of deadlock the difficulty which arises is
   a Starvation
   b System throughput
   c Low device utilization
   d Cycle stealing

78. On receiving an interrupt from an I/O device, the CPU
   a Halts for a predetermined time
   b Branches off to the interrupt service routine after completion of the current instruction
   c Branches off to the interrupt service routine immediately
   d Hands over control of address bus and data bus to the interrupting device

79.   Compared to CISC processors, RISC processors contain
        a   more register and smaller instruction set
        b   larger instruction set and less registers
        c   less registers and smaller instruction set
        d   more transistor elements

80.   Which of the following is/are true of the auto increment addressing mode?
        1. It is useful in creating self relocating code
        2. If it is included in an instruction set architecture, then an additional ALU
        is required for effective address calculation
        3. The amount of increment depends on the size of the data item accessed
        a   1 only
        b   2 only
        c   3 only
        d   2 and 3 only