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Fang, Xiongfeng; Li, Gen; Wang, Cheng; Li, Lei

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A Reverse-Biased Voltage Controlling Method for Mitigating Arm Overcurrent and Submodule Overvoltage in Hybrid MMCs During DC Faults

Xiongfeng Fang, *Member, IEEE*, Gen Li, *Senior Member, IEEE*, Cheng Wang, *Member, IEEE*, Lei Li, *Member, IEEE*

Abstract- **Blocking all submodules (SMs) of the hybrid modular multilevel converter is a simple way to clear dc fault currents. However, each arm's reverse-biased voltage (RBV) is uncontrolled in this method. In this case, the dc fault current will concentrate into two of the six arms. Thus, the maximum arm current will increase to the fault current in the dc line, which will lead to arm overcurrent. Moreover, full-bridge submodules (FB-SMs) will be charged by the large arm currents and may suffer from severe overvoltage. The arm overcurrent and FB-SM overvoltage problems have not been solved properly. This letter proposes a method to control the RBV of each arm during the dc fault-clearing process to relieve the arm overcurrent and FB-SM overvoltage. Thus, the safety of the converter can be improved. In the meantime, the impact on the dc fault clearing time is well limited. Simulations and experiments validated the proposed method.**

I. INTRODUCTION

The hybrid modular multilevel converter (HMMC) is composed of half-bridge submodules (HB-SMs) and full-bridge submodules (FB-SMs), as shown in Fig. 1(a), is attractive for its dc fault clearing capability and has been applied in the KunLiuLong ±800 kV dc transmission project in China [1], [2].

Generally, there are two ways for the HMMC to clear dc fault currents. One is blocking all HB- and FB-SMs, and the other is using the FB-SMs to regulate the dc voltage to be zero or negative while SMs are not blocked [3], [4]. The SM blocking method requires a lower proportion of FB-SMs than the SM unblocking method in achieving the same dc fault-clearing time. Thus, the SM blocking method can be more economical with a proper design.

However, FB-SMs will be charged by the fault current and may suffer severe SM overvoltage if the dc transmission line is long and/or if the ratio of FB-SMs is low [5]. Ref. [6] concludes that a long transmission line will lead to severe FB-SM overvoltage and increasing the SM capacitance or the ratio of FB-SMs can reduce the maximum FB-SM voltage. However, both methods will greatly increase the converter's cost and volume and, therefore, are not cost-effective. In [7], the ratio of FB-SMs is limited to 25% to reduce the cost and power losses of the converter. However, the maximum FB-SM voltage and the dc fault clearing time are increased. In [8], a SM unblocking method is adopted. Therefore, the excess energy of the dc side can be sent to the ac grid during the dc fault-clearing process to

Xiongfeng Fang, Cheng Wang, and Lei Li are with the School of Automation, Nanjing University of Science and Technology, Nanjing 210094, China (e-mail: fangxiongfeng@foxmail.com; chw714@njust.edu.cn; lileinjust@njust.edu.cn). *(Corresponding author: Cheng Wang.)*

Gen Li is with the Electric Energy Group, Department of Engineering Technology, Technical University of Denmark (DTU), 2750 Ballerup, Denmark (email: genli@dtu.dk).

mitigate FB-SM overvoltage. However, this method requires more FB-SMs, and its application is limited in some cases, for example, the ac grid may not be able to absorb the excess energy when it is connected to a wind farm.

In [9], a dynamic model considering the current commutation process between arms is proposed to calculate the dc fault clearing time and the maximum FBSM voltage after the dc fault current is entirely blocked. In [10], the FB-SM overvoltage problem during the dc fault-clearing process is analyzed, and an energy-absorption branch (EAB) composed of metal oxide varistors and thyristors is proposed to decrease the FB-SM voltage. Although the EAB can effectively avoid FB-SM overvoltage, extra components are still needed. In [11], an auxiliary circuit is proposed to change the direction of HMMC's dc fault current, which enables HB-SMs to participate in the dc fault clearance. Thus, the dc fault clearing time is reduced, and the ratio of FB-SMs can be reduced. Moreover, since more SMs can participate in the dc fault clearance, the maximum FB-SM voltage can be decreased. The above effective ways to solve the FB-SM overvoltage during dc fault are based on adding new components in the MMC, which will increase its cost and volume.
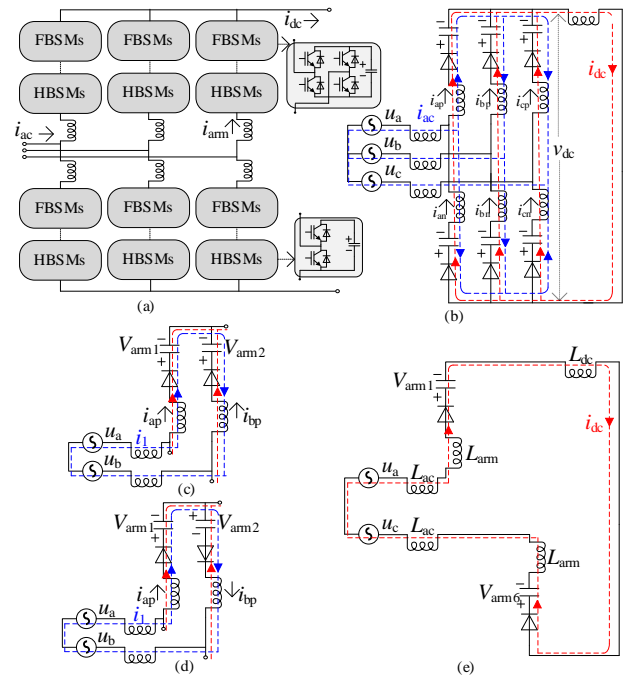

Fig. 1. The HMMC. (a) Topology of an HMMC; (b) equivalent circuit after SM blocking (when $u_a > u_b > u_c$); (c) one general ac current path; (d) one ac current path when one arm current decreases to zero; (e) one dc fault current path.

The FB-SM overvoltage is caused by the large arm current, which will also threaten the converter's safety while rarely

noted. After blocking all SMs, an ac short circuit will occur temporarily. The fast rise of ac current will affect arm currents. After a short current commutation process, the dc fault current will concentrate in one upper arm and one lower arm, which will increase the arm currents. Since the large arm currents will charge the blocked FB-SMs during the dc fault-clearing process, the FB-SM voltage of some arms may be extremely high. The arm overcurrent and FB-SM overvoltage during the dc fault-blocking process of the HMMC still need to be solved properly.

A reverse-biased voltage (RBV) control strategy is proposed in this letter to limit the changing of ac currents after SM blocking. The RBV can be changed by controlling the number of blocked FB-SMs. By reducing the RBV in the same direction as the ac current, the ac currents can be limited. Thus, the maximum arm current stress and FB-SM voltage can be reduced. Besides, particular consideration is paid to limit increasing the dc fault clearing time. The main contributions of this work are: 1) it is the first time to eliminate arm overcurrent and submodule overvoltage based on RBV control, with proper management of the dc fault clearing time; 2) it provides a solution that is very friendly to real practical due to the simplicity of the method itself and no additional hardware required for its implementation. Simulation and experiment results are presented to validate the proposed method.

II. REVERSE-BIASED VOLTAGE CONTROL METHOD

A. Arm Overcurrent and SM Overvoltage

In phase i ($i = a$, b, c), the upper arm current is i_{ip} and the lower arm current is i_{in}. They can be described as

$$\begin{cases} i_{ip} = \dfrac{i_{dc}}{3} + \dfrac{i_i}{2} \\ i_{in} = \dfrac{i_{dc}}{3} - \dfrac{i_i}{2} \end{cases}, \tag{1}$$

where i_{dc} is the dc current, i_i is the ac current. When a dc short circuit fault occurs, i_{dc} will rise quickly, as shown in (2), while the ac current is nearly unaffected.

$$\frac{di_{dc}}{dt} = \frac{v_{dc}}{L_{dc}} . \tag{2}$$

According to (1), if the dc current of each arm is significantly larger than the ac current, the currents of the six arms will be in the same direction as the dc fault current. When the dc short-circuit fault is detected, all FB-SMs of the HMMC will be blocked to provide RBV to clear the dc fault current, as shown in Fig.1 (b). Since arm currents are in the same direction as the dc fault current, the RBV of each arm is in the same direction. Each ac current circuit contains two opposite arm voltages, as shown in Fig. 1(c). The changing rate of the circulating current i_1 is

$$\frac{di_1}{dt} = \frac{u_a - u_b - V_{arm1} + V_{arm2}}{2L_{arm} + 2L_{ac}} . \tag{3}$$

Besides, since the number of blocked FB-SMs in each arm is the same, the value of the RBV in each arm is about the same as well, which means $V_{arm1} = V_{arm2}$. Thus, the changing rate of i_1 becomes (4), which means arm voltages will not limit the

changing of i_1 at this stage. i_1 will change quickly, which is equivalent to an ac short-circuit.

$$\frac{di_1}{dt} = \frac{u_a - u_b}{2L_{arm} + 2L_{ac}} . \tag{4}$$

According to (1), some arm currents will rise, and others will decrease due to the rise of ac currents. The ac current will flow from the phase with the highest ac voltage to the phase with the lowest ac voltage, as shown in Fig. 1(b). Thus, the current of the upper arm of the phase with high ac voltage (i_{ap} in Fig. 1(b)) will rise, and the current of the lower arm with low ac voltage (i_{cn} in Fig. 1(b)) will rise. The currents of the other four arms will decrease.

When the current of one arm decreases to zero, the voltage of this arm (V_{arm2} in Fig. 1(d)) will reverse, which will stop the changing of the ac current. Thus, the arm current will be kept at zero. Finally, the dc fault current will concentrate in the upper arm with the highest ac voltage and the lower arm with the lowest ac voltage. The current of the other arms will be small.

After the dc fault current is concentrated in two arms, the maximum arm current becomes equal to the dc side fault current, as shown in Fig. 1(e). Since the amplitude of the dc fault current i_{dcf} is much larger than the rated ac currents i_{ac}, the arm currents will be increased by the rise of ac current during dc fault clearance. The increment of arm current is

$$\Delta i_{arm} = i_{dcf} - (\frac{i_{dcf}}{3} \pm \frac{i_{ac}}{2}) = \frac{2i_{dcf}}{3} \pm \frac{i_{ac}}{2} . \tag{5}$$

Capacitors of FB-SMs will be charged by the large arm current, leading to FB-SM overvoltage, as shown in (6)

$$\Delta V_{FBmax} = \frac{\int_0^{t_c} |i_{arm}| dt}{C} , \tag{6}$$

where t_c is the charging time of FB-SMs, and C is SM capacitance.

B. Proposed Method to Limit the Arm Current

According to the analysis of Section A, it can be known that the fast-changing of ac currents will cause large arm currents and FB-SM overvoltage. Thus, the problem can be solved by limiting the changing of ac currents. According to (3), decreasing the RBV in the same direction as the ac current (V_{arm2} in Fig. 1(c)) can limit the ac current. However, the effect of decreasing the RBV on the dc fault-clearing time should be considered as well. The dc fault current clearing time is affected by the decreasing rate of the dc fault current, which is decided by the voltage V_L of the inductors (including arm inductor L_{arm} and dc side inductor L_{dc}).

$$-\frac{di_{dc}}{dt} = \frac{V_L}{2L_{arm} + L_{dc}} . \tag{7}$$

The dc fault current will mainly pass through two arms, as shown in Fig. 1(e). V_L is decided by the ac voltage and RBVs of the two arms. For example, if $v_a > v_b > v_c$, the dc fault current will be transferred to the upper arm of phase a and the lower arm of phase c. The lowest voltage of inductors V_L is

$$V_L = V_{arm1} + V_{arm6} - u_a + u_c . \tag{8}$$

The voltage of inductors in one of the other dc fault current paths (passing through the upper arm of phase *b* and the lower arm of phase *c*) is

$$V_{L}' = V_{arm2} + V_{arm6} - u_{b} + u_{c}. \tag{9}$$

To not slow down the dc fault clearing, the lowest voltage of inductors should not be decreased, as shown in (10):

$$V_{L}' \geq V_{L}. \tag{10}$$

Thus, the range of V_{arm2} is

$$V_{arm2} \geq V_{arm1} - u_{a} + u_{b} = 0.5V_{dc} - u_{ab}, \tag{11}$$

where V_{dc} is the rated dc voltage of the converter. According to (3), a small V_{arm2} can lead to a slow change of ac currents. Thus, the upper arm voltage v_{ip} of phase *i* will be

$$v_{ip} = 0.5V_{dc} - u_{ji}, \tag{12}$$

where phase *j* is the phase with the highest ac voltage. The lower arm voltage v_{in} of phased *i* can be calculated similarly

$$v_{in} = 0.5V_{dc} - u_{ik}, \tag{13}$$

where phase *k* is the phase with the lowest ac voltage.

If the dc side fault current has decreased to be little than the rated current of IGBTs, the converter will not be threatened by the dc fault current. Thus, the proposed method can be turned off to reduce the impact on the dc fault clearing time.

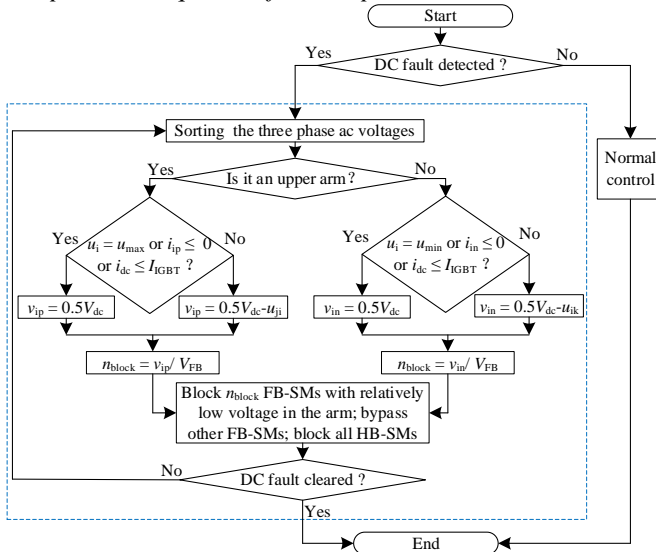### C. Operation Sequence of the Proposed RBV Control

Fig. 2. The proposed RBV control method.

The proposed RBV control method is shown in Fig. 2. The proposed method is not applied during normal operation. Thus, the proposed method will not affect the control system of the converter. If a dc short-circuit fault is detected, the proposed method will start to calculate arm voltages. u_{max} is the largest ac voltage, and u_{min} is the lowest ac voltage. For the upper arm with the highest ac voltage, the arm voltage is 0.5 V_{dc}, which means all FB-SMs should be blocked. For the other upper arms, the arm voltage is calculated by (12). For the lower arm with the lowest ac voltage, the arm voltage is 0.5 V_{dc}. For the other lower arms, the arm voltage is calculated by (13). When the arm currents become zero or negative, all SMs of the arm can be blocked since the RBV will reverse and stop the changing of

the circulating current. When the dc side fault current is smaller than the rated current of IGBTs I_{IGBT}, all SMs of the converter can be blocked. RBVs are provided by FB-SMs. The number of blocked FB-SMs in each arm is

$$n_{block} = \frac{v_{arm}}{V_{FB}}, \tag{14}$$

where V_{FB} is the rated voltage of each SMs. The arm voltage will be a step-wave. Other FB-SMs are bypassed. If v_{arm} is negative, all FB-SMs of the arm will be bypassed. Since only blocked FB-SMs will be charged, FB-SMs with lower voltage are selected to be blocked in each control cycle to maintain the balance of FB-SM voltages in each arm. All HB-SMs are blocked in the dc fault-clearing process. The dc fault clearing process will last several milliseconds, while the control cycle of the proposed method is less than 50 μs. Thus, there will be enough time to implement the proposed method during the post-fault transient.

D. Analysis of the Proposed Method

In the conventional SM blocking method, all SMs are controlled to block (turn off all IGBTs) simultaneously once a dc fault is detected [1], [9], [12]. With the proposed method, some SMs are bypassed temporarily (instead of being blocked directly) to limit the ac current. Since the proposed method belongs to the SM blocking method, it should be compared with the conventional SM blocking method to show its characteristics. The effect of the proposed method is concluded in Table I. The proposed method can not only relieve the arm overcurrent but also reduce the maximum FB-SM voltage of the HMMC after SM blocking. Although the dc fault clearing time is slightly increased, it is well limited.

The proposed method tries to balance the dc fault current in each phase and balance the energy absorption in each arm. However, since the range of RBV (V_{arm2} in (3)) is limited to $0\sim0.5V_{dc}$, the changing rate of the circulating current (i_1) may not be zero. Thus, the proposed method cannot strictly balance the dc fault current. The range of the maximum arm current with the proposed method is

$$\frac{i_{ac}}{2} + \frac{i_{dcf}}{3} < i_{arm} < i_{dcf}. \tag{15}$$

By increasing the ratio of FB-SMs, the range of RBV can be extended. When the maximum RBV of each arm is larger than the amplitude of ac line voltages, the proposed method can achieve the maximum effect.

Thanks to the reduced arm current, the maximum FB-SM voltage can be decreased according to (6). Moreover, since a part of SMs needs to be bypassed during dc fault blocking, the proposed method should be applied before the dc fault current exceeds twice of the rated current of IGBTs.

TABLE I
EFFECT OF THE PROPOSED METHOD

Items	Effect
Maximum arm current	Decreased significantly
Maximum FB-SM voltage	Reduced significantly
DC fault clearing time	Increased slightly

III. SIMULATION RESULTS

A symmetrical monopole hybrid MMC-HVDC link is built in Matlab/Simulink to verify the proposed method. Parameters are given in Table II. The dc fault detection time is selected as a typical value of 3 ms. A dc side pole-to-pole short circuit fault occurs at $t = 0.5$ s, and SMs start to block at $t = 0.503$ s.

Fig. 3(a) shows that after all SMs are blocked, the dc voltage becomes negative, and the dc current is decreased. The ac currents increase and then start to decrease. The fault currents are concentrated in two arms. The maximum arm current is 3.385 kA. FB-SM voltages increase a lot. The maximum FB-SM voltage is 2.525 kV. HB-SM voltages are not changed after SM blocking.

TABLE II
SETUP OF THE HYBRID MMC

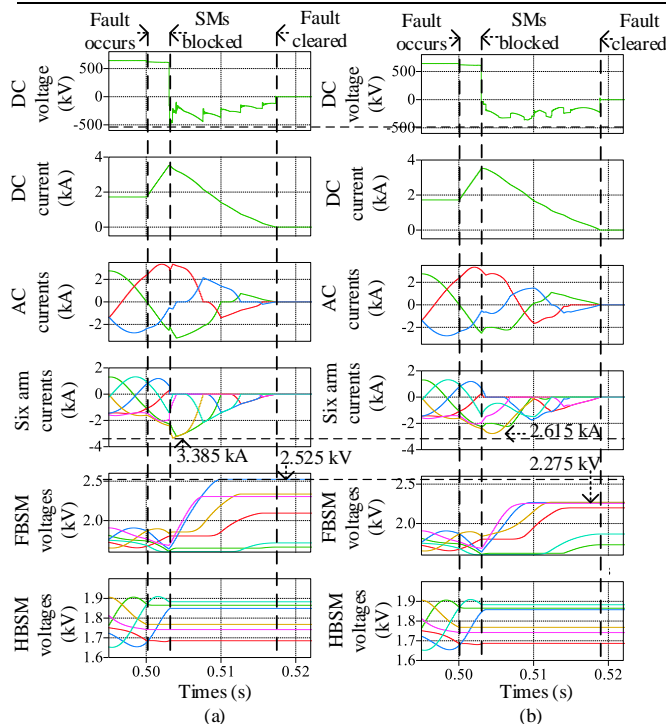| Parameters	Simulation	Experiment
Dc voltage	±320 kV	200 V
Rated dc current	1.56 kA	5 A
AC line voltage	333 kV	120 V
Number of HB-SMs per arm	178	1
Number of FB-SMs per arm	178	1
SM voltage	1.8 kV	100 V
SM capacitance	17 mF	560 μF
Arm inductance	52.94 mH	4.62 mH

Fig. 3. Simulation results. (a) The conventional method (all SMs are blocked), (b) the proposed method.

Fig. 3(b) shows the simulation results of the proposed method. After SMs start to block, the dc voltage is slightly lower than that of Fig. 3(a) since some RBVs are reduced. The dc fault clearing time is only marginally longer. The increase of ac current is limited after SM blocking. The maximum arm current decreases to 2.615 kA. The maximum FB-SM voltage decreases to 2.275 kV. HB-SM voltages remain constant. It can be seen that the proposed method can reduce the maximum arm current and the maximum FB-SM voltage.

IV. EXPERIMENTAL RESULTS

Experiments have been conducted using a three-phase hybrid MMC, as shown in Fig. 4. Parameters of the experiment setup are given in Table II. For the safety of the experiment setup, the overcurrent protection is used. In this case, the converter starts to clear the dc fault current once the dc current reaches 17 A.

Fig. 5(a) shows the experiment results of the conventional SM blocking method (all SMs are blocked) [1], [9], [12]. After SM blocking, the dc voltage becomes negative, and the dc fault current decreases. The maximum arm current is 14 A, and the highest FB-SM voltage is 160 V.
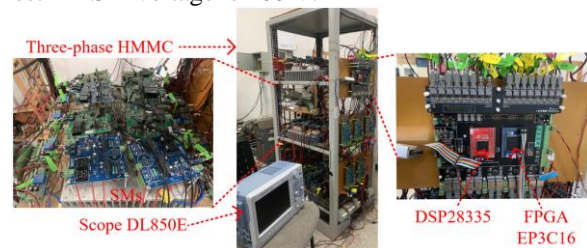

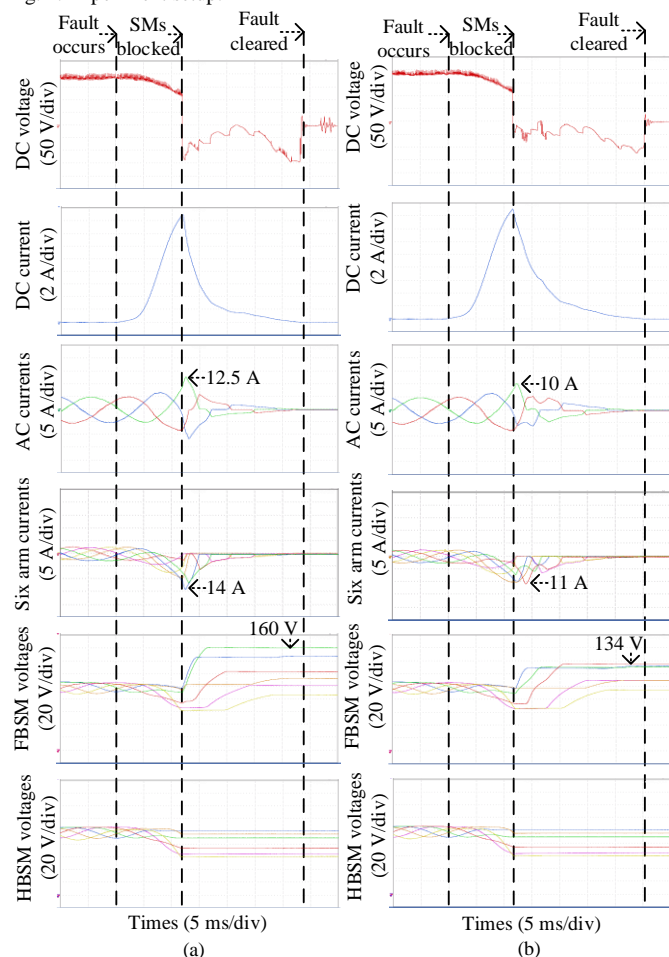Fig. 4. Experiment setup.

Fig. 5. Experiment results. (a) The conventional method, (b) the proposed method.

Fig. 5(b) shows the experiment results of the proposed method. Compared with Fig. 5(a), it can be seen that the negative dc voltage is slightly reduced after SM blocking. The dc fault clearing time is slightly longer. The increase of ac

current is limited after SM blocking. The maximum arm current stress is 11 A, and the maximum FB-SM voltage is 134 V, all lower than the conventional method. HB-SM voltages are not changed in both situations. Experiment results are consistent with the simulation results.

V. Conclusion

A reverse-biased voltage control method is proposed in this letter to limit the ac current during the dc fault-clearing process. Thanks to the limited ac currents, the maximum arm current stress, and the maximum SM voltage are reduced. Thus, the safety of the converter is improved. Besides, the proposed method's effect on the dc fault clearing time is well limited. The proposed method provides a safer way for the hybrid MMC to clear the dc fault current.

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