ShanghaiTech University

EE 115B: Digital Circuits

Solution

Fall 2024

Final Exam, January 7, 2025

My signature below indicates that I understand and have complied with the Academic Integrity Policy of ShanghaiTech University. I have neither received nor given any unauthorized aid.

Student ID: _____ Name in Chinese: _____

1. (5 points, 1 point each.) Short questions.
   (1) Convert $(32.4)_{16}$ to octal.

3 2 . 4
0011 0010 . 0100
6 2 . 2

$(32.4)_{16} = (62.2)_8$

   (2) Convert $(01100001)_{BCD}$ to hexadecimal.

$(0110\ 0001)_{BCD} = (61)_{10}$

$= (3D)_{16}$

		remainder
16 | 61		
16 | 3		13 → D
0		3

   (3) Draw the circuit symbol for the two-input XOR gate.

   (4) What does "VHDL" stand for?

VHSIC (Very High Speed Integrated Circuits)
Hardware Description Language

   (5) What does "FPGA" stand for?

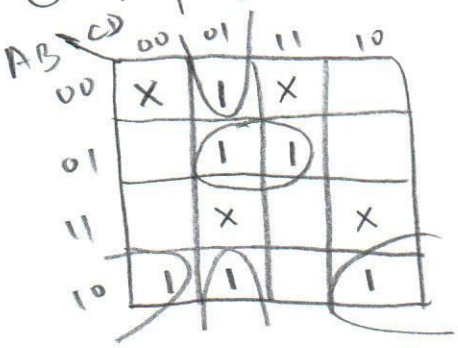
Field Programmable Gate Array

2. (20 points, 5 points each.) Develop the minimum sum of products (SOP) and product of sums (POS) expressions with and without the don't cares using Karnaugh map.

$$Y(A,B,C,D) = \sum m(1,5,7,8,9,10) + X(0,3,13,14)$$

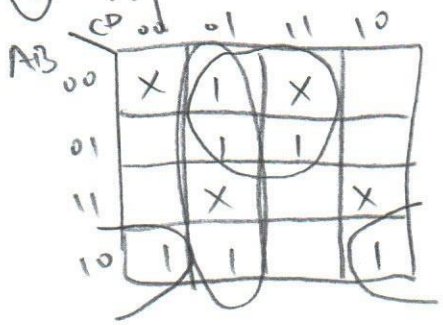
NOTE: There may be other minimum expressions.

① SOP without don't cares



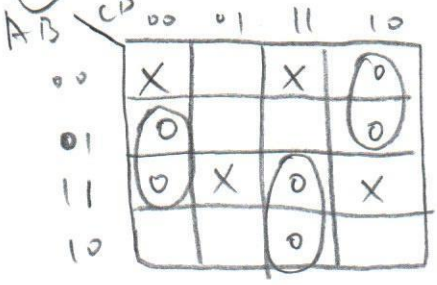
$$Y = \bar{B}\bar{C}D + \bar{A}BD + A\bar{B}\bar{D}$$

② SOP with don't cares



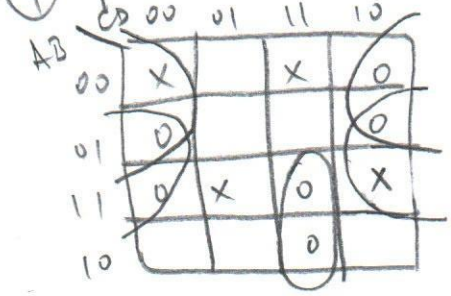
$$Y = \bar{A}D + \bar{C}D + A\bar{B}\bar{D}$$

③ POS without don't cares



$$Y = (\bar{B}+C+D)(\bar{A}+\bar{C}+\bar{D})(A+\bar{C}+D)$$

④ POS with don't cares



$$Y = (A+D)(\bar{B}+D)(\bar{A}+\bar{C}+\bar{D})$$

3. (15 points, 5 points each.) Convert the following AND-OR expression to NAND, AND-OR-Invert (AOI), and NOR expressions.

$$\boldsymbol{Y(A,B,C,D) = CD + B'D + BC'D' + A'BC}$$

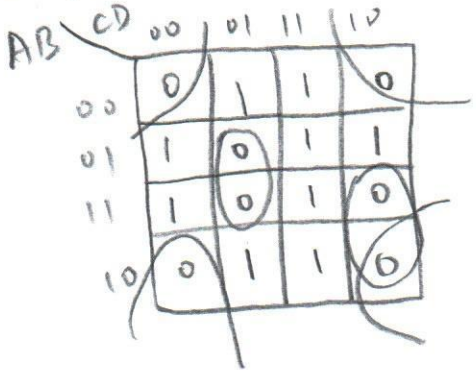
① NAND

$$Y = CD + \bar{B}D + B\bar{C}\bar{D} + \bar{A}BC$$

$$= \overline{CD + \bar{B}D + B\bar{C}\bar{D} + \bar{A}BC}$$

$$= \overline{\overline{CD} \cdot \overline{\bar{B}D} \cdot \overline{B\bar{C}\bar{D}} \cdot \overline{\bar{A}BC}}$$

② AOI



$$Y = \overline{\bar{B}\bar{D} + B\bar{C}D + AC\bar{D}}$$

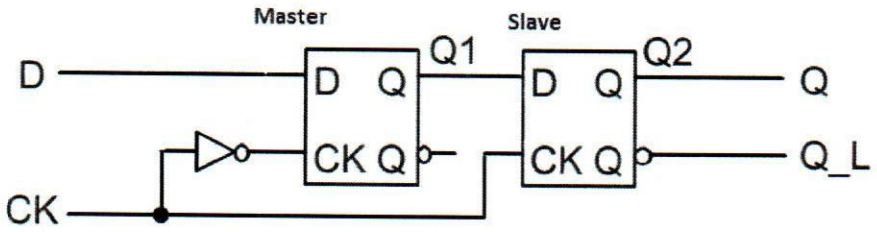
③ NOR

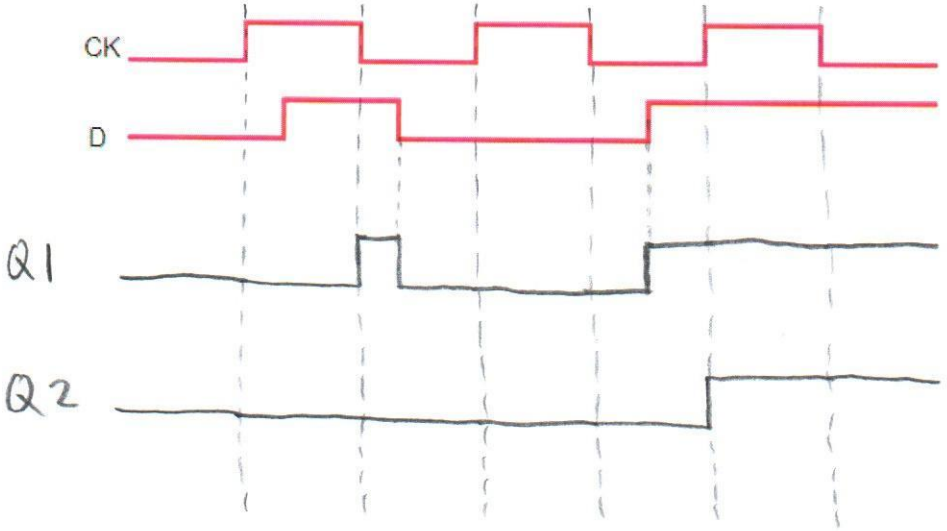
$$Y = \overline{\bar{B}\bar{D} + B\bar{C}D + AC\bar{D}}$$

$$= \overline{\overline{\bar{B}\bar{D}} + \overline{B\bar{C}D} + \overline{AC\bar{D}}}$$

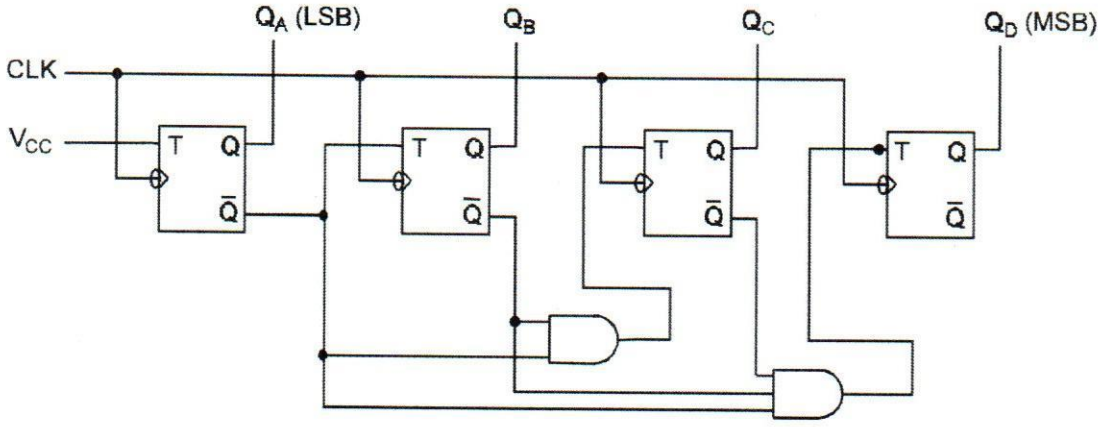
$$= \overline{\overline{B+D} + \overline{\bar{B}+C+\bar{D}} + \overline{\bar{A}+\bar{C}+D}}$$

4. (10 points, 5 points each.) Sketch the timing diagram of Q1 and Q2. Assume that the initial values of Q1 and Q2 are both 0. Ignore the propagation delay.



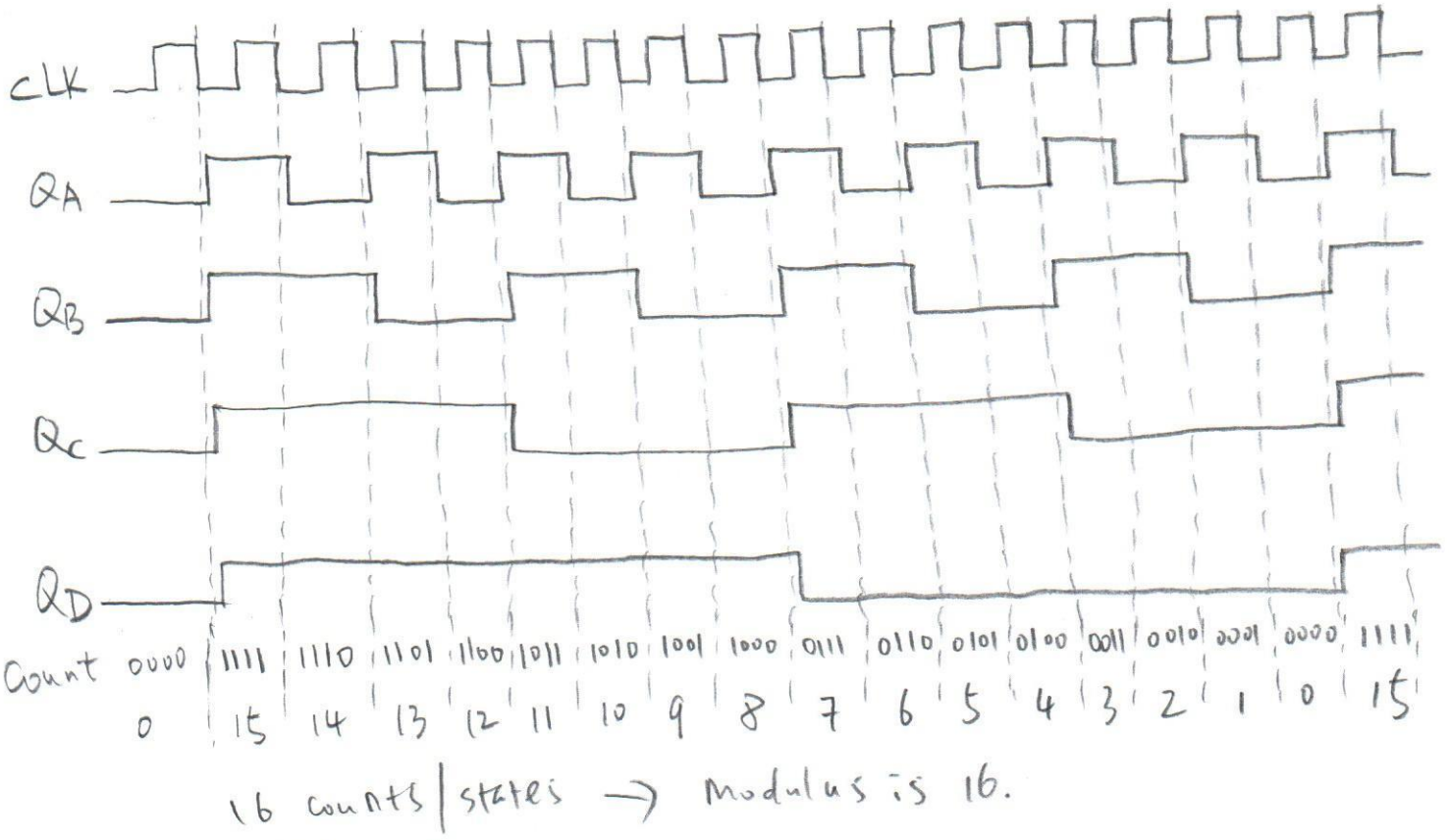


5. (30 points.) Consider the counter below. Note that V_{CC} means the logic value of 1.



(a) Sketch the timing diagram of Q_A, Q_B, Q_C, and Q_D. Analyze the binary sequence of this counter and identify its modulus. Assume that the initial states are Q_A=Q_B=Q_C=Q_D=0. The count is represented by "$Q_DQ_CQ_BQ_A$" with Q_D as the most significant bit (MSB) and Q_A as the least significant bit (LSB). (16 points for timing diagram, 4 points for binary sequence, and 4 points for modulus.)

$T_A = 1$, $T_B = \overline{Q_A}$, $T_C = \overline{Q_A}\,\overline{Q_B}$, $T_D = \overline{Q_A}\,\overline{Q_B}\,\overline{Q_C}$



16 counts | states → Modulus is 16.

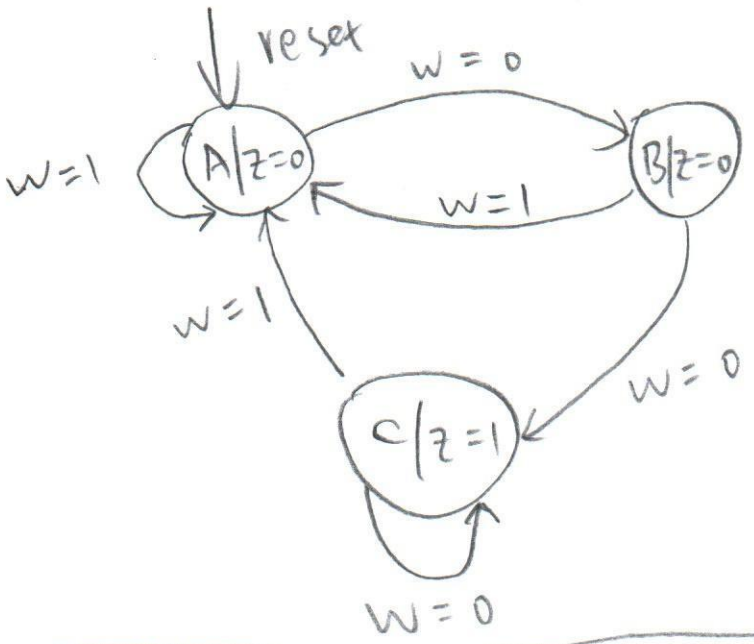
(b) (True or False, 3 points.) This counter is a synchronous counter. **Justify your answer.**

True. All the four stages are driven by the same clock.

(c) (True or False, 3 points.) This counter is an up-counter. **Justify your answer.**

False. For a complete period, the count decreases from 15 to 0. The counter is a down-counter.

6. (15 points.) Draw a state diagram for the following finite state machine. Below are the design specifications:
   (a) The machine has one input (w) and one output (z).
   (b) All changes occur at positive clock edges.
   (c) Operation: z=1 if w=0 during two immediately preceding clock cycles; z=0, otherwise.
   (d) When a reset signal is applied, the machine enters the first state.



optional for analysis only

State	bits received	bits needed	z
A	-/1	00	0
B	0	0	0
C	00	—	1

7. (5 points.) Consider an analog to digital converter (ADC). The highest frequency of the analog signal is 5 kHz.
   (a) Determine the Nyquist rate. (2 points.)

$f_N = 2 \times 5\,kHz = 10\,kHz$

   (b) Suppose the analog signal is sampled with a frequency of 20 kHz and the quantizer is composed of two 10-bit channels. Determine the data rate of this ADC. (3 points.)

Data rate = 2 x 10 bits/sample x 20 k samples/s

= 400 kbps

This page is intentionally left blank.
Do NOT use this page as an answer sheet.