ShanghaiTech University

EE 115B: Digital Circuits

Fall 2024

Solution

Homework 5

Total: 100 Points

Assigned: December 15, 2024. Due: 23:59 PM, December 29, 2024.

1. Assuming that the D and Clock inputs shown in Fig. 1 are applied to the circuits shown in Fig. 2, draw the waveforms for Q_a, Q_b, and Q_c. Assume that the initial states are Q_a=0, Q_b=1, and Q_c=0. Ignore the propagation delays. (30 points, 10 points each.)

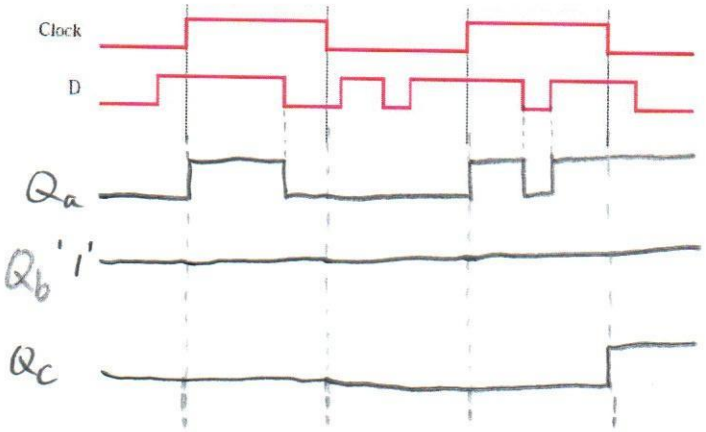


Fig. 1: Timing diagram.

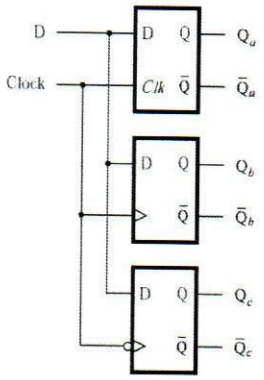


Fig. 2: Circuits.

2. The characteristic table and circuit symbol for a T flip-flop are shown in Fig. 3. For the inputs shown in Fig. 4, draw the Q waveform assuming that the initial state is Q=1. Ignore the propagation delays. (20 points.)

T	Q(t+1)
0	Q(t)'
1	Q(t)

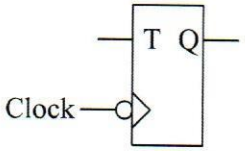


Fig. 3: T flip-flop.

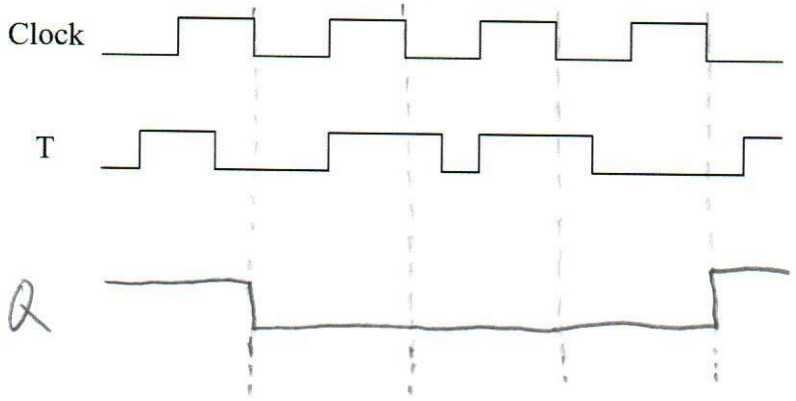


Fig. 4: Timing diagram.

3. Consider the universal shift register implemented in lab 3. For your reference, the block diagram as well as the signal and mode definitions are repeated as follows. Complete the table below to determine the output of the register during the next clock cycle. Specifically, suppose the present time is t0 and the clock cycle period is Δt. Based on the information of the serial input, parallel input, mode selection signal, and output at t=t0, determine the output at t=t0+Δt. (20 points, 5 points each.)

Serial_in (t=t0)	P(3:0) (t=t0)	M(1:0) (t=t0)	Q(3:0) (t=t0)	Q(3:0) (t=t0+Δt)
1	0110	10	0011	0011
0	0010	11	1011	0101
1	1101	00	0110	1101
0	1011	01	0111	1011

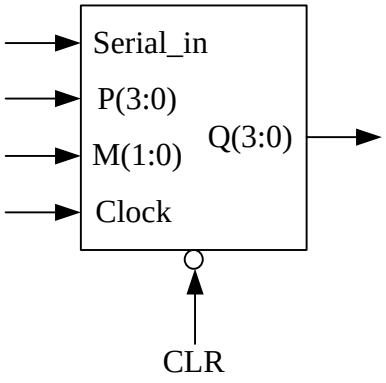


Fig. 4: Block diagram of universal shift register.

The signals are defined as follows:

M(1:0)	Mode selection signal
Serial_in	Serial input
P(3:0)	Parallel input
Clock	Clock signal: positive edge active
CLR	Asynchronous clear signal: active low
Q(3:0)	Output

The four operation modes are defined as follows:

M(1)	M(0)	Mode
0	0	Left shift: Serial_in to Q(0), Q(0) to Q(1), Q(1) to Q(2), Q(2) to Q(3)
0	1	Parallel load: P(3) to Q(3), P(2) to Q(2), P(1) to Q(1), P(0) to Q(0)
1	0	No change
1	1	Right shift: Serial_in to Q(3), Q(3) to Q(2), Q(2) to Q(1), Q(1) to Q(0)

4. The circuit shown in Fig. 5 is a counter. Analyze its binary sequence and identify its modulus. Assume that the initial states are $Q_0=Q_1=Q_2=0$. The count is represented by "$Q_2Q_1Q_0$" with Q_2 as the MSB and Q_0 as the LSB. (30 points.)

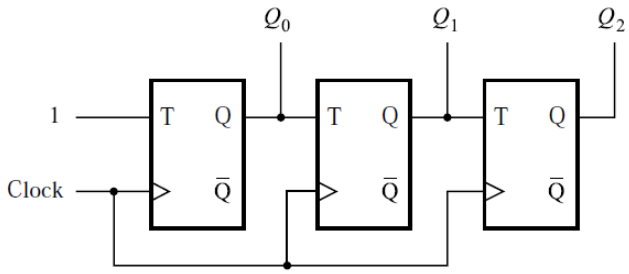
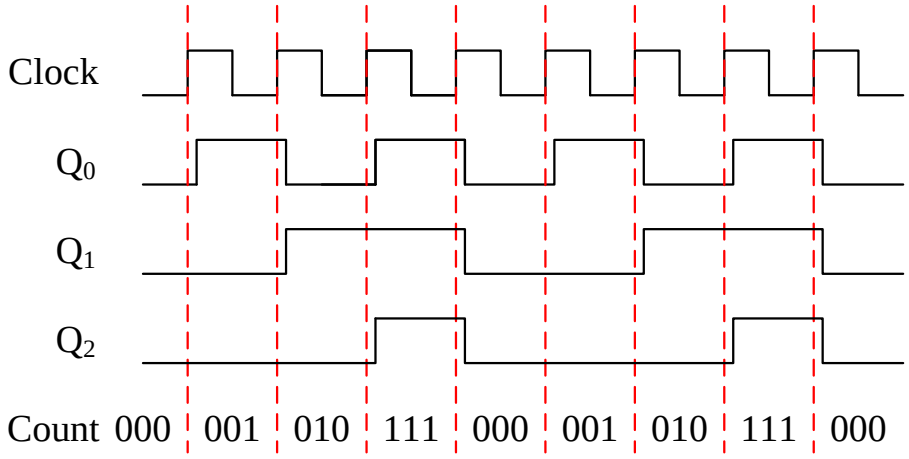


Fig. 5: Counter.

4. Timing diagram:



The binary sequence is 000, 001, 010, and 111.

Since this counter has four different counts (i.e., states), its modulus is 4.