ShanghaiTech University

EE 115B: Digital Circuits

Fall 2024

Final Exam, January 7, 2025

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Student ID: _____   Name in Chinese: _____

1. (5 points, 1 point each.) Short questions.
   (1) Convert $(32.4)_{16}$ to octal.

   (2) Convert $(01100001)_{BCD}$ to hexadecimal.

   (3) Draw the circuit symbol for the two-input XOR gate.

   (4) What does "VHDL" stand for?

   (5) What does "FPGA" stand for?

2. (20 points, 5 points each.) Develop the minimum sum of products (SOP) and product of sums (POS) expressions with and without the don't cares using Karnaugh map.

$$Y(A, B, C, D) = \sum m(1, 5, 7, 8, 9, 10) + X(0, 3, 13, 14)$$

3. (15 points, 5 points each.) Convert the following AND-OR expression to NAND, AND-OR-Invert (AOI), and NOR expressions.

$$Y(A, B, C, D) = CD + B'D + BC'D' + A'BC$$

4. (10 points, 5 points each.) Sketch the timing diagram of Q1 and Q2. Assume that the initial values of Q1 and Q2 are both 0. Ignore the propagation delay.
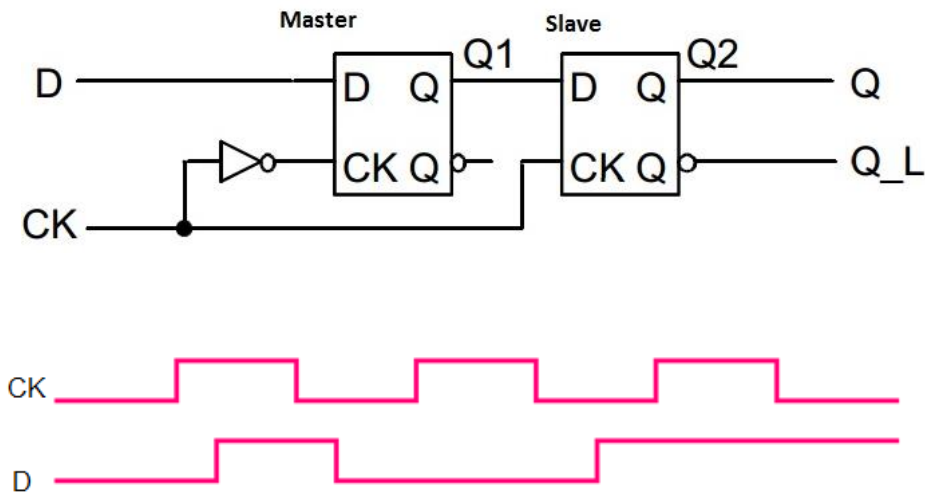
5. (30 points.) Consider the counter below. Note that V_{CC} means the logic value of 1.
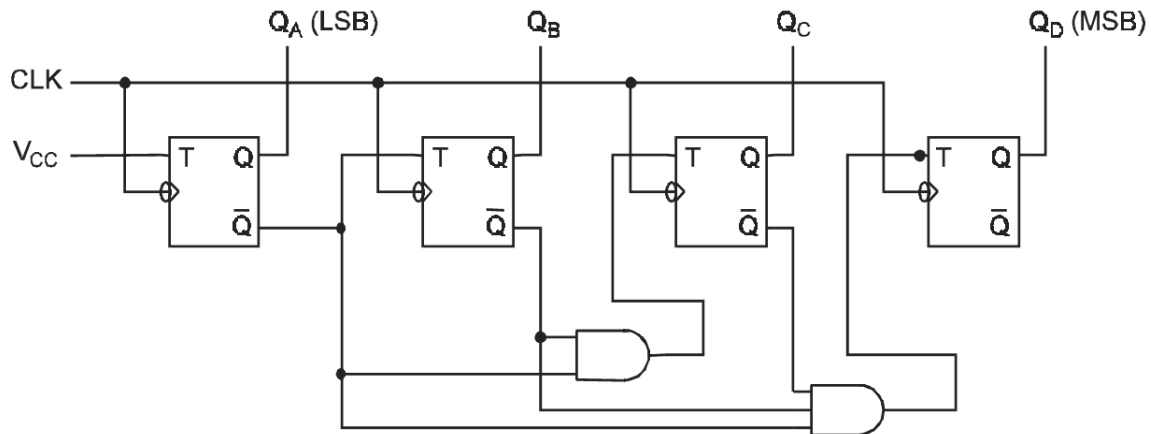
(a) Sketch the timing diagram of Q_A, Q_B, Q_C, and Q_D. Analyze the binary sequence of this counter and identify its modulus. Assume that the initial states are $Q_A=Q_B=Q_C=Q_D=0$. The count is represented by "$Q_D Q_C Q_B Q_A$" with Q_D as the most significant bit (MSB) and Q_A as the least significant bit (LSB). (16 points for timing diagram, 4 points for binary sequence, and 4 points for modulus.)

(b) (True or False, 3 points.) This counter is a synchronous counter. **Justify your answer.**

(c) (True or False, 3 points.) This counter is an up-counter. **Justify your answer.**

6. (15 points.) Draw a state diagram for the following finite state machine. Below are the design specifications:
   (a) The machine has one input (w) and one output (z).
   (b) All changes occur at positive clock edges.
   (c) Operation: z=1 if w=0 during two immediately preceding clock cycles; z=0, otherwise.
   (d) When a reset signal is applied, the machine enters the first state.

7. (5 points.) Consider an analog to digital converter (ADC). The highest frequency of the analog signal is 5 kHz.
   (a) Determine the Nyquist rate. (2 points.)

   (b) Suppose the analog signal is sampled with a frequency of 20 kHz and the quantizer is composed of two 10-bit channels. Determine the data rate of this ADC. (3 points.)

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Do NOT use this page as an answer sheet.