Lab1 Encoder Implementation

Objectives

1. To study the logic gates.
2. To familiarize with Combinational logic.
3. Design an 8-to-3 line Encoder using 74LS00 and 74LS02 Logic gates.
4. Use NI Multisim to simulate the 8-to-3 line Encoder using 74LS00 and 74LS02 Logic gates.
5. Construct and Verify the truth tables.

COMPONENTS

1. DC Power Supply
2. Multimeter
3. NAND Gate IC 74LS00 *2
4. NOR Gate IC 74LS02 *2
5. Bread board and connecting wires
6. LEDs and resistors

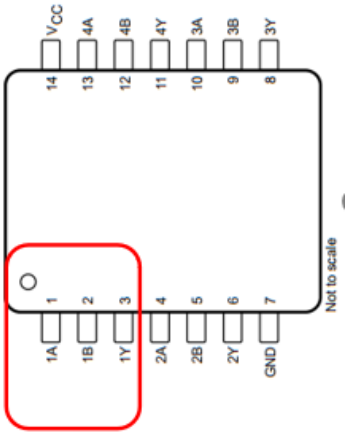
THEORY

Logic Gate

The logic gate is the fundamental building block in digital systems. Logic gates operate with binary numbers. Gates are therefore referred to as binary logic gates. All voltages used with logic gates will be either HIGH or LOW, where a HIGH voltage corresponds to a binary 1 and a LOW voltage signifies a binary 0.

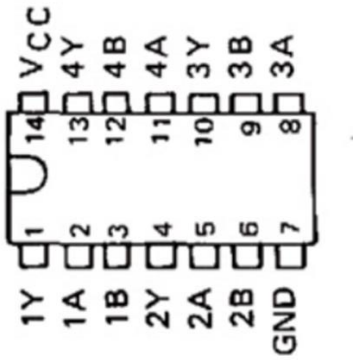
NAND Gate 74LS00

Logic Diagram



Pin Diagram

NOR Gate 74LS02



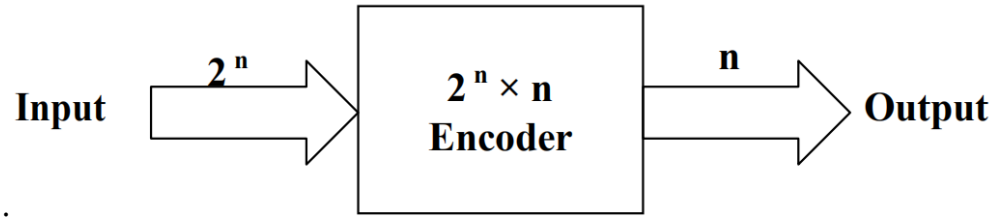
Logic Diagram Pin Diagram

Combinational Logic Circuits

Combinational Logic Circuits are memoryless digital logic circuits whose output are only determined by the logical function of their current input state, logic "0" or logic "1", at any given instant in time.

A Decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines.

An Encoder is a digital circuit that performs the opposite function of a decoder. An encoder has 2^n input lines and n output lines. The output lines generate the binary code corresponding to the input value. In encoders, it is assumed that only one input has a value of 1 at any given time. The encoders are specified as m to-n encoders where $m \leq 2^n$.



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Pre-Lab1 Report 8-to-3 line Encoder Design

Design a 8 to 3 line Encoder using 74LS00 and 74LS02 Logic gates. The 8 to 3 line Encoder consists of 8 inputs I_7, I_6, I_5, I_4, I_3, I_2, I_1 & I_0, and three outputs Y_2, Y_1 & Y_0. At any time, only one of these 8 inputs can be '1' in order to get the respective binary code at the output.

1. Truth table_____/6pt

2. Logical Expression for Y_2, Y_1 & Y_0 (NAND, NOR). _____/6pt

3. Draw the logic diagram based on the Logical Expression obtained in step 2 (2 input NAND gates, 2 input NOR gates). _____/6pt

4. Based on the above analysis results, use Multisim to simulate and verify the design (use IC 74LS00 and 74LS02 to construct the design).

1) 5V is used to represent logic value 1, while 0V is used to represent logic value 0. _____/6 pt

2) All 8 input patterns can be produced (to generate a truth table for the circuit) by manually toggling the inputs. _____/6 pt

3) Output Y_2, Y_1 & Y_0 are connected in series with yellow, green, and red LED through a 402Ω current limiting resistor respectively. _____/6 pt

4) Provide screenshot of the simulation schematic._____/6 pt

5) Summarize the simulation results and record the status of LED lights corresponding to each input combination for Y2 Y1 Y0. _____/7pt

Lab1 Report 8-to-3 line Encoder

Construct the circuit on breadboard using the given IC 74LS00 and 74LS02 as you design in the prelab. Connect outputs Y2, Y1, and Y0 in series with 402 Ω current-limiting resistors to yellow, green, and red LEDs, respectively. Observe the output for various combinations of inputs. **Record** the LED states corresponding to each input combination for Y2, Y1, and Y0 . _____/50 pt