Lab2 Adder Implementation

Objectives

1. To study the logic gates.
2. To familiarize with Combinational logic.
3. To understand the principle of binary addition.
4. To use NI Multisim to simulate the adder.
5. To implement a Full adder circuit and Verify the truth tables.

COMPONENTS

1. Multimeter
2. Bread board and connecting wires
3. LEDs and resistors
4. 2 input AND Gate IC : 74LS08
5. 2 input XOR IC: 74LS86
6. 2 input OR IC: 74LS32

THEORY

An adder is a circuit whose output is the binary sum of its inputs. Adders are categorized into two types. One is Half Adder, and another one is known as Full Adder.

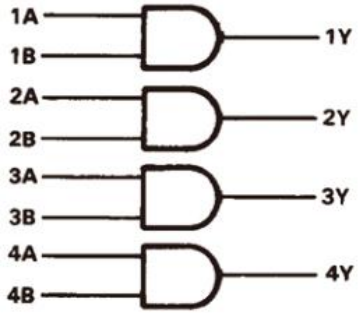
Half Adder

The Half Adder adds two binary digits (A & B), and produces two outputs as sum (SUM) and carry (CARRY).

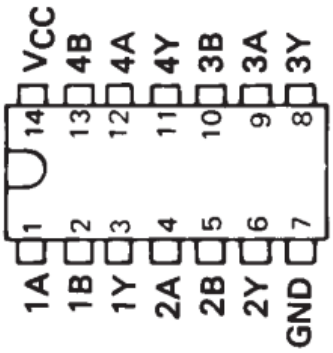
Full Adder

A full adder is a combinational circuit that performs an addition operation on three binary digits. It consists of three inputs (A, B, CARRY_IN) and two outputs (SUM, CARRY_OUT). The first two inputs are A and B and the third input is an input carry designated as CARRY_IN. The output carry is designated as CARRY_OUT and the normal output is designated as SUM.

2 input AND Gate 74LS08

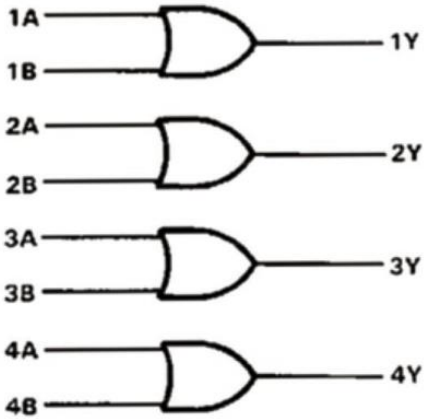


Logic Diagram

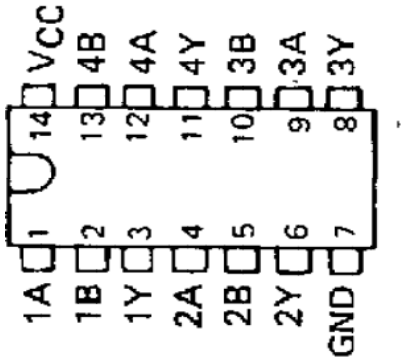


Pin Diagram

2 input OR Gate 74LS32



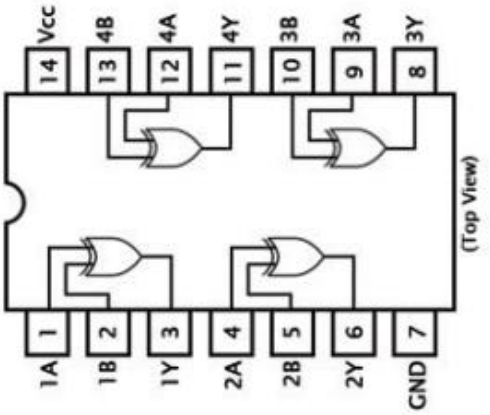
Logic Diagram



Pin Diagram

2 input XOR Gate 74LS86

Logic Diagram



Pin Diagram

Pre-Lab2 Report Adder Design

PART ONE：Half Adder

Design a Half Adder using X-OR&AND Gate.
Input variables: A, B;
Output variables: S(SUM), C(CARRY);
LED ON: Logic 1
LED OFF: Logic 0

1. Truth table_____/6pt

2. Logical Expression for S(SUM) & C(CARRY) (AND, XOR Gate). _____/6pt

3. Draw the logic diagram based on the Logical Expression obtained in step 2 (2 input AND gates, 2 input XOR gates). _____/6pt

4. Based on the above analysis results, use Multisim to simulate the the Half Adder(use IC 74LS08 and 74LS86 to construct the design). 5V is used to represent logic value 1, while 0V is used to represent logic value 0. _____/6 pt

1) All 2 input patterns can be produced (to generate a truth table for the circuit) by manually toggling the inputs. _____/6 pt

2) Output S(SUM) & C(CARRY) are connected in series with yellow, and red LED through a 402 Ω current limiting resistor respectively. _____/6 pt

3) Provide screenshot of the simulation schematic。_____/6 pt

4) Summarize the simulation results and record the status of LED lights corresponding to each input combination for S(SUM) & C(CARRY) . _____/7pt

PART Two：Full Adder

Implement a Full Adder using XOR OR & AND Gates.
Input variables: A, B, Cin (CARRY_IN);
Output variables: S(SUM), Cout (CARRY_OUT);
LED ON: Logic 1
LED OFF: Logic 0

1. Truth table_____/6pt

2. Logical Expression for S(SUM) & Cout (CARRY_OUT) (AND, XOR, OR).____/6pt

3. Draw the logic diagram based on the Logical Expression obtained in step 2 (2 input AND gates, 2 input XOR gates, 2 input OR gates). _____/6pt

4. Based on the above analysis results, use Multisim to simulate the the Full Adder. 5V is used to represent logic value 1, while 0V is used to represent logic value 0. _____/6 pt

5) All 3 input patterns can be produced (to generate a truth table for the circuit) by manually toggling the inputs. _____/6 pt

6) Output S(SUM), Cout(CARRY_OUT) are connected in series with yellow, and red LED through a 402 Ω current limiting resistor respectively. _____/6 pt

7) Provide screenshot of the simulation schematic._____/6 pt

8) Summarize the simulation results and record the status of LED lights corresponding to each input combination for S(SUM) & Cout(CARRY). _____/7pt

Lab1 Report Full Adder

Construct the circuit on breadboard as you design in the prelab. Observe the output and verify the truth table.

Connect outputs S(SUM), C(CARRY_OUT) in series with 402 Ω current-limiting resistors to yellow and red LEDs, respectively. Observe the output for various

combinations of inputs. **Record** the LED states corresponding to each input combination for A, B, CARRY_IN. _____/50 pt