

20.14.1. TC1 Control Register A

Name: TCCR1A

Offset: 0x80

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
	COM1	COM1	COM1	COM1			WGM11	WGM10
Access	R/W	R/W	R/W	R/W			R/W	R/W
Reset	0	0	0	0			0	0

Bits 4, 5, 6, 7 – COM1, COM1, COM1, COM1: Compare Output Mode for Channel

The COM1A[1:0] and COM1B[1:0] control the Output Compare pins (OC1A and OC1B respectively) behavior. If one or both of the COM1A[1:0] bits are written to one, the OC1A output overrides the normal port functionality of the I/O pin it is connected to. If one or both of the COM1B[1:0] bit are written to one, the OC1B output overrides the normal port functionality of the I/O pin it is connected to. However, note that the Data Direction Register (DDR) bit corresponding to the OC1A or OC1B pin must be set in order to enable the output driver.

When the OC1A or OC1B is connected to the pin, the function of the COM1x[1:0] bits is dependent of the WGM1[3:0] bits setting. The table below shows the COM1x[1:0] bit functionality when the WGM1[3:0] bits are set to a Normal or a CTC mode (non-PWM).

Table 20-3. Compare Output Mode, non-PWM

COM1A1/COM1B1	COM1A0/COM1B0	Description
0	0	Normal port operation, OC1A/OC1B disconnected.
0	1	Toggle OC1A/OC1B on Compare Match.
1	0	Clear OC1A/OC1B on Compare Match (Set output to low level).
1	1	Set OC1A/OC1B on Compare Match (Set output to high level).

The table below shows the COM1x[1:0] bit functionality when the WGM1[3:0] bits are set to the fast PWM mode.

Table 20-4. Compare Output Mode, Fast PWM

COM1A1/COM1B1	COM1A0/COM1B0	Description
0	0	Normal port operation, OC1A/OC1B disconnected.
0	1	WGM1[3:0] = 14 or 15: Toggle OC1A on Compare Match, OC1B disconnected (normal port operation). For all other WGM1 settings, normal port operation, OC1A/OC1B disconnected.

COM1A1/ COM1B1	COM1A0/ COM1B0	Description
1	0	Clear OC1A/OC1B on Compare Match, set OC1A/OC1B at BOTTOM (non-inverting mode)
1	1	Set OC1A/OC1B on Compare Match, clear OC1A/OC1B at BOTTOM (inverting mode)

Note:

1. A special case occurs when OCR1A/OCR1B equals TOP and COM1A1/COM1B1 is set. In this case the compare match is ignored, but the set or clear is done at BOTTOM. Refer to [Fast PWM Mode](#) for details.

The table below shows the COM1x1:0 bit functionality when the WGM1[3:0] bits are set to the phase correct or the phase and frequency correct, PWM mode.

Table 20-5. Compare Output Mode, Phase Correct and Phase and Frequency Correct PWM

COM1A1/ COM1B1	COM1A0/ COM1B0	Description
0	0	Normal port operation, OC1A/OC1B disconnected.
0	1	WGM1[3:0] = 9 or 11: Toggle OC1A on Compare Match, OC1B disconnected (normal port operation). For all other WGM1 settings, normal port operation, OC1A/OC1B disconnected.
1	0	Clear OC1A/OC1B on Compare Match when up-counting. Set OC1A/OC1B on Compare Match when down-counting.
1	1	Set OC1A/OC1B on Compare Match when up-counting. Clear OC1A/OC1B on Compare Match when down-counting.

Note:

1. A special case occurs when OCR1A/OCR1B equals TOP and COM1A1/COM1B1 is set. Refer to [Phase Correct PWM Mode](#) for details.

Bits 0, 1 – WGM10, WGM11: Waveform Generation Mode

Combined with the WGM1[3:2] bits found in the TCCR1B Register, these bits control the counting sequence of the counter, the source for maximum (TOP) counter value, and what type of waveform generation to be used. Modes of operation supported by the Timer/Counter unit are: Normal mode (counter), Clear Timer on Compare match (CTC) mode, and three types of Pulse Width Modulation (PWM) modes. (See [Modes of Operation](#)).

Table 20-6. Waveform Generation Mode Bit Description

Mode	WGM13	WGM12 (CTC1) ⁽¹⁾	WGM11 (PWM11) ⁽¹⁾	WGM10 (PWM10) ⁽¹⁾	Timer/ Counter Mode of Operation	TOP	Update of OCR1x at	TOV1 Flag Set on
0	0	0	0	0	Normal	0xFFFF	Immediate	MAX
1	0	0	0	1	PWM, Phase Correct, 8-bit	0x00FF	TOP	BOTTOM
2	0	0	1	0	PWM, Phase Correct, 9-bit	0x01FF	TOP	BOTTOM

Mode	WGM13	WGM12 (CTC1) ⁽¹⁾	WGM11 (PWM11) ⁽¹⁾	WGM10 (PWM10) ⁽¹⁾	Timer/ Counter Mode of Operation	TOP	Update of OCR1x at	TOV1 Flag Set on
3	0	0	1	1	PWM, Phase Correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCR1A	Immediate	MAX
5	0	1	0	1	Fast PWM, 8- bit	0x00FF	BOTTOM	TOP
6	0	1	1	0	Fast PWM, 9- bit	0x01FF	BOTTOM	TOP
7	0	1	1	1	Fast PWM, 10- bit	0x03FF	BOTTOM	TOP
8	1	0	0	0	PWM, Phase and Frequency Correct	ICR1	BOTTOM	BOTTOM
9	1	0	0	1	PWM, Phase and Frequency Correct	OCR1A	BOTTOM	BOTTOM
10	1	0	1	0	PWM, Phase Correct	ICR1	TOP	BOTTOM
11	1	0	1	1	PWM, Phase Correct	OCR1A	TOP	BOTTOM
12	1	1	0	0	CTC	ICR1	Immediate	MAX
13	1	1	0	1	Reserved	-	-	-
14	1	1	1	0	Fast PWM	ICR1	BOTTOM	TOP
15	1	1	1	1	Fast PWM	OCR1A	BOTTOM	TOP

Note:

1. The CTC1 and PWM1[1:0] bit definition names are obsolete. Use the WGM1[3:0] definitions. However, the functionality and location of these bits are compatible with previous versions of the timer.

20.14.2. TC1 Control Register B

Name: TCCR1B

Offset: 0x81

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
	ICNC1	ICES1		WGM13	WGM12	CS12	CS11	CS10
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	0	0	0	0

Bit 7 – ICNC1: Input Capture Noise Canceler

Writing this bit to '1' activates the Input Capture Noise Canceler. When the noise canceler is activated, the input from the Input Capture pin (ICP1) is filtered. The filter function requires four successive equal valued samples of the ICP1 pin for changing its output. The Input Capture is therefore delayed by four Oscillator cycles when the noise canceler is enabled.

Bit 6 – ICES1: Input Capture Edge Select

This bit selects which edge on the Input Capture pin (ICP1) that is used to trigger a capture event. When the ICES1 bit is written to zero, a falling (negative) edge is used as trigger, and when the ICES1 bit is written to '1', a rising (positive) edge will trigger the capture.

When a capture is triggered according to the ICES1 setting, the counter value is copied into the Input Capture Register (ICR1). The event will also set the Input Capture Flag (ICF1), and this can be used to cause an Input Capture Interrupt, if this interrupt is enabled.

When the ICR1 is used as TOP value (see description of the WGM1[3:0] bits located in the TCCR1A and the TCCR1B Register), the ICP1 is disconnected and consequently the Input Capture function is disabled.

Bits 3, 4 – WGM12, WGM13: Waveform Generation Mode

Refer to [TCCR1A](#).

Bits 0, 1, 2 – CS10, CS11, CS12: Clock Select 1 [n = 0..2]

The three Clock Select bits select the clock source to be used by the Timer/Counter. Refer to [Figure 20-10](#) and [Figure 20-11](#).

Table 20-7. Clock Select Bit Description

CS12	CS11	CS10	Description
0	0	0	No clock source (Timer/Counter stopped).
0		1	clk _{I/O} /1 (No prescaling)
0	1	0	clk _{I/O} /8 (From prescaler)
0	1	1	clk _{I/O} /64 (From prescaler)
1	0	0	clk _{I/O} /256 (From prescaler)
1	0	1	clk _{I/O} /1024 (From prescaler)

CS12	CS11	CS10	Description
1	1	0	External clock source on T1 pin. Clock on falling edge.
1	1	1	External clock source on T1 pin. Clock on rising edge.

20.14.3. TC1 Control Register C

Name: TCCR1C

Offset: 0x82

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
	FOC1A	FOC1B						
Access	R/W	R/W						
Reset	0	0						

Bit 7 – FOC1A: Force Output Compare for Channel A

Bit 6 – FOC1B: Force Output Compare for Channel B

The FOC1A/FOC1B bits are only active when the WGM1[3:0] bits specifies a non-PWM mode. When writing a logical one to the FOC1A/FOC1B bit, an immediate compare match is forced on the Waveform Generation unit. The OC1A/OC1B output is changed according to its COM1x[1:0] bits setting. Note that the FOC1A/FOC1B bits are implemented as strobes. Therefore it is the value present in the COM1x[1:0] bits that determine the effect of the forced compare.

A FOC1A/FOC1B strobe will not generate any interrupt nor will it clear the timer in Clear Timer on Compare match (CTC) mode using OCR1A as TOP. The FOC1A/FOC1B bits are always read as zero.

20.14.4. TC1 Counter Value Low byte

Name: TCNT1L

Offset: 0x84

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
	TCNT1L[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – TCNT1L[7:0]: Timer/Counter 1 Counter Value Low byte

The two Timer/Counter I/O locations (TCNT1H and TCNT1L, combined TCNT1) give direct access, both for read and for write operations, to the Timer/Counter unit 16-bit counter. To ensure that both the high and low bytes are read and written simultaneously when the CPU accesses these registers, the access is performed using an 8-bit temporary High Byte Register (TEMP). This temporary register is shared by all the other 16-bit registers. Refer to [Accessing 16-bit Registers](#) for details.

Modifying the counter (TCNT1) while the counter is running introduces a risk of missing a compare match between TCNT1 and one of the OCR1x Registers.

Writing to the TCNT1 Register blocks (removes) the compare match on the following timer clock for all compare units.

20.14.5. TC1 Counter High byte

Name: TCNT1H
Offset: 0x85
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	TCNT1H[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – TCNT1H[7:0]: Timer/Counter 1 High byte
Refer to [TCNT1L](#).

20.14.6. Input Capture Register 1 Low byte

Name: ICR1L

Offset: 0x86

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
	ICR1L[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – ICR1L[7:0]: Input Capture 1 Low byte

The Input Capture is updated with the counter (TCNT1) value each time an event occurs on the ICP1 pin (or optionally on the Analog Comparator output for Timer/Counter1). The Input Capture can be used for defining the counter TOP value.

The Input Capture Register is 16-bit in size. To ensure that both the high and low bytes are read simultaneously when the CPU accesses these registers, the access is performed using an 8-bit temporary High Byte Register (TEMP). This temporary register is shared by all the other 16-bit registers. Refer to [Accessing 16-bit Registers](#) for details.

20.14.7. Input Capture Register 1 High byte

Name: ICR1H
Offset: 0x87
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	ICR1H[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – ICR1H[7:0]: Input Capture 1 High byte
Refer to [ICR1L](#).

20.14.8. Output Compare Register 1 A Low byte

Name: OCR1AL

Offset: 0x88

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
	OCR1AL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – OCR1AL[7:0]: Output Compare 1 A Low byte

The Output Compare Registers contain a 16-bit value that is continuously compared with the counter value (TCNT1). A match can be used to generate an Output Compare interrupt, or to generate a waveform output on the OC1x pin.

The Output Compare Registers are 16-bit in size. To ensure that both the high and low bytes are written simultaneously when the CPU writes to these registers, the access is performed using an 8-bit temporary High Byte Register (TEMP). This temporary register is shared by all the other 16-bit registers. Refer to [Accessing 16-bit Registers](#) for details.

20.14.9. Output Compare Register 1 A High byte

Name: OCR1AH

Offset: 0x89

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
	OCR1AH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – OCR1AH[7:0]: Output Compare 1 A High byte

Refer to [OCR1AL](#).

20.14.10. Output Compare Register 1 B Low byte

Name: OCR1BL

Offset: 0x8A

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
	OCR1BL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – OCR1BL[7:0]: Output Compare 1 B Low byte

Refer to [OCR1AL](#).

20.14.11. Output Compare Register 1 B High byte

Name: OCR1BH

Offset: 0x8B

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
	OCR1BH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – OCR1BH[7:0]: Output Compare 1 B High byte

Refer to [OCR1AL](#).

20.14.12. Timer/Counter 1 Interrupt Mask Register

Name: TIMSK1

Offset: 0x6F

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
			ICIE			OCIEB	OCIEA	TOIE
Access			R/W			R/W	R/W	R/W
Reset			0			0	0	0

Bit 5 – ICIE: Input Capture Interrupt Enable

When this bit is written to '1', and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Counter1 Input Capture interrupt is enabled. The corresponding Interrupt Vector is executed when the ICF Flag, located in TIFR1, is set.

Bit 2 – OCIEB: Output Compare B Match Interrupt Enable

When this bit is written to '1', and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Counter Output Compare B Match interrupt is enabled. The corresponding Interrupt Vector is executed when the OCFB Flag, located in TIFR1, is set.

Bit 1 – OCIEA: Output Compare A Match Interrupt Enable

When this bit is written to '1', and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Counter Output Compare A Match interrupt is enabled. The corresponding Interrupt Vector is executed when the OCFA Flag, located in TIFR1, is set.

Bit 0 – TOIE: Overflow Interrupt Enable

When this bit is written to '1', and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Counter 1 Overflow interrupt is enabled. The corresponding Interrupt Vector is executed when the TOV Flag, located in TIFR1, is set.

20.14.13. TC1 Interrupt Flag Register

When addressing I/O Registers as data space using LD and ST instructions, the provided offset must be used. When using the I/O specific commands IN and OUT, the offset is reduced by 0x20, resulting in an I/O address offset within 0x00 - 0x3F.

Name: TIFR1

Offset: 0x36

Reset: 0x00

Property: When addressing as I/O Register: address offset is 0x16

Bit	7	6	5	4	3	2	1	0
			ICF			OCFB	OCFA	TOV
Access			R/W			R/W	R/W	R/W
Reset			0			0	0	0

Bit 5 – ICF: Timer/Counter1, Input Capture Flag

This flag is set when a capture event occurs on the ICP1 pin. When the Input Capture Register (ICR1) is set by the WGM1[3:0] to be used as the TOP value, the ICF Flag is set when the counter reaches the TOP value.

ICF is automatically cleared when the Input Capture Interrupt Vector is executed. Alternatively, ICF can be cleared by writing a logic one to its bit location.

Bit 2 – OCFB: Timer/Counter1, Output Compare B Match Flag

This flag is set in the timer clock cycle after the counter (TCNT1) value matches the Output Compare Register B (OCR1B).

Note that a Forced Output Compare (FOCB) strobe will not set the OCF1B Flag.

OCFB is automatically cleared when the Output Compare Match B Interrupt Vector is executed. Alternatively, OCF1B can be cleared by writing a logic one to its bit location.

Bit 1 – OCFA: Timer/Counter1, Output Compare A Match Flag

This flag is set in the timer clock cycle after the counter (TCNT1) value matches the Output Compare Register A (OCR1A).

Note that a Forced Output Compare (FOCA) strobe will not set the OCF1A Flag.

OCFA is automatically cleared when the Output Compare Match A Interrupt Vector is executed. Alternatively, OCF1A can be cleared by writing a logic one to its bit location.

Bit 0 – TOV: Timer/Counter1, Overflow Flag

The setting of this flag is dependent of the WGM1[3:0] bits setting. In Normal and CTC modes, the TOV1 Flag is set when the timer overflows. Refer to the Waveform Generation Mode bit description for the TOV Flag behavior when using another WGM1[3:0] bit setting.

TOV1 is automatically cleared when the Timer/Counter 1 Overflow Interrupt Vector is executed. Alternatively, TOV1 can be cleared by writing a logic one to its bit location.