Aman Hussain

Roll No.:M23EEV002
M.Tech - Intelligent VLSI Systems
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Education

Degree/Certificate	Institute/Board	CGPA/Percentage	Year
M.Tech.	Indian Institute of Technology, Jodhpur, Rajasthan	8.27	2023-2025
B.Tech.	Barak Valley Engineering College, Karimganj, Assam	79.09%	2017-2021
Senior Secondary	AHSEC Board	78.8%	2016
Secondary	SEBA Board	83.3%	2014

Projects

- **Design of In-Memory Multi-Bit Multiplication and Accumulation for Neural Network Acceleration** *Github*
  Associated with IIT Jodhpur, Rajasthan
  – **Outline**: The novel in-memory MAC design integrated into a 6T SRAM array offers a promising solution for neural network acceleration, with scope for future enhancements in accuracy and adaptability through linearity and transistor optimization. This work is carried out using Cadence Virtuoso.

- **System Verilog FIFO Design and Constrained Random Verification with Scoreboard and Monitor** *Github*
  Associated with IIT Jodhpur, Rajasthan
  – **Outline**: This project implements and verifies an 8-bit, 16-depth FIFO using SystemVerilog with constrained-random verification on EDA Playground. The testbench consists of Transaction, Generator, Driver, Monitor, Scoreboard, and Environment, using a mailbox for communication. The simulation ensures correct FIFO functionality by validating write/read operations, handling full/empty conditions, and detecting errors using a scoreboard.

- **Design and Verification of APB Protocol-Based Communication System Using Verilog** *Github*
  Associated with IIT Jodhpur, Rajasthan
  – **Outline**: This project focuses on the design and simulation of the AMBA APB (Advanced Peripheral Bus) protocol using Verilog HDL. The implementation includes modules for APB master, APB slave, and top-level integration. The design ensures proper read/write transactions, signal handshaking (psel, penable, pready), and address/data handling (paddr, pwdata, prdata) as per the APB specification.

- **Physical Design Flow for RISC-V: A Case Study with PicoRV32A** *Github*
  Associated with VLSI System Design, Bangalore
  – **Outline**: Completed ASIC flow from RTL to GDSII for PicoRV32A, including synthesis, place and route, and timing analysis. This work is carried out using Openlane flow.

Technical Skills

–**Programming Languages and Scripting**: Verilog, System Verilog*, Shell scripting*

–**Tools**: Xilinx Vivado, EDA Playground, Cadence Virtuoso, Openlane Flow, XSchem, NgSpice

–**Operating System**: Windows, Linux

** Elementary proficiency*

Relevant Coursework and Certifications

–Digital VLSI Design, IIT Jodhpur

–Digital ASIC Lab, IIT Jodhpur

–Analog IC Design, IIT Jodhpur

–Digital VLSI SoC Design and Planning, VLSI System Design

–Static Timing Analysis - 1, 2 by Kunal Ghosh, Udemy

–In-memory Computing, IIT Jodhpur

Positions of Responsibility

–**Sports Secretary**: Students' Union, BVEC (Apr. 2019 - Apr. 2020)