

Microprocessor

There are two way for Binary Addition

1) Normal Binary Addition

2) BCD Addition (Binary Coded Decimal No)

1) Normal Binary Addition

Input		Output	
A	B	sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

2) BCD Addition: These BCD Start from 0 and end with 9. They do not have any base

Number System

- 1) Decimal \rightarrow 10
- 2) Binary \rightarrow 2
- 3) Octal \rightarrow 8
- 4) Hexa decimal \rightarrow 16

- All of the instruction in Microprocessor written with hexa decimal no.
- Most of the system relates binary no. from any types of no. because binary no can easily be converted in octal no. as well as hexa decimal

$(100 \cdot 973)_{10}$

$$\begin{array}{r}
 2 | 100 \\
 2 | 50 - 0 \\
 2 | 25 - 0 \\
 2 | 12 - 1 \\
 2 | 6 - 0 \\
 2 | 3 - 0 \\
 \hline
 & 1 - 1
 \end{array}
 \quad
 \begin{array}{r}
 \cdot 973 \\
 \times 2 \\
 \hline
 1.946 \\
 \times 2 \\
 \hline
 1.892 \\
 \times 2 \\
 \hline
 1.784
 \end{array}$$

$(1100100 \cdot 111)_2$

$$\begin{array}{r}
 8 | 100 \\
 8 | 12 - 4 \\
 \hline
 & 1 - 4
 \end{array}
 \quad
 \begin{array}{r}
 \cdot 973 \\
 \times 8 \\
 \hline
 7.784 \\
 \times 8 \\
 \hline
 6.272
 \end{array}$$

$(114 \cdot 76)_8$

$$\begin{array}{r}
 -16 | 100 \\
 | 6 - 4
 \end{array}
 \quad
 \begin{array}{r}
 \cdot 973 \\
 \times 16 \\
 \hline
 5.858
 \end{array}$$

$(64 \cdot 50)_{16}$

$\rightarrow 100 + 973$

$$\begin{array}{r}
 0001\ 0000\ 0000 \\
 1001\ 0111\ 0011 \\
 \hline
 1010\ 0111\ 0011 \\
 0110 \\
 \hline
 1000\ 0111\ 0011 \\
 1073
 \end{array}$$

1073

Rules :- 1) When result of two no after normal binary addition is greater than 9 then 6 will be added.

- 2) If Result of two no less than 9 and carry will generate then 6 will be added.
- 3) If result of two no less than or equals 9 and carry will generate result will be same.

$$\begin{array}{r}
 \cancel{5} \cancel{7} 7 + 4 8 9 \\
 517 \quad 0 101 \overset{0}{\cancel{1}} \overset{1}{\cancel{1}} \overset{1}{\cancel{1}} \overset{1}{\cancel{1}} \overset{1}{\cancel{1}} \\
 489 \quad 0 100 \overset{1}{\cancel{0}} \overset{0}{\cancel{0}} \overset{0}{\cancel{0}} \overset{1}{\cancel{0}} \overset{0}{\cancel{1}} \\
 \hline
 & 1 0 10 0 000 0 000 \\
 & 0 110 0 110 0 110 \\
 \hline
 & 1 0 000 \underline{0} 110 \underline{0} 110 \\
 & 1 0 6 6
 \end{array}$$

→ Subtraction :- In ~~7~~ way subtraction can be done

1) Normal Binary Subtraction

Input Output

A - B Difference Borrow

0 0 0 0

0 1 1 1

1 0 1 0

1 1 0 0

2) 1's Complement Subtraction & Also Known as inversion

45 - 15

$\frac{32}{16} \frac{8}{4} \frac{2}{1}$

45 100101

101101

101101

15 001101

001111

110000

001111

101101

101101

$$\begin{array}{r} 1011101 \\ + 1 \\ \hline 1011110 \end{array}$$

2	30	32 16 8 4 2
2	15 - 0	0 11110
2	7 - 1	
2	3 - 1	
	1 - 1	

Q's Complement

64 32 16 8 4 2

BCD Subtraction \rightarrow Q's & 10's Complements are used in BCD subtraction.

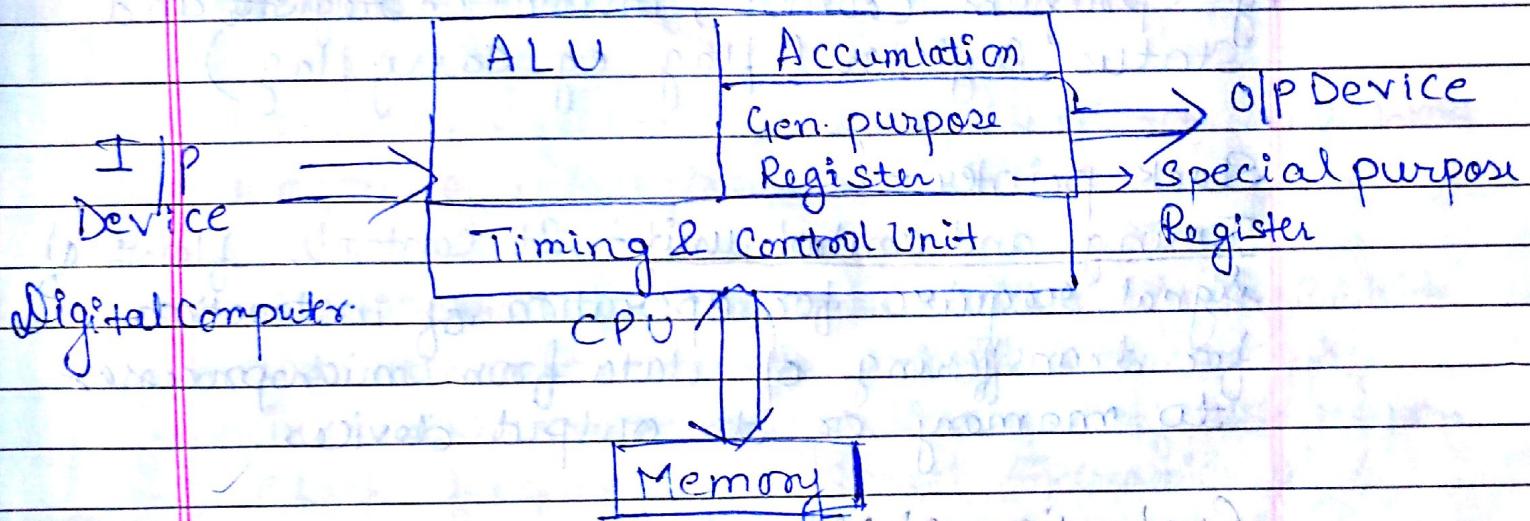
Microprocessor: 8085 is the most popular microprocessor in 8 bit series because it is fastest microprocessor because of NMOS Technology (N-channel Metal Oxide Semiconductor). In NMOS Current Conduction is only due to electrons. 8 bit microprocessor means 8 bit data can be executed at a time. For more than 8 bit first function related with first 8 bit after execution of first 8 bit another 8 will be executed means time level increase for more than 8 bit executed therefore of this region it operates at frequency of 3.07 megahz.

Another advantages is that it operate at

power supply of +5V

- One more advantage of 8085 it is compatible with TTL logical family
- It is 40 pin IC package Earlier Microprocessors intel 8080 uses p-n-p technology because of this 8080 is not studied.
- One more disadvantage is that it requires 3 power supply for its operation and it is not compatible with TTL Technology.

General Architecture of 8085+



ALU stands for Arithmetic and Logical Unit. All Arithmetic operations e.g. subtraction, addition and logical operations are performed using ALU. Apart from these ALU also performs rotation, shifting, clearing and refreshing.

Accumulator: It is the primary register of 8085. All the operations performed by ALU gives result that result is stored in Accumulator and also operations are performed.

using Accumulator

- General purpose Register: 8085 having 6 general purpose register. Each of 8 bit long (BCDEHL)
It is used for temporary storage during execution of instruction
- Special purpose Register: The Register are used by Microprocessor itself. User cannot use these Register
eg: program Counter, instruction register and Status Register (flag eg carry flag)
- Stack pointer:
- Timing and Control unit: It controls flows of signal require for operation of instruction for transferring of data from microprocessor to memory or to output devices.

Evaluation of Microprocessor:

Intel 4004 was first microprocessor based upon pmos technology. It was of 4 bit processing speed was very slow than 8 bit microprocessor was again developed by intel 8080 & 8085, 8080 was pMOS and 8085 based on N-MOS.

Intel then introduce 16 bit microprocessor 8086, 8088 and 80186 these 16 bit microprocessor were very fast because of VLSI Technology.

VLSI uses C-MOS logic family (complimentary metal Oxide semiconductor)

In this technology for designing any logic CKT there is need of Resister

Registers are passive elements and register design by active element. If register will not be used in the circuit having effect will be zero.

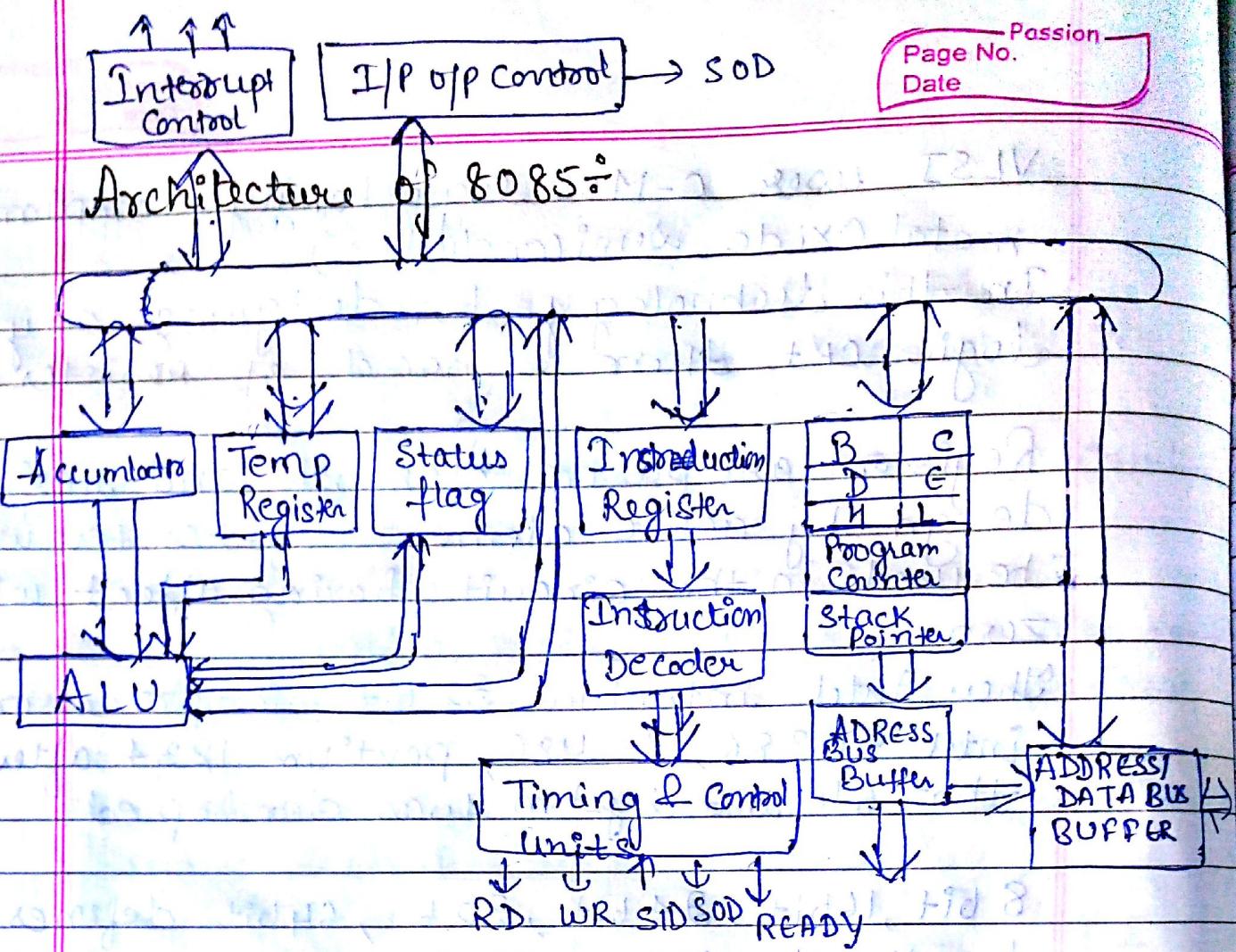
Then Intel introduce 32 bit microprocessors intel 80386, 80486, pentium 1, 2, 3, 4 after that 64 bit system was developed.

8 bit, 16 bit, 32 bit, 64 bit defines word length of microprocessor.

8 bit = 1 byte

32 bit microprocessors will perform 32 bit data at a time speed will increase by increasing word length because of this reason clock frequency or speed operation of microprocessor for different bits.

Intel	Year	Speed of operation	Bitwise	Memory
4004	1971	750 K Hertz	4 bit	1 Kilobyte
8085	1976	3.07 Megahertz	8 bit	64 Kb
8086	1982	5-10 MHz	16 bit	1 Megabyte
8086, 80386	1985	6-12 MHz, 20-33 MHz	16 bit	16 Mb
80486	1989	25-300 MHz	32 bit	4 gigabytes
pentium 1	1993	60-200 MHz	32 bit	4 gb
pentium 2	1997	230-400 MHz	32 bit	4-6 GB
pentium 3, 4	2000	upto 1.3 GHz, upto 1.3-1.5 GHz	32 bit	4-6 GB
Itanium	2001	upto 3 GHz	64 bit	4-12 GB



Registers:

- (1) Simple register (main register)
 - (2) General purpose register
 - (3) Special function register
 - (4) Other register
- Simple register/
- (1) Accumulator + (1) 8 bit
 - (2) Used as a register for storing one data when two^{no} are arithmetically and logically operated
 - (3) After ALU operation result is also stored in accumulator
 - (4) When single no is to be logically operated only accumulator is used as a storage as well as storing result after execution

- ② General purpose register: B, D, E, C, D, E, H & L are used as General purpose registers.
- ③ Each 8 bit long
- ④ Pairing can also be done in a standard way to stored 16 bit data
eg (B-C, D-E, H-L)
- ⑤ H-L pair is an exceptional pair which is used as a memory pointer to locate an address.
LXI H, 200H

H recognises H-L pair of general purpose register.

Load 16 bit data immediately in H-L pair. It means 200H is the location of memory where data is stored and it is recalled by an instruction MOV A, M

M locates memory location 200H which is pointed by H-L pair.

Exceptional point in 8085 microprocessor 16 bit additional can only be possible by using an instruction DAD

- ⑥ Special function registers: Stack pointer & Program Counter are two special function registers.
- These are those register which are used only by microprocessor not by user.

- program Counter: It is a 16 bit register used by microprocessor.
- (2) It holds the address of next instruction to be executed. For eg: After execution MOV A, instruction program Counter will be automatically incremented and points next location of memory where another data is stored.

Stack pointer: It is used when interrupt is generated by microprocessor. Interrupt is a command which stops the main program for a moment at that time program Counter location will be stored in a stack and program Counter will be loaded with a new address through which sub routine is called.

Sub-routine is a small program which is used many times by main program. For eg generating delay in main program after execution of each instruction.

Stack: Small memory location acquired by main program in RAM area.

- 4) Others Register: 1) Instruction register
2) Temporary register.

- 1) Instruction Register: 8 bit long
2) Will store opcode of (8 bit) of an instruction.

- 2) Temporary Registers :- i) 8 bit long
- ii) will store data temporarily before execution of instruction
- iii) Instruction Decoder :- Bits generated by instruction register will be decoded by instruction decoder, it means digital signal will be converted in analog signal and these signals will be sent to timing & control unit

Timing & Control Unit :-

Signal generated by T.C.U. will be provided by microprocessor by a controlled way using this unit eg :- RD, WR, SID, SOD

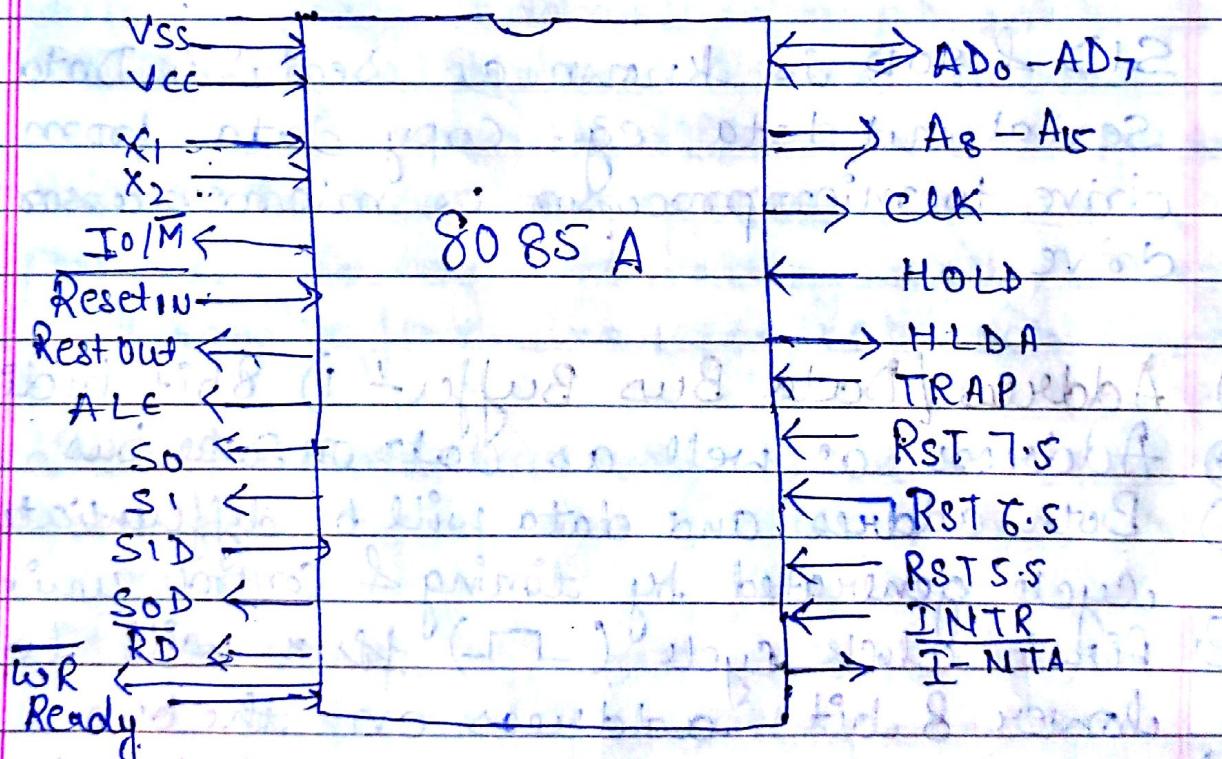
SID & SOD is known as Serial in Data and Serial out data eg :- copy data from pen drive to microprocessor or microprocessor to pen drive

- ③ Address / Data Bus Buffer :- i) 8 bit bidirectional
- ii) Address as well as data on same bus
- iii) Both address and data will be differentiate by clock cycle generated by timing & control unit
- ④ First clock cycle (\overline{RL}) bus will load lower 8 bit address on the bus
- ⑤ Two more clock cycle will load data on address bus : $AD_0 - AD_7$

4) Address BUS Buffer: A₈ - A₁₅ is higher order address bus unidirectional. Address Latch - 74373 will be used as a temporary storage for lower bit of address. If address ^{latch} will high then address is high or vice versa.

. 8085 AH 1 is only microprocessor which operates at 6 MHz because of H + MOS technology.

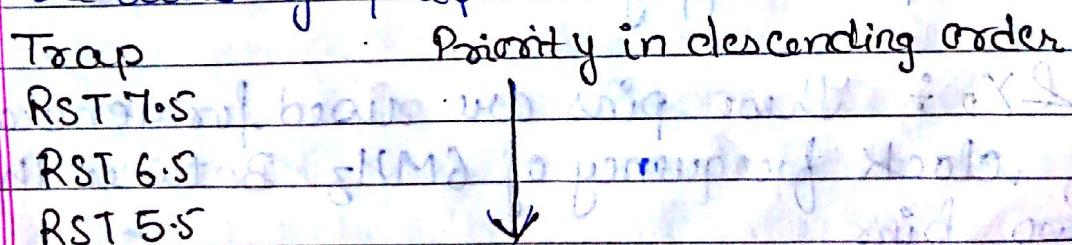
PIN Diagram of 8085: 40 pin IC package with DIP technology
↓ Dual inline



I) A₀-A₇: Address bus bidirectional. In this bus lower 8 bit address as well as the data transfer depending upon timings given by controlled ^{unit} using address latch.

during first clock cycle lower 8 bit address is transferred and two more clock cycles will be required to transfer data on the same bus. When address is transferred lower 8 bit will be stored in temporary register.

- 2) A₈-A₁₅ : This bus carry higher 8 bit address which will be present for all three cycles when lower 8 bit address as well as data is sending in bidirectional bus then 16 bit address will be stored and 8 bit data is transferred. This technique is known as time multiplexing technique because it depends upon time sharing of address and data on bus.
- 3) Clock : This pin generates clock frequency of 3.07 MHz and will be applied to other digital IC's which require some clock pulses.
- 4) (TRAP, RST 7.5, RST 6.5, RST 5.5) : These pins are known as interrupt and also define as hardware interrupt because these are generated through microprocessor. These interrupt are initialised on the basis of priorities.



Interrupts can also be differentiated on the basis of their processing and are known as maskable and non maskable interrupts.

TRAP → Non maskable interrupt

RST 7.5

RST 6.5

RST 5.5

→ Maskable interrupt

Maskable interrupt: There processing can be stopped at anytime. Trap exceptional interrupt because if executed can never be disabled.

→ INTR: Also known as hardware interrupt, processing little bit different. Amongst all interrupt this interrupt have lower priority. When this interrupt activated Program Counter does not increase its content.

→ T-NTA: Interrupt Acknowledge Symbol. Base defined as active low signal. If zero will apply to this pin T-NTA will activated mean acknowledge signal is generated only if interrupt request signal is received by microprocessor.

→ V_{SS}: Ground Signal.

→ V_{CC}: Power Supply +5V

→ X₁ & X₂: These pins are used for generation of clock frequency of 6MHz. Between these two pins

Circuit without any input generate oscillation it work only when output voltage is in phase with input voltage. When output applied to

Input known as positive feedback network

Frequency divider network is required to divide frequency from 6 to 3 MHz.

→ $T_{IO/M}$: This pin is used to define whether address is of memory or input output device.
If this pin is low address is of memory.

IN 01H : At this time input output (I_0/M) pin will be high. i.e. $I_0/M = 1$

→ RESET/IN : Active low signal, this pin when low used to reset the system.

→ RESET/OUT : When high it shows system has been reset.

→ ALE (Address Latch Enable) : When high lower bit address is transferred on the bus and when low data is transferred only using IC 7437.

→ S₀ & S₁ : Known as status signal used to define instruction operation.

S₁

S₀ operation.

0 : OPCODE ODELL op code fetch operation

0 : 0000 1111 for write operation

0 : Read operation

Halt operation (stop)

- SID (serial in Data) & SOD (serial out Data);
These two pin are use for serial operation
for example copy data from pendrive
to computer or computer to pendrive.
- RD : Read operation, Active low , data is easily
recognise from memory if $\overline{RD} = 0$.
- WR : When any operation is performed on
memory for eg moving content from accumulator
to memory.
- READY : When active high show that peripheral
device is high for transferring of data.
- HOLD Signal : This signal when activated show
that when any other device is requesting
for address and data bus , when activated
it release the use of these buses .
- HLDA & Hold request is received by microprocessor.
- Instruction of 8085 :
Instruction is a command given by Computer
to perform specific operation.
8085 microprocessor having 80 instruction sets
Each microprocessor of different Company
having different instruction set. And these
instruction set are not compatible with
each other for eg intel & motorola microprocessor
having their different instruction set .

These are divided into different group:

- 1) Data transfer group
- 2) Arithmetic Group
- 3) Logical Group.
- 4) Branch Control Group.
- 5) Input output & machine Control Group.

1) Data transfer group: Instruction related with transferring, loading, storing and some exceptional instruction related with stack pointer comes under this group for eg MDR, STA, LDA, STHL etc.

2) Arithmetic Group: Instructions related with Arithmetical operation comes under this group. for eg ADD, SUB, increment & decrement.

3) Logical group: Instruction related with logical operation for eg OR, EXOR, AND, Complement etc. Resetting can also be done using logical operation.

4) Branch control Group: Instruction related with Conditional operation comes under this group for eg jump, instruction related with subroutine (CALL & return) and restart instructions (instruction related with Software interrupt).

5) Input output & machine Control Group: All instruction are related with Input & output

ports as well as controlling of machine is also perform or comes under this group. eg IN, OUT, instruction related with enabling and disabling of Interrupt and also Halt operation comes under this group.

Addressing modes of 8085 :- 5 modes comes under this category

- 1) Direct Addressing mode.
- 2) Register Addressing mode
- 3) Indirect Addressing mode
- 4) Immediate Addressing mode
- 5) Implicit Addressing mode

Addressing mode :- These are define as the way of data transferring between register either having direct address or indirect address

- ① Data transferring within the register either direct or indirect
 - ② Operation on data either Self operation means single register will be used for whole of the operation or with the help of another register.
- i) Direct Addressing mode :- Address is given in the given instruction. for eg :- LDA 16 bit Address Load Directly the Contents given by 16 bit address in instruction to accumulator
- ii) Register Addressing mode :- This instruction copy the content of B register to accumulator

3) Indirect Addressing mode: LXI H, 2009H
MOV A, M

XI 2H 200H → This instruction will load 16 bit data in HL pair immediately. Now HL pair will act as a memory pointer which locate memory location in RAM area given by 200H.

MOV A, M: It will copy the content of memory specified by HL pointer into accumulator.

4) Immediate Addressing mode: Data is directly given in the instruction for eg. MVI A, 30H → 8 bit data. It is immediately copied into Accumulator.

5) Implicit Addressing mode: If Data operation is performed by itself (with the help of Accumulator) then known as implicit accumulator.

Accumulator is only register which stores result. For 16 bit operation HL register will be used.

Assignment:

- 1) Perform Data sheet of I₃, I₅, I₇ processors
- 2) Compare Pentium 1, 2, 3, 4 processors
- 3) Differentiate b/w Virtual & Cache memory.
- 4) Explain the Concept of Virtual memory with the help of Diagram.
- 5) Define interrupts why priority is required and how it is done.
- 6) Explain the Sequence that take place when an interrupt occurs.
- 7) As the following memory unit determine no of Address lines, no of pins and no of bytes.

① $64K \times 8$ ② $16M \times 32$ ③ $4G \times 16$ ④ $2K \times 16$

Instruction set of 8085 :- ① Data transfer group :-
MOV instruction can be done either ~~can~~ with
the help of Register or memory

$MOV A, R/M \rightarrow [B, C, D, E, H, L]$

1) from Register to Register $\rightarrow MOV A, R$

2) Register to Memory $\rightarrow MOV M, R$

3) Memory to Register $\rightarrow MOV R, M$

4) Immediate Data transferring MVI A, 8 bit $MVI M, 8 bit$

① $MOV A, R$:- Content of register (B, C, D, E, H, L)
are copied to the contents of accumulator

MOV related with Copy Contents

It means after execution of this instruction

Register R will have same 8 bit data as that of
accumulator data. This mode stored in register is
by addressing mode. No flag will affected

② $MOV M, R$:- This instruction copy the content of
register to memory (whose address is specified
by HI pair), Register indirect mode, No flag
will affected

③ $MOV R, M$:- Copy the content of memory to
register Register indirect, no flag

④ $MVI R, 8 \text{ bit data}$:- This instruction copy 8 bit
data into accumulator and result is store
in register accumulator

Immediate / register indirect No flag

MVT: 11, 8 bit data → 8 bit data directly copied into 8 bit memory. No flag, Immediate / Register - direct.

Store Instruction : Store operation with transferring of data; 16 bit address.

- (1) STA, 16 bit Address
- (2) SHLD, 16 bit Address.
- (3) STAX, rp

1) Flag & TA → 16 bit Address → Contents

→ Direct

STA, 16 bit Addressing mode → flag off activation accumulator contents will transfer to 16 bit address.

No flag is activate, This is of 3 byte instruction. perform opp. function w.r.t loading instruction. This instruction store the SHLD, 16 bit address → No flag will off. Direct Registers.

Content of HL pair transferred to 16 bit address

2) STAX, rp → Indirect, No flag

Content of accumulator transferred to given Register pair (BC, D-E, H-L)

4) Load instruction: These instruction are opposite to Store instruction.

(1) LDA 16 bit Address → Addressing mode → Direct flag. → No flag.

Content of given 16 bit address are transferred to accumulator result store in Accumulator.

(2) LHLD #, 16 bit address → Content of 16 bit address are transferred to H-L pair and result is also stored in H-L pair

No flag, Direct addressing mode

③ LDAX, rp : Contents of Register transferred to accumulator. Register, Direct addressing mode, flag none

④ LXI H, 16 bit data (Exceptional) : 16 bit data is transferred to H-L pair and H-L pair in this instruction act as a memory pointer, Immediate flag none

Exchange instruction :

① XCXH, rp

② XTHL

① XCXH, rp : This instruction will exchange the contents of register pair (B-C & D-E) with the content of H-L pair. Register Addressing mode, No flag
Exchange related with Swaping of content not transferring as well as Copied of Content

② XTHL : Exchange the content of H-L pair with Stack pointer.

③ STHL instruction : This instruction will transfer the content of H-L to stack pointer

Arithmetic instruction :

① ADD R/M } without carry

② A DI 8 bit data }

③ ADC R/M } with carry

④ ACI 8 bit data }

- ① ADD R/M $\frac{8}{8}$
 addressing mode flag instruction
 Register Address #11: Content of Registers / Memory
 mode will be added with Content of accumulator & data stored in accumulator
- ② ADD 8 bit data $\frac{8}{8}$ 8 bit data immediately added to accumulator with this instruction and the result is stored in accumulator. Immediate
- ③ ADC R/M $\frac{8}{8}$ Content of Registers / Memory are added with accumulator through Carry. ~~Carry~~ flag means Carry bit will also be added to accumulator either Set or Reset.
- ④ ACI 8 bit data $\frac{8}{8}$ 8 bit data immediately added with accumulator through carry. Immediate; All flags
- Subtraction: In Subtraction if a accumulator data is less than either register or memory or 8 bit data occurs borrow will generated. Borrow is nothing but again activation of carry flag.

- ① SUB R/M
 ② SUD 8 bit data
 ③ SBB R/M
 ④ SBI 8 bit data

- ① SUB R/M $\frac{8}{8}$
 Addressing Mode: Register Addressing mode Flag: Activation instruction
 Register Addressing mode #11: Activation

During subtraction 3 condition will lies

- ① If $A > R/M$ 8 bit data
- ② If carry flag both will reset
- ③ If $A = R/M$ 8 bit data zero flag will reset
- ④ If $A < R/M$ 8 bit data carry flag will set

Contents of R/M will be subtract from accumulator and flags will effects depending upon above 3 condition and result is stored in accumulator.

- ⑤ SUI 8 bit data \div 8 bit Content will immediately subtracted with Content of accumulator and flag will effect depending upon above condition. Immediate, AU flag.
- ⑥ SBB R/M \div Content of R/M will subtracted from accumulator through carry (Borrow is nothing i.e. is carry) Register Addressing mode, AU flag.
- ⑦ SBI 8 bit data \div 8 bit Content of R/M will immediately subtracted from G through carry (Borrow) Immediate.

Ques 1) Subtract two no - 15 - 20 Using 1's Complement & 2's Complement

(a) $-19(-4)$ Using 1's & 2's complement

(b) design logical gate which will perform all operation
NAND, NOR, NOT

$$-15 + (-20) = -15 - 20$$

(minus 15 → 00101000.10101
 minus 20 → 00100000
0011,0101,

35

Q) $-15 - (-20) = -15 + 20$

$$15 - 0.01111 - 100000$$

$$20 - 10100 - \underline{10100}$$

$$\underline{1100,100}$$

$$+ 1$$

$$\underline{0.0101},$$

$$5$$

$$15 - 01111 - 10000$$

$$20 - 10100 - \underline{01011}$$

$$\underline{11011}$$

$$32.16842$$

$$490 \textcircled{1} 390 \textcircled{2}$$