

MODULE: 01

Microprocessor: [CPU on a single chip]

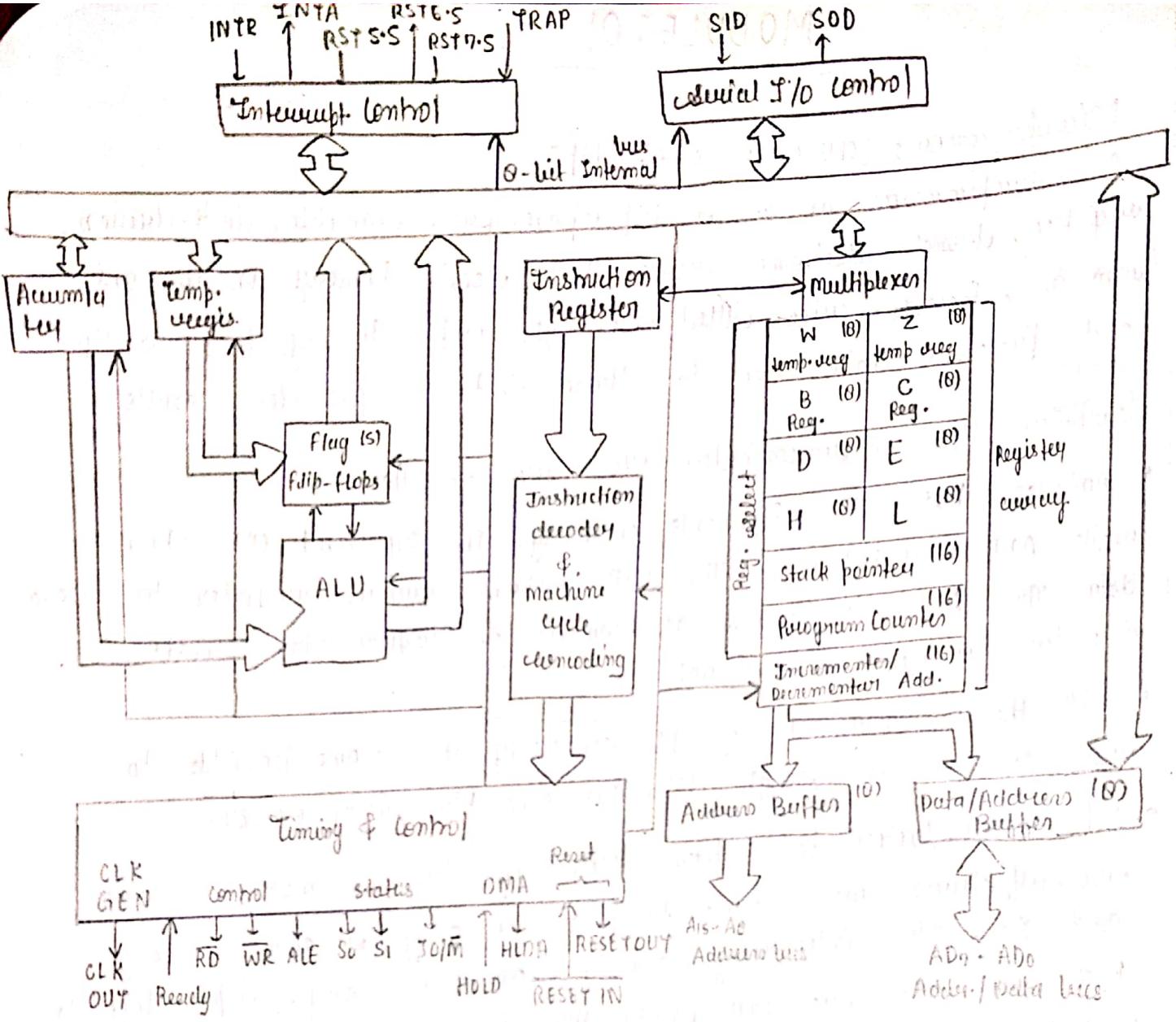
A microprocessor is a multipurpose, programmable, clock-driven, register based electronic device that reads binary instructions from a storage device called memory, accepts binary data as I/p and processes data acc. to those instrn & provides results.

Computer V/S microcomputer V/S micro controller

- Computer has 4 components memory, I/p, O/p and CPU which consists ALU & control unit. The CPU contains various register to store data. The ALU do perform arithmetic & logical operⁿ, instrⁿ, decoder, counters & control lines.
- With the advancement of IC technology it become possible to built CPU on a single chip. This is called microprocessor.
- As semiconductor fabrication technology became more advance manufacturers were able to place not only but also memory and I/p, O/p interfacing circuit on a single chip. This is called microcontroller. MC is essentially a computer on a single chip.

8085 microprocessor —

- It is a 8-bit microprocessor (MP)
- It has 16 transmission lines. [A₁₅ --- A₀ D₇ --- D₀]
- It has 40 pins in its IC.
- It Operates on frequency of 3 MHz.
- Its address bus & data bus are multiplexed (AD₇ - AD₀)
Address bus size is 16 bit (2^{16} location cover at a time).
- Data bus size 8 bit.
- 8085 can cover 64k location because of address size.



- Register block B, C, D, E, H, L, are registers which is given to and used for programming. They are general-purpose registers.
- W, Z are not general purpose registers, it is only to exchange means swap the data. [$DE \leftrightarrow HL$, $HL \rightarrow W$, $DE \rightarrow HL$.]
- Accumulator is used to load data for and used to accumulate the result also it placed at other place)
- Special purpose registers are stack pointer, Queue pointer, program counter, incrementer & decrementer.

Program Counter: Used to store the address of program.

Stack pointer: Registers do hold the address of stack pointer in memory. [only one pointer is required] LIFO.

Back end = insertion, front end = deletion!

Queue pointer: Based on FIFO, same as stack but uses 2 pointers for insertion or deletion.

Implementation & deimplementation: To shift the pointer, used for PUSH & POP operation.

- Multiplexers, used to share the data of registers on data bus.

Address Higher Address Data Address Register part of address
AD₁₅ - AD₈ AD₇ - AD₀

- Temporary register, stores the value of other operand (second Operand).
- Timing & controlling, is the brain of the microprocessor. It generates the signal which type of operation is to be done.
- Flag register, tells the status of current result. It is 8 bit in size.

8	7	6	5	4	3	2	1
S	Z	X	Ac	X	P	X	Cy

sine flag zero don't care Parity auxiliary carry carry

Sine flag: It sets to 1, when the result of two no. is -ve.

zero flag: It sets to 1, when both no. are equal (result 0 on subtraction).

Auxiliary carry: It sets if carry generated at 4th position (after nibble on intermediate carry generated).

Parity: If we send data from sender and it got distorted before reaching to receiver then we just the data if can be check by parity flag.

Carry: If carry generated on MSB they are set to 1.

Interrupt Control: It is an event which disturbs the normal flow of program.

It can be classified into two categories —

1. Maskable interrupt / Hardware interrupt / Vector

2. Non-maskable interrupt / software interrupt / Non-vector.

Maskable: They can be delayed with the help of SIM (Set Interrupt mask) & DI (disable interrupt) instrn.

Non-maskable: They can't be delayed. ex: TRAP (power supply failure)

RST 7.5 "Reset status of"
RST 6.5
RST 5.5 Maskable (SIM). (it sets zero effect of interrupt).
INTR

The priority of these interrupt are —

TRAP > RST 7.5 > RST 6.5 > RST 5.5 > INTR.

Hardware: Such as stack overflow. (RST 5.5).

Software: Such as exception are divided

RST 1 HALT.
RST 2

anyway instr last line

RST 1 HALT.

opcode 76.

RST 7

RE → moves & loads the value of stack pointer.

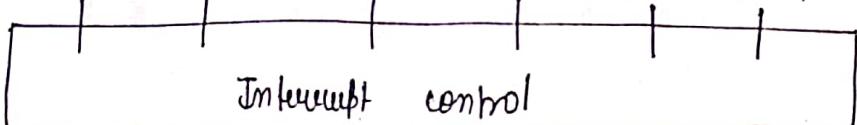
ISR → interrupt service routine.

Vector: if interrupt of address of service routine is fixed.

Non-vector: SR is not known

interrupt
↑ request. acknowledge
↑

INTR INTA RST 7.5 RST 6.5 5.5 TRAP.



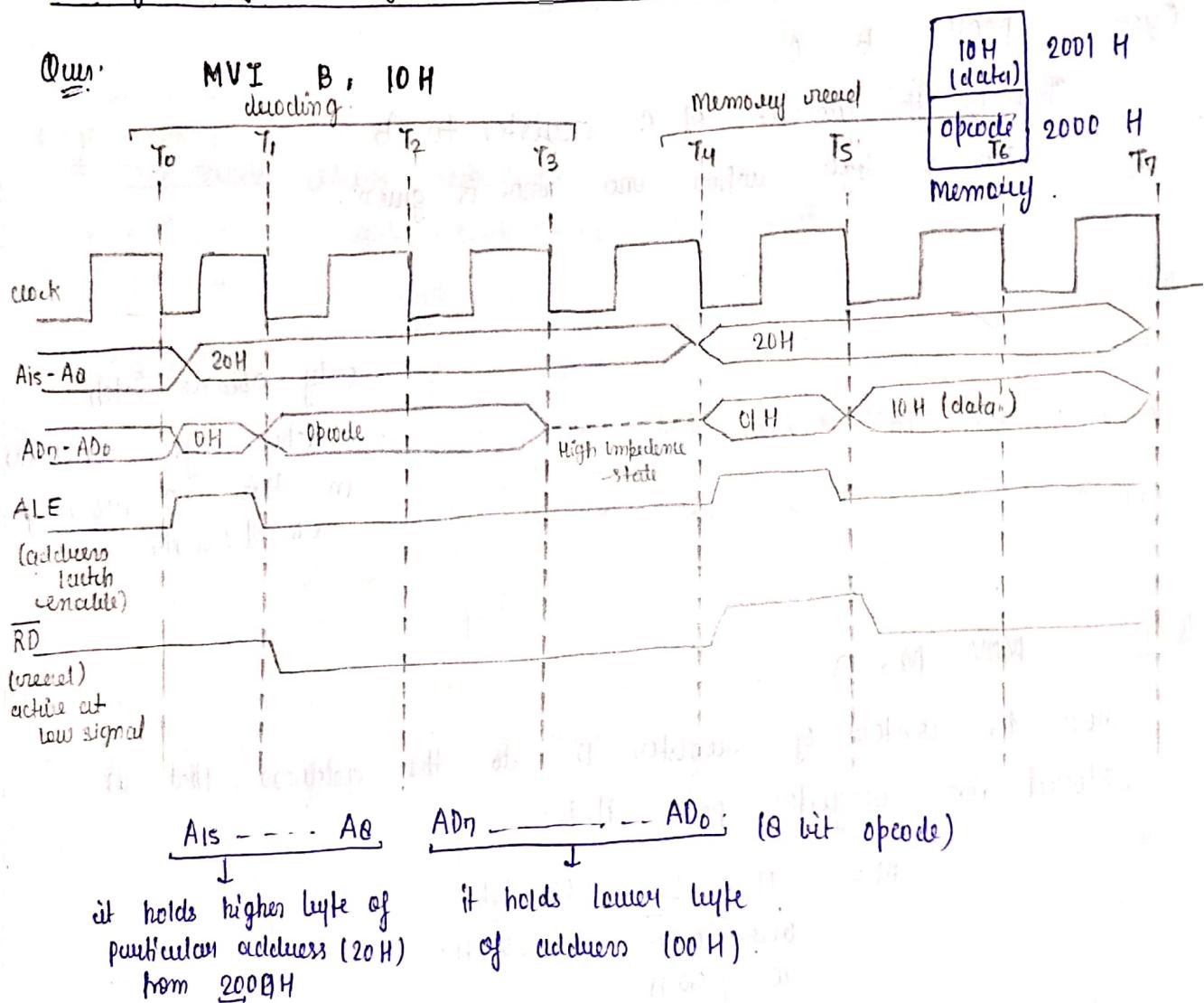
6 pins are available in interrupt.

Instructions: They are of different types —

1. Data transfer instrⁿ (Memory \longleftrightarrow register)
2. Arithmetic instrⁿ (to perform operⁿ)
3. Control instrⁿ (same as go to, JMP)

instrⁿ : MVI Registername 8 bit data.
↓
(Move immediate) 2 byte

Timing diagram of an instrⁿ in 8085 microinstruction



ALE (address latch enable): If ALE signal is high it indicates that the content of A₁₅ to A₀ (bus) is part of address if it is low it indicates content of A₁₅ to A₀ is data.

RD: when it gets low it starts reading opcode and at T₃ it starts decoding opcode at that time no other instrⁿ can access the content of that particular bus (H₁₅S).

Instⁿ cycle: (Memory write)

Opcode fetch & execute cycle
(made up of time period 't_p'
state)

Memory sheet

(3 + state)

T_4, T_5, T_6

Machine cycle: 2 (opcode fetch, memory read)

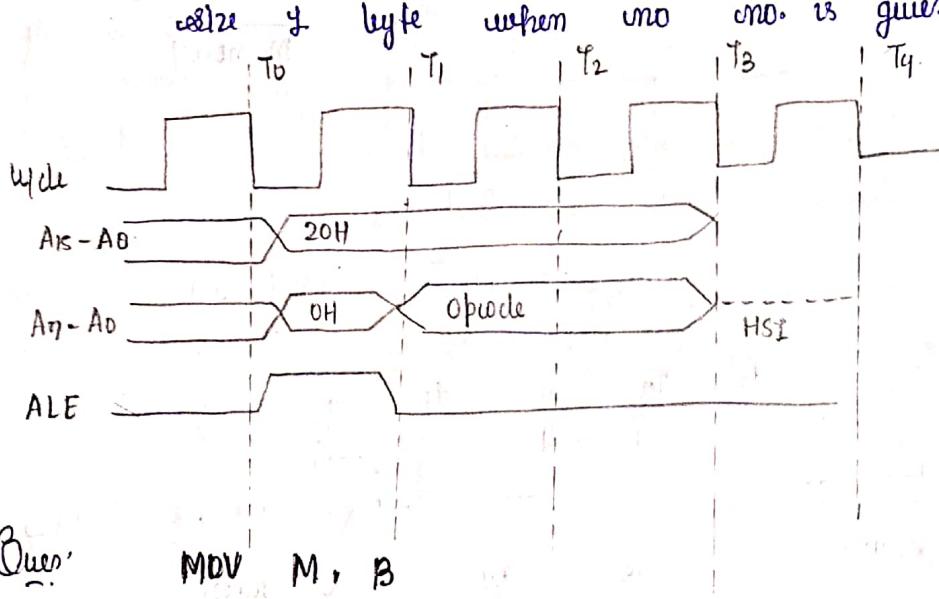
7 state: 4 γ , 3 γ super

Ques. MOV B, C

Transfer the content of C register to 'B'

opcode 200H

else if byte when no one is given.



only opcode fetch
machine cycle executes
in this no memory
read / write.

Ques. MDV M, B

Move the content of register 'B' do the addressers that is

stored in register pair H,L.

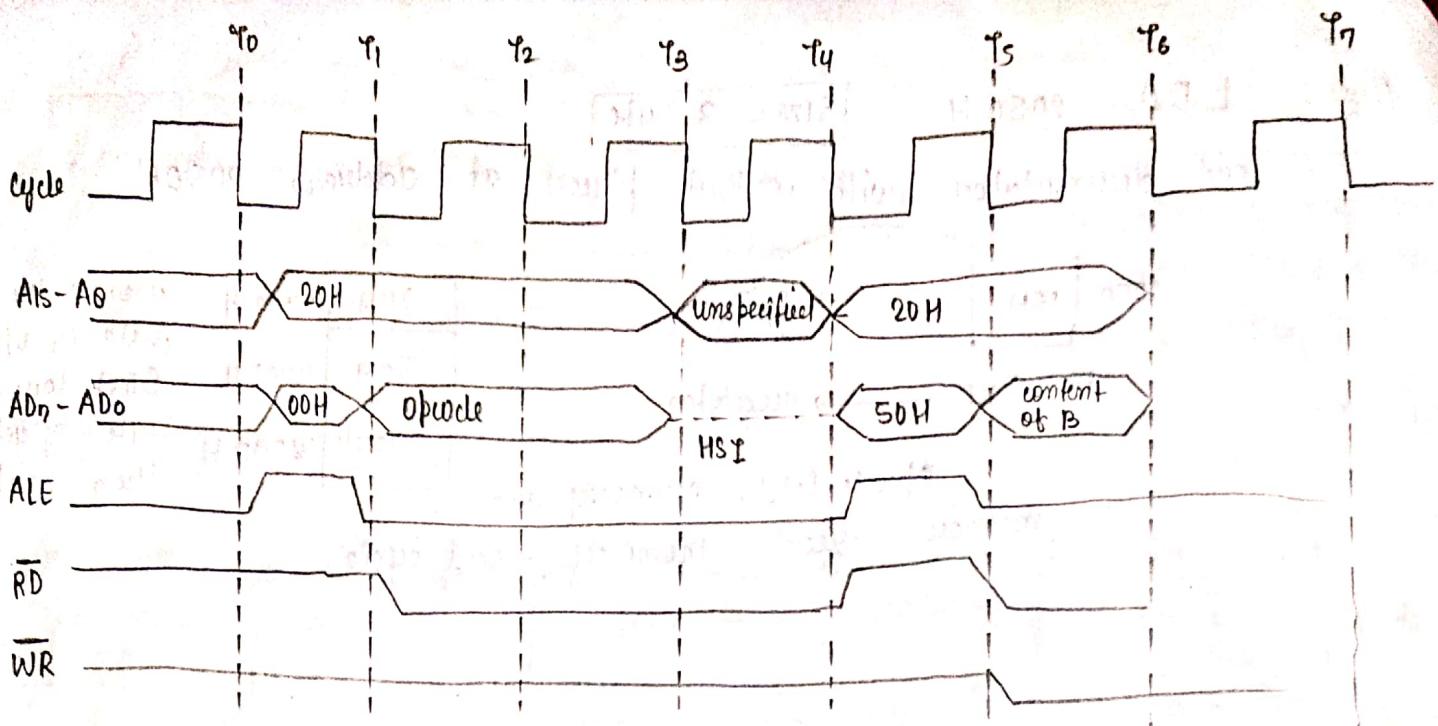
M =	H	L	(16-bit)
	0 bit	0 bit	20 50 H
	20	50 H.	

is it in another of the memory areas?

OProc. fetch - in 2000H

404
H SO₄
OH Ofeide

Memory 11-19 to four digits previously written. 139 Cycle Total.



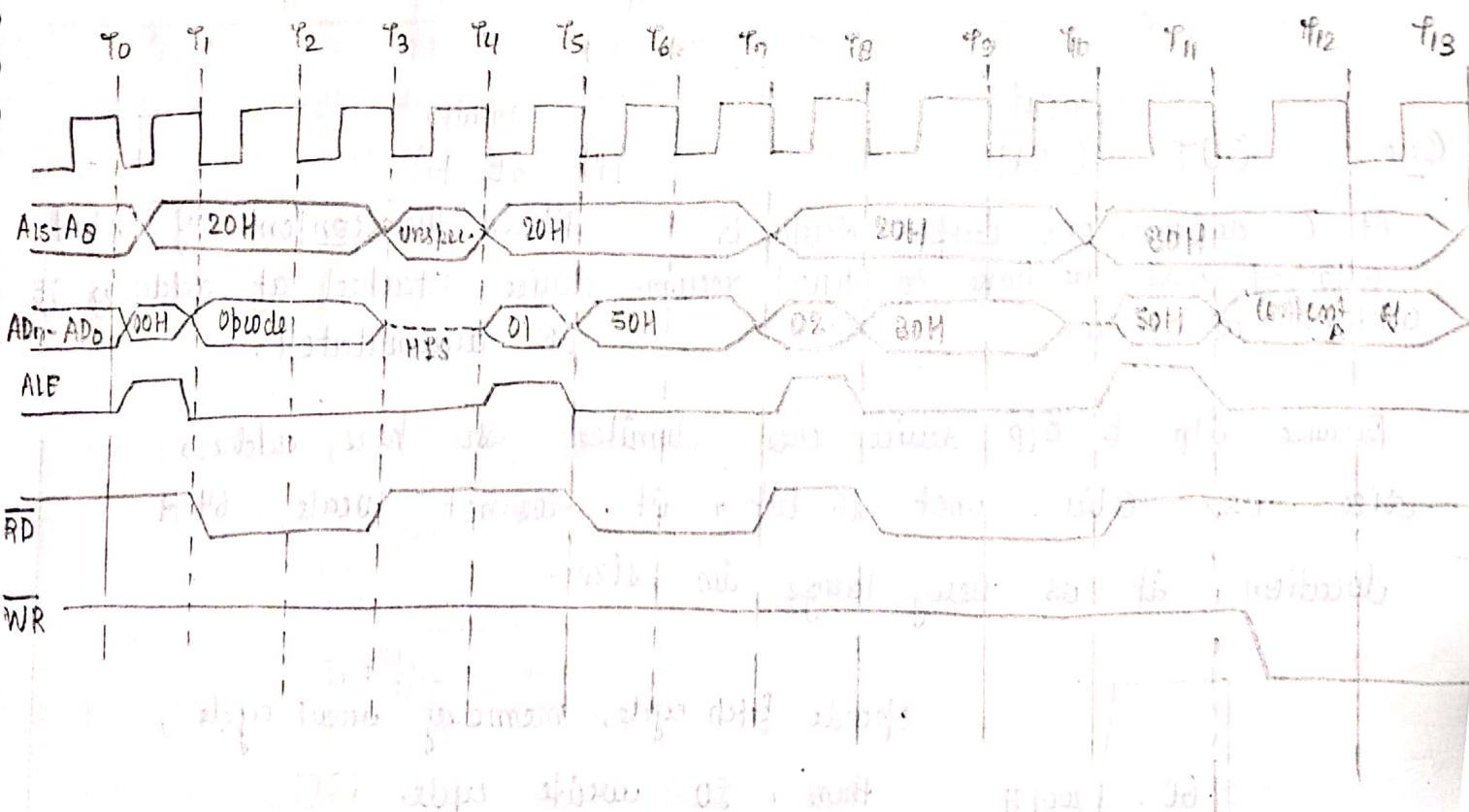
at t_3 , decoder starts decoding.

$t_0, t_1, t_2, t_3 \rightarrow$ opcode fetch cycle.

$t_3 - t_4$ decoding occurs

Ques: STA 3050 H

store the content of accumulator at address 3050.

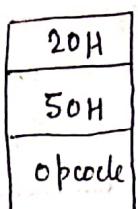
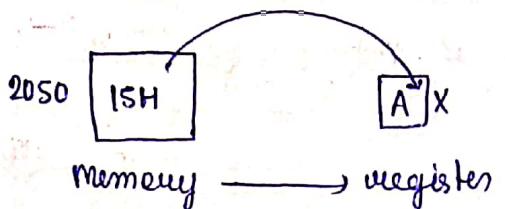


Ques.

L DA 2050 H

Size = 3 byte

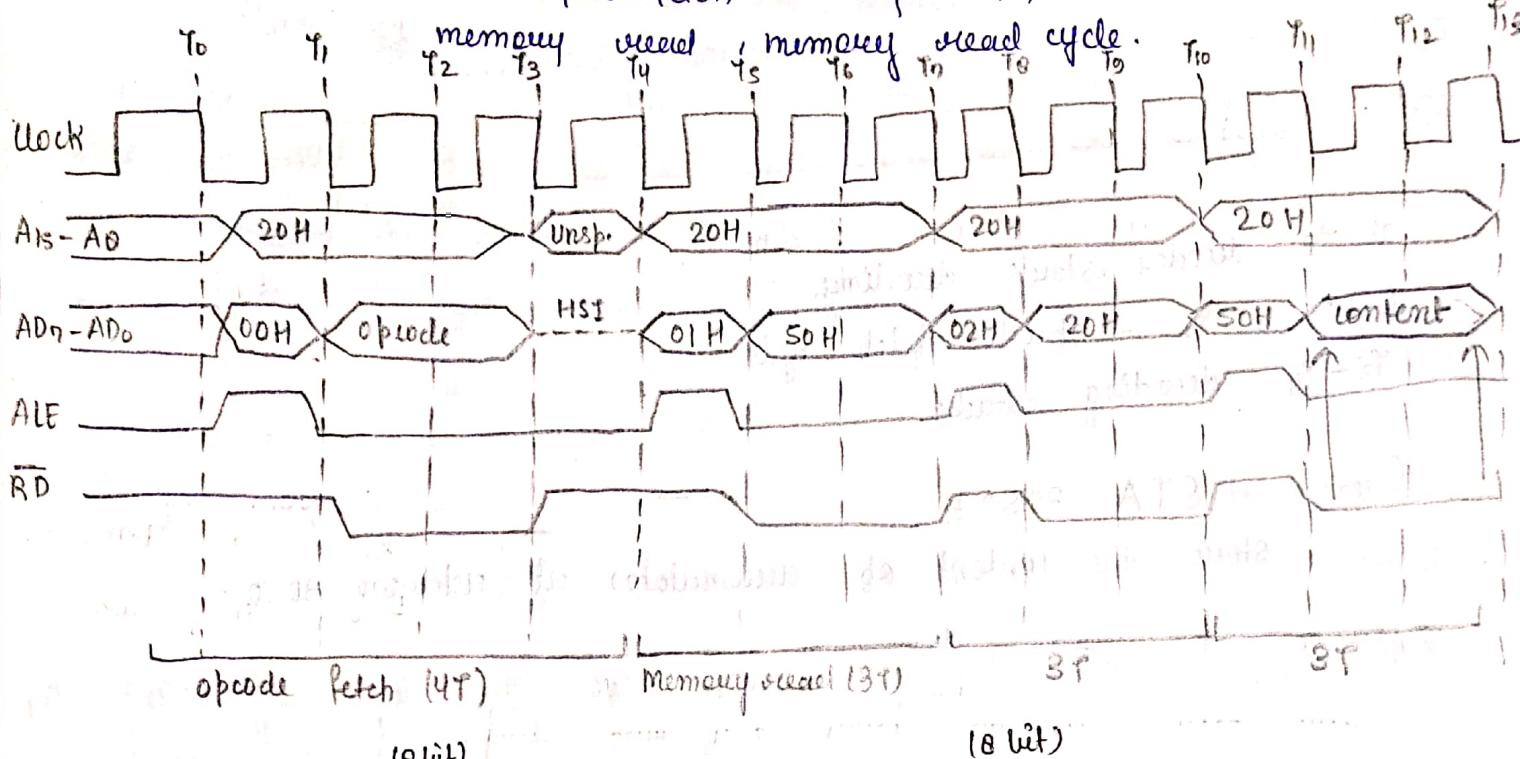
Load accumulator with content placed at address 2050H



2002 H
2001 H
2000 H

User enters instn in kth
feist memory
byte of word
higher.

Opcode fetch, Memory read,



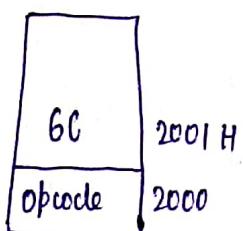
Ques.

OUT 6 CH

IN 6E H

Placed the content of input
At 6C address, one output device is
attached and we have to place accm. device attached at address 6E
content at there.

Because i/p & o/p device are limited so here address
size is 8 bit not 16 bit + it does not locate 64 k
location it is very large in size.

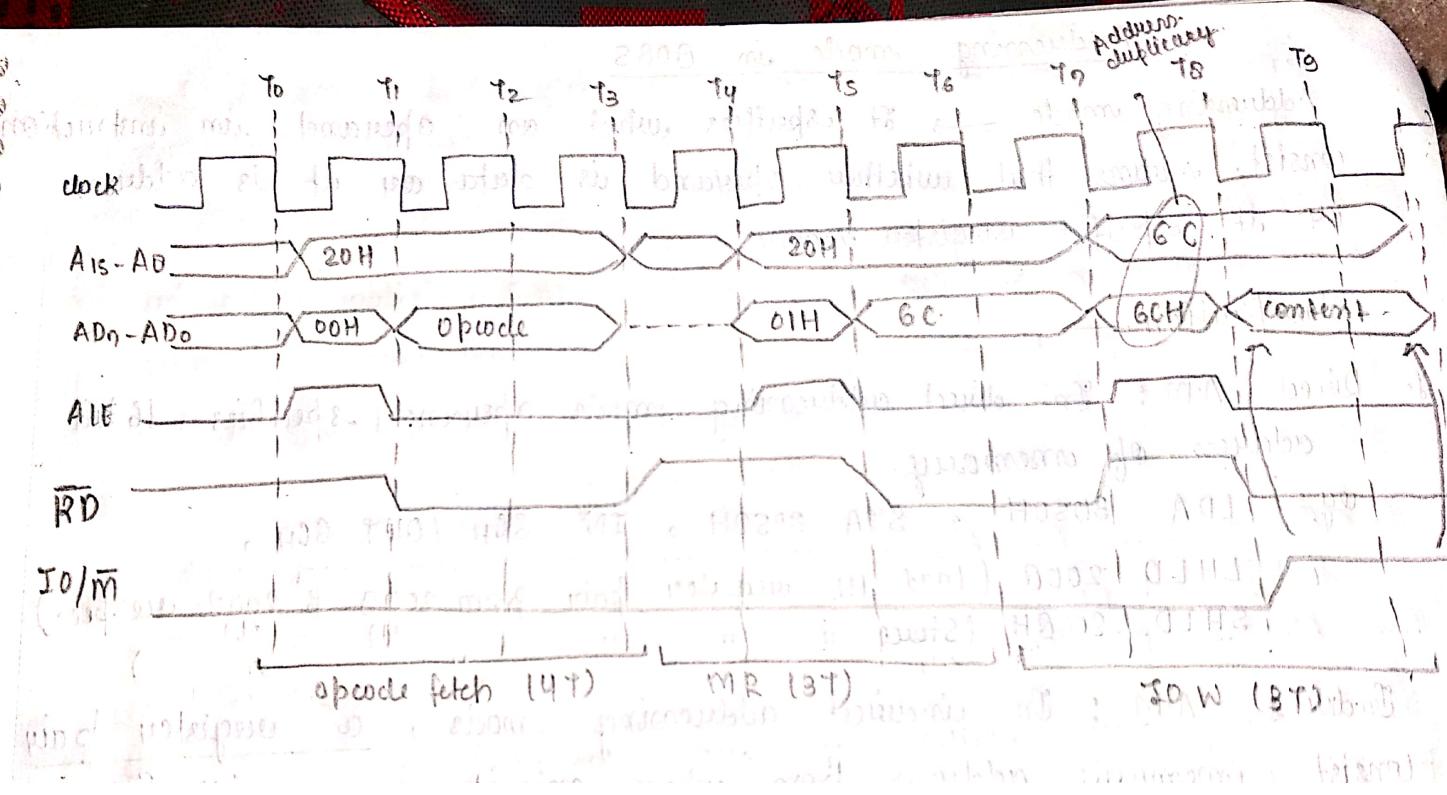


Opcode fetch cycle, memory read cycle,

then 80 write cycle. (3T)

80/m single signal is high.

Address dependency —



Addressing mode in 8085

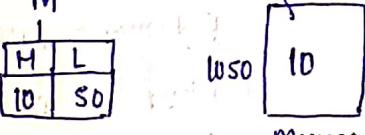
Addressing mode → It specifies what an operand in instruction consist. means that whether operand is data or it is address or it specifies register name.

Classification —

1. Direct A.M : In direct addressing mode operand specifies 16 bit address of memory.

e.g.: LDA 3050H , STA 3050H , IN 6CH / OUT 6CH ,
 LHLD 2000H (Load HL register pair from 2000H & 2008H resp.)
 SHLD 2000H (Store " " " " ")

2. Indirect A.M : In indirect addressing mode, a register pair consists memory address from where microprocessor will fetch data and will transfer data.

e.g.: MOV B M

 , MOV M, B , ADD M
 $A \leftarrow A + M[HL]$
 SUB M
 $A \leftarrow A - M[HL]$

ANA M (and operation with content of HL register pair & store in accumulator), ORA M , XRA M
 $A \leftarrow A \text{ AND } M[HL]$

3. Immediate A.M : In immediate addressing mode, operand specifies 8 bit data or 16 bit data.

e.g.: MVI B, 10H , LXI B, 1050H , ADI 10H (add) $[A \leftarrow A + 10]$
 SUB SUI 10H , ANI 10H $[A \leftarrow A \text{ AND } 10]$

$\begin{array}{r} 10101101 \\ 00010000 \\ \hline 00000000 \end{array}$ (in Hexadecimal)
 (Zero flag affected)

ORI 10H , XRI 10H

$\begin{array}{r} 10101101 \\ 00010000 \\ \hline 10111101 \end{array}$ (Null flag).

4. Register A.M.: In register A.M., operand is specified by register name.

ex: MOV B,C , ADD B , ANA B , ORA B

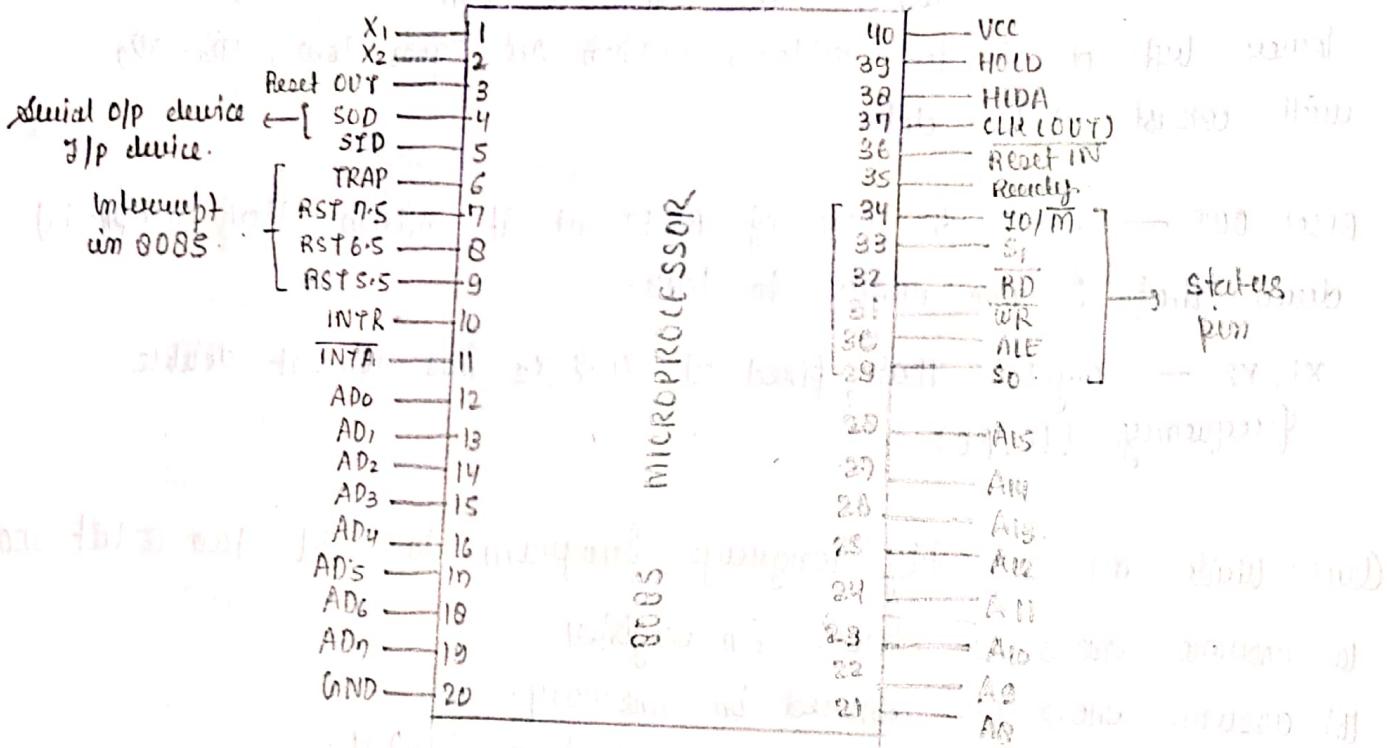
5. Implied / Implicit A.M.: In implied/implicit mode, default is operand is accumulator.

ex: CMA (complement the content of accum.)

$$A \rightarrow 1011100$$

$$CMA \rightarrow 01000110 \quad (4's \text{ comp.})$$

8085 I/O pin diagram



S0/M	S ₁	S ₀	Operation
0	0	0	HALT
0	0	1	memory write
0	1	0	memory read
1	0	1	I/O write
1	1	0	I/O read
0	1	1	opcode fetch
1	1	1	Interrupt acknowledge

Ready - As I/O/p device is ready then it transfers data with help of ready pin any peripheral device inform CPU whether it has been ready to transfer data to I/O or receive data from I/O.

Reset - With the help of Reset IN pin value PC value sets to 0000H.

CLR(OUT) — with the help of clock (out) it informs other device at what frequency CPU is operating (3 MHz).

HLDA / HOLD — whenever a request comes from DMA to microprocessor about releasing the control over the system buses it is being achieved by HOLD pin.

Request from DMA to CPU will be acknowledged by HLDA pin.

Vcc — used to give +5V power supply.

A8 - A15 — Bus A8 - A15 is responsible to transfer higher byte of 16 bit address.

A₀ - A₇ — Bus A₀ - A₇ is considered as a multiplexed bus. It means that when ALE signal is high it will consist lower byte of 16 bit address. When ALE goes low, A₀ - A₇ will consist 8 bit data.

Reset OUT — with the help of RESET out it informs other peripheral device that I am ready to take.

X₁, X₂ — crystal that fixed at X₁ & X₂ has almost double frequency (LC/RC).

Ques. Write an assembly language program to add two 8 bit no. —

(a) assume nos are stored in register.

(b) assume nos are stored in memory.

stored the result at memory location 8050H.

If carry is generated during addition stored carry at memory location 8051H.

(a) MVI B, 10H

MVI D, 20H

MOV A, D

ADD B (without carry)

STA 8050H

HLT

MVI C, 0DH

MVI B, 10H

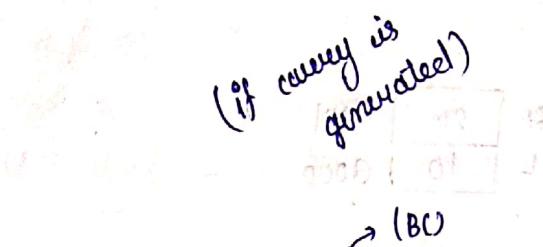
MVI D, 20H

MOV A, D

ADD B

JNC STORE (Jump when carry

INR C flag not set)
(increment)



(b) LXI B, 1050H
immediate 16 bit data not address.

MOV A, C
STA 0051H
HLT

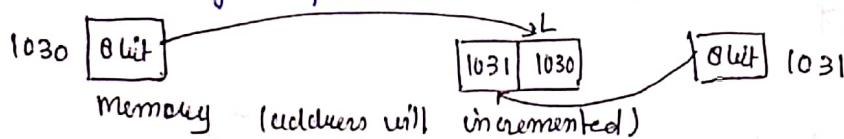
Memory only can store 8 bit data.

LDA 2050H
address (memory \rightarrow accum.)

LDAX (pair) B
 $\begin{array}{|c|c|} \hline B & C \\ \hline 10 & 20 \\ \hline \end{array}$ \rightarrow Address not data

LHLD 1030H

Local HL register pair 1030 is address.



MVI C, 00H

(b) LDA 0000H

MOV B, A

LDA 0001H

ADD B

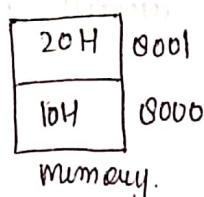
JNC SKIP

JNR C

SKIP 0050H

MOV A, C

STA 0051H



Ques. Write an assembly language program to 16 bit no. No. 1 first no. is stored from address 0000 to 0001 and second no. is stored from 0002 to 0003

Store the result at address 0004 to 0005 and if carry is generated show the carry at address 0006.

MVI B, 00H
 LHLD 0000H
 LDA 0002H
 ADD L.
 STA 0004H
 LDA 0003H
 ADC H (add with carry)
 JNC SKIP
 JMP C, SKIP or NOT
 SKIP STA 0005H
 MOV A, C
 STA 0006H
 HLT

Ans. 1st no. stored in register pair BC and 2nd no. stored in DE and result in HL.

H	20	0001
L	10	0000

H	40	0003
L	36	0002