# ALEXANDER M. MANLEY


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## EDUCATION

Exp. 2025 **Master of Science in Computer Engineering**
**The University of Kansas**
Focus: Computer Architecture and Systems

2023 **Bachelor of Science in Computer Engineering**
**The University of Kansas**
*Dean's List, Undergraduate Research Fellowship, Undergraduate Research Award, Distinction Scholarship*

## SKILLS

**Languages** Python, C++, C, VHDL, Scala, Assembly.

**Software** Cadence Genus, Cadence Innovus, Xilinx Vitis HLS, Xilinx Vivado, KiCAD, gem5, firesim, QEMU.

**Equipment** Multimeter, Function Generator, Oscilloscope, Soldering Station.

## EXPERIENCE

07.2023-Present **Graduate Research Assistant** — **The University of Kansas**
- Utilizing novel large language models and reinforcement learning for generative AI solutions to design space exploration.
- Developing a modern educational training platform to teach computer architecture integrated with gem5 simulation.
- Optimized custom IP to regulate memory accesses to shared LLC - providing defense against denial-of-service cache bank contention attacks in real-time systems.

2023, 2024 Senior Design **Graduate Teaching Assistant** — **The University of Kansas**
- Mentor students to achieve successful projects, ensuring safe environment and productive student collaboration.
- Provide flexible, adaptive advice based on the unique needs and goals of each team.
- Nurture a collaborative environment, fostering critical analysis and solution-oriented teamwork.

08.2020 - 05.2023 **Undergraduate Research Fellow** — **The University of Kansas**
- Applied processing-in-memory (PIM) techniques and alternative write queue models to mitigate the memory bottleneck of high-performance servers.
- Developed FPGA-accelerated FireSim simulation to discover hardware-level bottlenecks of gem5.
- Cross-compiled PARSEC benchmarks for the ARM ISA to run on gem5 full system environment.

## COURSES

- **gem5 Bootcamp**, UC Davis (July 2024), **Building RAG Agents with LLMs**, NVIDIA (Est. Oct 2024), **Hands-On RTL Design**, QuickSilicon (Est. Dec 2024)
- Digital Logic Design, Embedded Systems, Digital Systems Design, Computer Architecture, Operating Systems, Advanced Computer Architecture, Modern Computer Organization and Design, Embedded Machine Learning, Program Synthesis.

## PUBLICATIONS

- C. Sullivan, A. Manley, M. Alian, and H. Yun, **"Per-Bank Bandwidth Regulation of Shared Last-Level Cache for Real-Time Systems,"** 2024 IEEE RTSS.
- J. Umeike, N. Patel, A. Manley, A. Mamandipoor, H. Yun, and M. Alian, **"Profiling gem5 Simulator,"** 2023 IEEE ISPASS.
- N. Taheri, A. Manley, A. R. Pang, and M. Alian, **"Profiling an Architectural Simulator,"** 2022 IEEE ISPASS.

## PROJECTS

Computer Arch **MIPS Single Cycle Processor**
Written in VHDL, I designed registers, functional logic, and control subsystem. The design supports 16 individual operands including arithmetic, data movement, branches, and jump instructions. Through simulation, the processor could successfully compute the Fibonacci sequence recursively, up to the 15th digit.

Embedded **Automated Car**
I developed software for controlling servos and motors using datasheet details and microcontroller specifications. I incorporated UART and I2C communication protocols and leveraged the Raspberry Pi and RISC-V ISA development environment.