



Alexander Manley

Graduate Computer Engineer

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EDUCATION

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|-------------------|--|--------------|
| 08/2023 – 05/2025 | Master of Science in Computer Engineering
<i>University of Kansas</i> <ul style="list-style-type: none">• Focus: Computer Architecture, Hardware Systems, ML for System Design• Advanced Computer Architecture, Modern Computer Organization and Design, Embedded Machine Learning, Program Synthesis | Lawrence, KS |
| 08/2019 – 05/2023 | Bachelor of Science in Computer Engineering
<i>University of Kansas</i> <ul style="list-style-type: none">• Honors: Dean's List, Research Fellowship, 2x Research Award, Distinction Scholarship• Digital Logic Design, Embedded Systems, Digital Systems Design, Computer Architecture, Operating Systems | Lawrence, KS |

SKILLS

Languages

Python, C++, C, VHDL, Scala, Assembly

Software

Cadence Genus, Cadence Innovus, Xilinx Vitis HLS, Xilinx Vivado, KiCAD, gem5, firesim, QEMU

PROFESSIONAL EXPERIENCE

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| 08/2023 – Present | Graduate Research Assistant
<i>University of Kansas</i> <ul style="list-style-type: none">• Utilizing novel large language models and reinforcement learning for generative AI solutions to design space exploration.• Developing a modern educational training platform to teach computer architecture integrated with gem5 simulation.• Optimized custom IP to regulate memory accesses to shared LLC; providing defense against denial-of-service cache bank contention attacks in real-time systems. |
| 08/2023 – Present | Graduate Teaching Assistant
<i>University of Kansas</i> <ul style="list-style-type: none">• Mentor students to achieve successful projects, ensuring a safe environment and productive student collaboration.• Provide flexible, adaptive advice based on the unique needs and goals of each team.• Nurture a collaborative environment, fostering critical analysis and solution-oriented teamwork. |
| 11/2020 – 05/2023 | Undergraduate Research Fellow
<i>University of Kansas</i> <ul style="list-style-type: none">• Applied processing-in-memory (PIM) techniques and alternative write queue models to mitigate the memory bottleneck of high-performance servers.• Developed FPGA-accelerated FireSim simulation to discover hardware-level bottlenecks of gem5.• Cross-compiled PARSEC benchmarks for the ARM ISA to run on gem5 full system environment. |

PROFESSIONAL COURSES

gem5 bootcamp
UC Davis
July 2024

Building RAG Agents with LLMs
NVIDIA
October 2024

Hands-On RTL Design
QuickSilicon
December 2024

PUBLICATIONS

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|------|--|
| 2024 | Per-Bank Bandwidth Regulation of Shared Last-Level Cache for Real-Time Systems
<i>IEEE Real-Time Systems Symposium</i> |
| 2023 | Profiling gem5 Simulator
<i>IEEE International Symposium on Performance Analysis of Systems and Software</i> |
| 2022 | Profiling an Architectural Simulator
<i>IEEE International Symposium on Performance Analysis of Systems and Software</i> |

PROJECTS

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|------|---|
| 2024 | PixelForge
<i>Cloud Infrastructure</i> <ul style="list-style-type: none">• Developed a cutting-edge prototype for on-the-go image editing, powered by AI/ML models to enhance user experience• Utilized OpenShiftAI to retrieve image data from Dropbox using access tokens, ensuring secure and efficient data transfer• Implemented three distinct AI-driven stylization models, allowing users to seamlessly transform their images with advanced visual effects |
| 2022 | MIPS Single Cycle Processor
<i>Computer Architecture</i> <ul style="list-style-type: none">• Designed registers, functional logic, and control subsystems using VHDL, ensuring robust and efficient processor operation• Developed a custom architecture supporting 16 individual operands, including arithmetic operations, data movement, branching, and jump instructions• Conducted extensive simulations to verify functionality, demonstrating the processor's ability to compute the Fibonacci sequence recursively up to the 15th digit, validating the design's correctness and performance |
| 2021 | Car-Bedded
<i>Embedded Systems</i> <ul style="list-style-type: none">• Designed and implemented software solutions for precise control of servos and motors, aligning functionality with detailed datasheet specifications and microcontroller architecture requirements• Incorporated UART and I2C communication protocols to enable efficient data transfer between devices, ensuring seamless hardware integration and reliable system operation• Leveraged the Raspberry Pi platform and RISC-V ISA development environment to build a flexible and scalable control system, optimizing performance for embedded applications |