- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION
- Run Simulation

RTL ANALYSIS
- Run Linter
- Open Elaborated Design

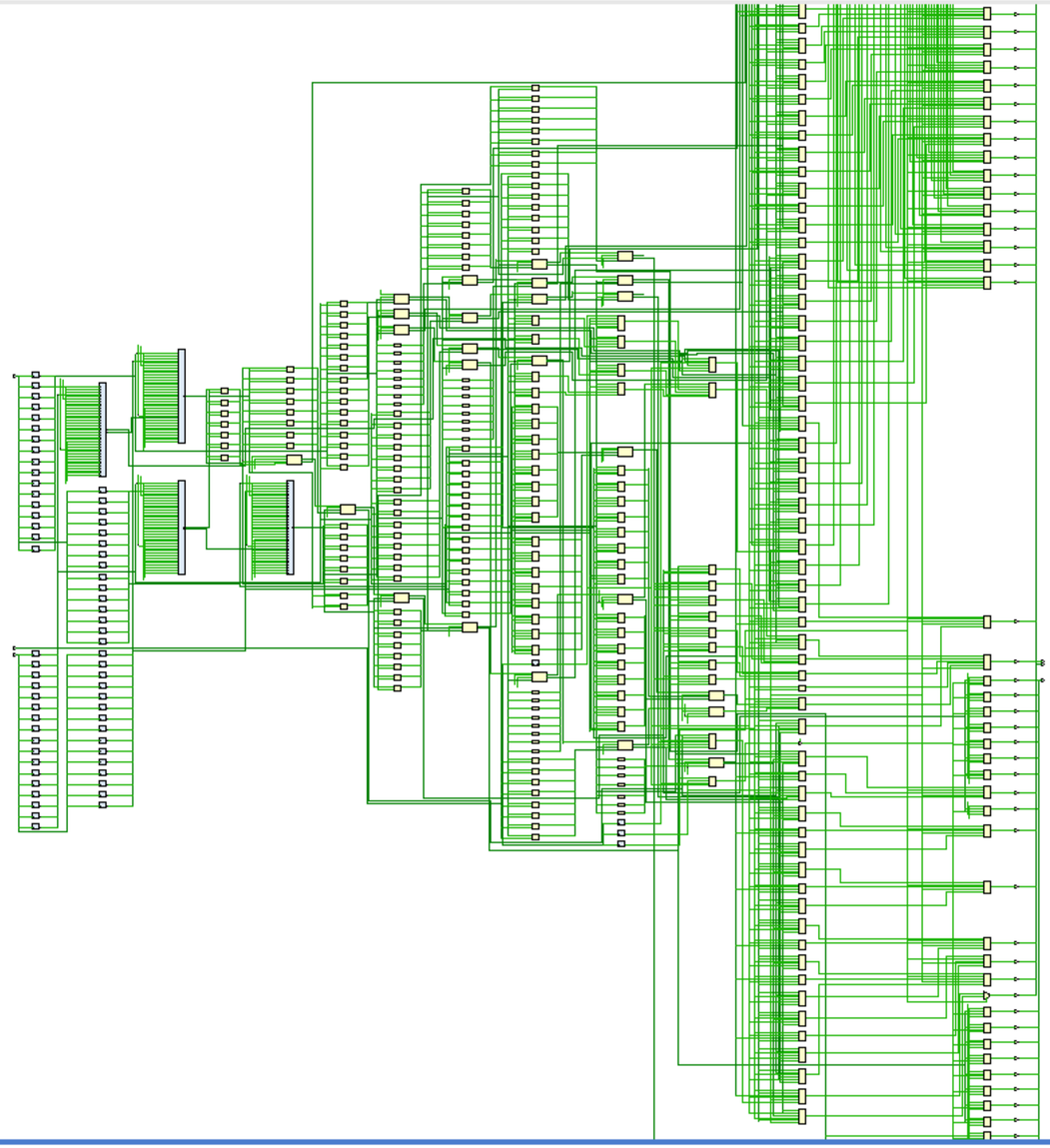
SYNTHESIS
- Run Synthesis
- **Open Synthesized Design**
  - Constraints Wizard
  - Edit Timing Constraints
  - Set Up Debug
  - Open Dataflow Design
  - Report Timing Summary
  - Report Clock Networks
  - Report Clock Interaction
  - Report Methodology
  - Report DRC
  - Report Utilization
  - Report Power
  - Schematic

IMPLEMENTATION

Sources | Netlist | Device Constraints | Source File Properties | Clock Regions

Package | Device | ALU_32_BIT_tb.vhd | **Schematic**

521 Cells | 133 I/O Ports | 1195 Nets



Open Elaborated Design
Report Methodology
Report DRC
Schematic

SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
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Open Dataflow Design
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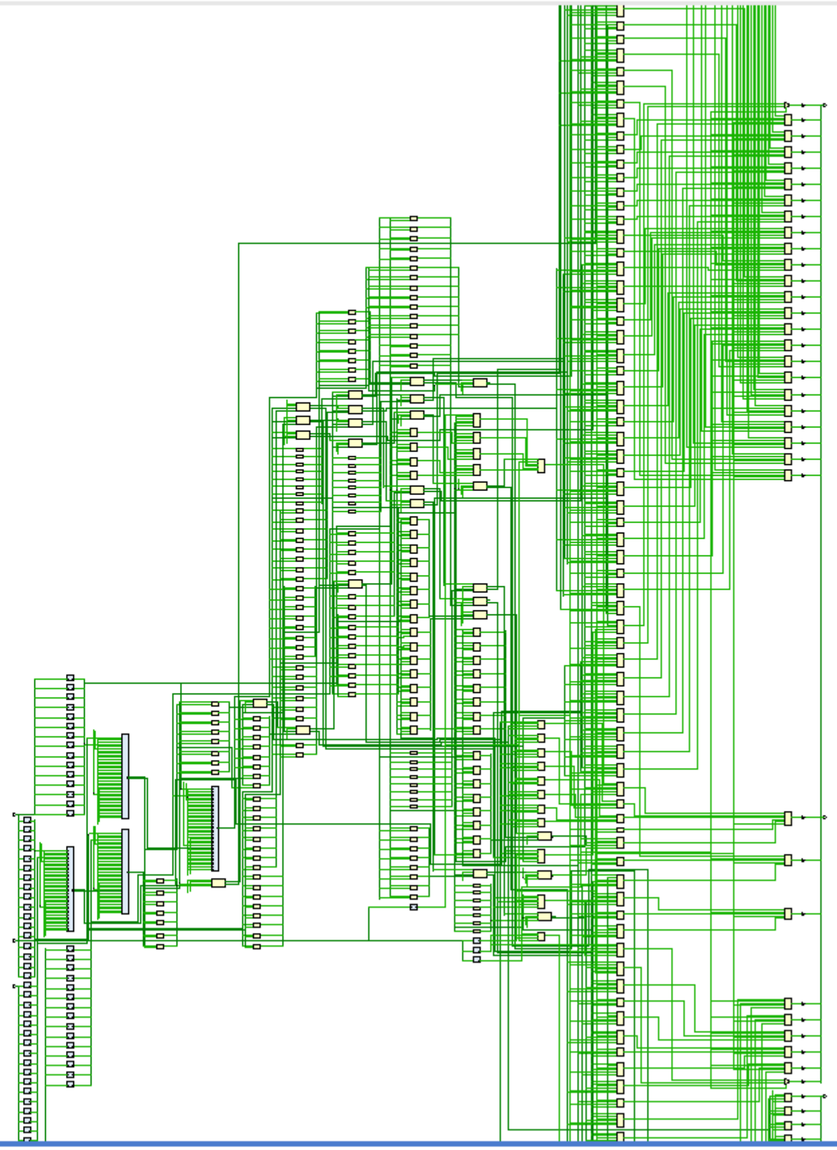
Report Power
Schematic

IMPLEMENTATION
Run Implementation
Open Implemented Design

PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager

521 Cells 133 I/O Ports 1195 Nets



- Open Elaborated Design
  - Report Methodology
  - Report DRC
  - Schematic

SYNTHESIS

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IMPLEMENTATION

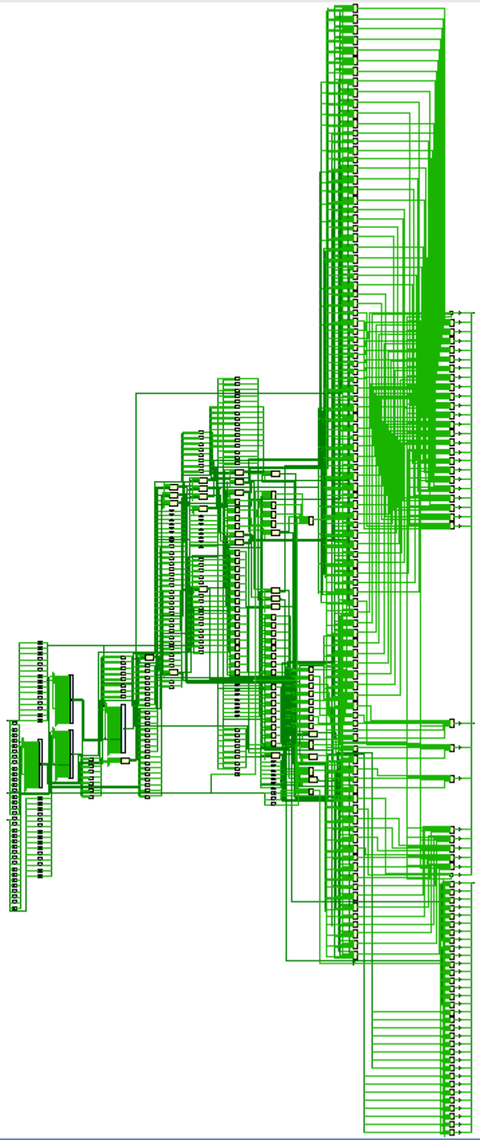
- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Package | Device | ALU_32_BIT_tb.vhd | **Schematic**

521 Cells 133 I/O Ports 1195 Nets



ALU_32_BIT - [C:/Vivado_projects/ALU_32_BIT/ALU_32_BIT.xpr] - Vivado 2025.1

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

I/O Planning

Flow Navigator

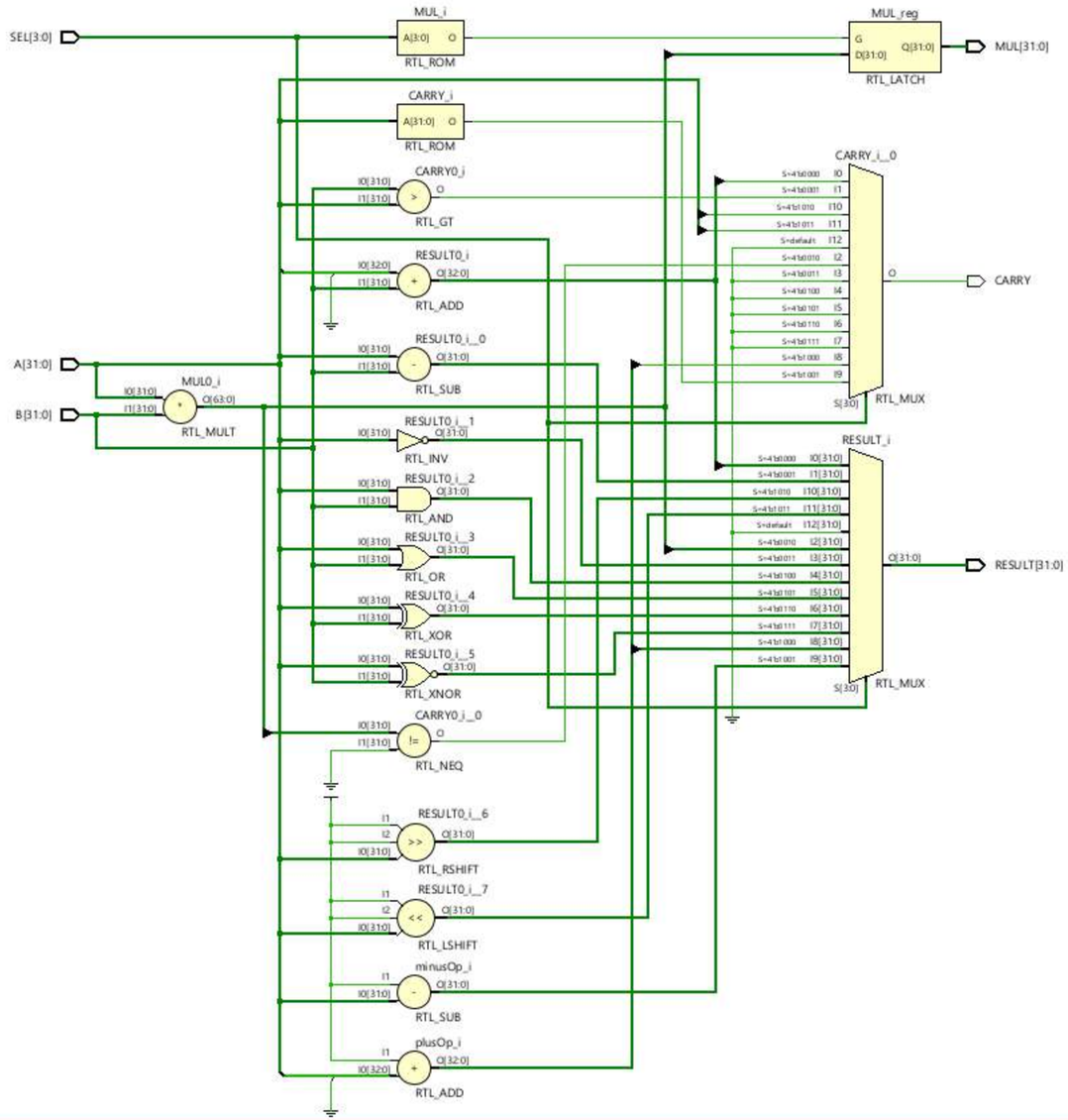
- **PROJECT MANAGER**
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- **IP INTEGRATOR**
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- **SIMULATION**
  - Run Simulation
- **RTL ANALYSIS**
  - Run Linter
  - Open Elaborated Design
    - Report Methodology
    - Report DRC
    - Schematic
- **SYNTHESIS**
  - Run Synthesis
  - Open Synthesized Design
- **IMPLEMENTATION**
  - Run Implementation
  - Open Implemented Design

ELABORATED DESIGN - xck24-ubva530-2LV-c

Sources | Netlist | Device Constraints | Source File Properties | Clock Regions

ALU_32_BIT_tb.vhd | **Schematic**

19 Cells | 133 I/O Ports | 557 Nets



Tcl Console | Messages | Log | Reports | Design Runs | Timing | Package Pins | I/O Ports | Linter

19°C Mostly sunny

Search

ENG IN

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