TSMC Libraries

Advanced Technology Standard Cells
Industry Standard I/Os

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Library Features

Standard cells

- 9 tracks, 600 cells
- Multiple Vt, ECO cells, low power architectures
- All major EDA views

General purpose I/Os

- Latch-up characterized to 200 milliamps
- Pad- and core-limited varieties available
- ESD characterized to 2kV/200V model (HBM/MM)

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TSMC Library Distribution and Support

- Developed and validated by TSMC
- Distributed by <Distributor>
  - Standard cells
  - General purpose digital I/O's
- Support provided by <Distributor>
  - Hotline and AE service in the excellent tradition of <Distributor>
  - Library updates and bug fixes are done by TSMC
  - If customized characterization or library elements are required, <Distributor> will direct those requests to TSMC

Why is TSMC Creating Libraries?

- To create a comprehensive choice of industry-leading standard cell, I/O and memory libraries in the leading process technologies, complementing internal offerings with 3rd party partner offerings
- To productize the cells used in wafer process development, and test them in real-world EDA flows, to provide process-tuned design architectures that fully utilize TSMC's silicon technology
- To set the industry standard for quality with TSMC 9000 compliant products
- To fulfill increasing demand for segment-targeted building blocks
- To utilize distribution partners with strong, global field organizations to serve designers throughout the design cycle

Who is Using TSMC Libraries?

- I/Os: In production, in hundreds of products
- Standard cells: Rapid customer adoption in
  - communications segment
  - consumer segment
- All geographic regions
  - Americas
  - Japan
  - Europe
  - Asia
- All leading processes
  - 0.15 μm
  - 0.13 μm
  - 90 nm

The advanced technology libraries for TSMC design

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TSMC Standard Cell Libraries

The advanced technology libraries for TSMC design

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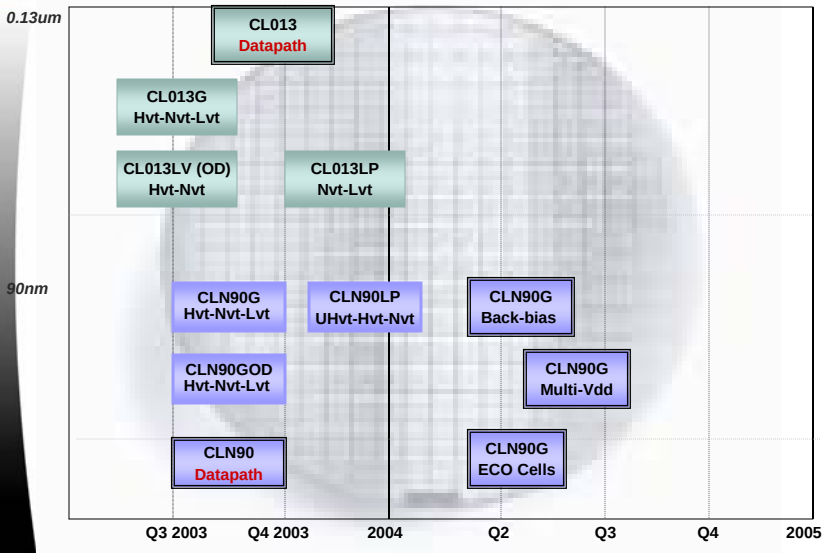
TSMC Standard Cell Roadmap



Left edge of each box represents first release schedule, when design kits are ready

Advanced Technology Library Features

- Ready for market
- Power
- Timing
- DFM

Advanced Technology Library Features

- **Ready for market**
  - Competitive cell density, 9 track architecture
  - Pre-tested with advanced design flows
  - Commercial and industry specs available
  - Tested in silicon
- Power
- Timing
- DFM

Advanced Technology Library Features

- Ready for market
- **Power**
  - Decoupling capacitors available in filler cells
  - Comprehensive libraries with standard, overdrive and multi-Vt cells
    - Overdrive 0.13µm LV
    - Multi-Vt all 0.13µm, all 90nm
  - Signal current characterization methodology for electromigration (EM) and wide wire routing
  - Added corners for advanced leakage characterization (90nm, 0.13µm)

- Timing
- DFM

Advanced Technology Library Features

- Ready for market
- Power
- **Timing**

  Most popular timing features
  - **Industry-standard 30-70 slew rate transition model**
  - **Setup/hold time uses "CLK-to-Q 10% push out" constraint**

- DFM

Advanced Technology Library Features

- Ready for market
- Power
- Timing
- **DFM**

  Built-in antenna diodes in clock buffer cells

  Advanced TSMC-tuned DFM features
  - **unidirectional gate poly**
  - **contact/metal overlap DFM guidelines used**

  Compliant with advanced TSMC "LOD" Spice model (90nm, Q4'03)

Multiple Threshold (Multi-Vt) for Both Power and Performance

- Best of both worlds
  - shorter delay (Low Vt)
  - lower power (Std and Hi Vt)
- Interchangeable footprints:
  - Freely swap cells from Hi, Std, or Low Vt
  - Vertical and horizontal abutment allowed
- Fully tested in TSMC Reference Flow

Unique to TSMC

Unique to TSMC

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New for Power Efficiency

The World's Most Advanced Power Architectures

- Back bias cells
  - Standby mode in addition to normal mode
  - Exponential decrease in leakage
- Multiple Vdd
  - Block based Vdd assignment
  - Lower switching current
- Pre-release in Q2'04

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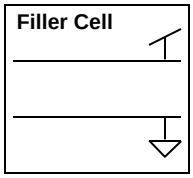
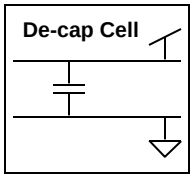
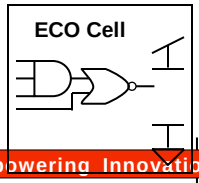
ECO Change for Design Flexibility

Advanced technology for faster time-to-market

- **Allows respin of chip with simple logic patches**
  - Logic elements to patch a circuit, in filler cell footprint
  - 30 different cells available
  - Modify contact, M1 (and above) to patch the logic for ECO
  - Decoupling caps may be placed in unused filler cells
- **Pre-release in Q2'04**







1 to TSMC

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Std Cell Design Kit Deliverables

New in Q4'03 !!

Abbreviation	Design Kits Description
rln syn pc	Release note Synopsys sdb, lib and clf for Apollo/Astro and Cadence tlf for Silicon Ensemble/SoC Encounter Physical synthesis
vlg vit	Verilog simulation model VHDL/Vital simulation model
mdt	Mentor DFT advisor and Fastscan model
apf/apt sef	Apollo frame view, cell view, timing view and power view Silicon Ensemble lef and technology files
cdb pgv ecsm	Celtic SI Voltage Storm Cadence DSM views Signal Strom
gds spi lpe	GDSII layout views LVS netlist in CDL format LPE Layout parasitic Extraction
doc	Datasheets and application notes

Notes:

1. Zero timing Verilog model for back-annotation
2. 7x7 Look-Up Table for Synopsys model
3. Composer symbol view design kits available upon request

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Standard Cell Categories

Cell Family	0.15um	0.13um	90nm	Drive Strength
(AND/NAND) / (OR/NOR) / (XOR/XNOR)	3 each	3 each	3 each	5 / 6 / 4 each
BUFFER / 3-STATE BUFFER: w/ & w/o enable/inverter	1 each	1 each	1 each	11 each
AOI / OAI / AO / OA / MAO / MOAI	12 each	39	39	4 each
ADDER: half/full adder	1 each	3	3	3/2 each
MUX: w & w/o inverted output	3 each	6	6	4 each
CLK BUFFER / Inverted CLK BUFFER / Gated CLK LATCH	1 each	1 each	1 each	11 / 11 / 10 each
DFF: pos-edge, neg-edge, async/sync R/S, w/o R/S	15	15	15	3 each
ENABLE DFF; async/sync R, w/o R flip-flop	6	6	6	3 each
SCAN DFF: all version of scan flip-flop	21	23	23	3 each
LATCH: active high/low enable, async R/S	8	8	8	3 each
INV/NAND/AND/MUX/XOR (balanced rise/fall)	1 each	5	5	4 each
DELAY/TIE-HIGH/TIE-LOW cell	1 each	4	4	4 / 1 / 1 (7/1/1)
ANTENNA/DECOUPLING cell	2, 7	7	7	N/A
Total Cell Number	514	600*	600*	

New in Q4'03 !!

*90nm and 0.13um libraries include over 30 datapath cells

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TSMC Std Cell Library Comparison

TECHNOLOGY (PROCESS)	PRODUCT NAME	Raw Gate Density (Kgates/mm^2)	Leakage (nW)	Internal Power (nW/MHz)	Speed (ns)	Voltage
CLN90G	TCBN90G	413	4.11	2.25	0.031	1.0V
	TCBN90GHVT		2.2	2.1	0.041	
	TCBN90GLVT		61.8	2.75	0.028	
	TCBN90GOD		7.62	3.85	0.026	1.2V
	TCBN90GODHVT (NEW)		4.84	3.2	0.0327	
	TCBN90GODLVT (NEW)		114.9	5.15	0.0237	
CLN90LP	TCBN90LP		0.13	2.45	0.04	
	TCBN90LPHVT (NEW)		0.02	2.4	0.05	
	TCBN90LPUHVT (NEW)		0.01	2.55	0.07	
CL013G	TCB013GHP	196	0.76	5.5	0.052	1.2V
	TCB013GHPHVT		0.2	5.3	0.067	
	TCB013GHPLVT		8.16	6.3	0.04	
CL013LV	TCB013LVHP		7.19	3.7	0.04	1.0V
	TCB013LVHPHVT		1.19	3.3	0.044	
	TCB013LVHPOD		12.5	6.2	0.0329	1.2V
	TCB013LVHPODHVT (NEW)		2.42	5.05	0.0351	
CL013LP	TCB013LPHP		0.008	8.5	0.067	1.5V
	TCB013LPHPLVT		0.171	7.4	0.042	
CL015G	TCB015G	131	0.058	9.8	0.055	1.5V
CL015LV	TCB015LV		0.51	6.1	0.05	1.2V

* All libraries use 9-track height cells; raw gates use ND2D1 area as 1 gate

* OD, HVT and LVT: Over Drive, High Vt and Low Vt nodes

NEW Added in 2H03

* Leakage/Power/Performance data are based on 2-input NAND gate (ND2D1) with 3X standard loads in nominal conditions

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New for 0.15 μm

- 8 track architecture
- High density
- Tuned for consumer applications
- Q4'03

New in Q4'03 !!

Standard Cell Timing Characterization Conditions

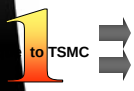
Type	Conditions		
	Voltage	Temperature	Process
Low Temperature (LTCOM)	VDD + 10%	-40°C	Fast-Fast
Best Case (BCCOM)	VDD + 10%	0°C	Fast-Fast
Typical Case (NCCOM)	VDD	25°C	Typical-Typical
Worst Case (WCCOM)	VDD - 10%	125°C	Slow-Slow

Some processes such as Overdrive have different conditions; check with TSMC

TSMC Standard Cell Characterization

Sets the industry standard

- **Extensive Characterization:**
  - **Input pin capacitance**
  - **Propagation Delay, Transition Time**
  - **Setup/Hold Time**
  - **Recovery/Removal Time/Minimum Pulse Width**
  - **Leakage, Internal Power**
- **High Accuracy:**
  - **7 X 7 Lookup Table for timing & power calculation**
- **Advanced Power Parameters:**
  - **Pin-to-Pin Power Table supported**
  - **State-dependent delay, internal power (selected cells)**
  - **Input pin state-dependent leakage**
  - **Cell output *Irms* characterized for EM at 500MHz**



Widespread Adoption, Working Silicon

- **90 nm**
  - **Customer #1: network**
    Taped out MPW in February 2003, **silicon functional**
  - **Customer #2: programmable logic**
    Taped out MPW in June 2003, **silicon functional**
  - **Customer #3: major IDM**
    Multiple tape-outs planned
- **0.13 μm**
  - **Customer #1: handset**
    Taped out 0.13G multi-Vt in April 2003, **silicon functional**
  - **Customer #2: wireless**
    Taped out 0.13G multi-Vt in July 2003 , **silicon functional**
  - **Customer #3: computer**
    Will tape out 0.13LV-OD in Q4/2003
  - **Customer #4: storage**
    Will tape out 0.13G in Q4/2003
- **0.15 μm**
  - **Customer #1: communication**
    In **pilot production** now (0.15G)
  - **Customer #2: consumer**
    Will tape out in Q4/2003 (0.15G)
  - **Customer #3: consumer**
    Will tape out in Q4/2003 (0.15LV)

Standard Cell Library
TSMC 9000 Validation Status

- **Level 1**

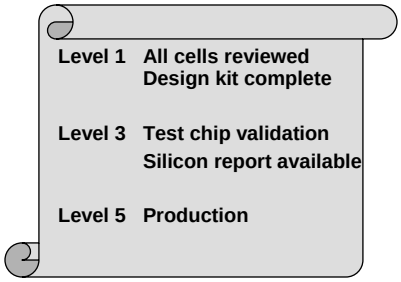
0.15 μm	All
0.13 μm	All
90 nm	All

- **Level 3**

0.13 μm	All
0.15 μm	All

- **Level 5**

0.15 μm	G



N90 Success Story – Processor Core

- **Design specification:** *Silicon Status: In progress*

Process:	TSMC 90nm logic 1P6M Low-K
Gate count:	1M gates
Memory:	140KB (20 memory instances)
Chip size:	3x3 mm square
Target Frequency:	350+MHz

- **Library & Flow:**

TSMC 90um multi-Vt Std. Cell library

TSMC digital I/O cells

Multi-Vt power/performance optimization

TSMC Reference Flow 4.0

Hierarchical partition and physical P&R implementation

CL013 Success Story – Cellular Phone Chip

- **Design specification:** *First time silicon success!*

Process:	TSMC 0.13 μm 1.2V/3.3V 1P6M FSG
Gate count:	1.44M gates
Memory:	485KB
Chip size:	9x9 mm square
Frequency Target:	122.5MHz
Package:	504 pins BGA

- **Library & Flow:**
  - TSMC 0.13 μm multi-Vt Std. cell library
  - TSMC digital & analog I/O cells
  - Multi-Vt script design methodology
  - Precise leakage cell modeling for leakage and speed trade-off

Summary

- Advanced DFM features
- Advanced power features
- Advanced ECO flexibility
- Most extensive characterization
- Flow proven and silicon validated
- Rapid market adoption

The advanced technology libraries for TSMC design

TSMC Standard I/O Libraries

The most widely used I/O libraries for TSMC design

TSMC Std I/O Portfolio Summary

Technology	Process	Voltage	Name	
90 nm	CLN90G	1.0/2.5V	TPDN90G2	
		1.0/3.3V	TPDN90G3	
	CLN90LP	1.2/2.5V	TPDN90LPN2	NEW
		1.2/3.3V	TPDN90LPN3	NEW
0.13μm	CL013G	1.2V/3.3V, 5V tol	TPZ013G3	
		1.2V/2.5V, 3.3V tol	TPZ013G2	
	CL013LV	1.0V/3.3V, 5V tol	TPZ013LG3	
		1.0V/2.5V, 3.3V tol	TPZ013LG2	
	CL013LVOD	1.0V/3.3V, 5V tol	TPZ013LODG3	NEW
		1.0V/2.5V, 3.3V tol	TPZ013LODG2	NEW
	CL013LP	1.5V/3.3V	TPD013LPN3	
0.15μm	CL015G	1.5V/3.3V, 5V tol	TPZ015G	
	CL015LV	1.2V/3.3V, 5V tol	TPZ015LG	

*** tol = tolerant**

NEW **Added in 2H03**

CL013 I/O Library Features

- **Process:** 0.13 µm logic salicide, from 4 to 8 metals
- **Voltage combinations**

Vdd-core / Vdd-IO	CL013LV (1.0V)	CL013G (1.2V)	CL013LP (1.5V)
2.5V	tpz013lg2 (3.3V tol)	tpz013g2 (3.3V tol)	
3.3V	tpz013lg3 (5V tol)	tpz013g3 (5V tol)	tpd013lpn3 (Linear)

* tol = tolerant

- **Cells:**
  - 123 I/O cells
  - 2 corner cells
  - 6 bond pads
  - 7 filler pads
- **Bonding type: staggered or linear**
- **Body cell width/height:**
  - 35µm x 246µm (tpz013g2/g3/lg2)
  - 35µm x 276µm (tpz013lg3)
  - 60µm x 150µm (tpd013lpn3)

CLN90 I/O Library Features

- **Process:** 90 nm logic salicide, from 5 to 9 metal layers
- **Voltage combinations**

Vdd-core / Vdd-I/O	CLN90G (1.0V)	CLN90LP (1.2V)
2.5V	tpdn90g2	tpdn90lpn2
3.3V	tpdn90g3	tpdn90lpn3

- **Cells:**
  - 18 I/O cells, programmable to over 75 configurations
  - 1 corner cell
  - 6 bond pads
  - 7 filler pads
- **Bonding type: linear**
- **Body cell width/height:**
  - 35µm x 210µm

CL015 I/O Library Features

- **Process:** 0.15 µm logic salicide, from 4 to 7 metals
- **Voltage combinations**

Vdd-core / Vdd-IO	CL015LV (1.2V)	CL015G (1.5V)
3.3V	tpz015lg (5V tol)	tpz015g (5V tol)

* tol = tolerant

- **Cells:**
  - 123 I/O cells
  - 1 corner cell
  - 2 bond pads
  - 7 filler pads
- **Bonding type:** staggered
- **Body cell width/height:**
  40µm x 230µm (tpz015lg/g)

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I/O Library
TSMC 9000 Validation Status

- **Level 1**

0.15 µm	All
0.13 µm	All
90 nm	All

- **Level 3**

0.13 µm	G

- **Level 5**

0.13 µm	Formal status underway Production of 2.5V + 3.3V : over 20,000 wafers!

Level 1 All cells reviewed
Design kit complete

Level 3 Test chip validation
Silicon report available

Level 5 Production

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Summary

- Available for production in TSMC processes
- Used in hundreds of products, tens of thousands of wafers
- Packaged by all leading backend houses

The most widely used I/O libraries for TSMC design