(10) ISO 17987 does not have a low battery specification. Using the ISO 17987 loads these low battery duty cycle parameters are covered for t_{BIT} values of 50 µs and 96 µs

6.8 AC Switching Characteristics

parameters valid over –40°C ≤ T_J ≤ 150 °C range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
t_{rx_pdr} t_{rx_pdf}	Receiver rising/falling propagation delay time (ISO/DIS 17987 Param 31)	R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF (See Figure 7-3, Figure 7-4)			6	µs
t_{rs_sym}	Symmetry of receiver propagation delay time Receiver rising propagation delay time (ISO/DIS 17987 Param 32)	Rising edge with respect to falling edge, (t_{rx_sym} = t_{rx_pdf} – t_{rx_pdr}), R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF (See Figure 7-3, Figure 7-4)	–2		2	µs
t_{LINBUS}	LIN wakeup time (minimum dominant time on LIN bus for wakeup)	See Figure 7-6, Figure 8-11 and Figure 8-12	25	100	150	µs
t_{CLEAR}	Time to clear false wakeup prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault)	See Figure 8-12	10		60	µs
t_{TXD_DTO}	Dominant state time out		20	45	80	ms
t_{EN}	Enable pin deglitch time	Time enable pin state change before initiating mode change or sampling TXD pin	3		12	µs
t_{MODE_CHANGE}	Mode change delay time	Time to change from normal mode to sleep mode through EN pin: See Figure 7-5			100	µs
t_{DETECT}	Time to detect Pin vs SPI and I/O voltage level at power up(1)	Time from coming out of UV_{CC} and device determines these states			2	µs
t_{DET_INH}	Time to detect which output INH or WKRQ at power up	Time from coming out of UV_{CC} and device determines these states			25	µs
$t_{NOMINIT}$	Normal mode initialization time	Time for normal mode to initialize and data on RXD pin to be valid, includes t_{MODE_CHANGE} for standby mode to normal mode See Figure 7-5			45	µs
t_{RSTN_act}	Time required for V_{CC} ≥ UV_{CC} to leave Restart mode	V_{CC} ≥ UV_{CC}	1.5	2	2.5	ms
t_{nRSTIN}	Input pulse required on the nRST pin to recognize a device reset.		120			µs
t_{NRST_TOG}	nRST pin output toggle high to low to high time	reg 29h[5] = 0 (Default value in SPI control. Value in pin control except for watchdog failure.)	1.5	2	2.5	ms
		reg 29h[5] = 1 (Value in pin control for watchdog failure.)	10	15	20	ms
t_{INITWD}	Initial long watchdog window time required to trigger first watchdog input trigger when entering Standby mode or Normal mode	WDI input trigger or SPI write command	150		200	ms
t_{INACT_FS}	Timer for inactivity coming out of sleep mode and when coming out of failsafe mode to determine if caused event has been cleared (1)	Default values and can be programmed to different values in SPI control.	4	5	6	min
t_{PWRUP}	Time from V_{SUP} exceeding UV_{SUP} until INH active	V_{CC} > UV_{CC}, INH = V_{SUP}, V_{CC} load of 50 mA @ 22 µF capacitance			3	ms
	Time from V_{SUP} exceeding UV_{SUP} and V_{CC} exceeding UV_{CC} until WKRQ active	V_{CC} > UV_{CC}, WKRQ = V_{CC}, V_{CC} load of 50 mA @ 22 µF capacitance			3	ms
t_{TOGGLE}	RXD pulse width when waking from sleep mode	register 'h12[2] = 1	5		15	µs
t_{UVFLTR}	Undervoltage detection delay time for V_{CC}		3		4	ms
t_{VSC}	Short to ground on VCC detection delay time		75	100	130	µs
t_{LDOON}	Time LDO is on to determine if a short circuit event is present after a previous uncleared detection		2		3	ms
$t_{MODE\_STBY\_NOM}$	Standby to normal mode change time based upon SPI write				70	µs
$t_{MODE\_NOM\_SLP}$	SPI write to go to sleep from normal	Time from SPI sleep command where LIN transceiver is off and RXD doesn't reflect the LIN bus			200	µs