

To configure permission settings in a memory region, perform the following steps.

1. Define the memory region by configuring [STARTADDR](#) and [ENDADDR](#). The values must be multiples of the override region granularity, which is 4096.
2. Use [PERMMASK](#) to define which of the access permissions in [PERM](#) to apply.
3. Enable and lock the override using the [CONFIG](#) register.

To prevent unintended reconfiguration of MPC, all overrides should be safeguarded by using the LOCK bit in the [CONFIG](#) register.

**Note:** For overlapping regions, MPC will perform a logical OR between the permission bits. The logical OR applies to both [PERMMASK](#) and [PERM](#) registers. Because of this, it is not possible to retract the READ, WRITE or EXECUTE permissions. For [PERM.SECURE](#), the OR operation between Secure (1) and NonSecure (0) will result in a Secure overlap region.

### 7.8.4.2 MPC error reporting

MPC reports an error when an access violation is detected.

MPC generates an [EVENTS\\_MEMACCERR](#) event when an erroneous transaction is detected. The following errors can be detected.

- The address cannot be decoded or the bus Manager does not have permissions to access the Subordinate. When this happens, the [MEMACCERR.ADDRESS](#) will capture the failing address issued by the bus Manager port and [MEMACCERR.INFO](#) will capture additional access information for the attempted transaction.
- If a transaction is routed to a Subordinate, but the Subordinate responds with an error.

The [MEMACCERR](#) registers will not be updated when [EVENTS\\_MEMACCERR](#) is set.

### 7.8.4.3 Registers

#### Instances

Instance	Domain	Base address	TrustZone			Split access	Description
			Map	Att	DMA		
MPC00	GLOBAL	0x50041000	HF	S	NA	No	Memory privilege controller MPC00

#### Configuration

Instance	Domain	Configuration
MPC00	GLOBAL	<p>The override region granularity is 4096 bytes</p> <p>Overrides 0 through 4 are available for override configuration. Override 5 can be configured for access blocking. Override 6 is reserved by the system and cannot be configured.</p>

#### Register overview

Register	Offset	TZ	Description
<a href="#">EVENTS_MEMACCERR</a>	0x100		Memory Access Error event
<a href="#">INTEN</a>	0x300		Enable or disable interrupt
<a href="#">INTENSET</a>	0x304		Enable interrupt
<a href="#">INTENCLR</a>	0x308		Disable interrupt