counter is set at one by default. The counter decrements for every correct input trigger and increments on every incorrect input trigger, but it never drops below zero. When the programmed counter is reached, the device transitions to restart mode, error counter is reset back to one, and the nRST pin pulls low for t_{NRST_TOG}. At the end of this time, the device transitions back to standby mode releasing the nRST pin to high. This counter can be changed to 1 (every error), 5, 9, or 15 using 8'h16[7:6]. The error counter can be read at register 8'h14[4:1]. In pin control, nWDR is pulled low for every watchdog error.

If the watchdog error count is set at one, the first input failure causes the device to transition to restart. This allows the system to check the counter after the first input trigger to see if a valid input was sent. Every incorrect watchdog input causes the interrupt to be set and nINT is pulled low.

8.3.22.10.4 Pin Control Mode

When using pin control for programming the watchdog, the WDT pin is used for this function. WDT sets the total window size of the window watchdog. It can be connected to VCC, GND or left open. See Section 8.3.5 or Section 6.7 for details on window timings. The ratio between the upper (open window) and lower (closed window) is 50/50. WDI pin is used by the controller to trigger the watchdog input. The WDI input is an edge-triggered event and supports both rising and falling edges. A filter time of t_W is used to avoid noise or glitches causing a false trigger. A pulse would be treated as a two input trigger events and cause the nWDR and nRST pins to be pulled low. nWDR pin can connected to the controller reset pin and if a watchdog event happens this pin is pulled low. The nRST pin may also be used for this function but includes other possible errors, like under-voltage or entering restart mode.

8.3.22.10.5 SPI Control Programming

In SPI control, registers 8'h13 through 8'h16 control the watchdog function. The device watchdog can be set as a timeout watchdog or window watchdog by setting 8'h13[7:6] to the method of choice. The timer is based upon register 8'h13[5:4] WD prescaler and register 8'h14[7:5] WD timer and is in ms. See Table 8-3 for the achievable times.

8.3.22.10.6 Watchdog Register Relationship

Table 8-3. Watchdog Window and Timeout Timer Configuration (ms)

WD_TIMER (ms)	Register 8'h13[5:4] WD_PRE			
Register 8'14[7:5]	00	01	10	11
000	4	8	12	16
001	32	64	96	128
010	128	256	384	512
011	256	384	512	768
100	512	1024	1536	2048
101	2048	4096	6144	8192
110	10240	20240	RSVD	RSVD
1111	RSVD	RSVD	RSVD	RSVD

8.3.22.10.7 Watchdog Timing

The TLIN1431x-Q1 provides two methods for setting up the watchdog when in SPI communication mode: window watchdog or timeout watchdog. If more frequent (i.e. <16 ms) input trigger events are desired it is suggested to use the timeout watchdog. When using timeout watchdog, the input trigger can occur anywhere before the timeout and is not tied to an open window.

When using the window watchdog, it is important to understand the closed and open window aspects. The device is set up with a 50%/50% open and closed window and is based on an internal oscillator with a ± 10% accuracy range. To determine when to provide the input trigger, this variance needs to be considered. For example, using the 64 ms nominal total window provides a closed and open window that are each 32 ms. Taking the ±10% internal oscillator into account means the total window could range from 57.6 ms to 70.4 ms. The closed and open window could then range from 22.4 ms to 35.2 ms. From the 57.6 ms total window and 35.2 ms