

## Enable interrupt

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				P O N M				L K J I H G F E D C B A																											
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value	Description																														
A-L	RW	COMPARE[i] (i=0..11)	W1S		Write '1' to enable interrupt for event COMPARE[i]																														
				Set	1	Enable																													
				Disabled	0	Read: Disabled																													
				Enabled	1	Read: Enabled																													
M	RW	RTCOMPARESYNC	W1S		Write '1' to enable interrupt for event RTCOMPARESYNC																														
				Set	1	Enable																													
				Disabled	0	Read: Disabled																													
				Enabled	1	Read: Enabled																													
N	RW	PWMPERIODEND	W1S		Write '1' to enable interrupt for event PWMPERIODEND																														
				Set	1	Enable																													
				Disabled	0	Read: Disabled																													
				Enabled	1	Read: Enabled																													
O	RW	PWMREADY	W1S		Write '1' to enable interrupt for event PWMREADY																														
				Set	1	Enable																													
				Disabled	0	Read: Disabled																													
				Enabled	1	Read: Enabled																													
P	RW	CLKOUTREADY	W1S		Write '1' to enable interrupt for event CLKOUTREADY																														
				Set	1	Enable																													
				Disabled	0	Read: Disabled																													
				Enabled	1	Read: Enabled																													

## 8.10.7.27 INTENCLR2

Address offset: 0x328

## Disable interrupt

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				P O N M				L K J I H G F E D C B A																											
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value	Description																														
A-L	RW	COMPARE[i] (i=0..11)	W1C		Write '1' to disable interrupt for event COMPARE[i]																														
				Clear	1	Disable																													
				Disabled	0	Read: Disabled																													
				Enabled	1	Read: Enabled																													
M	RW	RTCOMPARESYNC	W1C		Write '1' to disable interrupt for event RTCOMPARESYNC																														
				Clear	1	Disable																													
				Disabled	0	Read: Disabled																													
				Enabled	1	Read: Enabled																													
N	RW	PWMPERIODEND	W1C		Write '1' to disable interrupt for event PWMPERIODEND																														