6.7 Electrical Characteristics (continued)

parameters valid over –40°C ≤ T_J ≤ 150 °C range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{HYS}	Hysteresis voltage (ISO/DIS 17987 Param 20)(6) (7)	V_{HYS} = (V_{IL} - V_{IH}); Figure 7-2			0.175	V_{SUP}
V_{SERIAL_DIODE}	Serial diode LIN term pull-up path (ISO/DIS 17987 Param 21)	By design and characterization	0.4	0.7	1.0	V
R_{LIN}	Internal pull-up resistor to V_{SUP} on LIN (ISO/DIS 17987 Param 26)	Normal and Standby modes	20	45	60	kΩ
I_{RSLEEP}	Pull-up current source to V_{SUP}	Sleep mode, V_{SUP} = 12 V, LIN = GND	–20		–2	µA
$C_{LIN,PIN}$	Capacitance of the LIN pin	By design and characterization			25	pF
EN Input Terminal						
V_{IH}	High level input voltage		2		5.5	V
V_{IL}	Low level input voltage				0.8	V
V_{HYS}	Hysteresis voltage	By design and characterization	30		500	mV
I_{IL}	Low level input current	EN = Low	–8		8	µA
R_{EN}	Internal pull-down resistor		125	350	800	kΩ
LIMP Output Terminal (High Voltage Open-drain Output)						
ΔV_H	Hi-level voltage drop for LIMP with respect to V_{SUP}	I_{LIMP} = –60 mA		0.42	1.2	V
R_{dson}	LIMP output drain-to-source on resistance	I_O = –60 mA		7	20	Ω
$I_{LKG(LIMP)}$	Leakage current	LIMP = 0 V, Sleep Mode	–1		1	µA
HSS, INH high voltage open drain output pin						
V_{DET_INH}	Voltage on INH/WKRQ pin during t_{DET_INH} time	VSUP = 14V			1.5	V
ΔV_{HINH}	Hi-level voltage drop for INH with respect to V_{SUP}	I_{INH} = –6 mA		0.5	1	V
ΔV_{HHSS}	Hi-level voltage drop for HSS with respect to V_{SUP}	I_{HSS} = –60 mA		0.42	1.2	V
R_{dson}	HSS output drain-to-source on resistance	I_O = –60 mA		7	17	Ω
$I_{O(HSS)}$	Output current support	VSUP = 14 V,		60	100	mA
$I_{OC(HSS)}$	HSS overcurrent limit	VSUP = 14 V	150		300	mA
$I_{OL(HSS)}$	HSS open load current	VSUP = 14 V	–2.5			mA
$I_{OLHYS(HSS)}$	HSS open load current hysteresis	VSUP = 14 V	0.05	0.45	1	mA
I_{lkg}	Leakage current	INH, HSS = 0 V, Sleep Mode	–1		1	µA
$t_{R/F}$	Output rise and fall times (HSS)	5.5 V ≤ V_{SUP} ≤ 28 V, I_{LOAD} = 60 mA, R_L = 220 Ω, 80%/20%	0.6		2.5	V/µs
t_{HSS_on}	Switching on delay (HSS) from SPI command to on	V_{SUP} = 14 V, I_{LOAD} = 60 mA, V_{OUT} = 80% of V_{SUP}			60	µs
t_{HSS_off}	Switching off delay (HSS) from SPI command to off	V_{SUP} = 14 V, I_{LOAD} = 60 mA, V_{OUT} = 20% of V_{SUP}			140	µs
t_{OCFLTR}	HSS overcurrent filter time(2)	V_{SUP} = 14 V		16		µs
t_{OLFLTR}	HSS open load filter time(2)	V_{SUP} = 14 V		64		µs
t_{OCOFF}	HSS overcurrent shut off time	$I_{O(HSS)}$ > $I_{OC(HSS)}$	200		300	µs
WAKE Input Terminal						
V_{IH}	High-level input voltage	Sleep or Standby Mode, WAKE pin enabled	4			V
V_{IL}	Low-level input voltage	Sleep or Standby Mode, WAKE pin enabled			2	V
I_{IL}	Low-level input leakage current	WAKE = 1 V		15	25	µA
t_{WAKE}	Wake up hold time from a wake edge on WAKE in standby or sleep mode for static sensing..	See Figure 8-44 and Figure 8-45	140			µs
$t_{WAKE\_INVALID}$	WAKE pin pulses shorter than this will be filtered out in standby or sleep mode for static and cyclic sensing.	See Figure 8-44 and Figure 8-45			10	µs
WDI, SDI, CLK, nCS Input Terminal						
V_{IH}	High-level input voltage		2.19			V
V_{IL}	Low-level input voltage				0.8	V
I_{IH}	High-level input leakage current	Inputs = V_{CC}	–1		1	µA
I_{IL}	Low-level input leakage current	Inputs = 0 V, V_{CC} = Active	–50			µA