

## 6.7 Electrical Characteristics (continued)

parameters valid over  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$  range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>BATLINS3</sub>	Linear voltage range for V <sub>BAT</sub> for 3.3 V LDO and when I/O is 3.3 V with 5 V LDO <sup>(4)</sup>	R <sub>LOAD</sub> = 470 Ω ± 5% and C <sub>LOAD</sub> = 10 nF ± 10%; When capacitive load only 20 pF ± 20%, 5.5 V ≤ V <sub>BAT</sub> ≤ 20 V	0.561		2.27	V
V <sub>MAX5V</sub>	Maximum V <sub>PVOUT</sub>	28 V < V <sub>BAT</sub> ≤ 42 V, 470 Ω ± 5% and C <sub>LOAD</sub> = 10 nF ± 10%; When capacitive load only 20 pF ± 20%			5.1	V
V <sub>MAX3.3V</sub>	Maximum V <sub>PVOUT</sub> for 3.3 V LDO and when I/O is 3.3 V with 5 V LDO	20 V < V <sub>BAT</sub> ≤ 42 V, 470 Ω ± 5% and C <sub>LOAD</sub> = 10 nF ± 10%; When capacitive load only 20 pF ± 20%			3.36	V
V <sub>VCC5V_VIO3V</sub>	Voltage when V <sub>CC</sub> = 5 V and I/O is at 3.3 V	R <sub>LOAD</sub> = 470 Ω ± 5% and C <sub>LOAD</sub> = 10 nF ± 10%; When capacitive load only 20 pF ± 20% and I/O voltage is ≤ 3.6 V			3.36	V
C <sub>PIN</sub>	Pin capacitance			12		pF
t <sub>SET</sub>	Settling time of the buffer	470 Ω ± 5% and C <sub>LOAD</sub> = 10 nF ± 10%; When capacitive load only 20 pF ± 20%			50	μs

### Duty Cycle Characteristics

D1	Duty Cycle 1 (ISO/DIS 17987 Param 27 and J2602 Normal battery) <sup>(8) (9)</sup>	TH <sub>REC(MAX)</sub> = 0.744 × V <sub>SUP</sub> , TH <sub>DOM(MAX)</sub> = 0.581 × V <sub>SUP</sub> , V <sub>SUP</sub> = 7 V to 18 V, t <sub>BIT</sub> = 50/52 μs, D1 = t <sub>BUS_rec(min)</sub> /(2 × t <sub>BIT</sub> ) (See Figure 7-3, Figure 7-4)	0.396		
D2	Duty Cycle 2 (ISO/DIS 17987 Param 28 and J2602 Normal battery) <sup>(8) (9)</sup>	TH <sub>REC(MIN)</sub> = 0.422 × V <sub>SUP</sub> , TH <sub>DOM(MIN)</sub> = 0.284 × V <sub>SUP</sub> , V <sub>SUP</sub> = 7.6 V to 18 V, t <sub>BIT</sub> = 50/52 μs, D2 = t <sub>BUS_rec(MAX)</sub> /(2 × t <sub>BIT</sub> ) (See Figure 7-3, Figure 7-4)		0.581	
D3	Duty Cycle 3 (ISO/DIS 17987 Param 29 and J2602 Normal battery) <sup>(8) (9)</sup>	TH <sub>REC(MAX)</sub> = 0.778 × V <sub>SUP</sub> , TH <sub>DOM(MAX)</sub> = 0.616 × V <sub>SUP</sub> , V <sub>SUP</sub> = 7.0 V to 18 V, t <sub>BIT</sub> = 96 μs, D3 = t <sub>BUS_rec(min)</sub> /(2 × t <sub>BIT</sub> ) (See Figure 7-3, Figure 7-4)	0.417		
D4	Duty Cycle 4 (ISO/DIS 17987 Param 30 and J2602 Normal battery) <sup>(8) (9)</sup>	TH <sub>REC(MIN)</sub> = 0.389 × V <sub>SUP</sub> , TH <sub>DOM(MIN)</sub> = 0.251 × V <sub>SUP</sub> , V <sub>SUP</sub> = 7.6 V to 18 V, t <sub>BIT</sub> = 96 μs, D4 = t <sub>BUS_rec(MAX)</sub> /(2 × t <sub>BIT</sub> ) (See Figure 7-3, Figure 7-4)		0.59	
D1 <sub>LB</sub>	Duty Cycle 1 J2602 Low battery <sup>(9) (10)</sup>	TH <sub>REC(MAX)</sub> = 0.665 × V <sub>SUP</sub> , TH <sub>DOM(MAX)</sub> = 0.499 × V <sub>SUP</sub> , V <sub>SUP</sub> = 5.5 V to 7 V, t <sub>BIT</sub> = 50/52 μs, D1 = t <sub>BUS_rec(min)</sub> /(2 × t <sub>BIT</sub> ) (See Figure 7-3, Figure 7-4)	0.396		
D2 <sub>LB</sub>	Duty Cycle 2 J2602 Low battery <sup>(9) (10)</sup>	TH <sub>REC(MIN)</sub> = 0.496 × V <sub>SUP</sub> , TH <sub>DOM(MIN)</sub> = 0.361 × V <sub>SUP</sub> , V <sub>SUP</sub> = 6.1 V to 7.6 V, t <sub>BIT</sub> = 50/52 μs, D2 = t <sub>BUS_rec(MAX)</sub> /(2 × t <sub>BIT</sub> ) (See Figure 7-3, Figure 7-4)		0.581	
D3 <sub>LB</sub>	Duty Cycle 3 J2602 Low battery <sup>(9) (10)</sup>	TH <sub>REC(MAX)</sub> = 0.665 × V <sub>SUP</sub> , TH <sub>DOM(MAX)</sub> = 0.499 × V <sub>SUP</sub> , V <sub>SUP</sub> = 5.5 V to 7 V, t <sub>BIT</sub> = 96 μs, D1 = t <sub>BUS_rec(min)</sub> /(2 × t <sub>BIT</sub> ) (See Figure 7-3, Figure 7-4)	0.417		
D4 <sub>LB</sub>	Duty Cycle 4 J2602 Low battery <sup>(9) (10)</sup>	TH <sub>REC(MIN)</sub> = 0.496 × V <sub>SUP</sub> , TH <sub>DOM(MIN)</sub> = 0.361 × V <sub>SUP</sub> , V <sub>SUP</sub> = 6.1 V to 7.6 V, t <sub>BIT</sub> = 96 μs, D2 = t <sub>BUS_rec(MAX)</sub> /(2 × t <sub>BIT</sub> ) (See Figure 7-3, Figure 7-4)		0.59	

- (1) This is the measured voltage at the WDT pin when left floating. The WDT pin should be connected directly to V<sub>CC</sub>, GND or left floating.
- (2) Specified by design
- (3) V<sub>BATLINS5</sub> = [(1/7) \* V<sub>BAT</sub>] +/- 50 mV for the linear range of the PV buffer
- (4) V<sub>BATLINS3</sub> = [(1/9) \* V<sub>BAT</sub>] +/- 50 mV for the linear range of the PV buffer
- (5) SAE J2602 loads include: commander node: 5.5 nF; 4 kΩ and for a responder node: 5.5 nF; 875 Ω
- (6) V<sub>HYS</sub> is defined for both ISO 17987 and SAE J2602-1.
- (7) V<sub>HYS</sub> = (V<sub>th\_rec</sub> - V<sub>th\_dom</sub>) where V<sub>th\_rec</sub> and V<sub>th\_dom</sub> are the actual voltage values from V<sub>BUSrec</sub> and V<sub>BUSdom</sub>
- (8) ISO 17987 loads include 1 nF; 1 kΩ/ 6.8nF; 660 Ω/ 10 nF; 500 Ω; with t<sub>BIT</sub> values of 50 μs and 96 μs
- (9) SAE J2602 loads include: commander node: 5.5 nF; 4 kΩ/ 899 pF; 20 kΩ and for a responder node: 5.5 nF; 875 Ω/ 899 pF; 900 Ω; with t<sub>BIT</sub> values of 52 μs and 96 μs