

#### 8.24.10.40.2 DMA.RX.MATCH.CANDIDATE[n] (n=0..3)

Address offset: 0x728 + (n × 0x4)

The data to look for - any match will trigger the MATCH[n] event, if enabled.

**Note:** This register can be updated while a transfer is in progress, but the new value will not take effect until a match has been found or the transfer is done. That makes it possible to write a new set of match words which will be searched for immediately after the event triggers.

## 8.24.10.41 DMA.TX.PTR

Address offset: 0x73C

### RAM buffer start address

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
<b>Reset 0x20000000</b>	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	R/W	Field	Value ID	Value	Description																											
A	RW	PTR			RAM buffer start address for this EasyDMA channel. This address is a word aligned by 4 bytes.																											

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

## 8.24.10.42 DMA.TX.MAXCNT

Address offset: 0x740

Maximum number of bytes in channel buffer

## 8.24.10.43 DMA.TX.AMOUNT

Address offset: 0x744

Number of bytes transferred in the last transaction, updated after the END event.

Also updated after each MATCH event.