Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	E D C B A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

ID	R/W	Field	Value ID	Value	Description
E	R	ERRORSOURCE			Source of memory access error
			MPC	1	Error was triggered by MPC module
			Slave	0	Error was triggered by a Subordinate

7.8.4.3.6 OVERRIDE[n] (n=0..6)

Special privilege tables

7.8.4.3.6.1 OVERRIDE[n].CONFIG (n=0..6)

Address offset: 0x800 + (n × 0x20)

Override region n Configuration register

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	B A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

ID	R/W	Field	Value ID	Value	Description
A	RW1	LOCK			Lock Override region n
			Unlocked	0	Override region n settings can be updated
			Locked	1	Override region n settings can not be updated until next reset
B	RW	ENABLE			Enable Override region n
			Disabled	0	Override region n is not used
			Enabled	1	Override region n is used

7.8.4.3.6.2 OVERRIDE[n].STARTADDR (n=0..6)

Address offset: 0x804 + (n × 0x20)

Override region n Start Address

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

ID	R/W	Field	Value ID	Value	Description
A	RW	STARTADDR			Start address for override region n
					Address must be aligned to override region granularity, see the instance configuration table above for the override region granularity. The least significant bits of this register field are ignored based on the override region granularity and read as zero.

7.8.4.3.6.3 OVERRIDE[n].ENDADDR (n=0..6)

Address offset: 0x808 + (n × 0x20)

Override region n End Address

NORDIC
SEMICONDUCTOR