This register only exists if sbaccess128 is 1. If the bus master is busy then accesses set sbbusyerror, and don't do anything else

Bit number																																
ID																																
Reset 0x00000000																																
ID	R/W	Field	Value ID	Value	Description																											
A	R	DATA			Accesses bits 95:64 of sbdata (if the system bus is that wide).																											

8.26.1.34 DEBUGIF.SBDATA3

Address offset: 0x4FC

System Bus Data 127:96

This register only exists if sbaccess128 is 1. If the bus master is busy then accesses set sbbusyerror, and don't do anything else

Bit number																																
ID																																
Reset 0x00000000																																
ID	R/W	Field	Value ID	Value	Description																											
A	R	DATA			Accesses bits 127:96 of sbdata (if the system bus is that wide).																											

8.26.1.35 DEBUGIF.HALTSUM0

Address offset: 0x500

Halt summary 0

Each bit in this read-only register indicates whether one specific hart is halted or not. Unavailable/ nonexistent harts are not considered to be halted. This register might not be present if fewer than 2 harts are connected to this DM. The LSB reflects the halt status of hart hartsel[19:5] 0x0, and the MSB reflects halt status of hart hartsel[19:5] 0xf

Bit number																																
ID																																
Reset 0x00000000																																
ID	R/W	Field	Value ID	Value	Description																											
A	R	HALTSUM0			Halt summary 0																											

8.26.1.36 CPURUN

Address offset: 0x800

State of the CPU after a core reset