5 Power and clock management

The power and clock management system is optimized for ultra-low power applications to provide maximum power efficiency.

The power and clock management system is shown in the following figure.

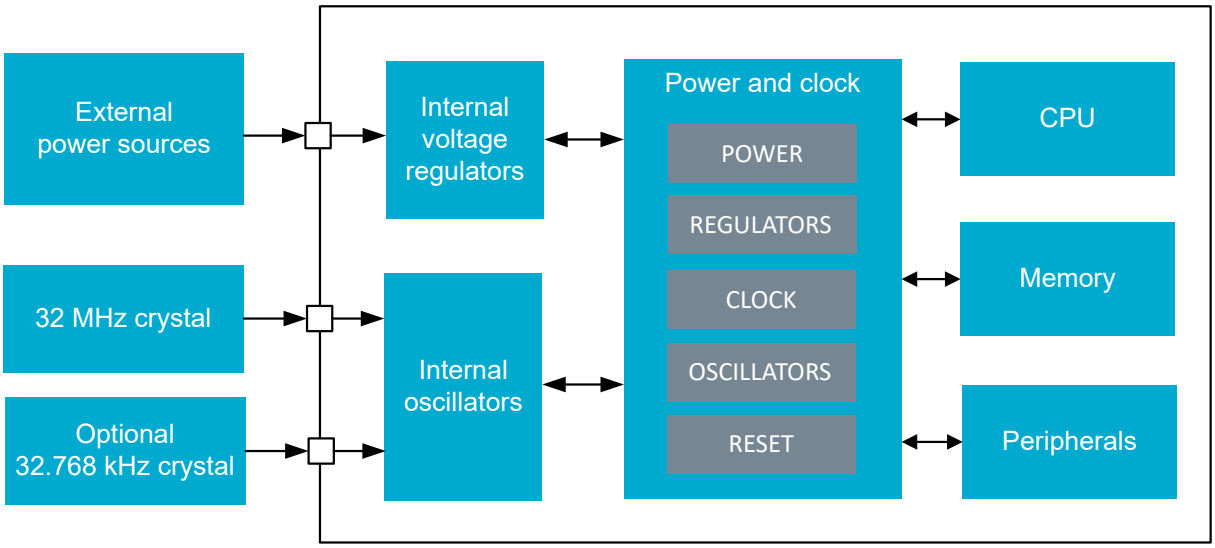

Figure 9: Power and clock management

The power and clock management system automatically tracks the power and clock resources requested by components in the system at any given time. To achieve the lowest power consumption possible, the system evaluates the requests, starts and stops clock sources, and chooses the most optimal regulator operation modes.

The device start-up sequence after reset is described in RESET — Reset control on page 101.

5.1 System ON mode

System ON is the default operation mode after power-on reset.

In System ON, all functional blocks, such as the CPU and peripherals, can be in an IDLE or RUN state depending on the configuration set by the software and the state of the executing application.

The power and clock management unit can switch the appropriate internal power domains on and off, depending on power requirements. A peripheral's power requirement is directly related to its activity level, which increases and decreases when specific tasks are triggered or events are generated.

5.1.1 Sub-power modes

In System ON mode, the system can reside in one of the two sub-power modes when the CPU and all peripherals are in an IDLE state.

The sub-power modes are the following:

- Constant Latency
- Low-power

In Constant Latency mode, the CPU wakeup latency and the PPI task response are constant and kept at a minimum. This is secured by forcing a set of basic resources to be turned on while in sleep mode. Constant