When the region configuration registers are writable, the region configuration registers can be updated until the lock bit is set to `Enabled`. However, the register fields Secure, Read, Write, amd Execute can be written to `0`, even if the lock bit is set to `Enabled`.

After changing the region protecton, CACHE must be invalidated to stay coherent with the updated RRAM configuration. Failure to do so will cause unpredictable results, such as being able to read cached content from a memory region that was just configured to be non-readable.

**Note:** The configuration registers for some of the regions are read-only and are reserved by the system configurations. See the register configuration table below for regions available for users.

### 4.2.6.5 Immutable boot region

RRAMC can make a part of the RRAM code memory immutable.

The immutable boot region has configurable permissions settings. Read, write, and execute permissions are configured individually. By making the region read-execute only, that memory range of the RRAM becomes immutable.

The region starts at address 0x00000000 and the size of the region is configurable. Note that the region does not add additional storage, but enforces permission settings on the memory range.

The size and permission settings of the immutable boot region is configured in UICR. If UICR.BOOTCONF is not configured, RRAMC will not enforce the protection.

Once the boot region protection is enabled, it can only be removed by ERASEALL. Erase protection can be enabled to prevent ERASEALL operation. For more information about erase protection, see CTRL-AP — Control access port on page 822.

### 4.2.6.6 Power-failure protection

Power failure protection is possible by using the power-fail comparator (POF) that is monitoring power supply.

If the power-fail comparator is enabled, and the power supply voltage is below the POF threshold, the power-fail comparator will prevent RRAMC from performing write operations. For more information about POF, see Power-fail comparator on page 69.

If a power failure warning is present at the start of an RRAM write operation, RRAMC will block the operation and a bus error will be signaled.

If a power failure warning occurs during an ongoing RRAM write, RRAMC can be configured to handle this in two ways:

- If POWER.CONFIG.POF = `Abort`, then RRAMC will stop the commit process from the internal write-buffer as soon as the condition occurs. After a power-failure event, the write buffer must be cleared by using the CLRWRITEBUF task before writing more data to RRAM.
- If POWER.CONFIG.POF = `Wait`, then RRAMC will try to complete the on-going write despite the warning of the operating voltage becoming too low.

### 4.2.6.7 Registers

#### Instances

| Instance | Domain | Base address | TrustZone | | | Split access | Description |
|---|---|---|---|---|---|---|---|
| | | | Map | Att | DMA | | |
| RRAMC | GLOBAL | 0x5004B000 | HF | S | NA | No | RRAM Non-Volatile Memory Controller |