| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| ID | R/W | Field | Value ID | Value | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A-f | RW | MEM[i] (i=0..31) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep the second bank in RAM block MEM[i] retained when in System OFF mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | All other RAM will be off in System OFF mode. Not all types of RAM blocks have two banks. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Off | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | On | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 4.2.6 RRAMC — Resistive random access memory controller

The resistive random access memory controller (RRAMC) is used for writing the internal RRAM memory, the secure information configuration region (SICR), and the user information configuration registers (UICR).

The main features of RRAMC are:

- Write and overwrite without erasing
- 128-bit word line with built in error correction code (ECC), detecting and correcting up to two bit errors per line
- Automatic standby or power-down modes
- One-time programmable (OTP) protection for user information configuration registers (UICR)
- Optional immutable boot region protection

### 4.2.6.1 Reading from RRAM

RRAM can be read using any natural alignment.

Read and execute operations are cachable through CACHE — Instruction/data cache on page 29. For execution performance figures, see CPU on page 19.

#### Low latency mode

The low power register allows making trade-offs between latency and power consumption. By default, RRAMC goes into PowerDown mode, so the wakeup time is variable. To enable a sleep mode with faster wake-up, configure Standby mode using register POWER.LOWPOWERCONFIG.MODE. In combination with Constant Latency sub-power mode, this ensures the lowest latency.

### 4.2.6.2 Writing to RRAM

When writing is enabled in register CONFIG.WEN, and CONFIG.WRITEBUFSIZE is set to `Unbuffered`, RRAM is written using any natural alignment (byte, half-word, 32-bit, or 64-bit).

RRAMC always writes full wordlines. When data is written to RRAM, the entire wordline is written and ECC is updated, even if only a single bit is changed. This has an effect on the endurance of the RRAM, as each write operation counts as a write to all bits in the wordline.

RRAMC is able to write both `0` and `1` to any bit in RRAM, even if that bit has been written before.

When writing with CONFIG.WRITEBUFSIZE set to `Unbuffered`, the written data (byte, half-word, 32-bit, or 64-bit) is committed to RRAM immediately.

#### 4.2.6.2.1 Buffered RRAM write

RRAMC enables fast buffered writes for contiguous memory regions.

RRAMC has an internal write-buffer that can be configured using CONFIG.WRITEBUFSIZE.