

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				F E D D C								B B B B B B B								A A A A A A A A A A															
Reset 0x30000000				0 0 1 1 0																															
D	R/W	Field	Value ID	Value	Description																														
			LOADTIMEOUTFAULT	0x1E	Load Timeout Fault																														
			STACKINGEXCFULT	0x1F	Fault on Exception Stacking																														
B	RW	MPIL			Previous interrupt level																														
C	RW	MPIE			Previous interrupt enable, same as MSTATUS.MPIE																														
D	R	MPP			Previous privilege mode, same as MSTATUS.MPP																														
E	RW	MINHV			In hardware vectoring																														
					Set by hardware at start of hardware vectoring, cleared by hardware at end of successful hardware vectoring																														
F	RW	INTERRUPT			Interrupt bit																														
			EXCEPTION	0	Set if the trap was caused by an interrupt																														
			INTERRUPT	1																															

8.26.3.9 MTVAL

Address offset: 0x343

Machine Trap Value

When a trap is taken into M-mode, MTVAL is either set to zero or written with exception-specific information to assist software in handling the trap. In VPR this register is ignored by exceptions and set to zero permanently

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				A A																															

8.26.3.10 MINTSTATUS

Address offset: 0x346

M-mode Interrupt Status

Holds the active interrupt level for M-mode

Bit number									31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID									A	A	A	A	A	A	A	A																									
Reset 0x00000000									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	R/W	Field	Value ID			Value				Description																															
A	R	MIL								M-Mode interrupt level																															

8.26.3.11 MINTTHRESH

Address offset: 0x347

M-mode Interrupt-level Threshold

Holds an 8-bit field for the threshold level of M-mode. Typical use is to implement critical sections. The current hart's effective interrupt level would then be: `effective_level = max(MINTSTATUS.MIL, MINTTHRESH.TH)`