

8.10.7.31 INTENCLR3

Address offset: 0x338

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID		P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A																		
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					
ID	R/W	Field	Value ID	Value	Description																														
A-L	RW	COMPARE[i] (i=0..11)			Write '1' to disable interrupt for event COMPARE[i]																														
		W1C																																	
			Clear	1	Disable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
M	RW	RTCOMPARESYNC			Write '1' to disable interrupt for event RTCOMPARESYNC																														
		W1C																																	
			Clear	1	Disable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
N	RW	PWMPERIODEND			Write '1' to disable interrupt for event PWMPERIODEND																														
		W1C																																	
			Clear	1	Disable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
O	RW	PWMREADY			Write '1' to disable interrupt for event PWMREADY																														
		W1C																																	
			Clear	1	Disable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
P	RW	CLKOUTREADY			Write '1' to disable interrupt for event CLKOUTREADY																														
		W1C																																	
			Clear	1	Disable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														

8.10.7.32 INTPEND3

Address offset: 0x33C

Pending interrupts

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID		P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A																		
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0							
ID	R/W	Field	Value ID	Value	Description																														
A-L	R	COMPARE[i] (i=0..11)			Read pending status of interrupt for event COMPARE[i]																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
M	R	RTCOMPARESYNC			Read pending status of interrupt for event RTCOMPARESYNC																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
N	R	PWMPERIODEND			Read pending status of interrupt for event PWMPERIODEND																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														