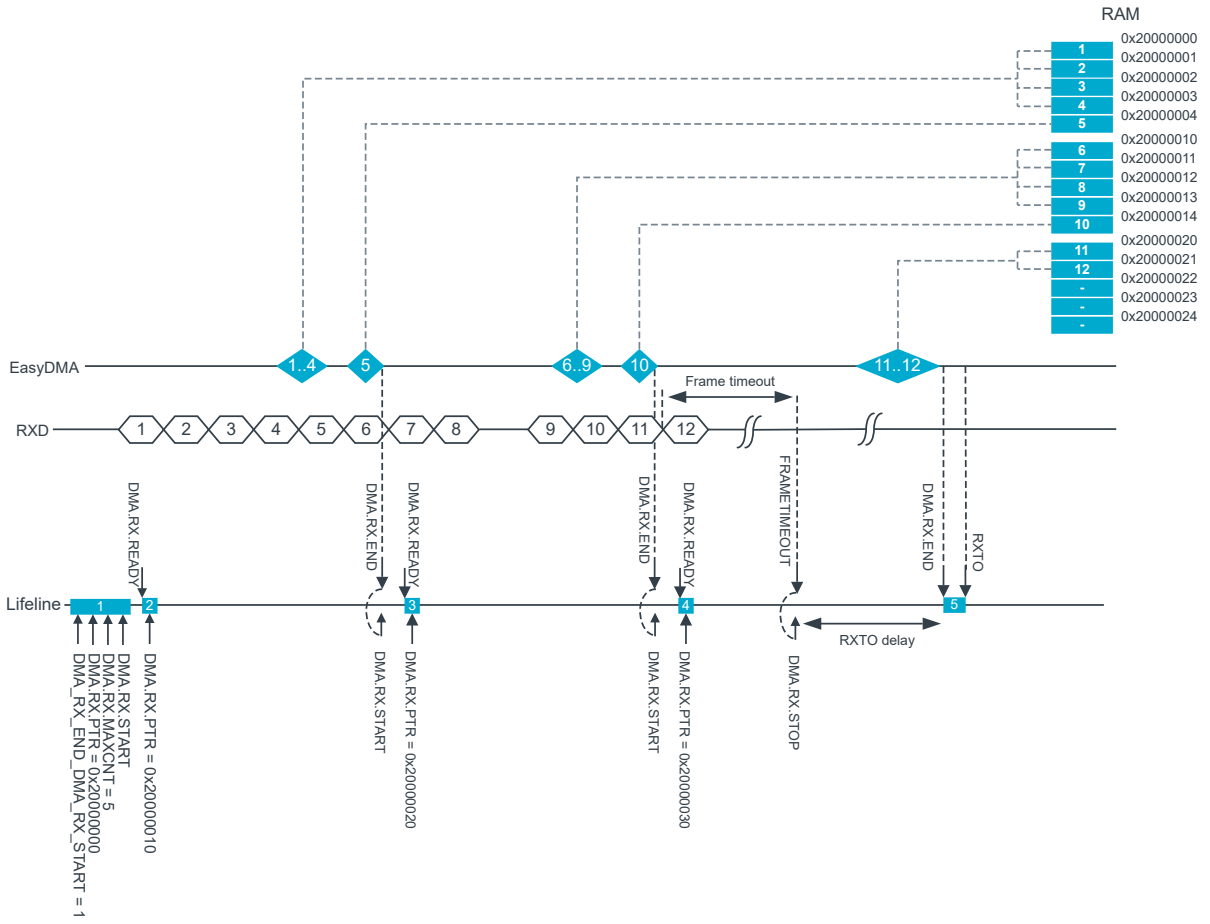


*Figure 163: UARTE reception frame timeout*

The minimum value of the FRAMETIMEOUT register must be set to a value larger than the configured UART frame length.

**Note:** Frames received after the RXTO event are discarded and not stored in memory. Reception will commence when DMA.RX.START is triggered.

## 8.25.7 Error conditions

An ERROR event, in the form of a framing error, will be generated if a valid stop bit is not detected in a frame. Another ERROR event, in the form of a break condition, will be generated if the RXD line is held active low for longer than the length of a data frame. A framing error is always generated before a break condition occurs.

An ERROR event will not stop reception. If the error was a parity error, the received byte is still transferred into RAM along with any following bytes. If a framing error occurs (wrong stop bit), that byte will not be stored in RAM but the next incoming bytes will.

## 8.25.8 Using the UARTE without flow control

If flow control is not enabled, the interface will behave as if the CTS and RTS lines are held active.

## 8.25.9 Parity and stop bit configuration

Automatic even parity generation for both transmission and reception can be configured using the register CONFIG on page 743. If odd parity is required, it can be configured using the register CONFIG on page 743. See the register description for details.