**Table 8-26. DEVICE_CONFIG Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 4 | LIMP_DIS | R/W | 0b | LIMP pin disable<br>0b = Enabled<br>1b = Disabled |
| 3-2 | LIMP_SEL_RESET | R/W | 0b | Selects the method to reset/turnoff the LIMP pin<br>00b = On third successful input trigger the error counter receives<br>01b = First correct input trigger<br>10b = SPI write to 8'h1A[1] = 1<br>11b = Reserved |
| 1 | LIMP_RESET | R/W1C | 0b | LIMP reset<br>Writing a one to this location resets the LIMP pin to off state and bit automatically clears |
| 0 | RSVD | R | 0b | Reserved |

### 8.6.17 DEVICE_CONFIG2 (Address = 1Bh) [reset = 0h]

DEVICE_CONFIG2 is shown in Figure 8-71 and described in Table 8-27

Return to Summary Table.

LIMP pin configuration and control.

**Figure 8-71. DEVICE_CONFIG2 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LIMP_HSS_SEL | | LIMP_HSS_CNTL | | | LIMP_HSS_ON | WAKE_WIDTH_MAX_DIS | RSVD |
| R/W-00b | | R/W-000b | | | R/W-0b | R/W-0b | R-0b |

**Table 8-27. DEVICE_CONFIG2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | LIMP_HSS_SEL | R/W | 00b | Selects LIMP pin function<br>00b = LIMP<br>01b = High side switch<br>10b = INH<br>11b = Reserved |
| 5-3 | LIMP_HSS_CNTL | R/W | 000b | Selects the method of control for the LIMP pin when configured as a high side switch<br>000b = On/Off<br>001b = PWM1<br>010b = PWM2<br>011b = Timer1<br>100b = Timer2<br>101b - 111b = Reserved |
| 2 | LIMP_HSS_ON | R/W | 0b | When LIMP is configured as HSS and control is On/Off this bit turns on or off the LIMP pin.<br>0b = Off<br>1b = On |
| 1 | WAKE_WIDTH_MAX_DIS | R/W | 0b | Disables the Max limit, $t_{WK\_PULSE\_WIDTH\_MAX}$ detection when pulse is selected for WAKE pin wake up.<br>0b = Enabled<br>1b = Disabled |
| 0 | RSVD | R | 0b | Reserved |

### 8.6.18 SWE_TIMER (Address = 1Ch) [reset = 30h]

SWE_TIMER is shown in Figure 8-72 and described in Table 8-28

Return to Summary Table.

Sleep wake error timer configuration. Power up always sets to default value.