8.6.30 nRST_CNTL (Address = 29h) [reset = 00h]

nRST_CNTL is shown in Figure 8-84 and described in Table 8-40

Return to Summary Table.

Configures nRST pin and FSO pin.

Figure 8-84. nRST_CNTL Register

7	6	5	4	3	2	1	0
RSVD		nRST_PULSE_WIDTH	FSO_POL_SEL	FSO_SEL			RSVD
R-00b		R/W-0b	R/W-0b	R/W/H-000b			R-0b

Table 8-40. nRST_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Reserved
5	nRST_PULSE_WIDTH	R/W	0b	Sets the pulse width for toggling nRST from high-->low-->high when device enters restart mode (ms) 0b = 2 1b = 15
4	FSO_POL_SEL	R/W	0b	Selects the polarity for the FSO pin 0b = Active low 1b = Active high **Note** Selects the output level when register 8'h29[3:1] = 110b making the pin a general-purpose output pin; 0 = Low and 1 = High
3-1	FSO_SEL	R/W/H	000b	Selects the information that will cause this pin to be pulled to the state selected by 'h29[4] 000b = V_{CC} Interrupt (overvoltage, undervoltage or short) 001b = WD interrupt event 010b = Reserved 011b = Local wake request (LWU) 100b = Bus wake request (WUP) 101b = Fail-safe mode entered 110b = General purpose output 111b = Reserved
0	RSVD	R	0b	Reserved

8.6.31 INT_GLOBAL Register (Address = 50h) [reset = A0h]

INT_GLOBAL is shown in Figure 8-85 and described in Table 8-41.

Return to Summary Table.

Logical OR of all to certain interrupts.

Figure 8-85. INT_GLOBAL Register

7	6	5	4	3	2	1	0
GLOBALERR	INT_1	INT_2	INT_3	RSVD	INT_4	RSVD	RSVD
RH-1b	RH-0b	RH-1b	RH-0b	RH-0b	RH-0b	R-0b	R-0b

Table 8-41. INT_GLOBAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GLOBALERR	RH	1b	Logical OR of all interrupts
6	INT_1	RH	0b	Logical OR of INT_1 register
5	INT_2	RH	1b	Logical OR of INT_2 register