

8.8.2 Pin sense mechanism.	275
8.8.3 Port capabilities.	276
8.8.4 Peripheral and subsystem assignment.	277
8.8.5 Clock pins.	278
8.8.6 Fast port control.	278
8.8.7 Reset behavior.	280
8.8.8 Registers.	280
8.9 GPIOTE — GPIO tasks and events.	285
8.9.1 Pin events and tasks.	286
8.9.2 Port event.	286
8.9.3 Tasks and events pin configuration.	287
8.9.4 Split security attribute.	287
8.9.5 Registers.	287
8.10 GRTC — Global real-time counter.	295
8.10.1 GRTC clock sources.	296
8.10.2 SYSCOUNTER.	296
8.10.3 Pulse Width Modulation (PWM).	299
8.10.4 Clock output.	300
8.10.5 Split Security.	300
8.10.6 Task priority.	301
8.10.7 Registers.	301
8.11 I ² S — Inter-IC sound interface.	322
8.11.1 Mode.	323
8.11.2 Transmitting and receiving.	323
8.11.3 Left right clock (LRCK).	324
8.11.4 Serial clock (SCK).	325
8.11.5 Master clock (MCK).	325
8.11.6 Width, alignment and format.	327
8.11.7 EasyDMA.	329
8.11.8 Module operation.	332
8.11.9 Pin configuration.	334
8.11.10 Registers.	335
8.12 LPCOMP — Low-power comparator.	348
8.12.1 Operation.	349
8.12.2 Shared resources.	350
8.12.3 Pin configuration.	350
8.12.4 Registers.	350
8.13 NFCT — Near field communication tag.	359
8.13.1 Overview.	360
8.13.2 Operating states.	362
8.13.3 Pin configuration.	363
8.13.4 EasyDMA.	364
8.13.5 Frame assembler.	364
8.13.6 Frame disassembler.	366
8.13.7 Frame timing controller.	367
8.13.8 Collision resolution.	368
8.13.9 Antenna interface.	369
8.13.10 NFCT antenna recommendations.	369
8.13.11 Battery protection.	370
8.13.12 Digital Modulation Signal.	370
8.13.13 References.	371
8.13.14 Registers.	371
8.14 PDM — Pulse density modulation interface.	398
8.14.1 Master clock generator.	399