C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. C_{pcb1} and C_{pcb2} are stray capacitance on the PCB. C_{pin} is the pin input capacitance on pins **XL1** and **XL2**. The load capacitors C1 and C2 must have the same value.

When using external capacitors, the internal capacitor is disabled by setting OSCILLATORS.XOSC32KI.INTCAP to `0`.

5.5.2.2 External source

The 32.768 kHz crystal oscillator (LFXO) is designed to work with external sources.

The device can use a rail-to-rail clock, where the signal should be applied to the **XL1** pin with the **XL2** pin left unconnected. To enable rail-to-rail clock, set XOSC32KI.BYPASS=`Enabled`.

Using an external source requires that CLOCK.LFCLK.SRC=`LFXO`.

5.5.3 CPU clock frequency selection

The CPU clock frequency is configurable on boot in the register PLL.FREQ (Retained) on page 91.

The device supports 64 or 128 MHz frequency.

The device starts at 64 MHz. For higher frequencies, it must be configured when the CPU starts and before any peripherals that use the high-frequency clock are enabled. Changing the frequency on a running system or to an unsupported value causes undefined system behavior and the device can malfunction.

5.5.4 Registers

Instances

Instance	Domain	Base address	TrustZone			Split access	Description
			Map	Att	DMA		
OSCILLATORS : S OSCILLATORS : NS	GLOBAL	0x50120000 0x40120000	US	S	NA	No	Oscillator control

Register overview

Register	Offset	TZ	Description
XOSC32M.CONFIG.INTCAP	0x71C		Crystal load capacitor as seen by the crystal across its terminals, including pin capacitance but excluding PCB stray capacitance.
PLL.FREQ	0x800		Set speed of MCU power domain, including CPU This register is retained.
PLL.CURRENTFREQ	0x804		Current speed of MCU power domain, including CPU This register is retained.
XOSC32KI.BYPASS	0x900		Enable or disable bypass of LFCLK crystal oscillator with external clock source
XOSC32KI.INTCAP	0x904		Programmable capacitance of XL1 and XL2 This register is retained.

5.5.4.1 XOSC32M

32 MHz oscillator control

5.5.4.1.1 XOSC32M.CONFIG.INTCAP

Address offset: 0x71C