9.6.5.1 Debug side registers

Register overview

Register	Offset	TZ	Description
RESET	0x000		System reset request and status
ERASEALL	0x004		Perform a secure erase of the device, where flash, SRAM, and UICR will be erased in sequence. The device will be returned to factory default settings upon next reset.
ERASEALLSTATUS	0x008		This is the status register for the ERASEALL operation.
ERASEPROTECT.STATUS	0x00C		Erase protection status.
ERASEPROTECT.DISABLE	0x010		This register disables ERASEPROTECT and performs Erase all.
APPROTECT.STATUS	0x014		This is the status register for the access port protection.
MAILBOX.TXDATA	0x020		Data sent from the debugger to the device.
MAILBOX.TXSTATUS	0x024		Status to indicate if data sent from the debugger to the device has been read.
MAILBOX.RXDATA	0x028		Data sent from the device to the debugger.
MAILBOX.RXSTATUS	0x02C		Status to indicate if data sent from the device to the debugger has been read.
INFO.PARTNO	0x030		Part number of the device
INFO.HWREVISION	0x034		Hardware Revision of the device
IDR	0x0FC		CTRL-AP Identification Register, IDR

9.6.5.1.1 RESET

Address offset: 0x000

System reset request and status

Only the enumerated values are supported, writing other values has unpredictable effect.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	W	RESET																																	
			NoReset	0																															
			SoftReset	1																															
			HardReset	2																															
			PinReset	4																															

Reset device to factory default settings

Trigger soft reset of the device. Use NoReset after the device has been reset.

Trigger hard reset of the device - as part of the ERASEALL sequence. Use NoReset after the device has been reset.

Trigger pin reset of the device. Use NoReset after the device has been reset.

9.6.5.1.2 ERASEALL

Address offset: 0x004

Perform a secure erase of the device, where flash, SRAM, and UICR will be erased in sequence. The device will be returned to factory default settings upon next reset.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	W	ERASEALL																																	
			NoOperation	0																															
			Erase	1																															

Return device to factory default settings

No operation

Erase flash, SRAM, and UICR in sequence