Note: Scan mode and oversampling should not be combined without burst.

1. The ADC must be enabled and started via the ENABLE register and START task.
2. At least one channel must be enabled (via the CH[n].CONFIG registers).
3. Now the ADC can be sampled, by triggering the SAMPLE task.

The ADC indicates a single ongoing conversion via the register STATUS. During scan mode, oversampling, noise shaping, or continuous modes, more than a single conversion takes place in the ADC. As consequence, the value reflected in STATUS register will toggle at the end of each single conversion.

8.18.5.1 One-shot mode

One-shot operation is configured by enabling only one of the available channels defined by CH[n].PSELP, CH[n].PSELN, and CH[n].CONFIG registers.

Upon a SAMPLE task, the ADC powers up and starts to sample the input voltage. The CH[n].CONFIG.TACQ controls the acquisition time.

The time it takes to perform the first sample is $t_{PWRUP} + t_{ACQ} + t_{CONV}$, where t_{ACQ} is the acquisition time, t_{CONV} is the conversion time, and t_{PWRUP} is the time it takes to power up the ADC.

If multiple samples are taken, some combinations of t_{ACQ} and t_{CONV} will allow SAADC to pipeline sampling and conversion, at which point the actual sampling time is just t_{CONV}.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA. For more information, see EasyDMA on page 559.

8.18.5.2 Continuous mode

Continuous sampling can be achieved by using the internal timer in the ADC, or triggering the SAMPLE task from one of the general purpose timers through the PPI system.

Care shall be taken to ensure that the sample rate fulfils the following criteria, depending on how many channels are active:

$$t_{SAMPLE} > t_{ACQ} + t_{CONV}$$

If t_{ACQ}=0 and t_{CONV}=0, SAADC will use pipelining to increase sampling speed. In this case, the time for the first sample to arrive is

$$t_{SAMPLE} = t_{PWRUP} + t_{ACQ} + t_{CONV}$$

and for subsequent samples

$$f_{SAMPLE} = 1/(t_{CONV})$$

The SAMPLERATE register can be used as a local timer instead of triggering individual SAMPLE tasks. When SAMPLERATE.MODE is set to Timers, it is sufficient to trigger SAMPLE task only once in order to start the SAADC and triggering the STOP task will stop sampling. The SAMPLERATE.CC field controls the sample rate.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA.