Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	G	F				E	D	C	B				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	R	TAG			Cache tag.
B-E	R	DUV[i] (i=0..3)			Data unit valid info. One info bit for each data unit in a line, LSB is the first data unit.
			Invalid	0	Invalid data unit
			Valid	1	Valid data unit
F	R	V			Line valid bit.
			Invalid	0	Invalid cache line
			Valid	1	Valid cache line
G	R	MRU			Most recently used way.
			Way0	0	Way0 was most recently used
			Way1	1	Way1 was most recently used

4.2.3.6 Registers

Instances

Instance	Domain	Base address	TrustZone			Split access	Description
			Map	Att	DMA		
ICACHEDATA	APPLICATION	0x02F00000	HF	S	NA	No	Instruction cache data

Configuration

Instance	Domain	Configuration
ICACHEDATA	APPLICATION	Number of sets : 0..127 Number of ways : 0..1 Number of data units : 0..3 Data width of a data unit : 0..1 words

Register overview

Register	Offset	TZ	Description
SET[n].WAY[o].DU[p].DATA[q]	0x0		Cache data bits for DATA[q] in DU[p] (DataUnit) of SET[n], WAY[o].

4.2.3.6.1 SET[n].WAY[o].DU[p].DATA[q] (n=0..127) (o=0..1) (p=0..3) (q=0..1)

Address offset: 0x0 + (n × 0x40) + (o × 0x20) + (p × 0x8) + (q × 0x4)

Cache data bits for DATA[q] in DU[p] (DataUnit) of SET[n], WAY[o].

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	R	Data			Data