Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				D	D																	C	C	B	B	B	B				A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	PIN																																	
																																			GPIO pin selection.
B	RW	PORT																																	
																																			GPIO Port selection
C	RW	INTERNAL																																	
																																			Internal input selection for analog negative input when CH[n].PSELN.CONNECT = Internal
			Avdd	0																															Connected to the internal 0.9V analog supply rail
			Dvdd	1																															Connected to the internal 0.9V digital supply rail
			Vdd	2																															Connected to VDD
D	RW	CONNECT																																	Connection
			NC	0																															Not connected
			AnalogInput	1																															Select analog input The analog input is connected based on CH[n].PSELN.PIN and CH[n].PSELN.PORT

8.18.11.32 CH[n].CONFIG (n=0..7)

Address offset: 0x518 + (n × 0x10)

Input configuration for CH[n]

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID					F	F	F				E	E	E	E	E	E	E	E	D			C	B	A	A	A									
Reset 0x00020000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	GAIN																																	Gain control
			Gain2	0																															2
			Gain1	1																															1
			Gain2_3	2																															2/3
			Gain2_4	3																															2/4
			Gain2_5	4																															2/5
			Gain2_6	5																															2/6
			Gain2_7	6																															2/7
			Gain2_8	7																															2/8
B	RW	BURST																																	Enable burst mode
			Disabled	0																															Burst mode is disabled (normal operation)
			Enabled	1																															Burst mode is enabled. SAADC takes 2^OVERSAMPLE number of samples as fast as it can, and sends the average to Data RAM.
C-	RW	REFSEL																																	Reference control
			Internal	0																															Internal reference (0.9 V)
			External	1																															External reference given at PADC_EXT_REF_1V2
D	RW	MODE																																	Enable differential mode
			SE	0																															Single ended, PSELN will be ignored, negative input to ADC shorted to GND
			Diff	1																															Differential
E	RW	TACQ		[1..319]																															Acquisition time, the time the ADC uses to sample the input voltage. Resulting acquistion time is ((TACQ+1) x 125 ns)
F	RW	TCONV		[1..7]																															Conversion time. Resulting conversion time is ((TCONV+1) x 250 ns)

8.18.11.33 CH[n].LIMIT (n=0..7)

Address offset: 0x51C + (n × 0x10)

High/low limits for event monitoring a channel