Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID						R	Q	P	O	N	M	L	K	J	I	H							G			F				E	D	C		B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
P	RW	DMATXREADY																																	
			Disabled	0																															
			Enabled	1																															
Q	RW	DMATXBUSERROR																																	
			Disabled	0																															
			Enabled	1																															
R	RW	FRAMETIMEOUT																																	
			Disabled	0																															
			Enabled	1																															

Description

Enable or disable interrupt for event DMATXREADY

Disable

Enable

Enable or disable interrupt for event DMATXBUSERROR

When this event is generated, the address which caused the error can be read from the BUSERRORADDRESS register.

Disable

Enable

Enable or disable interrupt for event FRAMETIMEOUT

Disable

Enable

8.25.13.25 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID						R	Q	P	O	N	M	L	K	J	I	H							G			F				E	D	C		B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW W1S	CTS																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
B	RW W1S	NCTS																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
C	RW W1S	TXDRDY																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
D	RW W1S	RXDRDY																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
E	RW W1S	ERROR																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
F	RW W1S	RXTO																																	
			Set	1																															

Description

Write '1' to enable interrupt for event CTS

Enable

Read: Disabled

Read: Enabled

Write '1' to enable interrupt for event NCTS

Enable

Read: Disabled

Read: Enabled

Write '1' to enable interrupt for event TXDRDY

Enable

Read: Disabled

Read: Enabled

Write '1' to enable interrupt for event RXDRDY

Enable

Read: Disabled

Read: Enabled

Write '1' to enable interrupt for event ERROR

Enable

Read: Disabled

Read: Enabled

Write '1' to enable interrupt for event RXTO

Enable