

8.10.7.24 INTPEND1

Address offset: 0x31C

Pending interrupts

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				P O N M				L K J I H G F E D C B A																											
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value		Description																													
A-L	R	COMPARE[i] (i=0..11)				Read pending status of interrupt for event COMPARE[i]																													
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
M	R	RTCOMPARESYNC				Read pending status of interrupt for event RTCOMPARESYNC																													
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
N	R	PWMPERIODEND				Read pending status of interrupt for event PWMPERIODEND																													
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
O	R	PWMREADY				Read pending status of interrupt for event PWMREADY																													
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
P	R	CLKOUTREADY				Read pending status of interrupt for event CLKOUTREADY																													
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														

8.10.7.25 INTEN2

Address offset: 0x320

Enable or disable interrupt

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				P O N M			L K J I H G F E D C B A																												
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value	Description																														
A-L	RW	COMPARE[i] (i=0..11)			Enable or disable interrupt for event COMPARE[i]																														
			Disabled	0	Disable																														
			Enabled	1	Enable																														
M	RW	RTCOMPARESYNC			Enable or disable interrupt for event RTCOMPARESYNC																														
			Disabled	0	Disable																														
			Enabled	1	Enable																														
N	RW	PWMPERIODEND			Enable or disable interrupt for event PWMPERIODEND																														
			Disabled	0	Disable																														
			Enabled	1	Enable																														
O	RW	PWMREADY			Enable or disable interrupt for event PWMREADY																														
			Disabled	0	Disable																														
			Enabled	1	Enable																														
P	RW	CLKOUTREADY			Enable or disable interrupt for event CLKOUTREADY																														
			Disabled	0	Disable																														
			Enabled	1	Enable																														

8.10.7.26 INTENSET2

Address offset: 0x324