8.8.7 Reset behavior

While the **nRESET** pin is asserted (falling edge and held low), GPIO pins will enter one of two states:

- Retain their current configuration (e.g., outputs remain outputs, inputs remain inputs)
- Switch to high impedance, which is the default state upon device startup

Once **nRESET** is deasserted (rising edge), all GPIOs transition to the high impedance state until device firmware configures them.

When GPIO pins are in a high-impedance state for a prolonged period, external circuits that depend on a clearly defined logic level (either high or low) might require the use of external pull-up or pull-down resistors to ensure reliable operation. However, in most cases this is not required, as the duration of the high-impedance state during the reset cycle is typically very short.

8.8.8 Registers

Instances

Instance	Domain	Base address	TrustZone			Split access	Description
			Map	Att	DMA		
P2 : S P2 : NS	GLOBAL	0x50050400 0x40050400	US	S	NA	Yes	General purpose input and output, port P2 Does not support pin sense mechanism, and DETECTMODE register has no effect. Supports extra high drive (DRIVE0=E0, DRIVE1=E1).
P1 : S P1 : NS	GLOBAL	0x500D8200 0x400D8200	US	S	NA	Yes	General purpose input and output, port P1
P0 : S P0 : NS	GLOBAL	0x5010A000 0x4010A000	US	S	NA	Yes	General purpose input and output, port P0

Configuration

Instance	Domain	Configuration
P2 : S P2 : NS	GLOBAL	P2 has 11 pins, P2.00 through P2.10.
P1 : S P1 : NS	GLOBAL	I/O pins on this port have pin sense mechanism P1 has 17 pins, P1.00 through P1.16.
P0 : S P0 : NS	GLOBAL	I/O pins on this port have pin sense mechanism P0 has 7 pins, P0.00 through P0.06.