Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	BYPASS			Enable or disable bypass of LFCLK crystal oscillator with external clock source
			Disabled	0	Disable (use crystal)
			Enabled	1	Enable (use rail-to-rail external source)

5.5.4.3.2 XOSC32KI.INTCAP (Retained)

Address offset: 0x904

Programmable capacitance of XL1 and XL2

Use the provided equation in OSCILLATORS — Oscillator control on page 86 to calculate the register value.

This register is retained.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A
Reset 0x00000017				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 1**
ID	R/W	Field	Value ID	Value	Description
A	RW	VAL			Crystal load capacitor as seen by the crystal across its terminals, including pin capacitance but excluding PCB stray capacitance. Use the provided equation in "Using internal capacitors section" to calculate the register value.

5.6 POWER — Power control

The POWER peripheral provides an interface for the power and clock subsystem for task, event, and interrupt related settings.

The POWER peripheral requests resources from the power and clock subsystem. The power and clock subsystem makes sure that the power mode with the proper latency settings is selected when requested. This means that the Constant Latency mode is prioritized over Low-power mode. For an overview of power modes, see Sub-power modes on page 67.

The event POFWARN is a system level event that enables the device to react quickly if there is a power failure. The power-fail comparator must be configured and enabled to receive the event, see Power-fail comparator on page 69 for more information.

Power control of the RAM blocks is controlled by the memory configuration peripheral (MEMCONF), see MEMCONF — Memory configuration on page 44.

Note: Registers INTEN on page 95, INTENSET on page 96, and INTENCLR on page 96 are shared between the POWER and CLOCK peripherals.