Operation modes

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

ID	R/W	Field	Value ID	Value	Description
A	RW	BITREVERSE			Reverse the endianness on bit level for the ECB output, INITIATOR, and REFLECTOR registers
					Enable bit reversal on each byte.
			Default	0	Default endianness
			Reversed	1	Reversed endianness

8.7 EGU — Event generator unit

Event generator unit (EGU) provides support for interlayer signaling. This means providing support for atomic triggering of both CPU execution and hardware tasks, from both firmware (by CPU) and hardware (by PPI). This feature can be used for triggering CPU execution at a lower priority execution from a higher priority execution, or to handle a peripheral's interrupt service routine (ISR) execution at a lower priority for some of its events. However, triggering any priority from any priority is possible.

Listed here are the main EGU features:

- Software-enabled interrupt triggering
- Separate interrupt vectors for every EGU instance
- Up to 16 separate event flags per interrupt for multiplexing

Each instance of EGU implements a set of tasks which can individually be triggered to generate the corresponding event. For example, the corresponding event for TASKS_TRIGGER[n] is EVENTS_TRIGGERED[n]. See for a list of EGU instances.

8.7.1 Registers

Instances

Instance	Domain	Base address	TrustZone			Split	Description
			Map	Att	DMA	access	
EGU10 : S	GLOBAL	0x50087000	US	S	NA	No	Event generator unit EGU10
EGU10 : NS		0x40087000					
EGU20 : S	GLOBAL	0x500C9000	US	S	NA	No	Event generator unit EGU20
EGU20 : NS		0x400C9000					

Configuration

Instance	Domain	Configuration
EGU10 : S	GLOBAL	16 events
EGU10 : NS		
EGU20 : S	GLOBAL	6 events
EGU20 : NS		

NORDIC
SEMICONDUCTOR