Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	W	TASKS_PREPARERX			Prepare the TWI slave to respond to a write command
			Trigger	1	Trigger task

8.24.10.5 TASKS_PREPARETX

Address offset: 0x024

Prepare the TWI slave to respond to a read command

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	W	TASKS_PREPARETX			Prepare the TWI slave to respond to a read command
			Trigger	1	Trigger task

8.24.10.6 TASKS_DMA

Peripheral tasks.

8.24.10.6.1 TASKS_DMA.RX

Peripheral tasks.

8.24.10.6.1.1 TASKS_DMA.RX.ENABLEMATCH[n] (n=0..3)

Address offset: 0x030 + (n × 0x4)

Enables the MATCH[n] event by setting the ENABLE[n] bit in the CONFIG register.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	W	ENABLEMATCH			Enables the MATCH[n] event by setting the ENABLE[n] bit in the CONFIG register.
			Trigger	1	Trigger task

8.24.10.6.1.2 TASKS_DMA.RX.DISABLEMATCH[n] (n=0..3)

Address offset: 0x040 + (n × 0x4)

Disables the MATCH[n] event by clearing the ENABLE[n] bit in the CONFIG register.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	W	DISABLEMATCH			Disables the MATCH[n] event by clearing the ENABLE[n] bit in the CONFIG register.
			Trigger	1	Trigger task