10 Hardware and layout

10.1 Pin assignments

The pin assignment figures and tables describe the pinouts for the product variants of the device.

As a general rule, peripherals must use GPIO pins in their own domain for all peripheral functions when selected in the PSEL register. Dedicated clock pin requirements are listed in Clock pins on page 860. In addition, there are some dedicated pin functions that allow pin connections between different power domains.

The block diagram shows which peripheral and port belong together, see Block diagram on page 9.

GPIO ports have their own properties. For details, see GPIO — General purpose input/output on page 274.

10.1.1 Dedicated pins

Some pins on the device are dedicated for a specific purpose. GPIO pin routing and configuration is flexible. Some pins have limitations or recommendations for configuration and use.

Peripheral	Description
UARTE20/21	Can use any pin on P1. Can connect across power domains to dedicated pins on P2 as described in the notes following this table.
SPIM00	Has dedicated pins on P2. For 32 MHz operation, the pins must be configured using extra high drive E0/E1 configuration in the DRIVE0/1 fields of the PIN_CNF GPIO register.
SPIM20/21	Can use any pins on P1; see Clock pins on page 860. Can connect across power domains to dedicated pins on P2 as described in the notes following this table.
SPIS20/21	Can use any pins on P1; see Clock pins on page 860. Can connect across power domains to dedicated pins on P2 as described in the notes following this table.
TRACE	Has dedicated pins that must be configured using extra high drive E0/E1 configuration in the DRIVE0/1 fields of the PIN_CNF GPIO register.
GRTC	Has dedicated pins for clock and PWM output.
TAMPC	Has dedicated pins for active shield input and output.
FLPR	Uses dedicated pins on P2 for emulated peripherals such as QSPI.
RADIO	Uses dedicated pins on P1 for antenna switch control (DFEGPIO for direction finding).
NFC	Uses dedicated pins as listed in the pin assignments table for the selected device. These pins are configured as NFC antenna pins from reset. To use the pins for Digital I/O, NFC function must be disabled in the NFCT — Near field communication tag on page 359 peripheral.

Table 76: Dedicated pin functions