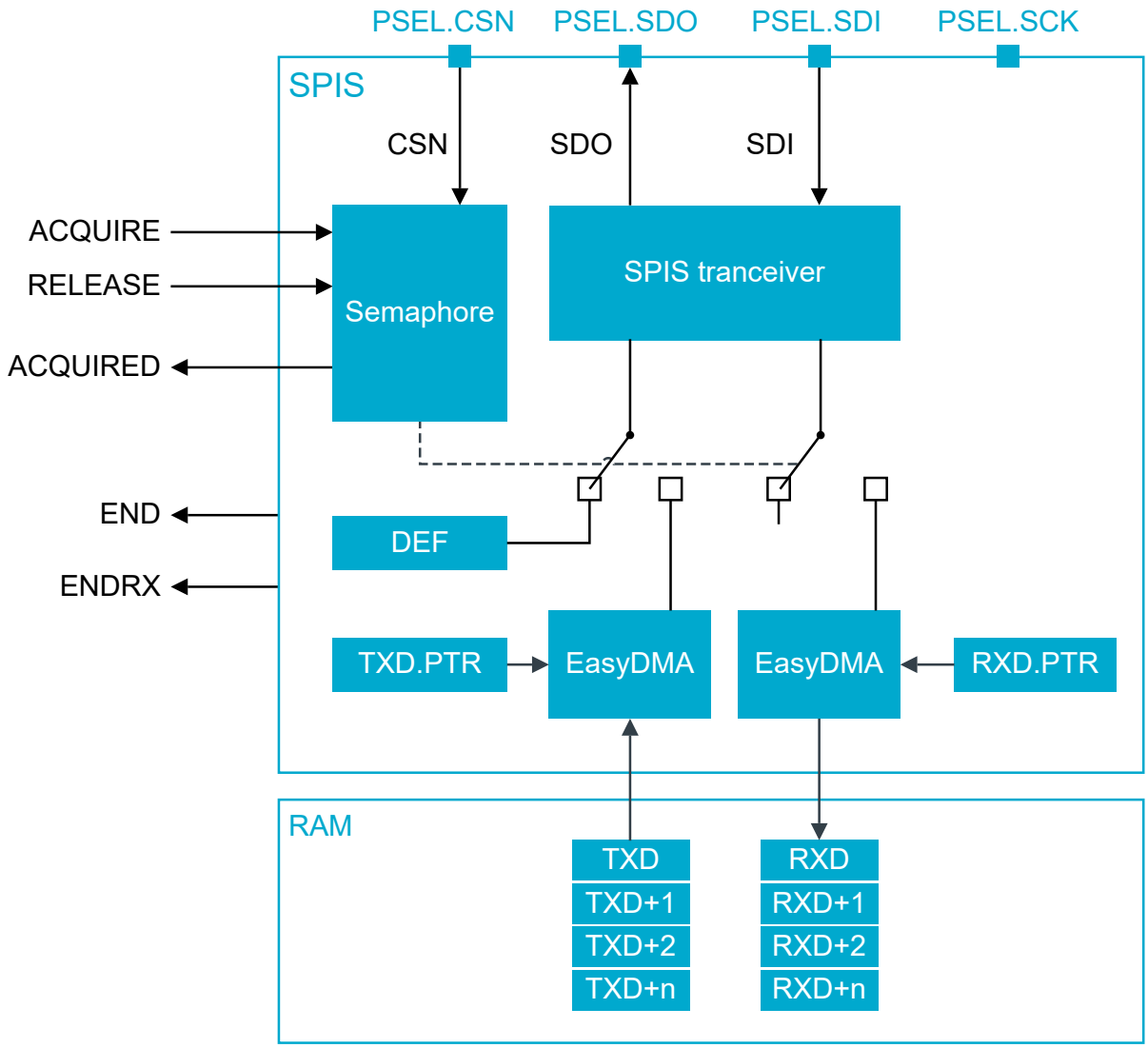

Figure 140: SPIS

8.20.1 SPI modes

SPIS supports SPI modes [0..3]. Modes CPOL and CPHA are set in the CONFIG register.

Mode	Clock polarity (CPOL)	Clock phase (CPHA)
SPI_MODE0	0 (Active `High`)	0 (Sample on Leading)
SPI_MODE1	0 (Active `High`)	1 (Sample on Trailing)
SPI_MODE2	1 (Active `Low`)	0 (Sample on Leading)
SPI_MODE3	1 (Active `Low`)	1 (Sample on Trailing)

Table 61: SPI modes

8.20.2 Shared resources

The SPIS peripheral shares registers and other resources with peripherals that have the same ID as SPIS. Before SPIS can be configured and used, all peripherals that have the same ID as SPIS must be disabled.