Module	Description	Implemented
MPU	Number of non-secure MPU regions	16
	Number of secure MPU regions	16
SAU	Number of SAU regions	4
FPU	Floating-point unit	Yes
DSP	Digital Signal Processing Extension	Yes
Arm TrustZone for Armv8-M	Armv8-M Security Extensions	Yes
CPIF	Coprocessor interface	No
ETM	Embedded Trace Macrocell	Yes
ITM	Instrumentation Trace Macrocell	Yes
MTB	Micro Trace Buffer	No
CTI	Cross Trigger Interface	No
BPU	Breakpoint Unit	Yes
INITSVTOR	Initial secure vector table offset	0x00000000
INITNSVTOR	Initial non-secure vector table offset	0x00000000

Table 13: Modules

4.1.2 CPUC — CPU control

CPUC controls elements of the Arm Cortex-M33 processor such as enabling floating-point exceptions. It is also able to lock certain features of the CPU and prevent them from being modified.

CPUC can generate events and CPU interupts for exceptions in the floating point unit (FPU), as shown in the following block diagram. Examples of such exceptions are divide-by-zero or floating-point overflow.

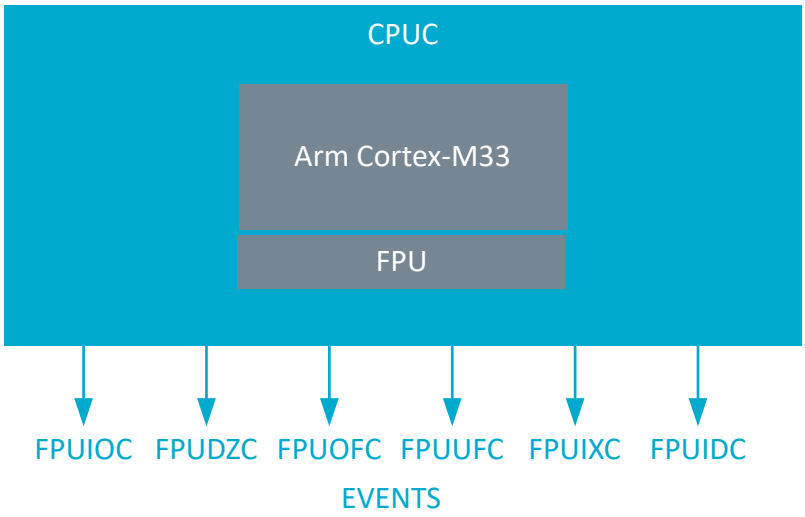

Figure 4: Block diagram

CPUC holds a CPU identifier CPUID, used in the system to uniquely identify the processing unit of a core.