8.3.8.2 LIMP in SPI Control Mode

In SPI control mode, the LIMP pin defaults to the limp home function. When fail-safe mode is enabled (default on) the pin behaves the same as stated in pin control mode with the exception of every watchdog error causing a reset. Programming register 8'h1A[3:2], LIMP_SEL_RESET, determines the condition for the LIMP pin to turn off. The three modes that the LIMP pin changes state is normal, fail-safe and standby mode. When in normal and standby mode the LIMP pin is off unless there is a watchdog failure event, which turns on the LIMP pin. When entering these two modes, there is an initial long window requiring a watchdog input trigger. This is treated as a WD failure and LIMP pin turns on if the window is missed. Any event that causes the device to enter fail-safe mode also turns on the LIMP pin. LIMP is turned off once the device enters standby mode from fail-safe mode except for a watchdog error as described previously. When fail-safe mode is disabled, a WD input failure causes the LIMP pin to turn on, and the device enters restart mode.

If the LIMP function is not needed, this pin can be configured to support either a high side switch in SPI mode by using register 8'h1B[7:6] = 01b or to the INH function by setting register 8'h1B[7:6] = 10b. When configured as a high side switch, the pin can support the same load as the HSS pin, but does not have the open load and over current detection features. When used as a high side switch, timing control is configurable using on/off, PWM or timer based. When using PWM, PWM1 or PWM2 can be assigned. When using the timer, timer1 or timer2 and be assigned.

8.3.9 nWDR/SDO (Watchdog Timeout Reset Output/SPI Serial Data Out)

When configured for pin control, the nWDR/SDO pin becomes the watchdog reset output pin, nWDR. When the watchdog times out, this pin goes low for time of 15 ms and then releases back to V_{CC}.

When configured for SPI control, the nWDR/SDO pin becomes the SPI serial data output pin, SDO.

8.3.10 HSS (High-side Switch)

This pin supports a high-side switch supporting up to a 100 mA load with 60 mA being typical with a 14 V V_{SUP}. In SPI mode, the HSS can be programmed to support a 200 Hz or 400 Hz 10-bit PWM. PWM1 or PWM2 can be assigned to the HSS. The HSS can be configured to use one of two timers that allows it to work with the WAKE pin. This supports cyclic sensing for sleep mode thus reducing sleep mode current. In pin mode this pin is controlled by the HSSC pin.

The switch supports open load detection and over current detection. When an over current is detected, there is a filter time, t_{OCFLTR}, to determine if over current is valid. If valid there is a shut off time, t_{OCOFF}, time for the HSS to shut off. When the HSS shuts off due to an over current event the HSS has to be re-enabled. This is accomplished differently depending upon whether the device is in pin control or SPI control. If in SPI control it will also depend upon how the HSS is configured.

Pin Control:
- HSS is controlled by the input signal on the HSSC pin.
- Once the over current fault is removed a high to low transition on the HSSC pin will re-enable the HSS output.

SPI Control and HSS_EN; 8'h1E[7] = 1b (enabled):
- When HSS is configured as On or HSSC controlled, HSS_CNTL 8'h1E[6:4] = 000b or 101b, the HSS will have to have the HSS_EN; 8'h1E[7] set to 0b (disabled) and then reset to 1b (enabled) or will turn on when HSSC receives the signal described above in "Pin Control."
- When HSS is configured utilizing a PWM or Timer, HSS_CNTL 8'h1E[6:4] = PWM1, PWM2, Timer1 or Timer2, the HSS will automatically turn on.

Note
- For resistive loads, an external capacitor to ground in not required.
- For inductive loads, an external 100 nF capacitor to ground is needed.
- When using the 10-bit PWM with the HSS or LIMP configured as a HSS, it is possible to select values that are unrealizable due to the on and off times of the switch. An example of this would be 00 0000 0001b

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