Configuration

Instance	Domain	Configuration
VPRCSR	FLPR	VEVIF indexes 16 through 19 maps onto DPPI channels 0 through 4 Use GPIO port P2 HARTNUM: 14 MCLICBASE: 0xF0000000 MULDIV: 2 HIBERNATE: 1 DBG: 1 Code patching (REMAP): 0 BUSWIDTH: 64 BKPT: 1 VPR can be retained. CSR VIOPINS value: 0x0000FFFF VEVIF tasks: 0..31 Mask of supported VEVIF tasks: 0xFFFFFFFF VEVIF DPPI indices: 16..19 VEVIF events: 0..31 Bit-Manipulation extension: 1 CACHE available. CACHEEXTRATAGBUF: 0 OUTMODE for shifting functionality available INSTNUM field is not available withing CSR MIMPID VPR does not support peripheral blocking access. VPR does not support branch predecoding.

Register overview

Register	Offset	Description
MSTATUS	0x300	Machine Status
MISA	0x301	Machine ISA
MTVEC	0x305	Machine Trap-Vector
MTVT	0x307	Machine Trap Vector Table
MCOUNTINHIBIT	0x320	Machine Counter-Inhibit
MSCRATCH	0x340	Machine Scratch
MEPC	0x341	Machine Exception Program Counter
MCAUSE	0x342	Machine Cause
MTVAL	0x343	Machine Trap Value
MINTSTATUS	0x346	M-mode Interrupt Status
MINTTHRESH	0x347	M-mode Interrupt-level Threshold
MCLICBASE	0x350	Machine CLIC Base
TSELECT	0x7A0	Trigger Select
TDATA1	0x7A1	Trigger Data 1
TDATA2	0x7A2	Trigger Data 2
TDATA3	0x7A3	Trigger Data 3