Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	B B B B B A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0

ID	R/W	Field	Value ID	Value	Description
A	RW	WEN			Write enable
			Disabled	0	Write is disabled
			Enabled	1	Write is enabled
B	RW	WRITEBUFSIZE		0..32	write-buffer size in number of 128-bit words
			Unbuffered	0	Disable buffering

4.2.6.7.22 READYNEXTTIMEOUT

Address offset: 0x50C

Configuration for ready next timeout counter, in units of AXI clock frequency

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	B A A A A A A A A A A A A
Reset 0x00000080	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0

ID	R/W	Field	Value ID	Value	Description
A	RW	VALUE		[0..4095]	Preload value for waiting for a next write
B	RW	EN			Enable ready next timeout
					The timeout value is number of RRAMC clock cycles. The timeout starts when the READYNEXT is set to ready
			Disable	0	Disable ready next timeout
			Enable	1	Enable ready next timeout

4.2.6.7.23 POWER.CONFIG

Address offset: 0x510

Power configuration

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	B A A A A A A A A A A A A A A A A
Reset 0x00000100	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0

ID	R/W	Field	Value ID	Value	Description
A	RW	ACCESSTIMEOUT			Access timeout, in 31.25 ns units, used for going into standby power mode or remain active on wake up
					The timeout counter counts down and is restarted on every RRAM access and on event WOKENUP
B	RW	POF			Power on failure warning handling configuration
			Wait	0	Wait until the current RRAM write finishes
			Abort	1	Abort the current RRAM write

4.2.6.7.24 POWER.LOWPOWERCONFIG

Address offset: 0x518

Low power mode configuration

The RRAMC low power mode is entered while the device goes into system on idle