8.22.5.20 CC[n] (n=0..7)

Address offset: 0x540 + (n × 0x4)

Capture/Compare register n

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	CC																																	

Capture/Compare value

Only the number of bits indicated by BITMODE will be used by the TIMER.

8.22.5.21 ONESHOTEN[n] (n=0..7)

Address offset: 0x580 + (n × 0x4)

Enable one-shot operation for Capture/Compare channel n

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	ONESHOTEN																																	

Configures the corresponding compare-channel for one-shot operation

Disable 0 — Disable one-shot operation

Compare event is generated every time the Counter matches CC[n]

Enable 1 — Enable one-shot operation

Compare event is generated the first time the Counter matches CC[n] after CC[n] has been written

8.23 TWIM — I²C compatible two-wire interface controller with EasyDMA

The TWI controller peripheral (TWIM) with EasyDMA provides a half duplex, two-wire synchronous serial communication interface which supports multiple targets in the same bus.

The main features of TWIM are the following:

- I²C compatible for 100 kbps and 400 kbps
- 1000 kbps bit rate support for selected pull-up resistor/bus capacitance combinations
- Supported baud rates:
  - 100 kbps
  - 400 kbps
  - 1000 kbps
- EasyDMA direct transfer to and from RAM
- Individual selection of I/O pins
- Support for clock stretching
- Transmissions can be suspended and resumed