Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	G F E D C B A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

ID	R/W	Field	Value ID	Value	Description
A-D	RW	INSTEN[i] (i=0..3)			Instruction event enable field.
			Disabled	0	The trace unit does not generate an Event element.
			Enabled	1	The trace unit generates an Event element for event i, in the instruction trace stream.
E	RW	DATAEN			Data event enable bit.
			Disabled	0	The trace unit does not generate an Event element if event 0 occurs.
			Enabled	1	The trace unit generates an Event element in the data trace stream if event 0 occurs.
F	RW	ATB			AMBA Trace Bus (ATB) trigger enable bit.
			Disabled	0	ATB trigger is disabled.
			Enabled	1	ATB trigger is enabled. If a CoreSight ATB interface is implemented then when event 0 occurs the trace unit generates an ATB event.
G	RW	LPOVERRIDE			Low-power state behavior override bit. Controls how a trace unit behaves in low-power state.
			Disabled	0	Trace unit low-power state behavior is not affected. That is, the trace unit is enabled to enter low-power state.
			Enabled	1	Trace unit low-power state behavior is overridden. That is, entry to a low-power state does not affect the trace unit resources or trace generation.

9.8.1.7 TRCSTALLCTLR

Address offset: 0x2C

Enables trace unit functionality that prevents trace unit buffer overflows.

Might ignore writes when the trace unit is enabled or not idle.

Must be programmed if TRCIDR3.STALLCTL == 1.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	G F E D C B A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

ID	R/W	Field	Value ID	Value	Description
A	RW	LEVEL		[15:0]	Threshold level field.
					If LEVEL is nonzero then a trace unit might suppress the generation of:
					Global timestamps in the instruction trace stream and the data trace stream.
					Cycle counting in the instruction trace stream, although the cumulative cycle count remains correct.
			Min	0	Zero invasion. This setting has a greater risk of a FIFO overflow
			Max	15	Maximum invasion occurs but there is less risk of a FIFO overflow.
B	RW	ISTALL			Instruction stall bit. Controls if a trace unit can stall the PE when the instruction trace buffer space is less than LEVEL.
			Disabled	0	The trace unit must not stall the PE.
			Enabled	1	The trace unit can stall the PE.
C	RW	DSTALL			Data stall bit. Controls if a trace unit can stall the PE when the data trace buffer space is less than LEVEL.
			Disabled	0	The trace unit must not stall the PE.
			Enabled	1	The trace unit can stall the PE.

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