

This sets or returns the value of counter n.

The count value is only stable when TRCSTATR.PMSTABLE == 1.

If software uses counter n then it must write to this register to set the initial counter value.

Might ignore writes when the trace unit is enabled or not idle.

9.8.1.28 TRCRSCTLR[n] (n=2..31)

Address offset: $0x200 + (n \times 0x4)$

Controls the selection of the resources in the trace unit.

Might ignore writes when the trace unit is enabled or not idle.

If software selects a non-implemented resource then CONSTRAINED UNPREDICTABLE behavior of the resource selector occurs, so the resource selector might fire unexpectedly or might not fire. Reads of the TRCRSCTRLn might return UNKNOWN.

9.8.1.29 TRCSSCCR0

Address offset: 0x280

Controls the single-shot comparator.

9.8.1.30 TRCSSCSRO

Address offset: 0x2A0

Indicates the status of the single-shot comparators. TRCSSCSR0 is sensitive to instruction addresses.