Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	TRACEID			Trace ID field. Sets the trace ID value for instruction trace. Bit[0] must be zero if data trace is enabled. If data trace is enabled then a trace unit sets the trace ID for data trace, to TRACEID+1.

9.8.1.13 TRCQCTLR

Address offset: 0x44

Controls when Q elements are enabled.

Might ignore writes when the trace unit is enabled or not idle.

This register must be programmed if it is implemented and TRCCONFIGR.QE is set to any value other than 0b00.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-H	RW	RANGE[i] (i=0..7)			Specifies the address range comparators to be used for controlling Q elements.
			Disabled	0	Address range comparator i is disabled.
			Enabled	1	Address range comparator i is selected for use.
I	RW	MODE			Selects whether the address range comparators selected by the RANGE field indicate address ranges where the trace unit is permitted to generate Q elements or address ranges where the trace unit is not permitted to generate Q elements:
			Exclude	0	Exclude mode. The address range comparators selected by the RANGE field indicate address ranges where the trace unit cannot generate Q elements. If no ranges are selected, Q elements are permitted across the entire memory map.
			Include	1	Include mode. The address range comparators selected by the RANGE field indicate address ranges where the trace unit can generate Q elements. If all the implemented bits in RANGE are set to 0 then Q elements are disabled.

9.8.1.14 TRCVICTLR

Address offset: 0x080

Controls instruction trace filtering.

Might ignore writes when the trace unit is enabled or not idle.

Only returns stable data when TRCSTATR.PMSTABLE == 1.

Must be programmed, particularly to set the value of the SSSTATUS bit, which sets the state of the start/stop logic.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				L K J I H G F E D C B A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	EVENT_SEL			Select which resource number should be filtered.