- All registers are reset to default values
- PWRON flag is set is with a hard reset (if previously cleared)

When pulling nRST pin low and releasing (SPI or PIN Mode), the following takes place:

- Device transitions to restart mode, nRST pin is pulled low for t_{NRST_TOG} and then transitions to standby mode.
- All registers retain the same value as before nRST reset
- V_{CC} stays in the same state it was in
- All pending interrupts are retained
- INH stays ON

8.3.22.3 TXD Dominant Time Out (DTO)

During normal mode, if TXD is inadvertently driven permanently low by a hardware or software application failure, the LIN bus is protected by the dominant state timeout timer. This timer is triggered by a falling edge on the TXD pin. If the low signal remains on TXD for longer than t_{TXD_DTO}, the transmitter is disabled, thus allowing the LIN bus to return to recessive state and communication to resume on the bus. The protection is cleared and the t_{TXD_DTO} timer is reset by a rising edge on TXD. The TXD pin has an internal pull-up to make sure the device fails to a known recessive state if TXD is disconnected. During this fault, the transceiver remains in normal mode (assuming no change of stated request on EN), the RXD pin reflects the LIN bus and the LIN bus pull-up termination remains on. The TLIN1431x-Q1 can turn off TXD dominant state timeout when in SPI mode by using register 8'h1D[5] = 1b.

8.3.22.4 Bus Stuck Dominant System Fault: False Wake Up Lockout

The device contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake-up logic is locked out until a valid recessive on the bus “clears” the bus stuck dominant, preventing excessive current use. Figure 8-11 and Figure 8-12 show the behavior of this protection.

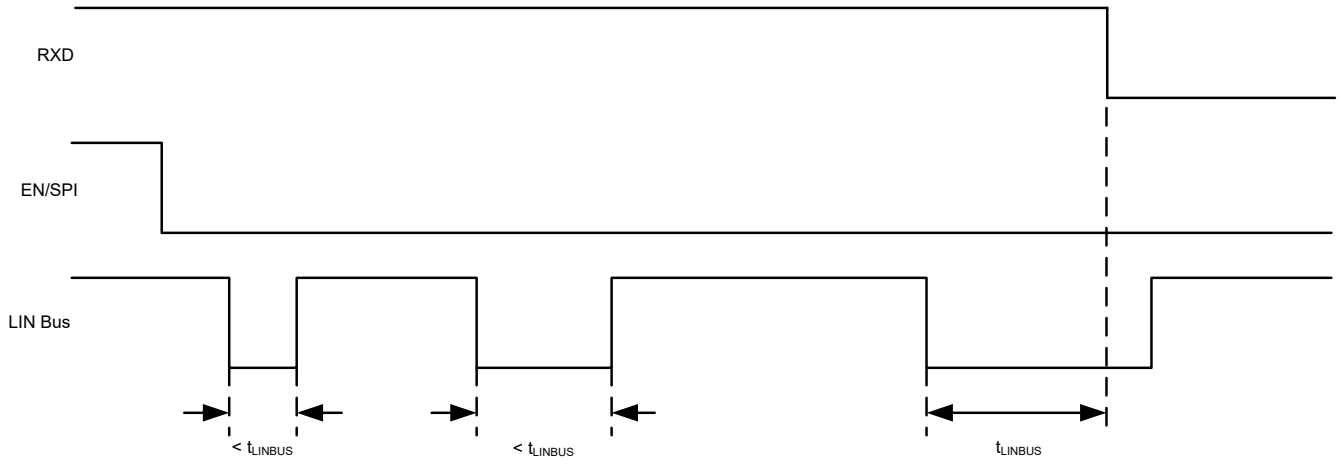

Figure 8-11. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wake Up