Reset reason

Before entering System OFF mode, the RESETREAS register must be cleared.

> **Note:** Unless cleared, the RESETREAS register will be cumulative. A field is cleared by writing 1 to it.

Bit number					31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID					N M L K J I H G F E D C B A
Reset 0x00000000					**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	RESETPIN			Reset from pin reset detected CTRL-AP generating a pin reset has its own bit
			NotDetected	0	Not detected
			Detected	1	Detected
B	RW	DOG0			Reset from watchdog timer 0 detected
			NotDetected	0	Not detected
			Detected	1	Detected
C	RW	DOG1			Reset from watchdog timer 1 detected
			NotDetected	0	Not detected
			Detected	1	Detected
D	RW	CTRLAPSOFT			Soft reset from CTRL-AP detected
			NotDetected	0	Not detected
			Detected	1	Detected
E	RW	CTRLAPHARD			Reset due to CTRL-AP hard reset
			NotDetected	0	Not detected
			Detected	1	Detected
F	RW	CTRLAPPIN			Reset due to CTRL-AP pin reset
			NotDetected	0	Not detected
			Detected	1	Detected
G	RW	SREQ			Reset from soft reset detected
			NotDetected	0	Not detected
			Detected	1	Detected
H	RW	LOCKUP			Reset from CPU lockup detected
			NotDetected	0	Not detected
			Detected	1	Detected
I	RW	OFF			Reset due to wakeup from System OFF mode when wakeup is triggered by DETECT signal from GPIO
			NotDetected	0	Not detected
			Detected	1	Detected
J	RW	LPCOMP			Reset due to wakeup from System OFF mode when wakeup is triggered by ANADETECT signal from LPCOMP
			NotDetected	0	Not detected
			Detected	1	Detected
K	RW	DIF			Reset triggered by Debug Interface
			NotDetected	0	Not detected
			Detected	1	Detected
L	RW	GRTC			Reset due to wakeup from GRTC
			NotDetected	0	Not detected
			Detected	1	Detected
M	RW	NFC			Reset after wakeup from System OFF mode due to NFC field being detected
			NotDetected	0	Not detected
			Detected	1	Detected