8.20.5 Semaphore operation

The semaphore is a mechanism implemented inside the SPIS peripheral that prevents SPIS and CPU from accessing data buffers simultaneously.

By default, the semaphore is assigned to the CPU after the SPIS peripheral is enabled. An ACQUIRED event will not be generated for this initial semaphore handover. If the ACQUIRE task is triggered while the semaphore is assigned to the CPU, an ACQUIRED event will be generated immediately. The following figure illustrates the transitions between states in the semaphore based on the relevant tasks and events.

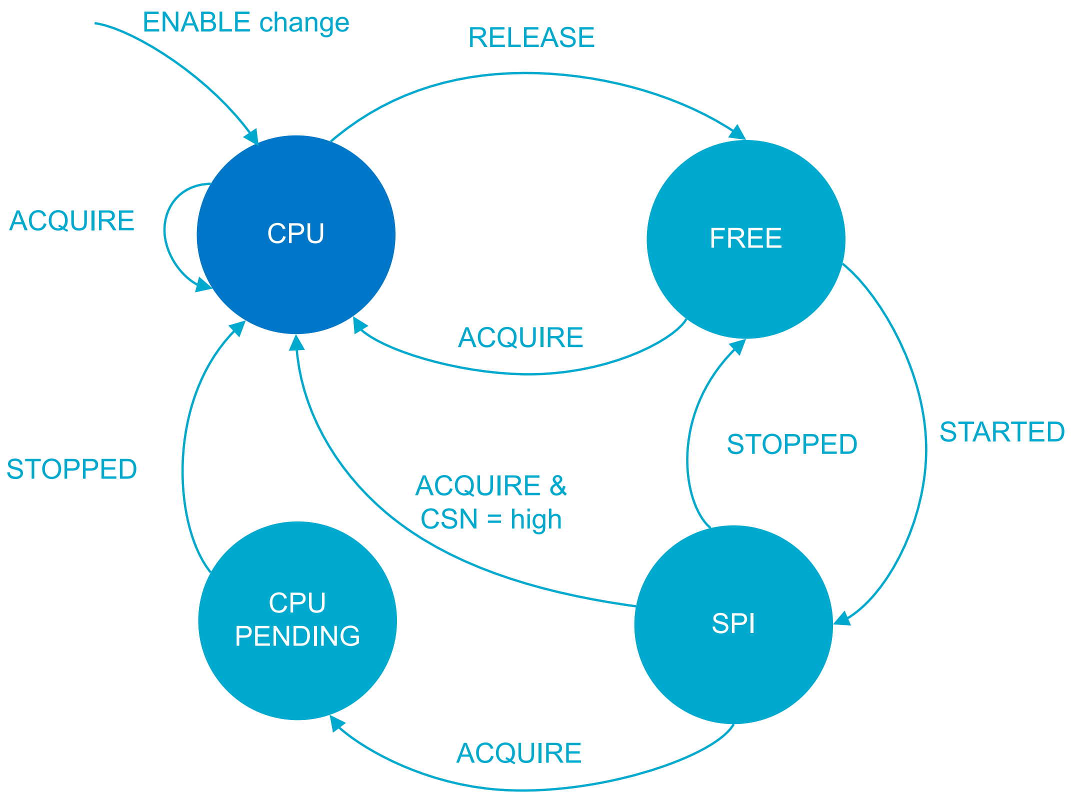

Figure 142: SPI semaphore FSM

> **Note:** The semaphore mechanism does not prevent the CPU from performing read or write access to the RXD.PTR register, TXD.PTR registers, or RAM that these pointers are pointing to. The semaphore is only telling when these can be updated by the CPU so that safe sharing is achieved.

SPIS will try to acquire the semaphore when the STARTED event is detected. If SPIS does not obtain the semaphore, the transaction will be ignored and the semaphore is retained by the CPU. All incoming data on SDI will be discarded and the DEF (default) character will be clocked out on the SDO line throughout the transaction. This is also true if the semaphore is released by the CPU during the transaction. If a race condition occurs where the CPU and SPIS try to acquire the semaphore at the same time, as illustrated in lifeline item 2 in figure SPI transaction when shortcut between END and ACQUIRE is enabled on page 613, the CPU is given the semaphore.

If SPIS acquires the semaphore, the transaction will be granted. The incoming data on SDI will be stored in the RXD buffer and the data in the TXD buffer will be clocked out on SDO.

When a transaction is complete and CSN goes `HIGH`, SPIS will automatically release the semaphore and generate the END event.

SPIS can be granted multiple transactions in a row as long as the semaphore is available.