Only one peripheral can be assigned to drive a GPIO pin at a time. Failing to do so may result in unpredictable behavior.

TWIS signal	TWIS pin	Direction	Output value	Drive strength
SCL	As specified in PSEL.SCL	Input	Not applicable	S0D1
SDA	As specified in PSEL.SDA	Input	Not applicable	S0D1

Table 68: GPIO configuration before enabling peripheral

8.24.10 Registers

Instances

Instance	Domain	Base address	TrustZone			Split access	Description
			Map	Att	DMA		
TWIS20 : S TWIS20 : NS	GLOBAL	0x500C6000 0x400C6000	US	S	SA	No	Two-wire interface target TWIS20
TWIS21 : S TWIS21 : NS	GLOBAL	0x500C7000 0x400C7000	US	S	SA	No	Two-wire interface target TWIS21
TWIS22 : S TWIS22 : NS	GLOBAL	0x500C8000 0x400C8000	US	S	SA	No	Two-wire interface target TWIS22
TWIS30 : S TWIS30 : NS	GLOBAL	0x50104000 0x40104000	US	S	SA	No	Two-wire interface target TWIS30

Configuration

Instance	Domain	Configuration
TWIS20 : S TWIS20 : NS	GLOBAL	Use GPIO port P1
TWIS21 : S TWIS21 : NS	GLOBAL	Use GPIO port P1
TWIS22 : S TWIS22 : NS	GLOBAL	Use GPIO port P1
TWIS30 : S TWIS30 : NS	GLOBAL	Use GPIO port P0

Register overview

Register	Offset	TZ	Description
TASKS_STOP	0x004		Stop TWI transaction
TASKS_SUSPEND	0x00C		Suspend TWI transaction
TASKS_RESUME	0x010		Resume TWI transaction
TASKS_PREPARERX	0x020		Prepare the TWI slave to respond to a write command
TASKS_PREPARETX	0x024		Prepare the TWI slave to respond to a read command
TASKS_DMA.RX.ENABLEMATCH[n]	0x030		Enables the MATCH[n] event by setting the ENABLE[n] bit in the CONFIG register.
TASKS_DMA.RX.DISABLEMATCH[n]	0x040		Disables the MATCH[n] event by clearing the ENABLE[n] bit in the CONFIG register.
SUBSCRIBE_STOP	0x084		Subscribe configuration for task STOP