8.3.22.8 Floating Pins

There are internal pull ups and pull downs on critical terminals to place the device into known states if the terminal floats. See Table 8-2 for details on terminal bias conditions.

Table 8-2. Internal Pull-ups and Pull-downs on Device Pins

Pin	Pull-up or Pull-down	Typical Value	Comment
TXD	Pull-up	350 kΩ	
WDT/CLK	Pull-up	240 kΩ	When device configured for SPI control, CLK
WDI/SDI	Pull-up	240 kΩ	
PIN/nCS	Pull-up	240 kΩ	When device configure for SPI control, nCS
DIV_ON	Pull-down	370 kΩ	
LIN	Pull-up	45 kΩ	
EN/nINT	Pull-down	350 kΩ	
HSSC/FSO	Pull-down	350 kΩ	
nRST	Pull-up	45 kΩ	

8.3.22.9 V_{CC} Voltage Regulator

The device has an integrated high-voltage input LDO that operates over a 5.5 V to 28 V input voltage range for both 3.3 V and 5 V V_{CC}. The device has an output current capability of 125 mA and support fixed output voltages of 3.3 V (TLIN14313-Q1) or 5 V (TLIN14315-Q1). It features thermal shutdown and short-circuit protection to prevent damage during over-temperature and over current conditions

8.3.22.9.1 Under or Over Voltage and Short Circuit

The V_{CC} pin is the current limited regulated output based supporting an accuracy of ±2.5%. In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UV_{SUP} threshold, the regulator turns off until the input voltage returns above the UV_{SUPR} level. When 5 V LDO is used, the device uses the voltage regulator during Init mode to determine the WKRQ/INH function, and the IO voltage. The device monitors V_{CC} for under-voltage, over-voltage, short to ground and thermal events. The device control method and whether fail-safe mode is enabled determine the behavior of the of the device for these events. Fail-safe mode is always active when the device is in pin control. In SPI control, the state diagram shows two paths: fail-safe mode enabled and fail-safe mode disabled. The path followed depends on whether fail-safe mode is enabled or disabled in 8'h17[0] FSM_DIS.

For an under-voltage event, V_{CC} is less than or equal to UV_{CCF}. After a 30us filter time, the device pulls nRST low and after the t_{UVFLTR} time, the interrupt flag is set and device transitions to restart mode, if fail-safe disabled, or fail-safe mode. When entering either mode, the SWE timer t_{INACT_FS} starts, and, in SPI control, the mode counter increments and the appropriate interrupt flags are set. To exit fail-safe mode, the under-voltage has to clear and a wake event takes place prior to the SWE timer timing out. If the under-voltage event has not cleared when the wake event takes place or if the SWE timer times out, the device enters sleep mode. Figure 8-13 shows how a UV_{CC} event is handled..