Feature		Package			
		QFN40	QFN48	QFN52	CSP47
Pins	GPIO pins	24	31	35	32
	Wakeup-pins	15	20	24	21
	Analog input pins	7	8	8	8
Security	Active tamper shield pin pairs (in/out)	2	4	4	4
Debug	ITM parallel trace	No	Yes	Yes	No
Device	Package availability				
	nRF54L05	Yes	Yes	Yes	
	nRF54L10	Yes	Yes	Yes	
	nRF54L15	Yes	Yes	Yes	Yes

Table 7: Package variants

3.3 Power domains

Multiple power domains ensure low-power operation.

The MCU domain contains an Arm Cortex-M33. The CPU is connected to a debug system that allows debug and ETM trace. The CPU executes program code from RRAM through an instruction cache. Data is stored in single-cycle RAM that is divided into multiple bus subordinates forming a continuous RAM space in the memory map. High-speed peripherals are also found in the MCU domain.

There are three additional domains that have peripherals allocated to them. They are the following:

- Radio domain – Contains the short-range radio and supporting peripherals used by the radio protocol stack. It runs at 32 MHz synchronously with the MCU domain.
- Peripheral domain – Contains most peripherals. It runs at 16 MHz synchronously with the MCU domain.
- Low-power domain – Contains peripherals for ultra-low power modes and can be used to wake the rest of the system, even when the peripheral domain is powered off. It runs at 16 MHz asynchronously to the MCU domain.

Each domain is mapped to one APB bus and can be powered independently. EasyDMA traffic from each domain is aggregated in a local AMBIX interconnect and can access RAM in the MCU domain.

Power domains have their own GPIO ports. GPIO pins can be used by peripherals in the same power domain. For exceptions, see GPIO — General purpose input/output on page 274 and pin assignments.

3.4 Address format

Addresses in the system memory map follow the address format described in the following tables.