

Consequently, the LRCK frequency is equivalent to the audio sample rate.

When operating in Master mode, the LRCK is generated from the MCK, and the frequency of LRCK is then given as:

$$\text{LRCK} = \text{MCK} / \text{CONFIG.RATIO}$$

LRCK always toggles around the falling edge of the serial clock SCK.

8.11.4 Serial clock (SCK)

The serial clock (SCK), often referred to as the serial bit clock, pulses once for each data bit being transferred on the serial data lines SDIN and SDOUT.

When operating in Master mode, the SCK is generated from the MCK, and the frequency of SCK is then given as:

$$\text{SCK} = 2 * \text{LRCK} * \text{CONFIG.SWIDTH}$$

The falling edge of the SCK falls on the toggling edge of LRCK.

When operating in Slave mode, SCK is provided by the external I²S master.

8.11.5 Master clock (MCK)

The master clock (MCK) is the clock from which LRCK and SCK are derived when operating in Master mode.

The master clock generator always needs to be enabled when in Master mode, but the generator can also be enabled when in Slave mode. Enabling the generator when in Slave mode can be useful in the case where the external master is not able to generate its own master clock.

MCK is generated from the [CONFIG.MCKFREQ](#) registers.

The following equation can be used to calculate the value of [CONFIG.MCKFREQ](#) for given MCK and clock source frequency:

$$\text{MCKFREQ} = 4096 \cdot \left\lfloor \frac{\text{f}_{\text{MCK}} \cdot 1048576}{\text{f}_{\text{source}} + \frac{\text{f}_{\text{MCK}}}{2}} \right\rfloor$$

Figure 66: MCK clock frequency equation

The parameter f_{MCK} is the requested MCK clock frequency in Hz, and f_{source} is the frequency of the selected clock source in Hz. Because of rounding errors, an accurate MCK clock may not be achievable. The equation does not take into account the maximum register value of [CONFIG.MCKFREQ](#) on page 342.

The actual MCK frequency can be calculated using the equation below.

$$f_{\text{actual}} = \frac{f_{\text{source}}}{\left[\frac{1048576 \cdot 4096}{\text{MCKFREQ}} \right]}$$

Figure 67: Actual MCK clock frequency

The clock error can be calculated using the equation below. The error e is the percentage difference from the requested f_{MCK} frequency.

$$e = 100 \cdot \frac{f_{\text{actual}} - f_{\text{MCK}}}{f_{\text{MCK}}} = 100 \cdot \frac{\frac{f_{\text{source}}}{\left[\frac{1048576 \cdot 4096}{\text{MCKFREQ}} \right]} - f_{\text{MCK}}}{f_{\text{MCK}}}$$

Figure 68: MCK frequency error equation