

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				D C B A																															
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value	Description																														
B	RW	RESOLVED W1S			Write '1' to enable interrupt for event RESOLVED																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
C	RW	NOTRESOLVED W1S			Write '1' to enable interrupt for event NOTRESOLVED																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
D	RW	ERROR W1S			Write '1' to enable interrupt for event ERROR																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														

8.3.5.14 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID			D C B A																															
Reset 0x00000000			0 0																															
ID	R/W	Field	Value ID	Value	Description																													
A	RW	END W1C			Write '1' to disable interrupt for event END																													
			Clear	1	Disable																													
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													
B	RW	RESOLVED W1C			Write '1' to disable interrupt for event RESOLVED																													
			Clear	1	Disable																													
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													
C	RW	NOTRESOLVED W1C			Write '1' to disable interrupt for event NOTRESOLVED																													
			Clear	1	Disable																													
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													
D	RW	ERROR W1C			Write '1' to disable interrupt for event ERROR																													
			Clear	1	Disable																													
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													

8.3.5.15 ERRORSTATUS

Address offset: 0x404