

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
ID	R/W	Field		Value ID		Value		Description																									
A	RW	CNT						Number of additional PWM periods between samples loaded into compare register (load every REFRESH.CNT+1 PWM periods)																									
		Continuous		0				Update every PWM period																									

### 8.15.5.36 SEQ[n].ENDDELAY (n=0..1)

Address offset: 0x52C + (n × 0x20)

Time added after the sequence

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	R/W	Field		Value ID		Value		Description																									
A	RW	CNT						Time added after the sequence in PWM periods																									

### 8.15.5.37 PSEL.OUT[n] (n=0..3)

Address offset: 0x560 + (n × 0x4)

Output pin select for PWM channel n

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID	C																								B	B	B	A	A	A	A	A	A
Reset 0xFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
ID	R/W	Field		Value ID		Value		Description																									
A	RW	PIN		[0..31]				Pin number																									
B	RW	PORT		[0..7]				Port number																									
C	RW	CONNECT						Connection																									
		Disconnected		1				Disconnect																									
		Connected		0				Connect																									

### 8.15.5.38 DMA.SEQ[n].PTR (n=0..1)

Address offset: 0x704 + (n × 0x24)

RAM buffer start address

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	R/W	Field		Value ID		Value		Description																									
A	RW	PTR						RAM buffer start address for this EasyDMA channel. This address is a word aligned Data RAM address.																									

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 8.15.5.39 DMA.SEQ[n].MAXCNT (n=0..1)

Address offset: 0x708 + (n × 0x24)