

- P1 peripheral domain – These I/O pins can wake the system up from System OFF or System ON sleep, and can be accessed by all peripherals in the peripheral domain.
- P2 MCU domain – These I/O pins are faster and can be used for high-speed signals such as trace or fast serial peripheral communication. GPIO P2 cannot wake the system from sleep. P2 does not have the GPIO SENSE or DETECT mechanism, or GPIOTE.

Peripherals must use pins in their own domain. However, some P2 pins can be used for select serial interfaces in the peripheral domain when the device is in Constant Latency sub-power mode. This is not the most power-efficient way of connecting these serial interfaces, but adds flexibility when designing a circuit board. These pins must be configured and used only for the function listed in the pin assignments table, see [Pin assignments](#) on page 859. When setting up the peripheral's PSEL registers, it must be connected to the corresponding function listed in the pin assignments table, e.g. a UARTE TXD pin must be configured in a PSEL.TXD register. For more information about Constant Latency sub-power mode, see [Sub-power modes](#) on page 67.

Peripherals cannot mix pins from different ports. All pins must be on the same port.

The following table lists the port special functions and characteristics.

Port	Wakeup source	Extra high drive strength (EOE1)	Pin sense/detect	GPIOTE	Maximum speed [MHz]
P0	Yes	No	Yes	Yes	8
P1	Yes	No	Yes	Yes	8
P2	No	Yes	No	No	64

*Table 40: Port capabilities*

In addition to the capabilities of the port, some specific pins have additional functions. These are listed in [Pin assignments](#) on page 859.

#### 8.8.4 Peripheral and subsystem assignment

System GPIO pins can be allocated to peripherals with dedicated pins or subsystems such as trace and debug.

The pins of the system are listed in [Pin assignments](#) on page 859.

A pin can be assigned to any of the following:

- GPIO or peripheral with PSEL registers
- Peripheral with dedicated pins (VPR and GRTC)
- Trace and debug (TND) subsystem

By default, all pins are assigned to GPIO or peripherals with PSEL registers. This is the default value of the CTRLSEL value in register [PIN\\_CNF\[n\] \(n=0..31\) \(Retained\)](#) on page 284.

To allocate a pin to a peripheral or subsystem with dedicated pins, such as GRTC or TND, change the CTRLSEL value in register [PIN\\_CNF\[n\] \(n=0..31\) \(Retained\)](#) on page 284 for that pin. This will connect the pin to the subsystem or peripheral.

Only the peripheral or subsystem where the pin was allocated can observe and control that pin's state. Reading a pin that is not allocated to the current subsystem will return zero, and writes will be ignored. If a pin is allocated to a subsystem that cannot access it, the pin stays under control of the GPIO peripheral.

When CTRLSEL is used to allocate a peripheral or subsystem, reading the GPIO peripheral registers will not reveal the state of the pins.