Lock the access to the SEED register.

Note. If SEEDVALID was not written prior to SEEDLOCK, the write to SEEDLOCK will also mark the SEED as valid.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	ENABLE			Enable the lock
					Only possible to write a value 1.
			Disabled	0	Lock disabled.
			Enabled	1	Lock enabled.

7.8.1.6.12 PROTECTEDRAMLOCK

Address offset: 0x444

Lock the access to the protected RAM.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	ENABLE			Enable the lock
					Only possible to write a value 1.
			Disabled	0	Lock disabled.
			Enabled	1	Lock enabled.

7.8.1.7 Registers

Instances

Instance	Domain	Base address	TrustZone			Split access	Description
			Map	Att	DMA		
CRACENCORE	GLOBAL	0x51800000	HF	S	NSA	No	CRACEN core

Configuration

Instance	Domain	Configuration
CRACENCORE	GLOBAL	CRYPTMSTRDMA registers included
		CRYPTMSTRHW registers included
		RNGCONTROL registers included
		PK registers included
		IKG registers included
		RNGDATA registers included
		PKDATAMEMORY registers included
		PKUCODE registers included
		Using CRACENCORE configuration reset values