Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A
Reset 0x00000013				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 1**
ID	R/W	Field	Value ID	Value	Description
			Neg8dBm	0x9	-8 dBm
			Neg9dBm	0x8	-9 dBm
			Neg10dBm	0x7	-10 dBm
			Neg12dBm	0x6	-12 dBm
			Neg14dBm	0x5	-14 dBm
			Neg16dBm	0x4	-16 dBm
			Neg18dBm	0x3	-18 dBm
			Neg20dBm	0x2	-20 dBm
			Neg22dBm	0x2	-22 dBm
			Neg28dBm	0x1	-28 dBm
			Neg40dBm	0x130	-40 dBm
			Neg46dBm	0x110	-46 dBm
			MindBm	0x0	Minimum output power

8.17.14.113 TIFS

Address offset: 0x714

Interframe spacing in µs

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	TIFS			Interframe spacing in us. Interframe space is the time interval between two consecutive packets. It is defined as the time, in microseconds, from the end of the last bit of the previous packet to the start of the first bit of the subsequent packet.

8.17.14.114 RSSISAMPLE

Address offset: 0x718

RSSI sample

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A
Reset 0x0000007F				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1**
ID	R/W	Field	Value ID	Value	Description
A	R	RSSISAMPLE			RSSI sample result. The value of this register is read as a positive value while the actual received signal strength is a negative value. Actual received signal strength is therefore as follows: received signal strength = -A dBm.

8.17.14.115 RXGAIN.CONFIG

Address offset: 0x7D4

Override configuration of receiver gain control loop

Overriding the default values can result in unpredictable behavior

This register will not be reset by the SOFTRESET task