

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				P O N M																L K J I H G F E D C B A															
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value	Description																														
			Clear	1	Disable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
O	RW	PWMREADY W1C			Write '1' to disable interrupt for event PWMREADY																														
			Clear	1	Disable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
P	RW	CLKOUTREADY W1C			Write '1' to disable interrupt for event CLKOUTREADY																														
			Clear	1	Disable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														

8.10.7.28 INTPEND2

Address offset: 0x32C

Pending interrupts

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				P O N M				L K J I H G F E D C B A																											
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value	Description																														
A-L	R	COMPARE[i] (i=0..11)			Read pending status of interrupt for event COMPARE[i]																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
M	R	RTCOMPARESYNC			Read pending status of interrupt for event RTCOMPARESYNC																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
N	R	PWMPERIODEND			Read pending status of interrupt for event PWMPERIODEND																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
O	R	PWMREADY			Read pending status of interrupt for event PWMREADY																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
P	R	CLKOUTREADY			Read pending status of interrupt for event CLKOUTREADY																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														

8.10.7.29 INTEN3

Address offset: 0x330

Enable or disable interrupt

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																
ID				P O N M L K J I H G F E D C B A																																
Reset 0x00000000				0 0																																
ID	R/W	Field	Value ID	Value																Description																
A-L	RW	COMPARE[i] (i=0..11)			Enable or disable interrupt for event COMPARE[i]																															