In order to prevent spurious interrupts from the PORT event while configuring the sources, the following must be performed:

1. Disable interrupts on the PORT event (through INTENCLR.PORT).
2. Configure the sources (PIN_CNF[n].SENSE in GPIO).
3. Clear any potential event that could have occurred during configuration (write '0' to EVENTS_PORT).
4. Enable interrupts (through INTENSET.PORT).

## 8.9.3 Tasks and events pin configuration

Each GPIOTE channel is associated with one physical GPIO pin through the CONFIG.PSEL field.

When Event mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an input, overriding the DIR setting in GPIO. Similarly, when Task mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an output overriding the DIR setting and OUT value in GPIO. When Disabled is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will use its configuration from the PIN[n].CNF registers in GPIO.

For the range of possible CONFIG.PORT values in the product, see Instances on page 287. Writing other values may lead to undefined behavior.

**Note:** A pin can only be assigned to one GPIOTE channel at a time. Failing to do so may result in unpredictable behavior.

## 8.9.4 Split security attribute

Individual GPIOTE channels and interrupts can have independent security attributes.

GPIOTE is implemented with split security, meaning it handles accesses from both secure and non-secure code. GPIOTE channels and interrupts can be defined as secure or non-secure.

For more information on GPIOTE security attributes, see GPIOTE on page 132.

## 8.9.5 Registers

### Instances

| Instance | Domain | Base address | TrustZone | | | Split access | Description |
|---|---|---|---|---|---|---|---|
| | | | Map | Att | DMA | | |
| GPIOTE20 : S<br>GPIOTE20 : NS | GLOBAL | 0x500DA000<br>0x400DA000 | US | S | NA | Yes | 8 channels and 2 interrupts for GPIO port P1<br>GPIO tasks and events GPIOTE20 |
| GPIOTE30 : S<br>GPIOTE30 : NS | GLOBAL | 0x5010C000<br>0x4010C000 | US | S | NA | Yes | 4 channels and 2 interrupts for GPIO port P0<br>GPIO tasks and events GPIOTE30 |