Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				G F E E E E D C B B B A
Reset 0x00001000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
			8bit	8	8 bit data frame size.
			7bit	7	7 bit data frame size.
			6bit	6	6 bit data frame size.
			5bit	5	5 bit data frame size.
			4bit	4	4 bit data frame size.
F	RW	ENDIAN			Select if data is trimmed from MSB or LSB end when the data frame size is less than 8.
			MSB	0	Data is trimmed from MSB end.
			LSB	1	Data is trimmed from LSB end.
G	RW	FRAMETIMEOUT			Enable packet timeout.
			DISABLED	0	Packet timeout is disabled.
			ENABLED	1	Packet timeout is enabled.
			Disabled	0	Packet timeout is disabled.
			Enabled	1	Packet timeout is enabled.

8.25.13.31 ADDRESS

Address offset: 0x574

Set the address of the UARTE for RX when used in 9 bit data frame mode.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	ADDRESS			Set address

8.25.13.32 FRAMETIMEOUT

Address offset: 0x578

Set the number of UARTE bits to count before triggering packet timeout.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A
Reset 0x00000010				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	COUNTERTOP			Number of UARTE bits before timeout.

8.25.13.33 PSEL.TXD

Address offset: 0x604

Pin select for TXD signal