Figure 8-76. PWM1_CNTL2 Register (continued)

R-0b	R/W-00b

Table 8-32. PWM1_CNTL2L Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	PWM1_RSVD	R	0b	Reserved
1-0	PWM1_DC_MSB	R/W	00b	Most significant two bits for 10-bit PWM1 duty cycle select. Works with 'h21[7:0] 00b = 100% off when used with 'h21[7:0] and it is 00h xxb = on time with an increase of ~ 0.1% when used with 'h21[7:0] 11b = 100% of when used with 'h21[7:0] and it is FFh

Note

Minimum on-time during PWM is limited to the on and off-time of the high side switch. This will make certain PWM values unusable like 00 0000 0001.

8.6.23 PWM1_CNTL3 (Address = 21h) [reset = 00h]

PWM1_CNTL3 is shown in Figure 8-77 and described in Table 8-33

Return to Summary Table.

Bits 0 - 7 of the 10-bit PWM1. Used with register h'20[1:0] PWM1_CNTL2.

Figure 8-77. PWM1_CNTL3 Register

7	6	5	4	3	2	1	0
PWM1_DC							
R/W-00h							

Table 8-33. PWM1_CNTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWM1_DC	R/W	00h	Bits 0 - 7 of the 10-bit PWM1 00h = 100% off when used with 'h20[1:0] = 00b xxh = On time with an increase of ~ 0.1% when used with 'h20[1:0] FFh = 100% on when used with 'h20[1:0] = 11b

8.6.24 PWM2_CNTL1 (Address = 22h) [reset = 0h]

PWM2_CNTL1 is shown in Figure 8-78 and described in Table 8-34

Return to Summary Table.

Sets the pulse width modulation frequency, PWM2.

Figure 8-78. PWM2_CNTL1 Register

7	6	5	4	3	2	1	0
PWM2_FREQ	PWM2_FREQ_RSVD						
R/W-0b	R-0b						

Table 8-34. PWM2_CNTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWM2_FREQ	R/W	0b	PWM frequency select (Hz) 0b = 200 1b = 400
6-0	PWM2_FREQ_RSVD	R	0b	Reserved