Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				F F F F E D C C C B A A
Reset 0x40000003				**0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1**
ID	R/W	Field	Value ID	Value	Description
B	RW	STEP			Step When set and not in Debug Mode, the hart will only execute a single instruction and then enter Debug Mode. If the instruction does not complete due to an exception, the hart will immediately enter Debug Mode before executing the trap handler, with appropriate exception registers set. The debugger must not change the value of this bit while the hart is running
C	R	CAUSE			Debug Mode enter cause When there are multiple reasons to enter Debug Mode in a single cycle, hardware should set cause to the cause with the highest priority. Values other than the following are reserved for future use
			EBREAK	1	An ebreak instruction was executed. (priority 3)
			TRIGGER	2	The Trigger Module caused a breakpoint exception. (priority 4, highest)
			HALTREQ	3	The debugger requested entry to Debug Mode using haltreq. (priority 1)
			STEP	4	The hart single stepped because step was set. (priority 0, lowest)
			RESETHALTREQ	5	The hart halted directly out of reset due to resethaltreq. It is also acceptable to report 3 when this happens. (priority 2)
D	RW	STEPIE			Step Interrupt Enable The debugger must not change the value of this bit while the hart is running
			Disabled	0	Interrupts are disabled during single stepping
			Enabled	1	Interrupts are enabled during single stepping. Implementations may hard wire this bit to 0. In that case interrupt behavior can be emulated by the debugger.
E	RW	EBREAKM			M-mode ebreak
			SPEC	0	ebreak instructions in M-mode behave as described in the Privileged Spe
			ENTERDBG	1	ebreak instructions in M-mode enter Debug Mode
F	R	XDEBUGVER			External Debug version
			STDDBG	4	External debug support exists as it is described in this document

8.26.3.20 DPC

Address offset: 0x7B1

Debug PC

Upon entry to debug mode, dpc is updated with the virtual address of the next instruction to be executed. When resuming, the hart's PC is updated to the virtual address stored in dpc. A debugger may write dpc to change where the hart resumes

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	VAL			Debug PC value

8.26.3.21 MCYCLE

Address offset: 0xB00

Machine Cycle Counter

Counts the number of clock cycles executed by the processor core on which the hart is running