								Retained registers			
Reset source	**Cold boot**	**CM33**	**Peri-pher-als**	**De-bug**	**RAM**	**WDT**	**REGU-LATOR OSCI-LLA-TORS and CPU speed**	**RESET-REAS**	**POWE GP-RET-REG**	**GPIO**	**GRTC. SYS-COU-NTER**
CPU lockup		x	x							x[1]	x
Soft reset and CTRL-AP soft reset		x	x							x[1]	
Wakeup from System Off mode		x	x			x					
CTRL-AP hard reset		x	x	x	x	x	x			x	x
CTRL-AP pin reset		x	x	x	x	x	x			x	x
Watchdog timer reset		x	x	x	x	x	x			x	
Pin reset		x	x	x	x	x	x			x	x
TAMPC reset		x	x	x	x	x	x			x	x
GLITCHDET reset		x	x	x	x	x	x	x	x	x	x
Brownout reset	x	x	x	x	x	x	x	x	x	x	x
Power-on reset	x	x	x	x	x	x	x	x	x	x	x

Table 22: Reset overview

[1]Except the CTRLSEL field.

For TAMPC reset sources, see TAMPC — Tamper controller on page 192.

5.8.11 Registers

Instances

Instance	Domain	Base address	TrustZone			Split access	Description
			Map	Att	DMA		
RESET : S RESET : NS	GLOBAL	0x5010E000 0x4010E000	US	S	NA	No	Reset status

Register overview

Register	Offset	TZ	Description
RESETREAS	0x600		Reset reason

5.8.11.1 RESETREAS

Address offset: 0x600