Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				Q P P P P O N M L K J I H G F E D C B A
Reset 0x00040000				**0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
			TEST	1	Test data register (test mode).
D	RW	CONDBYPASS			Conditioning function bypass.
			NORMAL	0	the conditioning function is used (normal mode).
			BYPASS	1	the conditioning function is bypassed (to observe entropy source directly).
E	RW	INTENREP			Interrupt enable for Repetition Count Test failure.
F	RW	INTENPROP			Interrupt enable for Adaptive Proportion Test failure (1024-sample window).
G	RW	INTENFULL			Interrupt enable for FIFO full.
H	RW	SOFTRST			Software reset: This bit is not cleared automatically.
			NORMAL	0	Normal mode.
			CTEST	1	The continuous test, the conditioning function and the FIFO are reset.
I	RW	INTENPRE			Interrupt enable for AIS31 preliminary noise alarm.
J	RW	INTENALM			Interrupt enable for AIS31 noise alarm.
K	RW	FORCEACTIVEROS			Force oscillators to run when FIFO is full.
L	RW	HEALTHTESTBYPASS			Bypass NIST tests such that the results of the start-up and online test do not affect the FSM state.
M	RW	AIS31BYPASS			Bypass AIS31 tests such that the results of the start-up and online tests do not affect the FSM state.
N	RW	HEALTHTESTSEL			Select input to health test module:
			BEFORE	0	Before conditioning.
			AFTER	1	After conditioning.
O	RW	AIS31TESTSEL			Select input to the AIS31 test module:
			BEFORE	0	Before conditioning.
			AFTER	1	After conditioning.
P	RW	NB128BITBLOCKS			Number of 128 bit blocks used in AES-CBCMAC post-processing. This value cannot be zero.
Q	RW	FIFOWRITESTARTUP			Enable write of the samples in the FIFO during start-up.

7.8.1.7.25 RNGCONTROL.FIFOLEVEL

Address offset: 0x1004

FIFO level register.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW	FIFOLEVEL			Number of 32 bits words of random values available in the FIFO.
	RME				Any read to this register clears the FULLINT flag in the STATUS register, but does not affect this register content. Note that if the FIFO is still full, the status flag and interrupt will be set back up right away

7.8.1.7.26 RNGCONTROL.FIFOTHRESHOLD

Address offset: 0x1008

FIFO threshold register.