4.2.3.1 Architecture

The following figure shows the cache architecture.

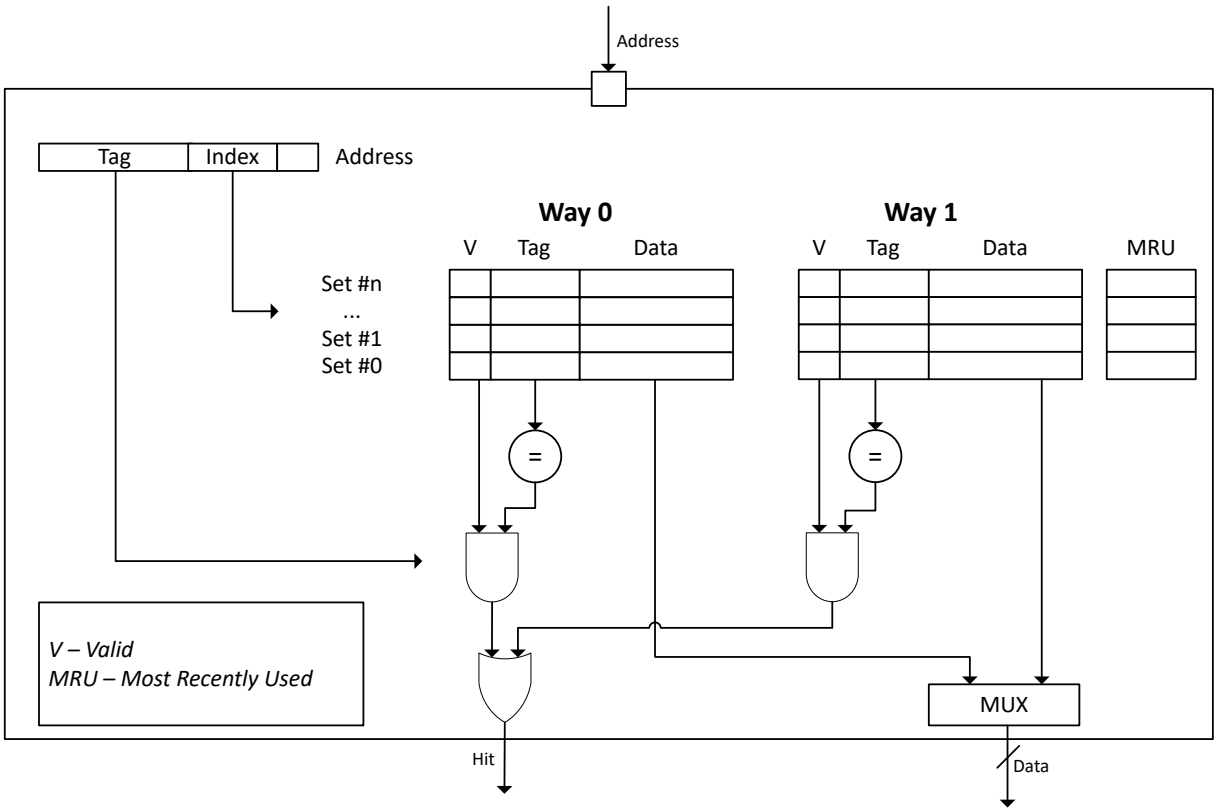

Figure 8: Cache overview

Bit	Name	Description
V	Valid	Indicates if a cache entry is valid. All V fields are cleared when enabling the cache, invalidating the cache, or when changing CACHE mode.
MRU	Most Recently Used	Updated on each fetch from the cache to indicate which Way was used most recently. Used to drive the cache replacement policy.

4.2.3.2 Profiling

The cache provides a scoreboard that tracks the hits and misses within the cache.

The results are available through a set of registers that can be used to indicate how well the cache is performing.

Profiling is enabled using PROFILING.ENABLE. All profiling counters can be cleared at any time using PROFILING.CLEAR. After being cleared, the counters will increment, according to the rules in the table below, at the next instruction- or data fetch.