- Compare match filter for generating events or interrupts

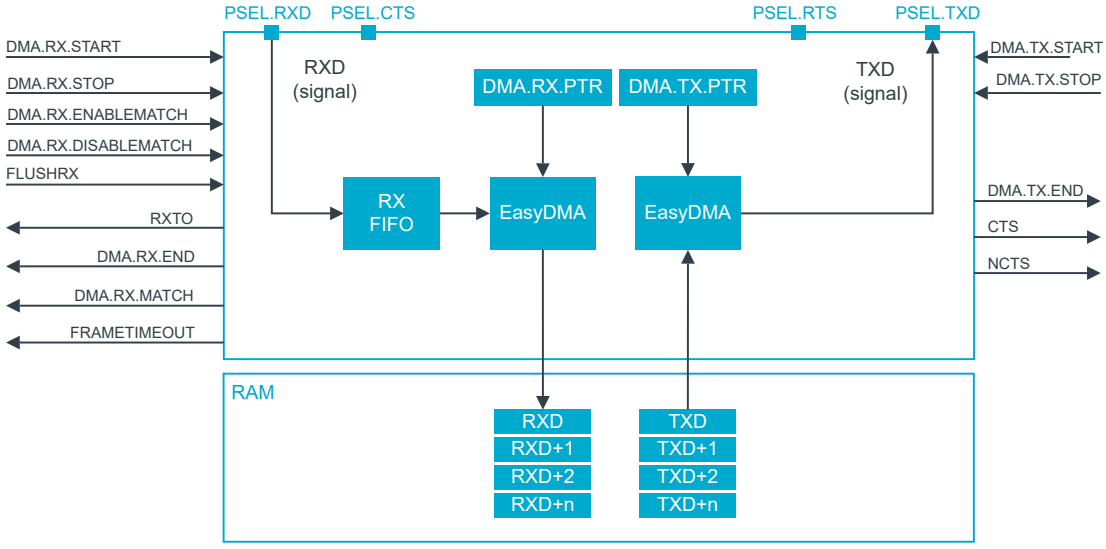

Figure 157: UARTE configuration

Note: The external crystal oscillator must be enabled to obtain sufficient clock accuracy for stable communication. See CLOCK — Clock control on page 70 for more information.

8.25.1 Baudrate

The UART baudrate defines the speed at which data is transmitted over the UART interface, measured in bits per second (bps).

The BAUDRATE register lists a set of precalculated values for the most common baudrates and 16 MHz PCLK. For the high speed instances (PCLK > 16 MHz), the baudrate is calculated as follows:

$$\mathrm{BAUDRATE} = 2^{12} \times \left\lfloor \frac{2^{20}}{\mathrm{round}\left(\frac{\mathrm{f\_PCLK}}{\mathrm{desired\_baudrate}}\right)} \right\rfloor$$

Figure 158: UARTE baudrate

- BAUDRATE is the value to be used in the UARTE BAUDRATE register.
- f_PCLK is the peripheral clock frequency for the UARTE instance, as defined in Instances on page 721.
- desired_baudrate is the desired baudrate in bits per second, such as 9600 or 115200.

8.25.2 EasyDMA

UARTE implements EasyDMA for reading and writing to and from RAM.

If the DMA.TX.PTR and the DMA.RX.PTR are not pointing to the RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See Memory on page 13 for more information about each memory region.

The DMA.RX.PTR, DMA.TX.PTR, DMA.RX.MAXCNT, and DMA.TX.MAXCNT registers are double-buffered. They can be updated and prepared for the next reception or transmission immediately after having received the DMA.RX.READY or DMA.TX.READY events.

The DMA.RX.END and DMA.TX.END events indicate that the EasyDMA is finished accessing the RX or TX buffer in RAM.

For detailed information regarding the use of EasyDMA, see EasyDMA on page 27.