Register	Offset	TZ	Description
INTENCLR	0x308		Disable interrupt
ERRORSRC	0x480		Error source
ENABLE	0x500		Enable UART
BAUDRATE	0x524		Baud rate. Accuracy depends on the HFCLK source selected.
CONFIG	0x56C		Configuration of parity, hardware flow control, framesize, and packet timeout.
ADDRESS	0x574		Set the address of the UARTE for RX when used in 9 bit data frame mode.
FRAMETIMEOUT	0x578		Set the number of UARTE bits to count before triggering packet timeout.
PSEL.TXD	0x604		Pin select for TXD signal
PSEL.CTS	0x608		Pin select for CTS signal
PSEL.RXD	0x60C		Pin select for RXD signal
PSEL.RTS	0x610		Pin select for RTS signal
DMA.RX.PTR	0x704		RAM buffer start address
DMA.RX.MAXCNT	0x708		Maximum number of bytes in channel buffer
DMA.RX.AMOUNT	0x70C		Number of bytes transferred in the last transaction, updated after the END event. Also updated after each MATCH event.
DMA.RX.TERMINATEONBUSERROR	0x71C		Terminate the transaction if a BUSERROR event is detected.
DMA.RX.BUSERRORADDRESS	0x720		Address of transaction that generated the last BUSERROR event.
DMA.RX.MATCH.CONFIG	0x724		Configure individual match events
DMA.RX.MATCH.CANDIDATE[n]	0x728		The data to look for - any match will trigger the MATCH[n] event, if enabled.
DMA.TX.PTR	0x73C		RAM buffer start address
DMA.TX.MAXCNT	0x740		Maximum number of bytes in channel buffer
DMA.TX.AMOUNT	0x744		Number of bytes transferred in the last transaction, updated after the END event. Also updated after each MATCH event.
DMA.TX.TERMINATEONBUSERROR	0x754		Terminate the transaction if a BUSERROR event is detected.
DMA.TX.BUSERRORADDRESS	0x758		Address of transaction that generated the last BUSERROR event.

8.25.13.1 TASKS_FLUSHRX

Address offset: 0x01C

Flush RX FIFO into RX buffer

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	TASKS_FLUSHRX			Flush RX FIFO into RX buffer
			Trigger	1	Trigger task

8.25.13.2 TASKS_DMA

Peripheral tasks.

8.25.13.2.1 TASKS_DMA.RX

Peripheral tasks.

8.25.13.2.1.1 TASKS_DMA.RX.START

Address offset: 0x028

Starts operation using easyDMA to load the values. See peripheral description for operation using easyDMA.