Linker flags:

```
--lto --remove
```

Symbol	Description	Min.	Typ.	Max.	Units
$CM_{RRAMCACHE128}$	CPU running CoreMark at 128 MHz from RRAM, cache enabled		503		CoreMark
$CM_{rram128/MHz}$	CoreMark per MHz, running from RRAM, cache enabled, HFXO128M		3.93		CoreMark/MHz
CM_{RAM128}	CPU running CoreMark at 128 MHz from RAM		464		CoreMark

11.4.2 CPU wakeup times

Symbol	Description	Min.	Typ.	Max.	Units
t_{R2ON}	Time from pin reset to CPU executes the first instruction		60		µs
t_{OFF2ON}	Time from wake-up from System OFF mode to CPU executes the first instruction		60		µs
$t_{IDLE2CPU}$	Wakeup time from CPU sleep (WFI,WFE) to CPU executes the next instruction		13		µs
$t_{IDLE2CPU,CONSTLAT}$	Wakeup time from CPU sleep (WFI,WFE) to CPU executes the next instruction in constant latency sub-mode		9		µs

11.5 GPIO Electrical specification

11.5.1 GPIO Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage	0.7 x VDD		VDD	V
V_{IL}	Input low voltage	VSS		0.3 x VDD	V
$V_{OH,SD}$	Output high voltage, standard drive, 0.5 mA, VDD ≥1.7	VDD - 0.4		VDD	V
$V_{OH,HDH}$	Output high voltage, high drive, 5 mA, VDD >= 2.7 V	VDD - 0.4		VDD	V
$V_{OH,HDL}$	Output high voltage, high drive, 3 mA, VDD >= 1.7 V	VDD - 0.4		VDD	V
$V_{OL,SD}$	Output low voltage, standard drive, 0.5 mA, VDD ≥1.7	VSS		VSS + 0.4	V
$I_{OL,SD}$	Current at VSS+0.4 V, output set low, standard drive, VDD ≥1.7	1	3	4	mA
$I_{OL,HDL}$	Current at VSS+0.4 V, output set low, high drive, VDD >= 1.7 V	3			mA
$I_{OL,ED}$	Current at VSS+0.4 V, output set low, extra drive, VDD >= 1.7 V	16			mA
$I_{OH,SD}$	Current at VDD-0.4 V, output set high, standard drive, VDD ≥1.7	1	3	4	mA
$I_{OH,HDL}$	Current at VDD-0.4 V, output set high, high drive, VDD >= 1.7 V	4			mA
$I_{OH,ED}$	Current at VDD-0.4 V, output set high, extra drive, VDD >= 1.7 V	14			mA
$I_{GPIO,TOTAL}$	Recommended maximum sustained current drawn by all GPIOs			15	mA
$t_{HRF,12pF}$	Rise/Fall time, high drive mode, 20-80%, 12 pF load[1]		4		ns
$t_{ERF,12pF}$	Rise/Fall time, extra drive mode, 20-80%, 12 pF load[1]		0.9		ns
R_{PU}	Pull-up resistance	12	14	16	kΩ
R_{PD}	Pull-down resistance	12	14	18	kΩ
$t_{OE,ED}$	Output enable delay in extra drive mode			855	ns
C_{PAD}	Pad capacitance		1		pF
C_{PAD_NFC}	Pad capacitance on NFC pads		5		pF