All GRTC registers must be restored at wakeup from system OFF before the next scheduled COMPARE[n] event is generated. The TIMEOUT register must be configured to a value higher than WAKETIME (TIMEOUT > WAKETIME + guard_time). This makes sure that GRTC is not entering sleep again if the next event is nearer than TIMEOUT LFCLK cycles. The minimum guard time is 1 LFCLK cycle.

Recommendation on reading SYSCOUNTER

The following steps are recommended while reading SYSCOUNTER:

1. Set the corresponding SYSCOUNTER[m].ACTIVE to Active
2. Wait until the corresponding status SYSCOUNTER[m].SYSCOUNTERH.BUSY is cleared
3. Read the corresponding SYSCOUNTER[m].SYSCOUNTERL/H values
4. Clear the SYSCOUNTER[m].ACTIVE set above

Entering System OFF mode

The following steps are recommended before entering System OFF mode:

1. Set the SYSCOUNTER in active state, either
   - Set MODE.AUTOEN
   - Set corresponding SYSCOUNTER[m].ACTIVE to Active
2. If GRTC is wakeup source, then set the corresponding CC[n] value to expected wakeup time
3. Set WAKETIME for the boot latency
4. Set the SYSCOUNTER in sleep state, by clearing the configuration set at step 1 above
5. Wait for either of EVENTS_RTCOMPARESYNC or any EVENTS_COMPARE[n]
   - If any EVENTS_COMPARE[n] triggered,
     a. Allow CPUs to wakeup on interrupts
     b. Do not enter System OFF mode
   - Else,
     a. Enter System OFF by using the SYSTEMOFF register

8.10.3 Pulse Width Modulation (PWM)

The GRTC peripheral has a built-in PWM that can drive one output pin as an 8-bit non-inverted pulse-width modulated output.

The PWM is based on the internal low frequency timer of the GRTC and the PWM has a period of 256 LFCLK clock cycles, resulting frequency is 128Hz.

The PWM can be started by the TASKS_PWMSTART task and can be stopped by the TASKS_PWMSTOP task. The PWM starts/stops on next time when the lower 8 bits of internal low frequency timer becomes to zero. It takes up to 256 LFCLK clock cycles to take these tasks to go into effect.

The STATUS.PWM.READY indicates busy while handling the tasks TASKS_PWMSTART and TASKS_PWMSTOP. These PWM tasks must be triggered only when the STATUS.PWM.READY status indicates ready. The EVENTS_PWMREADY event is generated when the STATUS.PWM.READY status changes from busy to ready.

The PWM compare value is configured using PWMCONFIG and the copied to the internal PWM compare register when the lower 8 bits of internal low frequency timer is 0.

The PWM output goes high when the the lower 8 bits of internal low frequency timer goes to zero and the PWM output goes low when the lower 8 bits of internal low frequency timer matches the PWM compare value. The EVENTS_PWMPERIODEND event is generated on the rising edge of the PWM output.