Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
E	RW W1C	FPUIXC			Write '1' to disable interrupt for event FPUIXC
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW W1C	FPUIDC			Write '1' to disable interrupt for event FPUIDC
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

4.1.2.1.10 LOCK

Address offset: 0x500

Register to lock the certain parts of the CPU from being modified.

Each bit can only be written once and can only be changed from 0 to 1.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	LOCKVTORAIRCRS			Locks both the Vector table Offset Register (VTOR) and Application Interrupt and Reset Control Register (AIRCR) for secure mode.
			NotLocked	0	Both VTOR and AIRCR can be changed.
			Locked	1	Prevents changes to both VTOR and AIRCR.
B	RW	LOCKVTORNS			Locks the Vector table Offset Register (VTOR) for non-secure mode.
			NotLocked	0	VTOR can be changed.
			Locked	1	Prevents changes to VTOR.
C	RW	LOCKMPUS			Locks the Memory Protection Unit (MPU) for secure mode.
			NotLocked	0	MPU registers can be changed.
			Locked	1	Prevents changes to MPU registers.
D	RW	LOCKMPUNS			Locks the Memory Protection Unit (MPU) for non secure mode.
			NotLocked	0	MPU registers can be changed.
			Locked	1	Prevents changes to MPU registers.
E	RW	LOCKSAU			Locks the Security Attribution Unit (SAU)
			NotLocked	0	SAU registers can be changed.
			Locked	1	Prevents changes to SAU registers.

4.1.2.1.11 CPUID

Address offset: 0x504

The identifier for the CPU in this subsystem.