8.26.1.6 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID										G	F	E	D	C	B	A																
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
	RW W1S	TRIGGERED[i] (i=16..22)			Write '1' to enable interrupt for event TRIGGERED[i] If RTPs are not enabled: writes to registers 15..0 are ignored, other read/write accesses operate normally If RTPs are enabled: reads or writes to these registers will be stalled if there is a simultaneous VPR CSR write access to any CSR register.
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

8.26.1.7 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID										G	F	E	D	C	B	A																
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
	RW W1C	TRIGGERED[i] (i=16..22)			Write '1' to disable interrupt for event TRIGGERED[i] If RTPs are not enabled: writes to registers 15..0 are ignored, other read/write accesses operate normally If RTPs are enabled: reads or writes to these registers will be stalled if there is a simultaneous VPR CSR write access to any CSR register.
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

8.26.1.8 INTPEND

Address offset: 0x30C

Pending interrupts