9.5 Trace

The device supports ETM and ITM trace.

Trace data from the ETM and ITM is sent to an external debugger through a 4-bit wide parallel trace port (TPIU), as illustrated in Access port unlocking.

In addition to parallel trace mode, the TPIU supports serial trace mode through the serial wire output (SWO) trace protocol. Parallel and serial trace modes cannot be used at the same time. ETM trace is only supported in parallel trace mode. ITM trace is supported in both parallel and serial trace mode. See the debug documentation of the IDE for more information.

TPIU trace pins are multiplexed with GPIO pins. The **SWO** and **TRACEDATA[0]** pins can use the same GPIO. The **SWO** pin can also use a separate GPIO on P2. See Pin assignments on page 859 for more information.

Trace speed is configured in the register TRACEPORTSPEED. Trace pin speed is determined by the GPIO drive setting of the multiplexed pins. See GPIO — General purpose input/output on page 274 for information on drive settings.

9.5.1 Enabling the trace port

A specific sequence of operations must be performed to enable the trace port.

1. Enable trace and debug using the following code.

```
NRF_TAD_S->ENABLE = TAD_ENABLE_ENABLE_Msk;
```

2. Set drive strength to the highest possible value to ensure fast operation. Do this for all trace pins that will be used.

```
#define TRACE_PIN_CLEAR     (~(GPIO_PIN_CNF_CTRLSEL_Msk | GPIO_PIN_CNF_DRIVE0_Msk \
                            | GPIO_PIN_CNF_DRIVE1_Msk))

#define TRACE_PIN_CONFIG    ((GPIO_PIN_CNF_DRIVE0_E0 << GPIO_PIN_CNF_DRIVE0_Pos) \
                            | (GPIO_PIN_CNF_DRIVE1_E1 << GPIO_PIN_CNF_DRIVE1_Pos))

// Clear the bitfields before configuring to make sure the correct value is written
NRF_P2_S->PIN_CNF[TRACE_TRACECLK_PIN] &= TRACE_PIN_CLEAR;
NRF_P2_S->PIN_CNF[TRACE_TRACEDATA0_PIN] &= TRACE_PIN_CLEAR;
NRF_P2_S->PIN_CNF[TRACE_TRACEDATA1_PIN] &= TRACE_PIN_CLEAR;
NRF_P2_S->PIN_CNF[TRACE_TRACEDATA2_PIN] &= TRACE_PIN_CLEAR;
NRF_P2_S->PIN_CNF[TRACE_TRACEDATA3_PIN] &= TRACE_PIN_CLEAR;

NRF_P2_S->PIN_CNF[TRACE_TRACECLK_PIN] |= TRACE_PIN_CONFIG;
NRF_P2_S->PIN_CNF[TRACE_TRACEDATA0_PIN] |= TRACE_PIN_CONFIG;
NRF_P2_S->PIN_CNF[TRACE_TRACEDATA1_PIN] |= TRACE_PIN_CONFIG;
NRF_P2_S->PIN_CNF[TRACE_TRACEDATA2_PIN] |= TRACE_PIN_CONFIG;
NRF_P2_S->PIN_CNF[TRACE_TRACEDATA3_PIN] |= TRACE_PIN_CONFIG;
```

3. Trace port speed is configured as a prescaled version of the CPU frequency and must be at least half the CPU frequency to avoid dropping trace packets.

```
NRF_TAD_S->TRACEPORTSPEED = TAD_TRACEPORTSPEED_TRACEPORTSPEED_DIV2;
```

Note: Do not run the trace port at less than half the CPU frequency, as this risks dropping trace packets.