8.11.6 Width, alignment and format

The register CONFIG.SWIDTH on page 344 defines the sample width of the data read and written to memory, as well as the number of SCK clock cycles per half-frame. Figure Aligned format, with CONFIG.SWIDTH configured to 16 bit samples in a 16 bit half-frame on page 327 illustrates a configuration with identical sample and half-frame widths. The number of SCK pulses matches the number of sample bits. Aligned format, with CONFIG.SWIDTH configured to 16-bit samples in a 24-bit half-frame on page 327 illustrates a configuration with greater half-frame width than sample width. The number of SCK pulses are greater than the number of sample bits, with the sample being left-aligned in the half-frame.

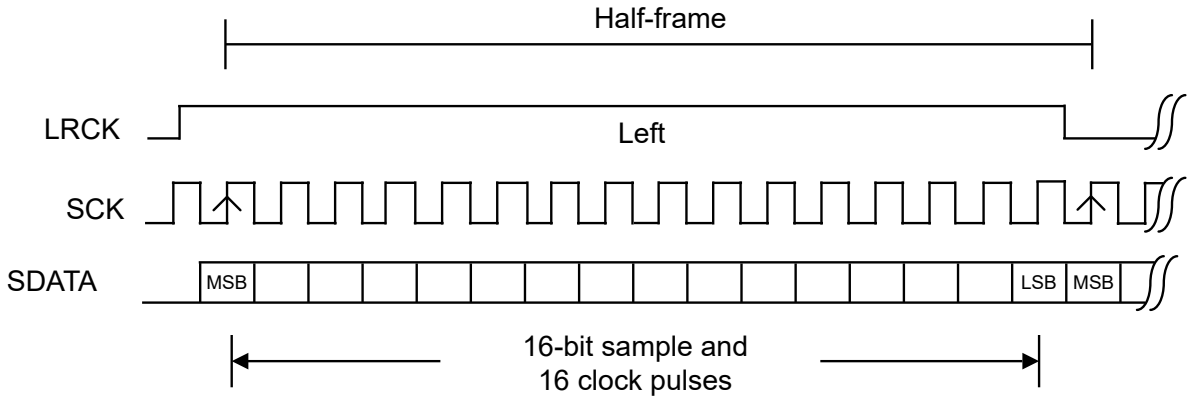

Figure 70: Aligned format, with CONFIG.SWIDTH configured to 16 bit samples in a 16 bit half-frame

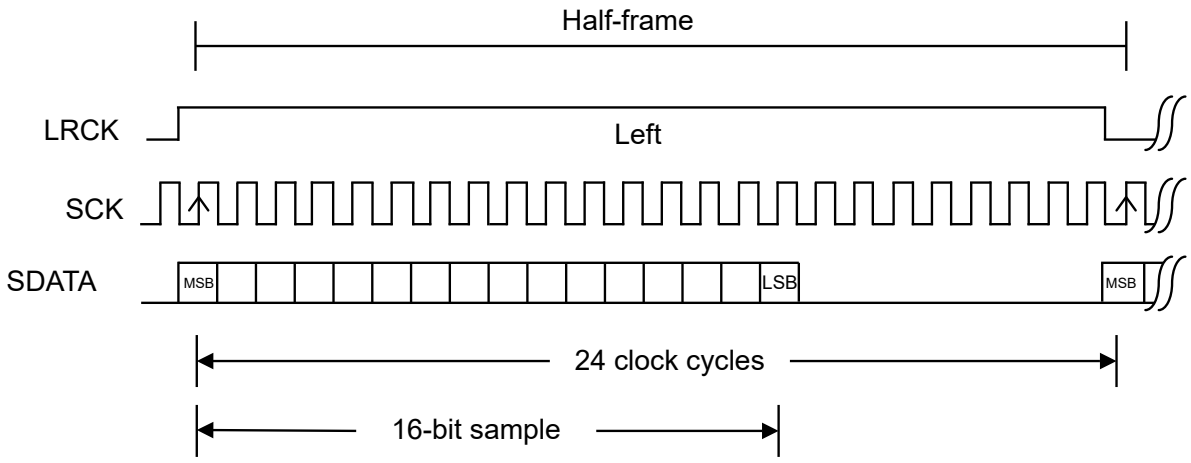

Figure 71: Aligned format, with CONFIG.SWIDTH configured to 16-bit samples in a 24-bit half-frame

The register CONFIG.FORMAT on page 344 is used to choose whether a word shall be aligned on the LRCK edge, or be delayed one bit period after this edge:

- When using Aligned format, the first bit in a half-frame gets sampled on the first rising edge of SCK following a LRCK edge, as illustrated in Aligned format. Identical sample width and half-frame width. Left sample on high level of LRCK on page 328. The left sample is transferred during the high half period of LRCK.
- When using I^2S format, the first bit in a half-frame (containing one left or right sample) gets sampled on the second rising edge of the SCK after a LRCK edge, as illustrated in I^2S format. Identical sample width and half-frame width. Left sample on low level of LRCK on page 328. The left sample is transferred during the low half period of LRCK.