| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| ID | | | | N M L K J I H G F E D C B B B B A A A A A A A A A A |
| **Reset 0x01F72200** | | | | **0 0 0 0 0 0 0 1 1 1 1 1 0 1 1 1 0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0** |
| ID | R/W | Field | Value ID | Value | Description |
| F | R | P256 | | | Support ECC P256 acceleration. |
| G | R | P384 | | | Support ECC P384 acceleration. |
| H | R | P521 | | | Support ECC P521 acceleration. |
| I | R | P192 | | | Support ECC P192 acceleration. |
| J | R | X25519 | | | Support Curve25519/Ed25519 acceleration. |
| K | R | AHBMASTER | | | Memory access |
| | | | SLAVE | 0 | Memory access through AHB Slave and internally in the PKE. |
| | | | MASTER | 1 | Memory access through AHB Master, outside the PKE. |
| L | R | DISABLESMX | | | State of DisableSMx input (high when SM2/SM9 operations are disabled). |
| M | R | DISABLECLRMEM | | | State of DisableClrMem input (high when automatic clear of the RAM after reset is disabled). |
| N | R | DISABLECM | | | State of DisableCM input (high when counter-measures are disabled). |

## 7.8.1.7.49 PK.OPSIZE

Address offset: 0x201C

Operand size register.

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| ID | | | | A A A A A A A A A A A A A A A A |
| **Reset 0x00001000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0** |
| ID | R/W | Field | Value ID | Value | Description |
| A | RW | OPSIZE | | | Operand size (number of bytes): This register is used when the memory is accessed via AHB Master |
| | | | OPSIZE256 | 0x0100 | 256 bytes. |
| | | | OPSIZE521 | 0x0209 | 521 bytes. |
| | | | OPSIZE2048 | 0x0800 | 2048 bytes. |
| | | | OPSIZE3072 | 0x0C00 | 3072 bytes. |
| | | | OPSIZE4096 | 0x1000 | 4096 bytes. |

## 7.8.1.7.50 PK.RAMERRORINJECT

Address offset: 0x2040

RAM error injection register.

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| ID | | | | B B B B B B B B B B A A A A A A A A A A |
| **Reset 0x03FF03FF** | | | | **0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1** |
| ID | R/W | Field | Value ID | Value | Description |
| A | RW | BITERROR1 | | | Bit position of first error |
| B | RW | BITERROR2 | | | Bit position of second error |

## 7.8.1.7.51 PK.RAMERRORSTATUS

Address offset: 0x2044

RAM error status register.