## 8.23.10.18 PUBLISH_LASTRX

Address offset: 0x1B4

Publish configuration for event LASTRX

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| ID | | | | B A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| ID | R/W | Field | Value ID | Value | Description |
| A | RW | CHIDX | | [0..255] | DPPI channel that event LASTRX will publish to |
| B | RW | EN | | | |
| | | | Disabled | 0 | Disable publishing |
| | | | Enabled | 1 | Enable publishing |

## 8.23.10.19 PUBLISH_LASTTX

Address offset: 0x1B8

Publish configuration for event LASTTX

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| ID | | | | B A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| ID | R/W | Field | Value ID | Value | Description |
| A | RW | CHIDX | | [0..255] | DPPI channel that event LASTTX will publish to |
| B | RW | EN | | | |
| | | | Disabled | 0 | Disable publishing |
| | | | Enabled | 1 | Enable publishing |

## 8.23.10.20 PUBLISH_DMA

Publish configuration for events

### 8.23.10.20.1 PUBLISH_DMA.RX

Publish configuration for events

#### *8.23.10.20.1.1 PUBLISH_DMA.RX.END*

Address offset: 0x1CC

Publish configuration for event END

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| ID | | | | B A A A A A A A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| ID | R/W | Field | Value ID | Value | Description |
| A | RW | CHIDX | | [0..255] | DPPI channel that event END will publish to |
| B | RW | EN | | | |
| | | | Disabled | 0 | Disable publishing |
| | | | Enabled | 1 | Enable publishing |

#### *8.23.10.20.1.2 PUBLISH_DMA.RX.READY*

Address offset: 0x1D0

Publish configuration for event READY