4.2.6.7.18 ACCESSERRORADDR

Address offset: 0x408

Address of the first access error

The event ACCESSERROR is generated on access error. When this event is cleared, this register is updated on the next access error

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00FFFFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A	R	ADDRESS																																	

Access error address

The most significant 8 bits are set to zero always

4.2.6.7.19 BUFSTATUS.WRITEBUFEMPTY

Address offset: 0x418

Internal write-buffer is empty

The internal write-buffer has been committed to RRAM and is now empty

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	EMPTY																																	
			NotEmpty	0																															
			Empty	1																															

The internal write-buffer has data that needs committing

The internal write-buffer is empty and has no content that needs to be committed

4.2.6.7.20 ECC.ERRORADDR

Address offset: 0x420

Address of the first ECC error that could not be corrected

The event ECCERROR is generated on ECC error. When this event is cleared, this register is updated on the next ECC error

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00FFFFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A	R	ADDRESS																																	

ECC error address

The most significant 8 bits are set to zero always

4.2.6.7.21 CONFIG

Address offset: 0x500

Configuration register