Register overview

Register	Offset	TZ	Description
TASKS_FLUSHRX	0x01C		Flush RX FIFO into RX buffer
TASKS_DMA.RX.START	0x028		Starts operation using easyDMA to load the values. See peripheral description for operation using easyDMA.
TASKS_DMA.RX.STOP	0x02C		Stops operation using easyDMA. This does not trigger an END event.
TASKS_DMA.RX.ENABLEMATCH[n]	0x030		Enables the MATCH[n] event by setting the ENABLE[n] bit in the CONFIG register.
TASKS_DMA.RX.DISABLEMATCH[n]	0x040		Disables the MATCH[n] event by clearing the ENABLE[n] bit in the CONFIG register.
TASKS_DMA.TX.START	0x050		Starts operation using easyDMA to load the values. See peripheral description for operation using easyDMA.
TASKS_DMA.TX.STOP	0x054		Stops operation using easyDMA. This does not trigger an END event.
SUBSCRIBE_FLUSHRX	0x09C		Subscribe configuration for task FLUSHRX
SUBSCRIBE_DMA.RX.START	0x0A8		Subscribe configuration for task START
SUBSCRIBE_DMA.RX.STOP	0x0AC		Subscribe configuration for task STOP
SUBSCRIBE_DMA.RX.ENABLEMATCH[n]	0x0B0		Subscribe configuration for task ENABLEMATCH[n]
SUBSCRIBE_DMA.RX.DISABLEMATCH[n]	0x0C0		Subscribe configuration for task DISABLEMATCH[n]
SUBSCRIBE_DMA.TX.START	0x0D0		Subscribe configuration for task START
SUBSCRIBE_DMA.TX.STOP	0x0D4		Subscribe configuration for task STOP
EVENTS_CTS	0x100		CTS is activated (set low). Clear To Send.
EVENTS_NCTS	0x104		CTS is deactivated (set high). Not Clear To Send.
EVENTS_TXDRDY	0x10C		Data sent from TXD
EVENTS_RXDRDY	0x110		Data received in RXD (but potentially not yet transferred to Data RAM)
EVENTS_ERROR	0x114		Error detected
EVENTS_RXTO	0x124		Receiver timeout
EVENTS_TXSTOPPED	0x130		Transmitter stopped
EVENTS_DMA.RX.END	0x14C		Generated after EasyDMA has completed its operation.
EVENTS_DMA.RX.READY	0x150		Generated when EasyDMA has buffered the .PTR and .MAXCNT registers for the channel, allowing them to be written to prepare for the next sequence.
EVENTS_DMA.RX.BUSERROR	0x154		An error occured during the bus transfer.
EVENTS_DMA.RX.MATCH[n]	0x158		Pattern match is detected on the DMA data bus.
EVENTS_DMA.TX.END	0x168		Generated after EasyDMA has completed its operation.
EVENTS_DMA.TX.READY	0x16C		Generated when EasyDMA has buffered the .PTR and .MAXCNT registers for the channel, allowing them to be written to prepare for the next sequence.
EVENTS_DMA.TX.BUSERROR	0x170		An error occured during the bus transfer.
EVENTS_FRAMETIMEOUT	0x174		Timed out due to bus being idle while receiving data.
PUBLISH_CTS	0x180		Publish configuration for event CTS
PUBLISH_NCTS	0x184		Publish configuration for event NCTS
PUBLISH_TXDRDY	0x18C		Publish configuration for event TXDRDY
PUBLISH_RXDRDY	0x190		Publish configuration for event RXDRDY
PUBLISH_ERROR	0x194		Publish configuration for event ERROR
PUBLISH_RXTO	0x1A4		Publish configuration for event RXTO
PUBLISH_TXSTOPPED	0x1B0		Publish configuration for event TXSTOPPED
PUBLISH_DMA.RX.END	0x1CC		Publish configuration for event END
PUBLISH_DMA.RX.READY	0x1D0		Publish configuration for event READY
PUBLISH_DMA.RX.BUSERROR	0x1D4		Publish configuration for event BUSERROR
PUBLISH_DMA.RX.MATCH[n]	0x1D8		Publish configuration for event MATCH[n]
PUBLISH_DMA.TX.END	0x1E8		Publish configuration for event END
PUBLISH_DMA.TX.READY	0x1EC		Publish configuration for event READY
PUBLISH_DMA.TX.BUSERROR	0x1F0		Publish configuration for event BUSERROR
PUBLISH_FRAMETIMEOUT	0x1F4		Publish configuration for event FRAMETIMEOUT
SHORTS	0x200		Shortcuts between local events and tasks
INTEN	0x300		Enable or disable interrupt
INTENSET	0x304		Enable interrupt

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