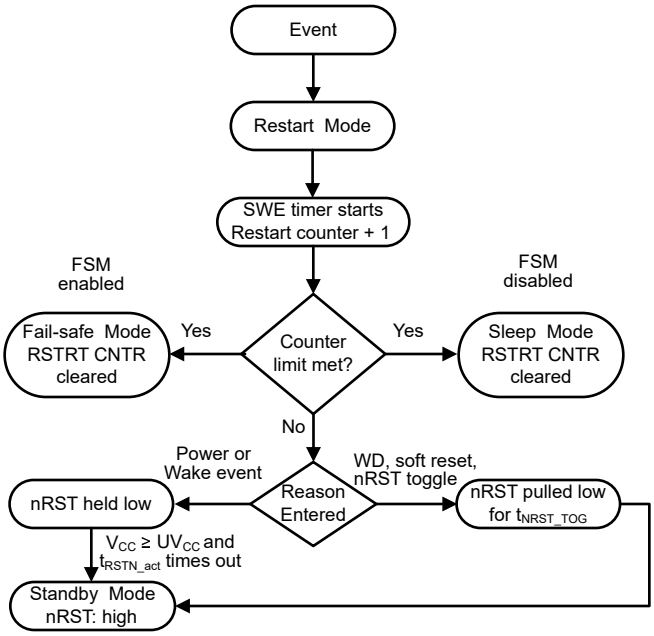

Note:
1. Wake event means entered from sleep or fail-safe modes
2. If SWE timer times out device will enter sleep or fail-safe mode
3. nRST toggle reason is an external toggle of nRST pin to reset device
4. A soft reset or external nRST toggle will reset t_{NRST_TOG} to default value, typically 2 ms

Figure 8-41. nRST Behavior in Restart Mode

8.4.7 Fail-safe Mode

When the TLIN1431x-Q1 has certain fault conditions, the device enters a fail-safe mode (FSM). This feature can be disabled in SPI control mode, but is always on in pin control mode. This mode turns on LIMP and brings all other function into lower power mode states. Fault conditions are over-voltage on V_{CC}, thermal shutdown, V_{CC} under-voltage events and reaching restart counter limit in SPI control mode. When entering FSM, a fail-safe mode counter is incremented. The counter limit is set at register 8'h18[7:4], FSM_CNTR_SET and should be set to greater than 1. To avoid unwanted actions the counter should be cleared by writing 0h to 8'h18[3:0]. If the limit is reached a programmed action will be executed, register 8'h17[7:4], FSM_CNTR_ACT. Once the fault conditions are cleared, the device can be put back into restart mode from a wake event. If a fault condition is still in effect after the wake event the device enters sleep. If no wake event takes place, the device enters sleep mode after the programmed SWE timer, t_{INACT_FS}, times out.

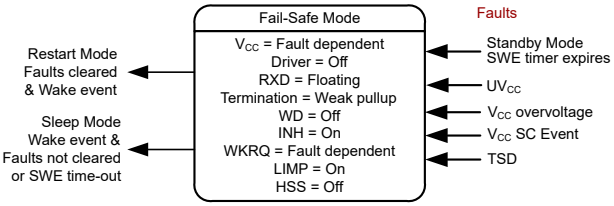

Figure 8-42. Fail-safe Mode Pin Control

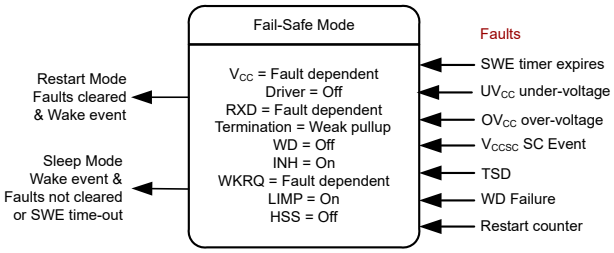

Figure 8-43. Fail-safe Mode SPI Control