Table 8-48. INT_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	RSVD	R	00b	Reserved

8.6.39 INT_EN_4 Register (Address = 5Eh) [reset = CCh]

INT_EN_4 is shown in Figure 8-93 and described in Table 8-49.

Return to Summary Table.

Interrupt mask for INT_4.

Figure 8-93. INT_EN_4 Register

7	6	5	4	3	2	1	0
LIN_WUP_EN	LIN_DTO_EN	RSVD		HSSOC_EN	HSSOL_EN	RSVD	
R/W-1b	R/W-1b	R-00b		R/W-1b	R/W-1b	R-00b	

Table 8-49. INT_EN_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LIN_WUP_EN	R/W	1b	LIN bus wake interrupt enable
6	LIN_DTO_EN	R/W	1b	LIN dominant state timeout interrupt enable
5-4	RSVD	R	00b	Reserved
3	HSSOC_EN	R/W	1b	High side switch over current interrupt enable
2	HSSOL_EN	R/W	1b	High side switch open load interrupt enable
1-0	RSVD	R	00b	Reserved

8.6.40 Reserved Registers

All other registers not provided up to 'h7F are reserved.