Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	EN			Controls CPU running state after a core reset.
			Stopped	0	CPU stopped. If this is the CPU state after a core reset, setting this bit will change the CPU state to CPU running.
			Running	1	CPU running. If this is the CPU state after a core reset, clearing this bit will change the CPU state to CPU stopped after a core reset.

8.26.1.37 INITPC

Address offset: 0x808

Initial value of the PC at CPU start.

Note: This address must be 64 bit aligned

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	INITPC			Initial value of the PC at CPU start. This value should be set before setting CPURUN.EN. After setting CPURUN.EN, this register can be reconfigured to prepare the CPU to start from a new initial PC upon receiving a reset request

8.26.2 Registers

Instances

Instance	Domain	Base address	TrustZone			Split access	Description
			Map	Att	DMA		
VPRCLIC	FLPR	0xF0000000	HF	NS	NA	No	VPR CLIC registers

Configuration

Instance	Domain	Configuration
VPRCLIC	FLPR	Supported interrupts (IRQNUM): 0..270 VEVIF tasks: 0..31 Mask of supported VEVIF tasks: 0xFFFFFFFF VPR counter (CNT0) interrupt handler number (COUNTER_IRQ_NUM): 31 CLIC configuration for VPR 1.2 enabled

Register overview

Register	Offset	TZ	Description
CLIC.CLICCFG	0x0000		CLIC configuration.
CLIC.CLICINFO	0x0004		CLIC information.
CLIC.CLICINT[n]	0x1000		Interrupt control register for IRQ number [n].