11.6 I2S Electrical specification

11.6.1 I2S timing specification

Symbol	Description	Min.	Typ.	Max.	Units
t_{SCK_LRCK}	SCLK falling to LRCK edge	-5	0	+5	ns
f_{MCK}	MCK frequency			8000	kHz
f_{LRCK}	LRCK frequency			100	kHz
f_{SCK}	SCK frequency			8000	kHz
DC_{CK}	Clock duty cycle (MCK, LRCK, SCK)	45		55	%

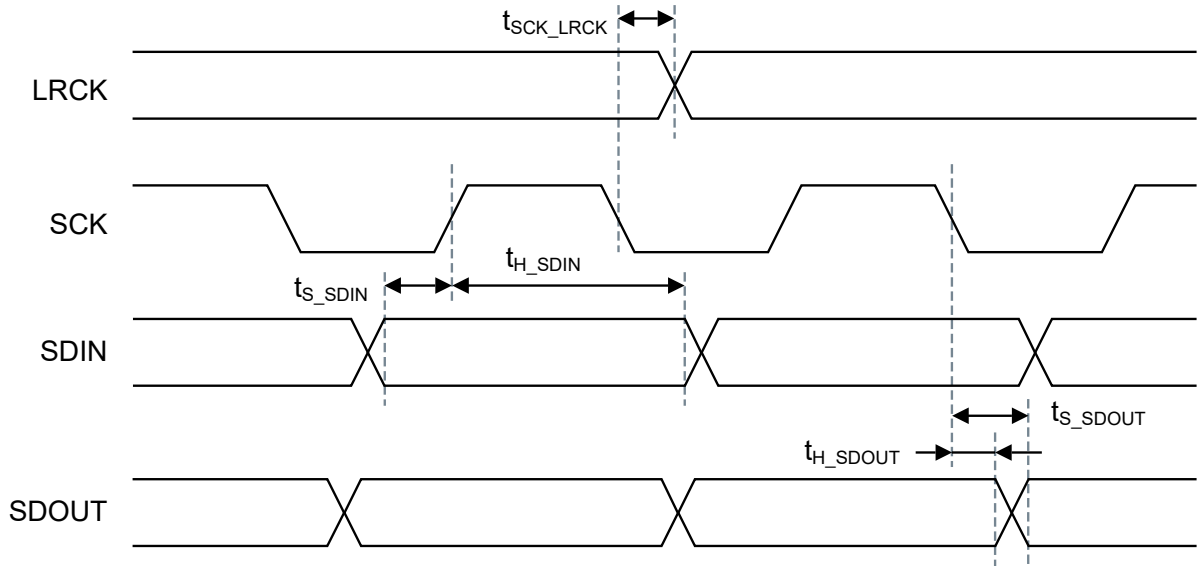

Figure 187: I2S timing diagram

11.6.2 Timing specifications for Slave mode

Symbol	Description	Min.	Typ.	Max.	Units
t_{S_SDIN}	SDIN setup time before SCK rising	14			ns
t_{H_SDIN}	SDIN hold time after SCK rising	6			ns
t_{S_SDOUT}	SCK falling edge to SDOUT valid			42	ns
t_{H_SDOUT}	SDOUT hold time after SCK falling	5			ns

11.6.3 Timing specifications for Master mode

Symbol	Description	Min.	Typ.	Max.	Units
t_{S_SDIN}	SDIN setup time before SCK rising	12			ns
t_{H_SDIN}	SDIN hold time after SCK rising	1			ns
t_{S_SDOUT}	SCK falling edge to SDOUT valid			65	ns
t_{H_SDOUT}	SDOUT hold time after SCK falling	4			ns