8.26.1.24 DEBUGIF.HALTSUM2

Address offset: 0x4D0

Halt Summary 2

Each bit in this read-only register indicates whether any of a group of harts is halted or not. Unavailable/ nonexistent harts are not considered to be halted. This register might not be present if fewer than 1025 harts are connected to this DM. The LSB reflects the halt status of harts hartsel[19:15] 0x0 through hartsel[19:15] 0x3ff. The MSB reflects the halt status of harts hartsel[19:15] 0x7c00 through hartsel[19:15] 0x7fff

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	R	HALTSUM2			Halt Summary 2

8.26.1.25 DEBUGIF.HALTSUM3

Address offset: 0x4D4

Halt Summary 3

Each bit in this read-only register indicates whether any of a group of harts is halted or not. Unavailable/ nonexistent harts are not considered to be halted. This register might not be present if fewer than 32769 harts are connected to this DM. The LSB reflects the halt status of harts 0x0 through 0x7fff. The MSB reflects the halt status of harts 0xf8000 through 0xfffff

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	R	HALTSUM3			Halt Summary 3

8.26.1.26 DEBUGIF.SBADDRESS3

Address offset: 0x4DC

System Bus Addres 127:96

If sbasize is less than 97, then this register is not present. When the system bus master is busy, writes to this register will set sbbusyerror and don't do anything else.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	R	ADDRESS			Accesses bits 127:96 of the physical address in sbaddress (if the system address bus is that wide).

8.26.1.27 DEBUGIF.SBCS

Address offset: 0x4E0

System Bus Access Control and Status