8.26.3.32 MHARTID

Address offset: 0xF14

Machine Hart ID

Contains the integer ID of the hardware thread running the code. Hart ID is unique for every VPR instance and this register's reset value is set to it

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x0000000E				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	HARTNUM																																	
																																			Machine Hart ID value

8.26.3.33 NORDIC.VPRNORDICCTRL

Address offset: 0x7C0

Nordic Core Control

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E									D	C			B			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	ENABLERTPERIPH																																	
																																			Control bit to enable Real-Time Peripherals When this bit is cleared, it will override the APB read value of the INTEN register to 0.
			Disabled	0																															
			Enabled	1																															
B	RW	ENABLEREMAP																																	Enable remap feature
			Disabled	0																															
			Enabled	1																															
C	RW	CNTIRQENABLE																																	Enables the generation of IRQ number COUNTER_IRQ_NUM
			Disabled	0x0																															
			Enabled	0x1																															
D	RW	VPRBUSPRI																																	Arbitration priority on bus Setting high priority will give VPR maximum priority and can cause starvation for other bus masters trying to access the same memory. It should only be used in limited sections of code and care must be taken to avoid continuous memory accesses to ensure other bus masters can perform interleaved accesses.
			LowPriority	0x0																															Low priority for VPR RAM transactions on bus
			HighPriority	0x1																															High priority for VPR RAM transactions on bus
E	W	NORDICKEY																																	Used in order to protect the write to this register
			Enabled	0x507D																															Write enabled

8.26.3.34 NORDIC.VPRNORDICSLEEPCTRL

Address offset: 0x7C1

Nordic Sleep Control