

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																												
ID				B																								A				A	A	A	A	A	A	A																									
Reset 0x00000000				0																																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	R/W	Field	Value ID	Value		Description																																																									
A	RW	CHIDX		[0..255]		DPPI channel that event <b>END</b> will publish to																																																									
B	RW	EN																																																													
			Disabled	0	Disable publishing																																																										
			Enabled	1	Enable publishing																																																										

#### 8.19.8.18.1.2 PUBLISH\_DMA.RX.READY

Address offset: 0x1D0

Publish configuration for event **READY**

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				B A A A A A A A A A																															
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value	Description																														
A	RW	CHIDX		[0..255]	DPPI channel that event <b>READY</b> will publish to																														
B	RW	EN																																	
			Disabled	0	Disable publishing																														
			Enabled	1	Enable publishing																														

#### 8.19.8.18.1.3 PUBLISH\_DMA.RX.BUSERROR

Address offset: 0x1D4

Publish configuration for event **BUSERROR**

When this event is generated, the address which caused the error can be read from the **BUSERRORADDRESS** register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																											
ID				B																								A				A	A	A	A	A	A	A																								
Reset 0x00000000				0																																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	R/W	Field	Value ID	Value		Description																																																								
A	RW	CHIDX		[0..255]		DPPI channel that event <b>BUSERROR</b> will publish to																																																								
B	RW	EN																																																												
			Disabled	0	Disable publishing																																																									
			Enabled	1	Enable publishing																																																									

#### 8.19.8.18.1.4 PUBLISH\_DMA.RX.MATCH[n] (n=0..3)

Address offset: 0x1D8 + (n × 0x4)

Publish configuration for event **MATCH[n]**

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																												
ID				B																								A				A	A	A	A	A	A	A																									
Reset 0x00000000				0																																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	R/W	Field	Value ID	Value				Description																																																							
A	RW	CHIDX		[0..255]				DPPI channel that event <b>MATCH[n]</b> will publish to																																																							
B	RW	EN																																																													
			Disabled	0				Disable publishing																																																							
			Enabled	1				Enable publishing																																																							