Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW W1C	TAMPER			Write '1' to disable interrupt for event TAMPER
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
B	RW W1C	WRITEERROR			Write '1' to disable interrupt for event WRITEERROR
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

7.8.6.6.6 INTPEND

Address offset: 0x30C

Pending interrupts

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	R	TAMPER			Read pending status of interrupt for event TAMPER
			NotPending	0	Read: Not pending
			Pending	1	Read: Pending
B	R	WRITEERROR			Read pending status of interrupt for event WRITEERROR
			NotPending	0	Read: Not pending
			Pending	1	Read: Pending

7.8.6.6.7 STATUS

Address offset: 0x400

The tamper controller status.

Note: Unless cleared, the STATUS register will be cumulative. A field is cleared by writing '1' to it.

Note: The glitch detectors must be reset using their CTRL registers before the STATUS register bits for glitch detectors can be cleared. The glitch detector continuously drives its output status signal to the STATUS register, hence clearing only the STATUS register is not sufficient.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW W1C	ACTIVESHIELD			Active shield detector detected an error.
			NotDetected	0	Not detected.
			Detected	1	Detected.