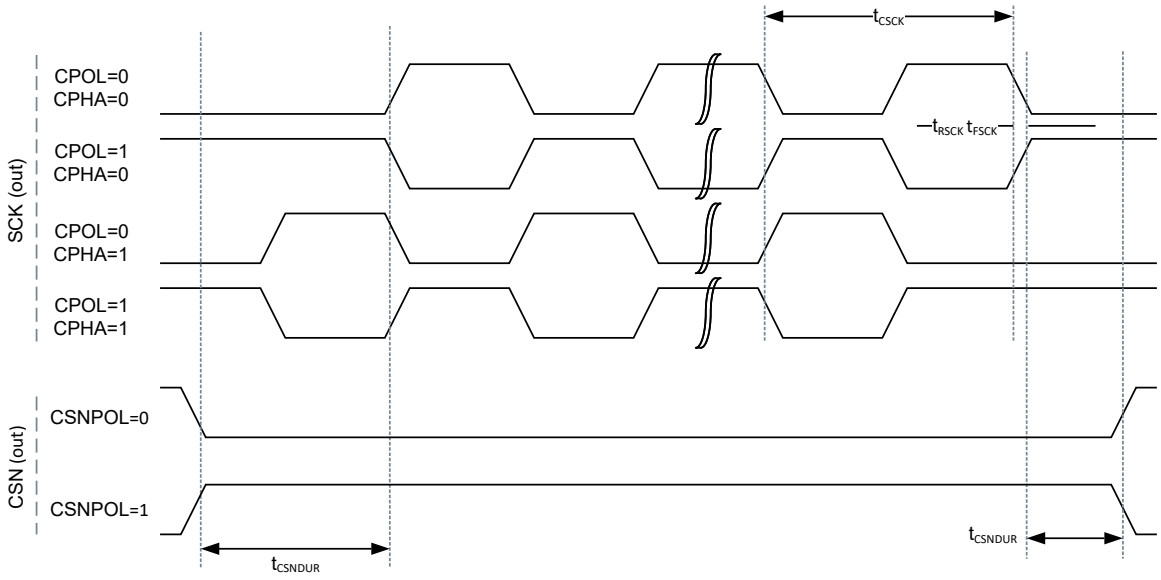

Figure 139: Polarity settings timing delay

8.19.4 Pin configuration

To configure pins for SPIM use, see the corresponding PSEL.n registers.

The contents of registers PSEL.SCK, PSEL.CSN, PSEL.DCX, PSEL.MOSI, and PSEL.MISO are only used when SPIM is enabled, and retained while the device is in System ON mode. The PSEL.n registers can be configured only when SPIM is disabled in register ENABLE on page 602.

To ensure correct behavior, the pins used by SPIM must be configured in the GPIO peripheral as described in GPIO configuration on page 586 before SPIM is enabled.

Only one peripheral can be assigned to drive a GPIO pin at a time. If more than one peripheral is assigned to a GPIO pin, it could result in unpredictable behavior.

SPIM signal	SPIM pin	Direction	Output value
SCK	As specified in PSEL.SCK on page 605	Output	Same as CONFIG.CPOL
CSN	As specified in PSEL.CSN on page 606	Output	Same as CONFIG.CPOL
DCX	As specified in PSEL.DCX on page 606	Output	1
SDO	As specified in PSEL.MOSI on page 605	Output	0
SDI	As specified in PSEL.MISO on page 606	Input	Not applicable

Table 58: GPIO configuration

SPIM supports SPI modes [0..3]. The clock polarity (CPOL) and the clock phase (CPHA) are configured in register CONFIG on page 603.