

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID			D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	C	C	C	C				B	A	
Reset 0x00000011			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
ID	R/W	Field	Value ID	Value	Description																														
B	W1	LOCK W1S			Lock this register to prevent changes to the VALUE field until next reset.																														
			Disabled	0	Lock disabled.																														
			Enabled	1	Lock enabled.																														
C	RW	WRITEPROTECTION			The write protection must be cleared to allow updates to the VALUE field.																														
					The write protection is cleared by writing CLEAR in a separate write operation prior to updating the VALUE and LOCK fields.																														
					The write protection is automatically enabled after the corresponding change to the VALUE field.																														
			Disabled	0x0	Read: Write protection is disabled.																														
			Enabled	0x1	Read: Write protection is enabled.																														
			Clear	0xF	Write: Value to clear write protection.																														
D	W	KEY			Required write key for upper 16 bits. Must be included in all register write operations.																														
			KEY	0x50FA	Write key value.																														

#### 7.8.6.6.22.2 PROTECT.GLITCHFASTDOMAIN.STATUS

Address offset: 0x94C

Status register for fast domain glitch detectors enable signal.

**Note:** Unless cleared, the STATUS register will be cumulative. A field is cleared by writing '1' to it.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A																															
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value				Description																											
A	RW	ERROR W1C						Error detection status.																											
			NoError	0				No error detected.																											
			Error	1				Error detected.																											

#### 7.8.6.6.23 PROTECT.EXTRESETEN

Trigger a reset when tamper is detected by the external tamper detectors.

This reset gives reset reason *SECTAMPER*

##### 7.8.6.6.23.1 PROTECT.EXTRESETEN.CTRL

Address offset: 0x970

Control register for external tamper reset enable signal.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	C	C	C	C			B	A	
Reset 0x00000010				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
ID	R/W	Field	Value ID	Value				Description																											
A	RW	VALUE						Set value of external tamper reset enable signal.																											
			Low	0				Signal is logic 0.																											