Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	EVENTS_FPUIDC			A floating-point input denormal exception has occurred in the FPU.
			NotGenerated	0	Event not generated
			Generated	1	Event generated

4.1.2.1.7 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	FPUIOC			Enable or disable interrupt for event FPUIOC
			Disabled	0	Disable
			Enabled	1	Enable
B	RW	FPUDZC			Enable or disable interrupt for event FPUDZC
			Disabled	0	Disable
			Enabled	1	Enable
C	RW	FPUOFC			Enable or disable interrupt for event FPUOFC
			Disabled	0	Disable
			Enabled	1	Enable
D	RW	FPUUFC			Enable or disable interrupt for event FPUUFC
			Disabled	0	Disable
			Enabled	1	Enable
E	RW	FPUIXC			Enable or disable interrupt for event FPUIXC
			Disabled	0	Disable
			Enabled	1	Enable
F	RW	FPUIDC			Enable or disable interrupt for event FPUIDC
			Disabled	0	Disable
			Enabled	1	Enable

4.1.2.1.8 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW W1S	FPUIOC			Write '1' to enable interrupt for event FPUIOC
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
B	RW W1S	FPUDZC			Write '1' to enable interrupt for event FPUDZC
			Set	1	Enable