8.6.34 INT_3 Register (Address 53h) [reset = 0h]

INT_3 is shown in Figure 8-88 and described in Table 8-44.

Return to Summary Table.

Figure 8-88. INT_3 Register

7	6	5	4	3	2	1	0
SPIERR	RSVD	FSM	CRCERR	VCCSC	RSRT_CNT	RSVD	
R/W1C-0b	R-0b	R/W1C-0b	R/W1C/U-0b	R/W1C/U-0b	R/W1C/U-0b	R-0b	

Table 8-44. INT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description0b
7	SPIERR	R/W1C	0b	Sets when SPI status bit sets
6	RSVD	R	0b	Reserved
5	FSM	R/W1C	0b	Entered fail-safe mode. Can be cleared while in failsafe mode.
4	CRCERR	R/W1C/U	0b	SPI CRC error detected
3	VCCSC	R/W1C/U	0b	V_{CC} short detected
2	RSRT_CNT	R/W1C/U	0b	Restart counter exceeded programmed count
1-0	RSVD	R	0b	Reserved

8.6.35 INT_EN_1 Register (Address = 56h) [reset = B0h]

INT_EN_1 is shown in Figure 8-89 and described in Table 8-45.

Return to Summary Table.

Interrupt mask for INT_1.

Figure 8-89. INT_EN_1 Register

7	6	5	4	3	2	1	0
WD_EN	RSVD	LWU_EN	WKERR_EN	RSVD			
R/W-1b	R-0b	R/W-1b	R/W-1b	R-0000b			

Table 8-45. INT_EN_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_EN	R/W	1b	Watchdog event interrupt enable
6	RSVD	R/W	0b	Reserved
5	LWU_EN	R/W	1b	Local wake up enable
4	WKERR_EN	R/W	1b	Wake error enable
3-0	RSVD	R	0000b	Reserved

8.6.36 INT_EN_2 Register (Address = 57h) [reset = 37h]

INT_EN_2 is shown in Figure 8-90 and described in Table 8-46.

Return to Summary Table.

Interrupt mask for INT_2.

Figure 8-90. INT_EN_2 Register

7	6	5	4	3	2	1	0
RSVD		OVCC_EN	UVSUP_EN	RSVD	UVCC_EN	TSD_VCC_LIN_EN	TSD_HSS_LMIP_EN
R-0b		R/W-1b	R/W-1b	R-0b	R/W-1b	R/W-1b	R/W-1b