

8.26.3.66 NORDIC.INMODE

Address offset: 0xBC3

Input Mode

Sets the sampling mode for values read through IN. Real Time Peripherals VIO

Shares a physical register with INTEN (lower 16 bits).

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
ID		A A			
Reset 0x00000000		0 0			
ID	R/W	Field	Value ID	Value	Description
A	RW	MODE			Input Mode
		CONTINUOUS	0x0		Continuous sampling (if CPU is not sleeping)
		EVENT	0x1		Sampling on Counter1 event
		SHIFT	0x2		Sampling and shifting on Counter1 event synchronized with OUT

8.26.3.67 NORDIC.OUTB

Address offset: 0xBC4

Buffered GPIO Output

Bits 15:0 in this register are passed to OUT on a Counter0 event (write sets dirty status). If external parameter RT_SHIFT_PRESENT = 1, OUTB bit width is 32 and in addition to the described behavior, OUTB[31:16] is passed to OUTB[15:0] on a Counter0 event as well. Real Time Peripherals VIO

OUTB[15:0] shares a physical register with MINSTRET (lower 16 bits) and EVENTS (lower 16 bits).

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
ID		f e d c b a Z Y X W V U T S R Q P O N M L K J I H G F E D C B A			
Reset 0x00000000		0 0			
ID	R/W	Field	Value ID	Value	Description
A-f	RW	PIN[i] (i=0..31)			
		LOW	0x0		Pin driver is low
		HIGH	0x1		Pin driver is high

8.26.3.68 NORDIC.DIRB

Address offset: 0xBC5

Buffered GPIO pin Direction

The value in this register is passed to DIR on a Counter0 event (write sets dirty status). Real Time Peripherals VIO.

Shares a physical register with MINSTRETH (lower 16 bits) and SUBSCRIBE (lower 16 bits).

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
ID		P O N M L K J I H G F E D C B A			
Reset 0x00000000		0 0			
ID	R/W	Field	Value ID	Value	Description
A-P	RW	PIN[i] (i=0..15)			
		INPUT	0x0		Pin is set as input
		OUTPUT	0x1		Pin is set as output