When a pin's PINx.DETECT signal goes high, a flag will be set in the register LATCH. For example, when the PIN0.DETECT signal goes high, bit 0 in the register LATCH will be set to 1. If the CPU performs a clear operation on a bit in the register LATCH when the associated PINx.DETECT signal is high, the bit in the register LATCH will not be cleared. The register LATCH will only be cleared if the CPU explicitly clears it by writing a 1 to the bit to be cleared. This means the register LATCH will not be affected by a PINx.DETECT signal being set low.

The LATCH register has split security. Non-secure code can only read the state of the non-secure pins, while the secure pins read as 0. Secure code is able to read the state of all pins.

The LDETECT signal will be set high when one or more bits in the register LATCH 1. The LDETECT signal will be set low when all bits in the register LATCH are successfully cleared to 0.

If one or more bits in the register LATCH are 1 after the CPU has performed a clear operation, a rising edge will be generated on the LDETECT signal. This is illustrated in DETECT signal behavior on page 276.

Note: The CPU can read the register LATCH at any time to check if a SENSE condition has been met on one or more of the GPIO pins. This is true even if that condition is no longer met at the time the CPU queries the register LATCH. This mechanism will work even if the LDETECT signal is not used as the DETECT signal.

LDETECT is enabled using the DETECTMODE register. See GPIO port and the GPIO pin details on page 274.

The following figure illustrates the DETECT signal behavior for these two alternatives.

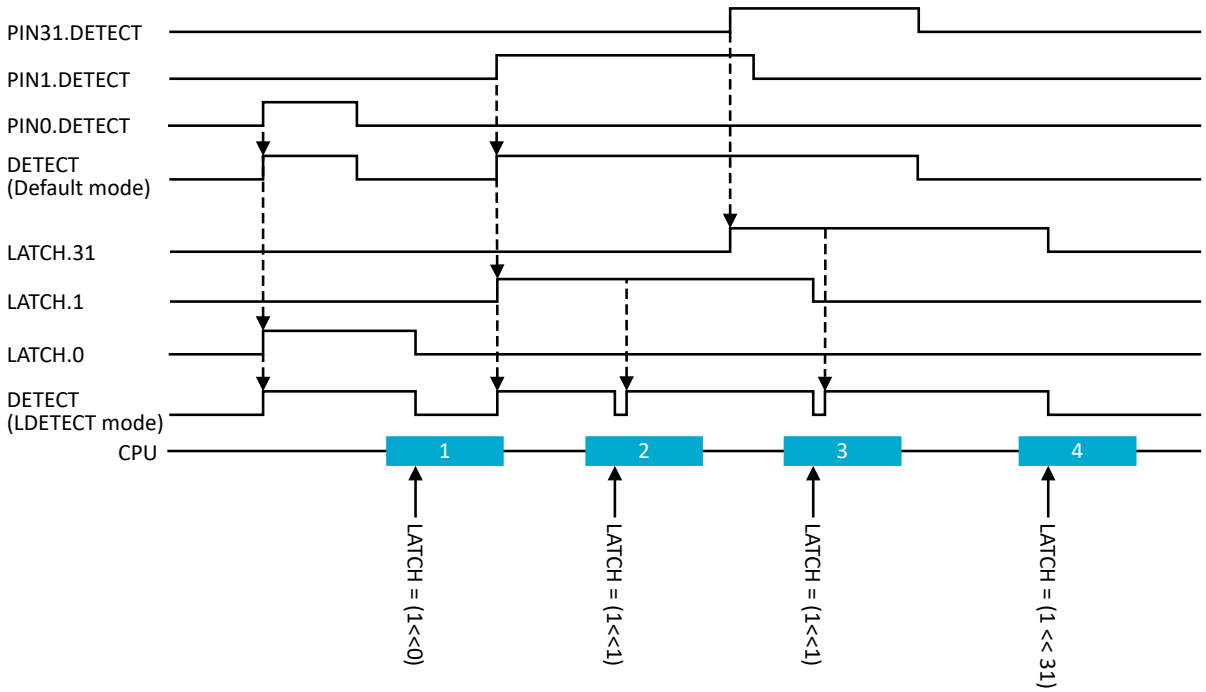

Figure 61: DETECT signal behavior

8.8.3 Port capabilities

The device power domains have their own GPIO ports with different capabilities.

The following is a list of all GPIO ports (P[n]) in the system.

- P0 low-power domain – These I/O pins can wake the system up from System OFF or System ON sleep, and can be accessed by all peripherals in the low-power domain.