Table 8-38. TIMER2_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	TIMER2_ON_WIDTH	R/W	0b	Sets the high side switch on time (ms) for timer 2 0000b = Off (HSS is high impedance) 0001b = 0.1 0010b = 0.3 0011b = 0.5 0100b = 1 0101b = 10 0110b = 20 0111b = 30 1000b = 40 1001b = 50 1010b = 60 1011b = 80 1100b = 100 1101b = 150 1110b = 200 1111b = On (HSS is on 100%) **Note** NOTE: t_{WK_CYC} which is set by $t_{WK\_CYC\_SET}$ works with these times to determine if a state change has taken place on the WAKE pin. When t_{WK_CYC} is set at 65 µs the 100 µs on width time cannot be used.
3	TIMER2_RSVD	R	0b	Reserved
2-0	TIMER2_PERIOD	R/W	0b	Sets the timer period (ms) for timer 2 000b = 10 001b = 20 010b = 50 011b = 100 100b = 200 101b = 500 110b = 1000 111b = 2000

8.6.29 RSRT_CNTR (Address = 28h) [reset = 40h]

RSRT_CNTR is shown in Figure 8-83 and described in Table 8-39

Return to Summary Table.

Restart mode counter set and counter. Determines the number of times the device has entered restart mode and when it will transition to sleep mode once programmed counter value has been reached. Counter should be reset often to avoid this transition.

Figure 8-83. RSRT_CNTR Register

7	6	5	4	3	2	1	0
RSRT_CNTR_SEL				RSRT_CNTR			
R/W-4h				R/W1C-0h			

Table 8-39. RSRT_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RSRT_CNTR_SEL	R/W	4h	Selects the number of times the device can enter restart mode prior to device entering sleep mode. Range is 0-15, representing entering restart mode 1-16 times.
3-0	RSRT_CNTR	R/W1C	0h	Provides the number of times the device has entered restart mode and should be cleared prior to reaching the RSRT_CNTR_SEL value