Table 8-46. INT_EN_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	0b	Reserved
5	OVCC_EN	R/W	1b	V_{CC} over voltage enable
4	UVSUP_EN	R/W	1b	V_{SUP} undervoltage enable
3	RSVD	R	0b	Reserved
2	UVCC_EN	R/W	1b	V_{CC} undervoltage enable
1	TSD_VCC_LIN_EN	R/W	1b	Thermal shutdown enable for VCC and LIN
0	TSD_HSS_LIMP_EN	R/W	1b	Thermal shutdown due to HSS or LIMP enable

8.6.37 INT_EN_3 Register (Address =58h) [reset = BCh]

INT_EN_3 is shown in Figure 8-91 and described in Table 8-47.

Return to Summary Table.

Interrupt mask for INT_3.

Figure 8-91. INT_EN_3 Register

7	6	5	4	3	2	1	0
SPIERR_EN	RSVD	FSM_EN	CRCERR_EN	VCCSC_EN	RSRT_CNT_EN	RSVD	
R/W-1b	R-0b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R-0b	

Table 8-47. INT_EN_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPIERR_EN	R/W	1b	SPI error interrupt enable
6	RSVD	R	0b	Reserved
5	FSM_EN	R/W	1b	Fail-safe mode interrupt enable
4	CRCERR_EN	R/W	1b	SPI CRC error interrupt enable
3	VCCSC_EN	R/W	1b	VCC short circuit interrupt enable
2	RSRT_CNT_EN	R/W	1b	Exceeding programmed restart counter interrupt enable
1-0	RSVD	R	0b	Reserved

8.6.38 INT_4 Register (Address = 5Ah) [reset = 0h]

INT_4 is shown in Figure 8-92 and described in Table 8-48.

Return to Summary Table.

Interrupt for LIN and high side switch.

Figure 8-92. INT_4 Register

7	6	5	4	3	2	1	0
LIN_WUP	LIN_DTO	RSVD		HSSOC	HSSOL	RSVD	
R/W1C-0b	R/W1C-0b	R-00b		R/W1C-0b	R/W1C-0b	R-00b	

Table 8-48. INT_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LIN_WUP	R/W1C	0b	LIN bus wake
6	LIN_DTO	R/W1C	0b	LIN dominant state timeout
5-4	RSVD	R	00b	Reserved
3	HSSOC	R/W1C	0b	High side switch over current
2	HSSOL	R/W1C	0b	High side switch open load