In cases where **left-alignment** is used, and the number of SCK pulses per frame is **lower** than the word width, the following will apply:

- Data sent and received on SDOUT and SDIN will be truncated with the LSBs being removed first.

In cases where **right-alignment** is used, and the number of SCK pulses per frame is **higher** than the configured width, the following will apply:

- For data received on SDIN, all bits before the MSB of the word value will be discarded.
- For data sent on SDOUT, all bits after the LSB of the word value will be 0 (same behavior as for left-alignment).

In cases where **right-alignment** is used, and the number of SCK pulses per frame is **lower** than the configured width, the following will apply:

- Data received on SDIN will be sign-extended to the same number of bits as the sample width before being written to memory.
- Data sent on SDOUT will be truncated with the LSBs being removed first (same behavior as for left-alignment).

8.11.7 EasyDMA

The I^{2}S module implements EasyDMA for accessing internal Data RAM without CPU intervention.

The source and destination pointers for the TX and RX data are configured in TXD.PTR on page 345 and RXD.PTR on page 345. The memory pointed to by these pointers will only be read or written when TX or RX are enabled in CONFIG.TXEN on page 342, and CONFIG.RXEN on page 341.

The addresses written to the pointer registers TXD.PTR on page 345 and RXD.PTR on page 345 are double-buffered in hardware. These double buffers are updated for every number of transmitted bytes given by RXTXD.MAXCNT on page 346 read from/written to memory. The events TXPTRUPD and RXPTRUPD are generated whenever the TXD.PTR and RXD.PTR are transferred to these double buffers.

If TXD.PTR on page 345 is not pointing to the Data RAM region when transmission is enabled, or RXD.PTR on page 345 is not pointing to the Data RAM region when reception is enabled, an EasyDMA transfer may result in a HardFault and/or memory corruption. See Memory on page 13 for more information about the different memory regions.

Due to the nature of I^{2}S, where the number of transmitted samples always equals the number of received samples (at least when both TX and RX are enabled), one common register RXTXD.MAXCNT on page 346 is used for specifying the sizes of these two memory buffers. The size of the buffers is specified in bytes.

In Stereo mode (CONFIG.CHANNELS on page 345=Stereo), the samples are stored as left and right sample pairs in memory. Memory mapping for 8-bit stereo. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo. on page 330, Memory mapping for 16-bit stereo. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Stereo. on page 330 and Memory mapping for 24-bit stereo. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Stereo. on page 331 show how the samples are mapped to memory in this mode. The mapping is valid for both RX and TX.

In Mono mode (CONFIG.CHANNELS on page 345=Left or Right), RX sample from only one channel in the frame is stored in memory, the other channel sample is ignored. Memory mapping for 8-bit mono. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Left. on page 330, Memory mapping for 16-bit mono, left channel only. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Left. on page 331 and Memory mapping for 24-bit mono, left channel only. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Left. on page 331 show how RX samples are mapped to memory in this mode. For TX, the same outgoing sample read from memory is transmitted on both left and right in a frame, resulting in a mono output stream.