Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	MODE			RRAM low power mode
			PowerDown	0	The RRAM goes into power down mode
			Standby	1	The RRAM automatically goes into standby mode while the RRAM is not being accessed This mode gives faster wake-ups, and is useful in combination with Constant Latency sub-power mode.
			NAP	2	The RRAM goes into NAP mode
			PowerOff	3	The RRAM is powered Off

4.2.6.7.25 ERASE.ERASEALL

Address offset: 0x540

Erase RRAM, including UICR

All information in SICR, including keys, are also erased

The status in READY is updated during this operation

Writes to this register are ignored when erase protect is enabled

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	ERASE			Erase RRAM
			NoOperation	0	No operation
			Erase	1	Start erase of chip

4.2.6.7.26 REGION[n] (n=0..4)

RRAMC can apply access privileges to regions of the RRAM. Some regions are dedicated for system use and are not available for configuration - refer to the instantiation table for details.

4.2.6.7.26.1 REGION[n].ADDRESS (n=0..4)

Address offset: 0x550 + (n × 0x8)

Region address

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	STARTADDR			Start address of the region [n] Bits [31:24] and bit [9:0] are read-only and set to zero

4.2.6.7.26.2 REGION[n].CONFIG (n=0..4)

Address offset: 0x554 + (n × 0x8)

Region configuration