Register	Offset	TZ	Description
INTEN	0x300		Enable or disable interrupt
INTENSET	0x304		Enable interrupt
INTENCLR	0x308		Disable interrupt
INTPEND	0x30C		Pending interrupts
STATUS	0x400		The tamper controller status.
ACTIVESHIELD.CHEN	0x404		Active shield detector channel enable register.
PROTECT.DOMAIN[n].DBGEN.CTRL	0x500		Control register for invasive (halting) debug enable for the local debug components within domain n.
PROTECT.DOMAIN[n].DBGEN.STATUS	0x504		Status register for invasive (halting) debug enable for domain n.
PROTECT.DOMAIN[n].NIDEN.CTRL	0x508		Control register for non-invasive debug enable for the local debug components within domain n.
PROTECT.DOMAIN[n].NIDEN.STATUS	0x50C		Status register for non-invasive debug enable for domain n.
PROTECT.DOMAIN[n].SPIDEN.CTRL	0x510		Control register for secure priviliged invasive (halting) debug enable for the local debug components within domain n.
PROTECT.DOMAIN[n].SPIDEN.STATUS	0x514		Status register for secure priviliged invasive (halting) debug enable for domain n.
PROTECT.DOMAIN[n].SPNIDEN.CTRL	0x518		Control register for secure priviliged non-invasive debug enable for the local debug components within domain n.
PROTECT.DOMAIN[n].SPNIDEN.STATUS	0x51C		Status register for secure priviliged non-invasive debug enable for domain n.
PROTECT.AP[n].DBGEN.CTRL	0x700		Control register to enable invasive (halting) debug in domain ns access port.
PROTECT.AP[n].DBGEN.STATUS	0x704		Status register for invasive (halting) debug enable for domain ns access port.
PROTECT.ACTIVESHIELD.CTRL	0x900		Control register for active shield detector enable signal.
PROTECT.ACTIVESHIELD.STATUS	0x904		Status register for active shield detector enable signal.
PROTECT.CRACENTAMP.CTRL	0x938		Control register for CRACEN tamper detector enable signal.
PROTECT.CRACENTAMP.STATUS	0x93C		Status register for CRACEN tamper detector enable signal.
PROTECT.GLITCHSLOWDOMAIN.CTRL	0x940		Control register for slow domain glitch detectors enable signal.
PROTECT.GLITCHSLOWDOMAIN.STATUS	0x944		Status register for slow domain glitch detectors enable signal.
PROTECT.GLITCHFASTDOMAIN.CTRL	0x948		Control register for fast domain glitch detectors enable signal.
PROTECT.GLITCHFASTDOMAIN.STATUS	0x94C		Status register for fast domain glitch detectors enable signal.
PROTECT.EXTRESETEN.CTRL	0x970		Control register for external tamper reset enable signal.
PROTECT.EXTRESETEN.STATUS	0x974		Status register for external tamper reset enable signal.
PROTECT.INTRESETEN.CTRL	0x978		Control register for internal tamper reset enable signal.
PROTECT.INTRESETEN.STATUS	0x97C		Status register for internal tamper reset enable signal.
PROTECT.ERASEPROTECT.CTRL	0x980		Control register for erase protection.
PROTECT.ERASEPROTECT.STATUS	0x984		Status register for eraseprotect.

7.8.6.6.1 EVENTS_TAMPER

Address offset: 0x100

Tamper controller detected an error.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	EVENTS_TAMPER			Tamper controller detected an error.
			NotGenerated	0	Event not generated
			Generated	1	Event generated

7.8.6.6.2 EVENTS_WRITEERROR

Address offset: 0x104

Attempt to write a VALUE in PROTECT registers without clearing the WRITEPROTECT.