Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
	RW	PUBLISH[i] (i=16..19)			
			Disabled	0x0	Publish disabled for EVENTS[i]
			Enabled	0x1	Publish enabled for EVENTS[i]

8.26.3.60 NORDIC.INTEN

Address offset: 0x7E4

DPPI Event Interrupt Enable

CSR view of the INTEN APB register (also modified through INTENSET and INTENCLR). Every bit enables interrupt generation sourced by the corresponding event. Real Time Peripherals VEVIF

Shares a physical register with INMODE.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				f e d c b a Z Y X W V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-f	RW	INTEN[i] (i=0..31)			
			Disabled	0x0	Interrupt disabled for EVENTS[i]
			Enabled	0x1	Interrupt enabled for EVENTS[i]

8.26.3.61 NORDIC.EVENTSB

Address offset: 0x7E5

Buffered DPPI Events

The value in this register is passed to EVENTS on a Counter0 event (write sets dirty status). Real Time Peripherals VEVIF

Shares a physical register with MINSTRET (lower 16 bits) and OUTB.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				f e d c b a Z Y X W V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-f	W	EVENTSB[i] (i=0..31)			
			Disabled	0x0	EVENTSB[i] disabled
			Enabled	0x1	EVENTSB[i] enabled

8.26.3.62 NORDIC.EVENTSBS

Address offset: 0x7E6

EVENTSB Dirty Status

Reads EVENTSB dirty status. Writes EVENTSB (sets dirty status)