Attribute	Value
Alen	11
Mlen	12
Adata	13
Mdata	14

Table 39: Attribute field

8.4.6 EasyDMA and ERROR event

The CCM implements an EasyDMA with scatter/gather mechanism for reading and writing to memory.

In cases where the CPU and other EasyDMA enabled peripherals are accessing the same RAM block at the same time, a high level of bus collisions may cause too slow operation for correct on the fly encryption. In this case the ERROR event will be generated.

EasyDMA will have finished accessing the memory when the END event is generated.

If the IN.PTR and the OUT.PTR are not pointing to memory with DMA connectivity, an EasyDMA transfer may result in a HardFault or memory corruption. See Memory on page 13 for more information about the different memory regions.

For instances supporting DMA error detection, the ERRORSTATUS register will report if a bus error has occurred during DMA access.

8.4.7 Registers

Instances

Instance	Domain	Base address	TrustZone			Split access	Description
			Map	Att	DMA		
CCM00 : S CCM00 : NS	GLOBAL	0x50046000 0x40046000	US	S	SA	No	AES CCM mode encryption CCM00, running of HCLKCORE

Configuration

Instance	Domain	Configuration
CCM00 : S CCM00 : NS	GLOBAL	Does not support on-the-fly decryption.

Register overview

Register	Offset	TZ	Description
TASKS_START	0x000		Start encryption/decryption. This operation will stop by itself when completed.
TASKS_STOP	0x004		Stop encryption/decryption
TASKS_RATEOVERRIDE	0x008		Override DATARATE setting in MODE register with the contents of the RATEOVERRIDE register for any ongoing encryption/decryption
SUBSCRIBE_START	0x080		Subscribe configuration for task START
SUBSCRIBE_STOP	0x084		Subscribe configuration for task STOP
SUBSCRIBE_RATEOVERRIDE	0x088		Subscribe configuration for task RATEOVERRIDE
EVENTS_END	0x104		Encrypt/decrypt complete or ended because of an error