6.6 Power Supply Characteristics (continued)

parameters valid over –40°C ≤ T_J ≤ 150 °C range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OV_{CC5R}	Over voltage 5 V VCC threshold (1)	Ramp Up		5.6	6.0	V
OV_{CC5F}	Over voltage 5 V VCC threshold (1)	Ramp Down	5.28	5.5		V
OV_{CC33R}	Over voltage 3.3 V VCC threshold (1)	Ramp Up		3.79	3.98	V
OV_{CC33F}	Over voltage 3.3 V VCC threshold (1)	Ramp Down	3.58	3.73		V
I_{CCOUT}	Output current	V_{CC} in regulation with 14V V_{SUP}	1		125	mA
I_{CCOUTL}	Output current limit	V_{CC} short to ground			275	mA
PSRR	Power supply rejection ripple rejection (1)	V_{RIP} = 0.5 V_{PP}, Load = 10 mA, f = 100 Hz, CO = 10 µF, V_{SUP} = 12 V and ambient temperature = 27 °C		60		dB
T_{SDR}	Thermal shutdown temperature (1)	Internal junction temperature; rising	160		185	°C
T_{SDF}	Thermal shutdown temperature (1)	Internal junction temperature; falling	150		170	°C
T_{SDHYS}	Thermal shutdown hysteresis (1)	V_{SUP} = 12 V		15		°C

(1) Specified by design
(2) Normal Mode: Ramp VSUP while LIN signal is a 10 kHz square wave with 50 % duty cycle and 18 V swing.

6.7 Electrical Characteristics

parameters valid over –40°C ≤ T_J ≤ 150 °C range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RXD Output Terminal						
V_{OH}	High level output voltage	I_O = –2 mA, V_{CC} = Active	0.8			V_{CC}
V_{OL}	Low level output voltage	I_O = 2 mA, V_{CC} = Active			0.2	V_{CC}
$I_{LKG(OFF)}$	Unpowered leakage current	Outputs = 5.25/3.465 V, V_{CC} = V_{SUP} = 0 V	–1		1	µA
TXD Input Terminal						
V_{IL}	Low level input voltage		–0.3		0.8	V
V_{IH}	High level input voltage		2		5.5	V
I_{IH}	High level input leakage current	TXD = V_{IH}	–5	0	5	µA
R_{TXD}	Internal pull-up resistor value		125	350	800	kΩ
LIN Terminal (Referenced to V_{SUP})						
V_{OH}	HIGH level output voltage(5)	LIN recessive, TXD = high, I_O = 0 mA, V_{SUP} = 5.5 V to 28 V	0.85			V_{SUP}
V_{OL}	LOW level output voltage(5)	LIN dominant, TXD = low, V_{SUP} = 5.5 V to 28 V			0.2	V_{SUP}
$V_{SUP\_NON\_OP}$	V_{SUP} where impact of recessive LIN bus < 5% (ISO/DIS 17987 Param 11)	TXD & RXD open V_{LIN} = 5.5 V to 45 V	–0.3		45	V
I_{BUS_LIM}	Limiting current (ISO/DIS 17987 Param 12)	TXD = 0 V, V_{LIN} = 28 V, R_{MEAS} = 440 Ω, V_{SUP} = 28 V, V_{BUSdom} ≤ 0.251 * V_{SUP}	40	90	200	mA
$I_{BUS\_PAS\_dom}$	Receiver leakage current, dominant (ISO/DIS 17987 Param 13)	V_{LIN} = 0 V, V_{SUP} = 12 V Driver off/recessive	–1			mA
$I_{BUS\_PAS\_rec1}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	V_{LIN} ≥ V_{SUP}, 5.5 V ≤ V_{SUP} ≤ 28 V Driver off			20	µA
$I_{BUS\_PAS\_rec2}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	V_{LIN} = V_{SUP}, Driver off	–5		5	µA
$I_{BUS\_NO\_GND}$	Leakage current, loss of ground (ISO/DIS 17987 Param 15)	GND = V_{SUP}, V_{SUP} = 12 V, 0 V ≤ V_{LIN} ≤ 28 V	–1		1	mA
$I_{BUS\_NO\_BAT}$	Leakage current, loss of supply (ISO/DIS 17987 Param 16)	0 V ≤ V_{LIN} ≤ 28 V, V_{SUP} = GND			10	µA
V_{BUSdom}	Low level input voltage (ISO/DIS 17987 Param 17)	LIN dominant (including LIN dominant for wake up); Figure 7-2			0.4	V_{SUP}
V_{BUSrec}	High level input voltage (ISO/DIS 17987 Param 18)	LIN recessive; Figure 7-2	0.6			V_{SUP}
V_{BUS_CNT}	Receiver center threshold (ISO/DIS 17987 Param 19)	V_{BUS_CNT} = (V_{IL} + V_{IH})/2; Figure 7-2	0.475	0.5	0.525	V_{SUP}