

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				R Q P O N M L K J I H G F E D C B A																															
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value	Description																														
K	RW	DMASEQ0BUSERROR W1C	Clear	1	Disable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
			Write '1' to disable interrupt for event DMASEQ0BUSERROR																																
			When this event is generated, the address which caused the error can be read from the BUSERRORADDRESS register.																																
			Clear	1	Disable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
L	RW	DMASEQ1END W1C	Clear	1	Disable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
			Write '1' to disable interrupt for event DMASEQ1END																																
M	RW	DMASEQ1READY W1C	Clear	1	Disable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
			Write '1' to disable interrupt for event DMASEQ1READY																																
N	RW	DMASEQ1BUSERROR W1C	Clear	1	Disable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
			Write '1' to disable interrupt for event DMASEQ1BUSERROR																																
			When this event is generated, the address which caused the error can be read from the BUSERRORADDRESS register.																																
O-R	RW	COMPAREMATCH[i] (i=0..3) W1C	Clear	1	Disable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
			Write '1' to disable interrupt for event COMPAREMATCH[i]																																

8.15.5.27 INTPEND

Address offset: 0x30C

Pending interrupts

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				R Q P O N M L K J I H G F E D C B A																															
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value	Description																														
A	R	STOPPED			Read pending status of interrupt for event STOPPED																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
B-C	R	SEQSTARTED[i] (i=0..1)			Read pending status of interrupt for event SEQSTARTED[i]																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
D-E	R	SEQEND[i] (i=0..1)			Read pending status of interrupt for event SEQEND[i]																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														