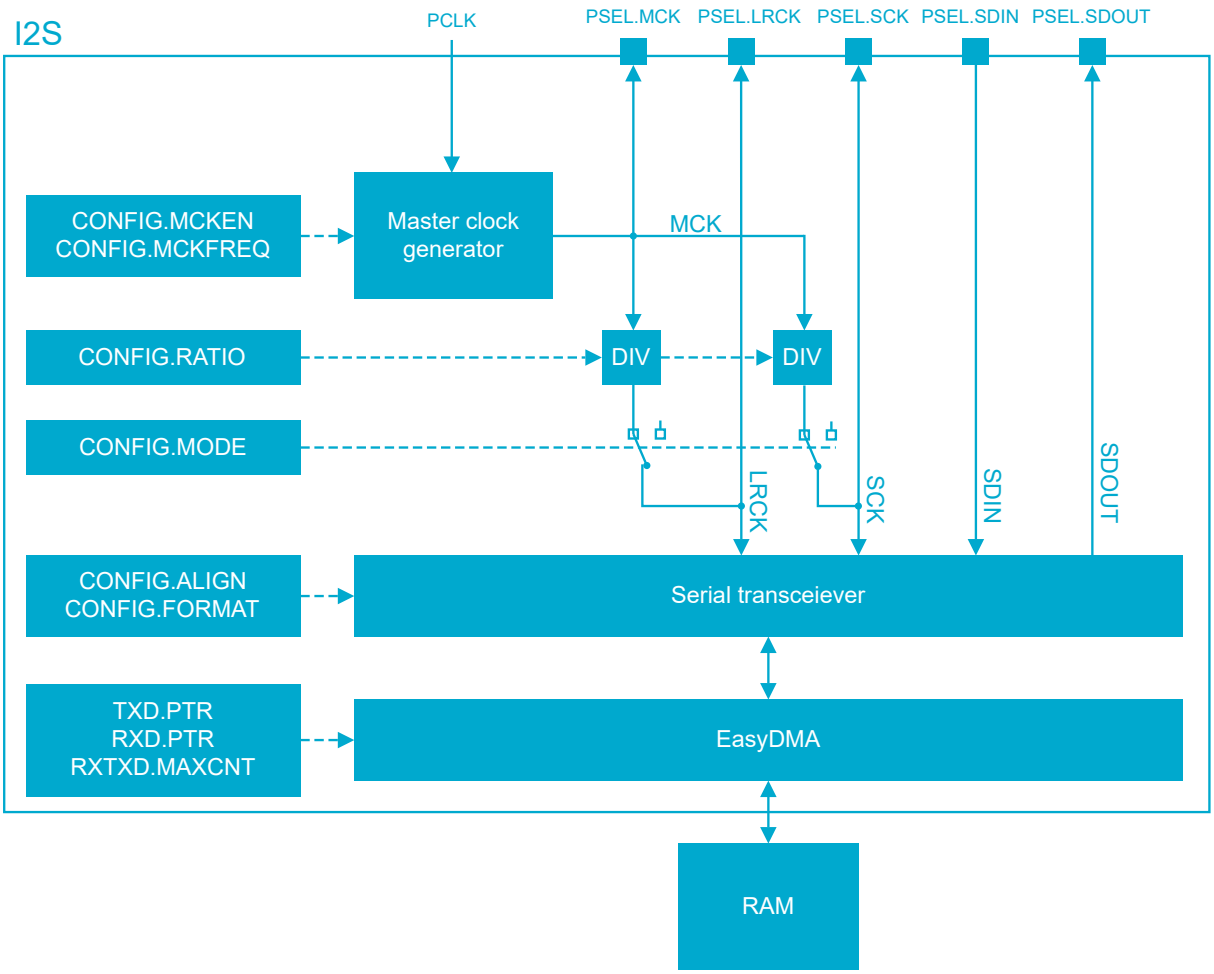


*Figure 64: I²S master*

## 8.11.1 Mode

The I²S protocol specification defines two modes of operation, Master and Slave.

In the I2S protocol, the Master always supplies the LRCK and SCK clock signals to the Slave. The device can use either the Master or Slave mode, configured using the CONFIG.MODE register.

## 8.11.2 Transmitting and receiving

The I²S module supports both transmission (TX) and reception (RX) of serial data. In both cases the serial data is shifted synchronously to the clock signals SCK and LRCK.

TX data is written to the SDOUT pin on the falling edge of SCK, and RX data is read from the SDIN pin on the rising edge of SCK. The most significant bit (MSB) is always transmitted first.

**Note:** When starting a transmission in master mode, the first frame is filled with zeros.

TX and RX are available in both Master and Slave modes and can be enabled/disabled independently in the CONFIG.TXEN on page 342 and CONFIG.RXEN on page 341.

Transmission and/or reception is started by triggering the START task. With transmission enabled in CONFIG.TXEN), the TXPTRUPD event is generated just before

```
ceil(RXTXD.MAXCNT/4)
```