Configuration

Instance	Domain	Configuration
VPR00 : S VPR00 : NS	GLOBAL	VEVIF indexes 16 through 19 maps onto DPPI channels 0 through 4 Supports RV32E (Base Integer Instruction Set embedded) Supports M extension (Integer Multiplication and Division) Supports C extension (compressed instructions) Supports Zba extension (Bit Manipulation - Address generation instructions) Supports Zbb extension (Bit Manipulation - Basic bit manipulation) Supports Zbc extension (Bit Manipulation - Carry-less multiplication) Supports Zbs extension (Bit Manipulation - Single bit instructions) Supports Zcb extension (code-size saving instructions) Does not support FENCE.I instruction (use FENCE instruction instead) Supports CSR (Control and Status Register) instructions Does not support CNTR (base counter) instructions Supports M-mode CLIC (interrupt controller) Supports MCLICCFG register Supports external debugger Debugger supports triggers (breakpoints) Boot vector (INIT_PC_RESET_VALUE): 0x00000000 Self-booting (VPR_START_RESET_VALUE): 0 VPR RAM base address (RAM_BASE_ADDR): 0x20000000 VPR RAM size (RAM_SZ): 20 (Value in bytes is computed as 2^(RAM size)) Retain registers in Deep Sleep mode: 0 Restore VPR context at VPR reset using register [NRF_MEMCONF->POWER1.RET].MEM[0] VPR context save address: 0x2003FE00 VPR context save size: 512 bytes VPR remap address: 0x00000000 VEVIF tasks: 16..22 Mask of supported VEVIF tasks: 0x007F0000 VEVIF DPPI indices: 16..19 Mask of supported VEVIF DPPI channels: 0x000F0000 VEVIF events: 16..22 Mask of supported VEVIF events: 0x00100000 Debugger interface register offset: 0x5004C400

Register overview

Register	Offset	TZ	Description
TASKS_TRIGGER[n]	0x000		VPR task [n] register
SUBSCRIBE_TRIGGER[n]	0x080		Subscribe configuration for task TASKS_TRIGGER[n]
EVENTS_TRIGGERED[n]	0x100		VPR event [n] register