The POF features a hysteresis of V_{HYST}, as illustrated in the following figure.

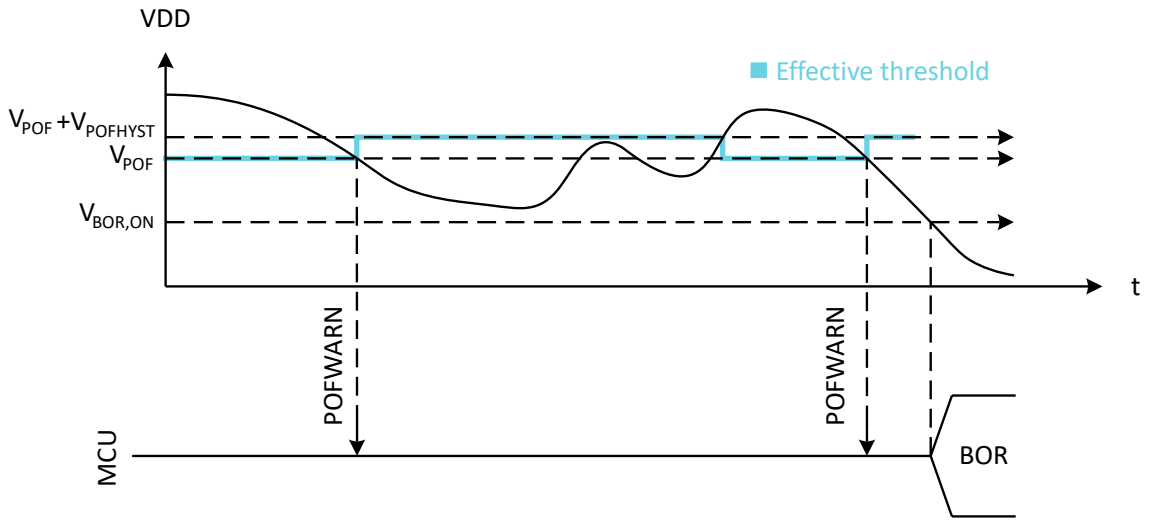

Figure 11: Power-fail comparator (BOR = Brownout reset)

To save power, the POF is not active in System ON when the HFCLK is not running, or in System OFF.

To measure the voltage, perform the following steps.

1. Disable POFWARN by writing `Disabled` to REGULATORS.POFCON.EVENTDISABLE.
2. Enable POF by writing `Enabled` to REGULATORS.POFCON.POF.
3. Loop over all threshold voltages by writing a threshold voltage into register REGULATORS.POFCON.THRESHOLD, starting at the lowest value enumerator until REGULATORS.POFSTAT toggles. This toggle indicates that the voltage has been found and can be read from register REGULATORS.POFCON.THRESHOLD.

5.4 CLOCK — Clock control

The clock control system sources the system clocks from internal or external high and low frequency oscillators. It distributes the clocks to modules based on their requirements. Clock distribution is automated and grouped independently by module to limit current consumption in unused branches of the clock tree.

The following are the main features for CLOCK:

- On-chip 128 MHz phase-locked loop (PLL) with internal oscillator
- 32 MHz crystal oscillator (when using the external 32 MHz crystal)
- 32.768 kHz RC oscillator
- 32.768 kHz crystal oscillator (when using the external 32.768 kHz crystal)
- Automatic clock control and distribution

The clock control system is responsible for requesting resources from the power and clock subsystem.