5 Pin Configuration and Functions

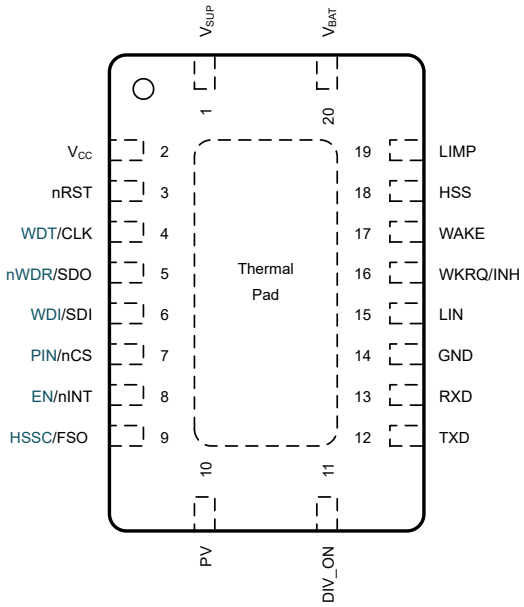


Figure 5-1. RGY Package, 20-Pin QFN (Top View)

Table 5-1. Pin Functions

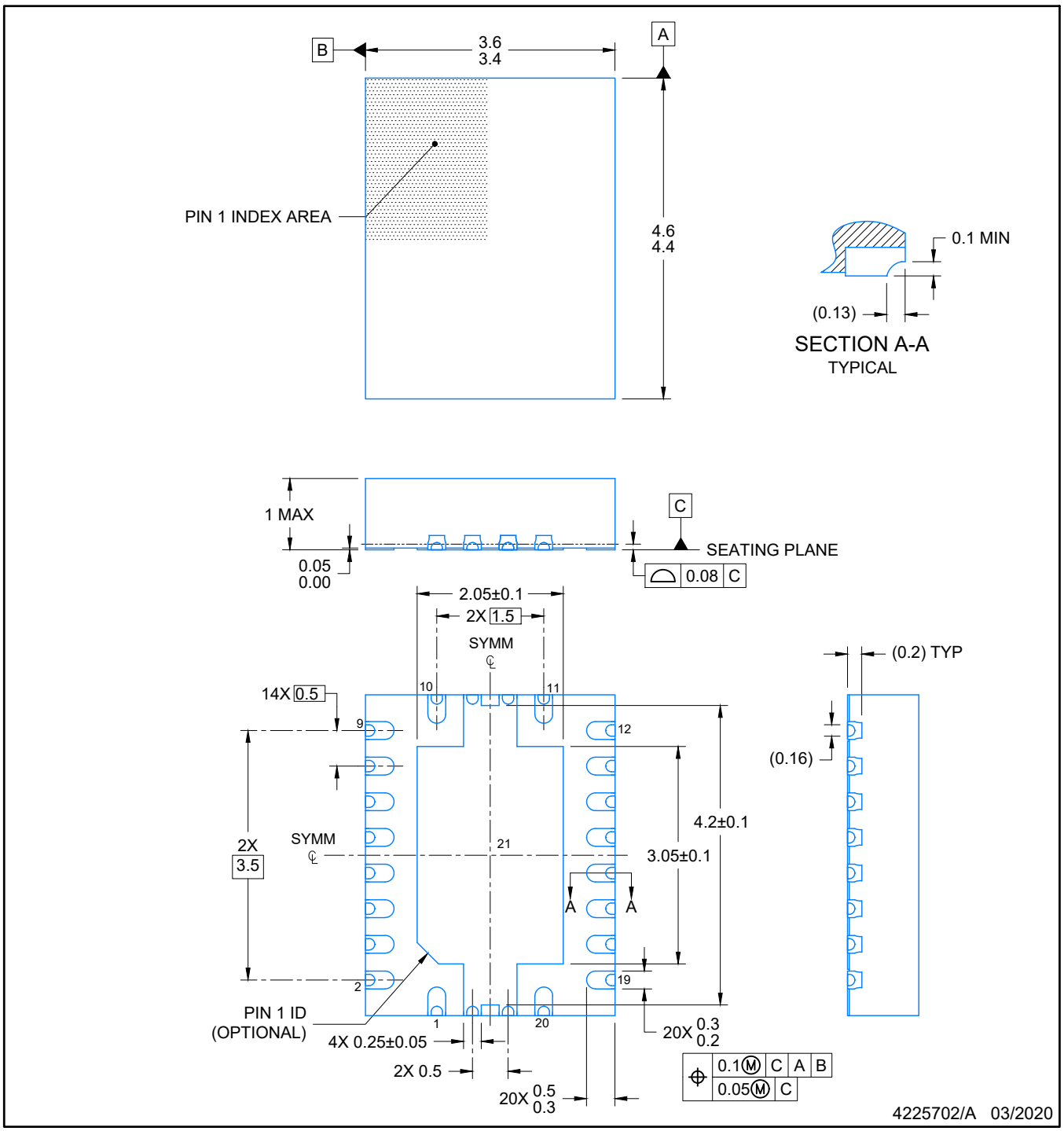
PIN		TYPE	DESCRIPTION
NAME	NO.		
V_{SUP}	1	I	Device supply voltage (connected to battery in series with external reverse blocking diode)
V_{CC}	2	O	Output voltage from integrated voltage regulator
nRST	3	I/O	Reset input/output (active low)
WDT/CLK	4	I	Pin control: WDT - Programmable watchdog window set input (3 levels) SPI control: CLK - SPI clock input
nWDR/SDO	5	O	Pin control: nWDR - Watchdog failure output trigger SPI control: SDO - SPI serial data output
WDI/SDI	6	I	Pin control: WDI - Watchdog timer trigger input active on both rising and falling edges (Must be driven at all times) SPI control: SDI - SPI serial data input
PIN/nCS	7	I	Pin or SPI control selection pin at power up. Pin control: does not change SPI control: nCS - SPI chip select (active low)
EN/nINT	8	I/O	Pin control: EN - Device mode change input pin SPI control: nINT - Device interrupt output pin
HSSC/FSO	9	I/O	Pin control: HSSC - High side switch control input pin SPI control: FSO - Function output pin
PV	10	O	Internal V_{BAT} voltage divider output
DIV_ON	11	I	Input to turn on the internal V_{BAT} voltage divider, active high
TXD	12	I	TXD input interface to control state of LIN output
RXD	13	O	RXD output interface reporting state of LIN bus voltage
GND, Pad	14	—	Ground
LIN	15	I/O	LIN bus single-wire transmitter and receiver
WKRQ/INH	16	O	Digital output for wake or high voltage inhibit output depending upon state of pin at power up
WAKE	17	I	High voltage local wake up (LWU) pin
HSS	18	O	High side switch
LIMP	19	O	Used for LIMP home, watchdog event causes this pin to switch V_{SUP}
V_{BAT}	20	I	Supply voltage divider sense input (connected to battery)

PACKAGE OUTLINE

RGY0020D

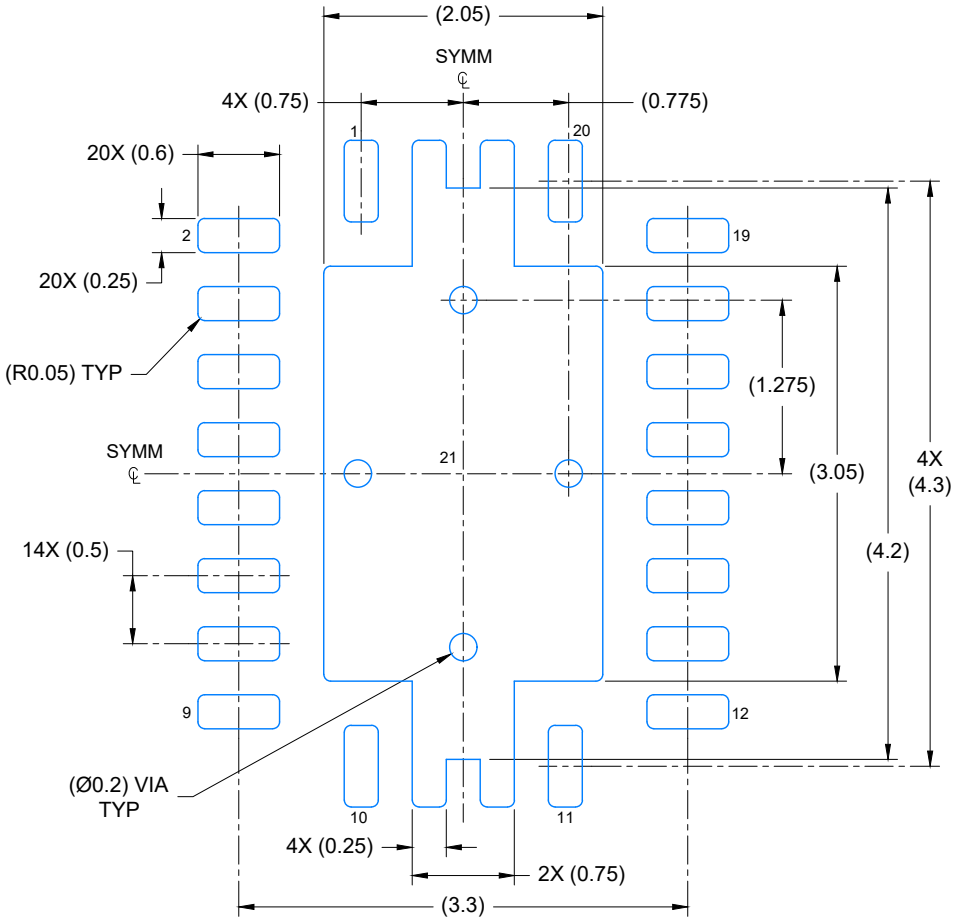
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

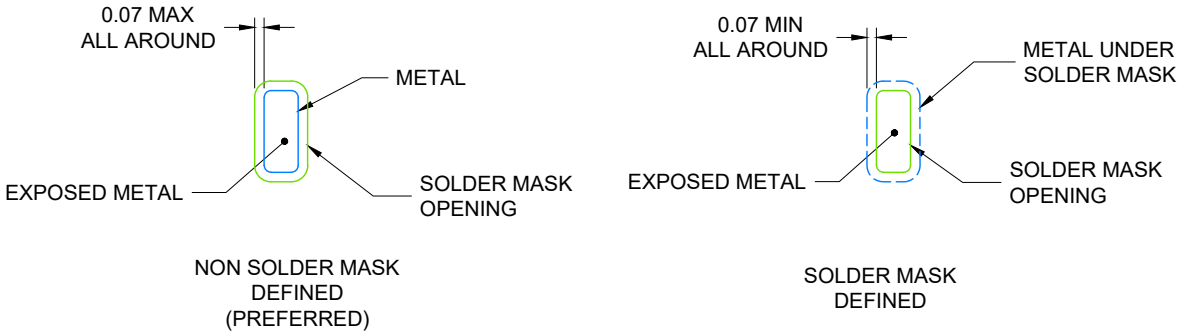
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 18X



SOLDER MASK DETAILS

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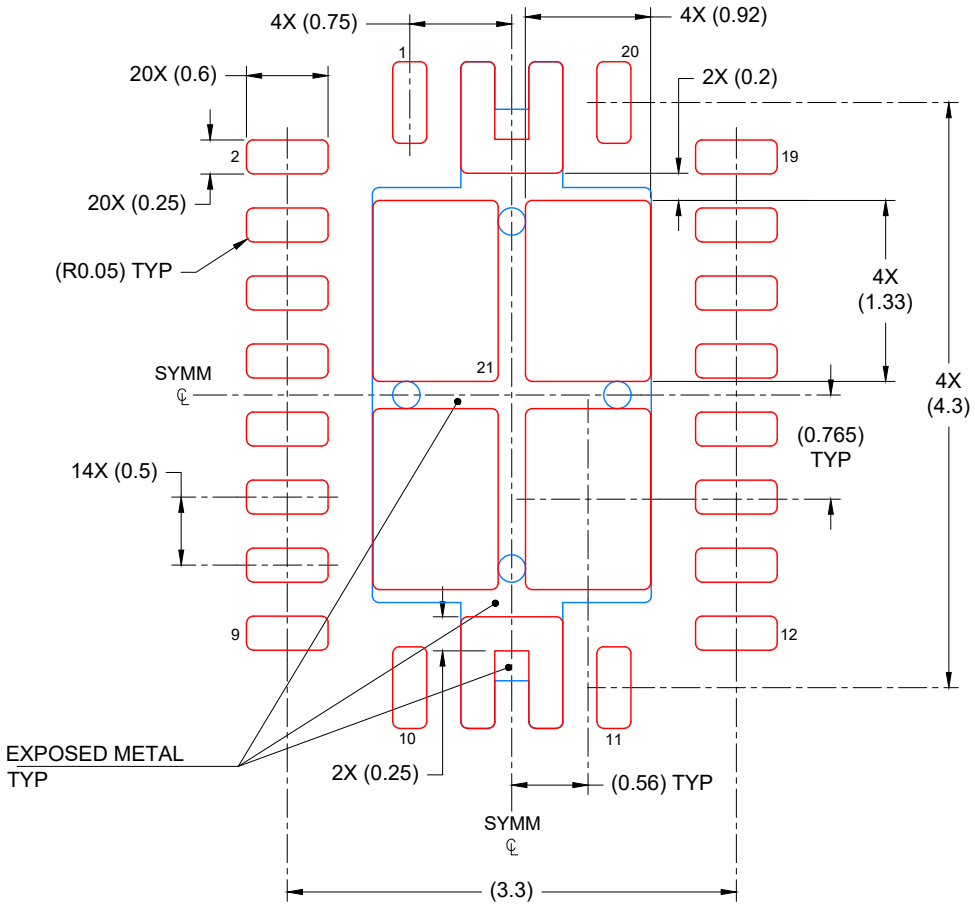
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED COVERAGE BY AREA
SCALE: 18X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.