8.26.2.1 CLIC.CLICCFG

Address offset: 0x0000

CLIC configuration.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																													C	C	B	B	B	B	A
Reset 0x00000011				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value																															
A	R	NVBITS																																	
			Implemented	1																															
B	R	NLBITS																																	
			Eight	8																															
C	R	NMBITS																																	
			ModeM	0																															

Description

A: Selective interrupt hardware vectoring.

Selective interrupt hardware vectoring is implemented

B: Interrupt level encoding.

Indicates how many upper bits are assigned to encode the interrupt level in CLICINT[n].PRIORITY

8 bits = interrupt levels encoded in eight bits

C: Interrupt privilege mode.

Indicates how many bits represent privilege mode

All interrupts are M-mode only

8.26.2.2 CLIC.CLICINFO

Address offset: 0x0004

CLIC information.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID					C	C	C	C	C	C					B	B	B	B	B	B	B	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00401FFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A	R	NUMINTERRUPTS																																	
B	R	VERSION																																	
C	R	NUMTRIGGER																																	

Description

A: Maximum number of interrupts supported.

B: Version

C: Number of maximum interrupt triggers supported

8.26.2.3 CLIC.CLICINT[n] (n=0..270)

Address offset: 0x1000 + (n × 0x4)

Interrupt control register for IRQ number [n].

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				H	H	H	H	H	H	H	H	G	G				F	F	E	D	D	D	D	D	D	C	B	B	B	B	B	B	B	A
Reset 0x3FC30000				**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	IP																																	
			NotPending	0																															
			Pending	1																															
B	R	READ1																																	
C	RW	IE																																	
			Disabled	0																															
			Enabled	1																															
D	R	READ2																																	
E	R	SHV																																	
			Vectored	1																															

Description

A: Interrupt Pending bit.

Interrupt not pending

Interrupt pending

B: Read as 0, write ignored.

C: Interrupt enable bit.

Interrupt disabled

Interrupt enabled

D: Read as 0, write ignored.

E: Selective Hardware Vectoring.

Hardware vectored