

9.8.1.31 TRCSSPCICR0

Address offset: 0x2C0

Selects the processor comparator inputs for Single-shot control.

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------------|-----|----------------|----------|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID | | | | | | | | | | | | | | | | | | | | | | | | | | | D | C | B | A | | |
| Reset 0x00000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| ID | R/W | Field | Value ID | Value | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A-D | RW | PC[i] (i=0..3) | | | Selects processor comparator i inputs for Single-shot control | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | Disabled | 0 | Processor comparator i is not selected for Single-shot control. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | Enabled | 1 | Processor comparator i is selected for Single-shot control. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

9.8.1.32 TRCPDCR

Address offset: 0x310

Controls the single-shot comparator.

9.8.1.33 TRCPDSR

Address offset: 0x314

Indicates the power down status of the ETM.