The amount of stop bits can be configured in the register CONFIG on page 743.

8.25.10 Compare match filter

UARTE has a compare match filter that can watch for a specific sequence of data. This feature is implemented in EasyDMA on the RX channel.

UARTE can generate events or interrupts when the specific data sequence is received. The event EVENTS_DMA.RX.MATCH[n] (n=0..3) on page 730 is generated when there is a match in the data stream being received. The number of MATCH can be different for each instance. See Registers on page 721 for how many MATCH events are implemented per instance.

Register DMA.RX.MATCH.CANDIDATE[n] (n=0..3) on page 747 configures the pattern for comparison. The filter is enabled with the corresponding ENABLE bit in register DMA.RX.MATCH.CONFIG on page 747. The DMA.RX.ENABLEMATCH task can be used to set that bit, and the DMA.RX.DISABLEMATCH task will clear that bit. If the ONESHOT[i] field in the CONFIG register is set, the corresponding ENABLE[i] bit will be cleared on a successful match.

For detailed information regarding the use of pattern matching in the EasyDMA engine, see EasyDMA on page 27.

8.25.11 Low power

To ensure lowest possible power consumption when the peripheral is not needed, stop and disable UARTE.

The DMA.TX.STOP and DMA.RX.STOP tasks are not always needed (the peripheral might already be stopped). If DMA.TX.STOP or DMA.RX.STOP is sent, software waits until the TXSTOPPED or RXTO event is received before disabling the peripheral through the ENABLE register.

8.25.12 Pin configuration

The RXD, CTS (Clear To Send, active low), RTS (Request To Send, active low), and TXD signals associated with UARTE are mapped to physical pins according to the configuration specified in the PSEL.n registers.

These registers and their configurations are only used when UARTE is enabled, and retained while the device is in System ON mode. The PSEL.n registers can be configured only when UARTE is disabled.

To ensure correct behavior when in System OFF mode, the pins must be configured in the GPIO peripheral as described in the following table.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

UARTE signal	UARTE pin	Direction	Output value
RXD	As specified in PSEL.RXD	Input	Not applicable
CTS	As specified in PSEL.CTS	Input	Not applicable
RTS	As specified in PSEL.RTS	Output	1
TXD	As specified in PSEL.TXD	Output	1

Table 69: GPIO configuration before enabling peripheral