

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				D C B A																															
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value	Description																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
C	RW	READYNEXT			Write '1' to enable interrupt for event <a href="#">READYNEXT</a>																														
		W1S			This event is not connected to PPI																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
D	RW	ACCESSERROR			Write '1' to enable interrupt for event <a href="#">ACCESSERROR</a>																														
		W1S			This event is not connected to PPI																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														

#### 4.2.6.7.14 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID			D C B A																															
Reset 0x00000000			0 0																															
ID	R/W	Field	Value ID	Value	Description																													
A	RW	WOKENUP  W1C			Write '1' to disable interrupt for event <span>WOKENUP</span>																													
					This event is triggered only if waken up by the <span>WAKEUP</span> task																													
			Clear	1	Disable																													
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													
B	RW	READY  W1C			Write '1' to disable interrupt for event <span>READY</span>																													
					This event is not connected to PPI																													
			Clear	1	Disable																													
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													
C	RW	READYNEXT  W1C			Write '1' to disable interrupt for event <span>READYNEXT</span>																													
					This event is not connected to PPI																													
			Clear	1	Disable																													
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													
D	RW	ACCESSERROR  W1C			Write '1' to disable interrupt for event <span>ACCESSERROR</span>																													
					This event is not connected to PPI																													
			Clear	1	Disable																													
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													

#### 4.2.6.7.15 INTPEND

Address offset: 0x30C

Pending interrupts