

9.6.5.1.3 ERASEALLSTATUS

Address offset: 0x008

This is the status register for the ERASEALL operation.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
ID																																				A	A	
Reset 0x00000000				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
ID	R/W	Field	Value ID	Value		Description																																
A	R	ERASEALLSTATUS				Status bits for the ERASEALL operation																																
			Ready	0		ERASEALL is ready																																
			ReadyToReset	1		Device is ready to be reset																																
			Busy	2		ERASEALL is busy (on-going)																																
			Error	3		Error during ERASEALL																																

9.6.5.1.4 ERASEPROTECT.STATUS

Address offset: 0x00C

Erase protection status.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				A																															
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value	Description																														
A	R	PALL			Erase protection status.																														
			Enabled	1	Erase protection is enabled.																														
			Disabled	0	Erase protection is not enabled and ERASEALL can be performed.																														

9.6.5.1.5 ERASEPROTECT.DISABLE

Address offset: 0x010

This register disables ERASEPROTECT and performs Erase all.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	R/W	Field	Value ID	Value				Description																											
A	RW	KEY						The Erase all sequence will be initiated if value of the KEY fields are non-zero and the KEY fields match on both the CPU and debugger sides.																											

9.6.5.1.6 APPROTECT.STATUS

Address offset: 0x014

This is the status register for the access port protection.