Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	R	CPUID			The CPU identifier.

4.1.3 Arm Cortex-M33 Peripherals

4.1.3.1 Instantiation

ID	Base address	Instance	TrustZone			Split access	Description
			Map	Att	DMA		
28	0x5001C000	SWI00	HF	S	NA	No	Software interrupt SWI00
29	0x5001D000	SWI01	HF	S	NA	No	Software interrupt SWI01
30	0x5001E000	SWI02	HF	S	NA	No	Software interrupt SWI02
31	0x5001F000	SWI03	HF	S	NA	No	Software interrupt SWI03
N/A	0x02F00000	ICACHEDATA	HF	S	NA	No	Instruction cache data
N/A	0x02F10000	ICACHEINFO	HF	S	NA	No	Instruction cache info
N/A	0xE0040000	TPIU	HF	NS	NA	No	Trace port interface unit (Trace and Debug)
N/A	0xE0041000	ETM	HF	NS	NA	No	Embedded trace macrocell
N/A	0xE0080000	CPUC	HF	S	NA	No	Cortex-M33 configuration
N/A	0xE0082000	ICACHE	HF	S	NA	No	Instruction cache

Table 14: Instantiation table

4.2 Core components

4.2.1 AMBA interconnect (AMBIX)

The AMBA interconnect (AMBIX) is a multilayer-capable bus interconnect that provides low latency access from Managers to Subordinates.

Manager and Subordinate connections are arranged in Manager and Subordinate pairs, allowing for a sparse bus matrix. The interconnect supports multiple concurrent transactions when targeting different Subordinates.

Some peripherals do not have the opportunity to pause incoming data. Being a low priority bus manager might cause loss of data for such peripherals upon bus contention. To avoid bus contention when using multiple bus managers, follow these guidelines:

- Avoid situations where more than one bus manager is accessing the same RAM subordinate.
- If more than one bus manager is accessing the same RAM subordinate, make sure that the bus bandwidth is not exhausted.

The interconnect enforces the TrustZone secure/non-secure attributes and is configured using MPC — Memory Privilege Controller on page 174.

4.2.1.1 AMBIX0 bus Managers and priority handling

The main interconnect (AMBIX0) has a bus matrix that handles bus arbitration.

AMBIX0 uses a round-robin bus Manager arbitration algorithm.

Some peripherals cannot pause incoming data. As a low priority bus Manager, data loss is possible for these peripherals when bus contention occurs. To avoid bus contention when using multiple bus Managers, follow these guidelines: