Figure 168: Access port unlocking

The debugger can read the access port protection status in the core's AHB-AP, using the Arm AHB-AP Control/Status Word register (CSW), defined in the *Arm CoreSight SoC-400 Technical Reference Manual*. The DbgStatus field indicates that the AHB-AP can perform AHB transfers, while the SPIStatus field indicates if secure AHB transfers are permitted. For a list of all debug access ports, see Debug access port on page 815.

9.3 Debug Interface mode

Before the external debugger can connect to an access port, the debugger must first request the device to power up through CxxxPWRUPREQ in the SWJ-DP.

The device remains in Debug Interface mode when the debugger requests power through CxxxPWRUPREQ. Otherwise, the device is in normal mode. When a debug session is over, the device must be set to normal mode by the external debugger, followed by a pin reset. This reduces overall power consumption.

Some peripherals behave differently in Debug Interface mode compared to normal mode. These differences are described in more detail in the corresponding peripheral chapter.

For details on how to use the debug capabilities, read the debug documentation of your IDE.

If the device is in System OFF when power is requested from CxxxPWRUPREQ, the system wakes up and the DIF flag in RESETREAS on page 104 is set.

9.4 Real-time debug

The device supports real-time debugging. This allows interrupts to execute to completion in real time when breakpoints are set in Thread mode or lower priority interrupts.

Real-time debugging enables setting a breakpoint for single-stepping through code. This prevents real-time event-driven threads from running at a higher priority. For example, this enables the device to continue to service high-priority interrupts of an external controller or sensor, without failure or loss of state synchronization, while stepping through code in a low-priority thread.

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