

Bit number					31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
ID																																						A
Reset 0x00000000					0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
ID	R/W	Field	Value ID	Value	Description																																	
A	RW	END			Generated after all MAXCNT bytes have been transferred																																	
			NotGenerated	0	Event not generated																																	
			Generated	1	Event generated																																	

8.20.7.9.1.2 EVENTS_DMA.RX.READY

Address offset: 0x150

Generated when EasyDMA has buffered the .PTR and .MAXCNT registers for the channel, allowing them to be written to prepare for the next sequence.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				A																															
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value	Description																														
A	RW	READY			Generated when EasyDMA has buffered the .PTR and .MAXCNT registers for the channel, allowing them to be written to prepare for the next sequence.																														
			NotGenerated	0	Event not generated																														
			Generated	1	Event generated																														

8.20.7.9.1.3 EVENTS_DMA.RX.BUSERROR

Address offset: 0x154

An error occurred during the bus transfer.

When this event is generated, the address which caused the error can be read from the BUSERRORADDRESS register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
ID				A																																			
Reset 0x00000000				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
ID	R/W	Field	Value ID	Value		Description																																	
A	RW	BUSERROR				An error ocured during the bus transfer.																																	
						When this event is generated, the address which caused the error can be read from the BUSERRORADDRESS register.																																	
			NotGenerated	0	Event not generated																																		
			Generated	1	Event generated																																		

8.20.7.9.1.4 EVENTS_DMA.RX.MATCH[n] (n=0..3)

Address offset: 0x158 + (n × 0x4)

Pattern match is detected on the DMA data bus.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				A																															
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value	Description																														
A	RW	MATCH			Pattern match is detected on the DMA data bus.																														
			NotGenerated	0	Event not generated																														
			Generated	1	Event generated																														