Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX		[0..255]	DPPI channel that event MHRMATCH will publish to
B	RW	EN			
			Disabled	0	Disable publishing
			Enabled	1	Enable publishing

8.17.14.83 PUBLISH_SYNC

Address offset: 0x358

Publish configuration for event SYNC

MODE=Ble_LR125Kbit, Ble_LR500Kbit, or Ieee802154_250Kbit: A possible preamble has been received. However, due to the sporadic reception of noise, this event can be falsely triggered.

For MODE=Nrf_1Mbit, Nrf_2Mbit, Ble_1Mbit, or Ble_2Mbit: A possible preamble and the first two bytes of the address field has been received. The event can be generated falsely also in this mode.

It is also possible that the event is not generated, or not generated before the ADDRESS event.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX		[0..255]	DPPI channel that event SYNC will publish to
B	RW	EN			
			Disabled	0	Disable publishing
			Enabled	1	Enable publishing

8.17.14.84 PUBLISH_CTEPRESENT

Address offset: 0x35C

Publish configuration for event CTEPRESENT

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX		[0..255]	DPPI channel that event CTEPRESENT will publish to
B	RW	EN			
			Disabled	0	Disable publishing
			Enabled	1	Enable publishing

8.17.14.85 PUBLISH_PLLREADY

Address offset: 0x3B0

Publish configuration for event PLLREADY