

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A																															
<b>Reset</b> 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
ID	R/W	Field	Value ID	Value	Description																											
A	RW	END			Generated after EasyDMA has completed its operation.																											
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

### ***8.25.13.12.2.2 EVENTS\_DMA.TX.READY***

Address offset: 0x16C

Generated when EasyDMA has buffered the .PTR and .MAXCNT registers for the channel, allowing them to be written to prepare for the next sequence.

### ***8.25.13.12.2.3 EVENTS DMA.TX.BUSERRO***

Address offset: 0x170

An error occurred during the bus transfer.

When this event is generated, the address which caused the error can be read from the **BUSERRORADDRESS** register.

## 8.25.13.13 EVENTS FRAMETIMEOUT

Address offset: 0x174

Timed out due to bus being idle while receiving data.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID																															A		
<b>Reset 0x00000000</b>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	R/W	Field	Value ID	Value	Description																												
A	RW	EVENTS_FRAME TIMEOUT			Timed out due to bus being idle while receiving data.																												
		NotGenerated	0		Event not generated																												
		Generated	1		Event generated																												