

For detailed information regarding the use of EasyDMA, see [EasyDMA](#) on page 27.

The STOPPED event indicates that EasyDMA is finished accessing the buffer in RAM.

#### 8.24.4 Read command response

Before TWIS can respond to a read command, it must be configured and enabled in the ENABLE register. When enabled, TWIS is in the IDLE state.

A read command is started when TWIM generates a start condition on the TWI bus. This is followed by clocking out the address and setting the READ/WRITE bit to 1 (READ=1, WRITE=0). The READ/WRITE bit is followed by an ACK/NACK bit (ACK = 0, NACK = 1) response from the TWIS.

TWIS can listen for two addresses at a time. This is configured in the ADDRESS registers and the CONFIG register.

TWIS only acknowledges (ACK) the read command if the address presented by the controller matches one of the addresses the target is configured to listen for. TWIS will generate a READ event when it acknowledges the read command.

TWIS only detects a read command from the IDLE state.

TWIS will set an internal **TX prepared** flag when the PREPARETX task is triggered.

When the read command is received, TWIS will enter the TX state if the internal **TX prepared** flag is set.

If the internal **TX prepared** flag is not set when the read command is received, TWIS will stretch the controller's clock until the PREPARETX task is triggered and the internal **TX prepared** flag is set.

TWIS will generate the EVENTS\_DMA.TX.READY event and clear the **TX prepared** flag when it enters the TX state. In this state, TWIS will send the data bytes found in the transmit buffer to the controller using the controller's clock.

TWIS returns to the IDLE state if the TWIS receives a restart command when it is in the TX state.

TWIS is stopped when it receives the stop condition from TWIM. A STOPPED event will be generated when the transaction has stopped. TWIS will clear the **TX prepared** flag and go back to the IDLE state when it has stopped.

The transmit buffer is located in RAM at the address specified in the TXD.PTR register. TWIS will only be able to send TXD.MAXCNT bytes from the transmit buffer for each transaction. If TWIM forces TWIS to send more than TXD.MAXCNT bytes, the target will send the byte specified in the ORC register to the controller instead. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers RXD.PTR, TXD.PTR, RXD.AMOUNT, and TXD.AMOUNT, are latched when the EVENTS\_DMA.TX.READY event is generated.

TWIS can be forced to stop by triggering the STOP task. A STOPPED event will be generated when TWIS has stopped. TWIS will clear the **TX prepared** flag and return to the IDLE state when it has stopped, see [Terminate an ongoing TWI transaction](#) on page 690.

Each byte sent from TWIS will be followed by an ACK/NACK bit sent from the controller. TWIM will generate a NACK following the last byte that it wants to receive to tell the target to release the bus allowing TWIM to generate the stop condition. The TXD.AMOUNT register can be queried after a transaction to see how many bytes were sent.

A typical TWIS read command response is illustrated in the following figure, including clock stretching following a SUSPEND task.