Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D D D D D D D D D D D D D D D D C C C C B A
Reset 0x00000010				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
C	RW	WRITEPROTECTION			The write protection must be cleared to allow updates to the VALUE field. The write protection is cleared by writing CLEAR in a separate write operation prior to updating the VALUE and LOCK fields. The write protection is automatically enabled after the corresponding change to the VALUE field.
			Disabled	0x0	Read: Write protection is disabled.
			Enabled	0x1	Read: Write protection is enabled.
			Clear	0xF	Write: Value to clear write protection.
D	W	KEY			Required write key for upper 16 bits. Must be included in all register write operations.
			KEY	0x50FA	Write key value.

7.8.6.6.12 PROTECT.DOMAIN[n].NIDEN.STATUS (n=0..0)

Address offset: 0x50C + (n × 0x20)

Status register for non-invasive debug enable for domain n.

Note: Unless cleared, the STATUS register will be cumulative. A field is cleared by writing '1' to it.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW W1C	ERROR			Error detection status.
			NoError	0	No error detected.
			Error	1	Error detected.

7.8.6.6.13 PROTECT.DOMAIN[n].SPIDEN.CTRL (n=0..0)

Address offset: 0x510 + (n × 0x20)

Control register for secure priviliged invasive (halting) debug enable for the local debug components within domain n.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D D D D D D D D D D D D D D D D C C C C B A
Reset 0x00000010				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	VALUE			Set value of spiden signal.
			Low	0	Signal is logic 0, indicating that secure priviliged invasive debug is disabled.
			High	1	Signal is logic 1, indicating that secure priviliged invasive debug is enabled.
B	W1 W1S	LOCK			Lock this register to prevent changes to the VALUE field until next reset.
			Disabled	0	Lock disabled.
			Enabled	1	Lock enabled.