Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				R Q P O N M L K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
G	RW W1S	LOOPSDONE			Write '1' to enable interrupt for event LOOPSDONE This event triggers after the last SEQ[1] completion of the loop, and only if looping was enabled (LOOP > 0) when the sequence playback was started.
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
H	RW W1S	RAMUNDERFLOW			Write '1' to enable interrupt for event RAMUNDERFLOW
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
I	RW W1S	DMASEQ0END			Write '1' to enable interrupt for event DMASEQ0END
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
J	RW W1S	DMASEQ0READY			Write '1' to enable interrupt for event DMASEQ0READY
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
K	RW W1S	DMASEQ0BUSERROR			Write '1' to enable interrupt for event DMASEQ0BUSERROR When this event is generated, the address which caused the error can be read from the BUSERRORADDRESS register.
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
L	RW W1S	DMASEQ1END			Write '1' to enable interrupt for event DMASEQ1END
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
M	RW W1S	DMASEQ1READY			Write '1' to enable interrupt for event DMASEQ1READY
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
N	RW W1S	DMASEQ1BUSERROR			Write '1' to enable interrupt for event DMASEQ1BUSERROR When this event is generated, the address which caused the error can be read from the BUSERRORADDRESS register.
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
O-R	RW W1S	COMPAREMATCH[i] (i=0..3)			Write '1' to enable interrupt for event COMPAREMATCH[i]
			Set	1	Enable
			Disabled	0	Read: Disabled