Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000001				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1**
ID	R/W	Field	Value ID	Value	Description
A	R	BA418SHA3HWCFG			Generic g_Sha3CtxtEn value. BA418-SHA3 configuration.

7.8.1.7.22 CRYPTMSTRHW.BA419SM4HWCFG

Address offset: 0x414

Generic g_SM4ModesPoss value.

BA419-SM4 engine configuration.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A A A A A A A A A
Reset 0x000201FF				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1**
ID	R/W	Field	Value ID	Value	Description
A	R	BA419SM4HWCFG			Generic g_SM4ModesPoss value. BA419-SM4 engine configuration.
B	R	USEMASKING			Generic g_sm4UseMasking value. BA419-SM4 engine configuration.

7.8.1.7.23 CRYPTMSTRHW.BA424ARIAHWCFG

Address offset: 0x418

Generic g_aria_modePoss value.

BA424-Aria engine configuration.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A
Reset 0x0000017F				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 1 1 1 1 1**
ID	R/W	Field	Value ID	Value	Description
A	R	BA424ARIAHWCFG			Generic g_aria_modePoss value. BA424-Aria engine configuration.

7.8.1.7.24 RNGCONTROL.CONTROL

Address offset: 0x1000

Control register

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				Q P P P O N M L K J I H G F E D C B A
Reset 0x00040000				**0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	ENABLE			Enable the RNG. Clearing this bit resets the RNG FSM.
B	RW	LFSREN			Select between the RNG with asynchronous free running ring oscillators (when 0) and the Pseudo-Random generator with synchronous oscillators for simulation purpose (when 1).
C	RW	TESTEN			Select input for conditioning function and continuous tests:
			NORMAL	0	Noise source (normal mode).