7.8.1.7.46 PK.STATUS

Address offset: 0x200C

Status register.

Bit number					31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID								D	D	D	D	D							C	B	A	A	A	A	A	A	A	A	A	A	A				
Reset 0x00000000					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description																															
A	R	ERRORFLAGS			These bits indicate an error condition. They are updated at the end of the operation. They are cleared when starting a new operation.																																
B	R	PKBUSY			This bit reflects the BUSY output value. It is set when the operation starts and it is cleared when the operation is finished.																																
C	R	INTRPTSTATUS			This bit reflects the IRQ output value. It is set when the operation is finished. It is cleared when the CPU writes the bit 1 of Control Register.																																
D	R	FAILPTR			These bits indicate which data location generated the error flag. They are not available for all error flags.																																

7.8.1.7.47 PK.TIMER

Address offset: 0x2014

Timer register.

Bit number					31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID					A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description																															
A	RW	TIMER			Number of core clock cycles.																																

7.8.1.7.48 PK.HWCONFIG

Address offset: 0x2018

Hardware configuration register.

Bit number					31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID					N	M	L				K	J	I	H	G	F		E	D	C	B	B	B	B	A	A	A	A	A	A	A	A	A	A	A
Reset 0x01F72200					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description																															
A	R	MAXOPSIZE			Maximum operand size (number of bytes).																																
B	R	NBMULT			Number of multipliers:																																
			MULT1	0	1 multiplier																																
			MULT4	1	4 multipliers																																
			MULT16	2	16 multipliers																																
			MULT64	4	64 multipliers																																
			MULT256	8	256 multipliers																																
C	R	PRIMEFIELD			Support prime field.																																
D	R	BINARYFIELD			Support binary field.																																
E	R	ECC			Support error correction.																																