Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				f e d c b a Z Y X W V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-f	RW	TASKS[i] (i=0..31)			
			Disabled	0x0	TASKS[i] diabled
			Enabled	0x1	TASKS[i] enabled

8.26.3.57 NORDIC.SUBSCRIBE

Address offset: 0x7E1

Enable Task Subscription

CSR view of SUBSCRIBE_TRIGGER[31:0] APB registers (Enable bits). Real Time Peripherals VEVIF

Shares a physical register with DIRB and MINSTRETH (lower 16 bits).

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
	RW	SUBSCRIBE[i] (i=16..19)			
			Disabled	0x0	Subscribe disabled for TASK[i]
			Enabled	0x1	Subscribe enabled for TASK[i]

8.26.3.58 NORDIC.EVENTS

Address offset: 0x7E2

DPPI Events

CSR view of EVENTS_TRIGGERED[31:0]APB registers. Real Time Peripherals VEVIF

Shares a physical register with MINSTRET (upper 16 bits) and OUT.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				f e d c b a Z Y X W V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-f	RW	EVENTS[i] (i=0..31)			
			Disabled	0x0	EVENTS[i] disabled
			Enabled	0x1	EVENTS[i] enabled

8.26.3.59 NORDIC.PUBLISH

Address offset: 0x7E3

Enable Event Publication

CSR view of PUBLISH_TRIGGERED[31:0] APB registers (Enable bits). Real Time Peripherals VEVIF

Shares a physical register with DIR and MINSTRETH (upper 16 bits).