Crystal load capacitor as seen by the crystal across its terminals, including pin capacitance but excluding PCB stray capacitance.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A
Reset 0x00000020				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	VAL			Crystal load capacitor value Use the provided equation in OSCILLATORS — Oscillator control on page 86 to calculate the register value.

5.5.4.2 PLL

Oscillator control

5.5.4.2.1 PLL.FREQ (Retained)

Address offset: 0x800

Set speed of MCU power domain, including CPU

This register is retained.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A
Reset 0x00000003				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1**
ID	R/W	Field	Value ID	Value	Description
A	RW	FREQ			Select CPU speed
			CK128M	1	128 MHz
			CK64M	3	64 MHz

5.5.4.2.2 PLL.CURRENTFREQ (Retained)

Address offset: 0x804

Current speed of MCU power domain, including CPU

This register is retained.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A
Reset 0x00000003				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1**
ID	R/W	Field	Value ID	Value	Description
A	R	CURRENTFREQ			Active CPU speed
			CK128M	1	128 MHz
			CK64M	3	64 MHz

5.5.4.3 XOSC32KI

32.768 kHz oscillator control

5.5.4.3.1 XOSC32KI.BYPASS

Address offset: 0x900

Enable or disable bypass of LFCLK crystal oscillator with external clock source