Figure 8-72. SWE_TIMER Register

7	6	5	4	3	2	1	0
SWE_DIS	SWE_TIMER_SET				RSVD		
R/W-0b	R/W-0110b				R		

Table 8-28. SWE_TIMER Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SWE_DIS	R/W	0b	Sleep wake error disable: NOTE: This disables the device from starting the t_{INACT_FS} timer. If enabled, a SPI read or write must take place within this window or the device will go back to sleep. 0b = Enabled 1b = Disabled
6-3	SWE_TIMER_SET	R/W	0110b	Sets the timer used for t_{INACT_FS} (minutes) 0000b = 2 0001b = 2.5 0010b = 3 0011b = 3.5 0100b = 4 0101b = 4.5 0110b = 5 (default) 0111b = 5.5 1000b = 6 1001b = 6.5 1010b = 8 1011b = 8.5 1100b = 10 1101b = 0.5 1111b = 1
2-0	RSVD	R	0b	Reserved

8.6.19 LIN_CNTL (Address = 1Dh) [reset = 00h]

LIN_CNTL is shown in Figure 8-73 and described in Table 8-29

Return to Summary Table.

LIN transceiver mode and DTO control. Port 1 is the TLIN1431x-Q1 LIN control.

Figure 8-73. LIN_CNTL Register

7	6	5	4	3	2	1	0
LIN_MODE		LIN_DTO_DIS	LIN_RSVD				
R/W/H-00b		R/W - 0b	R - 00000b				

Table 8-29. LIN_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LIN_MODE	R/W/H	00b	Port 1 LIN mode control 00b = Standby mode 01b = Sleep Mode 10b = Normal Mode 11b = Fast Mode
5	LIN_DTO_DIS	R/W	0b	Port 1 LIN dominant state timeout disable 0b = Enabled 1b = Disabled
4-0	LIN_RSVD	R	00000b	Reserved