Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				C C C C B B B B A A A A
Reset 0x00000EEE				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0 1 1 1 0 1 1 1 0**
ID	R/W	Field	Value ID	Value	Description
C	RW	DARCACHE			Memory type for data loads
			DEVNONBUFF	0x0	Device Non-Bufferable
			DEVBUFF	0x1	Device Bufferable
			NNONCACHENONBUFF	0x2	Normal Non-cacheable Non-bufferable
			NNONCACHEBUFF	0x3	Normal Non-cacheable Bufferable
			WRITETHNALLOC	0xA	Write-through No-allocate
			WRITETHRALLOC	0xE	Write-through Read-allocate
			WRITETHWALLOC	0xA	Write-through Write-allocate
			WRITETHRWALLOC	0xE	Write-through Read and Write-allocate
			WRITEBACKNALLOC	0xB	Write-back No-allocate
			WRITEBACKRALLOC	0xF	Write-back Read-allocate
			WRITEBACKWALLOC	0xB	Write-back Write-allocate
			WRITEBACKRWALLOC	0xF	Write-back Read and Write-allocate

8.26.3.39 NORDIC.CACHE.CTRL

Address offset: 0x7C8

Cache control

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	ENABLE			Enable cache
			Disabled	0	Cache disabled
			Enabled	1	Cache enabled
B	RW W1S	CACHECLR			Cache clear Writing this bit writes the tag cache region to 0. This should be done before enabling the cache. The CPU stalls until the operation is complete. Interrupts must be disabled when performing the cache clear operation.
			NoOperation	0	No Operation
			Clear	1	Cache clear

8.26.3.40 NORDIC.CACHE.CFG

Address offset: 0x7C9

Cache configuration

Configures the cache region size and line size