In addition, CPUC holds a LOCK register, which is used to lock certain CPU features and prevent them from being modified. One example is the LOCK.LOCKSAU field. When set to `Locked`, this prevents further modifications to the SAU registers.

4.1.2.1 Registers

Instances

Instance	Domain	Base address	TrustZone			Split access	Description
			Map	Att	DMA		
CPUC	APPLICATION	0xE0080000	HF	S	NA	No	Cortex-M33 configuration

Register overview

Register	Offset	TZ	Description
EVENTS_FPUIOC	0x100		An invalid operation exception has occurred in the FPU.
EVENTS_FPUDZC	0x104		A floating-point divide-by-zero exception has occurred in the FPU.
EVENTS_FPUOFC	0x108		A floating-point overflow exception has occurred in the FPU.
EVENTS_FPUUFC	0x10C		A floating-point underflow exception has occurred in the FPU.
EVENTS_FPUIXC	0x110		A floating-point inexact exception has occurred in the FPU.
EVENTS_FPUIDC	0x114		A floating-point input denormal exception has occurred in the FPU.
INTEN	0x300		Enable or disable interrupt
INTENSET	0x304		Enable interrupt
INTENCLR	0x308		Disable interrupt
LOCK	0x500		Register to lock the certain parts of the CPU from being modified.
CPUID	0x504		The identifier for the CPU in this subsystem.

4.1.2.1.1 EVENTS_FPUIOC

Address offset: 0x100

An invalid operation exception has occurred in the FPU.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	EVENTS_FPUIOC																																	An invalid operation exception has occurred in the FPU.
			NotGenerated	0																															Event not generated
			Generated	1																															Event generated

4.1.2.1.2 EVENTS_FPUDZC

Address offset: 0x104

A floating-point divide-by-zero exception has occurred in the FPU.