

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ID																															A		
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	R/W	Field	Value ID	Value	Description																												
A	W	START			Starts operation using easyDMA to load the values. See peripheral description for operation using easyDMA.																												
		Trigger	1	Trigger task																													

8.25.13.2.1.2 TASKS_DMA.RX STOP

Address offset: 0x02C

Stops operation using easyDMA. This does not trigger an END event.

8.25.13.2.1.3 TASKS_DMA.RX.ENABLEMATCH[n] (n=0..3)

Address offset: $0x030 + (n \times 0x4)$

Enables the MATCH[n] event by setting the ENABLE[n] bit in the CONFIG register.

8.25.13.2.1.4 TASKS DMA.RX.DISABLEMATCH[n] (n=0..3)

Address offset: $0x040 + (n \times 0x4)$

Disables the MATCH[n] event by clearing the ENABLE[n] bit in the CONFIG register.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A																															
Reset 0x00000000																																
ID	R/W	Field	Value ID	Value	Description																											
A	W	DISABLEMATCH			Disables the MATCH[n] event by clearing the ENABLE[n] bit in the CONFIG register.																											
		Trigger	1	Trigger task																												

8.25.13.2.2 TASKS DMA.TX

Peripheral tasks

8.25.13.2.2.1 TASKS DMA TX START

Address offset: 0x050