Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID					P	O		N		M														L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
			Pending	1																															
				Read: Pending																															

8.10.7.21 INTEN1

Address offset: 0x310

Enable or disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID					P	O		N		M														L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A-L	RW	COMPARE[i] (i=0..11)																																	
			Disabled	0																															
			Enabled	1																															
				Enable or disable interrupt for event COMPARE[i]																															
M	RW	RTCOMPARESYNC																																	
			Disabled	0																															
			Enabled	1																															
				Enable or disable interrupt for event RTCOMPARESYNC																															
N	RW	PWMPERIODEND																																	
			Disabled	0																															
			Enabled	1																															
				Enable or disable interrupt for event PWMPERIODEND																															
O	RW	PWMREADY																																	
			Disabled	0																															
			Enabled	1																															
				Enable or disable interrupt for event PWMREADY																															
P	RW	CLKOUTREADY																																	
			Disabled	0																															
			Enabled	1																															
				Enable or disable interrupt for event CLKOUTREADY																															

8.10.7.22 INTENSET1

Address offset: 0x314

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID					P	O		N		M														L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A-L	RW W1S	COMPARE[i] (i=0..11)																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
				Write '1' to enable interrupt for event COMPARE[i]																															
M	RW W1S	RTCOMPARESYNC																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
				Write '1' to enable interrupt for event RTCOMPARESYNC																															
N	RW W1S	PWMPERIODEND																																	
			Set	1																															
				Write '1' to enable interrupt for event PWMPERIODEND																															