

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				B A																															
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value	Description																														
A	RW	RXREADY W1C			Write '1' to disable interrupt for event RXREADY																														
					New data is available in MAILBOX.RXDATA.																														
			Clear	1	Disable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
B	RW	TXDONE W1C			Write '1' to disable interrupt for event TXDONE																														
					MAILBOX.TXDATA has been read.																														
			Clear	1	Disable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														

9.6.6.1.6 INTPEND

Address offset: 0x30C

Pending interrupts

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				B A																															
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value	Description																														
A	R	RXREADY			Read pending status of interrupt for event RXREADY																														
					New data is available in MAILBOX.RXDATA.																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
B	R	TXDONE			Read pending status of interrupt for event TXDONE																														
					MAILBOX.TXDATA has been read.																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														

9.6.6.1.7 MAILBOX.RXDATA

Address offset: 0x400

Data sent from the debugger to the CPU.

Reading from this register will automatically set field NoDataPending in register RXSTATUS.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	R/W	Field	Value ID	Value				Description																											
A	R	RXDATA						Data received from debugger.																											

9.6.6.1.8 MAILBOX.RXSTATUS

Address offset: 0x404

Status to indicate if data sent from the debugger to the CPU has been read.