Configuration

Instance	Domain	Configuration
MEMCONF : S MEMCONF : NS	GLOBAL	

Register overview

Register	Offset	TZ	Description
POWER[n].CONTROL	0x500		Control memory block power.
POWER[n].RET	0x508		RAM retention for RAM [n].
POWER[n].RET2	0x50C		RAM retention for the second bank in the RAM block

4.2.5.1.1 POWER[n].CONTROL (n=0..1)

Address offset: 0x500 + (n × 0x10)

Control memory block power.

Where n = 0 for memory blocks 0 to 31 and n = 1 for memory blocks 32 to 63.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A-f	RW	MEM[i] (i=0..31)																																	
			Off	0																															
			On	1																															

4.2.5.1.2 POWER[n].RET (n=0..1)

Address offset: 0x508 + (n × 0x10)

RAM retention for RAM [n].

Where n = 0 for RAM blocks 0 to 31 and n = 1 for RAM blocks 32 to 63.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A-f	RW	MEM[i] (i=0..31)																																	
			Off	0																															
			On	1																															

4.2.5.1.3 POWER[n].RET2 (n=0..1)

Address offset: 0x50C + (n × 0x10)

RAM retention for the second bank in the RAM block

Where n = 0 for RAM blocks 0 to 31 and n = 1 for RAM blocks 32 to 63.