Note: Ensure the Result buffer can hold at least one result for each enabled channel by setting RESULT.MAXCNT ≥ 2 × (number of enabled channels). Each sample requires two bytes. Insufficient space leads to undefined behavior.

8.18.7 Reference

The ADC can use different reference voltages VREF, controlled in the REFSEL field of the CH[n].CONFIG register.

These are:

- Internal reference, VREF = 0.9 V
- External reference, VREF provided by the EXTREF pin

Note: The external reference voltage should be close the internal reference voltage. Preferably no more than 5% deviation from the internal reference voltage, VREF. Using a lower reference voltage will lead to increased leakage, and can lead to undefined behaviour.

The SAADC is preceded by a gain stage which has a programmable gain. The voltage range seen at the input of the gain stage is:

```
VRangeDifferential = ± VREF/GAIN
```

```
VRangeSingleEnded = ± 0.5*VREF/GAIN
```

The AIN0-AIN7 inputs cannot exceed VDD, or be lower than VSS. The input ranges are also limited by the REFERENCE and GAIN used. The condition

```
 [V(P) - V(N) ] * GAIN/REFERENCE <= 1
```

must always hold true for valid measurements, otherwise the ADC will saturate and report the max value determined by the RESOLUTION.

8.18.8 Acquisition time

To sample the input voltage, the ADC connects a capacitor to the input.

For illustration, see the following figure. The acquisition time indicates how long the capacitor is connected, see TACQ field in CH[n].CONFIG register. The required acquisition time depends on the source (R_{source}) resistance. For high source resistance the acquisition time should be increased, see Acquisition time on page 561.