6 Event system

The distributed programmable peripheral interconnect (DPPI) system enables peripherals to interact autonomously with each other through tasks and events, without intervention from the CPU.

The DPPI channels are local to each power domain, but can be transferred between power domains using PPI bridges.

The following figure shows the power domains, the PPI controllers (DPPIC), and the PPI bridges (PPIB).

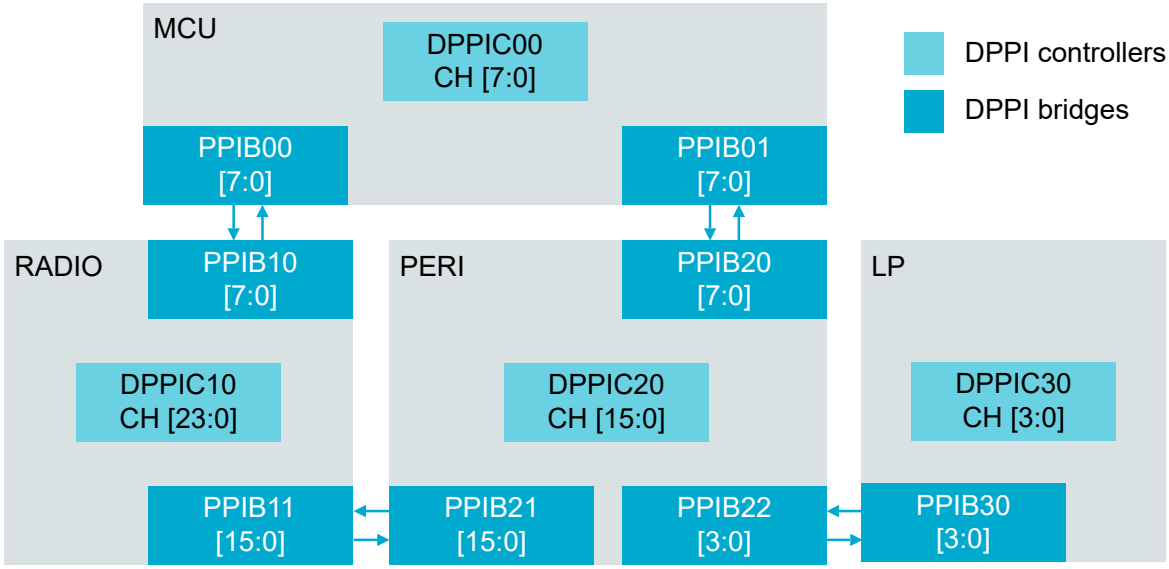

Figure 23: Power domains and PPI bridges

A subset of PPI channels from a power domain can be bridged across to a different power domain. For example, PPIB00 can bridge a set number of configurable DPPI channels to PPIB10. For more details on how to configure the PPI and bridge system, see DPPI — Distributed programmable peripheral interconnect on page 108 and PPIB — PPI Bridge on page 117.

6.1 DPPI latencies

DPPI task and event latency depends on the power domain of the source and destination peripherals.

DPPI signals operate on the HCLKCORE, PCLK32M, and PCLK16M clocks.

Power domain	Clock source
MCU	HCLKCORE (64 or 128 MHz)
RADIO	PCLK32M (32 MHz)
PERI	PCLK16M (16 MHz)
LP	PCLK16M (16 MHz)

Table 23: DPPI clock frequency

For peripherals in the same power domain, there is a two cycle delay from when an event is generated until a task subscribing to the same channel is triggered. Events that are generated while the system