Configures the fail-safe mode

Figure 8-67. FSM_CONFIG Register

7	6	5	4	3	2	1	0
FS_CNTR_ACT				FS_STAT			FSM_DIS
R/W-0000b				RH-000b			R/W-0b

Table 8-23. FSM_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FSM_CNTR_ACT	R/W	0000b	Action if fail safe counter exceeds programmed value 000b = Disabled 0001b = Pull WKRQ/INH low for 1 s 0010b = Perform soft reset 0011b = Perform hard reset - POR 0100b = Stop responding to wake events and go to sleep until power cycle reset 0101b = Reserved 0110b = Reserved 0111b = Reserved 1001b = Turn off VCC for 300 ms and set interrupt **Note** • If LIMP is configured as INH then 0001b will impact cause the LIMP pin to go low for 1 s. • All other values reserved
3-1	FSM_STAT	RH	000b	Reason for entering failsafe mode 000b = Not in FS mode 001b = Thermal shut down event 010b = Reserved 011b = UV_{CC} 100b = OV_{CC} 101b = V_{CCSC} 110b = Watchdog failure 111b = Restart counter exceeded These values are held until cleared by writing 0h to FSM_CNTR_STAT
0	FSM_DIS	R/W	0b	Fail safe mode disable: Excludes power up fail safe 0b = Enabled 1b = Disabled

8.6.14 FSM_CNTR Register (Address = 18h) [reset = 0h]

FSM_CNTR is shown in Figure 8-68 and described in Table 8-24.

Return to Summary Table.

Set fail safe counter and status

Figure 8-68. FSM_CNTR Register

7	6	5	4	3	2	1	0
FSM_CNTR_SET				FSM_CNTR_STAT			
R/W-0h				RH-0h			

Table 8-24. FSM_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FSM_CNTR_SET	R/W	0h	Sets the number of times FS mode enters before action taken. Value is one less than the number of times FS mode is entered. Range is 0-15, representing entering fail-safe mode 1-16 times.