Trace port speed

This register is retained.

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| ID | R/W | Field | Value ID | Value | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | TRACEPORTSPEED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DIV1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DIV2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DIV4 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DIV32 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

# 9.8 ETM — Embedded trace macrocell

The ARM embedded trace macrocell implements instruction, data and event tracing.

This document only provides a register-level description of this ARM component. See the Arm® Embedded Trace Macrocell Architecture Specification for more details

## 9.8.1 Registers

### Instances

| Instance | Domain | Base address | TrustZone | | | Split access | Description |
|---|---|---|---|---|---|---|---|
| | | | Map | Att | DMA | | |
| ETM | APPLICATION | 0xE0041000 | HF | NS | NA | No | Embedded trace macrocell |

### Register overview

| Register | Offset | TZ | Description |
|---|---|---|---|
| TRCPRGCTLR | 0x004 | | Enables the trace unit. |
| TRCPROCSELR | 0x008 | | Controls which PE to trace.<br>Might ignore writes when the trace unit is enabled or not idle.<br>Before writing to this register, ensure that TRCSTATR.IDLE == 1 so that the trace unit can synchronize with the chosen PE.<br>Implemented if TRCIDR3.NUMPROC is greater than zero. |
| TRCSTATR | 0x00C | | Idle status bit |
| TRCCONFIGR | 0x010 | | Controls the tracing options<br>This register must always be programmed as part of trace unit initialization.<br>Might ignore writes when the trace unit is enabled or not idle. |
| TRCEVENTCTL0R | 0x20 | | Controls the tracing of arbitrary events.<br>If the selected event occurs a trace element is generated in the trace stream according to the settings in TRCEVENTCTL1R.DATAEN and TRCEVENTCTL1R.INSTEN. |
| TRCEVENTCTL1R | 0x24 | | Controls the behavior of the events that TRCEVENTCTL0R selects.<br>This register must always be programmed as part of trace unit initialization.<br>Might ignore writes when the trace unit is enabled or not idle. |