8.3.22.10.2 Watchdog in SPI Control Mode

In SPI control, the window has extensive configurability including the ability to select the timeout watchdog. Watchdog is default enabled for standby mode, but can be disabled by setting register 8'h14[0] = 1b. Register 8'h13[7:6] can be set to 00b to disable the WD. There is a WD error counter available in SPI control mode, see Watchdog Error Counter for description of this counter. When a WD error occurs and if the WD error counter reaches programmed count, the device transitions to restart mode and pulls nRST low for t_{NRST_TOG}. Once this time has been met, the device transitions to standby mode and sets nRST pin high. See Figure 8-17 and Figure 8-18 for state diagrams on how the WD behaves.

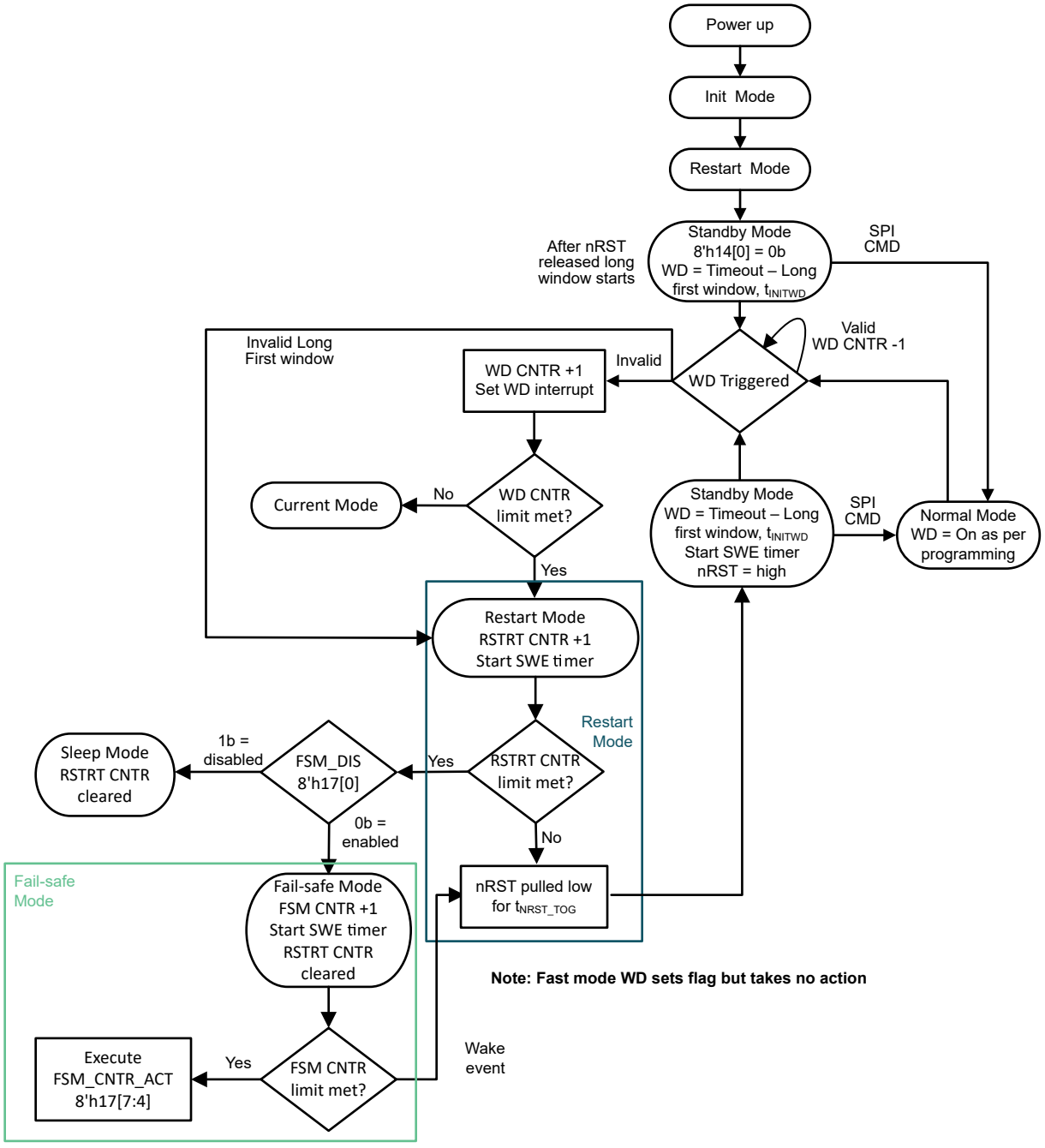

Figure 8-17. Watchdog state diagram in SPI mode; Standby Mode Enabled