8.17.14.171 RTT.SEGMENT67

Address offset: 0x1060

RTT segments 6 and 7

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	DATA			Data Bits 127 - 96

8.18 SAADC — Successive approximation analog-to-digital converter

The SAADC peripheral is a differential successive approximation register (SAR) analog-to-digital converter.

The main features of SAADC are the following:

- Four accuracy modes
  - 10-bit mode with a maximum sample rate of 2 Msps
  - 12-bit mode with a sample rate of 250 ksps
  - 14-bit mode with a sample rate of 31.25 ksps
  - Oversampling mode with configurable sample rate
- 10-bit resolution in single-ended mode, 11-bit resolution in differential mode, and 12/14-bit resolution with oversampling
- Multiple analog inputs
  - GPIO pins with analog function (input range 0 to VDD)
  - VDD (divided down to a valid range using using the programmable gain stage)
- Up to eight input channels
  - One input per single-ended channel, and two inputs per differential channel
  - Scan mode can be configured with both single-ended inputs and differential inputs
  - Each channel can be configured to select any of the above analog inputs
- Sampling triggered by a task from software or a DPPI channel for full flexibility on sample frequency source from low-power 32.768 kHz RTC or more accurate 1/16 MHz timers
- One-shot conversion mode to sample a single channel
- Scan mode to sample a series of channels in sequence with configurable sample delay
- Support for direct sample transfer to RAM using EasyDMA
- Interrupts on single sample and full buffer events
- Samples stored as 16-bit two's complement values for differential and single-ended sampling
- Continuous sampling without the need of an external timer
- On-the-fly limit checking

8.18.1 Shared resources

The ADC can coexist with COMP and other peripherals using one of AIN0-AIN7 , provided these are assigned to different pins.

It is not recommended to select the same analog input pin for both modules.