

The register fields READ, WRITE and EXECUTE can be written to 0, even when the LOCK field is set to Enabled.

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				H	H	H	H	H	G	F	E	E	E	D	C	B	A																	
Reset 0x00000000			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
ID R/W Field			Value ID	Value		Description																												
A RW READ						Read access																												
				NotAllowed		Read access to override region [n] is not allowed																												
				Allowed		Read access to override region [n] is allowed																												
B RW WRITE						Write access																												
				NotAllowed		Write access to override region [n] is not allowed																												
				Allowed		Write access to override region [n] is allowed																												
C RW EXECUTE						Execute access																												
				NotAllowed		Execute access to override region [n] is not allowed																												
				Allowed		Execute access to override region [n] is allowed																												
D RW SECURE						Secure access																												
				NonSecure		Both Secure and non-Secure access to override region [n] is allowed																												
				Secure		Only secure access to override region [n] is allowed																												
E RW OWNER						Owner ID																												
				NotEnforced		Owner ID protection is not enforced																												
F RW WRITEONCE						Write-once																												
				Disabled		Write-once disabled																												
				Enabled		Write-once enabled																												
G RW LOCK						Enable lock																												
				W1S																														
				Disabled		Lock disabled for region [n]																												
				Enabled		Lock enabled for region [n]																												
H RW SIZE						Size in KBytes of region [n]																												

4.2.7 SICR — Secure information configuration region

The secure information configuration region (SICR) is reserved for keys and device unique seed.

Access to SICR is managed by [KMU — Key management unit](#) on page 165. Bus transactions originating from CPU or other peripherals are blocked.

4.2.8 SWI — Software interrupts

A set of interrupts have been reserved for use as software interrupts.

These interrupts can be enabled and triggered by software by using the Arm Cortex-M33 NVIC registers, as described in the [Arm Cortex-M33 Processor Technical Reference Manual](#).

4.2.8.1 Registers

Instances

Instance	Domain	Base address	TrustZone			Split access	Description
			Map	Att	DMA		
SWI00	APPLICATION	0x5001C000	HF	S	NA	No	Software interrupt SWI00
SWI01	APPLICATION	0x5001D000	HF	S	NA	No	Software interrupt SWI01
SWI02	APPLICATION	0x5001E000	HF	S	NA	No	Software interrupt SWI02
SWI03	APPLICATION	0x5001F000	HF	S	NA	No	Software interrupt SWI03