

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0				
ID	A A A				
Reset 0x00000002	0 1 0				
ID	R/W	Field	Value ID	Value	Description
A	RW	RXDELAY	[7..0]		Sample delay for input serial data on SDI. The value specifies the number of SPIM core clock cycles delay from the sampling edge of SCK (leading edge for CONFIG.CPHA = 0, trailing edge for CONFIG.CPHA = 1) until the input serial data is sampled. As an example, if RXDELAY = 0 and CONFIG.CPHA = 0, the input serial data is sampled on the rising edge of SCK.

8.19.8.26 IFTIMING.CSNDUR

Address offset: 0x5B0

Minimum duration between edge of CSN and edge of SCK. When SHORTS.END_START is used, this is also the minimum duration CSN must stay high between transactions.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																										A	A	A	A	A	A	A
Reset 0x00000002																															0	1
ID	R/W	Field	Value ID	Value	Description																											
A	RW	CSNDUR	[0xFF..0]		Minimum duration between edge of CSN and edge of SCK. When SHORTS.END_START is used, this is the minimum duration CSN must stay high between transactions. The value is specified in number of SPIIM core clock cycles.																											
					Note that for low values of CSNDUR, the system turnaround time will dominate the actual time between transactions.																											

8.19.8.27 DCXCNT

Address offset: 0x5B4

DCX configuration

8.19.8.28 CSNPOL

Address offset: 0x5B8

Polarity of CSN output