8 Detailed Description

8.1 Overview

The TLIN1431x-Q1 LIN transceiver is a Local Interconnect Network (LIN) physical layer transceiver, compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987–4:2016, and SAE J2602:2021 with integrated wake-up and protection features. The LIN bus is a single-wire, bi-directional bus that typically is used in low speed in-vehicle networks with data rates that range up to 20 kbps. The device LIN receiver works up to 100 kbps supporting in-line programming in normal mode. When the device is placed into fast mode, both the transmitter and receiver support up to 200 kbps. The device converts the LIN protocol data stream on the TXD input into a LIN bus signal using a current-limited wave-shaping driver which reduces electromagnetic emissions (EME). The receiver converts the data stream to logic level signals that are sent to the microprocessor through the RXD pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor (45 kΩ) and a series diode.

Ultra-low current consumption is possible using the sleep mode. The TLIN1431x-Q1 provides three methods to wake up from sleep mode: EN pin, WAKE pin and LIN bus in pin control mode and two in SPI control mode, WAKE pin and LIN bus. The device integrates a low dropout voltage regulator with a wide input from V_{SUP} providing 5 V ±2.5% or 3.3 V ±2.5% with up to 125 mA of current depending upon system implementation.

The TLIN1431x-Q1 integrates a window-based watchdog supervisor which has a programmable delay and window ratio determined by pin strapping or SPI communication. The device watchdog is controlled by pin configuration or SPI depending upon the state of pin 7 at power up. During power up, if pin 7 is externally pulled to ground, the device is configured for pin control and all digital IO voltage levels will be dependent upon V_{CC}. If pin 7 is left floating or pulled up to V_{CC} the device is controlled by SPI communication and the pin becomes the nCS pin. For the 5 V V_{CC} version, the digital IO voltage levels are also determined during power up when the device is configured for SPI communication control. If pin 7 is left floating at power up, the internal pull up configures the device for 3.3 V SPI control. This means that all the digital IO for the device will be configured for 3.3 V electrical levels. If the processor needs 5 V IO, a 500 kΩ pull up resistor to the TLIN14315-Q1 V_{CC} pin will configure all digital IOs 5 V electrical levels. This allows the 5 V version of the device to work with both 3.3 V processors or 5 V processors. SPI communication is used for device configuration. This sets not only the SPI pins but also WKRQ, nRST, FSO, nINT, TXD and RXD pins. In pin configuration, nRST is asserted high when V_{CC} increases above UV_{CC} and stays high as long as V_{CC} is above this threshold and the device is not in restart mode.

When the watchdog is controlled by the device pins, the state of the WDT pin determines the window time. WDI is used as the watchdog input trigger which is expected in the open window. If a watchdog error event takes place, the nWDR pin goes low to reset the processors. When using SPI writing FFh to register 15h, WD_INPUT_TRIG, during the open window restarts the watchdog timer. The supervised processor must trigger the WDI pin or WD_INPUT_TRIG register within the defined window. When using SPI, the nRST pin can become the watchdog event output trigger for the processor if programmed this way, but the nRST function is lost. The watchdog timer has a long initial window when entering standby, normal and fast modes that a watchdog input trigger is expected.