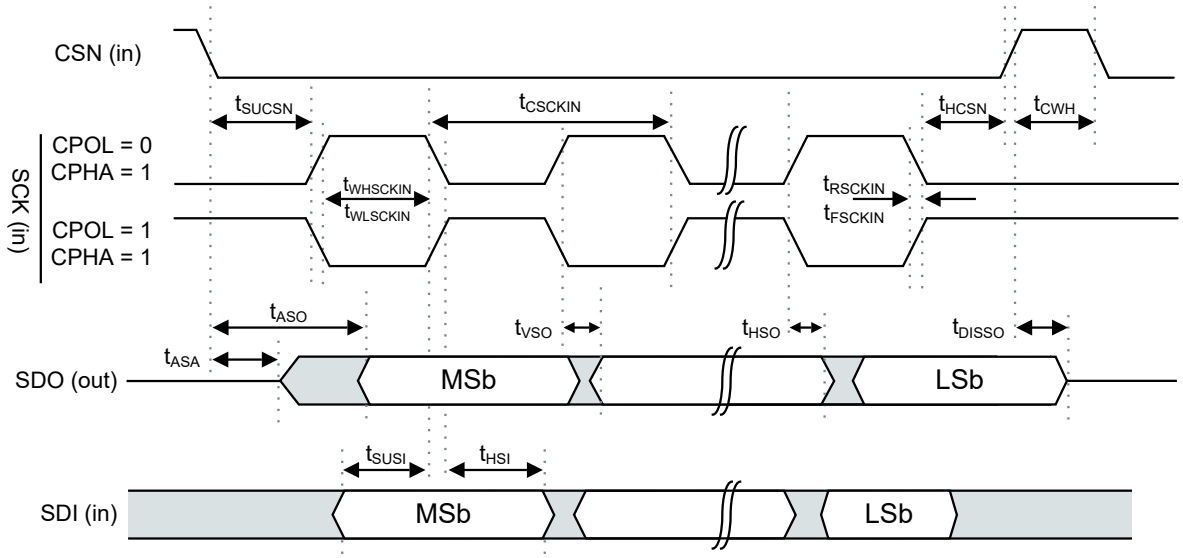

Figure 197: SPIS timing diagram, CPHA = 1

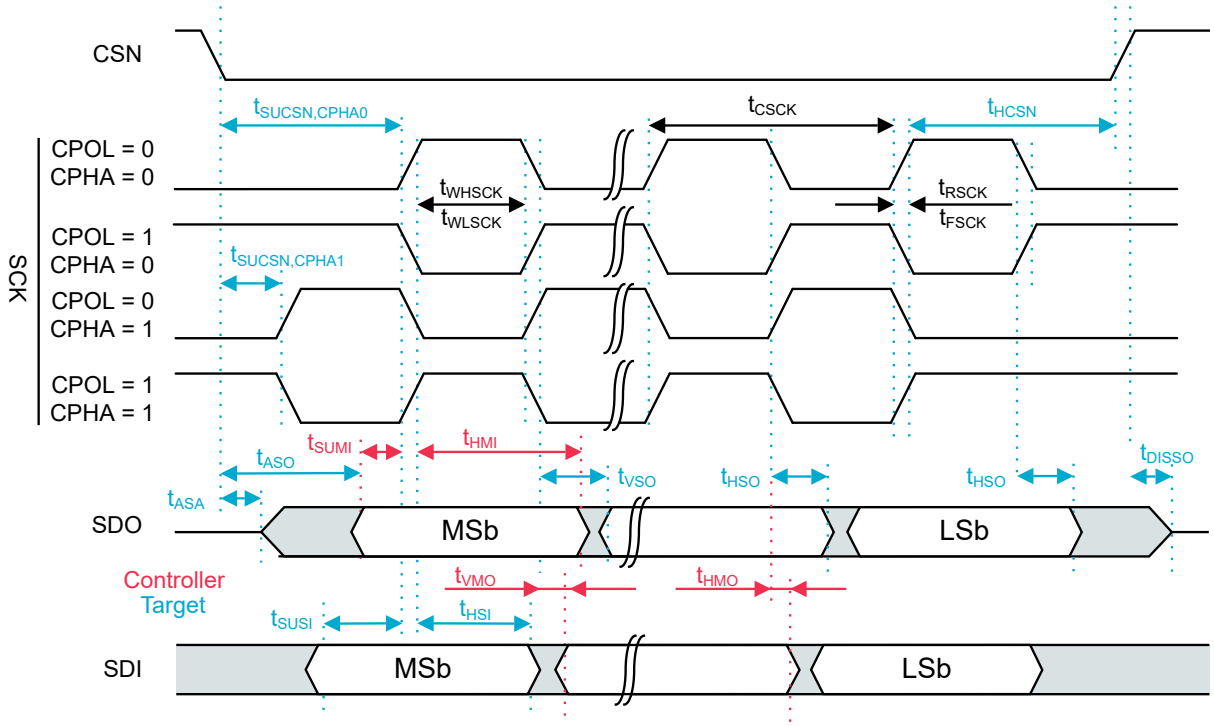

Figure 198: Common SPIM and SPIS timing diagram

11.19.3 Timing specifications for GPIO port P0 using Standard drive strength

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SPIS,VSO}$	CLK edge to SDO valid			59	ns
$t_{SPIS,HSO}$	SDO hold time after CLK edge	6			ns
$t_{SPIS,SUSI}$	SDI to CLK edge setup time	33			ns
$t_{SPIS,HSI}$	CLK edge to SDI hold time	1			ns