

### 8.15.5.32 DECODER

Address offset: 0x510

Configuration of the decoder

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																
ID																												B				A				A
Reset 0x00000000				0 0																																
ID	R/W	Field	Value ID	Value	Description																															
A	RW	LOAD			How a sequence is read from RAM and spread to the compare register																															
			Common	0	1st half word (16-bit) used in all PWM channels 0..3																															
			Grouped	1	1st half word (16-bit) used in channel 0..1; 2nd word in channel 2..3																															
			Individual	2	1st half word (16-bit) in ch.0; 2nd in ch.1; ...; 4th in ch.3																															
			WaveForm	3	1st half word (16-bit) in ch.0; 2nd in ch.1; ...; 4th in COUNTERTOP																															
B	RW	MODE			Selects source for advancing the active sequence																															
			RefreshCount	0	SEQ[n].REFRESH is used to determine loading internal compare registers																															
			NextStep	1	NEXTSTEP task causes a new value to be loaded to internal compare registers																															

### 8.15.5.33 LOOP

Address offset: 0x514

Number of playbacks of a loop

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				A A																															

### 8.15.5.34 IDLEOUT

Address offset: 0x518

Configure the output value on the PWM channel during idle

Writes to this register are ignored when the PWM is enabled.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																			
ID																																				D C B A			
Reset 0x00000000				0 0																																			
ID	R/W	Field	Value ID	Value				Description																															
A-D	RW	VAL[i] (i=0..3)		Idle output value for PWM channel [i]																																			

### 8.15.5.35 SEQ[n].REFRESH (n=0..1)

Address offset: 0x528 + (n × 0x20)

Number of additional PWM periods between samples loaded into compare register