

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
ID	R/W	Field	Value ID	Value	Description																											
A	RW	VAL	0.65535	value																												

8.18.11.29 ENABLE

Address offset: 0x500

Enable or disable ADC

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
ID	R/W	Field	Value ID	Value	Description																											
A	RW	ENABLE			Enable or disable ADC																											
			Disabled	0	Disable ADC																											
			Enabled	1	Enable ADC																											
					When enabled, the ADC will acquire access to the GPIO pins specified in the CH[n].PSEL and CH[n].PSELN registers.																											

8.18.11.30 CH[n].PSEL (n=0..7)

Address offset: 0x510 + (n × 0x10)

Input positive pin selection for CH[n]

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	D	D																	C	C	B	B	B	B	A	A	A	A	A	A		
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
ID	R/W	Field	Value ID	Value	Description																											
A	RW	PIN			GPIO pin selection.																											
B	RW	PORT			GPIO port selection																											
C	RW	INTERNAL			Internal input selection for analog positive input when CH[n].PSEL.PIN = Internal																											
			Avdd	0	Connected to the internal 0.9V analog supply rail																											
			Dvdd	1	Connected to the internal 0.9V digital supply rail																											
			Vdd	2	Connected to VDD																											
D	RW	CONNECT			Connection																											
			NC	0	Not connected																											
			AnalogInput	1	Select analog input																											
					The analog input is connected based on CH[n].PSEL.PIN and CH[n].PSEL.PORT																											
				Internal	2	Selects internal inputs.																										
					The analog input is connected based on CH[n].PSEL.INTERNAL																											

8.18.11.31 CH[n].PSELN (n=0..7)

Address offset: 0x514 + (n × 0x10)

Input negative pin selection for CH[n]