Interrupt Clear

Writing a 1 to a bit in this register disables the corresponding interrupt. Writing 0 has no effect.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																														F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	FETCHERBLOCKEND																																	
				Fetcher DMA reached the end of a block (if enabled in the descriptor; scatter-gather only)																																	
B	RW	FETCHERSTOPPED																																	
				Fetcher DMA reached the end of a block with Stop=1, or end of direct transfer																																	
C	RW	FETCHERERROR																																	
				Bus error during fetcher DMA access																																	
D	RW	PUSHERBLOCKEND																																	
				Pusher DMA reached the end of a block (if enabled in the descriptor; scatter-gather only)																																	
E	RW	PUSHERSTOPPED																																	
				Pusher DMA reached the end of a block with Stop=1, or end of direct transfer																																	
F	RW	PUSHERERROR																																	
				Bus error during pusher DMA access																																	

7.8.1.7.11 CRYPTMSTRDMA.INTSTATRAW

Address offset: 0x028

Interrupt Status Raw

Interrupt status before bitmasking with INTEN.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																														F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	FETCHERBLOCKEND																																	
				Fetcher DMA reached the end of a block (if enabled in the descriptor; scatter-gather only)																																	
B	RW	FETCHERSTOPPED																																	
				Fetcher DMA reached the end of a block with Stop=1, or end of direct transfer																																	
C	RW	FETCHERERROR																																	
				Bus error during fetcher DMA access																																	
D	RW	PUSHERBLOCKEND																																	
				Pusher DMA reached the end of a block (if enabled in the descriptor; scatter-gather only)																																	
E	RW	PUSHERSTOPPED																																	
				Pusher DMA reached the end of a block with Stop=1, or end of direct transfer																																	
F	RW	PUSHERERROR																																	
				Bus error during pusher DMA access																																	

7.8.1.7.12 CRYPTMSTRDMA.INTSTAT

Address offset: 0x02C

Interrupt Status

Interrupt Status after bitmasking with INTEN. If any bit of this register is high, this sub-module interrupt line towards the CRACEN interrupt generation logic is high.