

Profiling counter	Description
HIT	Incremented on a cache hit
MISS	Incremented on a cache miss (not counting write misses)
LMISS	Incremented when accessing different line than was accessed last time
READS	Incremented on a CPU read
WRITES	Incremented on a CPU write

Table 15: Profiling counters

#### 4.2.3.3 Debug

The CPU is able to read internal cache memories and tags for debug purposes.

The content of data and tag RAM's are accessible through registers **SET[n].WAY[o].INFO** ( $n=0..127$ ) ( $o=0..1$ ) on page 36 and **SET[n].WAY[o].DU[p].DATA[q]** ( $n=0..127$ ) ( $o=0..1$ ) ( $p=0..3$ ) ( $q=0..1$ ) on page 37.

Debug access is prevented by using register **DEBUGLOCK** on page 35.

#### 4.2.3.4 Registers

##### Instances

Instance	Domain	Base address	TrustZone			Split access	Description
			Map	Att	DMA		
ICACHE	APPLICATION	0xE0082000	HF	S	NA	No	Instruction cache

##### Configuration

Instance	Domain	Configuration
ICACHE	APPLICATION	Cache size: 8 KB. Sets: 128. Data unit: 64 bits. Line width = 4 data units.
		Supports line invalidation
		Supports cache erase
		Supports cache line maintain
		Supports extended profiling registers (LMISS / READS / WRITES)
		Supports debug lock
		Supports write lock
		Data bus width : 0..63

##### Register overview

Register	Offset	TZ	Description
TASKS_INVALIDATECACHE	0x008		Invalidate the cache.
TASKS_INVALIDATELINE	0x014		Invalidate the line.
TASKS_ERASE	0x020		Erase the cache.
STATUS	0x400		Status of the cache activities.
ENABLE	0x404		Enable cache.
LINEADDR	0x410		Memory address covered by the line to be maintained.
PROFILING.ENABLE	0x414		Enable the profiling counters.