Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	END_ACQUIRE			Shortcut between event END and task ACQUIRE
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
B-E	RW	DMA_RX_MATCH[i]_DMA_RX_ENABLEMA +1)%4] (i=0..3)			Shortcut between event DMA.RX.MATCH[n] and task DMA.RX.ENABLEMATCH[(i+1)%4] Allows daisy-chaining match events.
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
F-I	RW	DMA_RX_MATCH[i]_DMA_RX_DISABLEMATCH[i] (i=0..3)			Shortcut between event DMA.RX.MATCH[n] and task DMA.RX.DISABLEMATCH[n]
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut

8.20.7.14 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				L K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW W1S	END			Write '1' to enable interrupt for event END
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
B	RW W1S	ACQUIRED			Write '1' to enable interrupt for event ACQUIRED
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
C	RW W1S	DMARXEND			Write '1' to enable interrupt for event DMARXEND
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW W1S	DMARXREADY			Write '1' to enable interrupt for event DMARXREADY
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
E	RW W1S	DMARXBUSERROR			Write '1' to enable interrupt for event DMARXBUSERROR When this event is generated, the address which caused the error can be read from the BUSERRORADDRESS register.
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled