

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				B																								A A A A A A A A							
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value				Description																											
A	RW	CHIDX		[0..255]				DPPI channel that event READY will publish to																											
B	RW	EN																																	
			Disabled	0				Disable publishing																											
			Enabled	1				Enable publishing																											

8.23.10.20.1.3 PUBLISH_DMA.RX.BUSERROR

Address offset: 0x1D4

Publish configuration for event **BUSERROR**

When this event is generated, the address which caused the error can be read from the **BUSERRORADDRESS** register.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				B																								A A A A A A A A							
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value		Description																													
A	RW	CHIDX		[0..255]		DPPI channel that event BUSERROR will publish to																													
B	RW	EN																																	
			Disabled	0		Disable publishing																													
			Enabled	1		Enable publishing																													

8.23.10.20.1.4 PUBLISH_DMA.RX.MATCH[n] (n=0..3)

Address offset: 0x1D8 + (n × 0x4)

Publish configuration for event **MATCH[n]**

Bit number					31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID					B																								A A A A A A A A							
Reset 0x00000000					0 0																															
ID	R/W	Field	Value ID	Value	Description																															
A	RW	CHIDX		[0..255]	DPPI channel that event MATCH[n] will publish to																															
B	RW	EN																																		
			Disabled	0	Disable publishing																															
			Enabled	1	Enable publishing																															

8.23.10.20.2 PUBLISH_DMA.TX

Publish configuration for events

8.23.10.20.2.1 PUBLISH_DMA.TX.END

Address offset: 0x1E8

Publish configuration for event **END**