

8.6 Registers

The following tables contain the registers that the device use during SPI communication.

[Table 8-9](#) lists the memory-mapped registers for the Device registers. All register offset addresses not listed in [Table 8-9](#) should be considered as reserved locations and the register contents should not be modified.

Table 8-9. Device Registers

Address	Acronym	Register Name	Section
0h + formula	DEVICE_ID_y	Device Part Number	Go
8h	REV_ID_MAJOR	Major Revision	Go
9h	REV_ID_MINOR	Minor Revision	Go
Ah	CRC_CNTL	SPI CRC control	Go
Bh	CRC_POLY_SET	Sets SPI CRC polynomial	Go
Fh	Scratch_Pad_SPI	Read and Write Test Register SPI	Go
11h	WAKE_PIN_CONFIG1	WAKE pin configuration 1	Go
12h	WAKE_PIN_CONFIG2	WAKE pin configuration 2	Go
13h	WD_CONFIG_1	Watchdog configuration 1	Go
14h	WD_CONFIG_2	Watchdog configuration 2	Go
15h	WD_INPUT_TRIG	Watchdog input trigger	Go
16h	WD_RST_PULSE	Watchdog output pulse width	Go
17h	FSM_CONFIG	Fail safe mode configuration	Go
18h	FSM_CNTR	Fail safe mode counter	Go
19h	DEVICE_RST	Device reset	Go
1Ah	DEVICE_CONFIG1	Device configuration 1	Go
1Bh	DEVICE_CONFIG2	Device configuration 2	Go
1Ch	SWE_TIMER	Sleep wake error timer configuration	Go
1Dh	LIN_CNTL	LIN transceiver control	Go
1Eh	HSS_CNTL	High side switch 1 and 2 control	Go
1Fh	PWM1_CNTL1	Pulse width modulation frequency select	Go
20h	PWM1_CNTL2	Pulse width modulation duty cycle two MSB select	Go
21h	PWM1_CNTL3	Pulse width modulation duty cycle eight LSB select	Go
22h	PWM2_CNTL1	Pulse width modulation frequency select	Go
23h	PWM2_CNTL2	Pulse width modulation duty cycle two MSB select	Go
24h	PWM2_CNTL3	Pulse width modulation duty cycle eight LSB select	Go
25h	TIMER1_CONFIG	High side switch timer 1 configuration	Go
26h	TIMER2_CONFIG	High side switch timer 2 configuration	Go
28h	RSRT_CNTR	Restart counter configuration	Go
29h	nRST_CNTL	nRST and FSO pin control	Go
50h	INT_GLOBAL	Global Interrupts	Go
51h	INT_1	Interrupts	Go
52h	INT_2	Interrupts	Go
53h	INT_3	Interrupts	Go
56h	INT_EN_1	Interrupt enable for INT_1	Go
57h	INT_EN_2	Interrupt enable for INT_2	Go
58h	INT_EN_3	Interrupt enable for INT_3	Go
5Ah	INT_4	Interrupts	Go
5Eh	INT_EN_4	Interrupt enable for INT_4	Go