When configured for SPI control, the WDT/CLK pin becomes the SPI input clock, CLK. When configured as the CLK pin there is a 240 kΩ pull-up to V_{INT} enabled.

8.3.6 WDI or SDI (Watchdog Timer Input or SPI Serial Data In)

When configured for pin control, the WDI or SDI pin becomes the watchdog timer input trigger, WDI. This resets the timer with either a positive or negative transition from the processor. A filter time of t_W is used to avoid false triggers.

When configured for SPI control, the WDI/SDI pin becomes the SPI serial data input pin, SDI.

8.3.7 PIN or nCS (Pin Watchdog Select or SPI Chip Select)

This pin determines if the TLIN1431x-Q1 watchdog and mode changes are controlled by pin or SPI. At power up, the device monitors this pin and determine which method is to be used. When tied to GND, the device is pin programmable, see Figure 8-5. When connected to a high-Z processor IO pin or pulled up, the device is set up to support SPI, see Figure 8-6. In SPI control mode, if the LDO is being used to power up circuitry other than the processor a mismatch can take place. An example of this is using the TLIN14315-Q1 V_{CC} to power up a 5 V sensor and the processor supports 3.3 V IO electrical levels. This is accomplished by letting the PIN/nCS pin float at power up which configures the internal IO electrical levels to V_{INT} which is 3.3 V. For the IO to be 5 V, an external 500 kΩ resistor needs to be pulled up to the 5 V V_{CC} pin. This makes the IO 5 V. See Figure 8-4 to understand the three ways this pin can be connected for the 5 V LDO device.

Note

The behavior of the microprocessor used must be understood if connecting to this pin to control whether the device is to be pin controlled or SPI controlled. There is an internal pull-up that sets the device in SPI control mode. If the processor pin drives low during power up, the device is in pin control mode. To specify pin control mode place and external pull-down resister to ground.

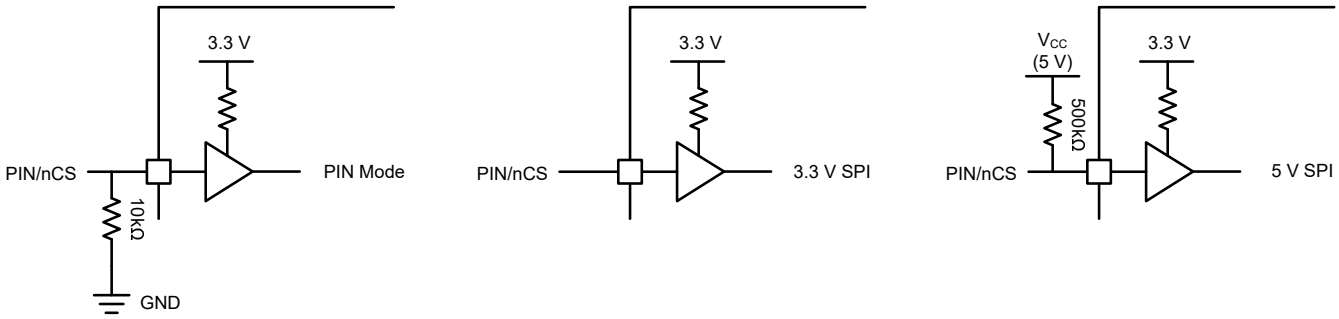

Figure 8-4. PIN/nCS configuration