Bit number					31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
ID					B		A A A A A A A A
Reset 0x00000000					0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
ID	R/W	Field	Value ID		Value	Description	
A	RW	CHIDX			[0..255]	DPPI channel that event END will publish to	
B	RW	EN					
			Disabled		0	Disable publishing	
			Enabled		1	Enable publishing	

8.20.7.11 PUBLISH_ACQUIRED

Address offset: 0x198

Publish configuration for event ACQUIRED

Bit number					31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
ID					B		A A A A A A A A
Reset 0x00000000					0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
ID	R/W	Field	Value ID		Value	Description	
A	RW	CHIDX			[0..255]	DPPI channel that event ACQUIRED will publish to	
B	RW	EN					
			Disabled		0	Disable publishing	
			Enabled		1	Enable publishing	

8.20.7.12 PUBLISH_DMA

Publish configuration for events

8.20.7.12.1 PUBLISH_DMA.RX

Publish configuration for events

8.20.7.12.1.1 PUBLISH_DMA.RX.END

Address offset: 0x1CC

Publish configuration for event END

Bit number					31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
ID					B		A A A A A A A A
Reset 0x00000000					0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
ID	R/W	Field	Value ID		Value	Description	
A	RW	CHIDX			[0..255]	DPPI channel that event END will publish to	
B	RW	EN					
			Disabled		0	Disable publishing	
			Enabled		1	Enable publishing	

8.20.7.12.1.2 PUBLISH_DMA.RX.READY

Address offset: 0x1D0

Publish configuration for event READY

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