| Bit number | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
| --- | --- |
| ID | P O N M L K J I H G F E D C B A |
| Reset 0x00000000 | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |

| ID | R/W | Field | Value ID | Value | Description |
| --- | --- | --- | --- | --- | --- |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| O | RW | PWMREADY | | | Enable or disable interrupt for event PWMREADY |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| P | RW | CLKOUTREADY | | | Enable or disable interrupt for event CLKOUTREADY |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |

## 8.10.7.18 INTENSET0

Address offset: 0x304

Enable interrupt

| Bit number | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
| --- | --- |
| ID | P O N M L K J I H G F E D C B A |
| Reset 0x00000000 | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |

| ID | R/W | Field | Value ID | Value | Description |
| --- | --- | --- | --- | --- | --- |
| A-L | RW W1S | COMPARE[i] (i=0..11) | | | Write '1' to enable interrupt for event COMPARE[i] |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| M | RW W1S | RTCOMPARESYNC | | | Write '1' to enable interrupt for event RTCOMPARESYNC |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| N | RW W1S | PWMPERIODEND | | | Write '1' to enable interrupt for event PWMPERIODEND |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| O | RW W1S | PWMREADY | | | Write '1' to enable interrupt for event PWMREADY |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| P | RW W1S | CLKOUTREADY | | | Write '1' to enable interrupt for event CLKOUTREADY |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

## 8.10.7.19 INTENCLR0

Address offset: 0x308

Disable interrupt

NORDIC
SEMICONDUCTOR