4 Application core

4.1 Arm Cortex-M33 CPU

4.1.1 CPU

The Arm Cortex-M33 processor has a 32-bit instruction set (Thumb®-2 technology) that implements a super set of 16- and 32-bit instructions to maximize code density and performance.

This processor has the following features that enable energy-efficient arithmetic and high-performance signal processing:

- Digital signal processing (DSP) instructions:
  - Single-cycle multiply and accumulate (MAC) instructions
  - 8- and 16-bit single instruction multiple data (SIMD) instructions
- Hardware divide
- Single-precision floating-point unit (FPU)
- Memory Protection Unit (MPU)
- Arm TrustZone for Armv8-M
- Stack limit checking

The Arm Cortex Microcontroller Software Interface Standard (CMSIS) is implemented and available for the processor.

Real-time execution is highly deterministic in Thread mode, to and from sleep modes, and when handling events at configurable priority levels via the Nested Vectored Interrupt Controller (NVIC).

Instruction cache on the C-bus (code bus) of the Cortex-M33 CPU improves performance when fetching instructions (or data) from internal non-volatile memory. For more information on cache, see CACHE — Instruction/data cache on page 29. CPU performance parameters including wait states for configurations, CPU current consumption and efficiency, and processing power and efficiency based on the CoreMark benchmark can be found in CPU Electrical specification on page 898.

4.1.1.1 Floating point interrupt

The floating point unit (FPU) may generate exceptions, for example, due to overflow or underflow. These exceptions may trigger interrupts when enabled in the FPU peripheral. For information on the FPU interrupts, see CPUC — CPU control on page 20.

4.1.1.2 CPU and support module configuration

The Arm Cortex-M33 processor has a number of CPU options and support modules implemented on the device.

Option	Description	Implemented
WIC	Wakeup Interrupt Controller	No
Endianness	Memory system endianness	Little endian
DWT	Data Watchpoint and Trace	Yes

Table 12: Core options