- Avoid situations where more than one bus Manager is accessing the same RAM Subordinate.
- If more than one bus Manager is accessing the same Subordinate, make sure that the bus bandwidth is not exhausted.

4.2.1.2 AMBIX0 override configuration

The main interconnect (AMBIX0) has a configurable bus matrix.

The overrides are used to configure the secure and non-secure memory regions in the device. They are also used to prevent or grant access to read, write, or execute from the memory region. For more details, see MPC — Memory Privilege Controller on page 174.

4.2.2 EasyDMA

EasyDMA is a module implemented by some peripherals as a bus manager for direct access to RAM. It cannot access non-volatile memory,

A peripheral can implement multiple EasyDMA instances to provide dedicated channels. For example, a channel can be dedicated for reading and writing data between the peripheral and RAM. This concept is illustrated in the following example figure, where READER is reading data from RAMc, while WRITER is writing data to RAMa and RAMb (each RAM being separate bus subordinates).

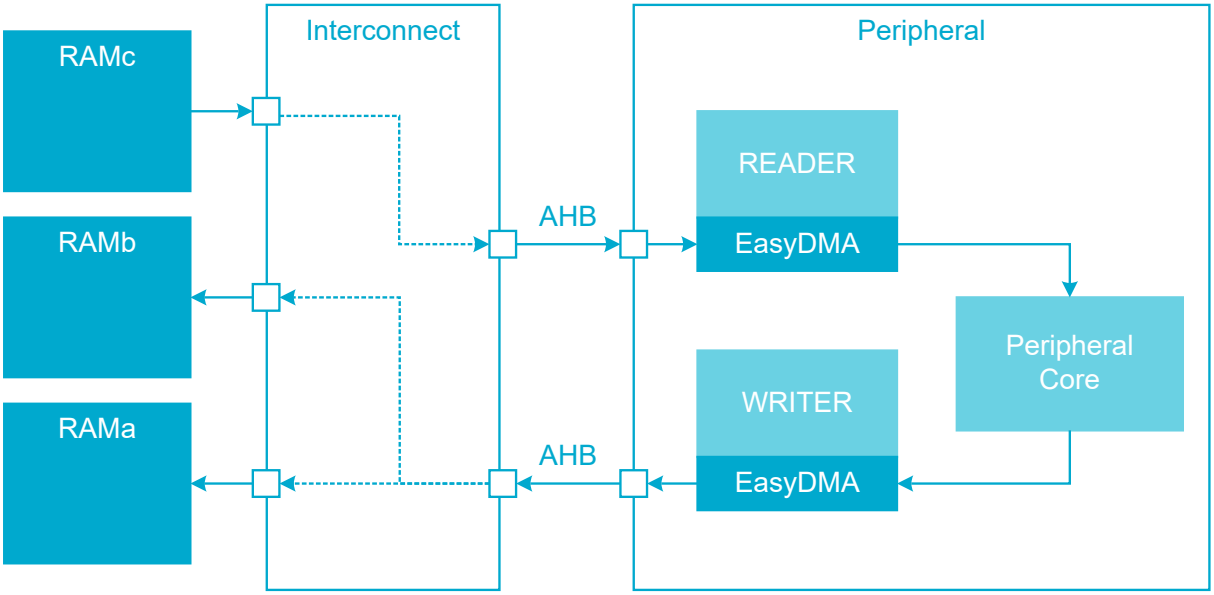

Figure 5: EasyDMA example

4.2.2.1 EasyDMA channel implementation