

4.2.2.3 Array list

EasyDMA can operate in Array List mode.

The Array List mode is implemented in channels where the LIST register is available.

The array list is not able to specify where the next item in the list is located. Instead, it assumes that the list is organized as a linear array where items are located one after the other in RAM.

The EasyDMA array list is implemented with the data structure `ArrayList_type`. This is illustrated in the following code example using a `READER` EasyDMA channel as an example.

```
#define BUFFER_SIZE 4

typedef struct ArrayList
{
    uint8_t buffer[BUFFER_SIZE];
} ArrayList_type;

ArrayList_type ReaderList[3] __at__ 0x20000000;

MYPERIPHERAL->READER.MAXCNT = BUFFER_SIZE;
MYPERIPHERAL->READER.PTR = &ReaderList;
MYPERIPHERAL->READER.LIST = MYPERIPHERAL_READER_LIST_ArrayList;
```

The data structure includes a buffer that is equal in size to the `READER.MAXCNT` register. EasyDMA uses the `READER.MAXCNT` register to determine when the buffer is full.

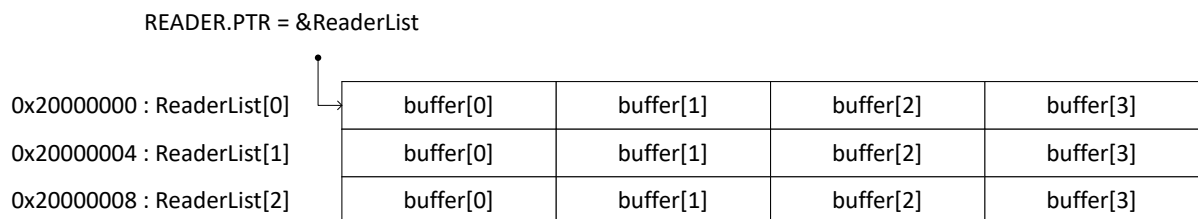


Figure 7: EasyDMA array list

4.2.3 CACHE — Instruction/data cache

The cache is two-way set associative with a least recently used (LRU) replacement policy. Both instruction and data accesses towards NVM memory are cached.

The cache has the following features:

- 4x64-bit cache line
- Ability to enable/disable cache at run-time
- Writes to cached memory are write-around and invalidate the cache line
- Manual invalidation and erase support
- Locking cache updates on cache misses
- Performance hit/miss counter registers for profiling CACHE operations
- Optional readable cache content for profiling
 - Data, tag, valid, and most recently used (MRU) bits
 - Can be disabled when not in use

The cache must be enabled by the `ENABLE` register.