These registers and their configurations are only used when TWIM is enabled, and retained while the device is in System ON mode. When the peripheral is disabled, the pins behave as regular GPIOs and are configured according to their respective OUT bit field and PIN_CNF[n] register. Configure registers PSEL.SCL and PSEL.SDA when TWIM is disabled.

Only one peripheral can be assigned to drive a GPIO pin at a time. If more than one peripheral is assigned to a GPIO pin, it could result in unpredictable behavior.

When TWIM is in System OFF mode or disabled, the pins using TWIM must be configured by the GPIO peripheral according to the following table to ensure correct pin behavior.

TWIM signal	TWIM pin	Drive strength	Direction	Output value
SCL	As specified in PSEL.SCL	S0D1	Input	Not applicable
SDA	As specified in PSEL.SDA	S0D1	Input	Not applicable

Table 65: GPIO configuration before enabling peripheral

8.23.9 Pull-up resistor

1000 kbps bit rate is supported when using H0D1 drive strength, 1 kΩ pull-up resistor, and maximum 50 pF bus capacitance. For other bit rates, see the following figure.

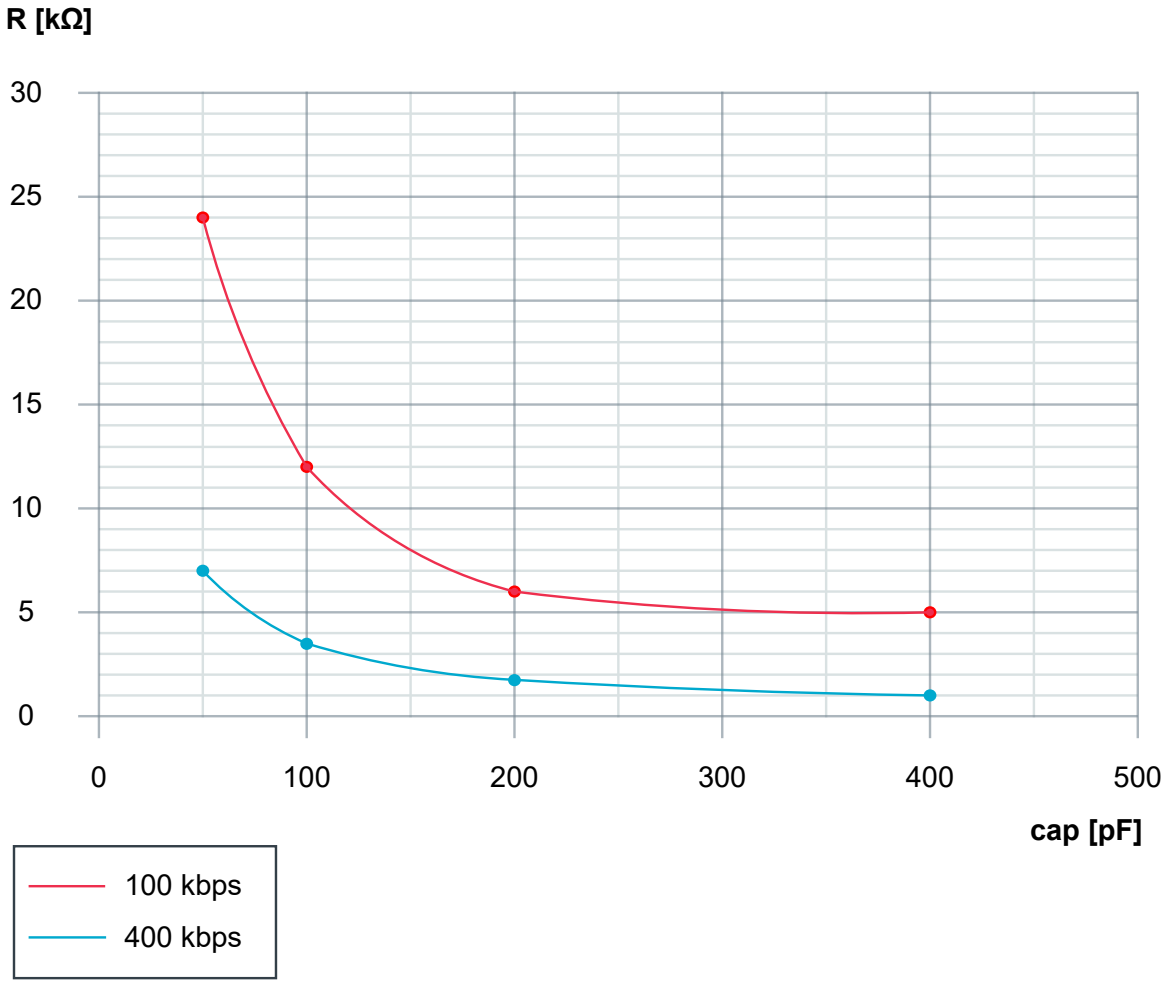

Figure 150: Recommended TWIM pull-up value vs. line capacitance