11.19 SPIS Electrical specification

11.19.1 SPIS slave interface electrical specifications

Symbol	Description	Min.	Typ.	Max.	Units
f_{SPIS}	Bit rates for SPIS[12]			8[13]	Mbps
$t_{SPIS,START}$	Time from RELEASE task to receive/transmit (CSN active)		1		µs

11.19.2 Serial Peripheral Interface Slave (SPIS) timing specifications

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SPIS,CSCKIN}$	SCK input period	125			ns
$t_{SPIS,RFSCKIN}$	SCK input rise/fall time			30	ns
$t_{SPIS,WHSCKIN}$	SCK input high time	30			ns
$t_{SPIS,WLSCKIN}$	SCK input low time	30			ns
$t_{SPIS,SUCSN}$	CSN to CLK setup time	1000[14]			ns
$t_{SPIS,HCSN}$	CLK to CSN hold time	1000			ns
$t_{SPIS,ASA}$	CSN to SDO driven			70	ns
$t_{SPIS,ASO}$	CSN to SDO valid[15]			1000	ns
$t_{SPIS,DISSO}$	CSN to SDO disabled[15]			70	ns
$t_{SPIS,CWH}$	CSN inactive time	300			ns

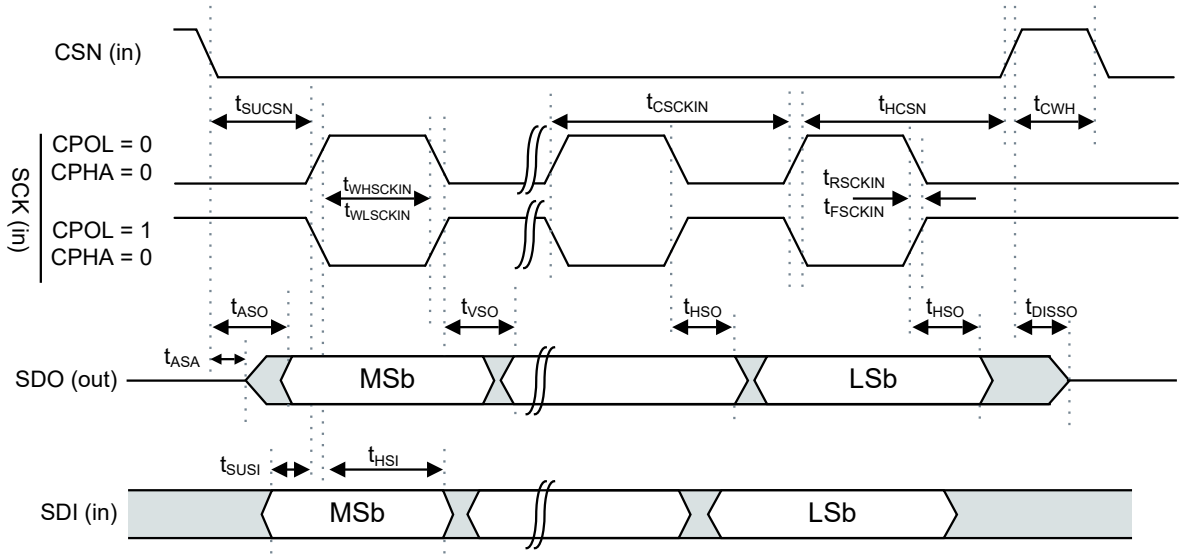

Figure 196: SPIS timing diagram, CPHA = 0

12 High bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.
13 The actual maximum data rate depends on the master's CLK to SDO and SDI setup and hold timings.
14 Excluding any start-up delay for the high frequency clock in low power mode.
15 At 25pF load, including GPIO capacitance, see GPIO spec.