Table 8-24. FSM_CNTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	FSM_CNTR_STAT	RH	0h	Reads back the number of time FSM has been entered in a row up to 15. Can be cleared by writing 0h.

8.6.15 DEVICE_RST Register (Address = 19h) [reset = 0h]

DEVICE_RST is shown in Figure 8-69 and described in Table 8-25.

Return to Summary Table.

Forces a soft or hard reset.

Figure 8-69. DEVICE_RST Register

7	6	5	4	3	2	1	0
RESERVED						SF_RST	HD_RST
R-00h						R/W1C-0b	R/W1C-0b

Table 8-25. DEVICE_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	00h	Reserved
1	SF_RST	R/W1C	0b	Soft Reset: Writing a 1 causes a soft reset. Device registers return to default values while keeping INH on.
0	HD_RST	R/W1C	0b	Hard Reset: Forces a power on reset when writing a 1. **Note** NOTE: This will set the PWRON interrupt flag.

8.6.16 DEVICE_CONFIG (Address = 1Ah) [reset = 80h]

DEVICE_CONFIG is shown in Figure 8-70 and described in Table 8-26

Return to Summary Table.

Enables SPI to work in sleep mode if V_{IO} is available.

WKRQ/INH and LIMP pin configuration.

Figure 8-70. DEVICE_CONFIG Register

7	6	5	4	3	2	1	0
WKRQ_POL_SEL	WKRQ_INH_DIS	INH_LIMP_SEL	LIMP_DIS	LIMP_SEL_RESET		LIMP_RESET	RSVD
R/W-1b	R/W-0b	R/W - 0b	R/W - 0b	R/W - 00b		R/W1C - 0b	R - 0b

Table 8-26. DEVICE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WKRQ_POL_SEL	R/W	1b	Selects the polarity for the WKRQ pin 0b = Low 1b = High
6	WKRQ_INH_DIS	R/W	0b	WKRQ/INH pin disable 0b = Enabled 1b = Disabled
5	INH_LIMP_SEL	R/W	0b	Pin function select function of INH pin 0b = INH 1b = LIMP Note: This only works if WKRQ/INH pin is configured for INH at power-up. If pin is WKRQ writing to this bit will be ignored.