			Reset source		
Register	Function	Reset value	Cat 1	Cat 2	Cat 3
PROTECT.DOMAIN[0].DBGEN	Allow invasive debugging in non-secure mode of Arm Cortex-M33.	0	x	x	
PROTECT.DOMAIN[0].NIDEN	Allow non-invasive debugging in non-secure mode of Arm Cortex-M33.	0	x	x	
PROTECT.DOMAIN[0].SPIDEN	Allow invasive debugging in secure mode of Arm Cortex-M33.	0	x	x	
PROTECT.DOMAIN[0].SPNIDEN	Allow non-invasive debugging in secure mode of Arm Cortex-M33.	0	x	x	
PROTECT.AP[0].DBGEN	Allow debugging of FLPR RISC-V CPU.	0	x	x	
PROTECT.ACTIVESHIELD	Enable active shield detector.	0	x	x	x
PROTECT.CRACENTAMP	Enable CRACEN tamper detector.	1	x	x	x
PROTECT.GLITCHSLOWDOMAIN	Enable slow domain glitch detector.	1	x	x	x
PROTECT.GLITCHFASTDOMAIN	Enable fast domain glitch detector.	1	x	x	x
PROTECT.EXTRESETEN	Enable automatic reset from external tamper detectors events.	0	x	x	x
PROTECT.INTRESETEN	Enable automatic reset from internal tamper detector events.	1	x	x	x
PROTECT.ERASEPROTECT	Allow device erase using CTRL-AP and RRAMC.	0	x	x	x

Table 34: TAMPC protected signals

7.8.6.6 Registers

Instances

Instance	Domain	Base address	TrustZone			Split access	Description
			Map	Att	DMA		
TAMPC	GLOBAL	0x500DC000	HF	S	NA	No	Tamper controller TAMPC

Configuration

Instance	Domain	Configuration
TAMPC	GLOBAL	For the active shield function, use dedicated pins on P1 Reset value of field VALUE in register PROTECT.INTRESETEN.CTRL: 1

Register overview

Register	Offset	TZ	Description
EVENTS_TAMPER	0x100		Tamper controller detected an error.
EVENTS_WRITEERROR	0x104		Attempt to write a VALUE in PROTECT registers without clearing the WRITEPROTECT.