

A peripheral configured as non-secure can only access non-secure pins. A peripheral configured as secure will be able to access all pins. An attempt to access a pin configured as secure by a non-secure peripheral is ignored.

GPIO pins can be read and written through individual bits in the GPIO port registers OUT, OUTSET, OUTCLR, and IN. GPIO pin direction is configured individually using bits in registers DIR, DIRSET, and DIRCLR. An attempt to access bits with a different security setting is ignored. Writing to these bits will have no effect, and read access returns a zero value.

The LATCH register has split security. Non-secure code can only read the state of the non-secure pins, while the secure pins read as zero. Secure code is able to read the state of all pins.

The DETECTMODE register applies to the entire port (both secure and non-secure pins), and determines if the latched or non-latched signals will generate the DETECT signal.

Pin security configuration

Access to device pins can be controlled by SPU. A pin can be set as secure so that only secure peripherals or secure code can access it. Pins set as non-secure can be accessed by both secure and non-secure peripherals or code.

The security attribute of each pin can be individually configured in [FEATURE.GPIO\[n\].PIN\[o\]](#) ($n=0..2$) ($o=0..31$) on page 189. When the secure attribute (SECATTR) is set for a pin, only peripherals that have the secure attribute set will be able to read the value of the pin or change it.

Peripherals can select the pins they need access to through their PSEL registers. If a peripheral has its attribute set to non-secure, but one of its PSEL registers selects a pin with the attribute set to secure, the SPU controlled logic will ensure that the pin selection is not propagated. In addition, the pin value will always be read as zero to prevent a non-secure peripheral from obtaining a value from a secure pin. Access to other pins with the attribute set as non-secure will not be blocked.

Pins can also be dedicated to peripherals by using the CTRLSEL field in the GPIO PIN_CNF[n] register. For pins controlled using CTRLSEL, the SPU PIN security setting is bypassed and pin access is controlled by the peripheral. This is illustrated in the following figure.

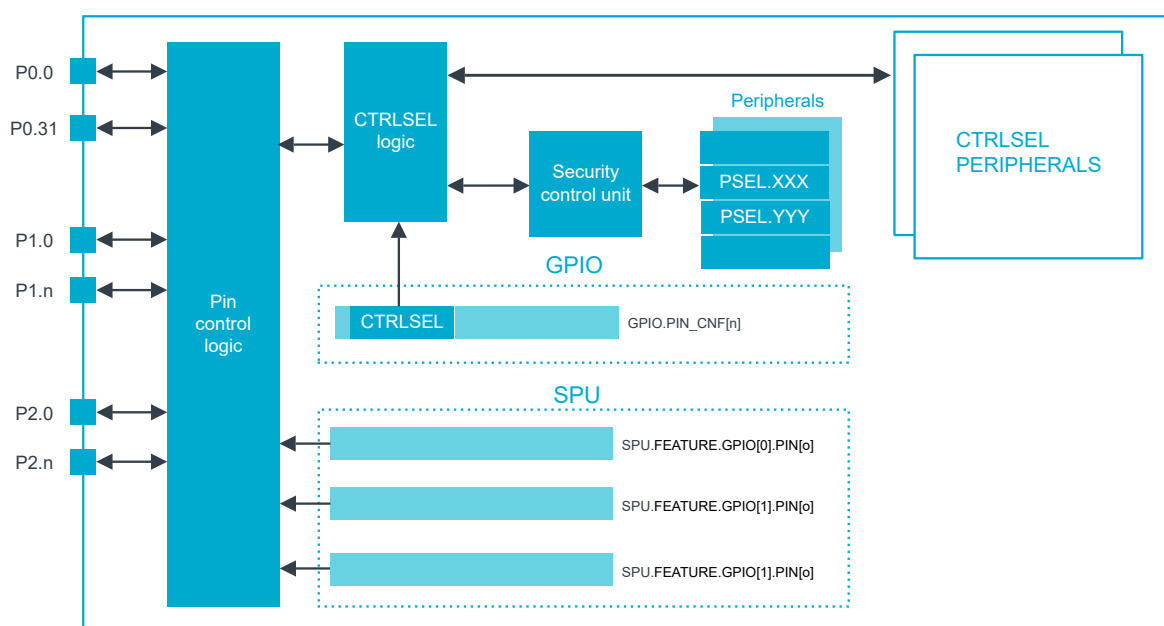


Figure 30: Pin access using CTRLSEL