6.2.6.4 CHENSET

Address offset: 0x504

Channel enable set register

> **Note:** Read: Reads value of CH[i] field in CHEN register

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	X W V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

ID	R/W	Field	Value ID	Value	Description
A-X	RW W1S	CH[i] (i=0..23)			Channel i enable set register. Writing 0 has no effect.
			Disabled	0	Read: Channel disabled
			Enabled	1	Read: Channel enabled
			Set	1	Write: Enable channel

6.2.6.5 CHENCLR

Address offset: 0x508

Channel enable clear register

> **Note:** Read: Reads value of CH[i] field in CHEN register

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	X W V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

ID	R/W	Field	Value ID	Value	Description
A-X	RW W1C	CH[i] (i=0..23)			Channel i enable clear register. Writing 0 has no effect.
			Disabled	0	Read: Channel disabled
			Enabled	1	Read: Channel enabled
			Clear	1	Write: Disable channel

6.2.6.6 CHG[n] (n=0..5)

Address offset: 0x800 + (n × 0x4)

Channel group n

Note: Writes to this register are ignored if either SUBSCRIBE_CHG[n].EN or SUBSCRIBE_CHG[n].DIS is enabled

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	X W V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

ID	R/W	Field	Value ID	Value	Description
A-X	RW	CH[i] (i=0..23)			Include or exclude channel i
			Excluded	0	Exclude
			Included	1	Include

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