

Figure 200: TWIM timing diagram, 1 byte transaction

11.23 TWIS Electrical specification

11.23.1 TWIS slave timing specifications

Symbol	Description	Min.	Typ.	Max.	Units
$f_{\text{TWIS,SCL}}$	Bit rates for TWIS ¹⁷	100		400	kbps
$t_{\text{TWIS,START}}$	Time from PREPARERX/PREPARETX task to ready to receive/transmit		1.5		μs
$t_{\text{TWIS,SU_DATI}}$	Input data setup time before positive edge on SCL – all modes	20			ns
$t_{\text{TWIS,HD_DATI}}$	Input data hold time after negative edge on SCL – all modes	0			ns
$t_{\text{TWIS,HD_DATO}}$	Output data hold time after negative edge on SCL – all modes	350		600	ns
$t_{\text{TWIS,HD_STA,100kbps}}$	TWI slave hold time from for START condition (SDA low to SCL low), 100 kbps	500			ns
$t_{\text{TWIS,HD_STA,400kbps}}$	TWI slave hold time from for START condition (SDA low to SCL low), 400 kbps	500			ns
$t_{\text{TWIS,SU_STO,100kbps}}$	TWI slave setup time from SCL high to STOP condition, 100 kbps	500			ns
$t_{\text{TWIS,SU_STO,400kbps}}$	TWI slave setup time from SCL high to STOP condition, 400 kbps	500			ns
$t_{\text{TWIS,BUF,100kbps}}$	TWI slave bus free time between STOP and START conditions, 100 kbps	500			ns
$t_{\text{TWIS,BUF,400kbps}}$	TWI slave bus free time between STOP and START conditions, 400 kbps	500			ns

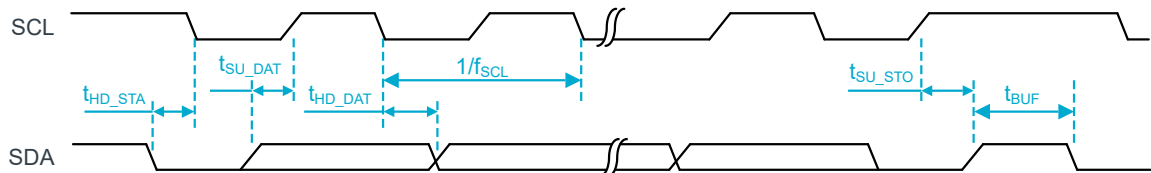


Figure 201: TWIS timing diagram, 1 byte transaction

11.24 UARTE Electrical specification

11.24.1 UARTE electrical specification

Symbol	Description	Min.	Typ.	Max.	Units
f_{UARTE}	Baud rate for UARTE			1000	kbps
$f_{\text{UARTE,HS}}$	Bit rates for high-speed UARTE instances ¹⁸			4000	kbps
$t_{\text{UARTE,CTSH}}$	CTS high time	0.5			μs
$t_{\text{UARTE,START}}$	Time from STARTRX/STARTTX task to transmission started		0.5		μs

¹⁷ High bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see [GPIO](#) chapter for more details.

¹⁸ High baud rates may require GPIOs to be set as High Drive, see [GPIO](#) chapter for more details.