Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A
Reset 0x0000001F				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1**
ID	R/W	Field	Value ID	Value	Description
A	RW	TH			M-Mode Interrupt-level Threshold
			DISABLED	0x0	Threshold disabled
			THRESHLEVEL0	0x3F	Threshold level 0 This enumerator is deprecated.
			THRESHLEVEL1	0x7F	Threshold level 1 This enumerator is deprecated.
			THRESHLEVEL2	0xBF	Threshold level 2 This enumerator is deprecated.
			THRESHLEVEL3	0xFF	Threshold level 3 This enumerator is deprecated.

8.26.3.12 MCLICBASE

Address offset: 0x350

Machine CLIC Base

Provides the base address of CLIC memory mapped registers. Its value should be configured or set up at the platform level to indicate the starting address of CLIC memory mapped registers. Since the CLIC memory map must be aligned at a 4KiB boundary, the mclicbase CSR has its 12 least-significant bits hardwired to zero. It is used to inform software about the location of CLIC memory mappped registers. CLIC Base address is unique for every VPR instance and this register's reset value is set to it

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0xF0000000				**1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	VAL			CLIC base address value

8.26.3.13 TSELECT

Address offset: 0x7A0

Trigger Select

This register determines which trigger is accessible through the other trigger registers. The set of accessible triggers must start at 0, and be contiguous

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	VAL			Trigger Select value

8.26.3.14 TDATA1

Address offset: 0x7A1

Trigger Data 1