| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| ID | | | | O N M L K J I H G F E D C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| ID | R/W | Field | Value ID | Value | Description |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| H | RW | DMARXBUSERROR | | | Enable or disable interrupt for event DMARXBUSERROR<br>When this event is generated, the address which caused the error can be read from the BUSERRORADDRESS register. |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| I-L | RW | DMARXMATCH[i] (i=0..3) | | | Enable or disable interrupt for event DMARXMATCH[i] |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| M | RW | DMATXEND | | | Enable or disable interrupt for event DMATXEND |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| N | RW | DMATXREADY | | | Enable or disable interrupt for event DMATXREADY |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |
| O | RW | DMATXBUSERROR | | | Enable or disable interrupt for event DMATXBUSERROR<br>When this event is generated, the address which caused the error can be read from the BUSERRORADDRESS register. |
| | | | Disabled | 0 | Disable |
| | | | Enabled | 1 | Enable |

## 8.23.10.23 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| ID | | | | O N M L K J I H G F E D C B A |
| **Reset 0x00000000** | | | | **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0** |
| ID | R/W | Field | Value ID | Value | Description |
| A | RW W1S | STOPPED | | | Write '1' to enable interrupt for event STOPPED |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| B | RW W1S | ERROR | | | Write '1' to enable interrupt for event ERROR |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| C | RW W1S | SUSPENDED | | | Write '1' to enable interrupt for event SUSPENDED |
| | | | Set | 1 | Enable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| D | RW W1S | LASTRX | | | Write '1' to enable interrupt for event LASTRX |
| | | | Set | 1 | Enable |