Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	D C B A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

ID	R/W	Field	Value ID	Value	Description
A	RW	PUSHLEN			Length of data block
B	RW	PUSHCSTADDR			Constant address
C	RW	PUSHREALIGN			Realign length
D	RW	PUSHDISCARD			Discard data

7.8.1.7.8 CRYPTMSTRDMA.INTEN

Address offset: 0x01C

Interrupt Enable mask

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	F E D C B A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

ID	R/W	Field	Value ID	Value	Description
A	RW	FETCHERBLOCKEND			Fetcher DMA reached the end of a block (if enabled in the descriptor; scatter-gather only)
B	RW	FETCHERSTOPPED			Fetcher DMA reached the end of a block with Stop=1, or end of direct transfer
C	RW	FETCHERERROR			Bus error during fetcher DMA access
D	RW	PUSHERBLOCKEND			Pusher DMA reached the end of a block (if enabled in the descriptor; scatter-gather only)
E	RW	PUSHERSTOPPED			Pusher DMA reached the end of a block with Stop=1, or end of direct transfer
F	RW	PUSHERERROR			Bus error during pusher DMA access

7.8.1.7.9 CRYPTMSTRDMA.INTENSET

Address offset: 0x020

Interrupt Set

Writing a 1 to a bit in this register enables the corresponding interrupt. Writing 0 has no effect.

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	F E D C B A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

ID	R/W	Field	Value ID	Value	Description
A	RW	FETCHERBLOCKEND			Fetcher DMA reached the end of a block (if enabled in the descriptor; scatter-gather only)
B	RW	FETCHERSTOPPED			Fetcher DMA reached the end of a block with Stop=1, or end of direct transfer
C	RW	FETCHERERROR			Bus error during fetcher DMA access
D	RW	PUSHERBLOCKEND			Pusher DMA reached the end of a block (if enabled in the descriptor; scatter-gather only)
E	RW	PUSHERSTOPPED			Pusher DMA reached the end of a block with Stop=1, or end of direct transfer
F	RW	PUSHERERROR			Bus error during pusher DMA access

7.8.1.7.10 CRYPTMSTRDMA.INTENCLR

Address offset: 0x024

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