Interrupts are generated when enabled events are triggered. When an event for a split security interrupt is triggered, the following applies.

- If an interrupt is configured as secure, an event associated to either a secure or non-secure feature can trigger the interrupt.
- If an interrupt is configured as non-secure, only events associated with non-secure features can trigger the interrupt.

An attempt to enable an interrupt for an event that does not match the ownership and security settings of the interrupt will be ignored and a security fault is not generated.

A non-secure event can be enabled to trigger a secure interrupt.

7.6.1 CRACEN

CRACEN protects the Protected RAM and the SEED register from being accessed by the CPU.

Only KMU is able to push assets to the Protected RAM and the SEED register. The CPU does not have access to these. The hardware has built in protection that does not need configuration.

7.6.2 DPPIC

Individual DPPI channels and channel groups can have independent security attributes that are defined as either secure or non-secure. DPPI supports split security, handling both secure and non-secure access.

DPPI channels

A peripheral configured as non-secure can only subscribe to or publish on non-secure DPPI channels. A peripheral configured as secure can access all DPPI channels. An attempt by a non-secure peripheral to subscribe to or publish on a DPPI channel configured as secure is ignored, and a PPI event is not issued.

DPPI channels are enabled or disabled through individual bits in registers CHEN, CHENSET, and CHENCLR.

The security of a DPPI channel is configured using FEATURE.DPPIC.CH[n] (n=0..23) on page 187.

DPPI channel groups

Channels can be grouped, which allows them to be enabled or disabled collectively.

A channel group is either secure or non-secure.

- Secure channel group – includes both secure and non-secure DPPI channels
- Non-secure channel group – only includes non-secure DPPI channels

An attempt to include a secure DPPI channel in a non-secure DPPI channel group is ignored.

Registers CHG[n], TASKS_CHG[n].EN, TASKS_CHG[n].DIS, SUBSCRIBE_CHG[n].EN, and SUBSCRIBE_CHG[n].DIS configure the DPPI channel groups. A security fault is triggered when an illegal access is made to these registers.

DPPIC subscribe to DPPIC channels through the SUBSCRIBE_CHG[] registers to trigger the task for enabling or disabling channel groups. An event from a secure channel is ignored if the group subscribing to that channel is non-secure. A secure group can subscribe to a non-secure channel or a secure channel.

The security of a DPPIC channel group is configured using FEATURE.DPPIC.CHG[n] (n=0..7) on page 188.

7.6.3 GPIO

GPIO pins can be either secure or non-secure.

GPIO supports split security, meaning the GPIO pins and registers can be accessed from both secure and non-secure peripherals.