

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID			W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A									
Reset 0x00000000			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
ID	R/W	Field	Value ID	Value	Description																													
			Clear	1	Disable																													
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													
O	RW	EDEND	Write '1' to disable interrupt for event EDEND																															
		W1C			Clear	1	Disable																											
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													
P	RW	EDSTOPPED	Write '1' to disable interrupt for event EDSTOPPED																															
		W1C			Clear	1	Disable																											
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													
Q	RW	CCAIDLE	Write '1' to disable interrupt for event CCAIDLE																															
		W1C			Clear	1	Disable																											
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													
R	RW	CCABUSY	Write '1' to disable interrupt for event CCABUSY																															
		W1C			Clear	1	Disable																											
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													
S	RW	CCASTOPPED	Write '1' to disable interrupt for event CCASTOPPED																															
		W1C			Clear	1	Disable																											
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													
T	RW	RATEBOOST	Write '1' to disable interrupt for event RATEBOOST																															
		W1C			Clear	1	Disable																											
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													
U	RW	MHRMATCH	Write '1' to disable interrupt for event MHRMATCH																															
		W1C			Clear	1	Disable																											
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													
V	RW	SYNC	Write '1' to disable interrupt for event SYNC																															
		W1C			MODE=Ble_LR125Kbit, Ble_LR500Kbit, or IEEE802154_250Kbit: A possible preamble has been received. However, due to the sporadic reception of noise, this event can be falsely triggered.																													
			For MODE=Nrf_1Mbit, Nrf_2Mbit, Ble_1Mbit, or Ble_2Mbit: A possible preamble and the first two bytes of the address field has been received. The event can be generated falsely also in this mode.																															
			It is also possible that the event is not generated, or not generated before the ADDRESS event.																															
			Clear	1	Disable																													
			Disabled	0	Read: Disabled																													