Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	WRITE_SUSPEND			Shortcut between event WRITE and task SUSPEND
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
B	RW	READ_SUSPEND			Shortcut between event READ and task SUSPEND
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
C-F	RW	DMA_RX_MATCH[i]_DMA_RX_ENABLEMATCH[(i+1)%4] (i=0..3)			Shortcut between event DMA.RX.MATCH[n] and task DMA.RX.ENABLEMATCH[(i+1)%4] Allows daisy-chaining match events.
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut
G-J	RW	DMA_RX_MATCH[i]_DMA_RX_DISABLEMA (i=0..3)			Shortcut between event DMA.RX.MATCH[n] and task DMA.RX.DISABLEMATCH[n]
			Disabled	0	Disable shortcut
			Enabled	1	Enable shortcut

8.24.10.24 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				N M L K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	STOPPED			Enable or disable interrupt for event STOPPED
			Disabled	0	Disable
			Enabled	1	Enable
B	RW	ERROR			Enable or disable interrupt for event ERROR
			Disabled	0	Disable
			Enabled	1	Enable
C	RW	WRITE			Enable or disable interrupt for event WRITE
			Disabled	0	Disable
			Enabled	1	Enable
D	RW	READ			Enable or disable interrupt for event READ
			Disabled	0	Disable
			Enabled	1	Enable
E	RW	DMARXEND			Enable or disable interrupt for event DMARXEND
			Disabled	0	Disable
			Enabled	1	Enable
F	RW	DMARXREADY			Enable or disable interrupt for event DMARXREADY
			Disabled	0	Disable
			Enabled	1	Enable
G	RW	DMARXBUSERROR			Enable or disable interrupt for event DMARXBUSERROR When this event is generated, the address which caused the error can be read from the BUSERRORADDRESS register.
			Disabled	0	Disable
			Enabled	1	Enable
H-K	RW	DMARXMATCH[i] (i=0..3)			Enable or disable interrupt for event DMARXMATCH[i]