7.8.4.3.4 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number					31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID					A
Reset 0x00000000					0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ID	R/W	Field	Value ID	Value	Description
A	RW	MEMACCERR			Write '1' to disable interrupt for event MEMACCERR
	W1C				
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

7.8.4.3.5 MEMACCERR

Memory Access Error status registers

7.8.4.3.5.1 MEMACCERR.ADDRESS

Address offset: 0x400

Target Address of Memory Access Error. Register content will not be changed as long as MEMACCERR event is active.

Bit number					31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID					A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000					0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ID	R/W	Field	Value ID	Value	Description
A	R	ADDRESS			Target address for erroneous access

7.8.4.3.5.2 MEMACCERR.INFO

Address offset: 0x404

Access information for the transaction that triggered a memory access error. Register content will not be changed as long as MEMACCERR event is active.

Bit number					31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID					E D C B A
Reset 0x00000000					0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ID	R/W	Field	Value ID	Value	Description
A	R	READ			Read bit of bus access
			Set	1	Read access bit was set
			NotSet	0	Read access bit was not set
B	R	WRITE			Write bit of bus access
			Set	1	Write access bit was set
			NotSet	0	Write access bit was not set
C	R	EXECUTE			Execute bit of bus access
			Set	1	Execute access bit was set
			NotSet	0	Execute access bit was not set
D	R	SECURE			Secure bit of bus access
			Set	1	Secure access bit was set
			NotSet	0	Secure access bit was not set

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