Through the debugger interface, CTRL-AP can generate three resets using register RESET on page 827. For more details, see CTRL-AP — Control access port on page 822.

Similar to a power-on reset (POR), the device is restarted after a CTRL-AP reset.

5.8.8 Watchdog timer reset

A watchdog timer (WDT) reset is generated when the watchdog timer times out.

Similar to a power-on reset (POR), the device is started after a watchdog reset.

5.8.9 Retained registers

A retained register is one that keeps its value when entering System OFF mode. See individual peripheral chapters for information about which registers are retained.

5.8.10 Reset behavior

The reset source determines the behavior of the device after a reset.

In System OFF mode, the watchdog timer is not running and CPU lockup is not possible. RAM may be fully or partially retained, depending on RAM retention settings in MEMCONF — Memory configuration on page 44.

If the device is in Debug Interface mode, the debug components are not reset. Additionally, CPU lockup does not generate a reset. See Debug and trace on page 815 for more information about the different debug components in the system.

An 'x' in the table means that the specific module or register is reset. The table also explicitly lists which reset sources are commonly referred to as 'cold boot'.