

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A																															
<b>Reset 0x00000000</b>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	R/W	Field	Value ID	Value	Description																											
A	RW	READY			Generated when EasyDMA has buffered the .PTR and .MAXCNT registers for the channel, allowing them to be written to prepare for the next sequence.																											
		NotGenerated	0	Event not generated																												
		Generated	1	Event generated																												

#### ***8.15.5.13.1.3 EVENTS\_DMA.SEQ[n].BUSERROR (n=0..1)***

Address offset:  $0x12C + (n \times 0xC)$

An error occurred during the bus transfer.

When this event is generated, the address which caused the error can be read from the **BUSERRORADDRESS** register.

#### 8.15.5.14 EVENTS COMPAREMATCH[n] (n=0..3)

Address offset: 0x13C + (n × 0x4)

This event is generated when the compare matches for the compare channel [n].

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A																															
<b>Reset 0x00000000</b>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	R/W	Field	Value ID	Value	Description																											
A	RW	EVENTS_COMPAREMATCH			This event is generated when the compare matches for the compare channel [n].																											
		NotGenerated	0		Event not generated																											
		Generated	1		Event generated																											

### 8.15.5.15 PUBLISH STOPPED

Address offset: 0x184

## Publish configuration for event STOPPED