

### 8.15.5.19 PUBLISH\_LOOPSDONE

Address offset: 0x19C

Publish configuration for event **LOOPSDONE**

This event triggers after the last SEQ[1] completion of the loop, and only if looping was enabled (LOOP > 0) when the sequence playback was started.

| Bit number       |     |       |          | 31       | 30                 | 29   | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
|------------------|-----|-------|----------|----------|--------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID               |     |       |          | B        |                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |     |       |          | 0        | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |   |
| ID               | R/W | Field | Value ID | Value    |                    | Description  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW  | CHIDX |          | [0..255] |                    | DPPI channel that event <b>LOOPSDONE</b> will publish to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW  | EN    |          |          |                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |     |       | Disabled | 0        | Disable publishing |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |     |       | Enabled  | 1        | Enable publishing  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 8.15.5.20 PUBLISH\_RAMUNDERFLOW

Address offset: 0x1A0

Publish configuration for event **RAMUNDERFLOW**

|                  |     |       |          |          |                    |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |  |   |  |  |
|------------------|-----|-------|----------|----------|--------------------|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|--|--|---|--|--|
| Bit number       |     |       |          | 31       | 30                 | 29  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |  |  |   |  |  |
| ID               |     |       |          | B        |                    |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   | A |   |   | A |  |  | A |  |  | A |  |  |
| Reset 0x00000000 |     |       |          | 0        |                    |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |  |   |  |  |
| ID               | R/W | Field | Value ID | Value    |                    | Description   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |  |   |  |  |
| A                | RW  | CHIDX |          | [0..255] |                    | DPPI channel that event <span>RAMUNDERFLOW</span> will publish to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |  |   |  |  |
| B                | RW  | EN    |          |          |                    |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |  |   |  |  |
|                  |     |       | Disabled | 0        | Disable publishing |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |  |   |  |  |
|                  |     |       | Enabled  | 1        | Enable publishing  |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |  |   |  |  |

### 8.15.5.21 PUBLISH\_DMA

Publish configuration for events

#### 8.15.5.21.1 PUBLISH\_DMA.SEQ[n] (n=0..1)

Publish configuration for events

##### 8.15.5.21.1.1 PUBLISH\_DMA.SEQ[n].END (n=0..1)

Address offset: 0x1A4 + (n × 0xC)

Publish configuration for event **END**

|                  |     |       |          |          |                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|-----|-------|----------|----------|--------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |     |       |          | 31       | 30                 | 29   | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |     |       |          | B        |                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |     |       |          | 0        |                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | R/W | Field | Value ID | Value    |                    | Description  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW  | CHIDX |          | [0..255] |                    | DPPI channel that event <b>END</b> will publish to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW  | EN    |          |          |                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |     |       | Disabled | 0        | Disable publishing |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |     |       | Enabled  | 1        | Enable publishing  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |