8.26.1.13 DEBUGIF.HARTINFO

Address offset: 0x448

Hart Information

This register gives information about the hart currently selected by hartsel. This register is optional. If it is not present it should read all-zero. If this register is included, the debugger can do more with the Program Buffer by writing programs which explicitly access the data and/or dscratch registers

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D D D D C B B B B A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	DATAADDR		-2048 .. 2047	Data Address If dataaccess is 0: The number of the first CSR dedicated to shadowing the data registers. If dataaccess is 1: Address of RAM where the data registers are shadowed. This address is sign extended and easily addressed with a load or store using x0 as the address register.
B	R	DATASIZE		0 .. 12	Data Size If dataaccess is 0: Number of CSRs dedicated to shadowing the data registers. If dataaccess is 1: Number of 32-bit words in the memory map dedicated to shadowing the data registers. Since there are at most 12 data registers, the value in this register must be 12 or smaller
C	R	DATAACCESS			Data Access
			No	0	The data registers are shadowed in the hart by CSRs. Each CSR is DXLEN bits in size, and corresponds to a single argument.
			Yes	1	The data registers are shadowed in the hart's memory map. Each register takes up 4 bytes in the memory map.
D	R	NSCRATCH			Number of dscratch registers Number of dscratch registers available for the debugger to use during program buffer execution, starting from dscratch0. The debugger can make no assumptions about the contents of these registers between commands.

8.26.1.14 DEBUGIF.HALTSUM1

Address offset: 0x44C

Halt Summary 1

Each bit in this read-only register indicates whether any of a group of harts is halted or not. Unavailable/ nonexistent harts are not considered to be halted. This register might not be present if fewer than 33 harts are connected to this DM. The LSB reflects the halt status of harts hartsel[19:10] 0x0 through 0x1f. The MSB reflects the halt status of harts hartsel[19:10] 0x3e0 through 0x3ff.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	HALTSUM1			Halt Summary 1

8.26.1.15 DEBUGIF.HAWINDOWSEL

Address offset: 0x450

Hart Array Window Select