

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				V U T S R Q P O N M L K J I H G F E D C B A																															
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value	Description																														
L	RW	CH2LIMITL W1S			Write '1' to enable interrupt for event CH2LIMITL																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
M	RW	CH3LIMITH W1S			Write '1' to enable interrupt for event CH3LIMITH																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
N	RW	CH3LIMITL W1S			Write '1' to enable interrupt for event CH3LIMITL																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
O	RW	CH4LIMITH W1S			Write '1' to enable interrupt for event CH4LIMITH																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
P	RW	CH4LIMITL W1S			Write '1' to enable interrupt for event CH4LIMITL																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
Q	RW	CH5LIMITH W1S			Write '1' to enable interrupt for event CH5LIMITH																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
R	RW	CH5LIMITL W1S			Write '1' to enable interrupt for event CH5LIMITL																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
S	RW	CH6LIMITH W1S			Write '1' to enable interrupt for event CH6LIMITH																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
T	RW	CH6LIMITL W1S			Write '1' to enable interrupt for event CH6LIMITL																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
U	RW	CH7LIMITH W1S			Write '1' to enable interrupt for event CH7LIMITH																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														