

9.8.1.19 TRCVDSACCTLR

Address offset: 0x0A4

ViewData include / exclude control.

Might ignore writes when the trace unit is enabled or not idle.

This register must be programmed when one or more address comparators are implemented.

9.8.1.20 TRCVDARCCTLR

Address offset: 0x0A8

ViewData include / exclude control.

Might ignore writes when the trace unit is enabled or not idle.

This register must be programmed when one or more address comparators are implemented.

9.8.1.21 TRCSEQEVR[n] (n=0..2)

Address offset: $0x100 \pm (n \times 0x4)$

Moves the sequencer state according to programmed events.