Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID					G	G	G											F	F					E	E	D	D					C	C	B	A
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value																															
E	RW	DRIVE1																																	
			S1	0																															
			H1	1																															
			D1	2																															
			E1	3																															
F	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															
G	RW	CTRLSEL																																	
			GPIO	0x0																															
			VPR	0x1																															
			GRTC	0x4																															

Drive configuration for '1'

Disconnect '1'(normally used for wired-or connections)

Extra high drive '1'

Note: The DRIVE0 must be E0 as well to work properly.

Pin sensing mechanism

Disabled

Sense for high level

Sense for low level

Select which module has direct control over this pin

Note: this field is only accessible from secure code

GPIO or peripherals with PSEL registers

VPR processor

GRTC peripheral

8.9 GPIOTE — GPIO tasks and events

The GPIO tasks and events (GPIOTE) peripheral provides functionality for accessing GPIO pins using tasks and events. Each GPIOTE channel can be assigned to one pin.

The main features of GPIOTE are the following:

- GPIO pin state change by triggering tasks
- Event generation on GPIO pin state change
- PORT event generation on GPIO DETECT signal
- Support for split security on individual GPIOTE channels

A GPIOTE block enables GPIOs to generate events on pin state change which can be used to carry out tasks through the PPI system. A GPIO can also be driven to change state on system events using the PPI system. See Peripheral interface on page 213 for additional information on tasks and events. GPIO is described in more detail in GPIO — General purpose input/output on page 274.

Detection of pin state changes when in low power mode is possible when in System ON or System OFF.

GPIOTE supports split-security. Each channel is assigned a security state (S/NS).

Up to three tasks can be used in each GPIOTE channel for performing write operations to a pin. Tasks SET and CLR are fixed. OUT can be configured to perform following operations:

- Set
- Clear
- Toggle

An event can be generated in each GPIOTE channel from one of the following input conditions:

- Rising edge
- Falling edge
- Any change