   2. SRC.VALUE = random[i], where i=0,1, and 2 (i.e. random number results from CRACEN.RND operation above)

2. Load seed from KMU to CRACEN:

   a. Push the KMU slots where the SEED is stored, e.g. KMU slots 0, 1, and 2
   b. Write CRACEN.SEEDVALID register to mark the seed as valid for the IKG
   c. To prevent any subsequent changes to the SEED, write CRACEN.SEEDLOCK register.

   Note: Any IKG key generations without valid seed (CRACEN.SEEDVALID) will fail.

7.8.1.5 Low power

To ensure lowest possible power consumption when the peripheral is not needed, disable CRACEN.

Make sure any operations are finished before disabling the peripheral in register ENABLE.

7.8.1.6 Registers

Instances

Instance	Domain	Base address	TrustZone			Split access	Description
			Map	Att	DMA		
CRACEN	GLOBAL	0x50048000	HF	S	NSA	No	Crypto accelerator

Configuration

Instance	Domain	Configuration
CRACEN	GLOBAL	Access to CRACEN registers is blocked while KMU is performing a PUSH operation. CRACEN cannot write RRAM.
		CRACEN CRYPTOACCELERATOR specific configuration registers included
		PKE data (address 0x51808000) must be read and written using aligned access, i.e. using an operation where a word-aligned address is used for a word, or a halfword-aligned address is used for a halfword access.
		PKE code (address 0x5180C000) must be read and written using aligned access, i.e. using an operation where a word-aligned address is used for a word, or a halfword-aligned address is used for a halfword access.

Register overview

Register	Offset	TZ	Description
EVENTS_CRYPTOMASTER	0x100		Event indicating that interrupt triggered at Cryptomaster
EVENTS_RNG	0x104		Event indicating that interrupt triggered at RNG
EVENTS_PKEIKG	0x108		Event indicating that interrupt triggered at PKE or IKG
INTEN	0x300		Enable or disable interrupt
INTENSET	0x304		Enable interrupt
INTENCLR	0x308		Disable interrupt
INTPEND	0x30C		Pending interrupts
ENABLE	0x400		Enable CRACEN peripheral modules.
SEEDVALID	0x404		Marks the SEED register as valid.
SEED[n]	0x410		Seed word [n] for symmetric and asymmetric key generation. This register is only writable from KMU.

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