

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
ID		A			
Reset 0x00000000		0 0			
ID	R/W	Field	Value ID	Value	Description
A	RW	READY			Generated when EasyDMA has buffered the .PTR and .MAXCNT registers for the channel, allowing them to be written to prepare for the next sequence.
			NotGenerated	0	Event not generated
			Generated	1	Event generated

8.24.10.17.2.3 EVENTS_DMA.TX.BUSERROR

Address offset: 0x170

An error occurred during the bus transfer.

When this event is generated, the address which caused the error can be read from the BUSERRORADDRESS register.

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
ID		A			
Reset 0x00000000		0 0			
ID	R/W	Field	Value ID	Value	Description
A	RW	BUSERROR			An error occurred during the bus transfer.
					When this event is generated, the address which caused the error can be read from the BUSERRORADDRESS register.
			NotGenerated	0	Event not generated
			Generated	1	Event generated

8.24.10.18 PUBLISH_STOPPED

Address offset: 0x184

Publish configuration for event **STOPPED**

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
ID		B A A A A A A A			
Reset 0x00000000		0 0			
ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX	[0..255]		DPPI channel that event STOPPED will publish to
B	RW	EN			
			Disabled	0	Disable publishing
			Enabled	1	Enable publishing

8.24.10.19 PUBLISH_ERROR

Address offset: 0x194

Publish configuration for event **ERROR**