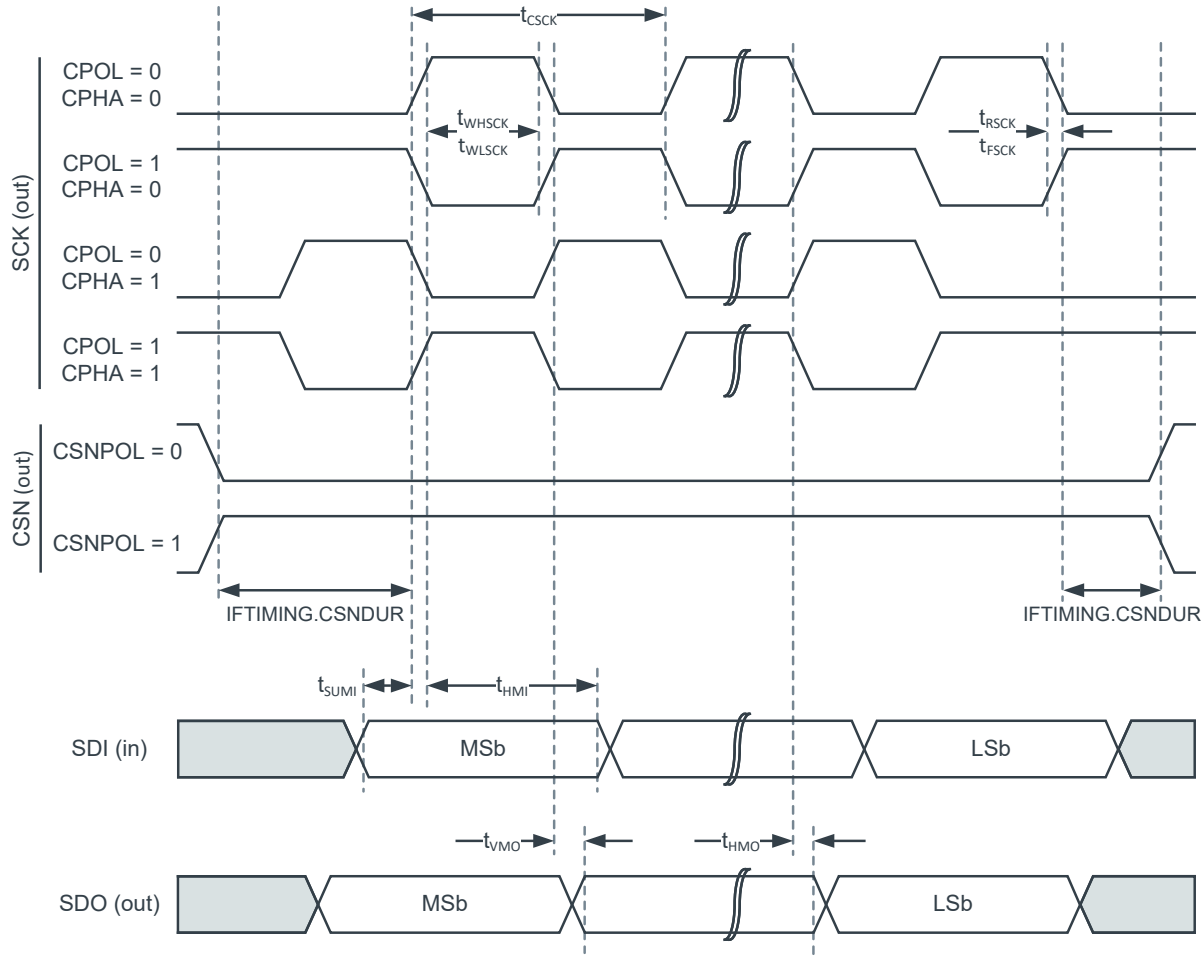

Figure 195: SPIM timing diagram

11.18.2 Timing specifications for GPIO port P0 using Standard drive strength

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SPIM,SUMI}$	SDI to CLK edge setup time	73			ns
$t_{SPIM,HMI}$	CLK edge to SDI hold time	0			ns
$t_{SPIM,VMO}$	CLK edge to SDO valid			28	ns
$t_{SPIM,HMO}$	SDO hold time after CLK edge	-8			ns

11.18.3 Timing specifications for GPIO port P0 using High drive strength

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SPIM,SUMI}$	SDI to CLK edge setup time	70			ns
$t_{SPIM,HMI}$	CLK edge to SDI hold time	0			ns
$t_{SPIM,VMO}$	CLK edge to SDO valid			28	ns
$t_{SPIM,HMO}$	SDO hold time after CLK edge	-6			ns