

#### 8.26.3.41 NORDIC.CACHE.DATATAGADDR

Address offset: 0x7CA

### Cache tag base address

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
ID	R/W	Field	Value ID	Value	Description																														
A	RW	VAL		0x0..0xFFFFFFFFC	Cache tag base address value  Defines where the tag cache region starts. The tag base address must be aligned with the data cache region size. The lower 2 bits are write ignored / read as zero, so the value must be rounded to a power of 2.																														

#### 8.26.3.42 NORDIC.CACHE.DATABASEADDR

Address offset: 0x7CB

### Cache data base address

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
<b>Reset 0x00000000</b>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	R/W	Field	Value ID	Value	Description																											
A	RW	VAL		0x0..0xFFFFFFF	Cache data base address value  Defines where the data cache region starts. The data base address must be aligned with the data cache region size. The lower 2 bits are write ignored / read as zero, so the value must be rounded to a power of 2.																											

### 8.26.3.43 NORDIC.RTPERIPHCTRL

Address offset: 0x7CC

## RT peripheral control