9.4 Layout

PCB design should start with design of the protection and filtering circuitry because ESD and EFT have a wide frequency bandwidth from approximately 3 MHz to 3 GHz. High frequency layout techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

9.4.1 Layout Guidelines

The layout example and information below are for a responder node with the following configuration: See Figure 9-14.

- Responder node
- SPI control
- WKRQ
- WAKE and High-side switch configured for cyclic sensing

The following are the layout guidelines based upon the provided configuration:

- **Pin 1 (V_{SUP}):** This is the supply pin for the device. A 100 nF decoupling capacitor (C1) should be placed as close to the device as possible. Other bulk decoupling capacitance should be considered.
- **Pin 2 (V_{CC}):** Output source, either 3.3 V or 5 V depending upon the version of the device and has a 10 µF decoupling capacitor (C2) to ground as close to the device as possible. This pin is connected to external circuitry for a limp home mode if the watchdog has timed out causing a reset
- **Pin 3 (nRST):** This pin connects to the processors and functions in one of two manners; as a reset pin for the TLIN1431x-Q1 or an indicator to the processor of an under-voltage and watchdog failure event. The pin has a 10 kΩ resistor (R1) pulled up to the processor I/O voltage rail.
- **Pin 4 (WDT/CLK):** In SPI control mode, this pin (CLK) is connected directly to the processor as the SPI CLK input to the TLIN1431x-Q1.
- **Pin 5 (nWDR/SDO):** In SPI control mode, this pin (SDO) is connected directly to the processor as the SPI serial data output from the TLIN1431x-Q1.
- **Pin 6 (WDI/SDI):** In SPI control mode, this pin (SDI) is connected directly to the processor as the SPI serial data input into the TLIN1431x-Q1.
- **Pin 7 (PIN/nCS):** For SPI control mode, this pin (nCS) should be connected directly to the processor as the SPI chip select to the TLIN1431x-Q1.
- **Pin 8 (EN/nINT):** In SPI control mode, this pin becomes an output interrupt pin that is provided to the processor.
- **Pin 9 (HSSC/FSO):** In SPI control mode, this pin (FSO) is connected directly to the processor, external transceiver or general purpose SBC as a selectable interrupt or control pin.
- **Pin 10 (PV):** This pin is connected directly to a processor ADC and has a 20 pF capacitor (C3) to GND.
- **Pin 11 (DIV_ON):** The pin is connected to a processor which controls when the V_{BAT} monitoring in the TLIN1431x-Q1 is enabled.
- **Pin 12 (TXD):** The TXD pin is the LIN transceiver input from the processors. A series resistor can be placed to limit the input current to the device in the event of an over-voltage on this pin. A capacitor to ground can be placed close to the input pin of the device to filter noise. These are system level dependent and not covered here as usually not needed.
- **Pin 13 (RXD):** The RXD is the LIN transceiver receive output to the processor. The pin is a push-pull output and can be connected directly to the processor without external pull-ups.
- **Pin 14 (GND):** This is the ground connection for the device. This pin should be tied to the ground plane through a short trace with the use of two vias to limit total return inductance.
- **Pin 15 (LIN):** This pin connects to the LIN bus. For responder nodes, a 220 pF capacitor (C4) to ground is implemented. For commander nodes, an additional series resistor and blocking diode should be placed between the LIN pin and the V_{SUP} pin.
- **Pin 16 (WKRQ/INH):** This pin can be the high-voltage inhibit output pin or the digital wake output pin. The example shows the pin configured as WKRQ which requires a 100 kΩ resistor (R2) to ground at power up.
- **Pin 17 (WAKE):** This pin connects to V_{SUP} through a resistor divider (R3 and R4) with the center tap connected to a switch to ground or V_{SUP} and is used as the local wake up pin. A 10 nF capacitor (C5) to