Register	Offset	TZ	Description
PUBLISH_TRIGGERED[n]	0x180		Publish configuration for event EVENTS_TRIGGERED[n]
INTEN	0x300		Enable or disable interrupt
INTENSET	0x304		Enable interrupt
INTENCLR	0x308		Disable interrupt
INTPEND	0x30C		Pending interrupts
DEBUGIF.DATA0	0x410		Abstract Data 0. Read/write data for argument 0
DEBUGIF.DATA1	0x414		Abstract Data 1. Read/write data for argument 1
DEBUGIF.DMCONTROL	0x440		Debug Module Control
DEBUGIF.DMSTATUS	0x444		Debug Module Status
DEBUGIF.HARTINFO	0x448		Hart Information
DEBUGIF.HALTSUM1	0x44C		Halt Summary 1
DEBUGIF.HAWINDOWSEL	0x450		Hart Array Window Select
DEBUGIF.HAWINDOW	0x454		Hart Array Window
DEBUGIF.ABSTRACTCS	0x458		Abstract Control and Status
DEBUGIF.ABSTRACTCMD	0x45C		Abstract command
DEBUGIF.ABSTRACTAUTO	0x460		Abstract Command Autoexec
DEBUGIF.CONFSTRPTR[n]	0x464		Configuration String Pointer [n]
DEBUGIF.NEXTDM	0x474		Next Debug Module
DEBUGIF.PROGBUF[n]	0x480		Program Buffer [n]
DEBUGIF.AUTHDATA	0x4C0		Authentication Data
DEBUGIF.HALTSUM2	0x4D0		Halt Summary 2
DEBUGIF.HALTSUM3	0x4D4		Halt Summary 3
DEBUGIF.SBADDRESS3	0x4DC		System Bus Addres 127:96
DEBUGIF.SBCS	0x4E0		System Bus Access Control and Status
DEBUGIF.SBADDRESS0	0x4E4		System Bus Addres 31:0
DEBUGIF.SBADDRESS1	0x4E8		System Bus Addres 63:32
DEBUGIF.SBADDRESS2	0x4EC		System Bus Addres 95:64
DEBUGIF.SBDATA0	0x4F0		System Bus Data 31:0
DEBUGIF.SBDATA1	0x4F4		System Bus Data 63:32
DEBUGIF.SBDATA2	0x4F8		System Bus Data 95:64
DEBUGIF.SBDATA3	0x4FC		System Bus Data 127:96
DEBUGIF.HALTSUM0	0x500		Halt summary 0
CPURUN	0x800		State of the CPU after a core reset
INITPC	0x808		Initial value of the PC at CPU start.

8.26.1.1 TASKS_TRIGGER[n] (n=16..22)

Address offset: 0x000 + (n × 0x4)

VPR task [n] register

If RTPs are not enabled: writes to registers 15..0 are ignored, other read/write accesses operate normally

If RTPs are enabled: reads or writes to these registers will be stalled if there is a simultaneous VPR CSR write access

to any CSR register.