Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				F E D C B B A A
Reset 0x8000002A				**1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 1 0**

ID	R/W	Field	Value ID	Value	Description
A	R	SECUREMAPPING			Read capabilities for TrustZone Cortex-M secure attribute
			NonSecure	0	This peripheral is always accessible as a non-secure peripheral
			Secure	1	This peripheral is always accessible as a secure peripheral
			UserSelectable	2	Non-secure or secure attribute for this peripheral is defined by the PERIPH[n].PERM register
			Split	3	This peripheral implements the split security mechanism.
B	R	DMA			Read the peripheral DMA capabilities
			NoDMA	0	Peripheral has no DMA capability
			NoSeparateAttribute	1	Peripheral has DMA and DMA transfers always have the same security attribute as assigned to the peripheral
			SeparateAttribute	2	Peripheral has DMA and DMA transfers can have a different security attribute than the one assigned to the peripheral
C	RW	SECATTR			Peripheral security mapping This bit has effect only if PERIPH[n].PERM.SECUREMAPPING is UserSelectable or Split
			Secure	1	Peripheral is mapped in secure peripheral address space
			NonSecure	0	If SECUREMAPPING == UserSelectable: Peripheral is mapped in non-secure peripheral address space. If SECUREMAPPING == Split: Peripheral is mapped in non-secure and secure peripheral address space.
D	RW	DMASEC			Security attribution for the DMA transfer This bit has effect only if PERIPH[n].PERM.SECATTR is set to secure and PERIPH[n].PERM.DMA is set to SeparateAttribute.
			Secure	1	DMA transfers initiated by this peripheral have the secure attribute set
			NonSecure	0	DMA transfers initiated by this peripheral have the non-secure attribute set
E	RW W1S	LOCK			Register lock
			Unlocked	0	This register can be updated
			Locked	1	The content of this register can not be changed until the next reset When Locked, it remains Locked until the next reset cycle.
F	R	PRESENT			Indicates if a peripheral is present with peripheral slave index n
			NotPresent	0	Peripheral is not present
			IsPresent	1	Peripheral is present

7.8.5.5.8 FEATURE.DPPIC.CH[n] (n=0..23)

Address offset: 0x680 + (n × 0x4)

Security configuration for channel n of DPPIC