8.13.14.37 PUBLISH_RXFRAMESTART

Address offset: 0x194

Publish configuration for event RXFRAMESTART

Bit number					31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
ID					B	A A A A A A A A
Reset 0x00000000					0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
ID	R/W	Field	Value ID	Value	Description	
A	RW	CHIDX		[0..255]	DPPI channel that event RXFRAMESTART will publish to	
B	RW	EN				
			Disabled	0	Disable publishing	
			Enabled	1	Enable publishing	

8.13.14.38 PUBLISH_RXFRAMEEND

Address offset: 0x198

Publish configuration for event RXFRAMEEND

Bit number					31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
ID					B	A A A A A A A A
Reset 0x00000000					0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
ID	R/W	Field	Value ID	Value	Description	
A	RW	CHIDX		[0..255]	DPPI channel that event RXFRAMEEND will publish to	
B	RW	EN				
			Disabled	0	Disable publishing	
			Enabled	1	Enable publishing	

8.13.14.39 PUBLISH_ERROR

Address offset: 0x19C

Publish configuration for event ERROR

Bit number					31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
ID					B	A A A A A A A A
Reset 0x00000000					0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
ID	R/W	Field	Value ID	Value	Description	
A	RW	CHIDX		[0..255]	DPPI channel that event ERROR will publish to	
B	RW	EN				
			Disabled	0	Disable publishing	
			Enabled	1	Enable publishing	

8.13.14.40 PUBLISH_RXERROR

Address offset: 0x1A8

Publish configuration for event RXERROR

NORDIC
SEMICONDUCTOR