

Contents

	Feature overview.	ii
1	Revision history.	3
2	About this document.	4
	2.1 Document status.	4
	2.2 Peripheral chapters.	4
	2.2.1 Peripheral naming conventions.	4
	2.2.2.1 Peripheral instantiation.	5
	2.3 Register overview table.	6
	2.4 Register tables.	6
	2.4.1 Fields and values.	6
	2.4.2 Permissions.	6
	2.5 Registers.	7
	2.5.1 DUMMY.	7
3	Product overview.	9
	3.1 Block diagram.	9
	3.2 Memory and package overview.	10
	3.3 Power domains.	11
	3.4 Address format.	11
	3.5 Memory.	13
	3.5.1 RAM — Random access memory.	13
	3.5.2 NVM — Non-volatile memory.	13
	3.5.3 Memory map.	14
	3.5.4 Instantiation.	15
4	Application core.	19
	4.1 Arm Cortex-M33 CPU.	19
	4.1.1 CPU.	19
	4.1.2 CPUC — CPU control.	20
	4.1.3 Arm Cortex-M33 Peripherals.	26
	4.2 Core components.	26
	4.2.1 AMBA interconnect (AMBIX).	26
	4.2.2 EasyDMA.	27
	4.2.3 CACHE — Instruction/data cache.	29
	4.2.4 FICR — Factory information configuration registers.	38
	4.2.5 MEMCONF — Memory configuration.	44
	4.2.6 RRAMC — Resistive random access memory controller.	47
	4.2.7 SICR — Secure information configuration region.	60
	4.2.8 SWI — Software interrupts.	60
	4.2.9 UICR — User information configuration registers.	61
5	Power and clock management.	67
	5.1 System ON mode.	67
	5.1.1 Sub-power modes.	67
	5.2 System OFF mode.	68
	5.2.1 Emulated System OFF mode.	68
	5.3 Power supply supervisors.	69