Figure 8-58. CRC_CNTL Register (continued)

R-0b	R/W-0b

Table 8-14. CRC_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	CRC_CNTL_RSVD	R	0b	CRC control reserved bits
0	CRC_EN	R/W	0b	CRC enable 0b = Disable 1b = Enable

8.6.5 CRC_POLY_SET (Address = Bh) [reset = 00h]

CRC_POLY_SET is shown Figure 8-59 and described in Table 8-15.

Return to Summary Table.

This register will set which polynomial will be set for CRC. Defaults to AutoSAR 8-bit 0x2F.

Figure 8-59. CRC_POLY_SET Register

7	6	5	4	3	2	1	0
RSVD							POLY_8_SET
R							R/W-0b

Table 8-15. CRC_POLY_SET Register Field Description

Bit	Field	Type	Reset	Description
7-1	RSVD	R	00h	Reserved
0	POLY_8_SET	R/W	0b	CRC polynomial select 0b = X^8 + X^5 + X^3 + X^2 + X + 1 (0x2F) 1b = X^8 + X^4 + X^3 + X^2 + 1 (0x1D SAE J1850)

8.6.6 Scratch_Pad_SPI Register (Address = Fh) [reset = 0h]

Scratch_Pad_SPI is shown in Figure 8-60 and described in Table 8-16.

Return to Summary Table.

Read and Write Test Register SPI

Figure 8-60. Scratch_Pad_SPI Register

7	6	5	4	3	2	1	0
Scratch_Pad							
R/W-0b							

Table 8-16. Scratch_Pad_SPI Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Scratch_Pad	R/W	0b	Read and Write Test Register SPI

8.6.7 WAKE_PIN_CONFIG1 Register (Address = 11h) [reset = 04h]

WAKE_PIN_CONFIG1 is shown in Figure 8-61 and described in Table 8-17.

Return to Summary Table.

Register to configure the behavior of the WAKE pin.

Figure 8-61. WAKE_PIN_CONFIG1 Register

7	6	5	4	3	2	1	0
WAKE_CONFIG		WAKE_STAT		WAKE_WIDTH_INVALID		WAKE_WIDTH_MAX	
R/W-00b		R/W0C/H-00b		R/W-01b		R/W-00b	