8.22.3 Task delays

After TIMER is started, the CLEAR, COUNT, and STOP tasks are guaranteed to take effect within one clock cycle of the PCLK.

8.22.4 Task priority

If the START task and the STOP task are triggered at the same time, meaning within the same period of PCLK, the STOP task is prioritized.

If one or more of the CAPTURE tasks and the CLEAR task are triggered at the same time, that is, within the same period of PCLK, the CAPTURE tasks are prioritized. This means that the CC registers will capture the counter value before the CLEAR tasks are triggered.

8.22.5 Registers

Instances

Instance	Domain	Base address	TrustZone			Split access	Description
			Map	Att	DMA		
TIMER00 : S TIMER00 : NS	GLOBAL	0x50055000 0x40055000	US	S	NA	No	Timer TIMER00
TIMER10 : S TIMER10 : NS	GLOBAL	0x50085000 0x40085000	US	S	NA	No	Timer TIMER10
TIMER20 : S TIMER20 : NS	GLOBAL	0x500CA000 0x400CA000	US	S	NA	No	Timer TIMER20
TIMER21 : S TIMER21 : NS	GLOBAL	0x500CB000 0x400CB000	US	S	NA	No	Timer TIMER21
TIMER22 : S TIMER22 : NS	GLOBAL	0x500CC000 0x400CC000	US	S	NA	No	Timer TIMER22
TIMER23 : S TIMER23 : NS	GLOBAL	0x500CD000 0x400CD000	US	S	NA	No	Timer TIMER23
TIMER24 : S TIMER24 : NS	GLOBAL	0x500CE000 0x400CE000	US	S	NA	No	Timer TIMER24