Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	H	H																	G	F				E				D		C	B	A
Reset 0x40001016	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**0**

ID	R/W	Field	Value ID	Value	Description
A	R	A			Atomic extension Indicates presence of standard A extension
			Disabled	0	
			Enabled	1	
B	R	B			Bit-Manipulation extension Indicates presence of standard B extension. Indicates BEXT parameter option
			Disabled	0	
			Enabled	1	
C	R	C			Compressed extension Indicates presence of standard C extension
			Disabled	0	
			Enabled	1	
D	R	E			RV32E base ISA Indicates presence of standard E extension
			Disabled	0	
			Enabled	1	
E	R	I			RV32I/64I/128I base ISA Indicates presence of standard I extension
			Disabled	0	
			Enabled	1	
F	R	M			Integer Multiply/Divide extension Indicates presence of standard M extension
			Disabled	0	
			Enabled	1	
G	R	N			User-level interrupts supported Indicates presence of standard N extension
			Disabled	0	
			Enabled	1	
H	R	MXL			Machine XLEN Encodes the native base integer ISA width. The MXL field may be writable in implementations that support multiple base ISA widths. The effective XLEN in M-mode, MXLEN, is given by the setting of MXL, or has a fixed value if misa is zero. The MXL field is always set to the widest supported ISA variant at reset
			XLEN32	1	XLEN is 32 bits
			XLEN64	2	XLEN is 64 bits
			XLEN128	3	XLEN is 128 bits

8.26.3.3 MTVEC

Address offset: 0x305

Machine Trap-Vector

Holds trap vector configuration, consisting of a vector base address (BASE) and a vector mode (MODE)