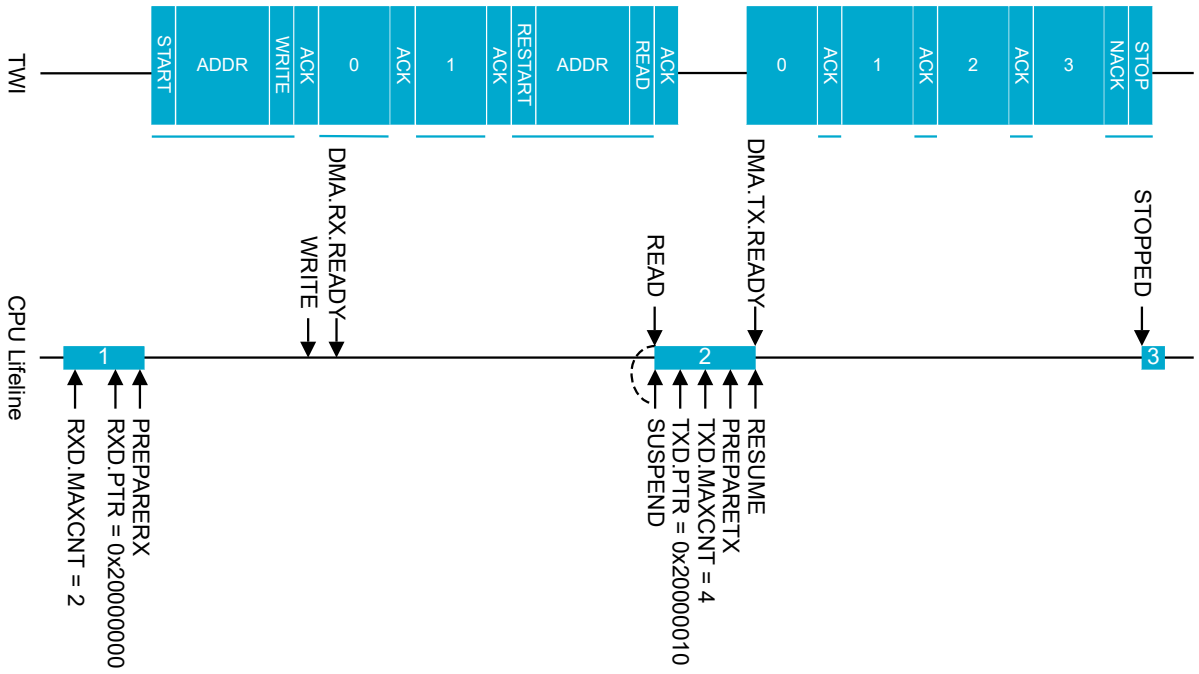


*Figure 156: Repeated start sequence*

In this example, the receiver does not know in advance what the controller wants to read. This information is in the first two received bytes of the write in the repeated start sequence. For the CPU to process the received data before TWIS replies to the read command, the SUSPEND task is triggered. This is enabled through a shortcut from the READ event generated when the read command is received. When the CPU has processed the incoming data and prepared the correct data response, the CPU will resume the transaction by triggering the RESUME task.

## 8.24.7 Terminate an ongoing TWI transaction

In some situations, an ongoing transaction must be terminated. This can happen when the external TWI controller is not responding correctly, for example.

To stop an ongoing transaction, trigger the STOP task. A STOPPED event will be generated when TWIS stops. It is not dependent on the STOP condition being generated on the TWI bus. TWIS will release the bus when it has stopped and returns to its IDLE state.

## 8.24.8 Low power

When the peripheral is not needed, stop and disable TWIS for lowest possible power consumption.

When the STOP task is sent, the software must wait until the STOPPED event is received before disabling the peripheral through the ENABLE register. If the peripheral is already stopped, the STOP task is not needed.

## 8.24.9 Target mode pin configuration

The SCL and SDA signals are mapped to physical pins using the PSEL.SCL and PSEL.SDA registers.

The PSEL.SCL and PSEL.SDA registers and their configurations are only used when TWIS is enabled, and retained while the device is in System ON mode. When the peripheral is disabled, the pins function as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register. Only configure PSEL.SCL and PSEL.SDA when TWIS is disabled.

When in System OFF mode or when TWIS is disabled, the TWIS pins must be configured in the GPIO peripheral as described in the following table to secure correct signal levels.