Register overview

Register	Offset	TZ	Description
OUT	0x000		Write GPIO port This register is retained.
OUTSET	0x004		Set individual bits in GPIO port
OUTCLR	0x008		Clear individual bits in GPIO port
IN	0x00C		Read GPIO port
DIR	0x010		Direction of GPIO pins This register is retained.
DIRSET	0x014		DIR set register
DIRCLR	0x018		DIR clear register
LATCH	0x020		Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE registers This register is retained.
DETECTMODE	0x024	S	Select between default DETECT signal behavior and LDETECT mode This register is retained.
PIN_CNF[n]	0x080		Pin n configuration of GPIO pin This register is retained.

8.8.8.1 OUT (Retained)

Address offset: 0x000

Write GPIO port

This register is retained.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A-f	RW	PIN[i] (i=0..31)			Pin i
			Low	0	Pin driver is low
			High	1	Pin driver is high

8.8.8.2 OUTSET

Address offset: 0x004

Set individual bits in GPIO port

Note: Read: reads value of OUT register.