6.8 AC Switching Characteristics (continued)

parameters valid over –40°C ≤ T_J ≤ 150 °C range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{MODE\_NOM\_STBY}$	SPI write to go to standby from normal mode				70	µs
t_{WKRQ_SLP}	Time WKRQ turns on after a wake event when device is in sleep mode	Dependent upon LDO turning on and ramp time. Time provided is based upon 1 µs ramp and LDO being at 2 V.	450			µs
t_{INH_SLP}	Time INH turns on after a wake event when device is in sleep mode				210	µs
$t_{INH\_NOM\_SLP}$	SPI write to go to sleep from normal mode and INH turns off				70	µs
$t_{WK\_WIDTH\_MIN}$	Minimum WAKE pin pulse width (SPI mode only) (2) (3) (4)	Minimum WAKE Pin pulse width Register 8'h11[3:2] = 00b; See Figure 8-46	10			ms
		Minimum WAKE Pin pulse width Register 8'h11[3:2] = 01b; See Figure 8-46	20			ms
		Minimum WAKE Pin pulse width Register 8'h11[3:2] = 10b; See Figure 8-46	40			ms
		Minimum WAKE Pin pulse width Register 8'h11[3:2] = 11b; See Figure 8-46	80			ms
$t_{WK\_WIDTH\_INVALID}$	Maximum Pulse width that is considered invalid (SPI mode only) (2) (3)	Maximum WAKE Pin pulse width that is considered invalid Register 8'h11[3:2] = 00b; See Figure 8-46			5	ms
		Maximum WAKE Pin pulse width that is considered invalid Register 8'h113:2] = 01b; See Figure 8-46			10	ms
		Maximum WAKE Pin pulse width that is considered invalid Register 8'h11[3:2] = 10b; See Figure 8-46			20	ms
		Maximum WAKE Pin pulse width that is considered invalid Register 8'h11[3:2] = 11b; See Figure 8-46			40	ms
$t_{WK\_WIDTH\_MAX}$	Maximum WAKE pin pulse width to be considered valid (SPI mode only) (2)	Maximum WAKE Pin pulse window Register 8'h11[1:0] = 00b; See Figure 8-46	750		950	ms
		Maximum WAKE Pin pulse window Register 8'h11[1:0] = 01b; See Figure 8-46	1000		1250	ms
		Maximum WAKE Pin pulse window Register 8'h11[1:0] = 10b; See Figure 8-46	1500		1875	ms
		Maximum WAKE Pin pulse window Register 8'h11[1:0] = 11b; See Figure 8-46	2000		2500	ms
t_{WK_CYC}	Sampling window for cyclic sensing wake; Standby or Sleep mode; see Figure 8-49	Register 8'h12[5] = 0	10	30	40	µs
		Register 8'h12[5] = 1	60	75	90	µs
Fast Mode						
DR	Data Rate	5.5 V ≤ V_{SUP} ≤ 18 V, R_{LIN} = 500 Ω and $C_{LIN(bus)}$ = 600 pF			200	kbps
t_{rx_pdr} t_{rx_pdf}	Receiver rising/falling propagation delay time (ISO/DIS 17987 Param 31)	R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF (See Figure 7-3, Figure 7-4			5	µs
$t_{txr/f}$	LIN transmitter rise and fall time	5.5 V ≤ V_{SUP} ≤ 18 V, R_{LIN} = 500 Ω and $C_{LIN(bus)}$ = 600 pF, 80%/20%			1.5	µs
t_{FM_CHANGE}	Fast mode determination time for entering or leaving	Based upon EN and TXD voltage levels	70	90	110	µs
t_{FMTXD}	TXD pin pulse width to enter fast mode	Pulse must start after t_{EN} and finish before t_{FM_CHANGE}	5		25	µs
SPI Switching Characteristics						
f_{SCK}	SCK, SPI clock frequency (1)				4	MHz
t_{SCK}	SCK, SPI clock period (1)	See Figure 7-7	250			ns
t_{RSCK}	SCK rise time (1)	See Figure 7-7			40	ns
t_{FSCK}	SCK fall time (1)	See Figure 7-7			40	ns
t_{SCKH}	SCK, SPI clock high (1)	See Figure 7-7	125			ns