Table 8-8. CRC8 SAE J1850 (continued)

SPI Transactions	
Polynomial	1Dh
Initial value	FFh
Input data reflected	No
Result data reflected	No
XOR value	FFh
Check	4Bh
Magic Check	C4h

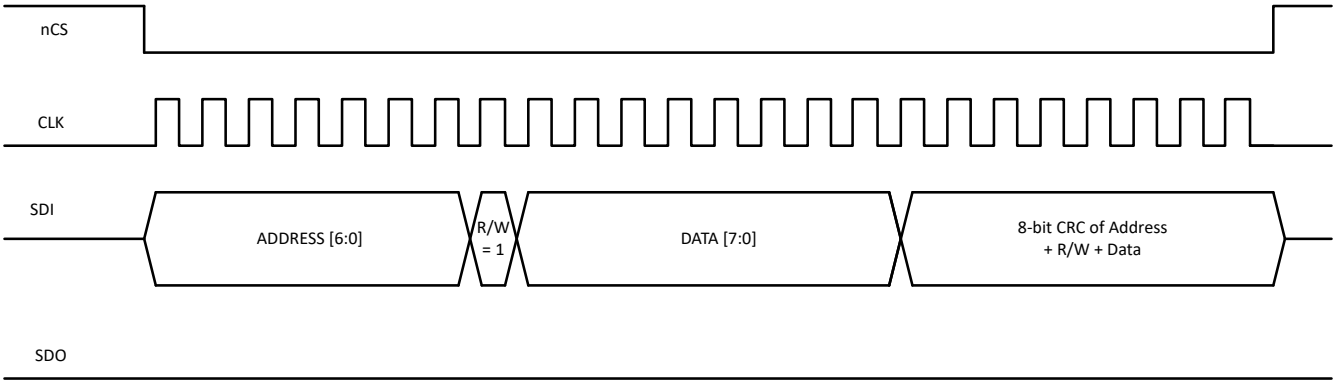

Figure 8-52. CRC SPI Write

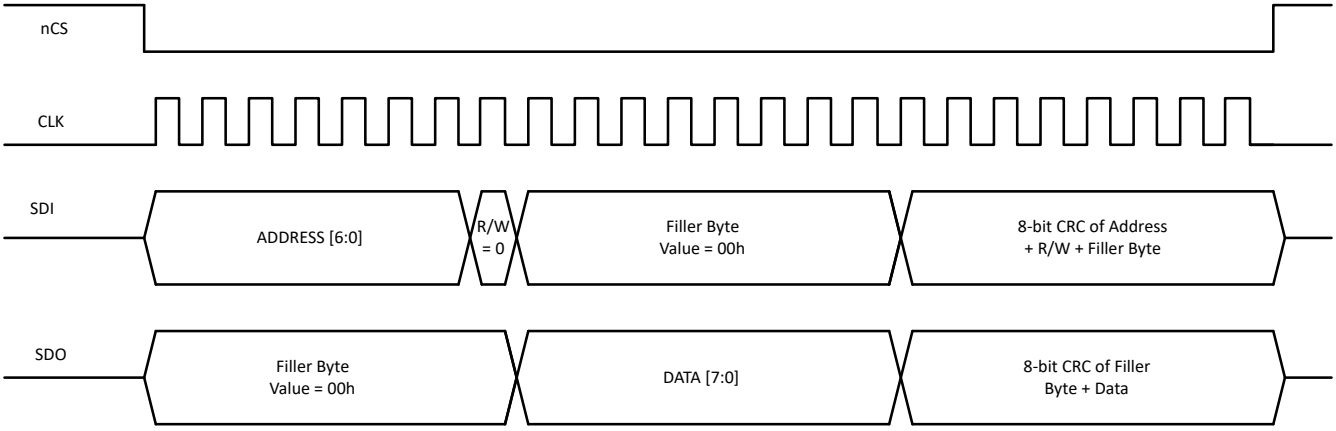

Figure 8-53. CRC SPI Read

8.5.1.2 Chip Select Not (nCS)

This input pin is used to select the device for a SPI transaction. The pin is active low, so while nCS is high the SPI Data Output (SDO) pin of the device is high impedance allowing an SPI bus to be designed. When nCS is low, the SDO driver is activated and communication may be started. The nCS pin is held low for a SPI transaction.

8.5.1.3 Serial Clock Input (CLK)

This input pin is used to input the clock for the SPI to synchronize the input and output serial data bit streams. The SPI Data Input is sampled on the rising edge of CLK and the SPI Data Output is changed on the falling edge of the CLK. See Figure 8-54 .