| Register | Offset | TZ | Description |
|---|---|---|---|
| PUBLISH_DMA.SEQ[n].BUSERROR | 0x1AC | | Publish configuration for event BUSERROR |
| PUBLISH_COMPAREMATCH[n] | 0x1BC | | Publish configuration for event COMPAREMATCH[n] |
| SHORTS | 0x200 | | Shortcuts between local events and tasks |
| INTEN | 0x300 | | Enable or disable interrupt |
| INTENSET | 0x304 | | Enable interrupt |
| INTENCLR | 0x308 | | Disable interrupt |
| INTPEND | 0x30C | | Pending interrupts |
| ENABLE | 0x500 | | PWM module enable register |
| MODE | 0x504 | | Selects operating mode of the wave counter |
| COUNTERTOP | 0x508 | | Value up to which the pulse generator counter counts |
| PRESCALER | 0x50C | | Configuration for PWM_CLK |
| DECODER | 0x510 | | Configuration of the decoder |
| LOOP | 0x514 | | Number of playbacks of a loop |
| IDLEOUT | 0x518 | | Configure the output value on the PWM channel during idle |
| SEQ[n].REFRESH | 0x528 | | Number of additional PWM periods between samples loaded into compare register |
| SEQ[n].ENDDELAY | 0x52C | | Time added after the sequence |
| PSEL.OUT[n] | 0x560 | | Output pin select for PWM channel n |
| DMA.SEQ[n].PTR | 0x704 | | RAM buffer start address |
| DMA.SEQ[n].MAXCNT | 0x708 | | Maximum number of bytes in channel buffer |
| DMA.SEQ[n].AMOUNT | 0x70C | | Number of bytes transferred in the last transaction, updated after the END event. |
| DMA.SEQ[n].CURRENTAMOUNT | 0x710 | | Number of bytes transferred in the current transaction |
| DMA.SEQ[n].TERMINATEONBUSERROR | 0x71C | | Terminate the transaction if a BUSERROR event is detected. |
| DMA.SEQ[n].BUSERRORADDRESS | 0x720 | | Address of transaction that generated the last BUSERROR event. |

### 8.15.5.1 TASKS_STOP

Address offset: 0x004

Stops PWM pulse generation on all channels at the end of current PWM period, and stops sequence playback

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| ID | R/W | Field | Value ID | Value | Description |
|---|---|---|---|---|---|
| A | W | TASKS_STOP | | | Stops PWM pulse generation on all channels at the end of current PWM period, and stops sequence playback |
| | | | Trigger | 1 | Trigger task |

### 8.15.5.2 TASKS_NEXTSTEP

Address offset: 0x008

Steps by one value in the current sequence on all enabled channels if DECODER.MODE=NextStep. Does not cause PWM generation to start if not running.

| Bit number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | A |
| **Reset 0x00000000** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

| ID | R/W | Field | Value ID | Value | Description |
|---|---|---|---|---|---|
| A | W | TASKS_NEXTSTEP | | | Steps by one value in the current sequence on all enabled channels if DECODER.MODE=NextStep. Does not cause PWM generation to start if not running. |
| | | | Trigger | 1 | Trigger task |