

**Note:** This register can be updated while a transfer is in progress, but the new value will not take effect until a match has been found or the transfer is done. That makes it possible to write a new set of match words which will be searched for immediately after the event triggers.

## 8.19.8.42 DMA.TX.PTR

Address offset: 0x73C

### RAM buffer start address

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
<b>Reset 0x20000000</b>	<b>0</b>	<b>0</b>	<b>1</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>		
ID	R/W	Field	Value ID	Value		Description																										
A	RW	PTR				RAM buffer start address for this EasyDMA channel. This address is a word aligned Data RAM address.																										

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 8.19.8.43 DMA.TX.MAXCNT

Address offset: 0x740

Maximum number of bytes in channel buffer

### 8.19.8.44 DMA-TX-AMOUNT

Address offset: 0x744

Number of bytes transferred in the last transaction, updated after the END event.

Also updated after each MATCH event.