If the CPU tries to acquire the semaphore while it is assigned to SPIS, an immediate handover will not be granted. After the granted transaction is complete, SPIS releases the semaphore to the CPU. If the END_ACQUIRE shortcut is enabled and the CPU has triggered the ACQUIRE task during a granted transaction, only one ACQUIRE request will be served following the END event.

8.20.6 Pin configuration

The CSN, SCK, SDI, and SDO signals associated with SPIS are mapped to physical pins according to the configuration specified in the PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers, respectively. If the CONNECT field is set to `Disconnected`, the associated SPIS signal will not be connected to any physical pins.

These registers and their configurations are only used when SPIS is enabled, and retained as long as the device is in System ON mode. See POWER — Power control on page 92 for more information about power modes. When the peripheral is disabled, the pins behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register. Only configure PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO when SPIS is disabled.

Before enabling SPIS, the pins used by SPIS must be configured in the GPIO peripheral as described in GPIO configuration before enabling peripheral on page 615. This ensures that the pins are driven correctly if SPIS becomes temporarily disabled, or if the device enters System OFF mode. This configuration must be retained in the GPIO for the selected pins to be recognized by an external SPI controller.

The SDO line is set `HIGH` as long as SPIS is not selected with CSN.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

SPI signal	SPI pin	Direction	Output value	Comment
CSN	As specified in PSEL.CSN	Input	Not applicable	
SCK	As specified in PSEL.SCK	Input	Not applicable	
SDI	As specified in PSEL.MOSI	Input	Not applicable	
SDO	As specified in PSEL.MISO	Input	Not applicable	Emulates that SPIS is not selected.

Table 63: GPIO configuration before enabling peripheral