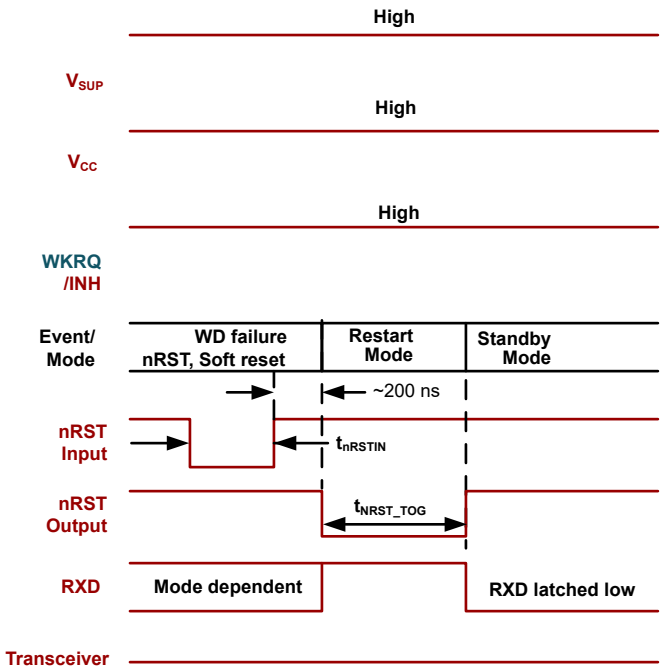

Note

- A watchdog failure, soft reset or nRST event resets t_{NRST_TOG} to default value of typically 2 ms
- The typical time between the release of a nRST input pulse for device to enter restart mode is ~ 200 ns

Figure 8-40. Entering Restart Mode

8.4.6.1 Restart Counter

This counter is programed by register 8'h28[7:4] which sets the number of times restart can be entered before transitioning to sleep or fail-safe mode, up to 14 times but should be programmed for greater than 1 to avoid possible loops. The default value is 4. Register 8'h28[3:0] is the counter. To prevent the transition to sleep or fail-safe mode, the counter should be cleared periodically. Entering sleep mode or fail-safe mode due to a meeting the restart counter automatically clears the restart counter.

8.4.6.2 nRST Behavior in Restart Mode

The nRST output pin behavior depends upon the reason the device entered restart mode. When entered from other modes due to a watchdog failure, soft reset or an external nRST toggle, the nRST pin is pulled low for t_{nRST_TOG} which is a default pulse width of 2 ms. This pulse width can be configured to 15 ms by changing register 8'h29[5] = 1b. In pin control, the pulse width on nRST is always nominally 15 ms for a watchdog failure. Once the timer expires, the device enters standby mode. From power up, sleep and certain fail-safe modes, the nRST behaves like the UV_{CC} event, pulling nRST low until V_{CC} > UV_{CC} and t_{RSTN_act} times out. See Figure 8-41 on how the nRST pin behaves when entering restart mode.

The nRST pin is also a TLIN1431x-Q1 reset input which transitions the device into restart mode when the pin is pulled low for t_{nRSTIN}.