The following figure illustrates how to assign a pin to a peripheral that has dedicated pins, or a subsystem such as trace and debug.

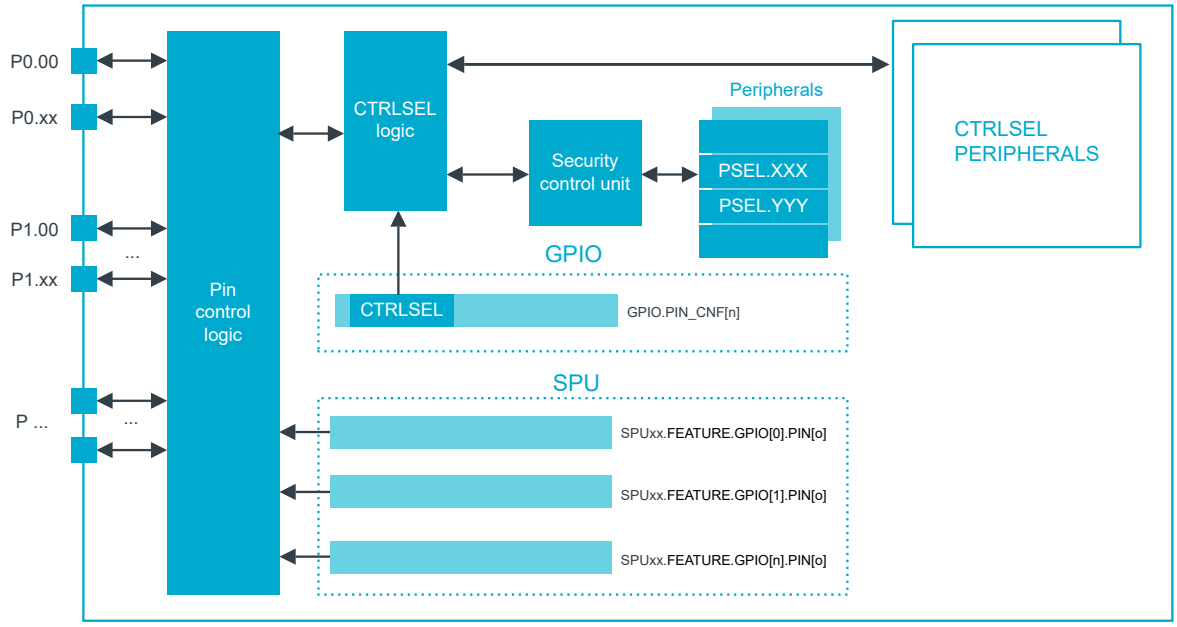

Figure 62: Pin access using CTRLSEL

For details on pin security, see Security on page 123.

Note: CTRLSEL must be configured before any pins are used, otherwise glitches on the GPIO pins of the corresponding port can occur.

8.8.5 Clock pins

The device has dedicated clock pins. Some peripherals, such as SPI, TWI, and TRACE, have clock signals.

The dedicated clock pins are optimized to ensure correct timing between the clock and data signals for these peripherals. All peripherals that have clock signals must use these pins. See Pin assignments on page 859 for the full list.

The data signal associated with the peripheral must use pins close to the clock pin. This ensures that the internal paths from the peripheral to the pin have the same delay, so that the data and clock signals reach the pins at the same time.

For high-speed signals, the printed circuit board (PCB) layout must use short PCB traces of identical length. This reduces delays and ensures the same delay on the clock and data path.

8.8.6 Fast port control

GPIOHSPADCTRL.BIAS.HSBIAS configures the slew rate of the GPIO pins on P2 in the E0 and E1 drive mode.

A higher slew rate is mandatory for fast signal switching and timing accuracy, helping to maintain correct data transfer at higher speeds. A lower slew rate helps minimize EMI, signal overshoot, and noise for better signal quality.