

Register	Offset	TZ	Description
IKG.START	0x3000		Start register.
IKG.STATUS	0x3004		Status register.
IKG.INITDATA	0x3008		InitData register.
IKG.NONCE	0x300C		Nonce register.
IKG.PERSONALISATIONSTRING	0x3010		Personalisation String register.
IKG.RESEEDINTERVALLSB	0x3014		Reseed Interval LSB register.
IKG.RESEEDINTERVALMSB	0x3018		Reseed Interval MSB register.
IKG.PKECONTROL	0x301C		PKE Control register.
IKG.PKECOMMAND	0x3020		PKE Command register.
IKG.PKESTATUS	0x3024		PKE Status register.
IKG.SOFRST	0x3028		SoftRst register.
IKG.HWCONFIG	0x302C		HwConfig register.

7.8.1.7.1 CRYPTMSTRDMA.FETCHADDRLSB

Address offset: 0x000

Fetch Address Least Significant Word

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID	R/W	Field	Value ID	Value	Description
A	RW	FETCHADDRLSB			Address
					In direct mode this register is written by SW with the address of the data block. In Scatter-gather mode this register is written by SW with the address of the first descriptor, and subsequently updated by the hardware after each processed descriptor.

7.8.1.7.2 CRYPTMSTRDMA.FETCHADDRMSB

Address offset: 0x004

Fetch Address Most Significant Word

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID	R/W	Field	Value ID	Value	Description
A	RW	FETCHADDRMSB			As the platform has 32bit addresses this register and ADDRMSB registers both give access to the same 32-bit register.

7.8.1.7.3 CRYPTMSTRDMA.FETCHLEN

Address offset: 0x008

Fetch DMA Length (only used in direct mode)