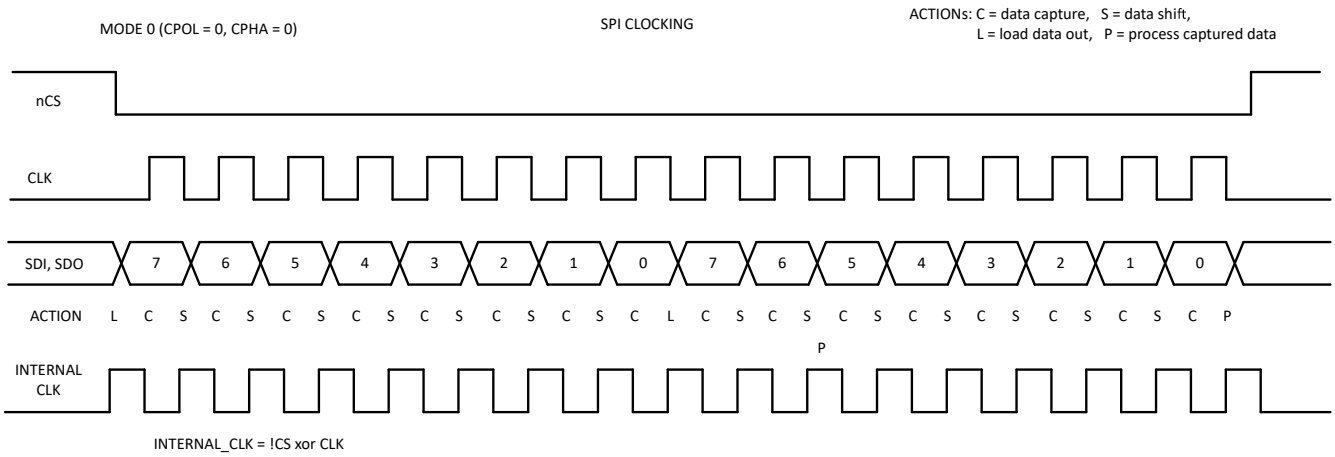

Figure 8-54. SPI Clocking

8.5.1.4 Serial Data Input (SDI)

This input pin is used to shift data into the device. Once the SPI is enabled by a low on nCS, the SDI samples the input shifted data on each rising edge of the SPI clock (SCK). The data is shifted into an 8-bit shift register. After eight (8) clock cycles and shifts, the addressed register is read giving the data to be shifted out on SDO. After eight clock cycles, the shift register is full and the SPI transaction is complete. If the command code is a write, the new data is written into the addressed register. When nCS has a falling edge, there will be 16-bits (CRC disabled) or 24-bits (CRC enabled) shifted in by CLK, at which time the nCS has a rising edge to deselect the device. 16 Clock cycles are required to shift 16-bits (CRC disabled) and 24 clock cycles for 24-bits (CRC enabled) during one SPI transaction (nCS is low). If more or less clock cycles than these are used, the SPIERR flag will be set. If CRC was enabled the CRCERR flag will be set. When writing to the device, any transaction other than 16 or 24 clock cycles could result in behavior that is outside of the specification.

8.5.1.5 Serial Data Output (SDO)

This pin is high impedance until the SPI output is enabled via nCS. Once the SPI is enabled by a low on nCS and a read command given, on the first falling edge of CLK, the shifting out of the data with each falling edge on CLK until all 8 bits have been shifted out the shift register.

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