

Bit number					31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID					N	N	N							M	L	K	J	J	J	I	H	G	G	G	F	F	F	F	F	F	F	E	D	C	B	A
Reset 0x20000000					0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D	R/W	Field	Value ID	Value	Description																															
M	R	SBBUSYERROR			Set when the debugger attempts to read data while a read is in progress, or when the debugger initiates a new access while one is already in progress (while sbbusy is set). It remains set until it’s explicitly cleared by the debugger. While this field is set, no more system bus accesses can be initiated by the Debug Module.																															
			noerror	0	No error.																															
			error	1	Debugger access attempted while one in progress.																															
N	R	SBVERSION																																		
			version0	0	The System Bus interface conforms to mainline drafts of thia RISC-V External Debug Support spec older than 1 January, 2018.																															
			version1	1	The System Bus interface conforms to RISC-V External Debug Support version 0.14.0-DRAFT. Other values are reserved for future versions.																															

8.26.1.28 DEBUGIF.SBADDRESS0

Address offset: 0x4E4

System Bus Address 31:0

If sbasize is 0, then this register is not present. When the system bus master is busy, writes to this register will set sbbusyerror and don't do anything else. If sberror is 0, sbbusyerror is 0, and sbreadonaddr is set then writes to this register start the following: 1. Set sbbusy. 2. Perform a bus read from the new value of sbaddress. 3. If the read succeeded and sbautoincrement is set, increment sbaddress. 4. Clear sbbusy.

Bit number					31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID					A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000					0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	R/W	Field		Value ID	Value					Description																										
A	R	ADDRESS								Accesses bits 31:0 of the physical address in sbaddress.																										

8.26.1.29 DEBUGIF.SBADDRESS1

Address offset: 0x4E8

System Bus Address 63:32

If sbasize is less than 33, then this register is not present. When the system bus master is busy, writes to this register will set sbbusyerror and don't do anything else.

Bit number					31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
ID					A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
Reset 0x00000000					0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
ID	R/W	Field	Value ID	Value	Description																																	
A	R	ADDRESS			Accesses bits 63:32 of the physical address in sbaddress (if the system address bus is that wide).																																	

8.26.1.30 DEBUGIF.SBADDRESS2

Address offset: 0x4EC

System Bus Address 95:64