Figure 8-3 shows a Commander Node configuration and how the voltage levels are defined.

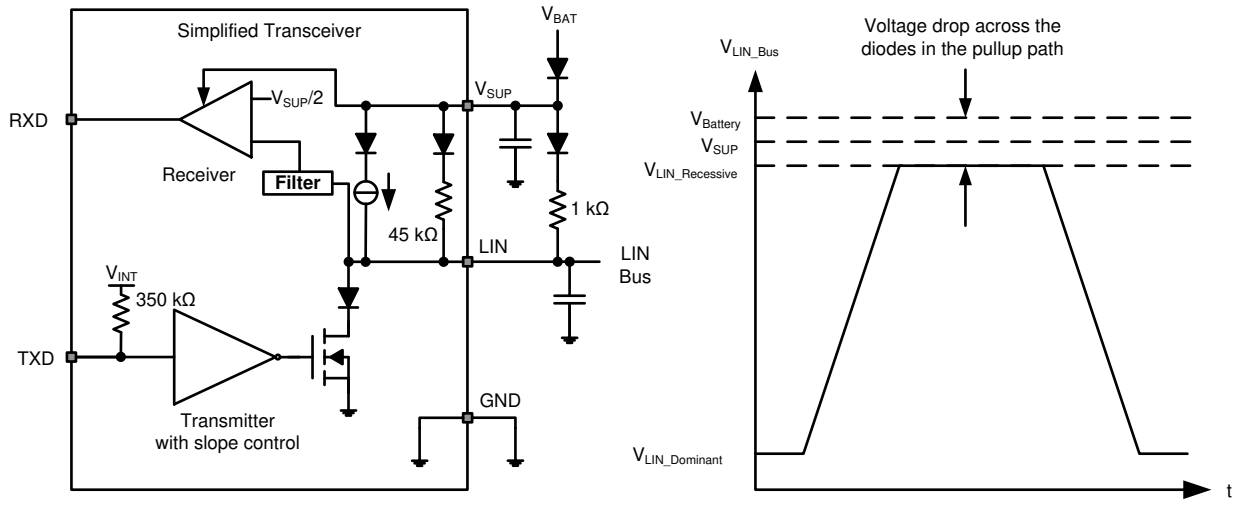

Figure 8-3. Commander Node Configuration with Voltage Levels

8.3.2 TXD (Transmit Input and Output)

TXD is the interface to the node processor LIN protocol controller that is used to control the state of the LIN output. When TXD is low, the LIN output is dominant (near ground). When TXD is high, the LIN output is recessive (near V_{SUP}). See Figure 8-3. The TXD input structure is compatible with processors with 3.3 V and 5 V logic I/O. TXD has an internal pull-up resistor to an internal voltage rail that either matches the processor I/O voltage rail or the LDO output rail, V_{CC} which is determined by the state of pin 7 at power up. The LIN bus is protected from being stuck dominant through a system failure driving TXD low through the dominant state timeout timer. The TXD pin is also used to help determine what mode to enter in pin control mode.

8.3.3 RXD (Receive Output)

RXD is the interface to the processors LIN protocol controller or SCI and UART, which reports the state of the LIN bus voltage. LIN recessive (near V_{SUP}) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. This device architecture allows the device to be used with 3.3 V and 5 V I/O processors. The RXD pin is a push-pull buffer and as such an external pull-up is not needed. In restart mode, the RXD pin is driven high. When V_{CC} > UV_{CC} for t_{RSTN_act}, the device automatically transitions to standby mode causing RXD is then pulled low to indicate a wake-up request. The RXD pin can be programmed to toggle low or high to indicate a wake up request with a pulse width of t_{TOGGLE}, see Figure 7-6 as an example of this feature.

8.3.4 WAKE (High Voltage Local Wake Up Input)

WAKE pin is used for a high voltage device local wake up (LWU). This function is explained further in Local Wake Up (LWU) via WAKE Terminal section. The pin is both rising and falling edge trigger, meaning it recognizes a LWU on either edge of WAKE pin transition. The pin can be configured to accept a pulse, see Figure 8-46 for timing diagram of this behavior. WAKE pin is also used as part of the cyclic sensing wake, see Cyclic Sense Wake. Registers WAKE_PIN_CONFIG1 Register (Address = 11h) [reset = 04h] and WAKE_PIN_CONFIG2 Register (Address = 12h) [reset = 2h] provide the various configurations for the WAKE pin.

8.3.5 WDT or CLK (Pin Programmable Watchdog Delay Input or SPI Clock)

When configured for pin control, the WDT or CLK pin becomes the pin programmable watchdog delay input, WDT. This pin sets the upper boundary of the window watchdog. It can be connected to V_{CC}, connected to GND, or left floating. When connected directly to V_{CC} or GND or left open, the window frame takes on one of three value ranges: GND – 32 ms to 48 ms, V_{CC} – 480 ms to 720 ms or left open – 4.8 s to 7.2 s. The closed versus open windows are based upon 50%/50%.