

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|-----|------------------|----------|-------|----|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| Reset 0x00000000 | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID | R/W | Field | Value ID | Value | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A-f | RW | PIN[i] (i=0..31) | | | | Pin i | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | Pin set as input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | Pin set as output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

8.8.8.6 DIRSET

Address offset: 0x014

DIR set register

Note: Read: reads value of DIR register.

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|-----|------------------|----------|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ID | | | | f e d c b a Z Y X W V U T S R Q P O N M L K J I H G F E D C B A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset 0x00000000 | | | | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ID | R/W | Field | Value ID | Value | | | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A-f | RW | PIN[i] (i=0..31) | | | | | | Set as output pin i | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | W1S | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | | | | Read: pin set as input | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | | | | Read: pin set as output | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | | | | Write: writing a '1' sets pin to output; writing a '0' has no effect | | | | | | | | | | | | | | | | | | | | | | | | | | | |

8.8.8.7 DIRCLR

Address offset: 0x018

DIR clear register

Note: Read: reads value of DIR register.

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|-----|------------------|----------|-------|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|
| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | |
| ID | | | | f | e | d | c | b | a | Z | Y | X | W | V | U | T | S | R | Q | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A | | | |
| Reset 0x00000000 | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| ID | R/W | Field | Value ID | Value | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A-f | RW | PIN[i] (i=0..31) | | | Set as input pin i | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | W1C | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Input | 0 | Read: pin set as input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Output | 1 | Read: pin set as output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Clear | 1 | Write: writing a '1' sets pin to input; writing a '0' has no effect | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

8.8.8.8 LATCH (Retained)

Address offset: 0x020

Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE registers

This register is retained.