| Register | Offset | Description |
|---|---|---|
| NORDIC.DIROUTB | 0xBC7 | Concatenation of DIRB and OUTB |
| NORDIC.OUTBRB | 0xBC8 | Byte reversed register OUTB |
| NORDIC.OUTBRW | 0xBC9 | Word reversed register OUTB |
| NORDIC.INBRB | 0xBCA | Byte reversed register INB |
| NORDIC.SHIFTCTRLB | 0xBCB | Buffered IO shift control |
| NORDIC.SHIFTCNTIN | 0xBCD | Number of frames to be shifted from INB before new data is required |
| NORDIC.SHIFTCNTOUT | 0xBCE | Number of frames to be shifted to OUTB before new data is required |
| NORDIC.SHIFTCNTB | 0xBCF | Buffered SHIFTCNTOUT and SHIFTCNTIN register |
| NORDIC.OUTTGL | 0xBD0 | GPIO Output Toggle |
| NORDIC.DIRTGL | 0xBD1 | GPIO pin Direction Toggle |
| NORDIC.OUTBTGL | 0xBD2 | Buffered GPIO Output Toggle |
| NORDIC.DIRBTGL | 0xBD3 | Buffered GPIO pin Direction Toggle |
| NORDIC.DIROUTTGL | 0xBD4 | DIROUT Toggle |
| NORDIC.DIROUTBTGL | 0xBD5 | DIROUTB Toggle |
| NORDIC.OUTBS | 0xBD8 | Buffered GPIO Output Dirty Status |
| NORDIC.DIRBS | 0xBD9 | Buffered GPIO pin Direction Dirty Status |
| NORDIC.DIROUTBS | 0xBDA | Combination of DIRB and OUTB Dirty Status |
| NORDIC.OUTBD | 0xBE0 | Concatenation of Buffered GPIO Output and GPIO Output |
| NORDIC.OUTBDTGL | 0xBE1 | OUTBD Toggle |
| NORDIC.OUTBDS | 0xBE2 | OUTBD Dirty Status |
| NORDIC.OUTMODE | 0xBE3 | Serial output mode |
| NORDIC.OUTMODEB | 0xBE4 | Buffered OUTMODE register |
| NORDIC.INMODEB | 0xBE5 | Buffered INMODE register |
| NORDIC.INB | 0xBE6 | Buffered GPIO input |

## 8.26.3.1 MSTATUS

Address offset: 0x300

Machine Status

Keeps track of and controls the hart current operating state. In VPR it only contains/controls information of machine privileged mode interrupts, see MIE and MPIE

| Bit number | | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID | | | | | | | | | | | | | | | | | | | | | | | | C | C | | | | B | | | | A | | | |
| **Reset 0x00001800** | | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| ID | R/W | Field | Value ID | Value | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | MIE | | | global interrupt enable for machine privilege mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | MPIE | | | Exists to support nested traps. Value of the interrupt-enable bit active prior to the trap for machine privilege mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | R | MPP | | | Exists to support nested traps. Value of the privlege mode prior to the trap for machine privilege mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 8.26.3.2 MISA

Address offset: 0x301

Machine ISA

Reports the ISA supported by the hart