Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	A A A A A A A A A A A A A A A A
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	R	INFO			Trigger Info value One bit for each possible type enumerated in tdata1. Bit N corresponds to type N. If the bit is set, then that type is supported by the currently selected trigger. If the currently selected trigger doesn't exist, this field contains 1. If type is not writable, this register may be unimplemented, in which case reading it causes an illegal instruction exception. In this case the debugger can read the only supported type from tdata1.

8.26.3.18 TCONTROL

Address offset: 0x7A5

Trigger Control

This optional register is one solution to a problem regarding triggers with action=0 firing in M-mode trap handlers

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	B A
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW	MTE			Mode Trigger Enable
			DONTMATCH	0	Triggers with action=0 do not match/fire while the hart is in M-mode
			MATCH	1	Triggers do match/fire while the hart is in M-mode. When a trap into M-mode is taken, mte is set to 0. When mret is executed, mte is set to the value of mpte
B	RW	MPTE			Mode Previous Trigger Enable When a trap into M-mode is taken, mpte is set to the value of mte

8.26.3.19 DCSR

Address offset: 0x7B0

Debug Control and Status

This register is only accesible from debug mode

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	F F F F E D C C C B A A
Reset 0x40000003	**0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1**

ID	R/W	Field	Value ID	Value	Description
A	R	PRV			Privilege level Contains the privilege level the hart was operating in when Debug Mode was entered. VPR only supports Machine Privilege Level.
			MACHINE	3	