

Publish configuration for event **ERROR**

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				B																								A A A A A A A A							
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value				Description																											
A	RW	CHIDX		[0..255]				DPPI channel that event <b>ERROR</b> will publish to																											
B	RW	EN																																	
			Disabled	0				Disable publishing																											
			Enabled	1				Enable publishing																											

## 8.4.7.11 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				B A																															
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value	Description																														
A	RW	END  W1S			Write '1' to enable interrupt for event <span>END</span>																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														
B	RW	ERROR  W1S			Write '1' to enable interrupt for event <span>ERROR</span>																														
			Set	1	Enable																														
			Disabled	0	Read: Disabled																														
			Enabled	1	Read: Enabled																														

## 8.4.7.12 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID			B A																															
Reset 0x00000000			0 0																															
ID	R/W	Field	Value ID	Value	Description																													
A	RW	END  W1C			Write '1' to disable interrupt for event <span>END</span>																													
			Clear	1	Disable																													
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													
B	RW	ERROR  W1C			Write '1' to disable interrupt for event <span>ERROR</span>																													
			Clear	1	Disable																													
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													