8.27.3 Watchdog reset

A TIMEOUT event automatically leads to a watchdog reset.

If the watchdog is configured to generate an interrupt on the TIMEOUT event, the watchdog reset is postponed by two 32.768 kHz clock cycles after the TIMEOUT event is generated. Once the TIMEOUT event is generated, and unless the watchdog is stopped, the impending watchdog reset will occur.

The watchdog can be reset from several reset sources, see Reset behavior on page 103. After a reset, the watchdog configuration registers are available for configuration.

See RESET — Reset control on page 101 for more information about reset sources.

The TIMEOUT event will also generate NMI interrupt, when NMI interrupt is supported. See the the instance's configuration in Instantiation on page 216 to see if NMI is supported.

8.27.4 Stopping the watchdog

By default, the watchdog cannot be stopped. It is possible to configure the watchdog to allow the STOP task.

To stop the watchdog, perform the following steps.

1. Set the CONFIG register's STOPEN field to `Enable` during watchdog configuration.
2. Write the special value 0x6E524635 to the TSEN register.
3. Invoke the STOP task.

When these conditions are met, the watchdog is stopped and a STOPPED event is issued.

When the watchdog is stopped, its configuration registers CRV, RREN, and CONFIG are no longer blocked.

> **Note:** It is recommended to write zeros to TSEN on page 813 after the watchdog has stopped, to avoid runaway code triggering the STOP task.

8.27.5 Registers

Instances

Instance	Domain	Base address	TrustZone			Split access	Description
			Map	Att	DMA		
WDT30	GLOBAL	0x50108000	HF	S	NA	No	Watchdog timer WDT30
WDT31 : S WDT31 : NS	GLOBAL	0x50109000 0x40109000	US	S	NA	No	Watchdog timer WDT31

Configuration

Instance	Domain	Configuration
WDT30	GLOBAL	Supports non-maskable interrupts (NMI).
WDT31 : S WDT31 : NS	GLOBAL	Does not generate non-maskable interrupts.

Register overview

Register	Offset	TZ	Description
TASKS_START	0x000		Start WDT