8.10.7.36 MODE

Address offset: 0x510

Counter mode selection

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	AUTOEN			Automatic enable to keep the SYSCOUNTER active.
			Default	0	Default configuration to keep the SYSCOUNTER active.
			CpuActive	1	In addition to the above mode, any local CPU that is not sleeping keep the SYSCOUNTER active.
B	RW	SYSCOUNTEREN			Enable the SYSCOUNTER
			Disabled	0	SYSCOUNTER disabled
			Enabled	1	SYSCOUNTER enabled

8.10.7.37 CC[n].CCL (n=0..11)

Address offset: 0x520 + (n × 0x10)

The lower 32-bits of Capture/Compare register CC[n]

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	CCL			Capture/Compare low value in 1 µs

8.10.7.38 CC[n].CCH (n=0..11)

Address offset: 0x524 + (n × 0x10)

The higher 32-bits of Capture/Compare register CC[n]

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	CCH			Capture/Compare high value in 1 µs

8.10.7.39 CC[n].CCADD (n=0..11)

Address offset: 0x528 + (n × 0x10)

Count to add to CC[n] when this register is written.