Figure 8-64. WD_CONFIG_2 Register

7	6	5	4	3	2	1	0
WD_TIMER			WD_ERR_CNT				WD_STBY_DIS
R/W-000b			RH-0001b				R/W-0b

Table 8-20. WD_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	WD_TIMER	R/W	000b	Sets window or timeout times based upon the WD_PRE setting See WD_TIMER table
4-1	WD_ERR_CNT	RH	0001b	Watchdog error counter Running count of errors up to 15 errors
0	WD_STBY_DIS	R/W	0b	Watchdog disable in standby mode 0b = Enabled 1b = Disabled

8.6.11 WD_INPUT_TRIG Register (Address = 15h) [reset = 0h]

WD_INPUT_TRIG is shown in Figure 8-65 and described in Table 8-21.

Return to Summary Table.

Writing FFh resets WD timer if accomplished at appropriate time.

Figure 8-65. WD_INPUT_TRIG Register

7	6	5	4	3	2	1	0
WD_INPUT							
R/W1C-00h							

Table 8-21. WD_INPUT_TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_INPUT	R/W1C	00h	Write FFh to trigger WD

8.6.12 WD_RST_PULSE Register (Address = 16h) [reset = 40h]

WD_RST_PULSE is shown in Figure 8-66 and described in Table 8-22.

Return to Summary Table.

Sets the watchdog error counter value.

Figure 8-66. WD_RST_PULSE Register

7	6	5	4	3	2	1	0
WD_ERR_CNT_SET		RSVD					
R/W-01b		R-000000b					

Table 8-22. WD_RST_PULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_ERR_CNT_SET	R/W	01b	Sets the watchdog event error counter that upon reaching the count value, will cause the watchdog action. 00b = Immediate trigger on each WD fail 01b = Triggers when counter reaches 5 10b = Triggers when counter reaches 9 11b = Triggers when counter reaches 15
5-0	RSVD	R	000000b	Reserved

8.6.13 FSM_CONFIG Register (Address = 17h) [reset = 0h]

FSM_CONFIG is shown in Figure 8-67 and described in Table 8-23.

Return to Summary Table.