Peripheral	Signal	Clock pin required
SPIM/SPIS	SDO	
	SDI	
	SCK	Yes
	CSN	
	DCX	
TWIM/TWIS	SCL	Yes
	SDA	
PDM	DIN	
	CLK	Yes
I2S	MCK	Yes
	LRCK	
	SCK	Yes
	SDIN	
	SDOUT	
TRACE	TRACEDATA[]	
	TRACECLK	Yes (dedicated pin)
GRTC	CLKOUT32K	Yes (dedicated pin)
	PWMOUT	Yes (dedicated pin)
	CLKOUTFAST	Yes (dedicated pin)

Table 77: List of peripheral signals and clock pin requirement

10.1.3 QFN40 (QDAA) package pin assignments

The QFN40 pin assignment figure and table describe the pinouts for this variant of the device.

Pins that can be used as clock signals are shown in as red in the figure. For more information about clock pins, see Clock pins on page 860.

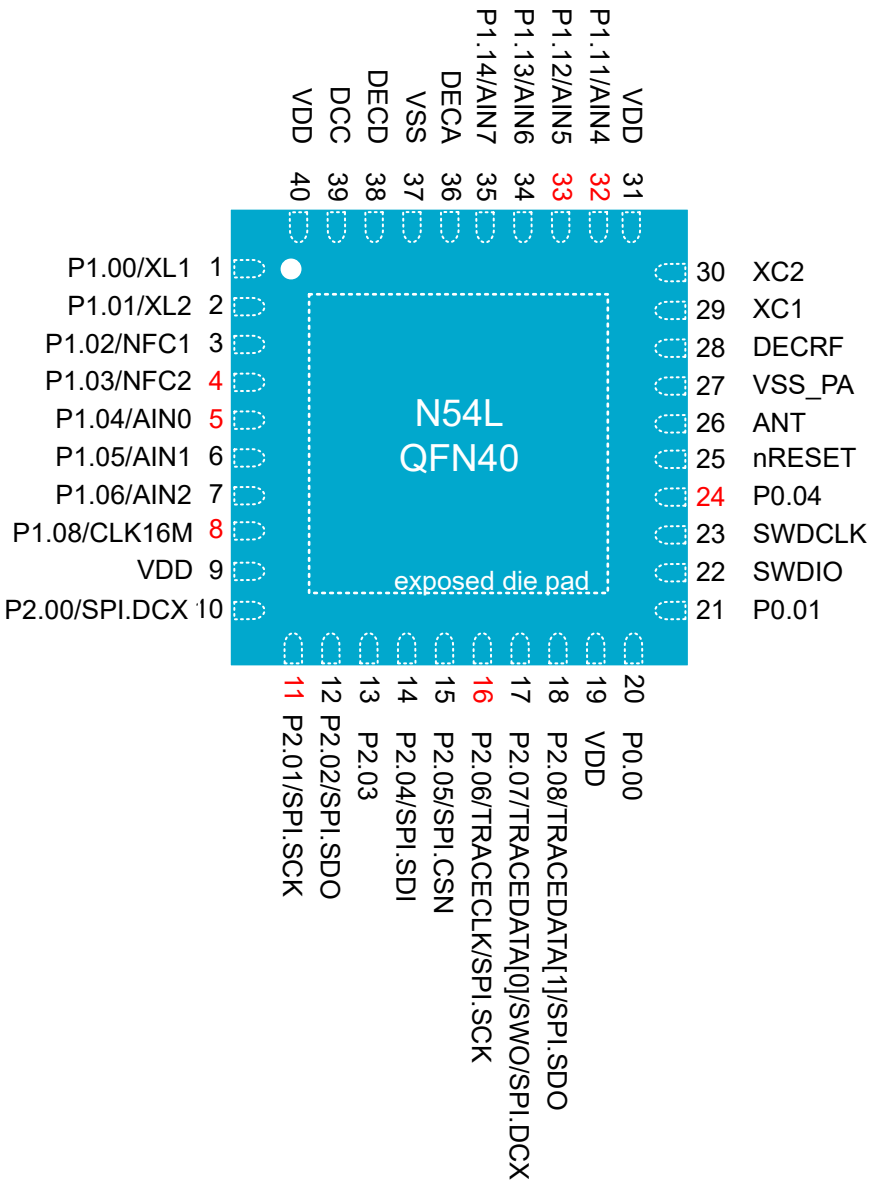

Figure 172: QFN40 pin assignments, top view

Pin	Clock pin	Name	Function	Description	Dedicated function
1		P1.00 XL1	Digital I/O Analog input	General purpose I/O Connection for 32.768 kHz crystal	
2		P1.01 XL2	Digital I/O Analog input	General purpose I/O Connection for 32.768 kHz crystal	
3		P1.02 NFC1	Digital I/O NFC input	General purpose I/O NFC antenna connection	
4	Yes	P1.03 NFC2	Digital I/O NFC input	General purpose I/O NFC antenna connection	
5	Yes	P1.04 ASO[0] AIN0	Digital I/O Digital I/O Analog input	General purpose I/O TAMPC active shield 0 output Analog input	TAMPC
6		P1.05 ASI[0] RADIO[6] AIN1	Digital I/O Digital I/O Digital I/O Analog input	General purpose I/O TAMPC active shield 0 input RADIO DFEGPIO Analog input	TAMPC RADIO
7		P1.06 ASO[1] AIN2	Digital I/O Digital I/O Analog input	General purpose I/O TAMPC active shield 1 output Analog input	TAMPC
8		P1.07 ASI[1] AIN3	Digital I/O Digital I/O Analog input	General purpose I/O TAMPC active shield 1 input Analog input	TAMPC
9	Yes	P1.08 EXTREF	Digital I/O Digital I/O Analog input	General purpose I/O GRTC CLKOUTFAST External reference for SAADC	
10		VDD	Power	Power supply	
11		P2.00	Digital I/O Digital I/O	General purpose I/O SPIM DCX	SPIM00/20

Pin	Clock pin	Name	Function	Description	Dedicated function
11	Yes	P2.01	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O SPIM SCK SPIS SCK FLPR.0 QSPI SCK	 SPIM00/20 SPIS00/20 FLPR FLPR (QSPI
12		P2.02	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O SPIM SDO SPIS SDO UARTE TXD FLPR.1 QSPI D0	 SPIM00/20 SPIS00/20 UARTE00/20 FLPR FLPR (QSPI)
13		P2.03	Digital I/O Digital I/O Digital I/O	General purpose I/O FLPR.3 QSPI D2	 FLPR FLPR (QSPI)
14		P2.04	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O SPIM SDI SPIS SDI UARTE CTS FLPR.2 QSPI D1	 SPIM00/20 SPIS00/20 UARTE00/20 FLPR FLPR (QSPI)
15		P2.05	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O SPIM CSN SPIS CSN UARTE RTS FLPR.5 QSPI CSN	 SPIM00/20 SPIS00/20 UARTE00/20 FLPR FLPR (QSPI)
16	Yes	P2.06	Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O FLPR.6 SPIM SCK SPIS SCK	 FLPR SPIM00/21 SPIS00/21

Pin	Clock pin	Name	Function	Description	Dedicated function
		TRACECLK	Digital I/O	Trace clock	Trace
17		**P2.07** **TRACEDATA[0]** **SWO**	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O FLPR.7 Trace data Serial wire output (SWO) SPIM DCX UARTE RXD	 FLPR Trace Trace SPIM00/21 UARTE00/21
18		**P2.08** **TRACEDATA[1]**	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O FLPR.8 Trace data SPIM SDO SPIS SDO UARTE TXD	 FLPR Trace SPIM00/21 SPIS00/21 UARTE00/21
19		**VDD**	Power	Power supply	
20		**P0.00**	Digital I/O	General purpose I/O	
21		**P0.01**	Digital I/O	General purpose I/O	
22		**SWDIO**	Debug	Serial wire data. Bidirectional with standard-drive and on-chip pull-up.	
23		**SWDCLK**	Debug	Serial wire clock. Input with on-chip pull-down.	
24	Yes	**P0.04**	Digital I/O Digital I/O	General purpose I/O GRTC CLKOUT32K	GRTC
25		**nRESET**	Reset	Pin reset with on-chip pull-up	
26		**ANT**	RF	Single ended radio antenna connection	See Reference circuitry on page 889 for guidelines on how to ensure good RF performance
27		**VSS_PA**	Power	Ground (radio supply)	

Pin	Clock pin	Name	Function	Description	Dedicated function
28		DECRF	Power	0.9 V regulator supply decoupling	Must be connected to DECA. See Reference circuitry on page 889.
29		XC1	Analog input	Connection for 32 MHz crystal	
30		XC2	Analog input	Connection for 32 MHz crystal	
31		VDD	Power	Power supply	
32	Yes	P1.11 ASO[3] RADIO[2] AIN4	Digital I/O Digital I/O Digital I/O Analog input	General purpose I/O TAMPC active shield 3 output RADIO DFEGPIO Analog input	 TAMPC RADIO
33	Yes	P1.12 ASI[3] RADIO[3] AIN5	Digital I/O Digital I/O Digital I/O Analog input	General purpose I/O TAMPC active shield 3 input RADIO DFEGPIO Analog input	 TAMPC RADIO
34		P1.13 RADIO[4] AIN6	Digital I/O Digital I/O Analog input	General purpose I/O RADIO DFEGPIO Analog input	 RADIO
35		P1.14 RADIO[5] AIN7	Digital I/O Digital I/O Analog input	General purpose I/O RADIO DFEGPIO Analog input	 RADIO
36		DECA	Power	0.9 V regulator supply decoupling	Must be connected to DECRF
37		VSS	Power	Ground	
38		DECD	Power	0.9 V regulator supply decoupling	
39		DCC	Power	DC/DC regulator output	

Pin	Clock pin	Name	Function	Description	Dedicated function
40		VDD	Power	Power supply	
41		VSS	Power	Ground pad (die pad)	

Table 78: QFN40 pin assignments

For the device to function properly, the exposed die pad (pin 49) must be connected to ground (VSS, pins 32 and 44).

10.1.4 QFN48 (QFAA) package pin assignments

The QFN48 pin assignment figure and table describe the pinouts for this variant of the device.

Pins that can be used as clock signals are shown in as red in the figure. For more information about clock pins, see Clock pins on page 860.

Config no.	Supply configuration	Enabled features
	VDD	NFC
Config 1	DCDC: supplied by battery or external supply	No

Table 86: Circuit configurations

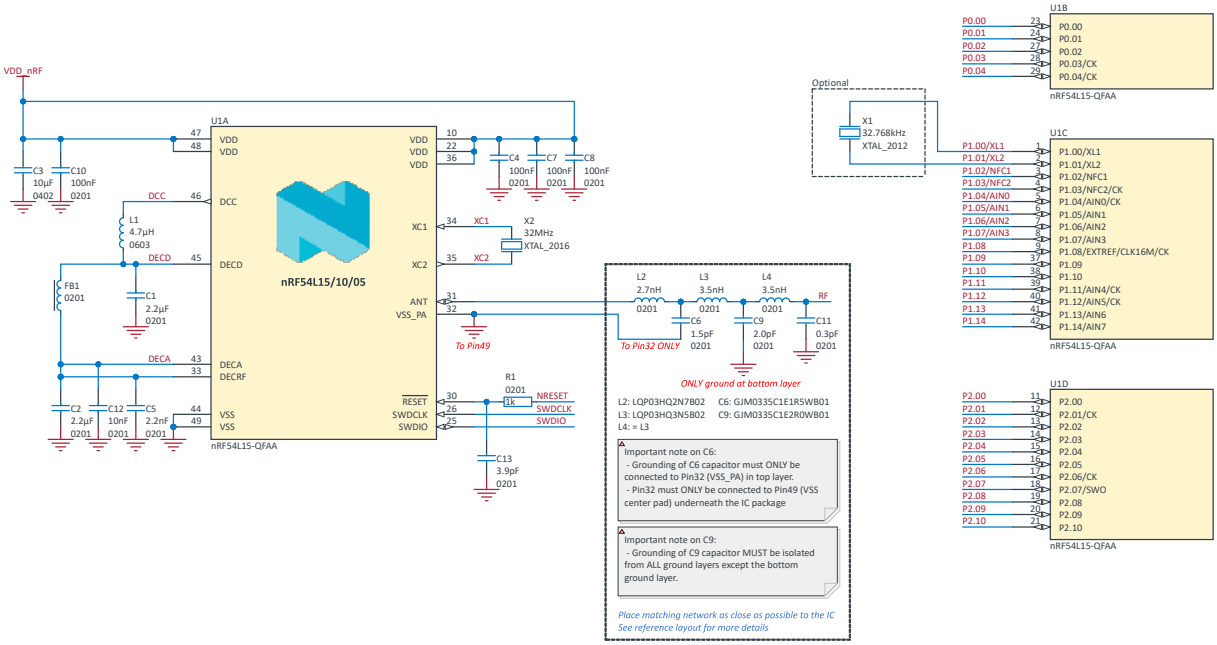

Figure 180: Circuit configuration 1 schematic

Note: For PCB reference layouts, see the product page for the device on www.nordicsemi.com.

Designator	Value	Description	Footprint
C1, C2	2.2 µF	Capacitor, X6T, ±20%, 2.5 V	0201
C3	10 µF	Capacitor, X6S, ±20%, 6.3 V	0402
C4, C7, C8, C10	100 nF	Capacitor, X7R, ±10%	0201
C5	2.2 nF	Capacitor, X7R, ±10%, 10V	0201
C6	1.5 pF	Capacitor, NP0, ±0.05 pF, 25 V, High Q	0201
C9	2.0 pF	Capacitor, NP0, ±0.05 pF, 25 V	0201
C11	0.3 pF	Capacitor, C0G, ±0.1 pF, 50 V	0201
C12	10 nF	Capacitor, X7R, 6.3 V	0201
C13	3.9 pF	Capacitor, C0G, ±0.25 pF, 50 V	0201
FB1	120 Ω	Ferrite bead, 120 Ω at 100 MHz, 200 mA, 500 mΩ Max	0201
L1	4.7 µH	Inductor, 120 mA, ±20%, 650 mΩ	0603
L2	2.7 nH	Inductor, 600 mA, ±0.1 nH, 120 mΩ	0201
L3, L4	3.5 nH	Inductor, 500 mA, ±0.1 nH, 170 mΩ	0201
R1	1 kΩ	Resistor, ±1%, 0.05 W	0201
U1	nRF54L15-QFAA	Multiprotocol Bluetooth Low Energy, IEEE 802.15.4, and 2.4GHz proprietary System on Chip	QFN-48
X1	32.768 kHz	Crystal SMD 2012, 32.768 kHz, Cl = 9 pF, Total tol: ±20 ppm	XTAL_2012
X2	32 MHz	Crystal SMD 2016, 32 MHz, Cl = 8 pF, Total Tol: ±40 ppm. For frequency tolerance requirements, see 32 MHz crystal oscillator (HFXO) on page 902.	XTAL_2016

Table 87: Bill of material for circuit configuration 1

Note: The antenna filtering components are subject to change.

10.3.2 Circuit configuration 1 for CSP47 (CAAA)

Config no.	Supply configuration	Enabled features
	VDD	NFC
Config 1	DCDC: supplied by battery or external supply	No

Table 88: Circuit configurations

10.2 Mechanical specifications

The mechanical specifications for the packages show the dimensions in millimeters.

10.2.1 QFN40 (QDAA) package

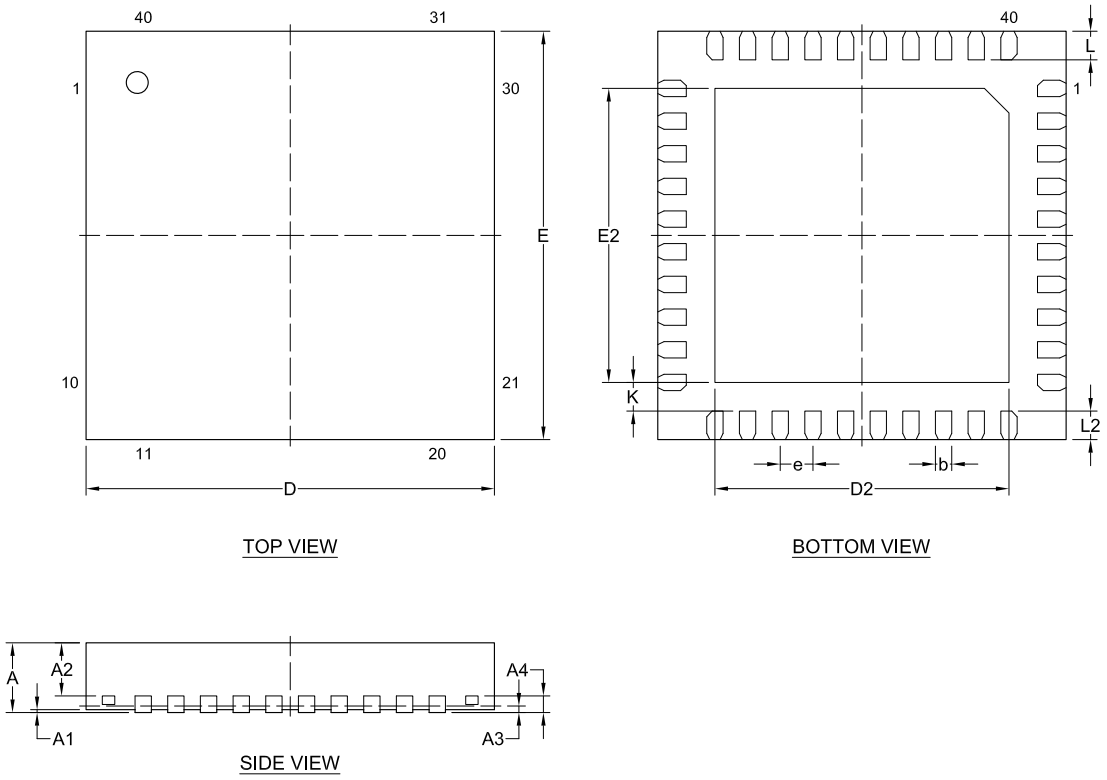

Figure 176: QFN40 5x5 mm package

	A	A1	A2	A3	A4	b	D, E	D2, E2	e	K	L	L2
Min.	0.80	0.000				0.15		3.5			0.30	0.25
Nom.	0.85	0.035	0.65	0.08	0.203	0.2	5	3.6	0.4	0.35	0.35	0.35
Max.	0.90	0.050				0.25		3.7			0.40	0.40

Table 82: Package dimensions in millimeters

10.2.2 QFN48 (QFAA) package