8.6.20 HSS_CNTL (Address = 1Eh) [reset = 0h]

HSS_CNTL is shown in Figure 8-74 and described in Table 8-30

Return to Summary Table.

HSS high side switch control.

Figure 8-74. HSS_CNTL Register

7	6	5	4	3	2	1	0
HSS_EN	HSS_CNTL			HSS_RSVD			
R/W-0b	R/W-000b			R-0000b			

Table 8-30. HSS_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HSS_EN	R/W	0b	High side switch, HSS, enable 0b = Disabled 1b = Enabled
6-4	HSS_CNTL	R/W	000b	Control for HSS 000b = On/Off 001b = PWM1 010b = PWM2 011b = Timer1 100b = Timer2 101b = HSSC 110b - 111b = Reserved Note: selecting HSSC control disables FSO output capability
3-0	HSS_RSVD	R/W	0000b	Reserved

8.6.21 PWM1_CNTL1 (Address = 1Fh) [reset = 0h]

PWM1_CNTL1 is shown in Figure 8-75 and described in Table 8-31

Return to Summary Table.

Sets the pulse width modulation frequency, PWM1.

Figure 8-75. PWM1_CNTL1 Register

7	6	5	4	3	2	1	0
PWM1_FREQ	PWM1_FREQ_RSVD						
R/W-0b	R-0b						

Table 8-31. PWM1_CNTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWM1_FREQ	R/W	0b	PWM frequency select (Hz) 0b = 200 1b = 400
6-0	PWM1_FREQ_RSVD	R	0b	Reserved

8.6.22 PWM1_CNTL2 (Address = 20h) [reset = 0h]

PWM1_CNTL2 is shown in Figure 8-76 and described in Table 8-32

Return to Summary Table.

Set the two most significant bit for the 10-bit PWM1. These work with register h'21 PWM1_CNTL3.

Figure 8-76. PWM1_CNTL2 Register

7	6	5	4	3	2	1	0
PWM1_RSVD						PWM1_DC_MSB	