11.10 PPI Electrical specification

11.10.1 Typical PPI latencies

Symbol	Description	Min.	Typ.	Max.	Units
t_{PPI}	PPI latency between same power-domain peripherals in RUN state (i.e. PCLK's are running)		2		cycles

11.11 PDM Electrical specification

11.11.1 PDM Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
$f_{PDM,CLK,64}$	PDM clock speed. PDMCLKCTRL = Default (Setting needed for 16 kHz sample frequency @ RATIO = Ratio64)		1.032		MHz
$f_{PDM,CLK,80}$	PDM clock speed. PDMCLKCTRL = 1280K (Setting needed for 16 kHz sample frequency @ RATIO = Ratio80)		1.280		MHz
$t_{PDM,JITTER}$	Jitter in PDM clock output				ns
$T_{dPDM,CLK}$	PDM clock duty cycle	40	50	60	%
$t_{PDM,DATA}$	Decimation filter delay			5	ms
$t_{PDM,s}$	Data setup time	41			ns
$t_{PDM,h}$	Data hold time	0			ns
$G_{PDM,default}$	Default (reset) absolute gain of the PDM module		0		dB

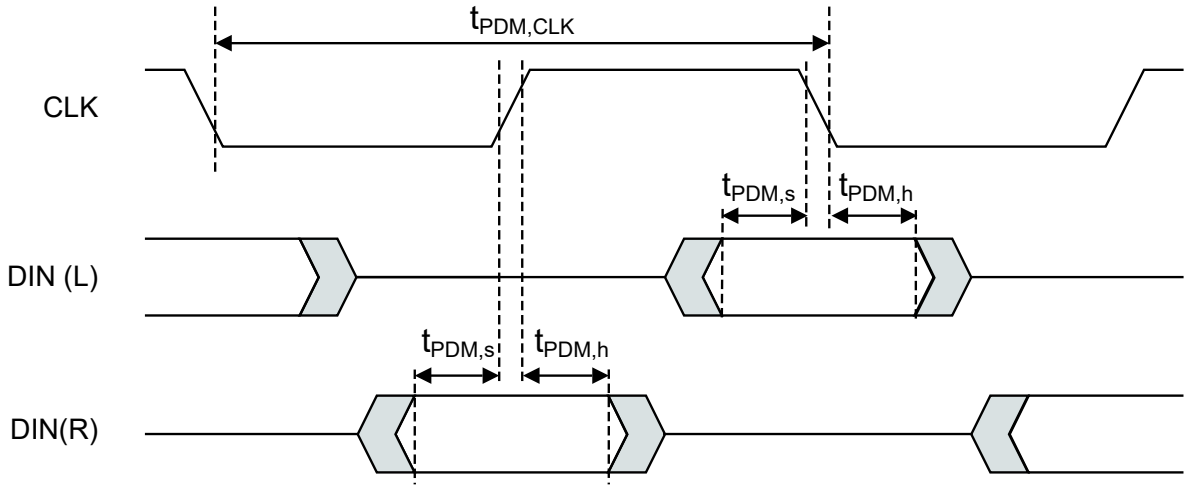

Figure 189: PDM timing diagram