6.7 Electrical Characteristics (continued)

parameters valid over –40°C ≤ T_J ≤ 150 °C range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance	4 MHz		10	15	pF
$I_{LKG(OFF)}$	Unpowered leakage current	Inputs = 5.25/3.465 V, V_{CC} = V_{SUP} = 0 V	–1		1	µA
R_{WDI_SDIpu}	Internal pull-up resistor on WDI/SDI pin		100	240	400	kΩ
R_{CLKpu}	Internal pull-up resistor on WDT/CLK pin	SPI control only for CLK	100	240	400	kΩ
R_{nCSpu}	Internal pull-up resistor on PIN/nCS pin	SPI control only for nCS	100	240	400	kΩ
WDT Input Terminal						
V_{IH}	High-level input voltage	Inputs = V_{CC}	0.8			V_{CC}
V_{IL}	Low-level input voltage	Inputs = V_{CC}			0.2	V_{CC}
$V_{IM(WDT)}$	WDT Mid-level input voltage(1)	Inputs = V_{CC}	0.4	0.5	0.6	V_{CC}
I_{IH}	High-level input leakage current	Inputs = V_{CC}	2.5		25	µA
I_{IL}	Low-level input leakage current	Inputs = 0 V, V_{CC} = Active	–25		–2.5	µA
$I_{LKG(OFF)}$	Unpowered leakage current	Inputs = 5.25/3.465 V, V_{CC} = V_{SUP} = 0 V	–3		3	µA
SDO Output Terminal						
V_{OH}	High level output voltage	I_O = –2 mA, V_{CC} = Active	0.8			V_{CC}
V_{OL}	Low level output voltage	I_O = 2 mA, V_{CC} = Active			0.2	V_{CC}
$I_{LKG(OFF)}$	Unpowered leakage current	Outputs = 5.25/3.465 V, V_{CC} = V_{SUP} = 0 V	–1		1	µA
nRST Terminal; input/output reset (Open-drain)						
I_{LKG}	Leakage current, high-level	LIN = V_{SUP}, nRST = V_{CC}	–5		5	µA
V_{OL}	Low-level output voltage	Based upon external pull up to V_{CC}			0.2	V_{CC}
I_{OL}	Low-level output current, open drain	LIN = 0 V, nRST = 0.4 V	1.5			mA
$V_{th(sw)}$	Switching threshold voltage		0.25		0.75	V_{CC}
R_{PU}	Pull-up resistance		30	45	65	kΩ
nINT, nWDR, WKRQ Terminal						
V_{OH}	High level output voltage	I_O = –2 mA, V_{CC} = Active	0.8			V_{CC}
V_{OL}	Low-level output voltage	I_O = 2 mA, V_{CC} = Active			0.2	V_{CC}
$I_{LKG(OFF)}$	Unpowered leakage current (nINT and nWDR pins)	Outputs = 5.25/3.465 V, V_{CC} = V_{SUP} = 0 V	–1		1	µA
HSSC						
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{IL}	Low-level input current	V_{IN} = 0 V	–1		1	µA
R_{HSSC}	Pull-down resistor		150	350	800	kΩ
f_{SW}	Switching frequency	V_{HSS} = 14 V, $I_{O(HSS)}$ = 60 mA			400	Hz
WDI, WDT TIMING and SWITCHING CHARACTERISTIC (RL = 1 MΩ, CL = 50 pF and T_J = -40°C to 150°C)						
t_W	WDI pulse width; see Figure 7-8	Filter time to avoid false input	30			µs
t_{WINDOW}	Closed Window + Open Window; See Figure 7-8	WDT = GND	32	40	48	ms
		WDT = V_{CC}	480	600	720	ms
		WDT = Floating	4.8	6	7.2	s
DIV_ON						
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{IL}	Low-level input current	V_{DIV_ON} = 0 V	–1		1	µA
R_{DIV_ON}	Pull-down resistor		150	370	800	kΩ
PV						
Ratio	Divider ratio 5 V VCC	V_{BAT} = 5.5 V to 28 V		1:7		
Ratio	Divider ratio 3.3 V VCC	V_{BAT} = 5.5 V to 20 V		1:9		
ERR	Divider ratio error	V_{BAT} = 5.5 V to 28 V	–2		2	%
$V_{BATLIN5}$	Linear voltage range for V_{BAT} for 5 V LDO (3)	R_{LOAD} = 470 Ω ± 5% and C_{LOAD} = 10 nF ± 10%; When capacitive load only 20 pF ± 20%, 5.5 V ≤ V_{BAT} ≤ 28 V	0.735		4.05	V