Register	Offset	TZ	Description
MEMACCERR.ADDRESS	0x400		Target Address of Memory Access Error. Register content will not be changed as long as MEMACCERR event is active.
MEMACCERR.INFO	0x404		Access information for the transaction that triggered a memory access error. Register content will not be changed as long as MEMACCERR event is active.
OVERRIDE[n].CONFIG	0x800		Override region n Configuration register
OVERRIDE[n].STARTADDR	0x804		Override region n Start Address
OVERRIDE[n].ENDADDR	0x808		Override region n End Address
OVERRIDE[n].PERM	0x810		Permission settings for override region n
OVERRIDE[n].PERMMASK	0x814		Masks permission setting fields from register OVERRIDE.PERM

7.8.4.3.1 EVENTS_MEMACCERR

Address offset: 0x100

Memory Access Error event

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	EVENTS_MEMACCERR			Memory Access Error event
			NotGenerated	0	Event not generated
			Generated	1	Event generated

7.8.4.3.2 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	MEMACCERR			Enable or disable interrupt for event MEMACCERR
			Disabled	0	Disable
			Enabled	1	Enable

7.8.4.3.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	MEMACCERR			Write '1' to enable interrupt for event MEMACCERR
	W1S				
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled