8.25.13.46 DMA.TX.TERMINATEONBUSERROR

Address offset: 0x754

Terminate the transaction if a BUSERROR event is detected.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	ENABLE																																	
			Disabled	0																															
			Enabled	1																															

8.25.13.47 DMA.TX.BUSERRORADDRESS

Address offset: 0x758

Address of transaction that generated the last BUSERROR event.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	ADDRESS																																	

8.26 VPR — RISC-V CPU

VPR is a small, efficient CPU developed by Nordic Semiconductor.

The VPR implementation is the Fast Lightweight Peripheral Processor (FLPR), optimized to implement coprocessor functions, and operating at the same frequency as the application processor.

VPR is compatible with the RISC-V instruction set and implements the following extensions:

- E – Integer instruction set with 16 registers
- M – Multiply and divide extension
- C – Compressed extension (compressed instructions)

VPR implements the machine mode CPU mode as well as the RISC-V CLIC specification for the interrupt controller.

VPR does not start on its own, but must be started by the application core processor by performing the following steps:

1. Configure VPR program counter (PC) to point to the peripheral binary image by using register INITPC on page 768.
2. Start VPR by using register CPURUN on page 767.