11.18.4 Timing specifications for GPIO port P1 using Standard drive strength

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SPIM,SUMI}$	SDI to CLK edge setup time	43			ns
$t_{SPIM,HMI}$	CLK edge to SDI hold time	0			ns
$t_{SPIM,VMO}$	CLK edge to SDO valid			14	ns
$t_{SPIM,HMO}$	SDO hold time after CLK edge	-12			ns

11.18.5 Timing specifications for GPIO port P1 using High drive strength

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SPIM,SUMI}$	SDI to CLK edge setup time	39			ns
$t_{SPIM,HMI}$	CLK edge to SDI hold time	0			ns
$t_{SPIM,VMO}$	CLK edge to SDO valid			12	ns
$t_{SPIM,HMO}$	SDO hold time after CLK edge	-10			ns

11.18.6 Timing specifications for GPIO port P2 using Standard drive strength

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SPIM,SUMI}$	SDI to CLK edge setup time	43			ns
$t_{SPIM,HMI}$	CLK edge to SDI hold time	0			ns
$t_{SPIM,VMO}$	CLK edge to SDO valid			14	ns
$t_{SPIM,HMO}$	SDO hold time after CLK edge	-12			ns

11.18.7 Timing specifications for GPIO port P2 using High drive strength

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SPIM,SUMI}$	SDI to CLK edge setup time	39			ns
$t_{SPIM,HMI}$	CLK edge to SDI hold time	0			ns
$t_{SPIM,VMO}$	CLK edge to SDO valid			12	ns
$t_{SPIM,HMO}$	SDO hold time after CLK edge	-10			ns

11.18.8 Timing specifications for GPIO port P2 using Extra high drive strength

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SPIM,SUMI}$	SDI to CLK edge setup time	15			ns
$t_{SPIM,HMI}$	CLK edge to SDI hold time	0			ns
$t_{SPIM,VMO}$	CLK edge to SDO valid			3	ns
$t_{SPIM,HMO}$	SDO hold time after CLK edge	-1			ns