Configuration

Instance	Domain	Configuration
DPPIC00 : S DPPIC00 : NS	GLOBAL	8 DPPI channels 2 DPPI groups
DPPIC10 : S DPPIC10 : NS	GLOBAL	24 DPPI channels 6 DPPI groups
DPPIC20 : S DPPIC20 : NS	GLOBAL	16 DPPI channels 6 DPPI groups
DPPIC30 : S DPPIC30 : NS	GLOBAL	4 DPPI channels 2 DPPI groups

Register overview

Register	Offset	TZ	Description
TASKS_CHG[n].EN	0x000		Enable channel group n
TASKS_CHG[n].DIS	0x004		Disable channel group n
SUBSCRIBE_CHG[n].EN	0x080		Subscribe configuration for task CHG[n].EN
SUBSCRIBE_CHG[n].DIS	0x084		Subscribe configuration for task CHG[n].DIS
CHEN	0x500		Channel enable register
CHENSET	0x504		Channel enable set register
CHENCLR	0x508		Channel enable clear register
CHG[n]	0x800		Channel group n Note: Writes to this register are ignored if either SUBSCRIBE_CHG[n].EN or SUBSCRIBE_CHG[n].DIS is enabled

6.2.6.1 TASKS_CHG[n] (n=0..5)

Channel group tasks

6.2.6.1.1 TASKS_CHG[n].EN (n=0..5)

Address offset: 0x000 + (n × 0x8)

Enable channel group n

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	EN			Enable channel group n
			Trigger	1	Trigger task

6.2.6.1.2 TASKS_CHG[n].DIS (n=0..5)

Address offset: 0x004 + (n × 0x8)

Disable channel group n