

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|-----|--|----------|---|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID | | | | I H G F E D C B A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset 0x00000000 | | | | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | R/W | Field | Value ID | Value | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | END_START | | | Shortcut between event END and task START | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Disable shortcut | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | Enable shortcut | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B-E | RW | DMA_RX_MATCH[i]_DMA_RX_ENABLEMA +1)%4] (i=0..3) | | | Shortcut between event DMA.RX.MATCH[n] and task DMA.RX.ENABLEMATCH[(i+1)%4] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | Allows daisy-chaining match events. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Disable shortcut | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | Enabled | 1 | Enable shortcut | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F-I | RW | DMA_RX_MATCH[i]_DMA_RX_DISABLEMATCH[i] (i=0..3) | | | Shortcut between event DMA.RX.MATCH[i] and task DMA.RX.DISABLEMATCH[i] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Disable shortcut | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | Enable shortcut | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

8.19.8.20 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number | | | | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|-----|-------------------|----------|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID | | | | M L K J I H G F E D C B A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset 0x00000000 | | | | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ID | R/W | Field | Value ID | Value | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | STARTED W1S | | | Write '1' to enable interrupt for event STARTED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | Enable | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | STOPPED W1S | | | Write '1' to enable interrupt for event STOPPED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | Enable | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | END W1S | | | Write '1' to enable interrupt for event END | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | Enable | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | RW | DMARXEND W1S | | | Write '1' to enable interrupt for event DMARXEND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | Enable | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | RW | DMARXREADY W1S | | | Write '1' to enable interrupt for event DMARXREADY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Set | 1 | Enable | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | Read: Disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | Read: Enabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |