Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				R Q P O N M L K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
			Disabled	0	Disable
			Enabled	1	Enable
K	RW	DMASEQ0BUSERROR			Enable or disable interrupt for event DMASEQ0BUSERROR When this event is generated, the address which caused the error can be read from the BUSERRORADDRESS register.
			Disabled	0	Disable
			Enabled	1	Enable
L	RW	DMASEQ1END			Enable or disable interrupt for event DMASEQ1END
			Disabled	0	Disable
			Enabled	1	Enable
M	RW	DMASEQ1READY			Enable or disable interrupt for event DMASEQ1READY
			Disabled	0	Disable
			Enabled	1	Enable
N	RW	DMASEQ1BUSERROR			Enable or disable interrupt for event DMASEQ1BUSERROR When this event is generated, the address which caused the error can be read from the BUSERRORADDRESS register.
			Disabled	0	Disable
			Enabled	1	Enable
O-R	RW	COMPAREMATCH[i] (i=0..3)			Enable or disable interrupt for event COMPAREMATCH[i]
			Disabled	0	Disable
			Enabled	1	Enable

8.15.5.25 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				R Q P O N M L K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW W1S	STOPPED			Write '1' to enable interrupt for event STOPPED
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
B-C	RW W1S	SEQSTARTED[i] (i=0..1)			Write '1' to enable interrupt for event SEQSTARTED[i]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D-E	RW W1S	SEQEND[i] (i=0..1)			Write '1' to enable interrupt for event SEQEND[i]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW W1S	PWMPERIODEND			Write '1' to enable interrupt for event PWMPERIODEND
			Set	1	Enable