Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				L K J I H G F E D C B A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
			Disabled	0	This event is not filtered.
			Enabled	1	This event is filtered.
B	RW	SSSTATUS			When TRCIDR4.NUMACPAIRS > 0 or TRCIDR4.NUMPC > 0, this bit returns the status of the start/stop logic.
			Stopped	0	The start/stop logic is in the stopped state.
			Started	1	The start/stop logic is in the started state.
C	RW	TRCRESET			Controls whether a trace unit must trace a Reset exception.
			Disabled	0	The trace unit does not trace a Reset exception unless it traces the exception or instruction immediately prior to the Reset exception.
			Enabled	1	The trace unit always traces a Reset exception.
D	RW	TRCERR			When TRCIDR3.TRCERR==1, this bit controls whether a trace unit must trace a System error exception.
			Disabled	0	The trace unit does not trace a System error exception unless it traces the exception or instruction immediately prior to the System error exception.
			Enabled	1	The trace unit always traces a System error exception, regardless of the value of ViewInst.
E-H	RW	EXLEVEL[i]_S (i=0..3)			In Secure state, each bit controls whether instruction tracing is enabled for the corresponding Exception level i.
			Disabled	1	The trace unit does not generate instruction trace, in Secure state, for Exception level i.
			Enabled	0	The trace unit generates instruction trace, in Secure state, for Exception level i.
I-L	RW	EXLEVEL[i]_NS (i=0..3)			In Non-secure state, each bit controls whether instruction tracing is enabled for the corresponding Exception level i.
			Disabled	1	The trace unit does not generate instruction trace, in Non-secure state, for Exception level i.
			Enabled	0	The trace unit generates instruction trace, in Non-secure state, for Exception level i.

9.8.1.15 TRCVIIECTLR

Address offset: 0x084

ViewInst exclude control.

Might ignore writes when the trace unit is enabled or not idle.

This register must be programmed when one or more address comparators are implemented.