Register overview

Register	Offset	TZ	Description
TASKS_START	0x000		Start SPI transaction
TASKS_STOP	0x004		Stop SPI transaction
TASKS_SUSPEND	0x00C		Suspend SPI transaction
TASKS_RESUME	0x010		Resume SPI transaction
TASKS_DMA.RX.ENABLEMATCH[n]	0x030		Enables the MATCH[n] event by setting the ENABLE[n] bit in the CONFIG register.
TASKS_DMA.RX.DISABLEMATCH[n]	0x040		Disables the MATCH[n] event by clearing the ENABLE[n] bit in the CONFIG register.
SUBSCRIBE_START	0x080		Subscribe configuration for task START
SUBSCRIBE_STOP	0x084		Subscribe configuration for task STOP
SUBSCRIBE_SUSPEND	0x08C		Subscribe configuration for task SUSPEND
SUBSCRIBE_RESUME	0x090		Subscribe configuration for task RESUME
SUBSCRIBE_DMA.RX.ENABLEMATCH[n]	0x0B0		Subscribe configuration for task ENABLEMATCH[n]
SUBSCRIBE_DMA.RX.DISABLEMATCH[n]	0x0C0		Subscribe configuration for task DISABLEMATCH[n]
EVENTS_STARTED	0x100		SPI transaction has started
EVENTS_STOPPED	0x104		SPI transaction has stopped
EVENTS_END	0x108		End of RXD buffer and TXD buffer reached
EVENTS_DMA.RX.END	0x14C		Generated after all MAXCNT bytes have been transferred
EVENTS_DMA.RX.READY	0x150		Generated when EasyDMA has buffered the .PTR and .MAXCNT registers for the channel, allowing them to be written to prepare for the next sequence.
EVENTS_DMA.RX.BUSERROR	0x154		An error occured during the bus transfer.
EVENTS_DMA.RX.MATCH[n]	0x158		Pattern match is detected on the DMA data bus.
EVENTS_DMA.TX.END	0x168		Generated after all MAXCNT bytes have been transferred
EVENTS_DMA.TX.READY	0x16C		Generated when EasyDMA has buffered the .PTR and .MAXCNT registers for the channel, allowing them to be written to prepare for the next sequence.
EVENTS_DMA.TX.BUSERROR	0x170		An error occured during the bus transfer.
PUBLISH_STARTED	0x180		Publish configuration for event STARTED
PUBLISH_STOPPED	0x184		Publish configuration for event STOPPED
PUBLISH_END	0x188		Publish configuration for event END
PUBLISH_DMA.RX.END	0x1CC		Publish configuration for event END
PUBLISH_DMA.RX.READY	0x1D0		Publish configuration for event READY
PUBLISH_DMA.RX.BUSERROR	0x1D4		Publish configuration for event BUSERROR
PUBLISH_DMA.RX.MATCH[n]	0x1D8		Publish configuration for event MATCH[n]
PUBLISH_DMA.TX.END	0x1E8		Publish configuration for event END
PUBLISH_DMA.TX.READY	0x1EC		Publish configuration for event READY
PUBLISH_DMA.TX.BUSERROR	0x1F0		Publish configuration for event BUSERROR
SHORTS	0x200		Shortcuts between local events and tasks
INTENSET	0x304		Enable interrupt
INTENCLR	0x308		Disable interrupt
ENABLE	0x500		Enable SPIM
PRESCALER	0x52C		The prescaler is used to set the SPI frequency.
CONFIG	0x554		Configuration register
IFTIMING.RXDELAY	0x5AC		Sample delay for input serial data on SDI
IFTIMING.CSNDUR	0x5B0		Minimum duration between edge of CSN and edge of SCK. When SHORTS.END_START is used, this is also the minimum duration CSN must stay high between transactions.
DCXCNT	0x5B4		DCX configuration
CSNPOL	0x5B8		Polarity of CSN output
ORC	0x5C0		Byte transmitted after TXD.MAXCNT bytes have been transmitted in the case when RXD.MAXCNT is greater than TXD.MAXCNT
PSEL.SCK	0x600		Pin select for SCK
PSEL.MOSI	0x604		Pin select for SDO signal
PSEL.MISO	0x608		Pin select for SDI signal
PSEL.DCX	0x60C		Pin select for DCX signal