

6.7 Electrical Characteristics (continued)

parameters valid over $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------------|---|---|-------|-------|------|---------------|
| V_{BATLIN3} | Linear voltage range for V_{BAT} for 3.3 V LDO and when I/O is 3.3 V with 5 V LDO ⁽⁴⁾ | $R_{\text{LOAD}} = 470\ \Omega \pm 5\%$ and $C_{\text{LOAD}} = 10\ \text{nF} \pm 10\%$; When capacitive load only $20\ \text{pF} \pm 20\%$, $5.5\ \text{V} \leq V_{\text{BAT}} \leq 20\ \text{V}$ | 0.561 | | 2.27 | V |
| V_{MAX5V} | Maximum V_{PVOU} | $28\ \text{V} < V_{\text{BAT}} \leq 42\ \text{V}$, $470\ \Omega \pm 5\%$ and $C_{\text{LOAD}} = 10\ \text{nF} \pm 10\%$; When capacitive load only $20\ \text{pF} \pm 20\%$ | | | 5.1 | V |
| $V_{\text{MAX3.3V}}$ | Maximum V_{PVOU} for 3.3 V LDO and when I/O is 3.3 V with 5 V LDO | $20\ \text{V} < V_{\text{BAT}} \leq 42\ \text{V}$, $470\ \Omega \pm 5\%$ and $C_{\text{LOAD}} = 10\ \text{nF} \pm 10\%$; When capacitive load only $20\ \text{pF} \pm 20\%$ | | | 3.36 | V |
| $V_{\text{VCC5V_VIO3V}}$ | Voltage when VCC = 5 V and I/O is at 3.3 V | $R_{\text{LOAD}} = 470\ \Omega \pm 5\%$ and $C_{\text{LOAD}} = 10\ \text{nF} \pm 10\%$; When capacitive load only $20\ \text{pF} \pm 20\%$ and I/O voltage is $\leq 3.6\ \text{V}$ | | | 3.36 | V |
| C_{PIN} | Pin capacitance | | | 12 | | pF |
| t_{SET} | Settling time of the buffer | $470\ \Omega \pm 5\%$ and $C_{\text{LOAD}} = 10\ \text{nF} \pm 10\%$; When capacitive load only $20\ \text{pF} \pm 20\%$ | | | 50 | μs |
| Duty Cycle Characteristics | | | | | | |
| D1 | Duty Cycle 1 (ISO/DIS 17987 Param 27 and J2602 Normal battery) ^{(8) (9)} | $\text{TH}_{\text{REC}}(\text{MAX}) = 0.744 \times V_{\text{SUP}}$, $\text{TH}_{\text{DOM}}(\text{MAX}) = 0.581 \times V_{\text{SUP}}$, $V_{\text{SUP}} = 7\ \text{V}$ to $18\ \text{V}$, $t_{\text{BIT}} = 50/52\ \mu\text{s}$, $D1 = t_{\text{BUS_rec}}(\text{min}) / (2 \times t_{\text{BIT}})$ (See Figure 7-3, Figure 7-4) | 0.396 | | | |
| D2 | Duty Cycle 2 (ISO/DIS 17987 Param 28 and J2602 Normal battery) ^{(8) (9)} | $\text{TH}_{\text{REC}}(\text{MIN}) = 0.422 \times V_{\text{SUP}}$, $\text{TH}_{\text{DOM}}(\text{MIN}) = 0.284 \times V_{\text{SUP}}$, $V_{\text{SUP}} = 7.6\ \text{V}$ to $18\ \text{V}$, $t_{\text{BIT}} = 50/52\ \mu\text{s}$, $D2 = t_{\text{BUS_rec}}(\text{MAX}) / (2 \times t_{\text{BIT}})$ (See Figure 7-3, Figure 7-4) | | 0.581 | | |
| D3 | Duty Cycle 3 (ISO/DIS 17987 Param 29 and J2602 Normal battery) ^{(8) (9)} | $\text{TH}_{\text{REC}}(\text{MAX}) = 0.778 \times V_{\text{SUP}}$, $\text{TH}_{\text{DOM}}(\text{MAX}) = 0.616 \times V_{\text{SUP}}$, $V_{\text{SUP}} = 7.0\ \text{V}$ to $18\ \text{V}$, $t_{\text{BIT}} = 96\ \mu\text{s}$, $D3 = t_{\text{BUS_rec}}(\text{min}) / (2 \times t_{\text{BIT}})$ (See Figure 7-3, Figure 7-4) | 0.417 | | | |
| D4 | Duty Cycle 4 (ISO/DIS 17987 Param 30 and J2602 Normal battery) ^{(8) (9)} | $\text{TH}_{\text{REC}}(\text{MIN}) = 0.389 \times V_{\text{SUP}}$, $\text{TH}_{\text{DOM}}(\text{MIN}) = 0.251 \times V_{\text{SUP}}$, $V_{\text{SUP}} = 7.6\ \text{V}$ to $18\ \text{V}$, $t_{\text{BIT}} = 96\ \mu\text{s}$, $D4 = t_{\text{BUS_rec}}(\text{MAX}) / (2 \times t_{\text{BIT}})$ (See Figure 7-3, Figure 7-4) | | 0.59 | | |
| D1 _{LB} | Duty Cycle 1 J2602 Low battery ^{(9) (10)} | $\text{TH}_{\text{REC}}(\text{MAX}) = 0.665 \times V_{\text{SUP}}$, $\text{TH}_{\text{DOM}}(\text{MAX}) = 0.499 \times V_{\text{SUP}}$, $V_{\text{SUP}} = 5.5\ \text{V}$ to $7\ \text{V}$, $t_{\text{BIT}} = 50/52\ \mu\text{s}$, $D1 = t_{\text{BUS_rec}}(\text{min}) / (2 \times t_{\text{BIT}})$ (See Figure 7-3, Figure 7-4) | 0.396 | | | |
| D2 _{LB} | Duty Cycle 2 J2602 Low battery ^{(9) (10)} | $\text{TH}_{\text{REC}}(\text{MIN}) = 0.496 \times V_{\text{SUP}}$, $\text{TH}_{\text{DOM}}(\text{MIN}) = 0.361 \times V_{\text{SUP}}$, $V_{\text{SUP}} = 6.1\ \text{V}$ to $7.6\ \text{V}$, $t_{\text{BIT}} = 50/52\ \mu\text{s}$, $D2 = t_{\text{BUS_rec}}(\text{MAX}) / (2 \times t_{\text{BIT}})$ (See Figure 7-3, Figure 7-4) | | 0.581 | | |
| D3 _{LB} | Duty Cycle 3 J2602 Low battery ^{(9) (10)} | $\text{TH}_{\text{REC}}(\text{MAX}) = 0.665 \times V_{\text{SUP}}$, $\text{TH}_{\text{DOM}}(\text{MAX}) = 0.499 \times V_{\text{SUP}}$, $V_{\text{SUP}} = 5.5\ \text{V}$ to $7\ \text{V}$, $t_{\text{BIT}} = 96\ \mu\text{s}$, $D1 = t_{\text{BUS_rec}}(\text{min}) / (2 \times t_{\text{BIT}})$ (See Figure 7-3, Figure 7-4) | 0.417 | | | |
| D4 _{LB} | Duty Cycle 4 J2602 Low battery ^{(9) (10)} | $\text{TH}_{\text{REC}}(\text{MIN}) = 0.496 \times V_{\text{SUP}}$, $\text{TH}_{\text{DOM}}(\text{MIN}) = 0.361 \times V_{\text{SUP}}$, $V_{\text{SUP}} = 6.1\ \text{V}$ to $7.6\ \text{V}$, $t_{\text{BIT}} = 96\ \mu\text{s}$, $D2 = t_{\text{BUS_rec}}(\text{MAX}) / (2 \times t_{\text{BIT}})$ (See Figure 7-3, Figure 7-4) | | 0.59 | | |

- (1) This is the measured voltage at the WDT pin when left floating. The WDT pin should be connected directly to V_{CC} , GND or left floating.
- (2) Specified by design
- (3) $V_{\text{BATLIN5}} = [(1/7) \times V_{\text{BAT}}] \pm 50\ \text{mV}$ for the linear range of the PV buffer
- (4) $V_{\text{BATLIN3}} = [(1/9) \times V_{\text{BAT}}] \pm 50\ \text{mV}$ for the linear range of the PV buffer
- (5) SAE J2602 loads include: commander node: 5.5 nF; 4 k Ω and for a responder node: 5.5 nF; 875 Ω
- (6) V_{HYS} is defined for both ISO 17987 and SAE J2602-1.
- (7) $V_{\text{HYS}} = (V_{\text{th_rec}} - V_{\text{th_dom}})$ where $V_{\text{th_rec}}$ and $V_{\text{th_dom}}$ are the actual voltage values from V_{BUSrec} and V_{BUSdom}
- (8) ISO 17987 loads include 1 nF; 1 k Ω / 6.8nF; 660 Ω / 10 nF; 500 Ω ; with t_{BIT} values of 50 μs and 96 μs
- (9) SAE J2602 loads include: commander node: 5.5 nF; 4 k Ω / 899 pF; 20 k Ω and for a responder node: 5.5 nF; 875 Ω / 899 pF; 900 Ω ; with t_{BIT} values of 52 μs and 96 μs