| Bit number | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|
| ID | W V U T S R Q P O N M L K J I H G F E D C B A |
| **Reset 0x00000000** | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |

| ID | R/W | Field | Value ID | Value | Description |
|---|---|---|---|---|---|
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| R | RW W1C | CCABUSY | | | Write '1' to disable interrupt for event CCABUSY |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| S | RW W1C | CCASTOPPED | | | Write '1' to disable interrupt for event CCASTOPPED |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| T | RW W1C | RATEBOOST | | | Write '1' to disable interrupt for event RATEBOOST |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| U | RW W1C | MHRMATCH | | | Write '1' to disable interrupt for event MHRMATCH |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| V | RW W1C | SYNC | | | Write '1' to disable interrupt for event SYNC |
| | | | | | MODE=Ble_LR125Kbit, Ble_LR500Kbit, or Ieee802154_250Kbit: A possible preamble has been received. However, due to the sporadic reception of noise, this event can be falsely triggered. |
| | | | | | For MODE=Nrf_1Mbit, Nrf_2Mbit, Ble_1Mbit, or Ble_2Mbit: A possible preamble and the first two bytes of the address field has been received. The event can be generated falsely also in this mode. |
| | | | | | It is also possible that the event is not generated, or not generated before the ADDRESS event. |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |
| W | RW W1C | CTEPRESENT | | | Write '1' to disable interrupt for event CTEPRESENT |
| | | | Clear | 1 | Disable |
| | | | Disabled | 0 | Read: Disabled |
| | | | Enabled | 1 | Read: Enabled |

## 8.17.14.97 INTENCLR11

Address offset: 0x4B4

Disable interrupt

NORDIC
SEMICONDUCTOR