8.25.13.14 PUBLISH_CTS

Address offset: 0x180

Publish configuration for event CTS

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
ID				B		A A A A A A A
Reset 0x00000000				0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
ID	R/W	Field	Value ID	Value	Description	
A	RW	CHIDX		[0..255]	DPPI channel that event CTS will publish to	
B	RW	EN				
			Disabled	0	Disable publishing	
			Enabled	1	Enable publishing	

8.25.13.15 PUBLISH_NCTS

Address offset: 0x184

Publish configuration for event NCTS

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
ID				B		A A A A A A A
Reset 0x00000000				0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
ID	R/W	Field	Value ID	Value	Description	
A	RW	CHIDX		[0..255]	DPPI channel that event NCTS will publish to	
B	RW	EN				
			Disabled	0	Disable publishing	
			Enabled	1	Enable publishing	

8.25.13.16 PUBLISH_TXDRDY

Address offset: 0x18C

Publish configuration for event TXDRDY

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
ID				B		A A A A A A A
Reset 0x00000000				0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
ID	R/W	Field	Value ID	Value	Description	
A	RW	CHIDX		[0..255]	DPPI channel that event TXDRDY will publish to	
B	RW	EN				
			Disabled	0	Disable publishing	
			Enabled	1	Enable publishing	

8.25.13.17 PUBLISH_RXDRDY

Address offset: 0x190

Publish configuration for event RXDRDY

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