Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	WOKENUP			Read pending status of interrupt for event WOKENUP This event is triggered only if waken up by the WAKEUP task
			NotPending	0	Read: Not pending
			Pending	1	Read: Pending
B	R	READY			Read pending status of interrupt for event READY This event is not connected to PPI
			NotPending	0	Read: Not pending
			Pending	1	Read: Pending
C	R	READYNEXT			Read pending status of interrupt for event READYNEXT This event is not connected to PPI
			NotPending	0	Read: Not pending
			Pending	1	Read: Pending
D	R	ACCESSERROR			Read pending status of interrupt for event ACCESSERROR This event is not connected to PPI
			NotPending	0	Read: Not pending
			Pending	1	Read: Pending

4.2.6.7.16 READY

Address offset: 0x400

RRAMC ready status

The event READY is generated when the status changes to Ready

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	READY			RRAMC is ready or busy The status is updated for all RRAMC operations except during read and writes to write-buffer
			Busy	0	RRAMC is busy
			Ready	1	The current RRAMC operation is completed and RRAMC is ready

4.2.6.7.17 READYNEXT

Address offset: 0x404

Ready next flag

The event READYNEXT is generated when the READYNEXT status changes to Ready

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	R	READYNEXT			RRAMC can accept a new write operation
			Busy	0	RRAMC cannot accept any write operation now
			Ready	1	RRAMC is ready to accept a new write operation