Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
B	RW W1C	PROTECT			Error detected for the protected signals.
			NotDetected	0	Not detected.
			Detected	1	Detected.
C	RW W1C	CRACENTAMP			CRACEN detected an error.
			NotDetected	0	Not detected.
			Detected	1	Detected.
D	RW W1C	GLITCHSLOWDOMAIN[i] (i=0..0)			Slow domain glitch detector i detected an error.
			NotDetected	0	Not detected.
			Detected	1	Detected.
E-H	RW W1C	GLITCHFASTDOMAIN[i] (i=0..3)			Fast domain glitch detector i detected an error.
			NotDetected	0	Not detected.
			Detected	1	Detected.

7.8.6.6.8 ACTIVESHIELD.CHEN

Address offset: 0x404

Active shield detector channel enable register.

Pins reserved for the active shield channels must be configured before the channels can be used. Pins reserved for unused channels can be used as GPIO.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A-D	RW	CH[i] (i=0..3)			Enable or disable active shield channel i.
			Disabled	0	Disable channel.
			Enabled	1	Enable channel.

7.8.6.6.9 PROTECT.DOMAIN[n].DBGEN.CTRL (n=0..0)

Address offset: 0x500 + (n × 0x20)

Control register for invasive (halting) debug enable for the local debug components within domain n.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D D D D D D D D D D D D D D D D C C C C B A
Reset 0x00000010				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0**

ID	R/W	Field	Value ID	Value	Description
A	RW	VALUE			Set value of dbgen signal.
			Low	0	Signal is logic 0, indicating that invasive debug is disabled.
			High	1	Signal is logic 1, indicating that invasive debug is enabled.
B	W1 W1S	LOCK			Lock this register to prevent changes to the VALUE field until next reset.
			Disabled	0	Lock disabled.
			Enabled	1	Lock enabled.