

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	R/W	Field		Value ID	Value	Description																													
A	W1	KEY			The ERASEALL sequence is initiated if the value of the KEY fields are non-zero and the KEY fields match on both the CPU and debugger sides.																														

9.6.6.1.13 RESET

Address offset: 0x520

System reset request.

Only the enumerated values are supported, writing other values has unpredictable effect.

Bit number					31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																	A	A	A	
Reset 0x00000000					0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID	R/W	Field	Value ID	Value	Description																															
A	W	RESET			Reset request																															
			NoReset	0	No reset is generated																															
			SoftReset	1	Perform a device soft reset																															
			HardReset	2	Perform a device hard reset																															
			PinReset	4	Perform a device pin reset																															

9.7 TAD — Trace and debug control

Configuration interface for trace and debug

Please refer to the [Trace](#) section for more information about how to configure the trace and debug interface.

Note: When the trace port is enabled, all pins assigned to the trace port are acquired by the TAD peripheral and cannot be used for GPIO or other functions. This applies even when using the serial trace mode (SWO). See [Pin assignment chapter](#) for more information.

9.7.1 Registers

Instances

Instance	Domain	Base address	TrustZone			Split access	Description
			Map	Att	DMA		
TAD : S	GLOBAL	0x50053000	US	S	NA	No	Trace and debug control
TAD : NS		0x40053000					