Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
	R	TRIGGERED[i] (i=16..22)			Read pending status of interrupt for event TRIGGERED[i] If RTPs are not enabled: writes to registers 15..0 are ignored, other read/write accesses operate normally If RTPs are enabled: reads or writes to these registers will be stalled if there is a simultaneous VPR CSR write access to any CSR register.
			NotPending	0	Read: Not pending
			Pending	1	Read: Pending

8.26.1.9 DEBUGIF.DATA0

Address offset: 0x410

Abstract Data 0. Read/write data for argument 0

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	DATA0			Abstract Data 0

8.26.1.10 DEBUGIF.DATA1

Address offset: 0x414

Abstract Data 1. Read/write data for argument 1

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	DATA1			Abstract Data 1

8.26.1.11 DEBUGIF.DMCONTROL

Address offset: 0x440

Debug Module Control

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				K J I H G F F F F F F F F F E E E E E E E E E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	DMACTIVE			Reset signal for the debug module.
			Disabled	0	Reset the debug module itself
			Enabled	1	Normal operation
B	RW	NDMRESET			Reset signal output from the debug module to the system.
			Inactive	0	Reset inactive
			Active	1	Reset active
C	W	CLRRESETHALTREQ			Clear the halt on reset request.