Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	W	VALUE			Count to add to CC[n]
B	W	REFERENCE			Configure the Capture/Compare register
			SYSCOUNTER	0	Adds SYSCOUNTER value. CC[n] becomes CCADD[n].VALUE + SYSCOUNTER when this register is written.
			CC	1	Adds CC value. CC[n] becomes CCADD[n].VALUE + CC[n] when this register is written.

8.10.7.40 CC[n].CCEN (n=0..11)

Address offset: 0x52C + (n × 0x10)

Configure Capture/Compare register CC[n]

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	ACTIVE			Configure the Capture/Compare register
			Disable	0	Capture/Compare register CC[n] Disabled.
			Enable	1	Capture/Compare register CC[n] enabled.

8.10.7.41 TIMEOUT

Address offset: 0x6A4

Timeout after all CPUs gone into sleep state to stop the SYSCOUNTER

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	VALUE			Number of 32Ki cycles

8.10.7.42 INTERVAL

Address offset: 0x6A8

Count to add to CC[0] when the event EVENTS_COMPARE[0] triggers.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	VALUE			Count to add to CC[0]

8.10.7.43 WAKETIME

Address offset: 0x6AC

GRTC wake up time.