The compare value for CC[n] can also be updated by adding a fixed value provided at CC[n].CCADD.VALUE. Based on the CC[n].CCADD.REFERENCE configuration, either the current CC value or the current SYSCOUNTER value is added to the CC[n].CCADD.VALUE to configure the new compare value. If the CC[n] overflows after writing to CC[n].CCADD.VALUE, then EVENTS_COMPARE[n] is generated immediately. Writing to CC[n].CCADD enables the corresponding compare channel.

Writes to CC[n].CCADD are ignored when the SYSCOUNTER is in sleep state.

Periodic interval

In addition to one-shot mode, the CC[0] can produce periodic EVENTS_COMPARE[0] event without any software interaction. The interval between these events can be programmed using INTERVAL register and non-zero interval enables this periodic interval feature. On every EVENTS_COMPARE[0] event, CC[0] becomes CC[0] + INTERVAL.

SYSCOUNTER sleep mode

SYSCOUNTER supports the following power modes:

- SYSCOUNTER is in active state
- SYSCOUNTER is in sleep state - This is the GRTC ultra-low power sleep mode

To save power, SYSCOUNTER automatically goes into sleep state when there is no activity.

Before SYSCOUNTER goes into sleep state, the GRTC configures the internal low frequency timer compare match based on the next expected SYSCOUNTER compare match using CC[n] configuration. An internal event on low frequency timer is generated when the compare match happens.

The internal counter at SYSCOUNTER is not ticking when SYSCOUNTER is in sleep state, the internal low frequency timer is configured as described above.

SYSCOUNTER returns to active state when any one of the following condition is met,

- Any of SYSCOUNTER[n].ACTIVE register is set to Active
- SYSCOUNTER counter value is read
- Any of the following registers are written:
  - MODE
  - CC[n]
  - INTENn/INTENSETn/INTENCLRn/INTENPENDn
  - Write to tasks TASKS_START, TASKS_STOP and TASKS_CLEAR
  - When internal low frequency timer compare match happens
- Any CPU is not sleeping, if MODE.AUTOEN is set

SYSCOUNTER goes back into sleep state when none of the above conditions met. However, the SYSCOUNTER active state can be extended by configuring the number of LFCLK cycles at TIMEOUT register.

On wake up to active state, SYSCOUNTER is updated based on the internal low frequency timer compare match. The status SYSCOUNTER[m].SYSCOUNTERH.BUSY indicates SYSCOUNTER is synchronized and valid after the SYSCOUNTER is woken up.

Before handling next scheduled EVENTS_COMPARE[n] event, GRTC must wake up from the low power state. The WAKETIME register configures the number of LFCLK cycles that GRTC will wake up before the compare event. This duration allows the device sufficient time to power up, initialize, and activate the necessary clocks to accurately generate and handle events from the GRTC SYSCOUNTER. A longer system wake-up time requires a larger WAKETIME value to ensure reliable event processing. When the device is in System OFF, the WAKETIME must cover the system wakeup time from System OFF mode and in addition the required time the system uses to configure GRTC and enable the event.