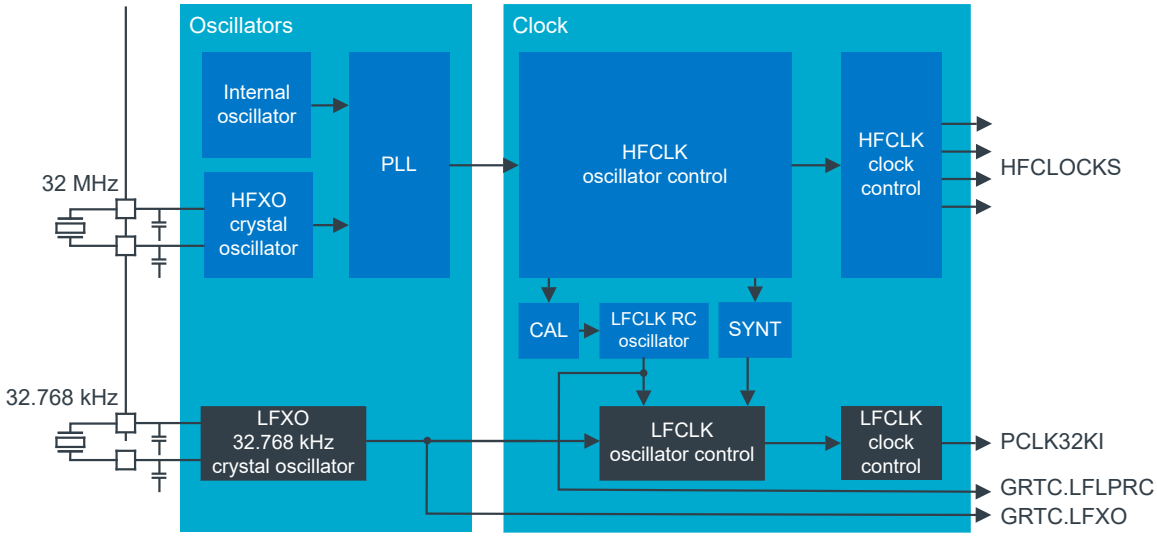

Figure 12: Clock control

5.4.1 HFCLK controller

The HFCLK clock controller provides the following clocks to the system.

Clock	Description
HCLKCORE	MCU power domain and CPU clock where 64 or 128 MHz can be selected
PCLK32M	32 MHz peripheral clock
PCLK16M	16 MHz peripheral clock
PCLK1M	1 MHz peripheral clock

Table 19: Clocks

Clock source	Description
HFINT	128 MHz internal oscillator
HFXO	32 MHz crystal oscillator

Table 20: Sources

The following HFCLK sources generate the HFCLK clocks:

- 128 MHz internal oscillator — PLL is operating in free running mode
- 32 MHz crystal oscillator — PLL is locked on a crystal (XOSC), optionally using built-in capacitors as described in OSCILLATORS — Oscillator control on page 86.

CPUs, peripherals, and other system components automatically request clocks. The HFCLK control passes the request to the power and clock subsystem. When the clocks are running, the HFCLK control distributes them to the components. The CPU clock frequency can be selected, as described in OSCILLATORS — Oscillator control on page 86.

When all HFCLK control requests end, the HFCLK control stops requesting CLOCK from the power and clock subsystem. For example, when the CPU enters sleep or when peripherals have completed their tasks, HFCLK stops CLOCK requests. If there are no requests for HFCLK or PCLK control, the power and clock subsystem automatically stops the clock.