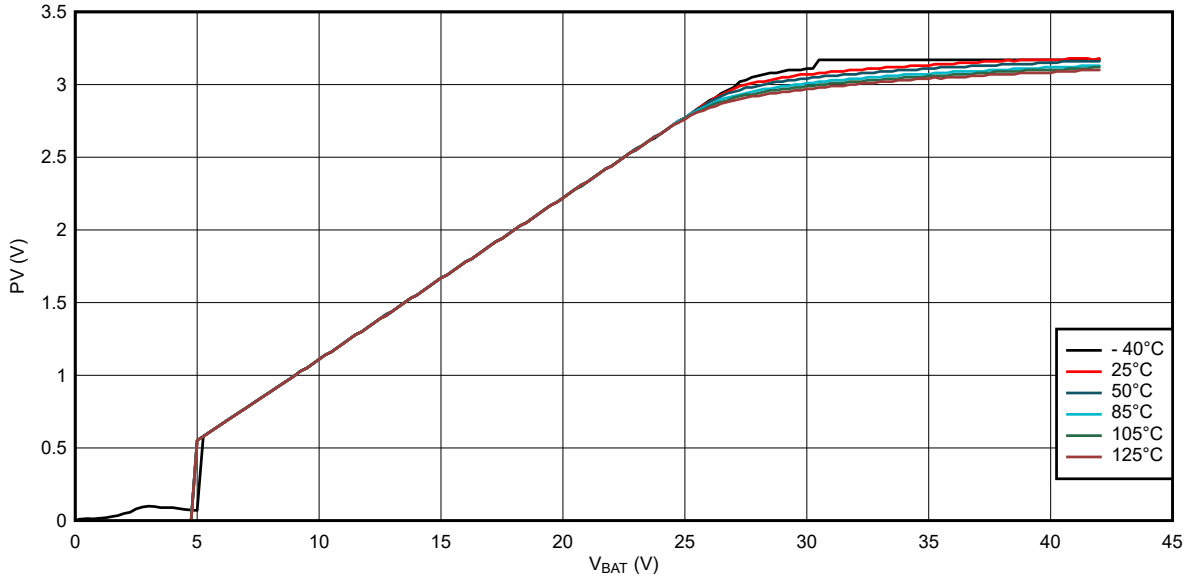

Figure 8-10. V_{BAT} vs PV for TLIN14315RGYQ1 for Different Ambient Temperatures

8.3.22 Protection Features

The device has several protections features that are described as follows.

8.3.22.1 Sleep Wake Error (SWE) Timer

The TLIN1431x-Q1 implements a sleep wake error timer, t_{INACT_FS}. The purpose of the SWE timer is to keep the device and the node from being stuck in a high-power state. This timer is used to place the device into fail-safe or sleep mode due to fault conditions. In Pin mode, the SWE timer starts automatically when entering fail-safe and restart modes. A wake event causes the device to move from sleep mode to restart mode and if V_{CC} does not exceed UV_{CC} before the SWE timer times out the device re-enters sleep mode. This happens in either SPI or pin control modes.

In SPI mode, the SWE timer, when enabled, automatically starts when the device enters fail-safe, restart and standby modes. When the device leaves restart mode and enters standby mode, the processor must initiate a SPI transaction before the SWE timer times out or the device will enter fail-safe mode if enabled or sleep mode. This timer can be disabled at register 8'h1C[7] = 1. If the SWE timer duration is changed, this is accomplished register 8'h1C[6:3]. It can be changed from default of 5 min to between 30 sec to 10 min.

8.3.22.2 Device Reset

The TLIN1431 device can be reset in various ways. In SPI mode, there are three methods to reset the device. Two are accomplished with SPI commands – soft reset and hard reset. Soft reset and hard reset are accomplished by writing 02h or 01h respectively to DEVICE_RST (Address 19h) register. nRST pin can also be used to reset the device by pulling nRST low for t_{nRSTIN} and releasing the pin. nRST pin reset works for both SPI and PIN mode.

When performing a soft reset (SPI Mode), the following takes place:

- Device transitions to restart mode, nRST pin is pulled low for t_{NRST_TOG} and then transitions to standby mode.
- All registers are reset to default values
- All pending interrupts are cleared (unless a fault persists). PWRON interrupt is not cleared by soft reset.
- V_{CC} stays in the same state it was in
- INH stays ON

When performing a hard reset (SPI Mode), the following takes place:

- Similar behavior as power-up
- Device transitions to Init mode – V_{CC} is re-enabled, INH/WKRQ is re-sampled, SPI/PIN mode determination is made