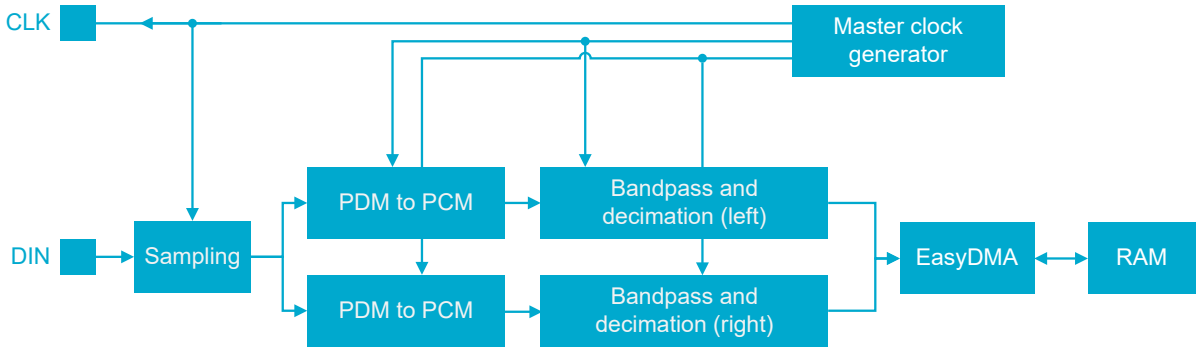

Figure 94: PDM module

8.14.1 Master clock generator

The master clock generator's PRESCALER register allows adjusting the PDM clock's frequency.

The master clock generator does not add any jitter to the HFCLK source chosen. It is recommended (but not mandatory) to use the Xtal as HFCLK source.

The PDM frequency can be adjusted by using PRESCALER, even while the clock generator is running. The PDM clock frequency CLK = PCLK32M/(2*PRESCALER)

Requested PDM frequency f_{pdm} [Hz]	f_{source} [Hz]	RATIO	PRESCALER	Actual PDM frequency f_{actual} [Hz]	Sample frequency [Hz]	Error [%]
1024000	32000000 (PCLK32M)	64	31	1032258	16129	0.81
1280000	32000000 (PCLK32M)	80	25	1280000	16000	0.0
800000	32000000 (PCLK32M)	50	40	800000	16000	0.0

Table 46: Configuration examples

8.14.2 Module operation

By default, bits from the left PDM microphone are sampled on PDM_CLK falling edge, and bits for the right are sampled on the rising edge of PDM_CLK, resulting in two bitstreams. Each bitstream is fed into a digital filter which converts the PDM stream into 16-bit PCM samples, then filters and down-samples them to reach the appropriate sample rate.

The EDGE field in the MODE register allows swapping left and right, so that left will be sampled on rising edge, and right on falling.

The PDM module uses EasyDMA to store the samples coming out from the filters into one buffer in RAM. Depending on the mode chosen in the OPERATION field in the MODE register, memory either contains alternating left and right 16-bit samples (Stereo), or only left(or only right, depending on the value of the EDGE field) 16-bit samples (Mono). To ensure continuous PDM sampling, it is up to the application to update the EasyDMA destination address pointer as the previous buffer is filled.

The continuous transfer can be started or stopped by sending the START and STOP tasks. STOP becomes effective after the current frame has finished transferring, which will generate the STOPPED event. The STOPPED event indicates that all activity in the module is finished, and that the data is available in RAM