Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B B B B B B B B B B B B B B B B B B B B B B B B B B B B A A
Reset 0x00000003				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1**
ID	R/W	Field	Value ID	Value	Description
A	R	MODE			Mode
			CLIC	3	Core Local Interrupt Controller (CLIC) interrupt handling mode
B	RW	BASE			Vector base address
					The value in the BASE field must always be aligned on a 8-byte boundary

8.26.3.4 MTVT

Address offset: 0x307

Machine Trap Vector Table

Holds the base address of the trap vector table, aligned on a 64-byte or greater power-of-two boundary. The actual alignment can be determined by writing ones to the low-order bits then reading them back.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	VAL			Machine Trap Vector Table base address value for CLIC vectored interrupts

8.26.3.5 MCOUNTINHIBIT

Address offset: 0x320

Machine Counter-Inhibit

Register that controls which of the hardware performance-monitoring counters increment.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A
Reset 0x00000005				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1**
ID	R/W	Field	Value ID	Value	Description
A	RW	CY			
			INCREMENT	0x0	MCYCLE increments as usual
			INHIBIT	0x1	MCYCLE doesn't increment
B	RW	IR			
			INCREMENT	0x0	MINSTRET increments as usual
			INHIBIT	0x1	MINSTRET doesn't increment

8.26.3.6 MSCRATCH

Address offset: 0x340

Machine Scratch

Register dedicated for use by machine mode. Typically, it is used to hold a pointer to a machine-mode hart-local context space and swapped with a user register upon entry to an M-mode trap handler.