3.5 Memory

The CPU and peripherals with EasyDMA can access memory through the AMBIX interconnects. The same interconnect is used by the CPU to access peripheral registers. The following figure is a simplified interconnect diagram.

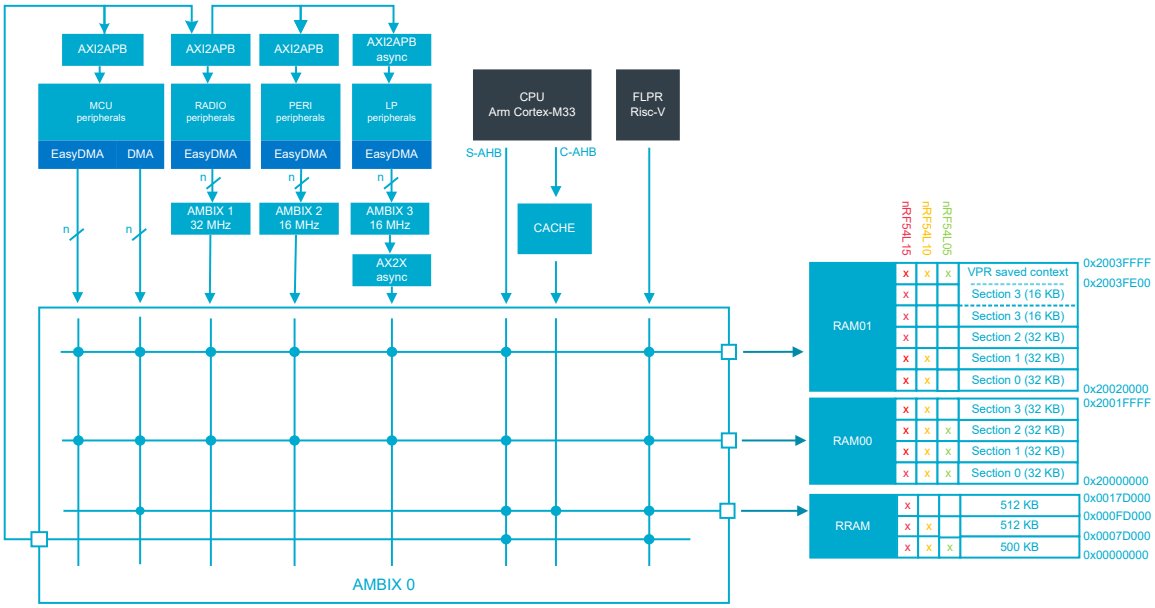

Figure 2: Memory layout

See Block diagram on page 9, AMBA interconnect (AMBIX) on page 26, and EasyDMA on page 27 for more information about the AMBIX interconnects and EasyDMA.

RAM and RRAM memory regions are protected with TrustZone security and are secure after reset. Memory regions can be configured to be non-secure by using MPC — Memory Privilege Controller on page 174.

3.5.1 RAM — Random access memory

The device RAM has regions arranged in one contiguous memory range, accessible from both the CPU and peripherals.

Each RAM region has separate power control for System ON and System OFF mode. This preserves RAM contents in sleep modes or powers off RAM to save power. The sections are illustrated in Memory layout on page 13, and the register interface is described in MEMCONF — Memory configuration on page 44.

3.5.2 NVM — Non-volatile memory

The CPU can read from non-volatile memory (RRAM) an unlimited number of times, but is restricted in how it writes to memory and the number of writes it can perform.

Writing to RRAM is managed by the RRAM controller (RRAMC), see RRAMC — Resistive random access memory controller on page 47.

The Arm Cortex-M33 CPU can access RRAM using the C-AHB (code) bus as shown in Memory layout on page 13. The code bus (C-AHB) interface is used for any instruction fetch or data access fetch to the code region of the Arm memory model. C-AHB bus access is cached, see CACHE — Instruction/data cache on page 29.