Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	ENDADDR			End address for override region n Address must be aligned to override region granularity, see the instance configuration table above for the override region granularity. The least significant bits of this register field are ignored based on the override region granularity and read as zero.

7.8.4.3.6.4 OVERRIDE[n].PERM (n=0..6)

Address offset: 0x810 + (n × 0x20)

Permission settings for override region n

See section *Validate an access* above.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																													D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	READ			Read access
			NotAllowed	0	Read access to override region n is not allowed
			Allowed	1	Read access to override region n is allowed
B	RW	WRITE			Write access
			NotAllowed	0	Write access to override region n is not allowed
			Allowed	1	Write access to override region n is allowed
C	RW	EXECUTE			Software execute
			NotAllowed	0	Software execution from override region n is not allowed
			Allowed	1	Software execution from override region n is allowed
D	RW	SECATTR			Security mapping
			Secure	1	Override region n is mapped in secure memory address space
			NonSecure	0	Override region n is mapped in non-secure memory address space

7.8.4.3.6.5 OVERRIDE[n].PERMMASK (n=0..6)

Address offset: 0x814 + (n × 0x20)

Masks permission setting fields from register OVERRIDE.PERM

See section *Validate an access* above.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																													D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	READ			Read mask
			Masked	0	Permission setting READ in OVERRIDE register will not be applied
			UnMasked	1	Permission setting READ in OVERRIDE register will be applied
B	RW	WRITE			Write mask
			Masked	0	Permission setting WRITE in OVERRIDE register will not be applied
			UnMasked	1	Permission setting WRITE in OVERRIDE register will be applied
C	RW	EXECUTE			Execute mask
			Masked	0	Permission setting EXECUTE in OVERRIDE register will not be applied
			UnMasked	1	Permission setting EXECUTE in OVERRIDE register will be applied