LPCOMP is operational in both System ON and System OFF mode when enabled through the ENABLE register. See POWER — Power control on page 92 for more information about power modes. Entering System OFF is not allowed when a READY event is pending to be generated.

All LPCOMP registers, including ENABLE, are classified as retained registers when the LPCOMP is enabled. However, when the device wakes up from System OFF, all LPCOMP registers are reset.

LPCOMP can wake up the system from System OFF by asserting the ANADETECT signal. The ANADETECT signal can be derived from any of the event sources that generate UP, DOWN, and CROSS events. If wakeup from System OFF occurs, only the ANADETECT signal is generated. See the ANADETECT register (ANADETECT on page 359) for more information on configuring the ANADETECT signal.

The immediate value of the LPCOMP can be sampled to RESULT on page 357 by triggering the SAMPLE task.

See RESETREAS on page 104 for more information on how to detect a wakeup from LPCOMP.

8.12.2 Shared resources

LPCOMP shares analog resources with SAADC. While it is possible to use the SAADC at the same time as the LPCOMP, selecting the same analog input pin for both modules is not supported.

Additionally, LPCOMP shares registers and other resources with other peripherals that have the same ID as the LPCOMP. See Peripherals with shared ID on page 214 for more information.

The LPCOMP peripheral should not be disabled (by writing to the ENABLE register) before the peripheral has stopped. Failing to do so may result in unpredictable behavior.

8.12.3 Pin configuration

The LPCOMP.PSEL register is used to select an analog input pin for LPCOMP. The pins available are **AIN0** through **AIN7**.

See GPIO — General purpose input/output on page 274 for more information about the pins. Similarly, you can use EXTREFSEL on page 359 to select one of the analog reference input pins, **AIN0** and **AIN1**, as input for AREF if it is selected in EXTREFSEL on page 359. The selected analog pins are acquired by LPCOMP when it is enabled through ENABLE on page 358.

8.12.4 Registers

Instances

Instance	Domain	Base address	TrustZone			Split	Description
			Map	Att	DMA	access	
LPCOMP : S LPCOMP : NS	GLOBAL	0x50106000 0x40106000	US	S	NA	No	Low-power comparator LPCOMP

Register overview

Register	Offset	TZ	Description
TASKS_START	0x000		Start comparator
TASKS_STOP	0x004		Stop comparator
TASKS_SAMPLE	0x008		Sample comparator value. This task requires that LPCOMP has been started by the START task.
SUBSCRIBE_START	0x080		Subscribe configuration for task START
SUBSCRIBE_STOP	0x084		Subscribe configuration for task STOP
SUBSCRIBE_SAMPLE	0x088		Subscribe configuration for task SAMPLE

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