Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				W V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
U	RW W1S	MHRMATCH			Write '1' to enable interrupt for event MHRMATCH
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
V	RW W1S	SYNC			Write '1' to enable interrupt for event SYNC MODE=Ble_LR125Kbit, Ble_LR500Kbit, or Ieee802154_250Kbit: A possible preamble has been received. However, due to the sporadic reception of noise, this event can be falsely triggered. For MODE=Nrf_1Mbit, Nrf_2Mbit, Ble_1Mbit, or Ble_2Mbit: A possible preamble and the first two bytes of the address field has been received. The event can be generated falsely also in this mode. It is also possible that the event is not generated, or not generated before the ADDRESS event.
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
W	RW W1S	CTEPRESENT			Write '1' to enable interrupt for event CTEPRESENT
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

8.17.14.95 INTENSET11

Address offset: 0x4AC

Enable interrupt

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW W1S	PLLREADY			Write '1' to enable interrupt for event PLLREADY
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
B	RW W1S	RXADDRESS			Write '1' to enable interrupt for event RXADDRESS
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
C	RW W1S	AUXDATADMAEND			Write '1' to enable interrupt for event AUXDATADMAEND
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled