data words have been transmitted. Similarly, with reception enabled in CONFIG.RXEN, the RXPTRUPD event will be generated for every

```
ceil(RXTXD.MAXCNT/4)
```

data words.

The FRAMESTART event is generated synchronously to the active LRCK edge at the beginning of a frame after transmitting

```
ceil(RXTXD.MAXCNT/4)
```

data words. The initial FRAMESTART event is generated at the first active edge of LRCK after the START task has been triggered. The FRAMESTART event is only defined for transmitting full left and right sample pairs. If RXTXD.MAXCNT is configured so that the frame ends between the left and right sample pairs, the missing left or right sample pairs will be transmitted as zeros.

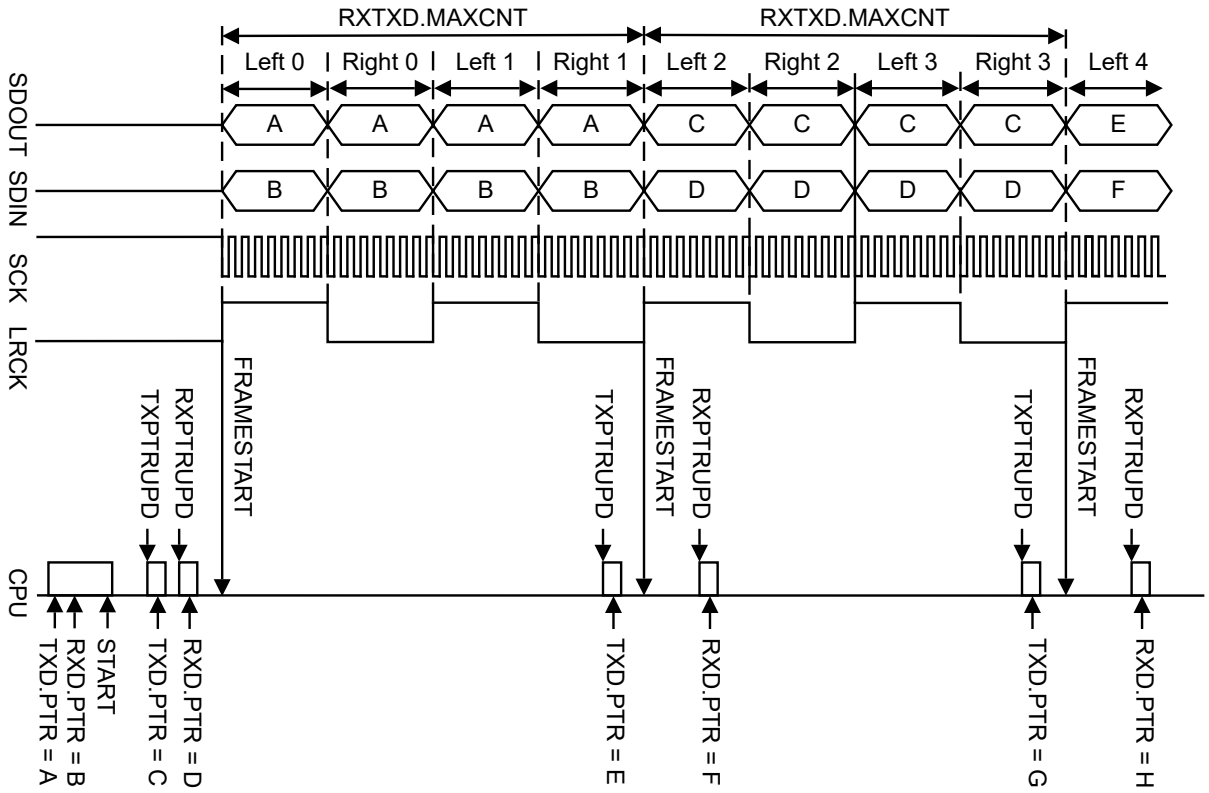

Figure 65: Transmitting and receiving. CONFIG.FORMAT = Aligned, CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo, RXTXD.MAXCNT = 4

8.11.3 Left right clock (LRCK)

The left right clock (LRCK), often referred to as word clock, sample clock, or word select in I^2S context, is the clock defining the frames in serial bitstreams sent and received on SDOUT and SDIN, respectively.

In I2S format, each frame contains one left and/or right sample pair. The left sample is transferred during the low half period of LRCK, followed by the right sample being transferred during the high half period of LRCK.

In Aligned format, each frame contains one left and/or right sample pair. The left sample is transferred during the high half period of LRCK, followed by the right sample being transferred during the low half period of LRCK.

For mono, the frame will contain only zeros for the unused half period of LRCK.