

This event triggers after the last SEQ[1] completion of the loop, and only if looping was enabled (LOOP > 0) when the sequence playback was started.

8.15.5.12 EVENTS RAMUNDERFLOW

Address offset: 0x120

Emitted when retrieving from RAM does not complete in time for the PWM module

8.15.5.13 EVENTS_DMA

Peripheral events.

8.15.5.13.1 EVENTS DMA.SEQ[n] (n=0..1)

Peripheral events.

8.15.5.13.1.1 EVENTS_DMA.SEQ[n].END (n=0..1)

Address offset: 0x124 + (n × 0xC)

Generated after all MAXCNT bytes have been transferred

8.15.5.13.1.2 EVENTS_DMASEQ[n].READY (n=0..1)

Address offset: 0x128 + (n × 0xC)

Generated when EasyDMA has buffered the .PTR and .MAXCNT registers for the channel, allowing them to be written to prepare for the next sequence.