Table 8-18. WAKE_PIN_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TWK_CYC_SET	R/W	0b	Sets the t_{WK_CYC} time (µs) for sampling the WAKE pin status (used for cyclic sensing) 0b = 30 1b = 75 **Note** NOTE: $t_{WK\_CYC\_SET}$ works with timer1 and timer2. When using 75 µs t_{WK_CYC}, 100 µs TIMER1/2_ON_WIDTH cannot be used.
4-3	nINT_SEL	R/W	00b	nINT configuration selection: active low 00b = Global interrupt 01b = Watchdog failure output 10b = Reserved 11b = Wake request
2	RXD_WK_CONFIG	R/W	0b	Configures RXD pin behavior from a wake event 0b = Pulled low 1b = Toggle
1-0	WAKE_LEVEL	R/W	10b	WAKE pin threshold level; Mid-point value in 2 V window. 00b = 2.5 V 01b = 2.8 V 10b = 3 V 11b = 3.3 V

8.6.9 WD_CONFIG_1 Register (Address = 13h) [reset = 90h]

WD_CONFIG_1 is shown in Figure 8-63 and described in Table 8-19.

Return to Summary Table.

Watchdog configuration register.

Figure 8-63. WD_CONFIG_1 Register

7	6	5	4	3	2	1	0
WD_CONFIG		WD_PRE		RSVD			
R/W-10b		R/W-01b		R-0000b			

Table 8-19. WD_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_CONFIG	R/W	10b	Watchdog configuration 00b = Disabled 01b = Timeout 10b = Window 11b = Reserved
5-4	WD_PRE	R/W	01b	Watchdog prescalar 00b = Factor 1 01b = Factor 2 10b = Factor 3 11b = Factor 4
3-0	RSVD	R	0000b	Reserved

8.6.10 WD_CONFIG_2 Register (Address = 14h) [reset = 02h]

WD_CONFIG_2 is shown in Figure 8-64 and described in Table 8-20.

Return to Summary Table.

Watchdog timer and error counter register.