7.8.1.7.62 IKG.SOFTRST

Address offset: 0x3028

SoftRst register.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	SOFTRST			Software reset:
					This bit is not cleared automatically.
			NORMAL	0	Normal mode.
			KEY	1	The Isolated Key Generation logic and the keys are reset.

7.8.1.7.63 IKG.HWCONFIG

Address offset: 0x302C

HwConfig register.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	K	K	K	K	J	J	J	J	I	I	I	I	H	H	H	H	G	G	G	F	E	E	D	C	B	B	B	B	A	A	A	A
Reset 0xCC4C8312	**1**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**0**

ID	R/W	Field	Value ID	Value	Description
A	R	NBSYMKEYS			Number of Symmetric Keys generated.
B	R	NBPRIVKEYS			Number of Private Keys generated.
C	R	IKGCM			Countermeasures for IKG operations are implemented when 1.
D	R	HWHEALTHTEST			CTR_DRBG health test is implemented when 1.
E	R	CURVE			ECC curve for IKG (input).
					Note: value 3 is reserved
			P256	0	P256.
			P384	1	P384.
			P521	2	P521.
F	R	DF			Derivation function is implemented in the CTR_DRBG when 1.
G	R	KEYSIZE			AES Key Size support for the AES Core embedded in the CTR_DRBG.
					[0]: supports AES128 when 1 [1]: supports AES192 when 1 [2]: supports AES256 when 1
			AES128	1	supports AES128
			AES192	2	supports AES192
			AES256	4	supports AES256
H	R	ENTROPYINPUTLENGTH			Value of g_entropy_input_length/32.
I	R	NONCELENGTH			Value of g_nonce_length/32.
J	R	PERSONALIZATIONSTRINGLENGTH			Value of g_personalization_string_length/32.
K	R	ADDITIONALINPUTLENGTH			Value of g_additional_input_length/32.

7.8.2 GLITCHDET — Voltage glitch detectors

The system has voltage glitch detectors.

The voltage glitch detectors are automatically enabled after reset. To save power, the glitch detectors must be disabled when not in use.