11.19.9 Timing specifications for GPIO port P2 using Extra high drive strength

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SPIS,VSO}$	CLK edge to SDO valid			15	ns
$t_{SPIS,HSO}$	SDO hold time after CLK edge	3			ns
$t_{SPIS,SUSI}$	SDI to CLK edge setup time	6			ns
$t_{SPIS,HSI}$	CLK edge to SDI hold time	1			ns

11.20 SWDP Electrical specification

11.20.1 SW-DP

Symbol	Description	Min.	Typ.	Max.	Units
R_{pull}	Internal SWDIO and SWDCLK pull up/down resistance		14		kΩ
f_{SWDCLK}	SWDCLK frequency	0.125		8	MHz
t_{SUI}	SWDIO input setup before SWDCLK	20			ns
t_{HK}	SWDIO input hold after SWDCLK	1			ns
t_{VO}	SWDCLK to SWDIO output valid			36	ns
t_{HO}	SWDIO output hold after SWDCLK	5			ns

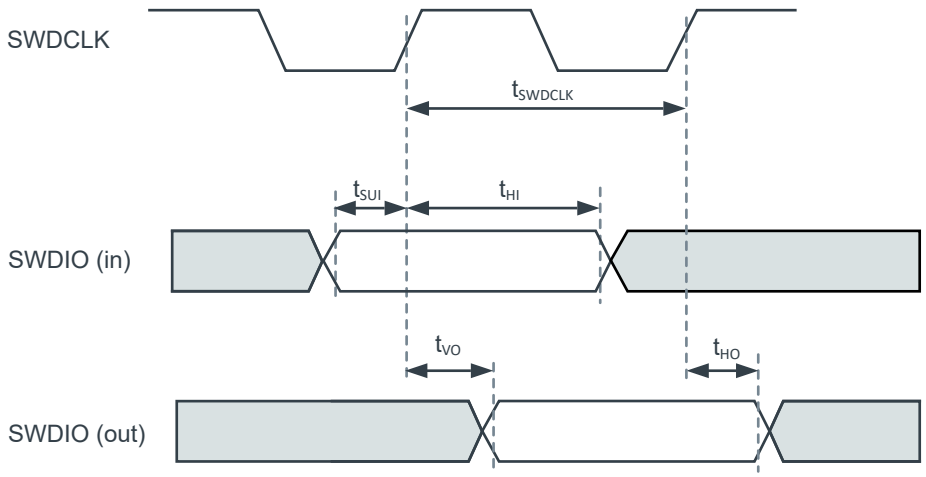

Figure 199: SWD timing diagram

11.20.2 Trace port

Symbol	Description	Min.	Typ.	Max.	Units
T_{cyc}	Clock period, as defined by Arm in Embedded Trace Macrocell Architecture Specification	15.625		250	ns