The master clock generator does not add any jitter to the clock source chosen.

The master clock generator is enabled/disabled using CONFIG.MCKEN on page 342, and the generator is started or stopped by the START or STOP tasks respectively.

The MCK frequency can be adjusted on-the-fly by using MCKFREQ.

In Master mode, the LRCK and the SCK frequencies are closely related as both are derived from MCK and set indirectly through CONFIG.RATIO on page 343 and CONFIG.SWIDTH on page 344.

When configuring these registers, the user is responsible for fulfilling the following requirements:

1. The SCK frequency can never exceed the MCK frequency.
2. The MCK/LRCK ratio shall be a multiple of 2 * CONFIG.SWIDTH.

The MCK signal can be routed to an output pin (specified in PSEL.MCK) to supply external I^{2}S devices that require the MCK to be supplied from the outside.

When operating in Slave mode, the I^{2}S module does not use the MCK and the MCK generator does not need to be enabled.

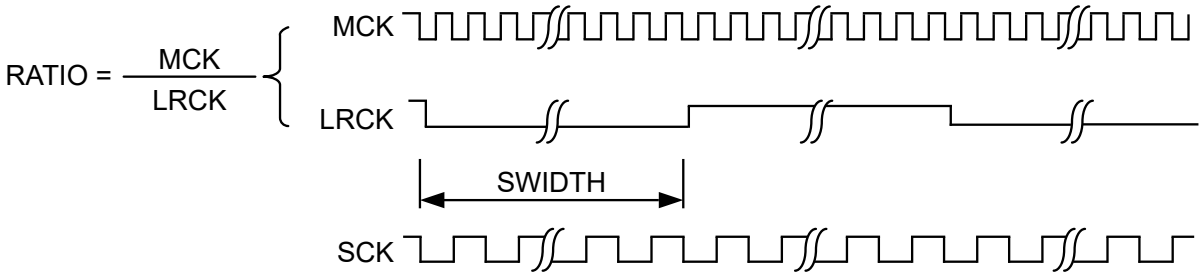

Figure 69: Relation between RATIO, MCK and LRCK

8.11.5.1 Configuration examples

The following are example configurations for popular sample rates.

Source frequency [Hz]	Requested LRCK [Hz]	RATIO	Requested MCK [Hz]	MCKFREQ	MCK [Hz]	LRCK [Hz]	LRCK error [%]
32000000	16000	32	512000	68173824	507936	15873	-0.8
32000000	16000	64	1024000	135274496	1032258	16129	0.8
32000000	16000	256	4096000	516685824	4000000	15625	-2.3
32000000	32000	32	1024000	135274496	1032258	32258	0.8
32000000	32000	64	2048000	266350592	2000000	31250	-2.3
32000000	32000	256	8192000	974741504	8000000	31250	-2.3
32000000	44100	32	1411200	185319424	1391304	43478	-1.4
32000000	44100	64	2822400	362815488	2909090	45455	3.1
32000000	48000	32	1536000	201326592	1523809	47619	-0.8
32000000	48000	64	3072000	393428992	3200000	50000	4.2
32000000	96000	32	3072000	393428992	3200000	100000	4.2
32000000	96000	64	6144000	752402432	6400000	100000	4.2

Table 42: Configuration examples for 32 MHz PCLK