

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				B																								A A A A A A A							
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value		Description																													
A	RW	CHIDX		[0..255]		DPPI channel that event <b>PLLREADY</b> will publish to																													
B	RW	EN																																	
			Disabled	0	Disable publishing																														
			Enabled	1	Enable publishing																														

#### 8.17.14.86 PUBLISH\_RXADDRESS

Address offset: 0x3BC

Publish configuration for event **RXADDRESS**

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				B																								A A A A A A A A							
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value		Description																													
A	RW	CHIDX		[0..255]		DPPI channel that event <b>RXADDRESS</b> will publish to																													
B	RW	EN																																	
			Disabled	0	Disable publishing																														
			Enabled	1	Enable publishing																														

#### 8.17.14.87 PUBLISH\_AUXDATADMAEND

Address offset: 0x3C0

Publish configuration for event **AUXDATADMAEND**

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
ID				B																								A				A	A	A	A	A	A	A
Reset 0x00000000				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
ID	R/W	Field	Value ID	Value		Description																																
A	RW	CHIDX		[0..255]		DPPI channel that event <a href="#">AUXDATADMAEND</a> will publish to																																
B	RW	EN																																				
			Disabled	0	Disable publishing																																	
			Enabled	1	Enable publishing																																	

#### 8.17.14.88 PUBLISH\_CSTONESEND

Address offset: 0x3C8

Publish configuration for event **CSTONESEND**

The results are available in the CSTONE registers

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
ID				B																								A				A	A	A	A	A	A	A
Reset 0x00000000				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
ID	R/W	Field	Value ID	Value		Description																																
A	RW	CHIDX		[0..255]		DPPI channel that event <b>CSTONESEND</b> will publish to																																
B	RW	EN																																				
			Disabled	0	Disable publishing																																	
			Enabled	1	Enable publishing																																	