8.6.25 PWM2_CNTL2 (Address = 23h) [reset = 0h]

PWM2_CNTL2 is shown in Figure 8-79 and described in Table 8-35

Return to Summary Table.

Set the two most significant bit for the 10-bit PWM2. These work with register h'24 PWM2_CNTL3.

Figure 8-79. PWM2_CNTL2 Register

7	6	5	4	3	2	1	0
PWM2_RSVD						PWM2_DC_MSB	
R-0b						R/W-00b	

Table 8-35. PWM2_CNTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	PWM2_RSVD	R	0b	Reserved
1-0	PWM2_DC_MSB	R/W	00b	Most significant two bits for 10-bit PWM2 duty cycle select. Works with 'h24[7:0] 00b = 100% off when used with 'h24[7:0] and it is 00h xxb = on time with an increase of ~ 0.1% when used with 'h24[7:0] 11b = 100% of when used with 'h24[7:0] and it is FFh

8.6.26 PWM2_CNTL3 (Address = 24h) [reset = 0h]

PWM2_CNTL3 is shown in Figure 8-80 and described in Table 8-36

Return to Summary Table.

Bits 0 - 7 of the 10-bit PWM2. Used with register h'23[1:0] PWM2_CNTL2.

Figure 8-80. PWM2_CNTL3 Register

7	6	5	4	3	2	1	0
PWM2_DC							
R/W-00h							

Table 8-36. PWM2_CNTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWM2_DC	R/W	00h	Bits 0 - 7 of the 10-bit PWM2 00h = 100% off when used with 'h23[1:0] = 00b xxh = On time with an increase of ~ 0.1% when used with 'h23[1:0] FFh = 100% on when used with 'h23[1:0] = 11b

Note

Minimum on-time during PWM is limited to the on and off-time of the high side switch. This will make certain PWM values unusable like 00 0000 0001.

8.6.27 TIMER1_CONFIG (Address = 25h) [reset = 00h]

TIMER1_CONFIG is shown in Figure 8-81 and described in Table 8-37

Return to Summary Table.

Sets timer 1 period and on time. Careful selection is important as selecting a 200ms on width and a 10ms period is not possible.

Figure 8-81. TIMER1_CONFIG Register

7	6	5	4	3	2	1	0
TIMER1_ON_WIDTH				TIMER1_RSVD	TIMER1_PERIOD		