

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
ID	H	H	H	H	G	G	G	F	F	F	E	D	D	D	C	C	C	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00023282	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	1	0	1	0	0	0	0	0	1	0		
ID	R/W	Field	Value ID	Value	Description																													
			125ns	6	0.125us																													
G	RW	REPEATPATTERN			Repeat every antenna pattern N times.																													
		NoRepeat	0		Do not repeat (1 time in total)																													
H	RW	AGCBACKOFFGAIN			Gain will be lowered by the specified number of gain steps at the start of CTE																													
Note: First LNAGAIN gain drops, then MIXGAIN, then AAEGAIN																																		

8.17.14.123 DFECTRL2

Address offset: 0xD14

Start offset for Direction finding

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
ID	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	R/W	Field	Value ID	Value	Description																													
A	RW	TSWITCHOFFSET			Signed value offset after the end of the CRC before starting switching in number of 16M cycles																													
B	RW	TSAMPLEOFFSET			Signed value offset before starting sampling in number of 16M cycles relative to the beginning of the REFERENCE state - 12 us after switching start																													

8.17.14.124 SWITCHPATTERN

Address offset: 0xD28

GPIO patterns to be used for each antenna

Maximum 8 GPIOs can be controlled. To secure correct signal levels on the pins, the pins must be configured in the GPIO peripheral as described in Pin configuration.

If the total number of antenna slots is bigger than the number of patterns, we loop back to the pattern used after the reference pattern.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ID	R/W	Field	Value ID	Value	Description																													
A	RW	SWITCHPATTERN			Fill array of GPIO patterns for antenna control																													
					The GPIO pattern array size is 40 entries.																													
					When written, bit n corresponds to the GPIO configured in PSEL.DFEGPIO[n].																													
					When read, returns the number of GPIO patterns written since the last time the array was cleared. Use CLEARPATTERN to clear the array.																													

8.17.14.125 CLEARPATTERN

Address offset: 0xD2C

Clear the GPIO pattern array for antenna control