allow for this, while following the DMA.RX.END event, the DMA.RX.AMOUNT register will indicate the actual number of bytes received.

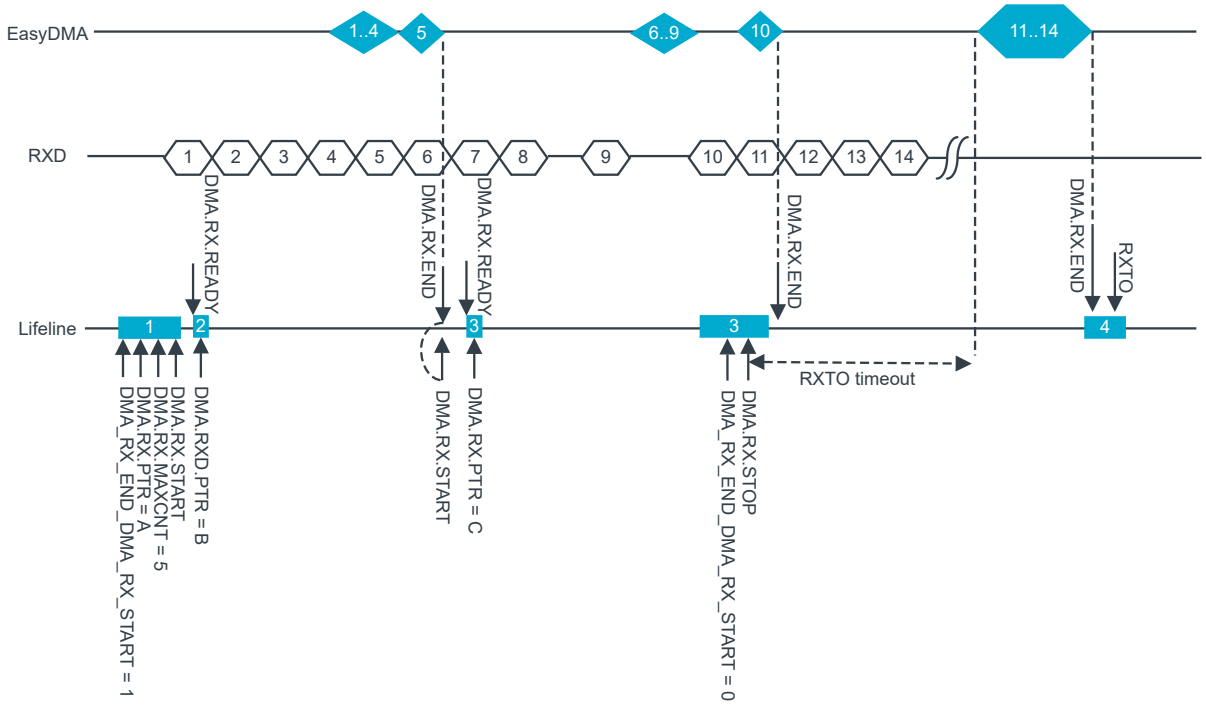


*Figure 161: UARTE reception with forced stop through DMA.RX.STOP*

If hardware flow control is enabled in the HWFC field in the CONFIG register, the RTS signal will be deactivated when the receiver is stopped via the DMA.RX.STOP task, or when UARTE can only receive three more bytes in its internal RX FIFO.

With flow control disabled, the UARTE will function in the same way as when the flow control is enabled, except that the RTS line will not be used. This means that no signal will be generated when UARTE is only able to receive three additional bytes in its internal RX FIFO. Data received when the internal RX FIFO is full, will be lost.

The UARTE receiver is least active when it is stopped, consuming the least amount of energy. This is before it is started via DMA.RX.START, or after it has been stopped via DMA.RX.STOP and the RXTO event has been generated. See POWER — Power control on page 92 for more information about power modes.

## 8.25.5 Data frame size

UARTE implements a configurable data frame size of 4 bits to 9 bits and is set in the register CONFIG on page 743. If a value greater than 9 or less than 4 is written to this register, the frame size will be set to 8 bits and the register will read back a value of 8.

When UARTE is used with the 9 bit frame size, a 9th bit is added after the MSB of the 8 bit data frame, and before the parity and stop bits, as shown in the following figure. This bit indicates if the 8 bit data is an address or data. If the 9th bit is `1`, the 8 bit data is interpreted as an address. If the 9th bit is `0`, the 8 bit data is interpreted as data.

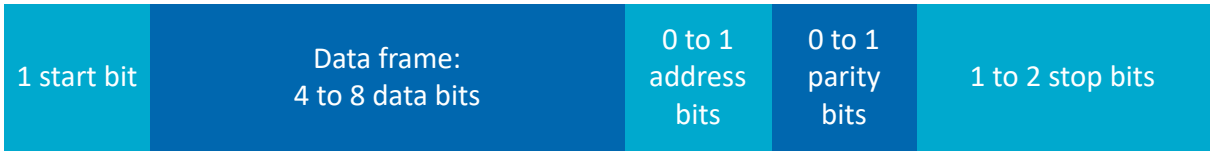


*Figure 162: UARTE frame*