



Figure 134: Example of limits monitoring on channel 'n'

Note that when setting the limits, `CH[n].LIMIT.HIGH` shall always be higher than or equal to `CH[n].LIMIT.LOW`. In other words, an event can be generated only when the input signal has been sampled outside of the defined limits. It is not possible to fire an event when the input signal is inside a defined range by swapping high and low limits.

The comparison to limits always takes place, there is no need to enable it. If comparison is not required on a channel, the software shall simply ignore the related events. In that situation, the value of the limits registers is irrelevant, so it does not matter if `CH[n].LIMIT.LOW` is lower than `CH[n].LIMIT.HIGH` or not.

8.18.10 Performance factors

Clock jitter, affecting sample timing accuracy, and circuit noise can affect ADC performance.

Jitter can be between `START` tasks or from `START` task to acquisition. `START` timer accuracy and startup times of regulators and references will contribute to variability. Sources of circuit noise may include CPU activity and the DC/DC regulator. Best ADC performance is achieved using `START` timing based on the TIMER module, HFXO clock source, and Constant Latency mode.