

| ID | Base address | Instance | TrustZone | | | Split access | Description |
|-----|--------------|---------------|-----------|-----|-----|--------------|---|
| | | | Map | Att | DMA | | |
| 65 | 0x50041000 | MPC00 | HF | S | NA | No | Memory privilege controller MPC00 |
| 66 | 0x50042000 | DPPIC00 : S | US | S | NA | Yes | DPPI controller DPPIC00 |
| 66 | 0x40042000 | DPPIC00 : NS | | | | | |
| 67 | 0x50043000 | PPIB00 : S | US | S | NA | No | PPI bridge PPIB00 |
| 67 | 0x40043000 | PPIB00 : NS | | | | | |
| 68 | 0x50044000 | PPIB01 : S | US | S | NA | No | PPI bridge PPIB01 |
| 68 | 0x40044000 | PPIB01 : NS | | | | | |
| 69 | 0x50045000 | KMU | HF | S | NSA | No | Key management unit |
| 70 | 0x50046000 | AAR00 : S | US | S | SA | No | Accelerated address resolver 00 |
| 70 | 0x40046000 | AAR00 : NS | | | | | |
| 70 | 0x50046000 | CCM00 : S | US | S | SA | No | AES CCM mode encryption CCM00, running on HCLKCORE |
| 70 | 0x40046000 | CCM00 : NS | | | | | AES ECB mode encryption 00 |
| 71 | 0x50047000 | ECB00 : S | US | S | SA | No | When configuring this peripheral's DMA security using SPU configuration (DMASEC field of SPU->PERIPH[apb_slave_index]), use apb_slave_index 6 (same as AAR00 and CCM00) |
| 71 | 0x40047000 | ECB00 : NS | | | | | |
| 72 | 0x50048000 | CRACEN | HF | S | NSA | No | Crypto accelerator |
| 74 | 0x5004A000 | SPIM00 : S | US | S | SA | No | SPI controller SPIM00 |
| 74 | 0x4004A000 | SPIM00 : NS | | | | | |
| 74 | 0x5004A000 | SPIS00 : S | US | S | SA | No | SPI peripheral SPIS00 |
| 74 | 0x4004A000 | SPIS00 : NS | | | | | |
| 74 | 0x5004A000 | UARTE00 : S | US | S | SA | No | Universal asynchronous receiver/transmitter UARTE00 |
| 74 | 0x4004A000 | UARTE00 : NS | | | | | |
| 75 | 0x5004B000 | GLITCHDET | HF | S | NA | No | Glitch detectors |
| 75 | 0x5004B000 | RRAMC | HF | S | NA | No | RRAM Non-Volatile Memory Controller |
| 76 | 0x5004C000 | VPRO0 : S | US | NS | NSA | No | FLPR - VPR peripheral registers |
| 76 | 0x4004C000 | VPRO0 : NS | | | | | |
| 80 | 0x50050400 | GPIOHSPADCTRL | HF | S | NA | No | GPIO HS pad control GPIOHSPADCTRL |
| 80 | 0x50050400 | P2 : S | US | S | NA | Yes | General purpose input and output, port P2 |
| 80 | 0x40050400 | P2 : NS | | | | | Does not support pin sense mechanism, and DETECTMODE register has no effect. Supports extra high drive (DRIVE0=E0, DRIVE1=E1). |
| 82 | 0x50052000 | CTRLAP : S | US | S | NSA | No | Control access port CPU side |
| 82 | 0x40052000 | CTRLAP : NS | | | | | |
| 83 | 0x50053000 | TAD : S | US | S | NA | No | Trace and debug control |
| 83 | 0x40053000 | TAD : NS | | | | | |
| 85 | 0x50055000 | TIMER00 : S | US | S | NA | No | Timer TIMER00 |
| 85 | 0x40055000 | TIMER00 : NS | | | | | |
| 128 | 0x50080000 | SPU10 | HF | S | NA | No | System protection unit SPU10 |
| 130 | 0x50082000 | DPPIC10 : S | US | S | NA | Yes | DPPI controller DPPIC10 |
| 130 | 0x40082000 | DPPIC10 : NS | | | | | |
| 131 | 0x50083000 | PPIB10 : S | US | S | NA | No | PPI bridge PPIB10 |
| 131 | 0x40083000 | PPIB10 : NS | | | | | |
| 132 | 0x50084000 | PPIB11 : S | US | S | NA | No | PPI bridge PPIB11 |
| 132 | 0x40084000 | PPIB11 : NS | | | | | |
| 133 | 0x50085000 | TIMER10 : S | US | S | NA | No | Timer TIMER10 |
| 133 | 0x40085000 | TIMER10 : NS | | | | | |
| 135 | 0x50087000 | EGU10 : S | US | S | NA | No | Event generator unit EGU10 |
| 135 | 0x40087000 | EGU10 : NS | | | | | |