## 8.27.5.16 RREN

Address offset: 0x508

Enable register for reload request registers

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID | | | | | | | | | | | | | | | | | | | | | | | | | | | | H | G | F | E | D | C | B | A |
| **Reset 0x00000001** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| ID | R/W | Field | Value ID | Value | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A-H | RW | RR[i] (i=0..7) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disabled | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enabled | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 8.27.5.17 CONFIG

Address offset: 0x50C

Configuration register

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C | | | B | | | A |
| **Reset 0x00000001** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| ID | R/W | Field | Value ID | Value | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | RW | SLEEP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure WDT to either be paused, or kept running, while the CPU is sleeping | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | **Note:** This feature will not affect power consumed by the WDT. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pause | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pause WDT while the CPU is sleeping | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Run | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep WDT running while the CPU is sleeping | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | RW | HALT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Configure WDT to either be paused, or kept running, while the CPU is halted by the debugger | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Pause | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Pause WDT while the CPU is halted by the debugger | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Run | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Keep WDT running while the CPU is halted by the debugger | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | RW | STOPEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Allow stopping WDT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Disable | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Do not allow stopping WDT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Allow stopping WDT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 8.27.5.18 TSEN

Address offset: 0x520

Task stop enable

| Bit number | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID | | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **Reset 0x00000000** | | | | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| ID | R/W | Field | Value ID | Value | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | W | TSEN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Allow stopping WDT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Enable | 0x6E524635 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Value to allow stopping WDT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## 8.27.5.19 RR[n] (n=0..7)

Address offset: 0x600 + (n × 0x4)