8.1.10 Interrupts

All peripherals support interrupts generated by events.

A peripheral can occupy single or multiple interrupts. For single interrupts, the interrupt number follows the peripheral ID. For example, the peripheral with ID=4 is connected to interrupt number 4 in the nested vectored interrupt controller (NVIC). In this case, only single INTEN registers are available.

Events generated by a peripheral can be configured to generate interrupts using registers INTEN, INTENSET, and INTENCLR. Multiple events can be enabled to generate interrupts simultaneously. Event registers in the peripheral register event group indicate the source.

Some peripherals implement only INTENSET and INTENCLR registers. The INTEN register is not available on those peripherals. See the individual peripheral chapters for details. In all cases, reading back the INTENSET or INTENCLR register returns the same information as INTEN.

The INTPEND register contains the interrupt pending status of events generated by a peripheral. This is a read-only register.

Peripherals implementing multiple interrupts have several INTEN registers that follow the convention of INTENn, where n is the interrupt number from the peripheral. This also applies to corresponding INTPEND, INTENSET, and INTENCLR registers. This feature enables any event to generate an interrupt from the peripheral.

Peripherals implementing more than 32 events have access to multiple INTEN registers that follow the convention of INTENn, where n is the event group number. The 32 lowest events in the peripheral make event group 0. The next 32 events in the peripheral make event group 1, and so on. This convention is also applicable for corresponding INTPEND, INTENSET, and INTENCLR registers.

Peripherals implementing both multiple interrupts and more than 32 events have multiple INTEN registers. In this case, registers follow the convention of INTENnm, where n is interrupt number from the peripheral and m is event group number. This convention is also applicable for corresponding INTPEND, INTENSET, and INTENCLR registers.

Each event implemented in the peripheral is associated with a specific bit position in the INTEN, INTENSET, and INTENCLR registers.

To ensure the lowest possible power consumption while in sleep, perform either of the following steps on any pending interrupts:

- Clear the pending interrupt by writing `0` to the corresponding EVENT register
- Disable the interrupt by using the INTEN or INTENCLR registers

This has to be done even if the peripheral is disabled in its ENABLE or POWER register.

The relationship between tasks, events, shortcuts, and interrupts is illustrated in Peripheral interface on page 213.

8.1.10.1 Interrupt clearing and disabling

Interrupts must be cleared by writing `0` to the corresponding EVENT register.

Interrupts are immediately re-triggered until cleared. Routines for software interrupt services continue to execute, even if a new event has not been received.

8.2 Instantiation

ID	Base address	Instance	TrustZone			Split access	Description
			Map	Att	DMA		
64	0x50040000	SPU00	HF	S	NA	No	System protection unit SPU00