

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				R Q P O N M L K J I H G F E D C B A																															
Reset 0x00000000				0 0																															
ID	R/W	Field	Value ID	Value	Description																														
F	R	PWMPERIODEND			Read pending status of interrupt for event <a href="#">PWMPERIODEND</a>																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
G	R	LOOPSDONE			Read pending status of interrupt for event <a href="#">LOOPSDONE</a>																														
					This event triggers after the last SEQ[1] completion of the loop, and only if looping was enabled (LOOP > 0) when the sequence playback was started.																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
H	R	RAMUNDERFLOW			Read pending status of interrupt for event <a href="#">RAMUNDERFLOW</a>																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
I	R	DMASEQ0END			Read pending status of interrupt for event <a href="#">DMASEQ0END</a>																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
J	R	DMASEQ0READY			Read pending status of interrupt for event <a href="#">DMASEQ0READY</a>																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
K	R	DMASEQ0BUSERROR			Read pending status of interrupt for event <a href="#">DMASEQ0BUSERROR</a>																														
					When this event is generated, the address which caused the error can be read from the BUSERRORADDRESS register.																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
L	R	DMASEQ1END			Read pending status of interrupt for event <a href="#">DMASEQ1END</a>																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
M	R	DMASEQ1READY			Read pending status of interrupt for event <a href="#">DMASEQ1READY</a>																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
N	R	DMASEQ1BUSERROR			Read pending status of interrupt for event <a href="#">DMASEQ1BUSERROR</a>																														
					When this event is generated, the address which caused the error can be read from the BUSERRORADDRESS register.																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														
O-R	R	COMPAREMATCH[i] (i=0..3)			Read pending status of interrupt for event <a href="#">COMPAREMATCH[i]</a>																														
			NotPending	0	Read: Not pending																														
			Pending	1	Read: Pending																														

### 8.15.5.28 ENABLE

Address offset: 0x500

PWM module enable register