**Table 8-41. INT_GLOBAL Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 4 | INT_3 | RH | 0b | Logical OR of INT_3 register |
| 3 | RSVD | RH | 0b | Reserved |
| 2 | INT_4 | RH | 0b | Logical OR of INT_4 register |
| 1 | RSVD | RH | 0b | Reserved |
| 0 | RSVD | RH | 0b | Reserved |

### 8.6.32 INT_1 Register (Address = 51h) [reset = 0h]

INT_1 is shown in Figure 8-86 and described in Table 8-42.

Return to Summary Table.

**Figure 8-86. INT_1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| WD | RSVD | LWU | WKERR | RSVD | | | |
| R/W1C-0b | R-0b | R/W1C-0b | R/W1C-0b | R-0b | | | |

**Table 8-42. INT_1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | WD | R/W1C | 0b | Watchdog event interrupt.<br>NOTE: This interrupt bit will be set for every watchdog error event and does not rely upon the Watchdog error counter |
| 6 | RSVD | R | 0b | Reserved |
| 5 | LWU | R/W1C | 0b | Local wake up |
| 4 | WKERR | R/W1C | 0b | Wake error bit is set when the SWE timer has expired and the state machine has returned to Sleep mode |
| 3-0 | RSVD | R | 0b | Reserved |

### 8.6.33 INT_2 Register (Address = 52h) [reset = 40h]

INT_2 is shown in Figure 8-87 and described in Table 8-43.

Return to Summary Table.

**Figure 8-87. INT_2 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SMS | PWRON | OVCC | UVSUP | RSVD | UVCC | TSD_VCC_LIN | TSD_HSS_LIMP |
| R/W1C-0b | R/W1C-1b | R/W1C-0b | R/W1C-0b | R-0b | R/W1C-0b | R/W1C-0b | R/W1C-0b |

**Table 8-43. INT_2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SMS | R/W1C | 0b | Sleep mode status flag. Only sets when sleep mode is entered by a fault |
| 6 | PWRON | R/W1C | 1b | Power on |
| 5 | OVCC | R/W1C | 0b | $V_{CC}$ overvoltage |
| 4 | UVSUP | R/W1C | 0b | $V_{SUP}$ undervoltage |
| 3 | RSVD | R | 0b | Reserved |
| 2 | UVCC | R/W1C | 0b | $V_{CC}$ undervoltage |
| 1 | TSD_VCC_LIN | R/W1C | 0b | Thermal Shutdown due to VCC or LIN |
| 0 | TSD_HSS_LIMP | R/W1C | 0b | Thermal Shutdown due to HSS or LIMP |