5.6.1 Registers

Instances

Instance	Domain	Base address	TrustZone			Split access	Description
			Map	Att	DMA		
POWER : S	GLOBAL	0x5010E000	US	S	NA	No	Power control
POWER : NS		0x4010E000					

Register overview

Register	Offset	TZ	Description
TASKS_CONSTLAT	0x30		Enable Constant Latency mode
TASKS_LOWPWR	0x34		Enable Low-power mode (variable latency)
SUBSCRIBE_CONSTLAT	0xB0		Subscribe configuration for task CONSTLAT
SUBSCRIBE_LOWPWR	0xB4		Subscribe configuration for task LOWPWR
EVENTS_POFWARN	0x130		Power failure warning
EVENTS_SLEEPENTER	0x134		CPU entered WFI/WFE sleep
EVENTS_SLEEPEXIT	0x138		CPU exited WFI/WFE sleep
PUBLISH_SLEEPENTER	0x1B4		Publish configuration for event SLEEPENTER
PUBLISH_SLEEPEXIT	0x1B8		Publish configuration for event SLEEPEXIT
INTEN	0x300		Enable or disable interrupt
INTENSET	0x304		Enable interrupt
INTENCLR	0x308		Disable interrupt
GPREGRET[n]	0x500		General purpose retention register This register is retained.
CONSTLATSTAT	0x520		Status of constant latency

5.6.1.1 TASKS_CONSTLAT

Address offset: 0x30

Enable Constant Latency mode

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID			A
Reset 0x00000000			0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

ID	R/W	Field	Value ID	Value	Description
A	W	TASKS_CONSTLAT			Enable Constant Latency mode
			Trigger	1	Trigger task

5.6.1.2 TASKS_LOWPWR

Address offset: 0x34

Enable Low-power mode (variable latency)

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SEMICONDUCTOR