8.8.1 Pin configuration

The GPIO port peripheral implements up to 32 pins, `PIN[n]` (n = 0..31), that can be individually configured in the PIN_CNF[n] registers (n=0..31).

The following parameters can be enabled or configured in these registers:

- Direction
- Drive strength
- Pull-up and pull-down resistors
- Pin sensing
- Input buffer disconnect
- Analog input (for selected pins)

All write-capable registers are retained registers. See POWER — Power control on page 92 for more information.

When not used as an input, disconnect the input buffer of the GPIO pin to save power. An input must be connected to get a valid value in the IN register and for the sense mechanism to have access to the pin.

Other peripherals in the system can connect to GPIO pins to override their output value, override their configuration, or read their analog or digital input value.

Selected pins also support analog input signals (ANAIN). The assignment of the analog pins can be found in Pin assignments on page 859.

GPIO drive strength is configured using the DRIVE0 and DRIVE1 fields of register PIN_CNF[n] (n=0..31) (Retained) on page 284. Some pins may not support every drive configuration, see Pin assignments on page 859 for more information.

When a pin is configured as digital input, it is important to minimize increased current consumption when the input voltage is between V_{IL} and V_{IH}. It is a good practice to ensure that the external circuitry does not drive the pin to levels between V_{IL} and V_{IH} for a long period of time.

For more information on pin assignment and the corresponding effect of read and write operations of GPIO registers, see Peripheral and subsystem assignment on page 277.

Note: NFCT uses two pins to connect to the antenna, which are shared with GPIOs. NFC pins are enabled from reset. To use them as GPIO pins, NFC use must be disabled using register PADCONFIG on page 398. For more details, see NFCT — Near field communication tag on page 359.

8.8.2 Pin sense mechanism

Pin sensitivity can be individually configured through the SENSE field in the PIN_CNF[n] register to detect a high level or a low level on their input. When the correct level is detected, the sense mechanism will set the DETECT signal `high`. Each pin has a separate DETECT signal.

The default behavior for the DETECT signal is defined by the register DETECTMODE. By default, the DETECT signals from all pins in the GPIO port are combined into one common DETECT signal that is routed throughout the system, and can be utilized by other peripherals. This mechanism is functional in both System ON and System OFF modes.The DETECTMODE applies to both secure and non-secure pins.

Pins must be in a level that cannot trigger the sense mechanism before enabling it. When the sense mechanism is enabled, the DETECT signal will immediately go high if the SENSE condition configured in the PIN_CNF registers is met. This will trigger a PORT event if the DETECT signal was low before enabling the sense mechanism.

The DETECT signal is used by the power and clock management system to exit from System OFF mode, and by the GPIOTE peripheral to allow pins to generate events and interrupts.