Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				P O N M L K J I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-H	RW	START[i] (i=0..7)			Selects which PE comparator inputs are in use with ViewInst start/stop control, for the purpose of starting trace
			Disabled	0	The single PE comparator input i, is not selected as a start resource.
			Enabled	1	The single PE comparator input i, is selected as a start resource.
I-P	RW	STOP[i] (i=0..7)			Selects which PE comparator inputs are in use with ViewInst start/stop control, for the purpose of stopping trace.
			Disabled	0	The single PE comparator input i, is not selected as a stop resource.
			Enabled	1	The single PE comparator input i, is selected as a stop resource.

9.8.1.18 TRCVDCTLR

Address offset: 0x0A0

Controls data trace filtering.

Might ignore writes when the trace unit is enabled or not idle.

This register must be programmed when data tracing is enabled, that is, when either TRCCONFIGR.DA == 1 or TRCCONFIGR.DV == 1.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				L K J I I H G F E D C B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A-H	RW	EVENT[i] (i=0..7)			Event unit enable bit.
			Disabled	0	The trace event is not selected for trace filtering.
			Enabled	1	The trace event is selected for trace filtering.
I	RW	SPREL			Controls whether a trace unit traces data for transfers that are relative to the Stack Pointer (SP).
			Enabled	0	The trace unit does not affect the tracing of SP-relative transfers.
			DataOnly	2	The trace unit does not trace the address portion of SP-relative transfers. If data value tracing is enabled then the trace unit generates a P1 data address element.
			Disabled	3	The trace unit does not trace the address or value portions of SP-relative transfers.
J	RW	PCREL			Controls whether a trace unit traces data for transfers that are relative to the Program Counter (PC).
			Enabled	0	The trace unit does not affect the tracing of PC-relative transfers.
			Disabled	1	The trace unit does not trace the address or value portions of PC-relative transfers.
K	RW	TBI			Controls which information a trace unit populates in bits[63:56] of the data address.
			SignExtend	0	The trace unit assigns bits[63:56] to have the same value as bit[55] of the data address, that is, it sign-extends the value.
			Copy	1	The trace unit assigns bits[63:56] to have the same value as bits[63:56] of the data address.
L	RW	TRCEXDATA			Controls the tracing of data transfers for exceptions and exception returns on Armv6-M, Armv7-M, and Armv8-M PEs.
			Disabled	0	Exception and exception return data transfers are not traced.
			Enabled	1	Exception and exception return data transfers are traced if the other aspects of ViewData indicate that the data transfers must be traced.