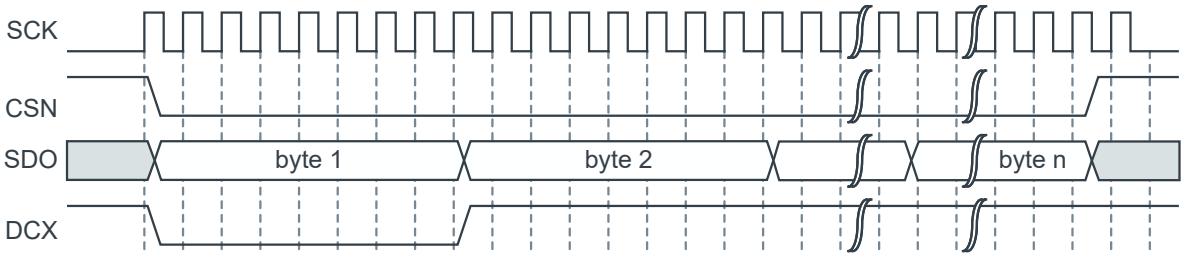

Figure 137: D/CX example

8.19.3 Chip select hardware control

To use CSN hardware control, set register PSEL.CSN on page 606 according to the Pin configuration on page 586.

When enabled, CSN is asserted automatically after TASKS_START on page 590 is triggered, and deasserted after EVENTS_END on page 594. The value in register IFTIMING.CSNDUR on page 604 sets the time between the falling edge of CSN and the first SCK edge. The same delay is used between the last SCK edge and the rising edge of CSN at the end of a transfer. It is also used between two transfers as the minimum CSN inactive time when the END_START short is enabled. The IFTIMING.CSNDUR is expressed in number of SPIM core clock periods.

The following figure shows a timing diagram with two SPI transmissions where the delay is controlled by IFTIMING.CSNDUR and is represented by t_{CSNDUR}.

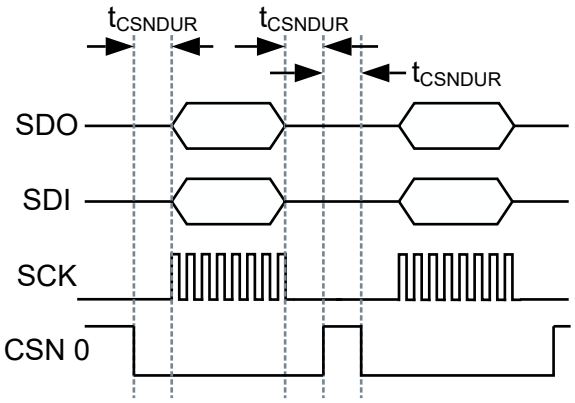

Figure 138: CSNDUR example

The following figure shows the timing delay for the combinations of polarity and phase settings. The register CSNPOL on page 604 determines the active polarity of the signal.