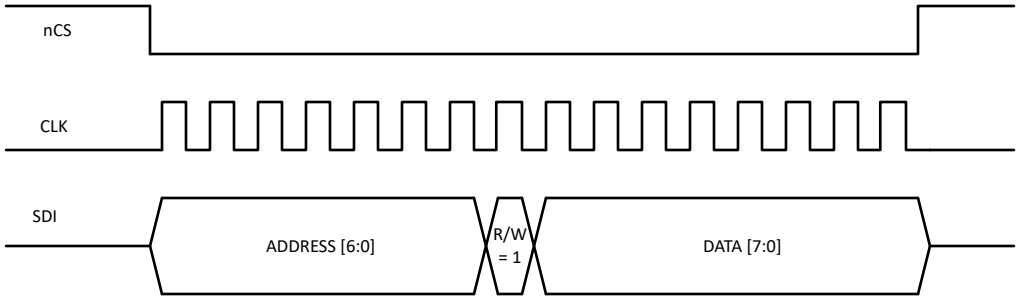

Figure 8-50. SPI Write

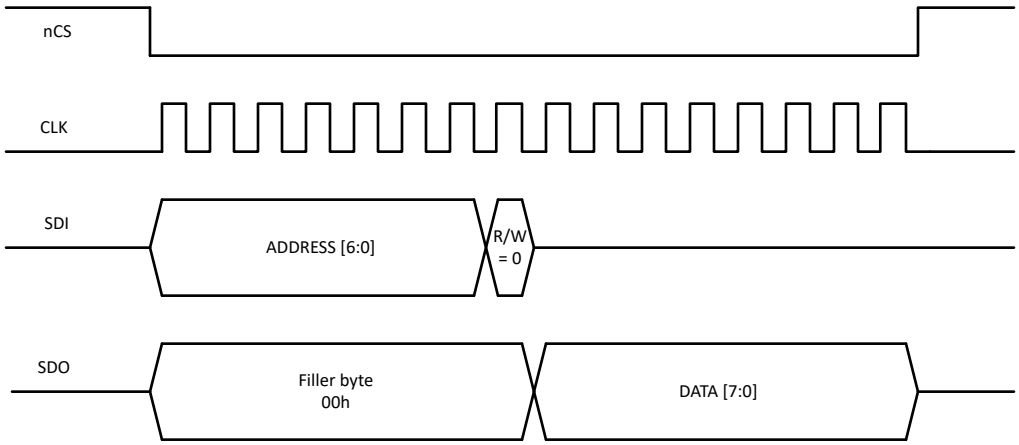

Figure 8-51. SPI Read

8.5.1.1 Cyclic Redundancy Check

The TLIN1431x supports cyclic redundancy check (CRC) for SPI transactions and is default disabled. Register 8'h0A[0] can be used to enable this feature. The default polynomial supports AutoSAR CRC8H2F, $X^8 + X^5 + X^3 + X^2 + X + 1$, see Table 8-7. CRC8 according to SAE J1850 is also supported and can be selected at register 8'h0B[0].

When CRC is enabled, a filler byte of 00h is used to calculate the CRC value during a read/write operation, see Figure 8-52 and Figure 8-53.

Table 8-7. CRC8H27

SPI Transactions	
CRC result width	8 bits
Polynomial	2Fh
Initial value	FFh
Input data reflected	No
Result data reflected	No
XOR value	FFh
Check	DFh
Magic Check	42h

Table 8-8. CRC8 SAE J1850

SPI Transactions	
CRC result width	8 bits