can receive, the extra bytes are discarded and NACKed by the target. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers, RXD.PTR, TXD.PTR, RXD.AMOUNT, and TXD.AMOUNT, are latched when the EVENTS_DMA.RX.READY event is generated.

TWIS can be forced to stop by triggering the STOP task. A STOPPED event will be generated when TWIS has stopped. TWIS will clear the internal **`RX prepared`** flag and return to the IDLE state when it has stopped, see Terminate an ongoing TWI transaction on page 690.

TWIS will generate an ACK after every byte received from the controller. The RXD.AMOUNT register can be queried after a transaction to see how many bytes were received.

A typical TWIS write command response is illustrated in the following figure, including clock stretching following a SUSPEND task.

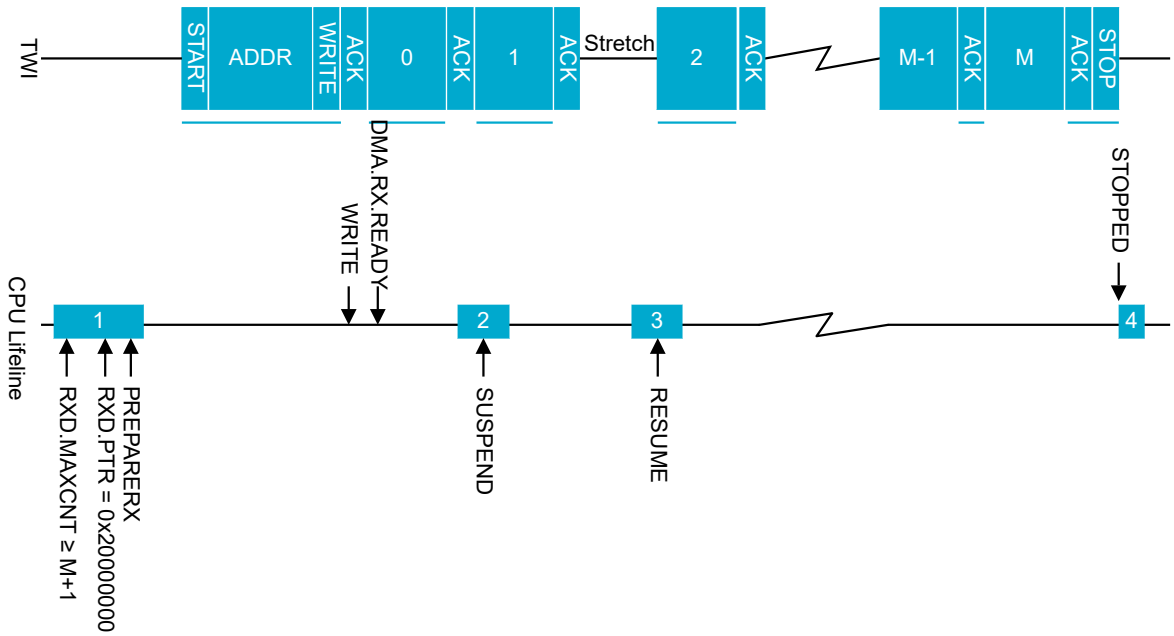

Figure 155: TWIS responding to a write command

8.24.6 TWI controller repeated start sequence

A repeated start sequence is where the TWI controller writes two bytes to TWIS, followed by reading four bytes from the target. This is shown in the following figure.