Register	Offset	TZ	Description
FEATURE.GPIO[n].PIN[o]	0x800		Security configuration for GPIO[n] PIN[o]
FEATURE.CRACEN.SEED	0x980		Configuration for CRACEN SEED
FEATURE.GRTC.CC[n]	0xD00		Security configuration for CC n of GRTC
FEATURE.GRTC.PWMCONFIG	0xD74		Security Configuration for PWMCONFIG of GRTC
FEATURE.GRTC.CLK	0xD78		Security configuration for CLKOUT/CLKCFG of GRTC
FEATURE.GRTC.SYSCOUNTER	0xD7C		Security configuration for SYSCOUNTERL/SYSCOUNTERH of GRTC
FEATURE.GRTC.INTERRUPT[n]	0xD80		Security configuration for interrupt n of GRTC

7.8.5.5.1 EVENTS_PERIPHACCERR

Address offset: 0x100

A security violation has been detected on one or several peripherals

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	EVENTS_PERIPHACCERR			A security violation has been detected on one or several peripherals
			NotGenerated	0	Event not generated
			Generated	1	Event generated

7.8.5.5.2 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	PERIPHACCERR			Enable or disable interrupt for event PERIPHACCERR
			Disabled	0	Disable
			Enabled	1	Enable

7.8.5.5.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	PERIPHACCERR			Write '1' to enable interrupt for event PERIPHACCERR
	W1S				
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

7.8.5.5.4 INTENCLR

Address offset: 0x308