11.19.4 Timing specifications for GPIO port P0 using High drive strength

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SPIS,VSO}$	CLK edge to SDO valid			56	ns
$t_{SPIS,HSO}$	SDO hold time after CLK edge	6			ns
$t_{SPIS,SUSI}$	SDI to CLK edge setup time	33			ns
$t_{SPIS,HSI}$	CLK edge to SDI hold time	1			ns

11.19.5 Timing specifications for GPIO port P1 using Standard drive strength

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SPIS,VSO}$	CLK edge to SDO valid			43	ns
$t_{SPIS,HSO}$	SDO hold time after CLK edge	5			ns
$t_{SPIS,SUSI}$	SDI to CLK edge setup time	5			ns
$t_{SPIS,HSI}$	CLK edge to SDI hold time	2			ns

11.19.6 Timing specifications for GPIO port P1 using High drive strength

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SPIS,VSO}$	CLK edge to SDO valid			39	ns
$t_{SPIS,HSO}$	SDO hold time after CLK edge	5			ns
$t_{SPIS,SUSI}$	SDI to CLK edge setup time	5			ns
$t_{SPIS,HSI}$	CLK edge to SDI hold time	2			ns

11.19.7 Timing specifications for GPIO port P2 using Standard drive strength

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SPIS,VSO}$	CLK edge to SDO valid			43	ns
$t_{SPIS,HSO}$	SDO hold time after CLK edge	5			ns
$t_{SPIS,SUSI}$	SDI to CLK edge setup time	6			ns
$t_{SPIS,HSI}$	CLK edge to SDI hold time	0			ns

11.19.8 Timing specifications for GPIO port P2 using High drive strength

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SPIS,VSO}$	CLK edge to SDO valid			39	ns
$t_{SPIS,HSO}$	SDO hold time after CLK edge	5			ns
$t_{SPIS,SUSI}$	SDI to CLK edge setup time	6			ns
$t_{SPIS,HSI}$	CLK edge to SDI hold time	1			ns