Address bits	Description	Enumeration
[28:0]	Address space	
[31:29]	Address regions	0: Program memory 1: Data memory 2: Peripherals/APB space 7: CPU internal peripherals, like Arm Cortex private peripheral bus (PPB)

Table 8: Address regions format

The program and data memory address format is described in the following table.

Address bits	Description	Enumeration
[23:0]	Address space	
[28:24]	Reserved	Set to zero
[31:29]	Address regions	0: Program memory 1: Data memory

Table 9: Program memory and data memory address format

The peripheral address format is described in the following table.

Address bits	Description	Enumeration
[11:0]	Peripheral address space	
[17:12]	Peripheral subordinate index	Used for configuring the SPU — System protection unit on page 180, as the index *n* of register SPU.PERIPH[*n*].PERM.
[20:12]	Interrupt vector number	The index in the interrupt vector table
[23:18]	Peripheral APB bus number	1: APB peripherals in MCU power domain 2: APB peripherals in RADIO power domain 3: APB peripherals in PERI power domain 4: APB peripherals in LP power domain
[27:24]	Reserved	Set to zero
[28]	Security	0: Non-secure 1: Secure
[31:29]	Address regions	2: Peripherals on APB bus

Table 10: Peripheral address format

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