Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A	RW1	PALL																																	
			Unprotected	0xFFFFFFFF																															
				Leaves TAMPC PROTECT.DOMAIN SPIDEN and SPNIDEN signal protectors unlocked and under CPU control.																																

4.2.9.1.3 AUXAPPROTECT[n] (n=0..0)

Access Port Protection Registers

4.2.9.1.3.1 AUXAPPROTECT[n].PROTECT0 (n=0..0)

Address offset: 0x040 + (n × 0x20)

Access port protection

Any other value than Unprotected will lock TAMPC PROTECT.AP signal protectors.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A	RW1	PALL																																	
			Unprotected	0xFFFFFFFF																															
				Leaves TAMPC PROTECT.AP DBGEN signal protector unlocked and under CPU control.																																

4.2.9.1.3.2 AUXAPPROTECT[n].PROTECT1 (n=0..0)

Address offset: 0x05C + (n × 0x20)

Access port protection register

Any other value than Unprotected will lock TAMPC PROTECT.AP signal protectors.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A	RW1	PALL																																	
			Unprotected	0xFFFFFFFF																															
				Leaves TAMPC PROTECT.AP DBGEN signal protector unlocked and under CPU control.																																

4.2.9.1.4 ERASEPROTECT[n] (n=0..0)

Erase Protection Registers

4.2.9.1.4.1 ERASEPROTECT[n].PROTECT0 (n=0..0)

Address offset: 0x60 + (n × 0x20)

Erase protection

Any other value than `Protected` will leave the TAMPC PROTECT.ERASEPROTECT signal protector unlocked, so that CPU can control its value.