Configuration

Instance	Domain	Configuration
GRTC : S GRTC : NS	GLOBAL	Local CPUs connected to MODE.AUTO.EN.CpuActive : Application core Arm Cortex-M33. CLKSEL settings XO and LFLPRC must be used for lowest possible power consumption in sleep modes. Width of the RTCOUNTERH, RTCOMPAREH and RTCOMPARESYNCH registers : 0..14 Number of compare/capture registers : 0..11 Width of the TIMEOUT register : 0..15 Number of GRTC interrupts : 0..3 The PWM registers are available. The CLKOUT register is available. The CLKCFG.CLKSEL register is available. The CLKCFG.CLKSEL register supports LFLPRC. The CC[n].CCADD register has write access only. The ready status and events are available. SYSCOUNTER[n].SYSCOUNTERH.LOADED status is not available CC[n].CCEN.PASTCC status is not available 4 interrupts with interrupt remapping 12 capture compare channels implemented

Register overview

Register	Offset	TZ	Description
TASKS_CAPTURE[n]	0x000		Capture the counter value to CC[n] register
TASKS_START	0x060		Start the counter
TASKS_STOP	0x064		Stop the counter
TASKS_CLEAR	0x068		Clear the counter
TASKS_PWMSTART	0x06C		Start the PWM
TASKS_PWMSTOP	0x070		Stop the PWM
SUBSCRIBE_CAPTURE[n]	0x080		Subscribe configuration for task CAPTURE[n]
EVENTS_COMPARE[n]	0x100		Compare event on CC[n] match
EVENTS_RTCOMPARESYNC	0x164		The GRTC low frequency timer is synchronized with the SYSCOUNTER
EVENTS_PWMPERIODEND	0x16C		Event on end of each PWM period
EVENTS_PWMREADY	0x174		Event on STATUS.PWM.READY status changed to ready
EVENTS_CLKOUTREADY	0x178		Event on STATUS.CLKOUT.READY status changed to ready
PUBLISH_COMPARE[n]	0x180		Publish configuration for event COMPARE[n]
PUBLISH_PWMREADY	0x1F4		Publish configuration for event PWMREADY
PUBLISH_CLKOUTREADY	0x1F8		Publish configuration for event CLKOUTREADY
SHORTS	0x200		Shortcuts between local events and tasks
INTEN0	0x300		Enable or disable interrupt
INTENSET0	0x304		Enable interrupt
INTENCLR0	0x308		Disable interrupt
INTPEND0	0x30C		Pending interrupts
INTEN1	0x310		Enable or disable interrupt
INTENSET1	0x314		Enable interrupt