TRAFFIC LIGHT CONTROLLER

# DESIGN ASSIGNMENT #3

PROBLEM

Design a digital controller to control traffic at an intersection of a busy main street (North-South) and an occasionally used side street (East-West).

-North South must be Green for a <u>minimum</u> of 25 seconds and will remain Green until traffic is present on East-West

-East West will remain Green for a <u>maximum</u> of 25 seconds

-Yellow lights on both streets must be for 4 seconds
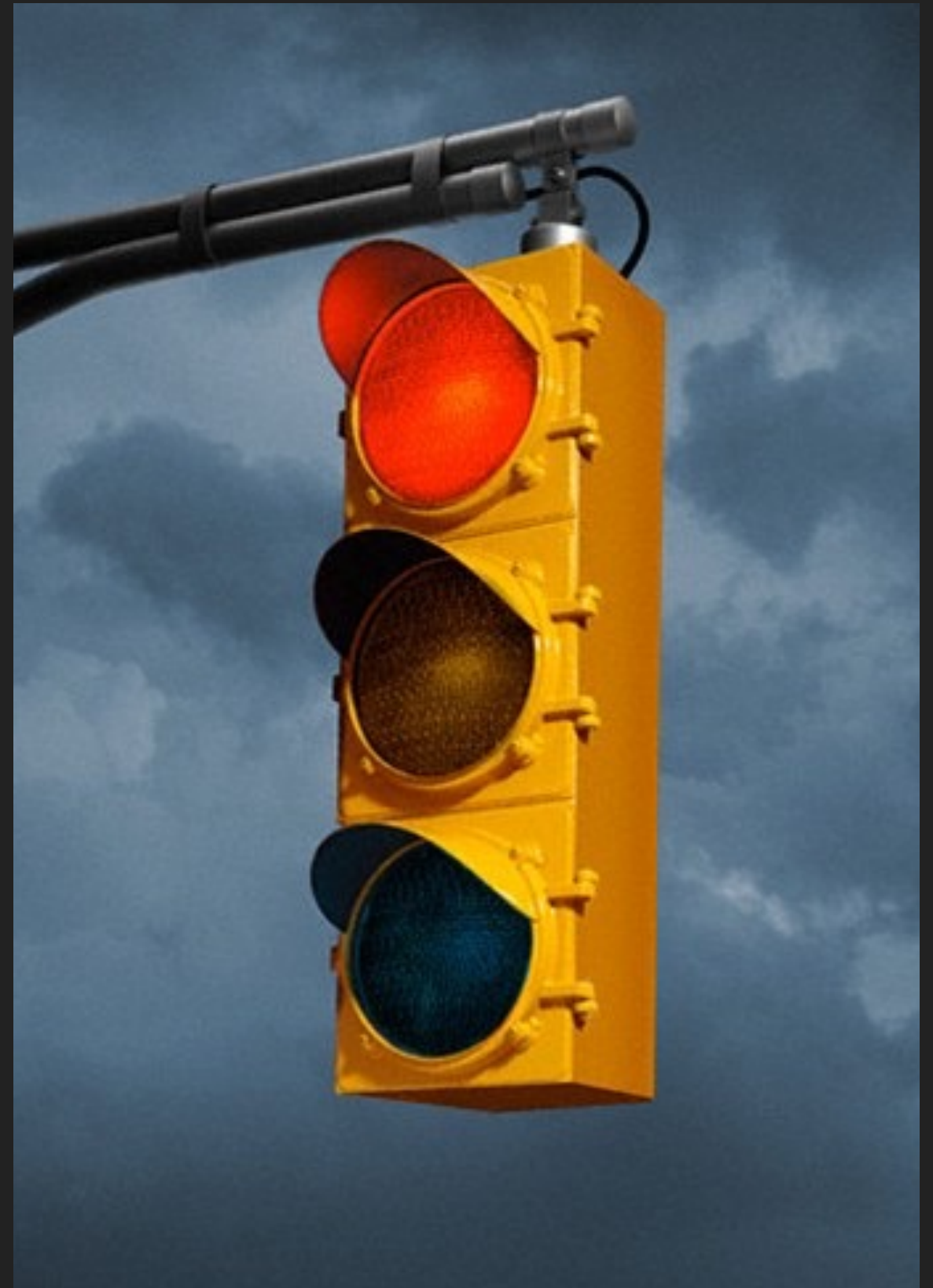
SPECIFICATIONS

TIME

SIGNALS

TIME SPECIFICATIONS

North-South	East-West	Both Streets
32 SECONDS	16 SECONDS	4 SECONDS

32 SECONDS

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```verilog
module nsCounter
(
    input clk,
    output [4:0] count
);

wire clk;
reg[4:0] count;

initial
    count = 0;

always @( negedge clk )
    count[0] <= ~count[0];

always @( negedge count[0] )
    count[1] <= ~count[1];

always @( negedge count[1] )
    count[2] <= ~count[2];

always @( negedge count[2] )
    count[3] <= ~count[3];

always @( negedge count[3] )
    count[4] <= ~count[4];

endmodule
```

16 SECONDS

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```verilog
module ewCounter
(
    input clk,
    output [3:0] count
);

wire clk;
reg[3:0] count;

initial
    count = 0;

always @( negedge clk )
    count[0] <= ~count[0];

always @( negedge count[0] )
    count[1] <= ~count[1];

always @( negedge count[1] )
    count[2] <= ~count[2];

always @( negedge count[2] )
    count[3] <= ~count[3];

endmodule
```

4 SECONDS

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```verilog
module yellowCounter
(
    input clk,
    output [1:0] count
);

wire clk;
reg[1:0] count;

initial
    count = 0;

always @( negedge clk )
    count[0] <= ~count[0];

always @( negedge count[0] )
    count[1] <= ~count[1];

endmodule
```

TIME SPECIFICATIONS

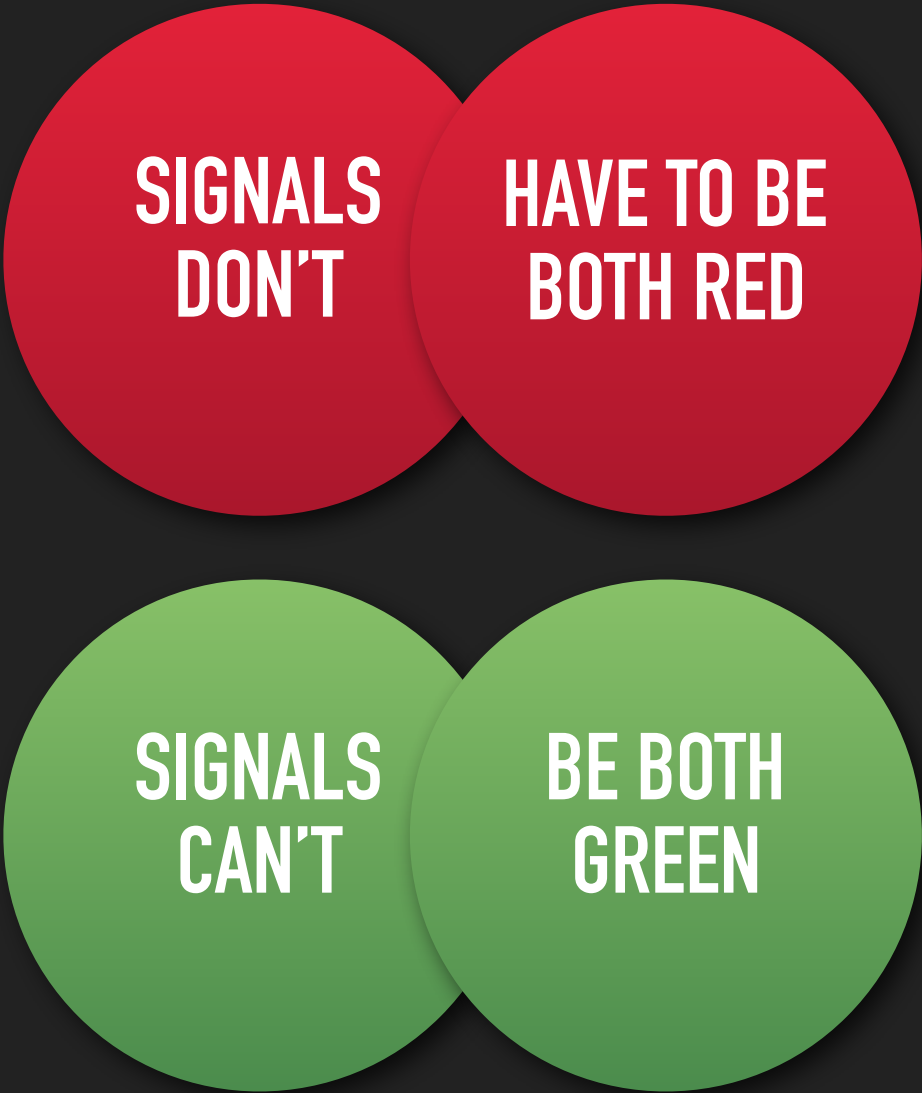| North-South	East-West	Both Streets
32 SECONDS	16 SECONDS	4 SECONDS

SIGNAL SPECIFICATIONS

East-West

Both Streets

NO GREEN LIGHT UNTIL VEHICLE PRESENT

SIGNALS DON'T — HAVE TO BE BOTH RED

SIGNALS CAN'T — BE BOTH GREEN

STATE DIAGRAM

EW_Vehicle_Detect = 0

EW_Vehicle_Detect = 1
AND
32 seconds

001100
S1

010100
S2

START

4 seconds

4 seconds

100010
S4

100001
S3

16 seconds
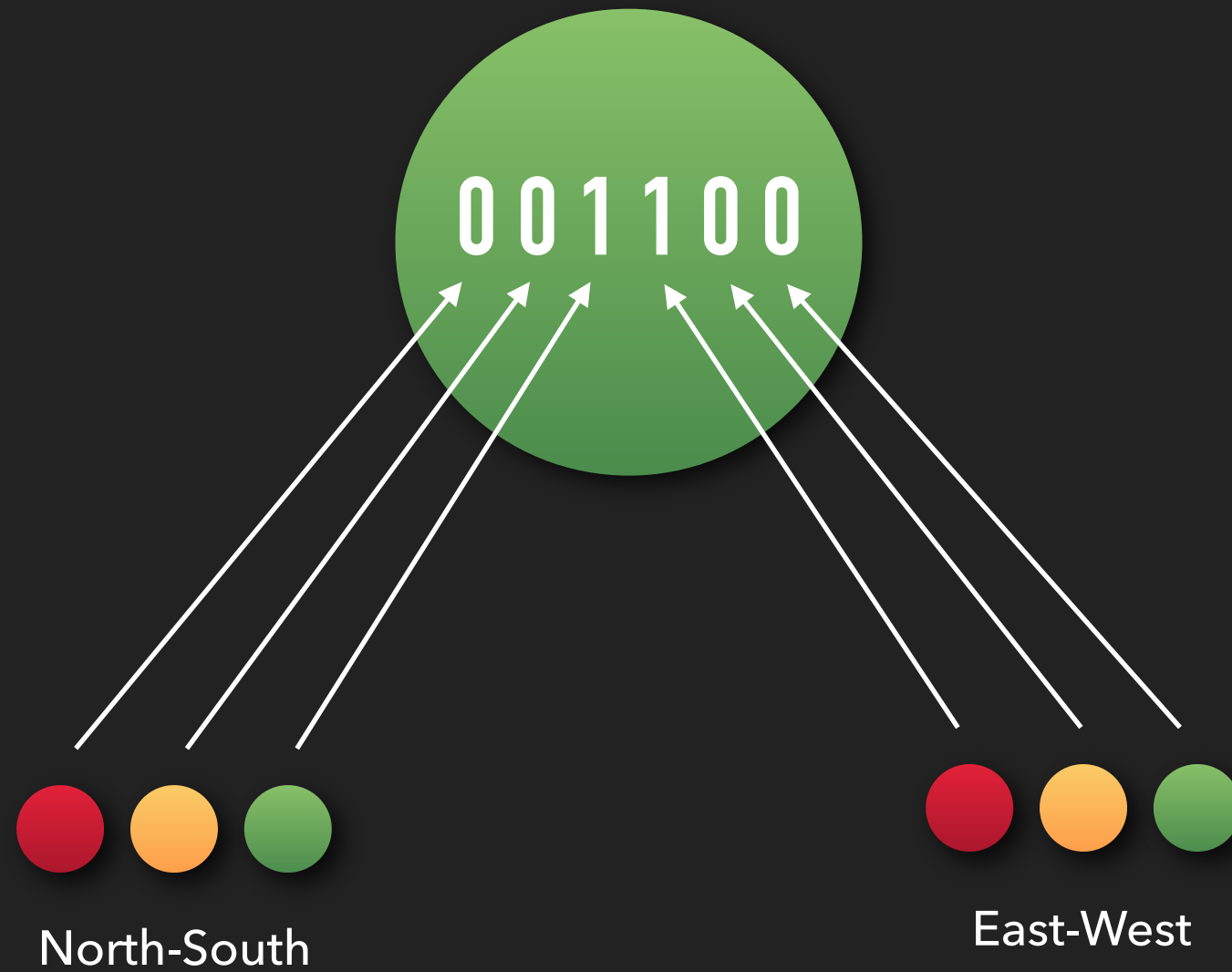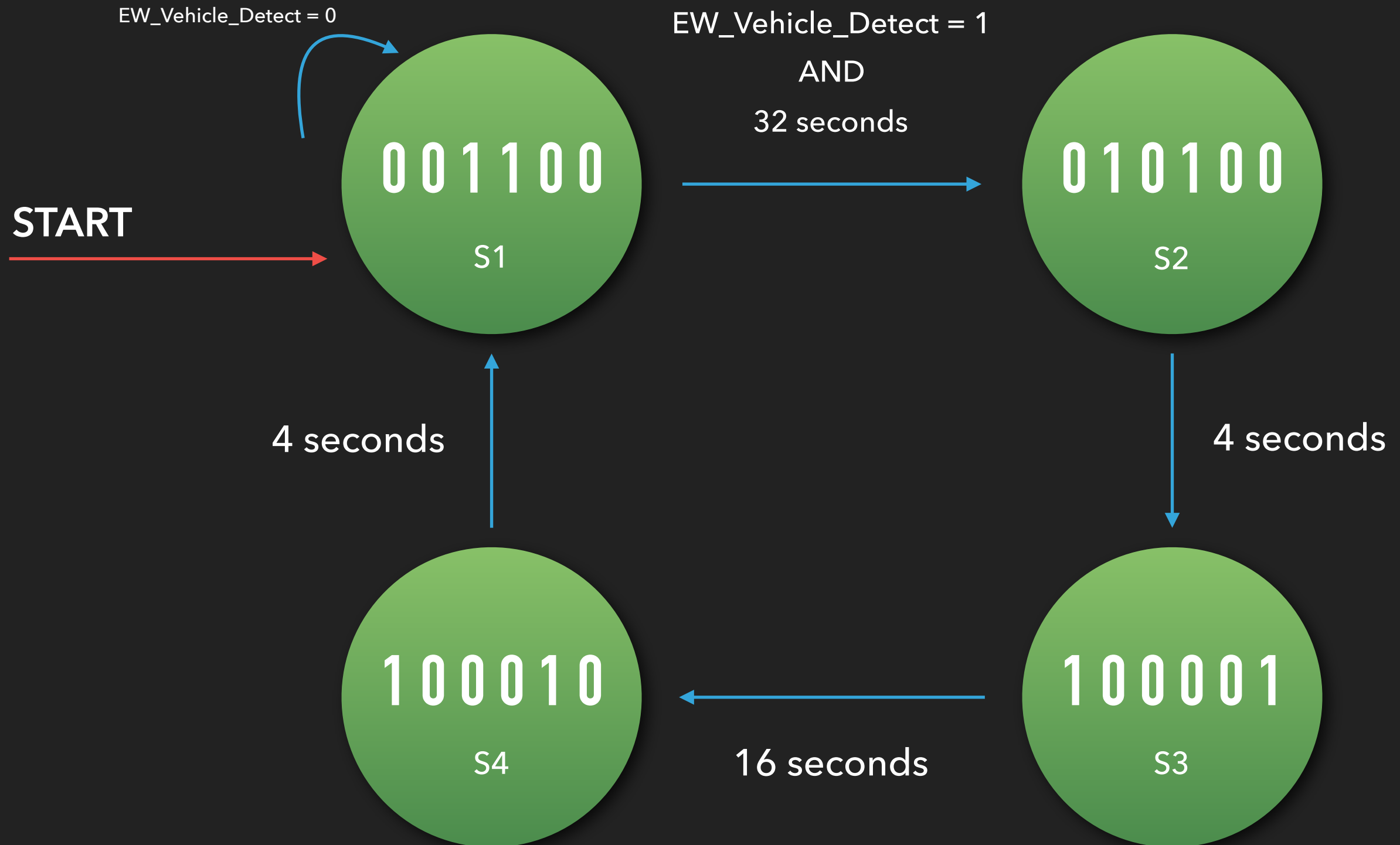
INPUTS AND OUTPUTS

Inputs (8)

NS Red

NS Yellow

NS Green

EW Red

EW Yellow

EW Green

Traffic on EW

Timer

Outputs (6)

NS Red

NS Yellow

NS Green

EW Red

EW Yellow

EW Green

TRUTH TABLE

Present State						Inputs		Future State					
	NS			EW					NS			EW	
R	Y	G	R	Y	G	EW	TIME	R	Y	G	R	Y	G
0	0	1	1	0	0	0	x	0	0	1	1	0	0
0	0	1	1	0	0	1	0	0	0	1	1	0	0
0	0	1	1	0	0	1	1	0	1	0	1	0	0
0	1	0	1	0	0	x	0	0	1	0	1	0	0
0	1	0	1	0	0	x	1	1	0	0	0	0	1
1	0	0	0	0	1	x	0	1	0	0	0	0	1
1	0	0	0	0	1	x	1	1	0	0	0	1	0
1	0	0	0	1	0	x	0	1	0	1	0	1	0
1	0	0	0	1	0	x	1	0	0	1	1	0	0

K MAP OUTPUT (NORTH–SOUTH RED)

A = NS Red   D = EW Red   G = Traffic on EW
B = NS Yellow   E = EW Yellow   H = Timer
C = NS Green   F = EW Green

	$\bar E.\bar F.\bar G.\bar H$	$\bar E.\bar F.\bar G.H$	$\bar E.\bar F.G.\bar H$	$\bar E.\bar F.G.H$	$\bar E.F.\bar G.\bar H$	$\bar E.F.\bar G.H$	$\bar E.F.G.\bar H$	$\bar E.F.G.H$	$E.\bar F.\bar G.\bar H$	$E.\bar F.\bar G.H$	$E.\bar F.G.\bar H$	$E.\bar F.G.H$	$E.F.\bar G.\bar H$	$E.F.\bar G.H$	$E.F.G.\bar H$	$E.F.G.H$
$\bar A.\bar B.\bar C.\bar D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\bar A.\bar B.\bar C.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\bar A.\bar B.C.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\bar A.\bar B.C.\bar D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\bar A.B.\bar C.\bar D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\bar A.B.\bar C.D$	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
$\bar A.B.C.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\bar A.B.C.\bar D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.B.\bar C.\bar D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.B.\bar C.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.B.C.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.B.C.\bar D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.\bar B.\bar C.\bar D$	0	0	0	0	1	1	1	1	0	0	0	0	1	0	0	1
$A.\bar B.\bar C.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.\bar B.C.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.\bar B.C.\bar D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

A'BC'DE'F'H + AB'C'DE'F + AB'C'D'EF'H' = 0101001 + 100101 + 1000100

K MAP OUTPUT (NORTH–SOUTH YELLOW)

A = NS Red D = EW Red G = Traffic on EW
B = NS Yellow E = EW Yellow H = Timer
C = NS Green F = EW Green

	$\overline{E}.\overline{F}.\overline{G}.\overline{H}$	$\overline{E}.\overline{F}.\overline{G}.H$	$\overline{E}.\overline{F}.G.\overline{H}$	$\overline{E}.\overline{F}.G.H$	$\overline{E}.F.\overline{G}.\overline{H}$	$\overline{E}.F.\overline{G}.H$	$\overline{E}.F.G.\overline{H}$	$\overline{E}.F.G.H$	$E.\overline{F}.\overline{G}.\overline{H}$	$E.\overline{F}.\overline{G}.H$	$E.\overline{F}.G.\overline{H}$	$E.\overline{F}.G.H$	$E.F.\overline{G}.\overline{H}$	$E.F.\overline{G}.H$	$E.F.G.\overline{H}$	$E.F.G.H$
$\overline{A}.\overline{B}.\overline{C}.\overline{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{A}.\overline{B}.\overline{C}.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{A}.\overline{B}.C.D$	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{A}.\overline{B}.C.\overline{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{A}.B.\overline{C}.\overline{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{A}.B.\overline{C}.D$	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{A}.B.C.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{A}.B.C.\overline{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.B.\overline{C}.\overline{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.B.\overline{C}.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.B.C.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.B.C.\overline{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.\overline{B}.\overline{C}.\overline{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.\overline{B}.\overline{C}.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.\overline{B}.C.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.\overline{B}.C.\overline{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

A'B'CDE'F'GH + A'BC'DE'F'H' = 00110100 + 0101000

K MAP OUTPUT (NORTH–SOUTH GREEN)

A = NS Red	D = EW Red	G = Traffic on EW
B = NS Yellow	E = EW Yellow	H = Timer
C = NS Green	F = EW Green	

	E'.F'.G'.H'	E'.F'.G'.H	E'.F'.G.H	E'.F'.G.H'	E'.F.G'.H'	E'.F.G'.H	E'.F.G.H	E'.F.G.H'	E.F.G'.H'	E.F.G'.H	E.F.G.H	E.F.G.H'	E.F'.G'.H'	E.F'.G'.H	E.F'.G.H	E.F'.G.H'
A'.B'.C'.D'	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A'.B'.C'.D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A'.B'.C.D	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
A'.B'.C.D'	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A'.B.C'.D'	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A'.B.C'.D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A'.B.C.D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A'.B.C.D'	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A.B.C'.D'	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A.B.C'.D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A.B.C.D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A.B.C.D'	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A.B'.C'.D'	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
A.B'.C'.D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A.B'.C.D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A.B'.C.D'	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

A'B'CDE'F'G' + AB'C'D'EF'H + A'B'CDE'F'GH' = 0011000 + 1000101 + 00110010

TRAFFIC LIGHT CONTROLLER

K MAP OUTPUT (EAST–WEST RED)

A = NS Red   D = EW Red   G = Traffic on EW
B = NS Yellow   E = EW Yellow   H = Timer
C = NS Green   F = EW Green

	$\bar{E}.\bar{F}.\bar{G}.\bar{H}$	$\bar{E}.\bar{F}.\bar{G}.H$	$\bar{E}.\bar{F}.G.H$	$\bar{E}.\bar{F}.G.\bar{H}$	$\bar{E}.F.\bar{G}.\bar{H}$	$\bar{E}.F.\bar{G}.H$	$\bar{E}.F.G.H$	$\bar{E}.F.G.\bar{H}$	$E.F.\bar{G}.\bar{H}$	$E.F.\bar{G}.H$	$E.F.G.H$	$E.F.G.\bar{H}$	$E.\bar{F}.\bar{G}.\bar{H}$	$E.\bar{F}.\bar{G}.H$	$E.\bar{F}.G.H$	$E.\bar{F}.G.\bar{H}$
$\bar{A}.\bar{B}.\bar{C}.\bar{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\bar{A}.\bar{B}.\bar{C}.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\bar{A}.\bar{B}.C.D$	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
$\bar{A}.\bar{B}.C.\bar{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\bar{A}.B.\bar{C}.\bar{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\bar{A}.B.\bar{C}.D$	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
$\bar{A}.B.C.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\bar{A}.B.C.\bar{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.B.\bar{C}.\bar{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.B.\bar{C}.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.B.C.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.B.C.\bar{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.\bar{B}.\bar{C}.\bar{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
$A.\bar{B}.\bar{C}.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.\bar{B}.C.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.\bar{B}.C.\bar{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

A'B'CDE'F' + A'BC'DE'F'H' + AB'C'D'E'F'H = 001100 + 0101000 + 1000001

K MAP OUTPUT (EAST–WEST YELLOW)

A = NS Red   D = EW Red   G = Traffic on EW
B = NS Yellow   E = EW Yellow   H = Timer
C = NS Green   F = EW Green

	$\overline{E}.\overline{F}.\overline{G}.\overline{H}$	$\overline{E}.\overline{F}.\overline{G}.H$	$\overline{E}.\overline{F}.G.H$	$\overline{E}.\overline{F}.G.\overline{H}$	$\overline{E}.F.\overline{G}.\overline{H}$	$\overline{E}.F.\overline{G}.H$	$\overline{E}.F.G.H$	$\overline{E}.F.G.\overline{H}$	$E.F.\overline{G}.\overline{H}$	$E.F.\overline{G}.H$	$E.F.G.H$	$E.F.G.\overline{H}$	$E.\overline{F}.\overline{G}.\overline{H}$	$E.\overline{F}.\overline{G}.H$	$E.\overline{F}.G.H$	$E.\overline{F}.G.\overline{H}$
$\overline{A}.\overline{B}.\overline{C}.\overline{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{A}.\overline{B}.\overline{C}.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{A}.\overline{B}.C.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{A}.\overline{B}.C.\overline{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{A}.B.\overline{C}.\overline{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{A}.B.\overline{C}.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{A}.B.C.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{A}.B.C.\overline{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.B.\overline{C}.\overline{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.B.\overline{C}.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.B.C.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.B.C.\overline{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.\overline{B}.\overline{C}.\overline{D}$	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1
$A.\overline{B}.\overline{C}.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.\overline{B}.C.D$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A.\overline{B}.C.\overline{D}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AB'C'D'E'FH + AB'C'D'EF'H' = 1000011 + 1000100

K MAP OUTPUT (EAST–WEST GREEN)

A = NS Red   D = EW Red   G = Traffic on EW
B = NS Yellow   E = EW Yellow   H = Timer
C = NS Green   F = EW Green

	E̅.F̅.G̅.H̅	E̅.F̅.G̅.H	E̅.F̅.G.H	E̅.F̅.G.H̅	E̅.F.G̅.H̅	E̅.F.G̅.H	E̅.F.G.H	E̅.F.G.H̅	E.F̅.G̅.H̅	E.F̅.G̅.H	E.F̅.G.H	E.F̅.G.H̅	E.F.G̅.H̅	E.F.G̅.H	E.F.G.H	E.F.G.H̅
A̅.B̅.C̅.D̅	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A̅.B̅.C̅.D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A̅.B̅.C.D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A̅.B̅.C.D̅	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A̅.B.C̅.D̅	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A̅.B.C̅.D	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
A̅.B.C.D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A̅.B.C.D̅	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A.B.C̅.D̅	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A.B.C̅.D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A.B.C.D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A.B.C.D̅	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A.B̅.C̅.D̅	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0
A.B̅.C̅.D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A.B̅.C.D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A.B̅.C.D̅	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

A'BC'DE'F'H + AB'C'D'E'FH' = 0101000 + 1000010

STATE DIAGRAM

EW_Vehicle_Detect = 0

EW_Vehicle_Detect = 1
AND
32 seconds

001100
S1

010100
S2

START

4 seconds

4 seconds

100010
S4

100001
S3

16 seconds

MODULE

```
`timescale 1ns / 1ps

/*
    Group Members: Kevin Ingram and Warren Seto

    Lab Name: Traffic Light Controller (Lab 3)
    Project Name: eng312_proj3
    Design Name: Traffic_eng312_proj3.v
    Design Description: Verilog Module to Implement
*/

module Traffic
(
    input [4:0] nsCounter,
    input [3:0] ewCounter,
    input [1:0] yellowCounter,
    input NS_VEHICLE_DETECT,
    input EW_VEHICLE_DETECT,
    output reg NS_RED,
    output reg NS_YELLOW,
    output reg NS_GREEN,
    output reg EW_RED,
    output reg EW_YELLOW,
    output reg EW_GREEN
);

          begin
       _RED <= 0;
       NS_YELLOW <= 0;
       NS_GREEN <= 1;
       EW_RED <= 1;
       EW_YELLOW <= 0;
       EW_GREEN <= 0;
    end
```

001100

S1

MODULE
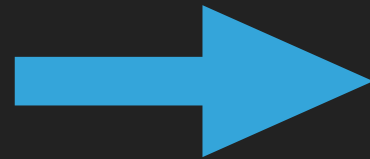

```
always @ (nsCounter) begin
    if (nsCounter == 31 & EW_VEHICLE_DETECT &
NS_GREEN) begin
        NS_RED <= 0;
        NS_YELLOW <= 1;
        NS_GREEN <= 0;
        EW_RED <= 1;
        EW_YELLOW <= 0;
        EW_GREEN <= 0;
    end
end
```
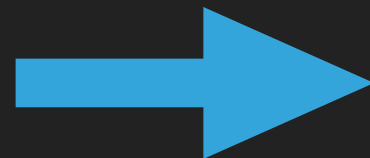
```
always @ (ewCounter) begin
    if (ewCounter == 15 & EW_GREEN) begin
        NS_RED <= 1;
        NS_YELLOW <= 0;
        NS_GREEN <= 0;
        EW_RED <= 0;
        EW_YELLOW <= 1;
        EW_GREEN <= 0;
    end
end
```

010100
S2

100010
S4

MODULE

001100

S1

100001

S3

```
always @ (yellowCounter) begin
    if (yellowCounter == 3 & NS_YELLOW) begin
        NS_RED <= 1;
        NS_YELLOW <= 0;
        NS_GREEN <= 0;
        EW_RED <= 0;
        EW_YELLOW <= 0;
        EW_GREEN <= 1;
    end

    if (yellowCounter == 3 & EW_YELLOW) begin
        NS_RED <= 0;
        NS_YELLOW <= 0;
        NS_GREEN <= 1;
        EW_RED <= 1;
        EW_YELLOW <= 0;
        EW_GREEN <= 0;
    end
end
endmodule
```
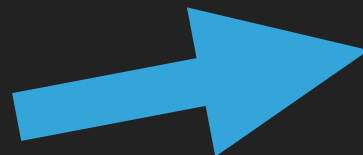
TESTS

```verilog
`timescale 1ns / 1ps

/*
    Group Members: Kevin Ingram and Warren Seto

    Lab Name: Traffic Light Controller (Lab 3)
    Project Name: eng312_proj3
    Design Name: Traffic_Test_A_eng312_proj3.v
    Design Description: Verilog Test Bench to Implement Test A (3 AM)
*/


module Traffic_Test;

    // Inputs
    reg NS_VEHICLE_DETECT;
    reg EW_VEHICLE_DETECT;

    // Outputs
    wire NS_RED;
    wire NS_YELLOW;
    wire NS_GREEN;
    wire EW_RED;
    wire EW_YELLOW;
    wire EW_GREEN;

    // Clock
    reg clk;

    // Counters
    wire[4:0] count1;
    wire[3:0] count2;
    wire[1:0] count3;

    // Counter Modules
    nsCounter clock1(clk, count1);      // Count a total of 32 seconds
    ewCounter clock2(clk, count2);      // Counts a total of 16 seconds
    yellowCounter clock3(clk, count3); // Counts a total of 4 seconds

    // Main Traffic Module
    Traffic CORE (count1, count2, count3, NS_VEHICLE_DETECT, EW_VEHICLE_DETECT, NS_RED, NS_YELLOW,
NS_GREEN, EW_RED, EW_YELLOW, EW_GREEN);
```

TEST A (3 AM)
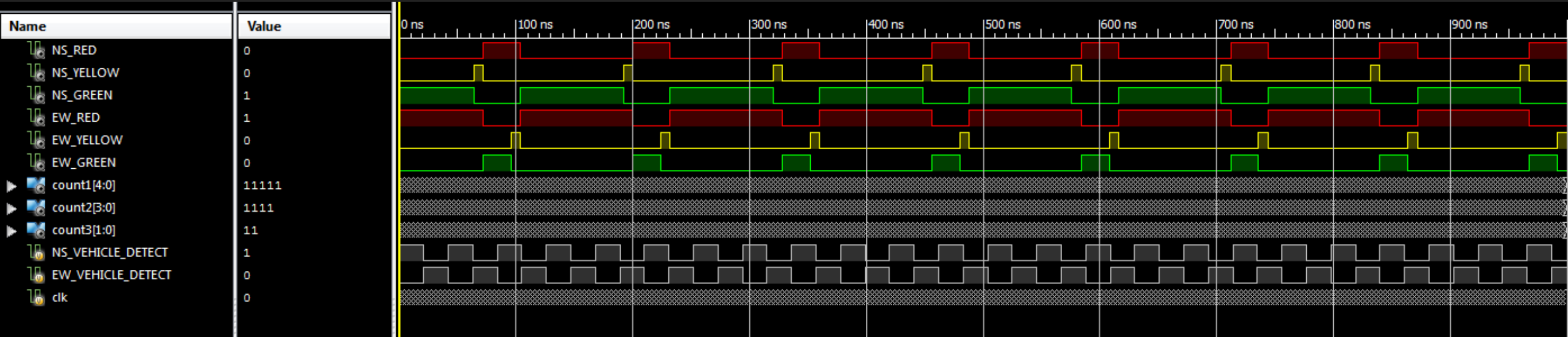
```
initial begin
     clk = 0;
     NS_VEHICLE_DETECT = 0;
     EW_VEHICLE_DETECT = 0;

   $display("              NS | EW ");
     $display("             R Y G R Y G ");


#1000 $finish;
end

always begin
#1 clk = ~clk;
end
```

Name	Value
NS_RED	0
NS_YELLOW	0
NS_GREEN	1
EW_RED	1
EW_YELLOW	0
EW_GREEN	0
count1[4:0]	11111
count2[3:0]	1111
count3[1:0]	11
NS_VEHICLE_DETECT	0
EW_VEHICLE_DETECT	0
clk	0
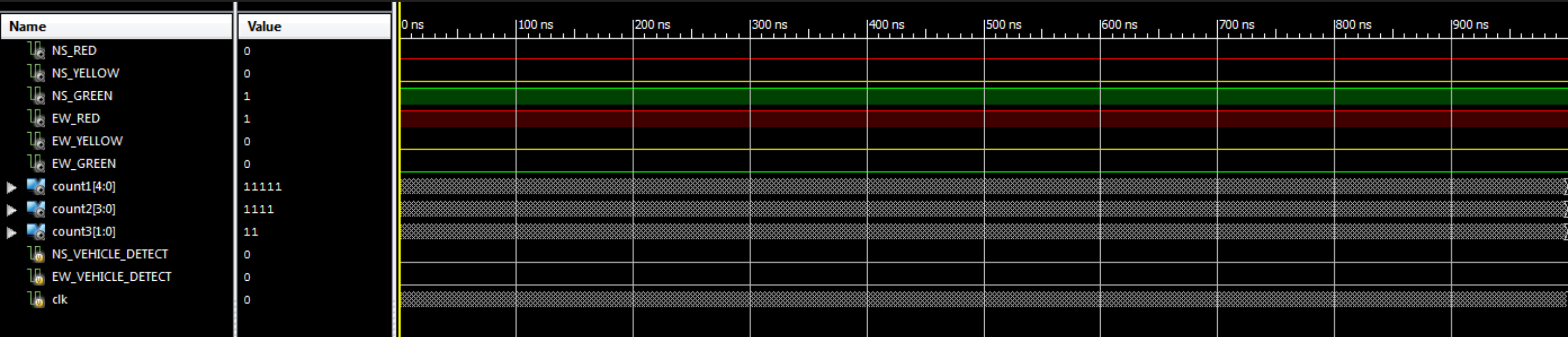
TEST B (6 AM)

```
initial begin
    clk = 0;
    NS_VEHICLE_DETECT = 0;
    EW_VEHICLE_DETECT = 1;

  $display("                NS | EW ");
    $display("              R Y G R Y G ");

  #1000 $finish;
  end

  always begin
  #1 clk = ~clk;
  end

always @ (clk) begin
  if ($time % 21 == 0) begin
        NS_VEHICLE_DETECT = ~NS_VEHICLE_DETECT;
        EW_VEHICLE_DETECT = ~EW_VEHICLE_DETECT;
    end
end
```
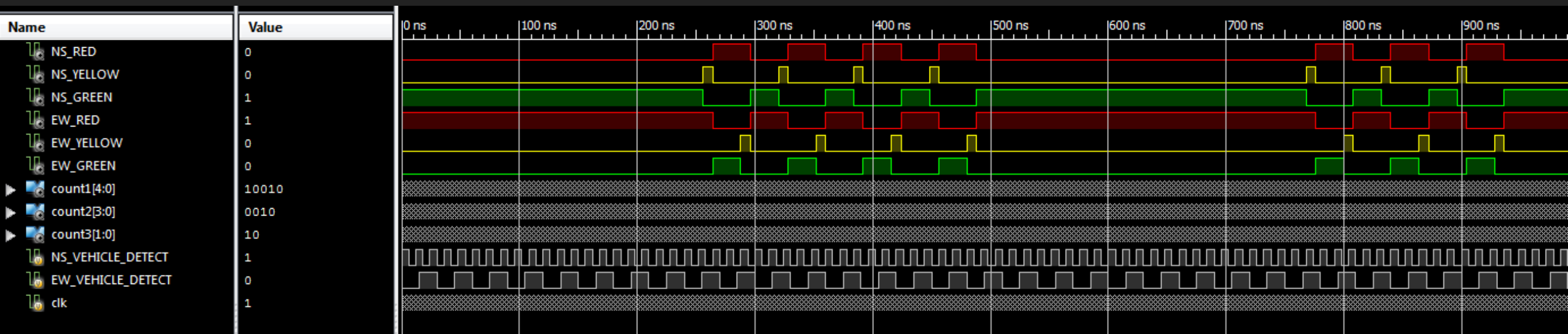
TEST C (9 AM)

```verilog
initial begin
    clk = 0;
    NS_VEHICLE_DETECT = 0;
    EW_VEHICLE_DETECT = 1;

  $display("             NS | EW ");
    $display("             R Y G R Y G ");

  #1000 $finish;
  end

  always begin
  #1 clk = ~clk;
  end

always @ (clk) begin
  if ($time % 15 == 0) begin
        NS_VEHICLE_DETECT = ~NS_VEHICLE_DETECT;
  end

  if ($time % 6 == 0) begin
        EW_VEHICLE_DETECT = ~EW_VEHICLE_DETECT;
  end
end
```
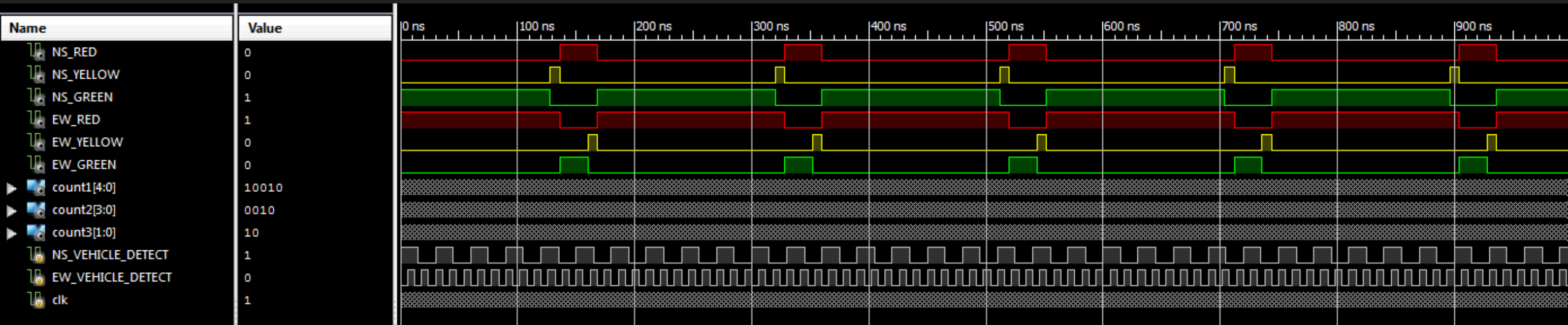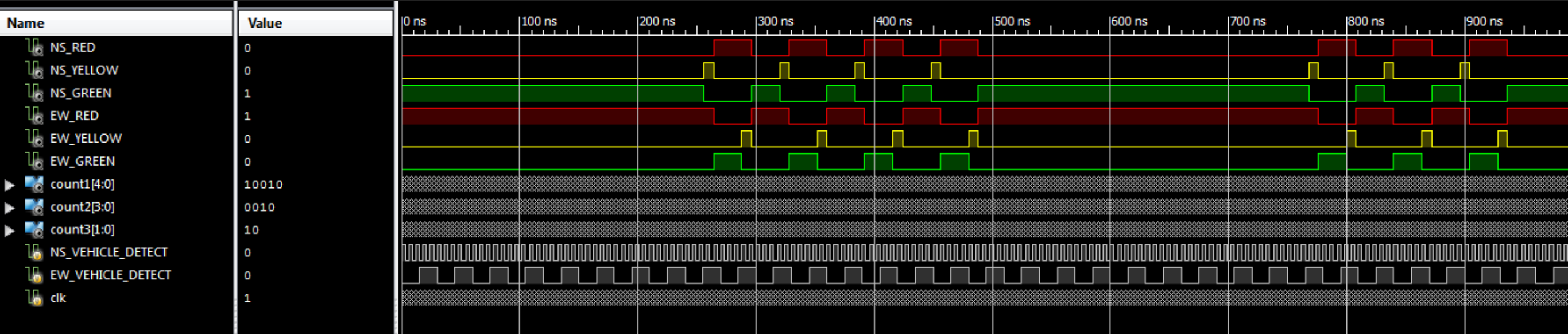
TEST D (11 AM)

```
initial begin
     clk = 0;
     NS_VEHICLE_DETECT = 0;
     EW_VEHICLE_DETECT = 1;

   $display("              NS | EW ");
     $display("              R Y G R Y G ");

   #1000 $finish;
   end

   always begin
   #1 clk = ~clk;
   end

always @ (clk) begin
  if ($time % 6 == 0) begin
       NS_VEHICLE_DETECT = ~NS_VEHICLE_DETECT;
   end

  if ($time % 15 == 0) begin
       EW_VEHICLE_DETECT = ~EW_VEHICLE_DETECT;
   end
end
```

TEST E (1 PM)

```
initial begin
    clk = 0;
    NS_VEHICLE_DETECT = 0;
    EW_VEHICLE_DETECT = 1;

  $display("             NS | EW ");
    $display("           R Y G R Y G ");

  #1000 $finish;
  end

  always begin
  #1 clk = ~clk;
  end

always @ (clk) begin
  if ($time % 2 == 0) begin
      NS_VEHICLE_DETECT = ~NS_VEHICLE_DETECT;
  end

  if ($time % 15 == 0) begin
      EW_VEHICLE_DETECT = ~EW_VEHICLE_DETECT;
  end
end
```
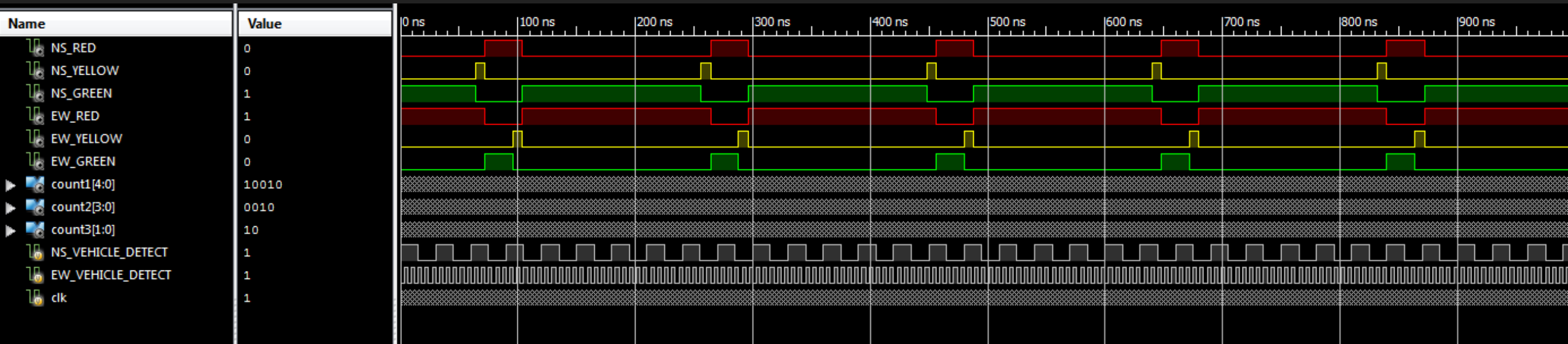
TEST F (2 PM)

```
    initial begin
        clk = 0;
        NS_VEHICLE_DETECT = 0;
        EW_VEHICLE_DETECT = 1;

       $display("              NS | EW ");
        $display("              R Y G R Y G ");


       #1000 $finish;
       end

       always begin
       #1 clk = ~clk;
       end

    always @ (clk) begin
      if ($time % 15 == 0) begin
           NS_VEHICLE_DETECT = ~NS_VEHICLE_DETECT;
      end

      if ($time % 2 == 0) begin
           EW_VEHICLE_DETECT = ~EW_VEHICLE_DETECT;
      end
    end
```
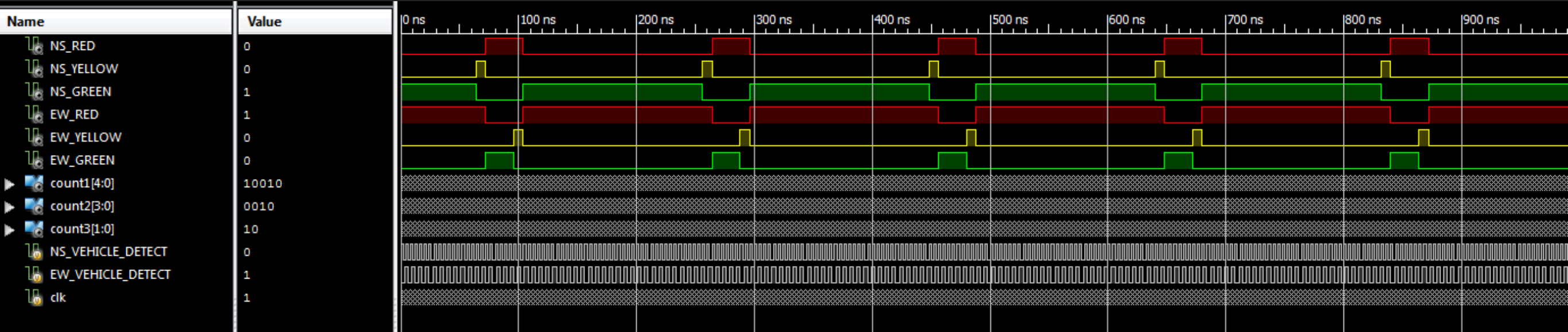
TEST G (3 PM)

```verilog
initial begin
    clk = 0;
    NS_VEHICLE_DETECT = 0;
    EW_VEHICLE_DETECT = 1;

  $display("            NS | EW ");
    $display("            R Y G R Y G ");

  #1000 $finish;
  end

  always begin
  #1 clk = ~clk;
  end

always @ (clk) begin
  if ($time % 2 == 0) begin
      NS_VEHICLE_DETECT = ~NS_VEHICLE_DETECT;
  end

  if ($time % 3 == 0) begin
      EW_VEHICLE_DETECT = ~EW_VEHICLE_DETECT;
  end
end
```
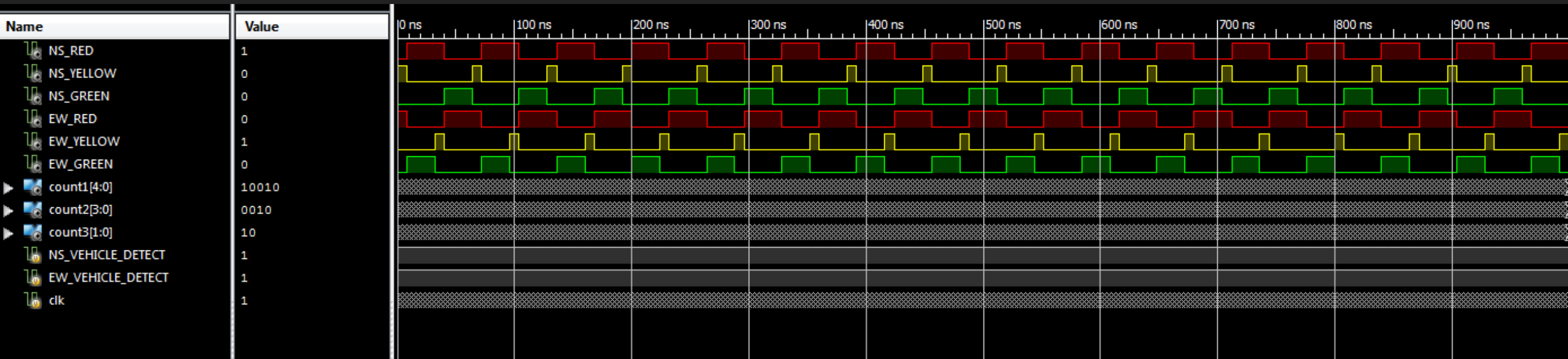
TEST H (RUSH HOUR)

```
initial begin
    clk = 0;
    NS_VEHICLE_DETECT = 1;
    EW_VEHICLE_DETECT = 1;

    $display("            NS | EW ");
    $display("            R Y G R Y G ");

#1000 $finish;
end

always begin
#1 clk = ~clk;
end
```

TRAFFIC LIGHT CONTROLLER

Kevin Ingram
Warren Seto