

LECTURE : 04

Date / /

#. Bus System:-

Topics -

Q. Bus System

Q. Bus Architecture

Q. Types of Architecture of Bus

Q. Bus Arbitration

* ----- *

Q. Bus System: A bus is a collection of wires that connects several devices.

→ Each wire can transfer 1 bit (0/1) of information at a time.

→ Buses are used to send control signals and data between the processor and other components.

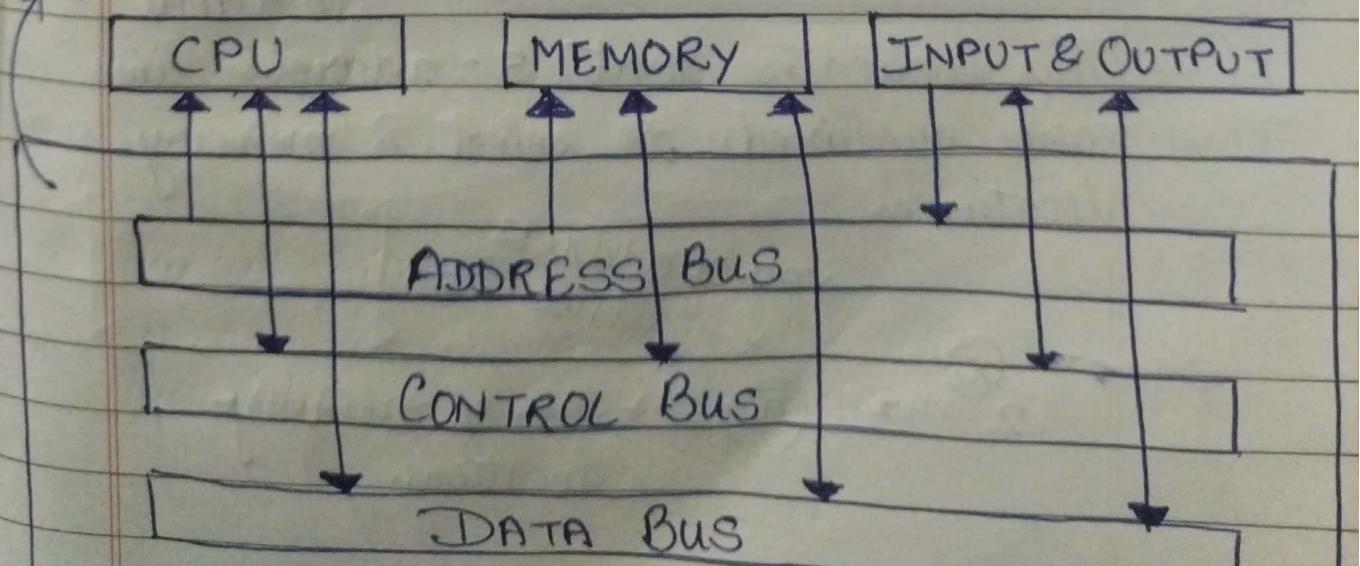
→ There are three types of buses in the bus system;

(i). Address Bus → Unidirectional

(ii). Data Bus → Bidirectional

(iii). Control Bus → Bidirectional

System
bus.



In 8085 Microprocessor: $\frac{A_{15} - A_8}{8}$ $\frac{AD_7 - AD_0}{8}$

$$2^X = 2^{16} = 64\text{K Cells} \\ = 64\text{KB.}$$

8DLS \rightarrow word length is
of 8 bits.

(i). Address Bus:

- It is a unidirectional ~~part of bus~~ system.
- When the address of current instruction in execution is transferred from the program counter (PC) to MAR i.e., Memory address Register. Then MAR locates that address in the memory unit via 'Address Bus.'
- Address bus width determines the maximum memory capacity.

Eg. If address bus is of 3-bit

$$\text{This 3 bits means } \rightarrow 2^3 = 8$$

Memory locations

This indicates that 3 - address lines are required to select 8 memory locations.

$$2^x = n \rightarrow \begin{array}{l} \text{no. of address lines} \\ \text{no. of memory locations.} \end{array}$$

In 8086 Microprocessor: $A_{19} - A_{16}$ $AD_{15} - AD_0$
 $2^x = 2^{20} = 1M$ cells
 $= 1MB.$ | 16 DLS \rightarrow word length is
of 16 bits. Date / /

(iii). Data Bus :-

- It is a bi-directional bus system.
- It is a group of wires that carries data information bits from processor to peripherals and vice-versa.
- Data Bus width determines the system performance i.e., the word length of the computer.
- It fetches instructions from the memory.

$$2^x = 2^3 = 8$$

The eight Memory locations

0		000	"word length"
1		001	
2		010	
3		011	
4		100	
5		101	
6		110	
7		111	

MEMORY STACK

(iii). Control Bus:-

- It is a bidirectional system bus.
- It is a group of wires that carries signals for data information synchronizing signals from the processor to peripherals for vice-versa.
- Control signals like ;

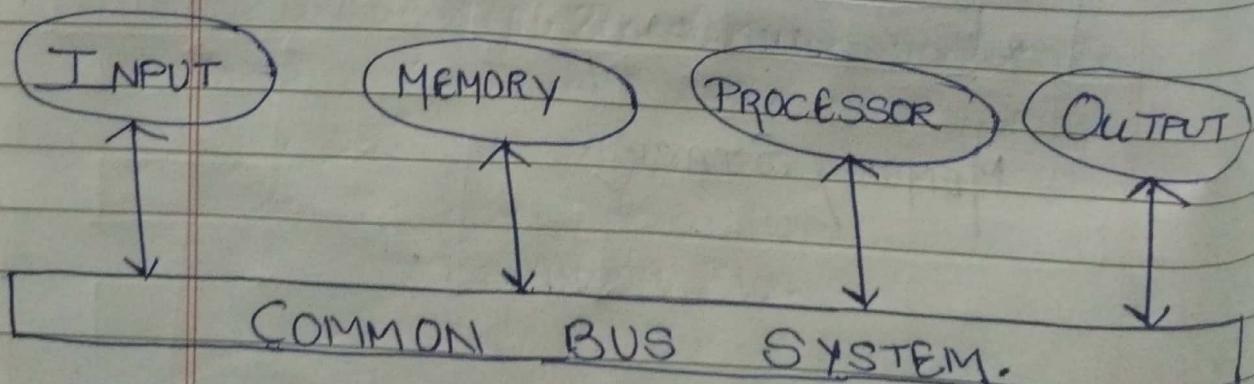
J10 read, J10 write etc....

4. Bus Structure :-

There are two types bus structures;

- (i). Single Bus structure
- (ii). Multi Bus structure

(i). Single Bus Structure:-



- It is the simple yet inefficient way to interconnect functional units.
- Here, a single bus system is used to communicate between peripherals and microprocessor.
- Single bus system does not transfer ~~multiple~~ multiple data simultaneously rather it does one transfer at a time. Thus, only two units are active at one scenario of transfer.

Two units means; one sender and other one is receiver.

- Bus control lines are used to arbitrate multiple requests for use of one bus.

→ Advantages;

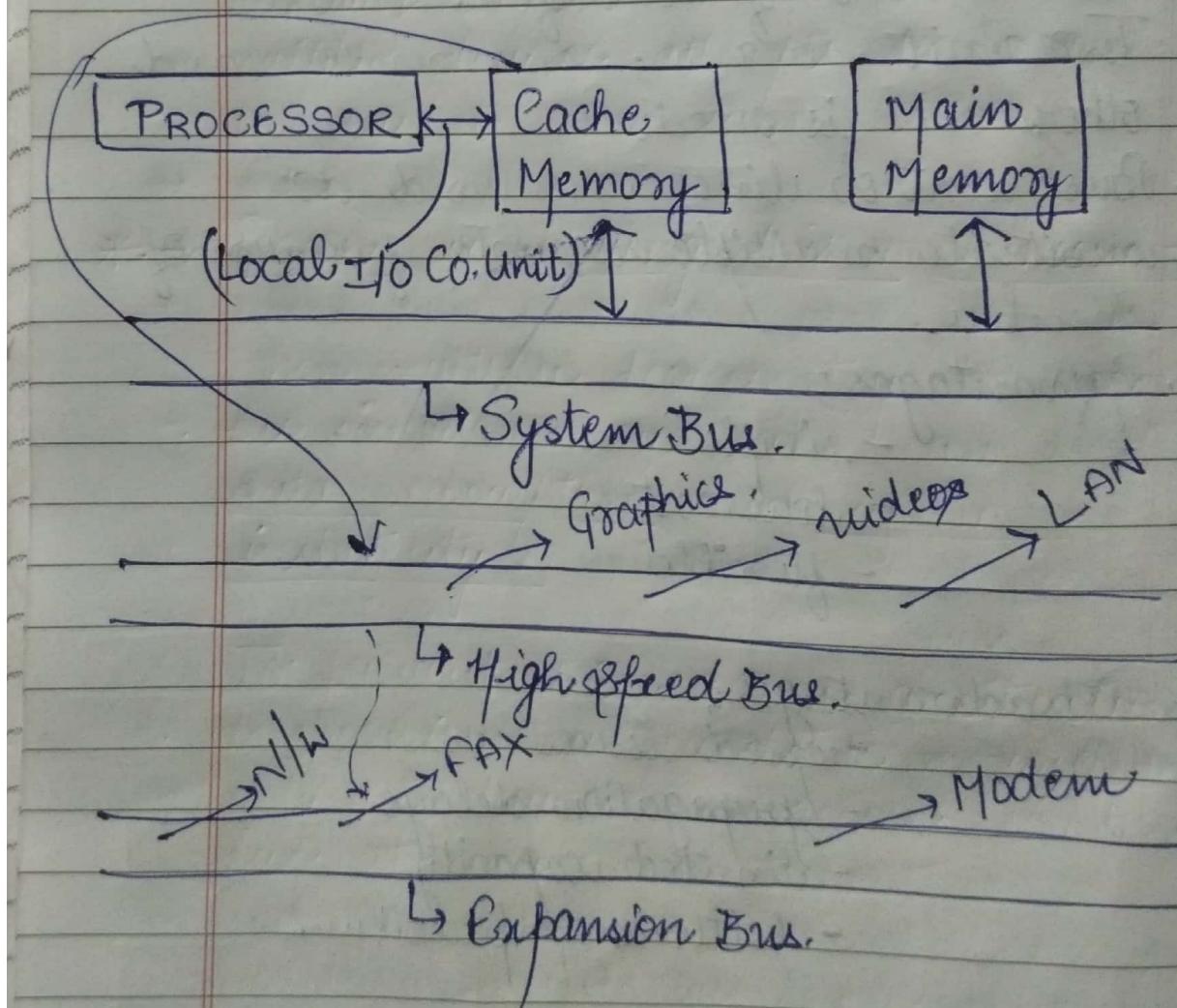
- simple
- low cost
- flexible

→ Disadvantages;

- speed issues
- propagation delays
- limited capacity
- bottle neck problem.

→ The solution for this structural Bus architecture is improving the structure by introducing registers and dividing the system bus into different forms of system bus i.e., data bus, control bus and address bus.

(ii). Multi-Bus structure:-



f. Bus Arbitration :-

→ Definition - The bus arbitration is the process by which the active bus master access the bus, relinquishes the control of it and then transfer it to a different bus-seeking processor unit.

Note: A 'bus master' is a controller that can access the bus for a given instance.

→ A conflict occurs if multiple DMA controllers, other controllers or processor attempt to access the common bus simultaneously, yet only one is allowed to dedicatedly access the bus at a time.

The 'bus master' status can only be held by one processor controller at once. By coordinating the actions of all devices or processor units seeking memory transfer, the bus arbitration method is used to resolve these disputes.

Approaches:

1. Centralized Bus Arbitration
2. Distributed Bus Arbitration
3. De-Centralized Bus Arbitration.

- In a computer system, multiple devices such as; CPU, memory and I/O controllers, are connected to a common communication pathway, known as the bus.
- In order to transfer data between these devices, they need to have access to the bus.
- Bus Arbitration; is the process of resolving conflicts that arise when multiple devices attempts to access the bus at the same time.

*. → Reason for having this mechanism -

When multiple devices try to use the bus simultaneously, it can lead to data corruption and system instability.

To prevent this, a bus arbitration mechanism is used to ensure that only one device has access to the bus at any given time.

→ As already stated, three approaches are there in this mechanism; centralized, decentralized and distributed.

* General Definitions and Meaning of each approach;

(i). Centralized Bus Arbitration; each device has its own priority. A single device, known as the controller, is responsible for managing access to the bus.

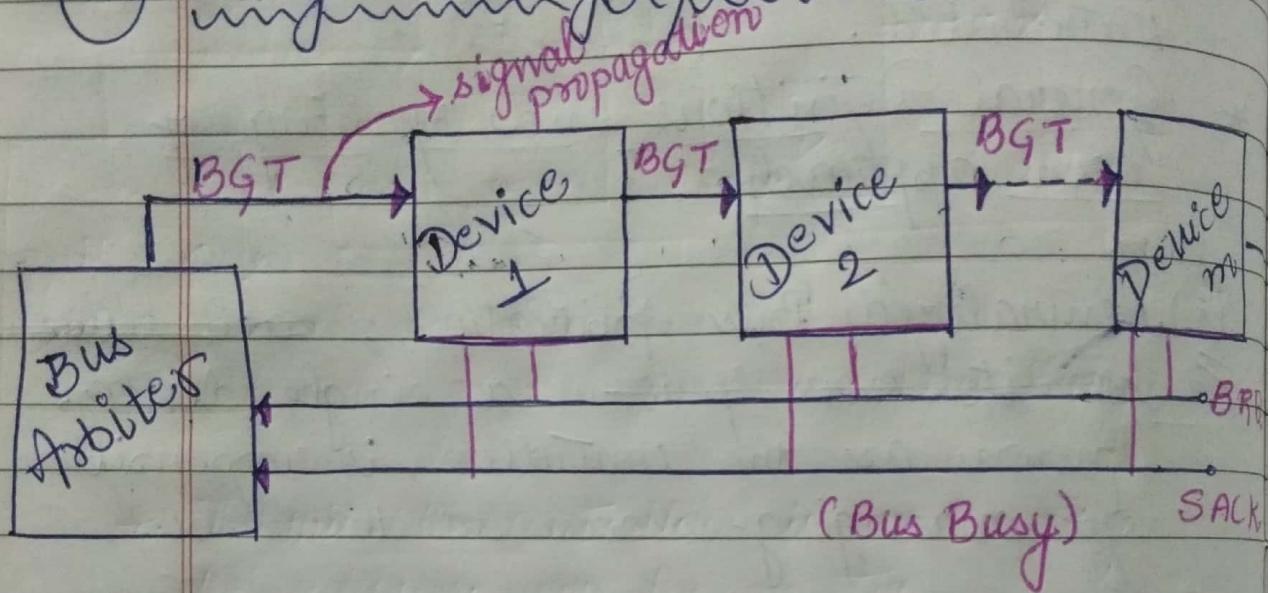
(ii). Decentralized Bus Arbitration; each device has its own priority level and the device with the highest priority is given access to the bus.

(iii). Distributed Bus Arbitration; devices compete for access to the bus by sending a request signal and waiting for a grant signal.

Note: The controller that has access to a bus at an instance is known as 'Bus Master.' The Bus Arbiter

decides who becomes the current Bus Master.

METHODS OF:

#. CENTRALIZED Bus ARBITRATION:(A). Daisy Chaining Method:

- It is simple and cheaper method where all the bus masters use the same line for making 'Bus Request.'
- The Bus grant signal (BGT) propagates through each bus master until it encounters the first one that is requesting access to the bus.
- The current bus master blocks the propagation of the bus grant signal, therefore only other requesting module will not receive the grant signal in the current bus cycle and hence cannot access the bus.

- By this way, this methodology of the centralized bus arbitration ensures there should be no data corruption or system instability.
- During any bus cycle, the bus may be any device - the processor or any DMA controller unit connected to the bus.
BGT

ADVANTAGES -

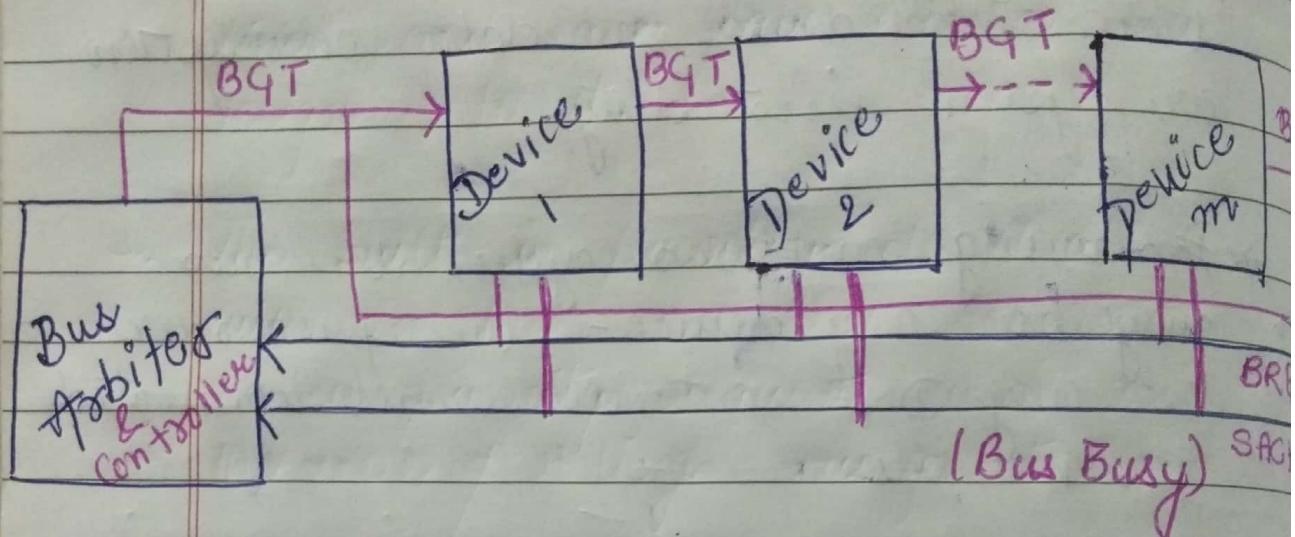
1. Simplicity and Scalability
2. The user can add more devices anywhere along the chain, up to a certain maximum value.

DISADVANTAGES -

1. The value of priority assigned to a device depends on the position of the master bus.
2. Propagation delay arises in this method.
3. If one device fails then the entire system will stop working.

(B)

Polling or Rotatory Priority Method



- In this, the controller is used to generate the address for the master.
- The controller generates the sequence of master addresses.
- When the requesting bus master recognizes its address, it activates the busy line and begins to use the bus.
- Here, the no. of address lines depends upon the no. of devices (masters) connected in the system.

ADVANTAGES:

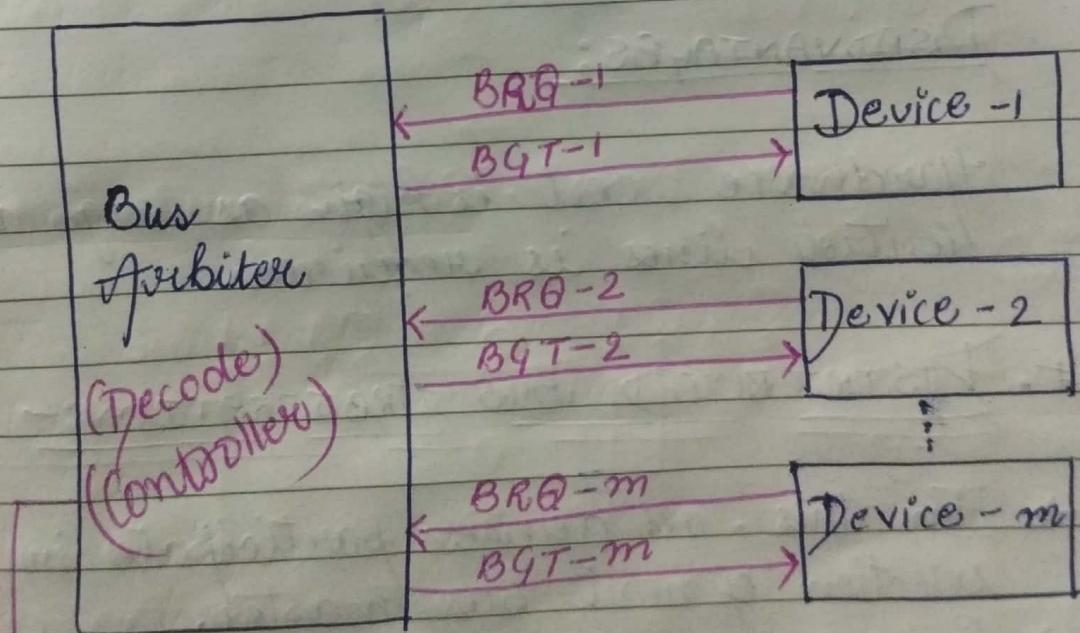
1. This method does not favour any particular device over processor.

2. This method is also quite simple.
3. If one device fails then the entire system will ~~stop~~ not stop working.

DISADVANTAGES:

1. Adding Bus masters is difficult as increases the number of address lines of the ~~circuit~~ circuit.
2. Efficient yet non-scalable.

(C). Fixed-Priority or Independent Request Method:



- Assigns Priority based upon request received.
- Non Scalable and Efficient both.

- In this, each master has a separate pair of bus request and bus grant lines and each pair has a priority assigned to it.
- The built-in priority decoder within the controller selects the highest priority request and asserts the corresponding bus grant signal.
- ADVANTAGES:

- 1. This method generates a fast response.

DISADVANTAGES:

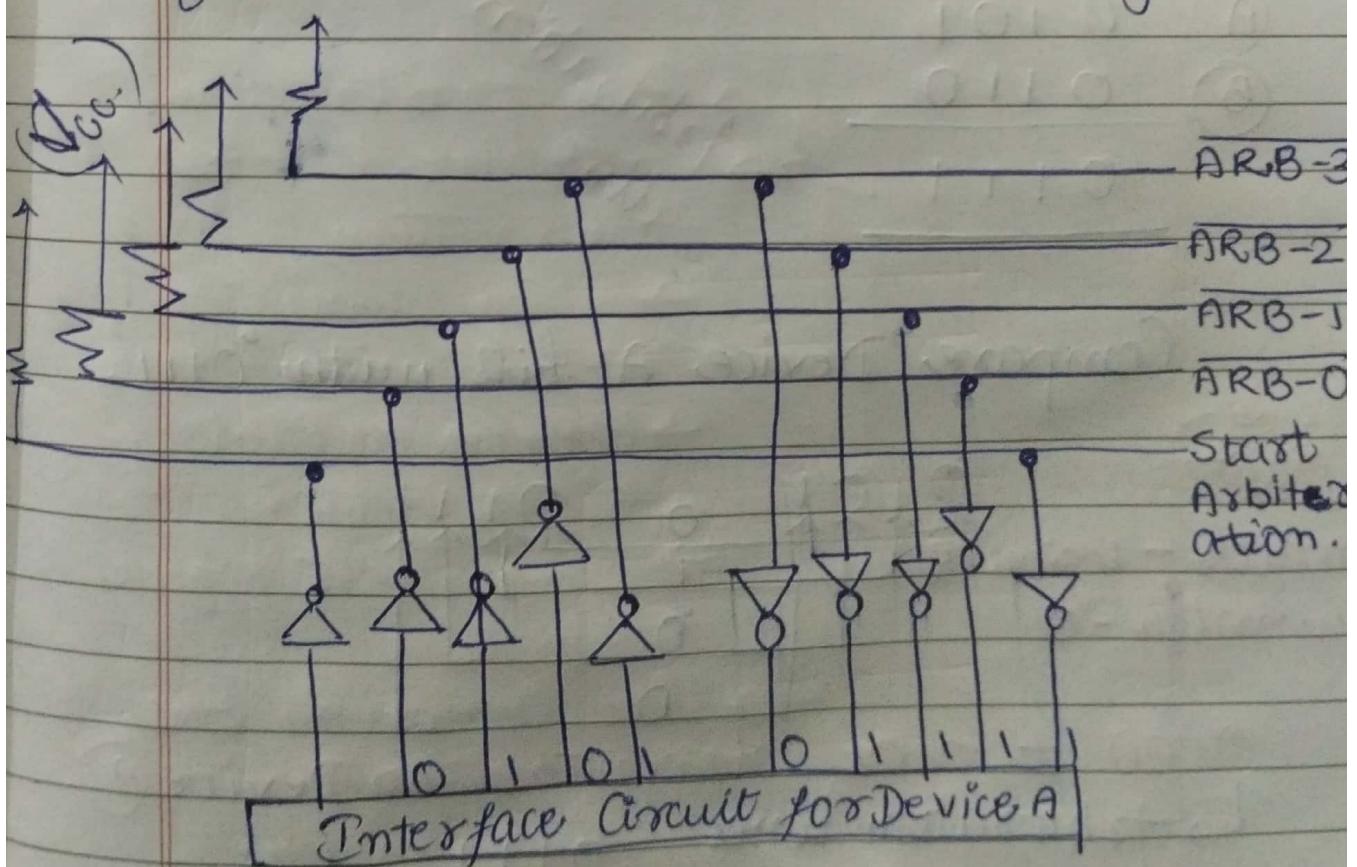
- 1. Hardware cost is high as large no. of control lines is required.

#. DISTRIBUTED Bus ARBITRATION:-

- In this, all devices participate in the selection of next bus master.
- Each device on the bus is assigned a 7-bit identification number. The priority of the device is generated based upon the generated ID.

Date / /

- All devices waiting to use the bus, share the responsibility of carrying out the arbitration process as the arbitration process does not depend on a central arbiter and hence distributed bus arbitration process has higher priority.
- All devices are connected using 5-lines, 4 arbitration lines to transmit the ID and one line for the start-arbitration signal.



Logical 'OR' -

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

Device - A - 5 \rightarrow 0101

Device - B - 6 \rightarrow 0110

Logical OR of 6 & 5 is;

(A) 0101

(B) 0110

0111

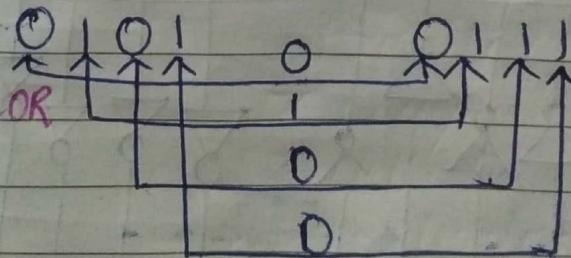
Arbitration
line.

Compare Device A bits with '0111'.

Logical
(OR)

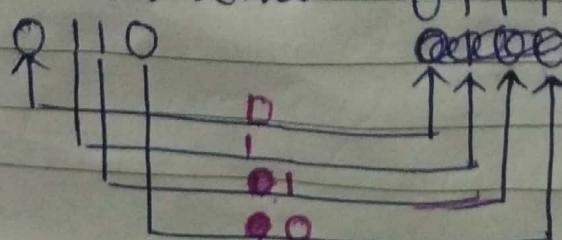
match - logical OR

unmatch - 0



$0100 \neq 0101$ no control to Device A

Arbitration lines



f. Uses of Bus Arbitration :-

1. Efficient use of system resources
2. Minimizing data corruption
3. Support for multiple devices.
4. Real-time system support.
5. Improved system-stability.

f. Applications of Bus Arbitration :-

1. Shared Memory System
2. Multi-Processor Systems
3. Input/Out Devices synchronization
4. Real time systems
5. Embedded systems.

System Bus.

→ Types of Buses in
Any System Bus

→ Address Bus

→ Control Bus

→ Data Bus.

→ Bus System Architecture

→ single Bus
architecture

→ Multi-Bus architecture

→ Bus Arbitration

→ Centralized Bus
Arbitration

→ Daisy Chaining
Method

→ Polling or Rotatory
Priority Method

→ Independent Request
Method.

→ Decentralized Bus
Arbitration

→ Distributed Bus
Arbitration

* uses | Applications