

# Field Effect Transistor (FET)

## Contents :

- Introduction to BJT
- Transistor construction
- Transistor symbols.

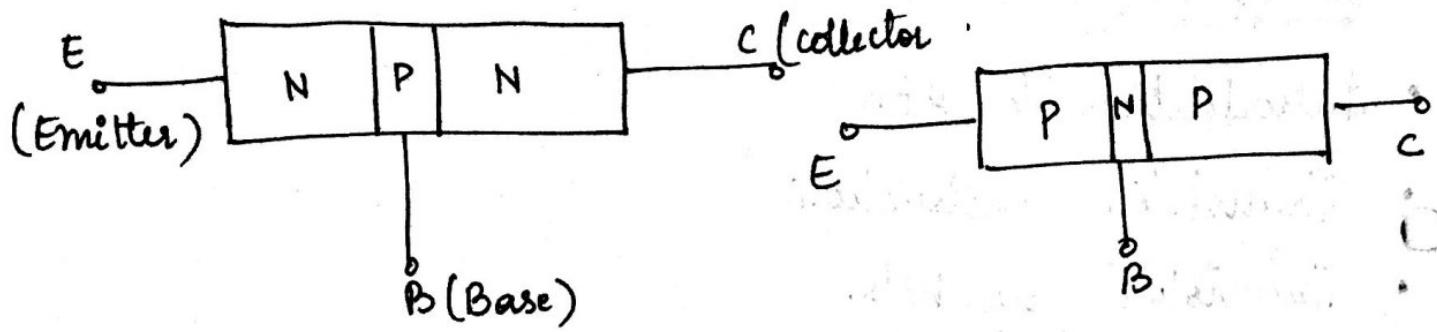
## Introduction to BJT

- Bipolar Junction Transistor is a three terminal device. The terminals are emitter, base and collector.
- Main application - Amplification.
- BJT is called bipolar because the conduction in BJT is due to both electrons and holes.
- BJT is a current controlled device.
- The term transistor is derived from 'transistor' and resistor. In the operation of BJT, the input current is transferred from a low resistance circuit to a high resistance circuit.

- Types of Transistors :

- pnp
- npn.

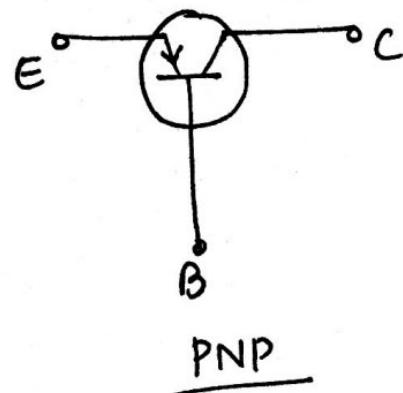
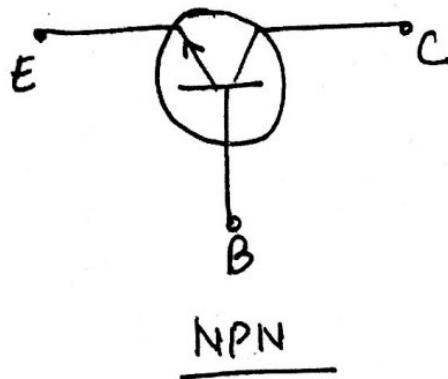
## Transistor Construction



- BJT is a three layer semiconductor device consisting of either two n and one p type layer <sup>(NPN)</sup> or two p and one n type layer (PNP).
- The emitter is heavily doped, because the function of emitter is to produce the charge carriers, so more the doping, more will be the charge carriers.
- Base is thin and very lightly doped, because the function of base is to pass on the charge carriers to the collector. So in order to minimize recombination, base is made thin and lightly doped.

collector is made wide and moderately doped.

## Transistor Symbols



NPN transistor is preferred over PNP transistor because NPN has majority of electrons whereas PNP has majority carriers as holes. The mobility of electrons is high as compared to that of holes. More the mobility, more will be the resulting current. Hence NPN transistor is preferred over PNP.

## University Questions

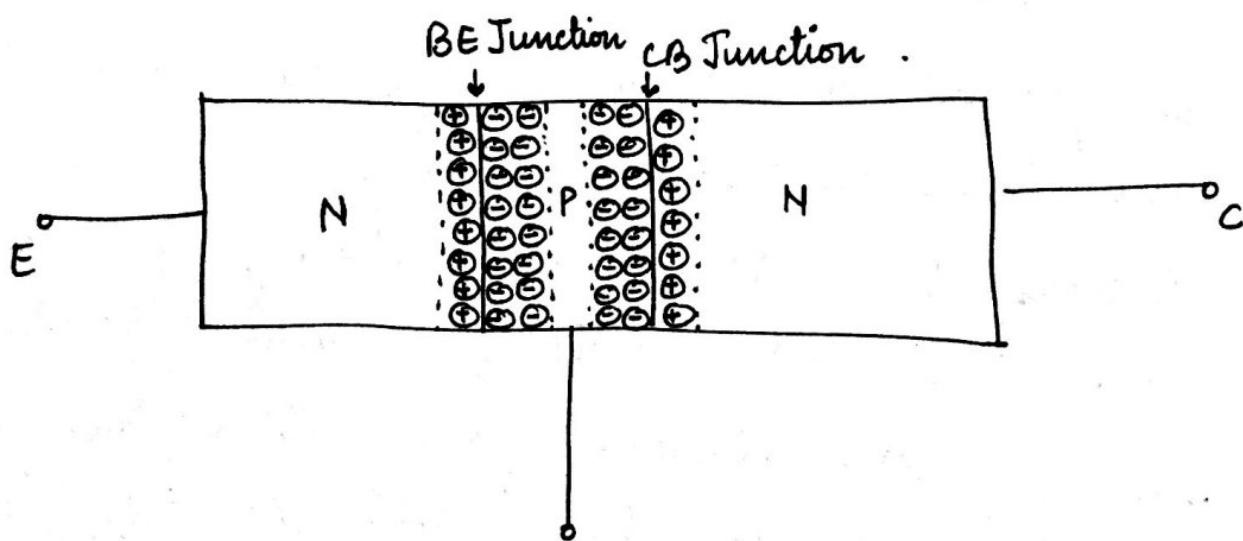
- Q1. Explain why BJT is a bipolar device. (2 Marks)  
(2015-16).
- Q2. The thickness of base is typically smaller than emitter and collector. Why? (2016-17)  
(2 Marks)

## Unit 2 : BJT and FET

### Contents :

- Unbiased BJT
- Transistor operation
- Transistor as two port Network.

### Unbiased Bipolar Junction Transistor (BJT)



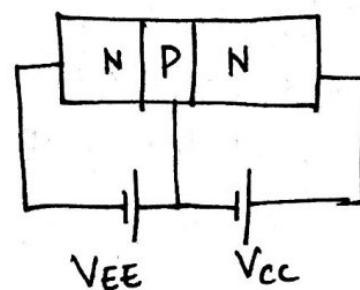
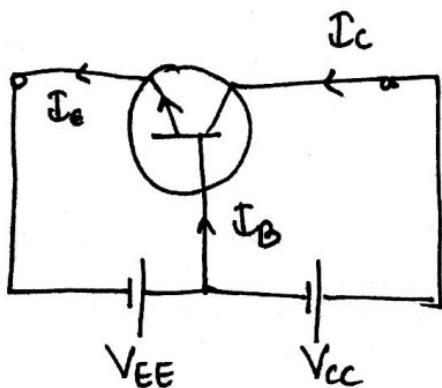
- The depletion layers are formed at B-E and C-B junction.
- The depletion layer extends more into the base as it is lightly doped.

### Biassing of BJT

| S.N | <u>B-E Junction</u> | <u>C-B Junction</u> | <u>Operation Region</u> |
|-----|---------------------|---------------------|-------------------------|
| 1.  | Forward             | Reverse             | Active (Amplifier)      |
| 2.  | Forward             | Forward             | Saturation (switch)     |
| 3.  | Reverse             | Reverse             | Cut off                 |
| 4.  | Reverse             | Forward             | Inverted                |

# Transistor operation

## NPN transistor operation in Active Region

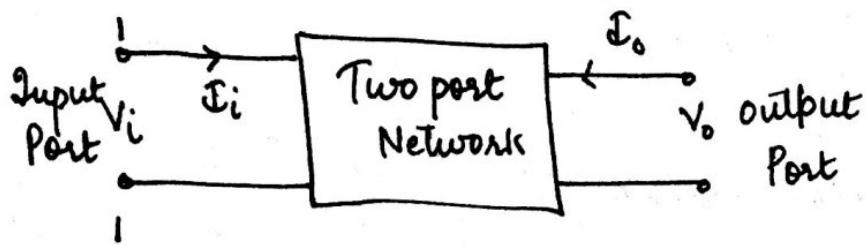


- $V_{EE}$  forward biases the E-B junction and  $V_{CC}$  reverse biases the C-B junction.
- Electrons in emitter start flowing towards the base. This will constitute emitter current  $I_E$ .
- Some of the electrons from emitter then recombine with the holes in the base. As base is thin and lightly doped, holes are very few. This constitute a very small base current  $I_B \approx 0$ .
- The remaining large number of electrons pass through the depletion layer of C-B junction and are attracted towards the positive terminal of  $V_{CC}$ . This constitutes collector current  $I_C$ .

$$I_E = I_C + I_B$$

Transistor current equation

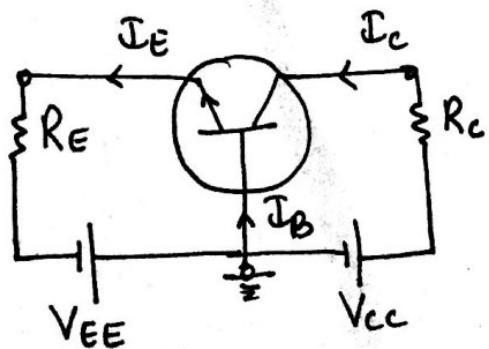
# Transistor as two port Network



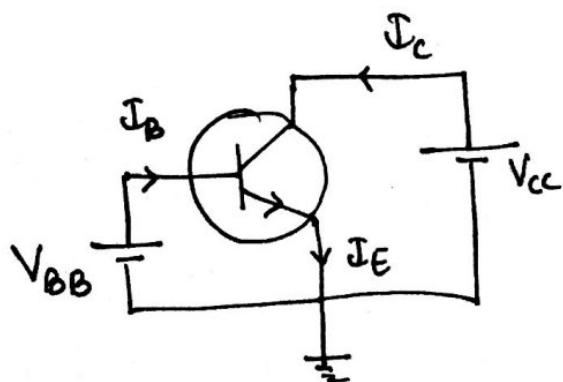
Depending on which terminal is made common to input and output port, there are three transistor configurations.

- Common Base
- Common Emitter
- Common Collector

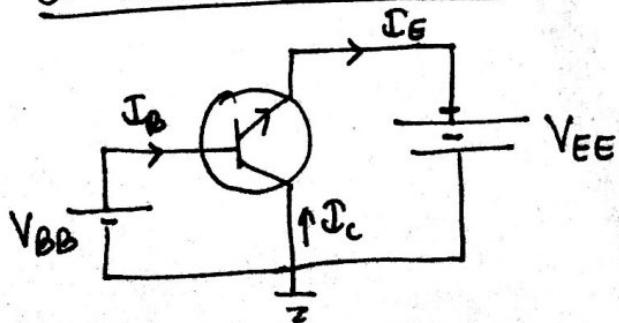
## Common Base



## Common Emitter



## Common Collector



## University Questions

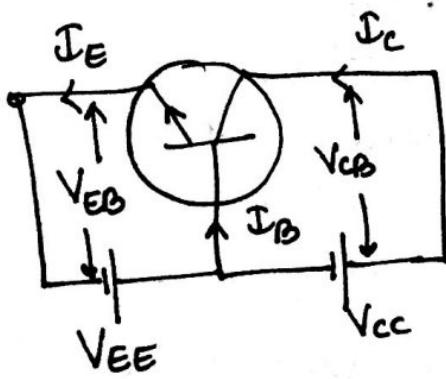
- Q. How the two transistor junctions must be biased for proper operation of transistor amplifier (2 Marks) (2012-13).
- Q. Which of the transistor currents is always the largest? Which one is the smallest? Which two are relatively close in magnitude? (5 Marks) (2009-10)
- Q. Explain the operation of npn transistor. Write down the transistor current equation.

## Unit 2: BJT and FET

### Contents :

- Common Base Configuration. (C-B)
- Current gain common base configuration.
- Input and output characteristics of common base configuration.

### Common Base Configuration



$$I_E = I_C + I_B$$

The collector current consist of two components : majority and minority carrier current.

$$I_C = I_{C\text{majority}} + I_{C\text{minority}} \quad (\text{leakage current})$$

### Current gain in Common Base

$$\text{current gain } \alpha = \frac{I_C}{I_E}$$

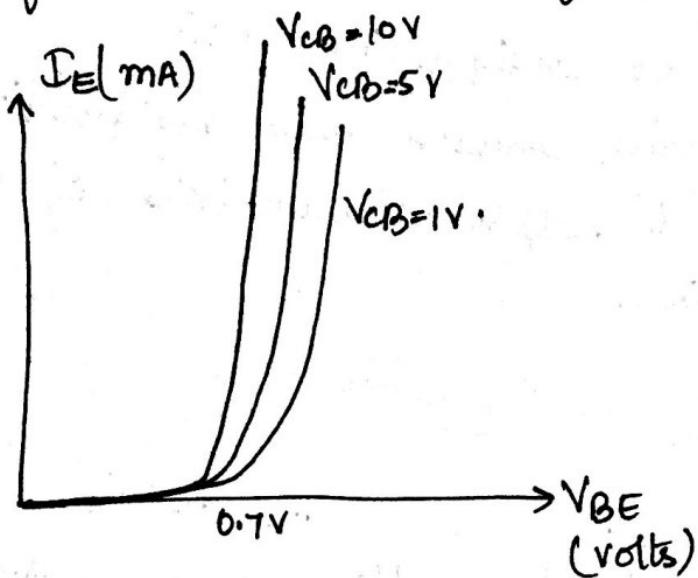
$$I_C = \alpha I_E + I_{CB0}$$

(current in collector to base when emitter is open)

$$\alpha < 1$$

## Characteristics of Common Base Configuration

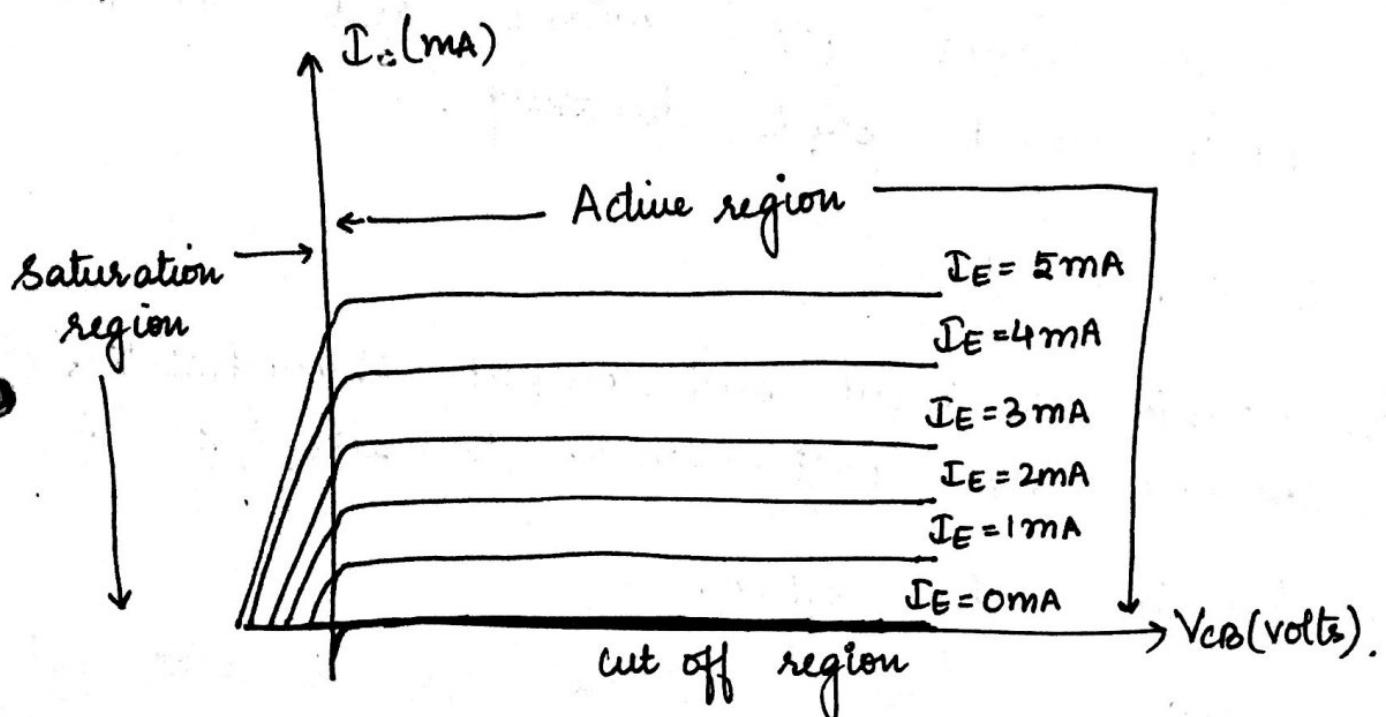
Input characteristics: Input characteristics of common base is the curve of input current ( $I_E$ ) versus input voltage ( $V_{EB}$ ) for constant values of output voltage ( $V_{CB}$ ).



- The input characteristics of common base is similar to that of a forward biased PN diode.
- When  $V_{CB}$  increases,  $I_E$  increases and the curve shifts towards left. This is due to early effect.
- Early Effect: When  $V_{CB}$  increases, the reverse bias in the collector base junction increases, due to which the width of depletion layer in C-B junction also increases. The depletion layer penetrates more into the base. Thus the effective width of base where recombination can take place decreases. Therefore  $I_B$  decreases and  $I_E$  increases.

## Output characteristics :

The output characteristics is the graph of output current ( $I_c$ ) versus output voltage ( $V_{CB}$ ) for different values of input current ( $I_E$ ).



- The output characteristic curve shows three regions : active, cut off, saturation ..
- $I_c = \alpha I_E + I_{CBO}$ .  
When  $I_E = 0$ ,  $I_c = I_{CBO}$ .  $I_{CBO}$  is very small in magnitude.  $I_{CBO} \approx 0$  and hence  $I_c \approx 0$ .
- When  $I_E$  becomes non zero, according to transistor current relation  $I_c \approx I_E$  in active region.
- $V_{CB}$  does not have any effect on  $I_c$  in active region.

- In the cut off region  $I_C = 0$  A.
- The saturation region lies to the left of  $V_{CB} = 0$  V. When  $V_{CB}$  becomes negative, it becomes forward biased. The direction of collector current gets reversed and the overall collector current starts decreasing.

### University Questions:

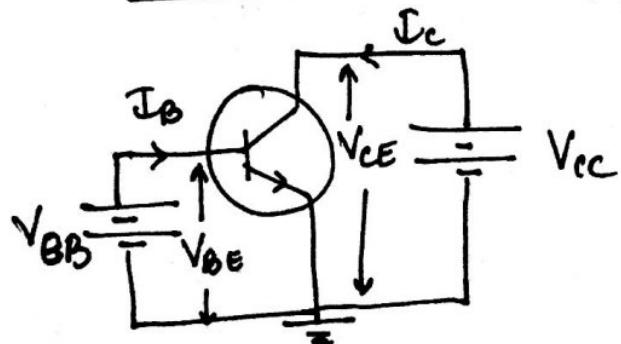
- Q. Explain the input and output characteristics of common base configuration. (5 Marks) (2015-16).
- Q. Explain early effect.
- Q. Draw the basic structure of CB BJT and explain its principle of operation with neat diagram along with its input and output characteristics.

## Unit 2: BJT and FET

### Contents :

- Common emitter configuration
- Current gain
- Relation between  $\alpha$  and  $\beta$
- Characteristics of common emitter.

### Common emitter Configuration



### Current gain in common emitter

$$\beta = \frac{I_c}{I_B} \quad (\beta \gg 1)$$

$$I_c = \beta I_B + I_{CEO}$$

(leakage current).

### Relation between $\alpha$ and $\beta$

$$I_E = I_c + I_B$$

divide by  $I_c$

$$\frac{I_E}{I_C} = 1 + \frac{I_B}{I_C}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\frac{1}{\alpha} = \frac{\beta+1}{\beta}$$

$$\boxed{\alpha = \frac{\beta}{1+\beta}}$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

$$I_C = \alpha I_E + I_{CBO} \quad (\text{common base configuration})$$

$$I_C = \alpha(I_C + I_B) + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha} \quad (\alpha = \frac{\beta}{1+\beta})$$

$$\boxed{I_C = \beta I_B + (1+\beta) I_{CBO}} \quad (\text{common emitter})$$

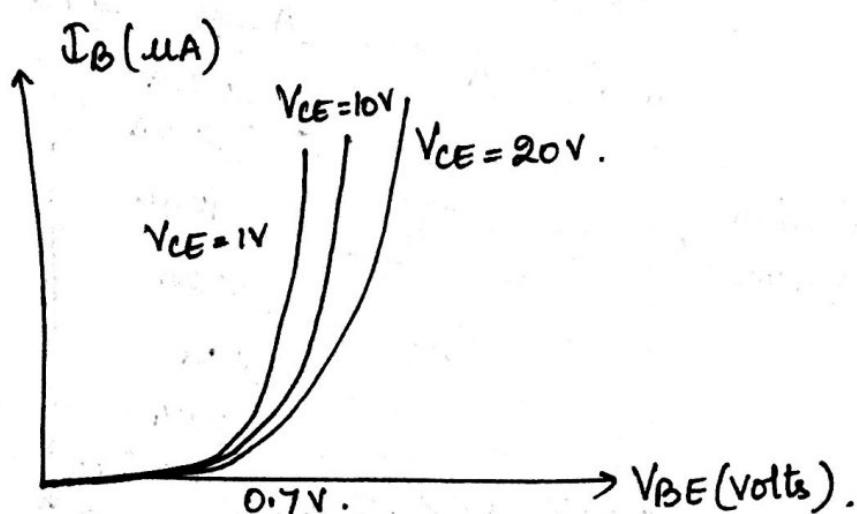
↓  
leakage current

$$I_C = \beta I_B + I_{CEO}$$

$$\boxed{I_{CEO} = (1+\beta) I_{CBO}}$$

## Characteristics of Common Emitter

Input characteristics : Input characteristics is the curve of input current ( $I_B$ ) versus input voltage ( $V_{BE}$ ) for different values of output voltage ( $V_{CE}$ ).



- The input characteristics of common emitter is similar to that of a forward biased PN junction diode.
- The curve shifts towards right on increasing the values of  $V_{CE}$ .

$$V_{CE} = V_{CB} + V_{BE}$$

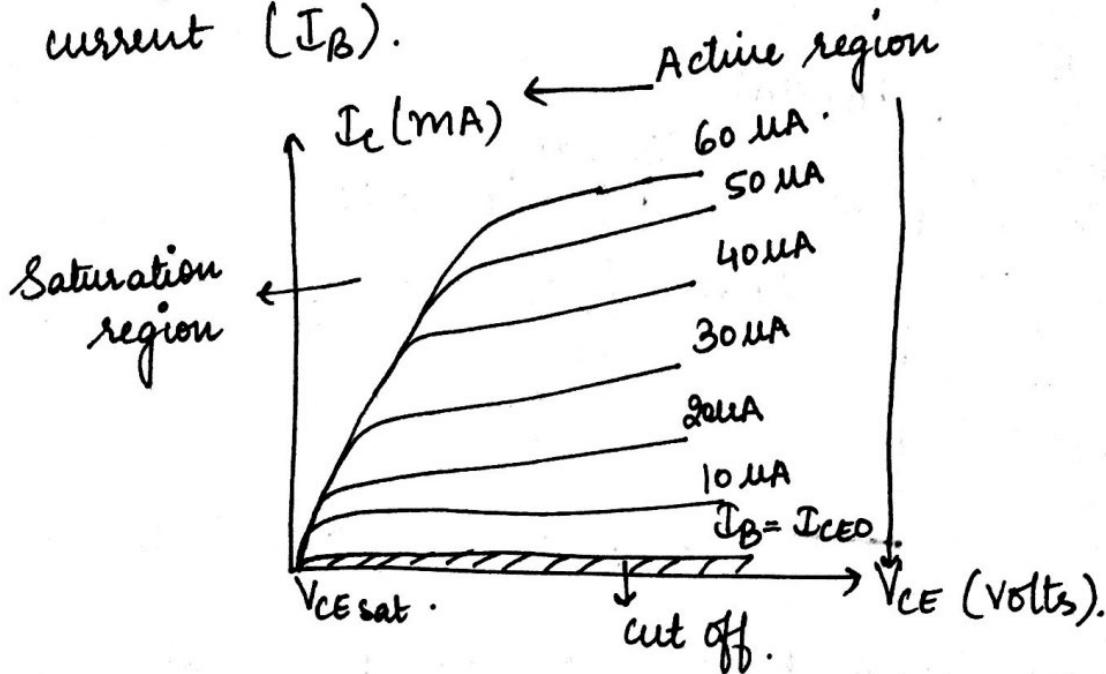
As can be seen from the curve,  $V_{BE} = 0.7$  V for any level  $I_E$  above 0 mA.

Therefore as  $V_{CE}$  increases  $V_{CB}$  increases and due to early effect  $I_B$  decreases.

(discussed in lecture 18).

Thus the curve shifts towards right.

Output characteristics : Output characteristics is the curve of output current ( $I_C$ ) versus output voltage ( $V_{CE}$ ) for different values of input current ( $I_B$ ).



- The output characteristic curve of common emitter shows three regions : active, saturation and cut off.

- $I_C = \beta I_B + I_{CEO}$   
(Leakage current)

When  $I_B = 0$   $I_C = I_{CEO}$ ,  $I_{CEO}$  value is greater than that of  $I_{CBO}$  as  $I_{CEO} = (1+\beta) I_{CBO}$  and  $\beta \gg 1$ .

- For the cut off region  $I_C = 0$  A.

In the active region,  $I_C$  increases slightly with an increase in  $V_{CE}$ . This slope is again due to early effect. (discussed in lecture 18).

- However, with small increase in  $I_B$ ,  $I_C$  increases considerably because  $I_C = \beta I_B$ .
- Thus the output current depends on the input current.
- The region to the left of  $V_{CESAT}$  is the saturation region.

$$V_{CE} = V_{CB} + V_{BE} \quad (V_{BE} = 0.7 \text{ V})$$

$$\boxed{V_{CB} = V_{CE} - 0.7}$$

As  $V_{CE}$  drops down to 0.2 V,  $V_{CB}$  becomes negative and hence collector-Base junction becomes forward biased.

- In this region (saturation), transistor behaves as a switch.

## University Questions

very important  
Q. Draw and explain the input and output characteristics of common emitter configuration  
(5 Marks) (2015-16)

- Q. Establish the relationship between  $I_{CBO}$  and  $I_{CEO}$  (2 marks) (2013-14).
- Q. Define  $\alpha$  and  $\beta$  with respect to BJT and derive relationship between them (5 marks)  
(2008-09) (2017-18)

## Numericals.

Q1. The collector and base current of NPN transistor are measured as  $I_C = 5 \text{ mA}$ ,  $I_B = 50 \mu\text{A}$  and  $I_{CBO} = 1 \mu\text{A}$ .  
 $\alpha = 0.99$     $\beta = 100$   
• Determine  $\alpha$ ,  $\beta$  and  $I_E$        $I_E = 5.050 \text{ mA}$

Q2. In an NPN transistor  $\alpha = 0.98$ ,  $I_E = 10 \text{ mA}$ ,  $I_{CBO} = 1 \mu\text{A}$ . Determine  $I_C$ ,  $I_B$ ,  $\beta$ ,  $I_{CEO}$ .

Ans:  $I_C = 9.80 \text{ mA}$     $I_B = 0.199 \text{ mA}$     $\beta = 49$ ,

Q3. If the base current of transistor is  $\frac{I_{CBO}}{\alpha} = 50 \mu\text{A}$  when  $I_E = 7.2 \text{ mA}$ , what are the values of  $\alpha$  and  $\beta$ .

Ans:  $\alpha = 0.99$   
 $\beta = 239$ .

Q4. An npn transistor with  $\beta = 98$  is operated in common base configuration, if the emitter current is  $2 \text{ mA}$  and reverse saturation current is  $12 \mu\text{A}$ . What are the base and collector current? (2016-17)

$$\alpha = 0.98$$

$$I_c = 1.97 \text{ mA}$$

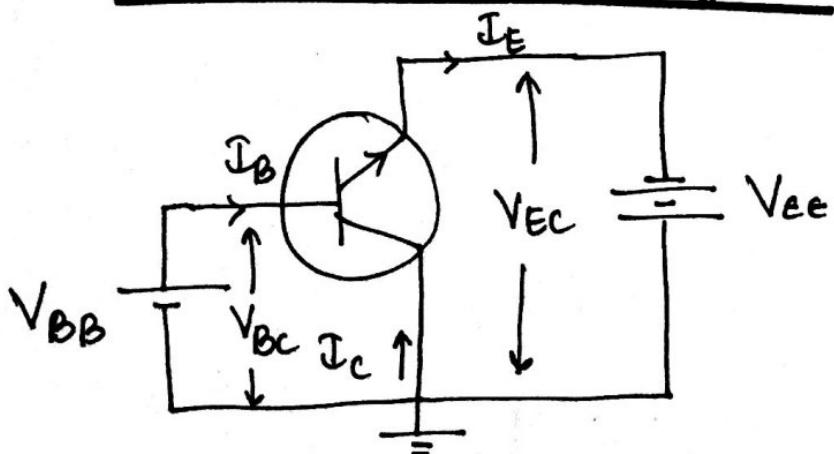
$$I_B = 28 \mu\text{A}$$

## Unit 2 : BJT and FET

### Contents :

- Common collector configuration (cc)
- current gain in CC
- Relation between  $\alpha$ ,  $B$  and  $\gamma$ .
- comparison of CB, CE and cc.

### Common Collector Configuration



- Also called as Emitter follower.
- The common collector configuration is used mainly for impedance matching purposes because it has high input impedance and low output impedance. and its voltage gain is unity

### Current gain

$$\gamma = \frac{I_E}{I_B} \quad \gamma \gg 1$$

## Relation between $\alpha$ , $B$ and $\gamma$

$$\alpha = \frac{I_C}{I_E} \quad B = \frac{I_C}{I_B} \quad \gamma = \frac{I_E}{I_B}$$

$$I_E = I_C + I_B.$$

## Relation between $\alpha$ and $\gamma$

Dividing the transistor current equation by  $I_E$  we get.

$$1 = \frac{I_C}{I_E} + \frac{I_B}{I_E}$$

$$1 = \alpha + \frac{1}{\gamma}$$

$$\alpha = 1 - \frac{1}{\gamma}$$

$$\boxed{\alpha = \frac{\gamma - 1}{\gamma}}$$

$$\boxed{\gamma = \frac{1}{1 - \alpha}}$$

## Relation between $\gamma$ and $B$

Dividing the transistor current relation by  $I_B$  we get.

$$\frac{I_E}{I_B} = \frac{I_C}{I_B} + 1$$

$$\boxed{\gamma = 1 + B}$$

$$\boxed{\gamma = \frac{1}{1-\alpha}}$$

$$\boxed{\gamma = 1+\beta}$$

$$\Rightarrow 1 = \gamma(1-\alpha) \quad 1 = \gamma - \beta$$

As the L.H.S of above equations are equal,  
lets equate the R.H.S of the equations

$$\gamma(1-\alpha) = \gamma - \beta$$

$$\gamma - \gamma\alpha = \gamma - \beta$$

$$\gamma\alpha = \beta$$

$$\boxed{\gamma = \frac{\beta}{\alpha}}$$

Note: The characteristics of common collector are almost similar to that of common emitter configuration.

### Comparison of CB, CE, CC Configuration

| S.N | Parameters      | CB                                   | CE                                    | CC                                      |
|-----|-----------------|--------------------------------------|---------------------------------------|---|
| 1.  | Common terminal | Base                                 | Emitter                               | Collector                               |
| 2.  | Input current   | $I_E$                                | $I_B$                                 | $I_B$                                   |
| 3.  | Output current  | $I_C$                                | $I_C$                                 | $I_E$                                   |
| 4.  | Current gain.   | $\alpha = \frac{I_C}{I_E} \approx 1$ | $\beta = \frac{I_C}{I_B} \beta \gg 1$ | $\gamma = \frac{I_E}{I_B} \gamma \gg 1$ |
| 5.  | Input voltage   | $V_{EB}$                             | $V_{BE}$                              | $V_{BC}$                                |
| 6.  | Output voltage  | $V_{CB}$                             | $V_{CE}$                              | $V_{EC}$                                |

| <u>S.N</u> | <u>Parameters</u>                                    | <u>C-B</u>                       | <u>C-E</u>                   | <u>CC</u>           |
|------------|--|----------------------------------|------------------------------|---------------------|
| 7.         | voltage gain   | Medium                           | Medium                       | low                 |
| 8.         | Input resistance very low<br>( $20\text{k}\Omega$ )  | Low ( $1\text{k}\Omega$ )        | High ( $500\text{k}\Omega$ ) |                     |
| 9.         | Output resistance very high<br>( $1\text{M}\Omega$ ) | High<br>( $40\text{k}\Omega$ )   |                              | low ( $50\Omega$ )  |
| 10.        | Applications.  | preamplifier<br>audio amplifiers |                              | Impedance Matching. |

Note : Out of these three configurations, CE is the most popular and widely used configuration, due to the following reasons.

- It has high voltage gain and current gain
- As voltage and current gain are high, therefore it has high power gain.
- CE configuration has moderate values of  $R_i$  and  $R_o$ . Therefore it does not require any additional impedance matching circuits.

### University Questions :

- Q. Explain with proper reason the use of emitter follower (2 Marks) (2015-16)
- Q. Explain the operation of common collector configuration with suitable characteristics in detail (10 Marks) (2014-15)

Unit 2 : BJT and FETContents:

- FET (Field Effect Transistor) Basics
- Construction of JFET
- Operation of JFET.

FET Basics

- FET is a three terminal device — Drain(D), Gate(G), Source(S).
- Applications are similar to that of BJT.

Major differences between BJT and FETFET

1. voltage controlled device. i.e output current ( $I_D$ ) depends on input voltage ( $V_{GS}$ )

2. Unipolar device. i.e conduction is either due to electrons or holes.

BJT

1. Current controlled device. i.e output current  $I_C$  depends on input current  $I_B$ .

2. Bipolar device. i.e conduction is due to both electrons and holes.

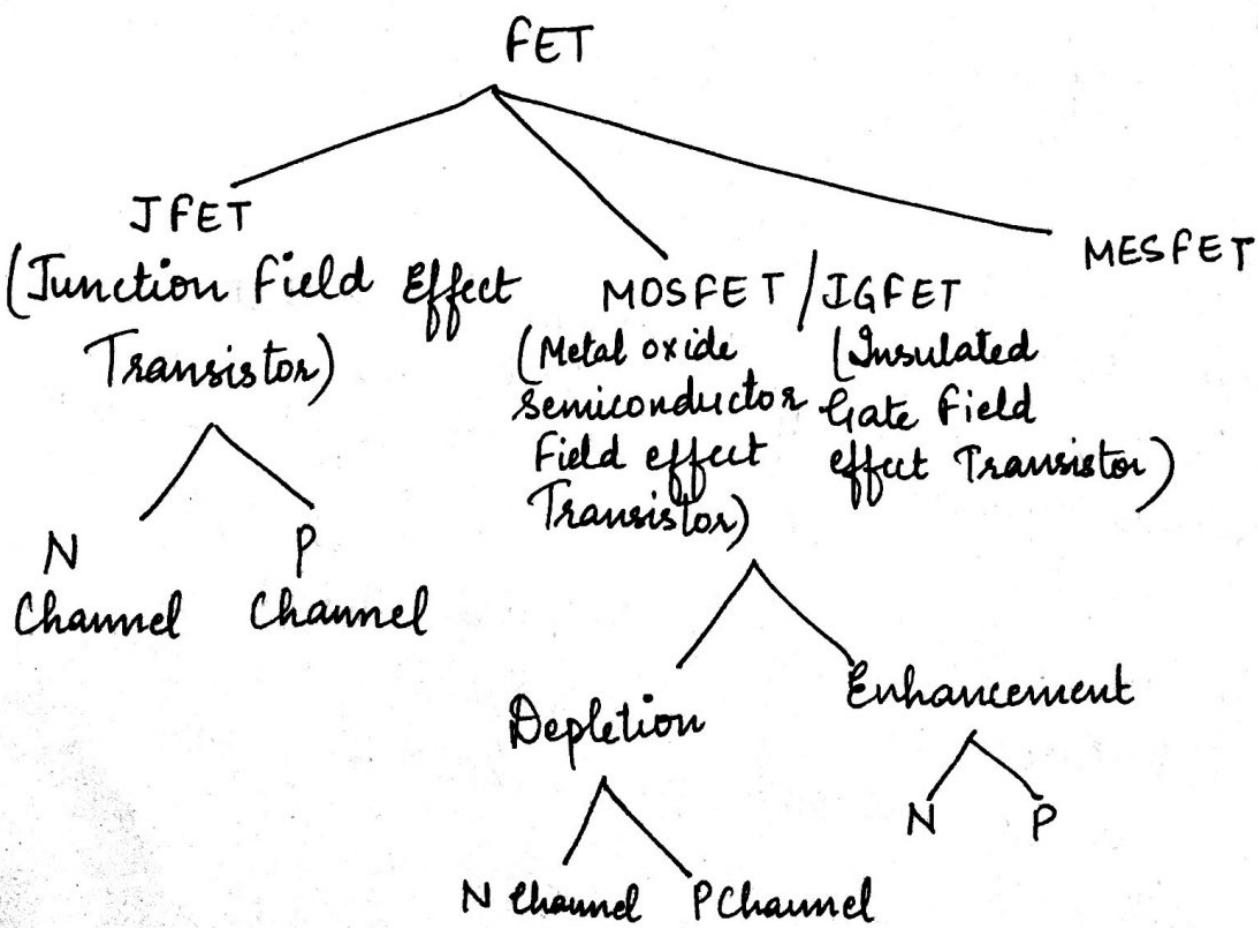
### FET

3. Three terminals  $\rightarrow$  D, S and G
4. High input impedance
5. More temperature stable
6. Small is size
7. less Noisy.

### BJT

3. Three terminals  $\rightarrow$  B, E, C
4. low input impedance
5. less temperature stable.
6. Size is more as compared to that of FET.
7. More Noisy.

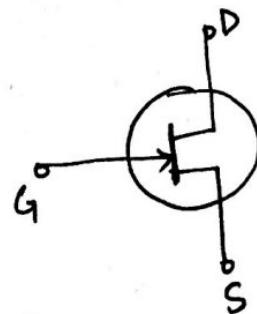
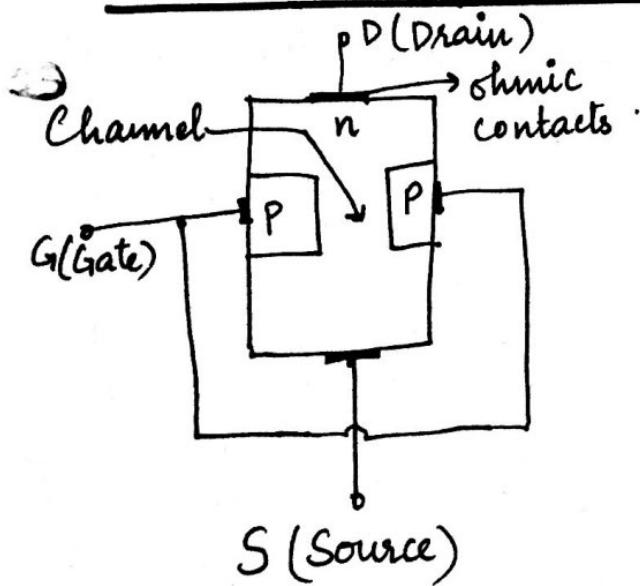
### Types of FET



Q. Why the name field effect?

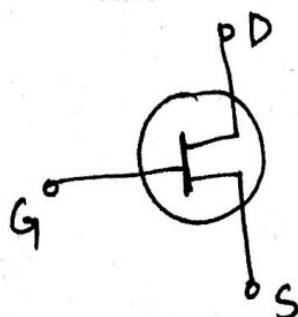
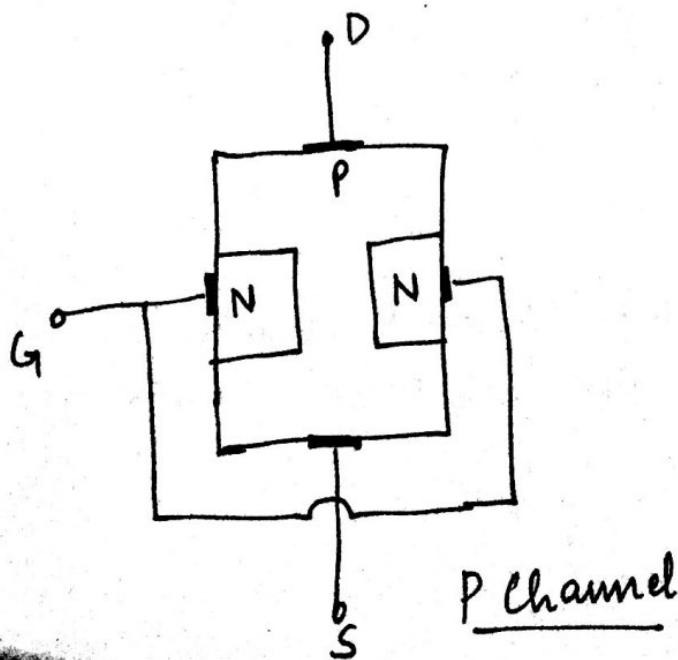
→ The name field effect is derived from the fact that current flow in FET is controlled by the electric field set by an external voltage.

## Construction of JFET



(N channel)

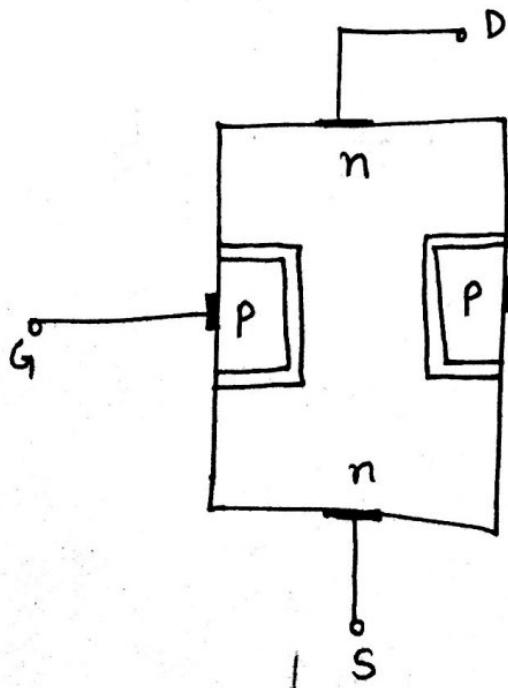
N channel



P Channel

- A semiconductor bar of n type material is taken and ohmic contacts are made to form D, G and S.
- On both sides of bar, heavily doped P regions have been formed by alloying or by diffusion. Both these regions are internally connected.
- The supply voltage is connected between G and S terminals and hence the current  $I_D$  flows from D to S.

### Unbiased JFET



In the absence of any applied potentials, the JFET has two PN junctions under no bias condition.

The result is a depletion region at each junction.

## Operation of JFET

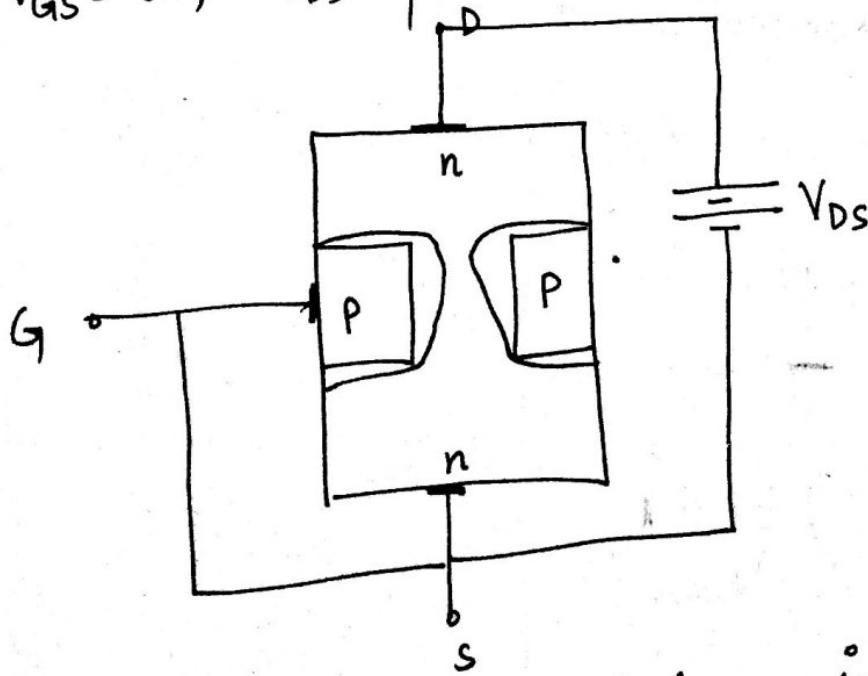
The operation of N channel JFET will be studied for the following three conditions :

→  $V_{GS} = 0\text{ V}$   $V_{DS}$  positive

→  $V_{GS}$  = small negative  $V_{DS}$  positive

→ Negative  $V_{GS}$ ,  $V_{DS}$  positive increases

$V_{GS} = 0\text{ V}$ ,  $V_{DS}$  positive



When  $V_{GS} = 0\text{ V}$ , the electrons in  $n$  type material is attracted towards the positive terminal of  $V_{DS}$  and hence current  $I_D$  flows from D to S.

As  $V_{DS}$  increases, the depletion regions also increase and the channel width decreases.

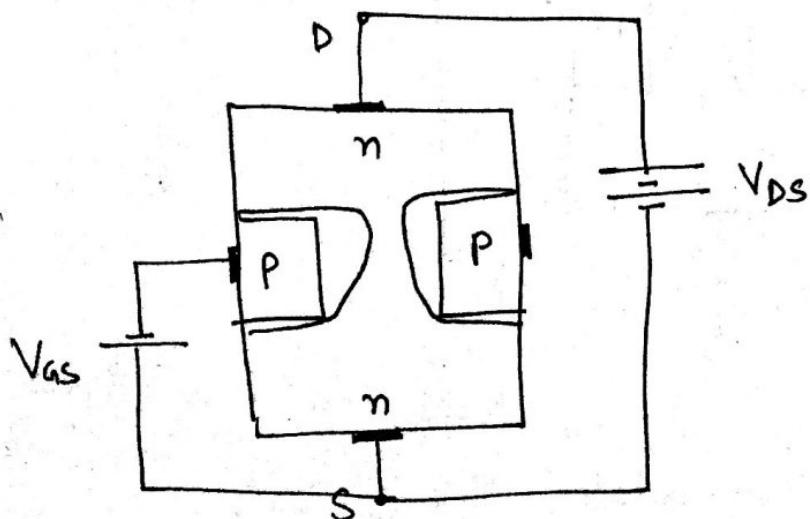
If  $V_{DS}$  is increased to a level, such that depletion regions appear to touch each other, this condition is called pinch off. In this condition, the channel width does not reduce to zero and  $I_D$  becomes constant.

Q. What is pinch off voltage?

→ Pinch off voltage ( $V_p$ ) is defined at  $V_{GS} = 0V$ . It is that value of  $V_{DS}$  for which  $I_D$  becomes constant and is referred to as  $I_{DSS}$ .

Note:  $I_{DSS}$  is maximum current for JFET.

$V_{GS}$  = small negative,  $V_{DS}$  positive.



When negative  $V_{GS}$  is applied, the reverse bias increases and hence the depletion layer increases,

channel width reduces and hence  $I_D$  decreases

$V_{GS}$  = large negative,  $V_{DS}$  positive

When a large negative  $V_{GS}$  is applied, the depletion layer increases further and the channel width reduces to zero and hence  $I_D$  reduces to zero.

This value of  $V_{GS}$  at which drain current  $I_D$  becomes zero is called cut off voltage ( $V_{GS} = V_p$ )

Shockley Equation

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_p} \right)^2$$

University Questions

- Q1. Explain the formation of depletion region  
in JFET (2016-17)

## Unit 2: BJT and FET

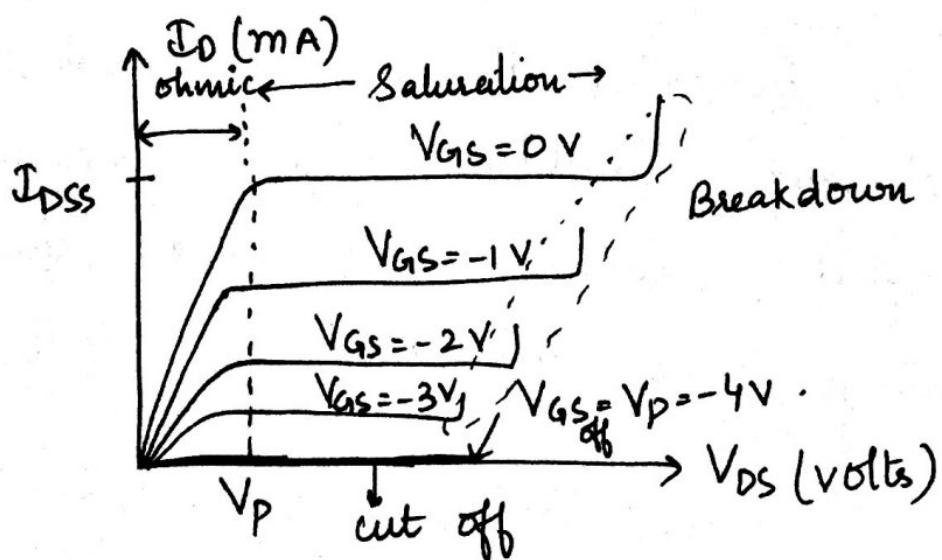
### Contents:

- JFET Characteristics
- Parameters of JFET.

### JFET Characteristics

- Drain characteristics
- Transfer Characteristics.

### Drain characteristics



ohmic region

At small values of  $V_{DS}$ , the resistance remains constant  $I_D$  increases linearly with  $V_{DS}$ . (Ohm's law).

## Saturation region

When  $V_{DS}$  increases above  $V_p$ , the resistance increases, thereby reducing the channel width and  $I_D$  becomes constant. In this region, the resistance is approaching to infinite.

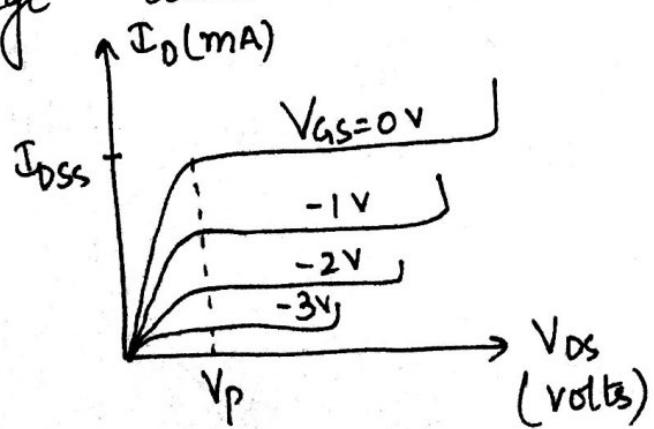
## Cut off Region

When  $V_{GS}$  is made more and more negative, the channel width reduces to zero and hence  $I_D$  also reduces to zero.

## Breakdown Region

When  $V_{DS}$  is increased to a large extent, due down to the gate channel junction breaks down due to avalanche effect and  $I_D$  increases suddenly. It can damage the device.

**Q** <sup>v. important</sup> Explain FET as voltage variable Resistor or voltage controlled Resistor (2017-18)



The region to the left of  $V_p$  is the ohmic region or voltage controlled region. In this region FET act as voltage variable resistor whose resistance is controlled by applied  $V_{GS}$ .

The resistance of FET between D and S for  $V_{DS} < V_p$  increases with increase in negative  $V_{GS}$ .

$$r_d = \frac{r_0}{(1 - V_{GS}/V_p)^2}$$

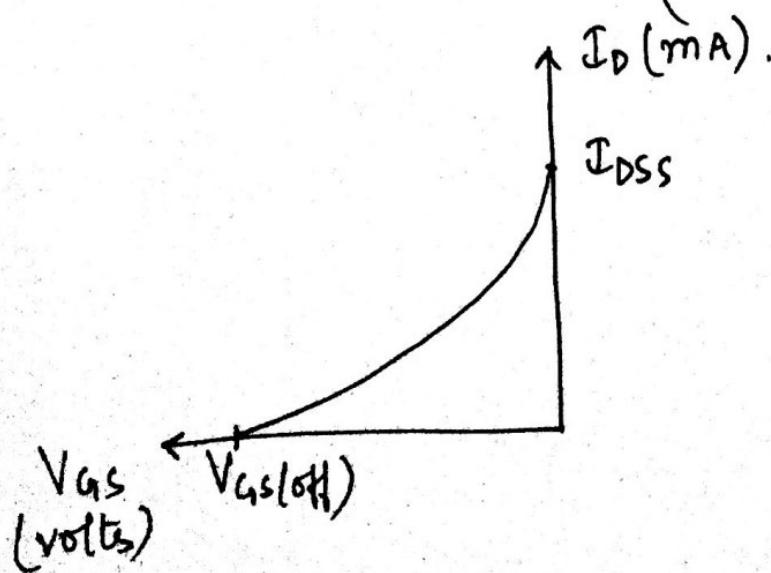
$r_0$  = resistance with  $V_{GS} = 0\text{ V}$

$r_d$  = resistance at a particular level of  $V_{GS}$ .

### Transfer Characteristics (N channel)

$I_D$  and  $V_{GS}$  are related by Shockley's equation

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)^2$$



# University Questions

- Q. Explain FET as voltage variable resistor. (2 Marks)  
(2015-16) (2015-16)  
even odd.
- Q. Describe the VI characteristics of JFET with different operating regions in detail (10 Marks)  
(2014-15)
- Q. Enlist the differences between JFET and BJT (2 Marks) (2013-14).
- Q. Explain the construction and working of N channel JFET. Define pinch off voltage (10 Marks) (2013-14).

## Parameters of JFET

- dynamic Resistance ( $r_d$ )

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$$

- Transconductance ( $g_m$ )

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

## Mathematical expression of $g_m$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Differentiate w.r.t  $V_{GS}$

$$\frac{dI_D}{dV_{GS}} = -\frac{2I_{DSS}}{V_P} \left(1 - \frac{V_{GS}}{V_P}\right)$$

$$g_m = -\frac{2I_{DSS}}{V_P} \left(1 - \frac{V_{GS}}{V_P}\right)$$

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_P}\right) \quad \text{where } g_{m0} = -\frac{2I_{DSS}}{V_P}$$

unit of  $g_m$  = mho or S

• Amplification factor ( $\mu$ )

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

$$\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\mu = r_d \times g_m$$

## Unit 2: BJT and FET

### Contents

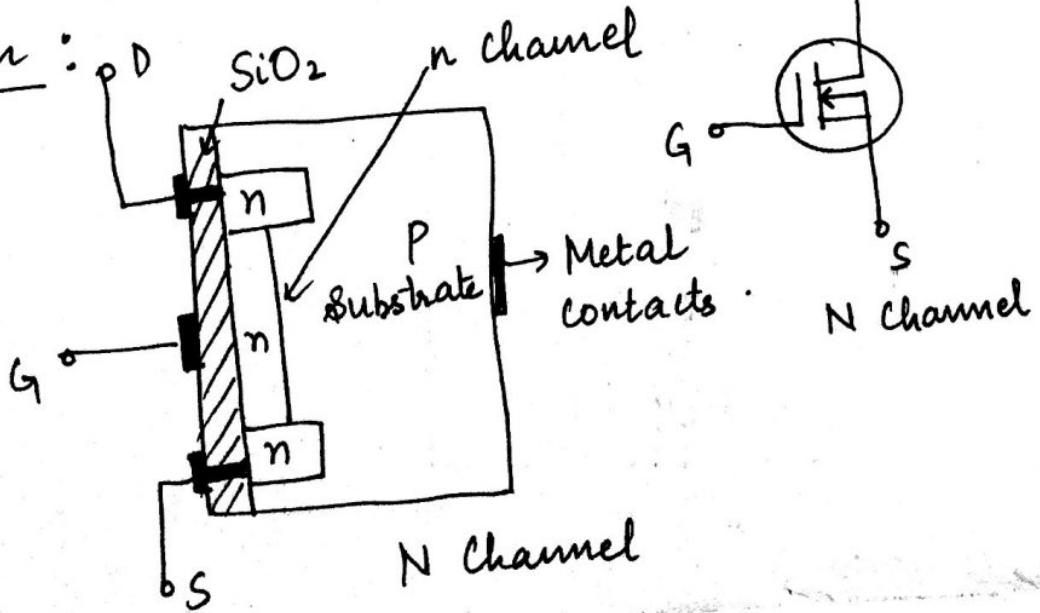
- MOSFET Basics.
- Depletion Type : Construction, operation.
- Characteristics of Depletion MOSFET.

### MOSFET Basics

- Input impedance of MOSFET is higher than that of BJT and JFET.
- Most widely used in digital computers.
- Two Types: Depletion and Enhancement.

### Depletion Type MOSFET

Construction :



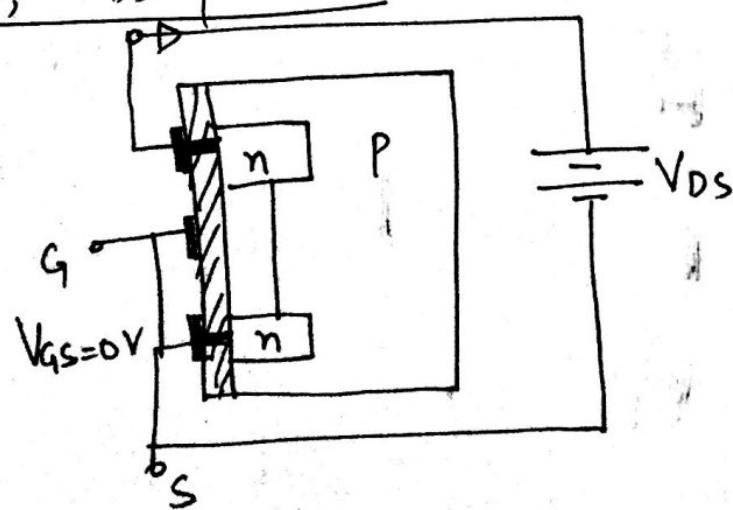
- A P type of semiconductor material is used as substrate.
- The drain and source terminals are connected to n type regions through metallic contacts.
- The n type regions are linked to each other by a n channel.
- The gate terminal is insulated from n channel by a thin  $\text{SiO}_2$  layer. This  $\text{SiO}_2$  layer increases the input impedance of MOSFET due to which  $I_G = 0$ .

### operation (N channel Depletion MOSFET)

The operation of N channel Depletion MOSFET is studied for the following conditions.

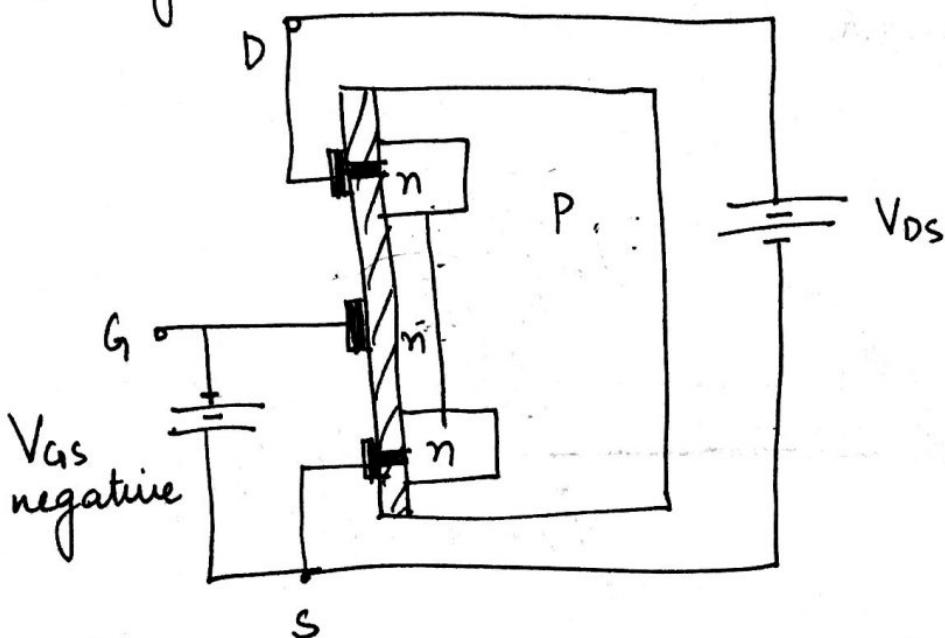
- $V_{GS} = 0V$ ,  $V_{DS}$  positive
- $V_{GS}$  = negative,  $V_{DS}$  positive
- $V_{GS}$  = positive,  $V_{DS}$  positive.

$V_{GS} = 0V$ ,  $V_{DS}$  positive



when  $V_{GS} = 0V$  is applied, the electrons travel from source to drain due to the effect of positive  $V_{DS}$  and hence  $I_D$  flows from drain to source.  $I_D$  is referred as  $I_{DSS}$  at  $V_{GS} = 0V$ .

$V_{GS}$  negative,  $V_{DS}$  positive



When negative  $V_{GS}$  is applied, electrons in n channel are repelled towards p substrate and holes from p substrate are attracted. This will reduce the channel and hence  $I_D$  decreases.

$V_{GS}$  positive,  $V_{DS}$  positive

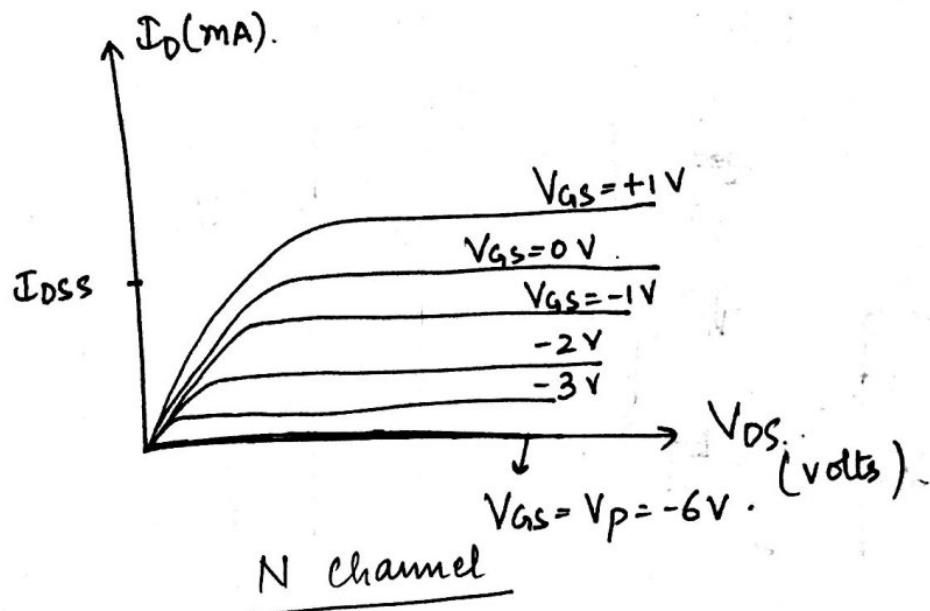
When positive  $V_{GS}$  is applied, electrons in n channel are attracted and also the minority

electrons in P type substrate are attracted towards the positive terminal of the  $V_{GS}$ . Hence the channel width increases. Therefore

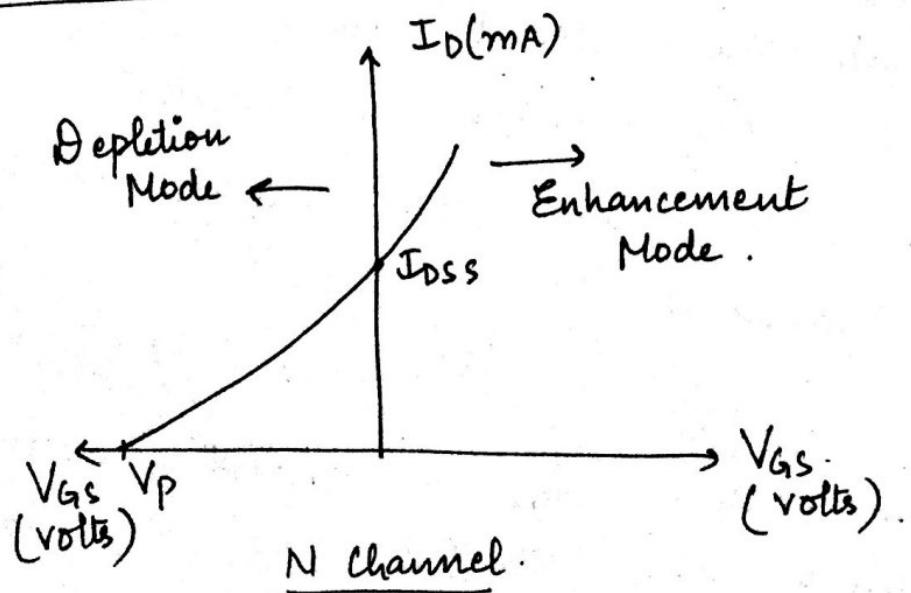
$$I_D \text{ increases. } I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

## Characteristics of Depletion MOSFET

- Drain Characteristics



- Transfer Characteristics



Draw the drain and transfer characteristics of P Channel depletion MOSFET.

Note: Depletion MOSFET is called normally 'ON' MOSFET at  $V_{GS} = 0\text{ V}$ ,  $I_D = I_{DSS}$ .

### University Questions

- Q. Explain the construction, working and characteristics of Depletion type MOSFET.  
● (5 Marks) (2015-16).
- Q. Draw the circuit of n channel depletion type MOSFET & explain its operation. Also draw its drain and transfer characteristics. (2017-18)(even sem)  
● (7 Marks),

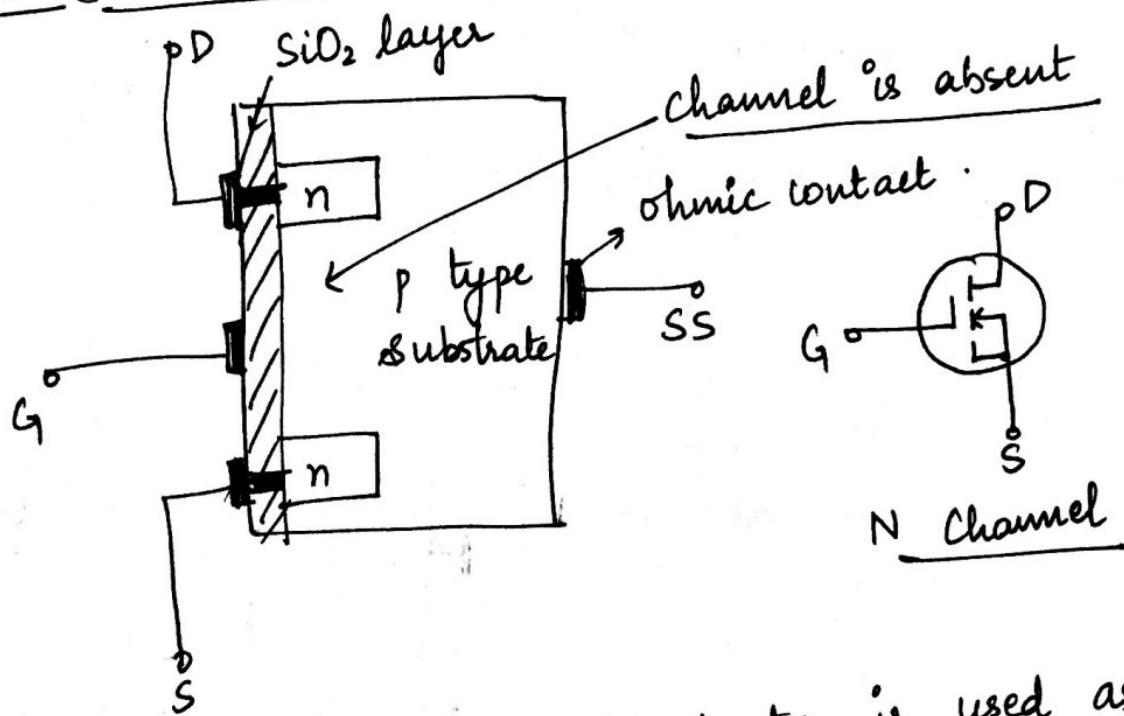
## Unit 2 : BJT and FET

### Contents :

- Enhancement Type MOSFET : construction, operation
- Characteristics of Enhancement MOSFET.

### Enhancement Type MOSFET.

#### Construction (N channel)



- A piece of P type Semiconductor is used as substrate.
- The drain and source terminals are connected to n type doped regions through the metallic contacts.
- Channel is absent here

- Gate is insulated from the channel by  $\text{SiO}_2$  layer.

## Operation of Enhancement MOSFET (n channel).

The operation of n channel enhancement MOSFET will be studied for the following three conditions:

→  $V_{GS} = 0 \text{ V}$ ,  $V_{DS}$  positive

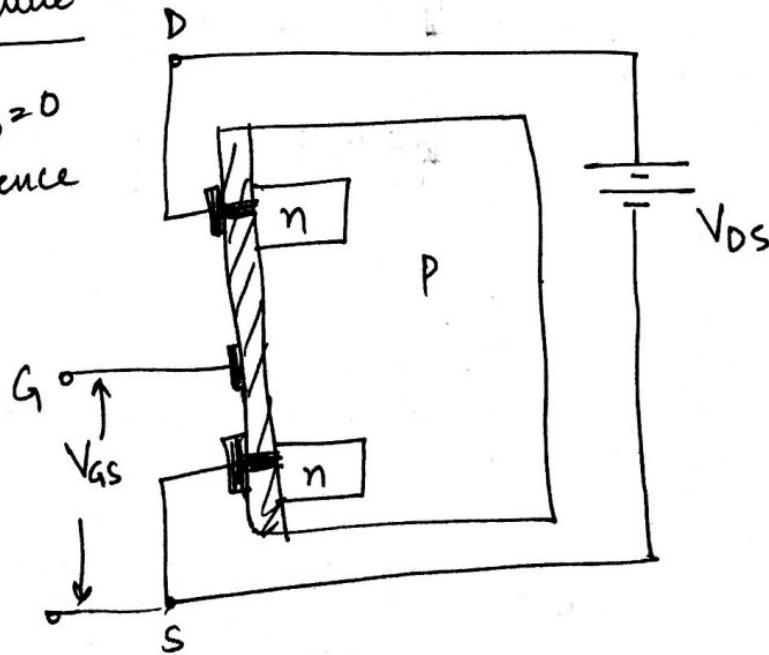
→  $V_{GS}$  = negative,  $V_{DS}$  positive

→  $V_{GS}$  = positive,  $V_{DS}$  positive

$V_{GS} = 0 \text{ V}$ ,  $V_{DS}$  positive

When  $V_{GS} = 0 \text{ V}$ ,  $I_D = 0$

due to the absence  
of channel.



$V_{GS} = \text{negative}$ ,  $V_{DS}$  positive

When negative  $V_{GS}$  is applied, holes of P substrate are attracted towards the gate. Hence  $I_D = 0$  due to absence of channel made of

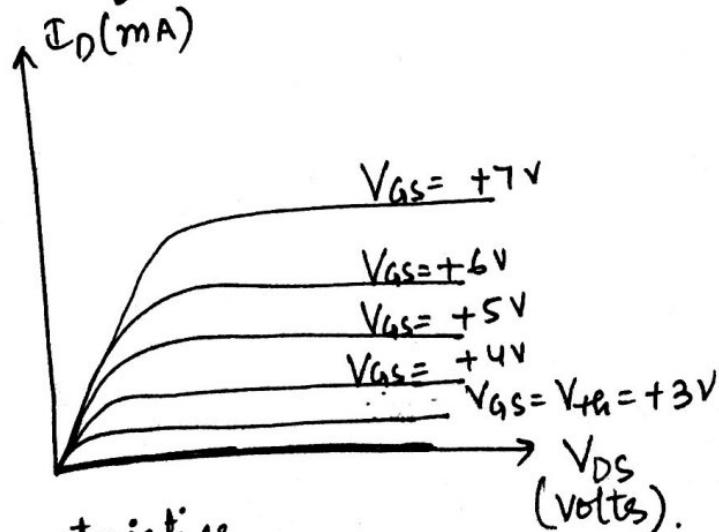
electrons.

$V_{GS}$  = positive,  $V_{DS}$  positive

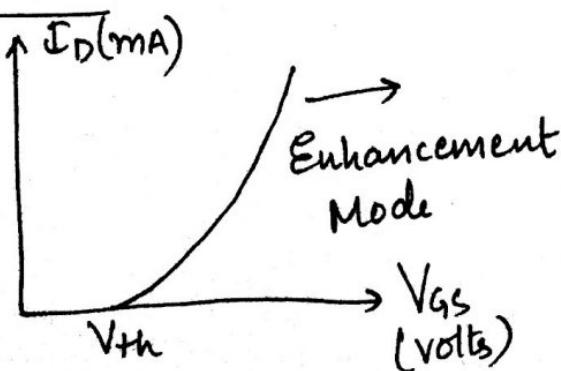
- When positive  $V_{GS}$  is applied, electrons from P type substrate are attracted towards the gate. As we keep on increasing positive  $V_{GS}$ , a point comes when sufficient number of electrons are attracted towards the gate to form the channel. This value of  $V_{GS}$  at which channel is induced starts flowing.
- threshold voltage ( $V_{th}$ ) and  $I_D$
- $$I_D = k(V_{GS} - V_{th})^2$$

### Characteristics of Enhancement MOSFET

- Drain Characteristics



- Transfer Characteristics



Q Draw the characteristics of P channel Enhancement MOSFET.

Note: Enhancement MOSFET is called normally 'OFF' MOSFET because at  $V_{GS} = 0V$ ,  $I_D = 0$ .

### University Questions

Q. Explain -the construction, working and characteristics of P channel Enhancement MOSFET (5 Marks)  
(2015-16)