UNIT-4

DAQ

Definition and Concept

* An instrumentation or Data Acquisition System is an assembly of devices united by some form of regular interaction of an interdependence.

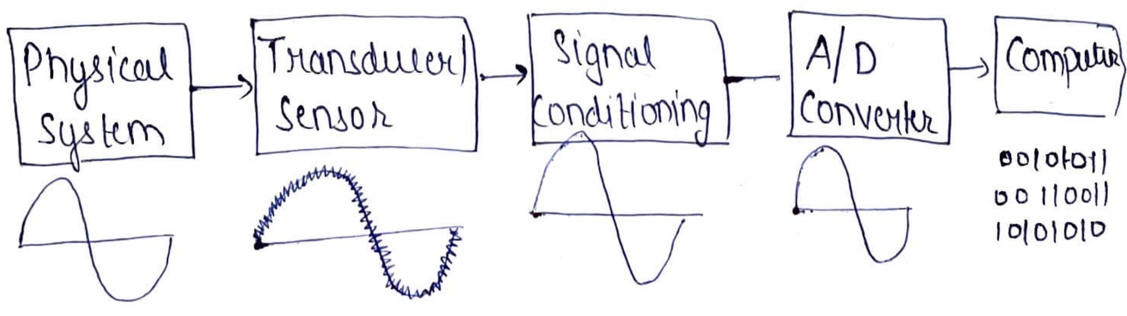
* It is a group of diverse units or devices so combined by nature or by an art to form in integral part and to function, operate or move in unison (given strategy) and often in obedience to some form of control system.

* A DAQ is a collection of diverse sensors and devices connected in a manner such that it produces a usable output which further can be utilized to control a process of a system for being a part of an instrumentation

* The system is meant for data measurement, control and monitoring

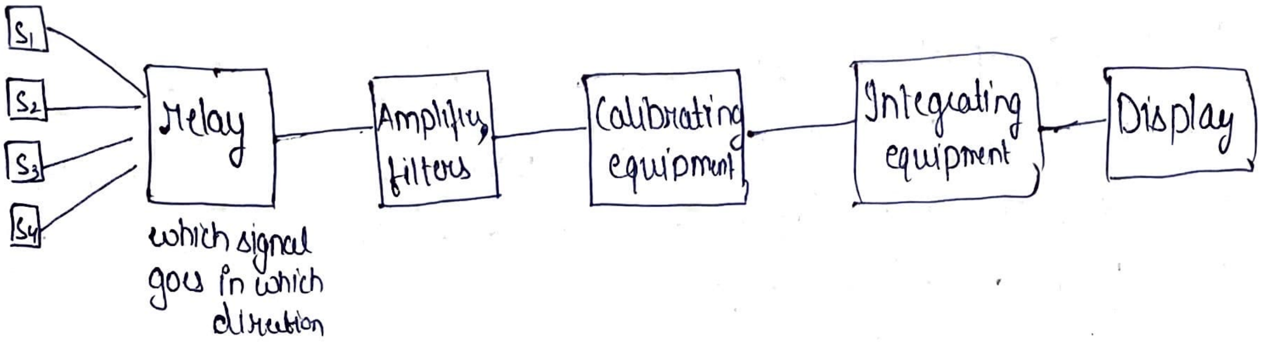
* Can be classified as

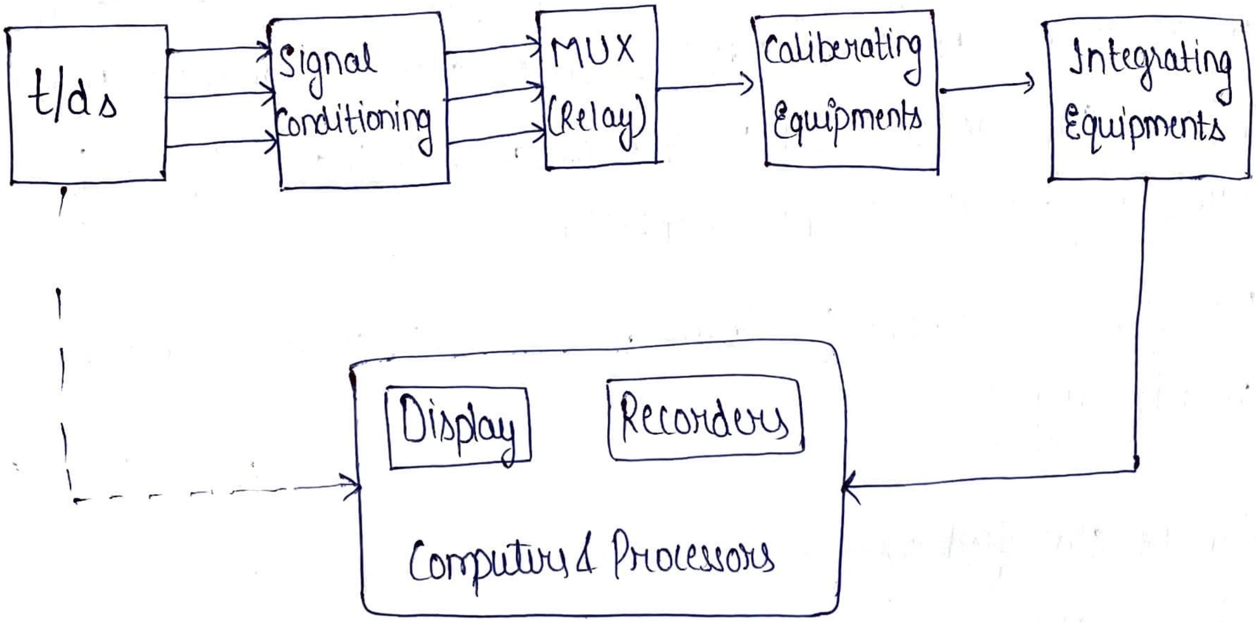
1. Analog DAQ
2. Digital DAQ



Analog DAQ

* These systems deals with the information in analog form





General Architecture of Analog DAQ

Componets

1. Transducers
2. Signal Condiotioning
3. Relays
4. Calibrating Equipment
5. Integrating Equipment
6. Displays & Recorders.

Transducers: To convert physical parameters to electric signals

Signal Conditioning: It is for amplifying, refining or selecting certain portions of these signals.

Relays: for scanning different signal sources

Visual displays: Devices for continuous monitoring of the signal

Graphic Recorder: for obtaining permanent records of input data

Magnetic Recorder: for preserving and reproducing data.

Objectives of Data Acquisition System

1. It must acquire the necessary data, at correct speed and at the correct time.
2. Use of all data efficiently to inform the operator about the state of the system.
3. It must monitor the complete plant operation to maintain on-line optimum and safe operations.

4. It must provide an effective human communication system and be able to identify problem areas, thereby minimizing unit availability and maximizing unit through point at minimum cost.
5. It must be able to collect, summarize and store data for diagnosis of operation and record purpose.
6. It must be able to compute unit performance indices using online, real-time data.
7. It must be flexible and capable of being expanded for future require
8. It must be reliable and not have a down time greater than 0.1 %.

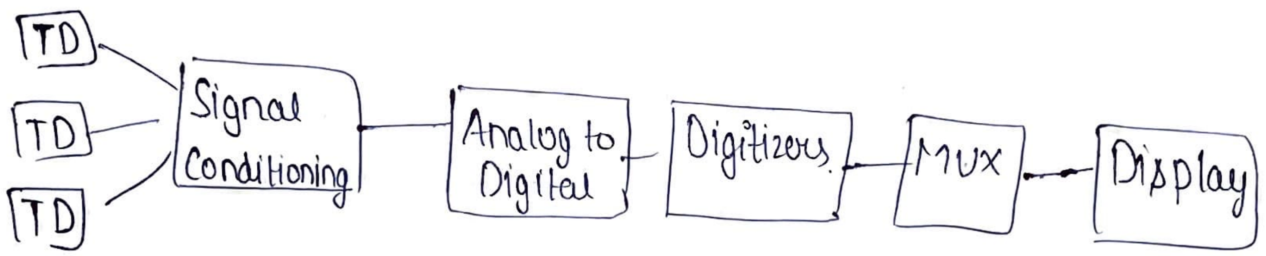
Physical System/Conditions

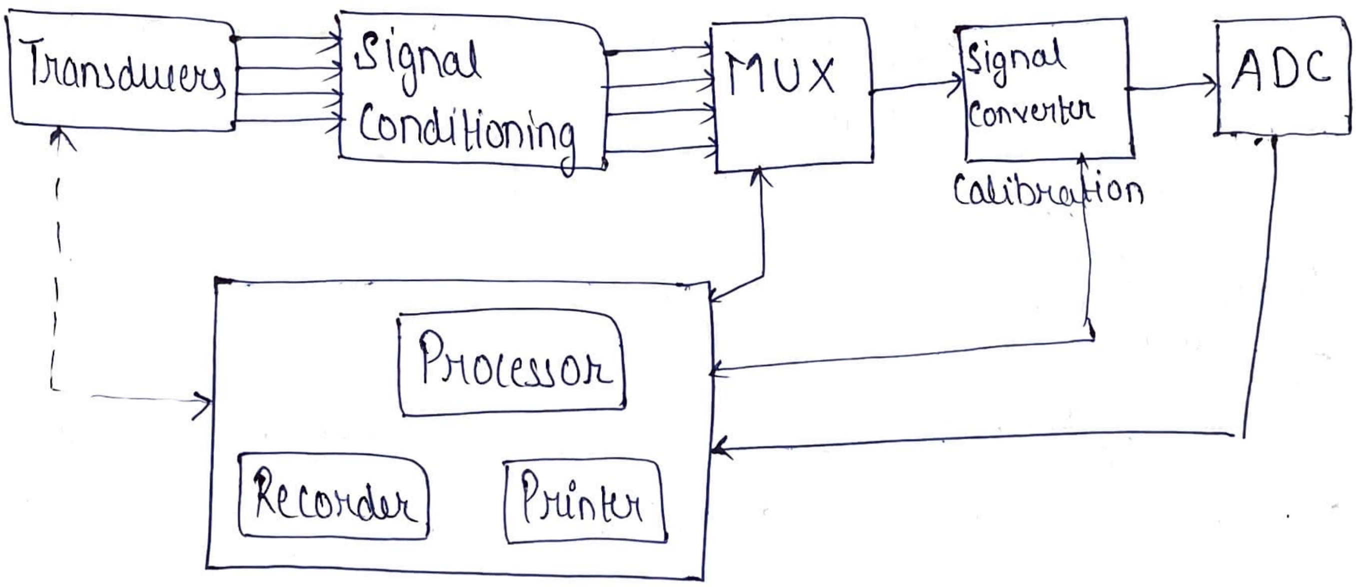
Physical condition that can be used as input of DAS or which can be represented in Digital form are as under.....

- → Temperature
- → Pressure
- → Light
- → Force
- → Displacement
- → level
- → Electric signals
- → ON/OFF switch

Digital DAQ

* These systems deals with the information in analog form
* Most of the transducers produces output in analog form.
* ADC are used for converting them in to discrete data





Components

1. Transducers
2. Signal Conditioning
3. MUX / DeMUX
4. Signal Converters:
5. ADCs:
6. Display & Recorders!

1. Transducer - It converts physical quantities in to electric signals

2. Signal Conditioner - It performs the functions like amplification and selection of desired portion of the Signal.

3. Multiplexer - Connects one of the multiple inputs to output. So, it acts as parallel to serial converter.

4. Analog to Digital Converter - It converts the analog input in to its equivalent digital output.

5. Display device: It display the data in digital format.

6. Digital Recorder: It is used to record the data in digital format.

Analog / Digital

Analog systems are used when wide bandwidth is required or when lower accuracy can be allowed.

Digital systems are used when the physical process being monitored slowly varies and when high accuracy and low per channel cost is required.

Analog and Digital IO

Input Conditioning Equipments

(i) Amplifiers & filters → Several type of amplifiers are used in data acquisition systems. Mainly the use of amplification in DAS is to amplify or de-amplify the signal coming from the transducer as per the levels of the instruments used in the system.

Filters are used for signal conditioning of the signals coming from the amplifier. Certain low and high pass filters are used as per the requirement of DAS.

(ii) Multiplexers and De-multiplexers → These components are used for the sharing of the signal coming from various transducers after its conditioning and to provide signal and control signals to them respectively for the uninterrupted functioning of the system.

(iii) ADC & DAC → In order to convert the signals as per the need of the connected instruments, ADC and DAC are used. The main aim of these converter is to digitize & linearize the data for the subsequent operations.

Counters and Timers

A counter is a sequential logic device which stores (and sometimes displays) the number of times a particular event or process has occured, often in relationship to a clock signal.

The basic elements in the counters are flip-flop which are able to store one bit of data.

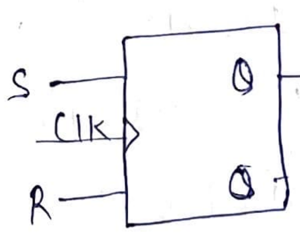
The counters can be designed up to the max. value according to the no of bits as well as upto the required no.

There are several type of flip-flops that can be used to design the counters such as D-flipflop, SR flipflop, JK flipflop, T flipflop.

* For n-flip-flops - there are 2^n possible states
* For 3-flip-flops → there are 8 possible states which are (0-7)

SR → D flipflop

JK → T flipflop



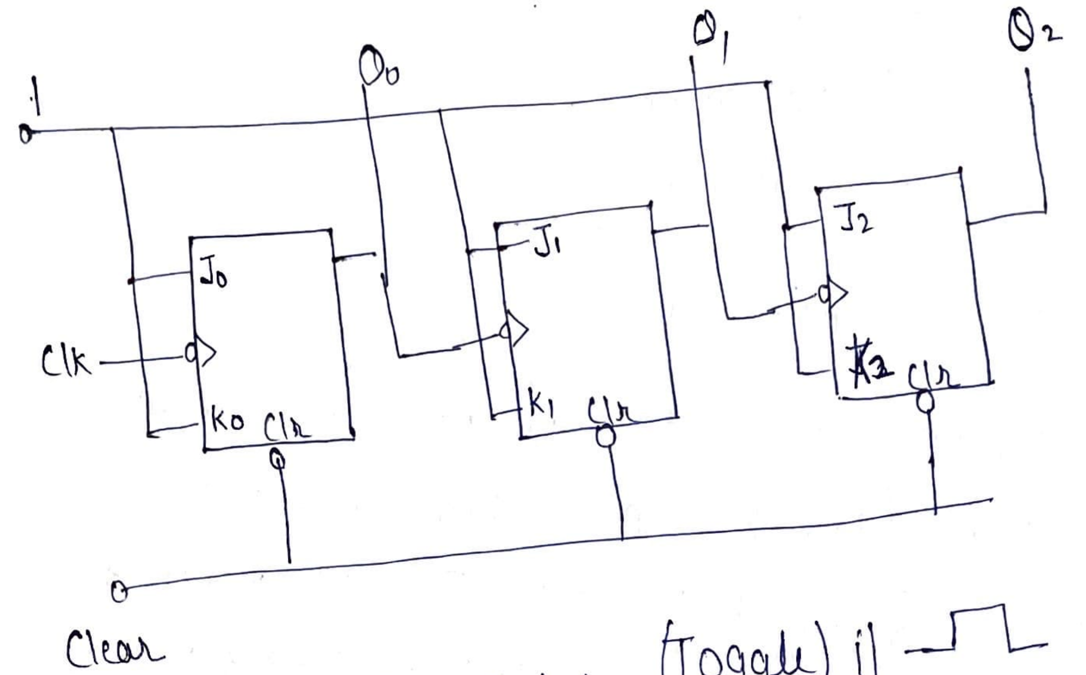
$Q = f(S, R)$

$\bar{Q} =$

At time 't' $Q(t) = [f\ S, R, Q(t_0)]$ → initial state

Sequential Logic Circuit

* 3 flip flop means 3-bit data i.e 000 - 111



$Q \rightarrow$ 0 to 1 (Toggle) if
1 to 0

T	Clk	$Q_2\ Q_1\ Q_0$
1	0	0 0 0
1	1	0 0 1
1	2	0 1 0
1	3	0 1 1
1	4	1 0 0
1	5	1 0 1
1	6	1 1 0
1	7	1 1 1

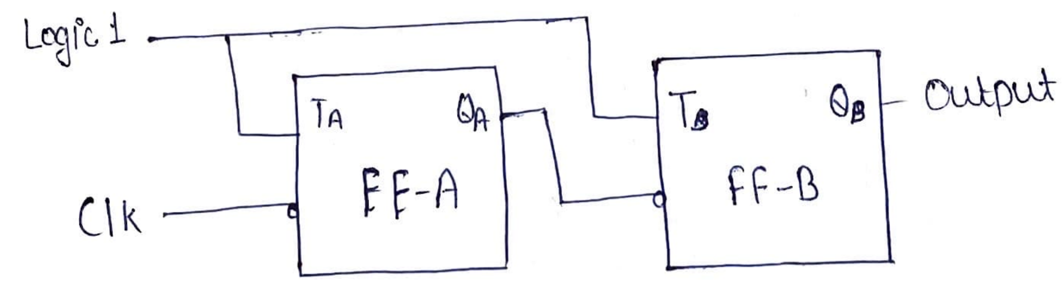
Types of Counters

1. Ripple or Asynchronous Counters
2. Synchronous Counters
   - up/down
   - Modulus

Asynchronous or ripple counters

The logic diagram of a 2-bit ripple up counter is given below. The toggle (T) flip-flop are being used. But we can use the JK flip-flop also with J and K connected permanently to logic 1. External clock is applied to the clock input of flip-flop A and Q_A output is applied to the clock input of the next flip-flop i.e FF-B

Logical Diagram



Operation

S.No.	Condition	Operation
1.	Initially let both the FFs be in the reset state	$Q_B Q_A = 00$ initially
2.	After 1st negative clock edge	As soon as the first negative clock edge is applied, FF-A will toggle and Q_A will be equal to 1.

Q_A is connected to clock input of FF-B. Since Q_A has changed from 0 to 1, it is treated as the positive clock edge by FF-B. There is no change in Q_B because FF-B is a negative edge triggered FF.

$Q_B Q_A = 01$ after the first clock pulse.

3. After 2nd negative clock edge

On the arrival of second negative clock edge, FF-A toggles again and $Q_A = 0$. The change in Q_A acts as a negative clock edge for FF-B. So it will also toggle and Q_B will be 1.

$Q_B Q_A = 10$ after the second clock pulse.

4. After 3rd negative clock edge

On the arrival of 3rd negative clock edge, FF-A toggles again and Q_A become 1 from 0. Since this is a positive going change, FF-B does not respond to it and remains inactive. So Q_B does not change and continues to be equal to 1.

$Q_B Q_A = 11$ after the third clock pulse.

5. After 4th negative clock edge

On the arrival of 4th negative clock edge, FF-A toggles again and Q_A becomes 1 from 0. This negative change in Q_A acts as clock pulse for FF-B. Hence it toggles to change Q_B from 1 to 0.

$Q_B Q_A = 00$ after the fourth clock pulse.

Truth Table

Clock	Counter Output Q_B	Counter Output Q_A	State Number	Decimal Counter Output
Initially	0	0	–	0
1st	0	1	1	1
2nd	1	0	2	2
3rd	1	1	3	3
4th	0	0	4	0

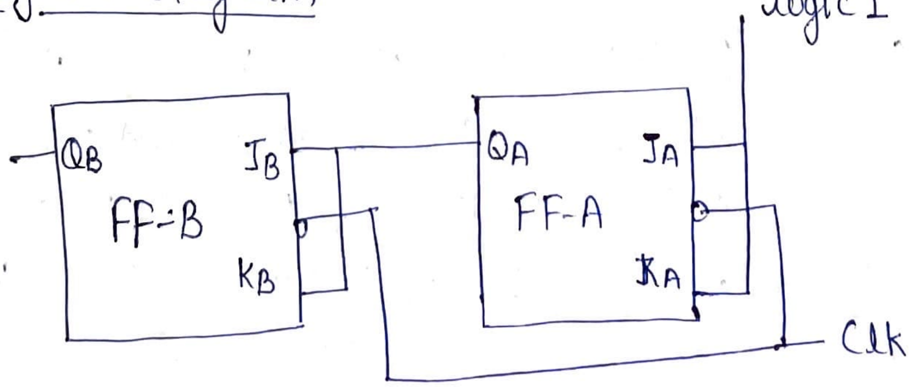
Synchronous Counters

If the "clock" pulses are applied to all the flip-flop in a counter simultaneously, then such a counter is called as synchronous counter.

2-bit Synchronous up Counter

The J_A and K_A inputs of FF-A are tied to logic 1. So FF-A will work as a toggle flip-flop. The J_B and K_B inputs are connected to Q_A.

Logical Diagram



Operation

S.No	Condition	Operation
1.	Initially let both the FFs be in the reset state	$Q_B Q_A = 00$ initially
2.	After 1st negative clock edge	As soon as the first negative clock edge is applied, FF-A will toggle and Q_A will change from 0 to 1. But at the instant of application of negative clock edge, Q_A, $J_B = K_B = 0$. Hence FF-B will not change its state. So Q_B will remain 0. $Q_B Q_A = 01$ after the first clock pulse.
3.	After 2nd negative clock edge	On the arrival of second negative clock edge, FF-A toggles again and Q_A changes from 1 to 0. But at this instant Q_A was 1. So $J_B = K_B = 1$ and FF-B will toggle. Hence Q_B changes from 0 and 1. $Q_B Q_A = 10$ after the second clock pulse.
4.	After 3rd negative clock edge	On application of the third falling clock edge, FF-A will toggle from 0 to 1 but there is no change of state for FF-B. $Q_B Q_A = 11$ after the third clock pulse.
5.	After 4th negative clock edge	On application of the next clock pulse Q_A will change from 1 to 0 as Q_B will also change from 1 to 0. $Q_B Q_A = 00$ after the fourth clock pulse

UP/DOWN Counter

Up Counter and down counter is combined together to obtain an UP/Down counter. A mode control (M) input is also provided to select either up or down mode. A combinational circuit is required to be designed and used between each pair of flip-flop in order to achieve the up/down operation.

Modulus Counter (MOD-N Counter)

The 2-bit ripple counter as MOD-4 counter and 3-bit ripple counter is called as MOD-8 counter. So in general, an ~~[illegible]~~ n-bit ripple counter is called as modulo-N counter. where MOD number $= 2^n$.

Types of modulus

- 2-bit up or down (MOD-4)
- 3-bit up or down (MOD-8)
- 4-bit up or down (MOD-16)

Timers - A timer is a specialized type of clock used for measuring specific time intervals. Most of the digital system require some kind of timing waveform (e.g. a source of trigger pulses). In digital systems a rectangular waveform is most desirable. These generators of rectangular waveform are called as multivibrators.

They are classified as

* Astable (free-running)
* Monostable
* Bistable

Astable Multivibrator

It is known as free runing multivibrator. It is also called as square wave generator. The circuit has two quasi-stable states (no stable state). Thus three is an oscillation between two state and no external signals are required to produce change in state. Astable circuits are used to generate square wave. for example clock generators in digital system.

Monostable Multivibrator

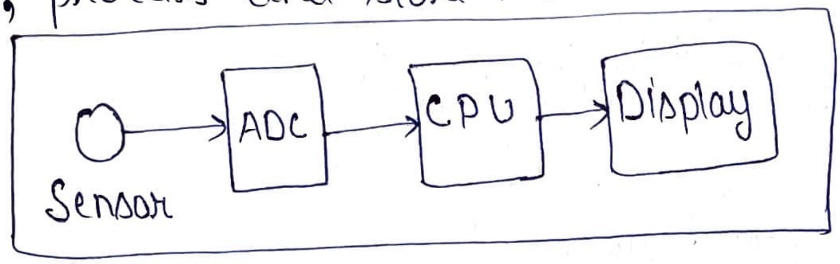
The monostable or one-shot multivibrator generates a signal pulse of specified duration to each external trigger. As its name implies only one stable state exist. Applications of each trigger causes a change to the quasi stable state. The circuit remains in the quasi stable state for a fixed internal of time and then revert to its original stable state. In fact an internal trigger signal is generated which produces the transition to the stable state. Usually the charging and discharging of capacitor provide this internal trigger signal.

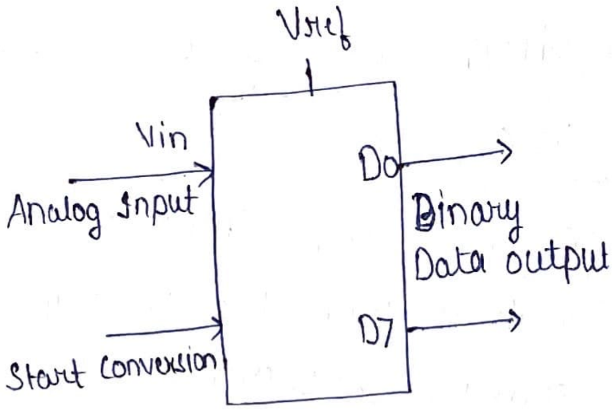
Bistable Multivibrator

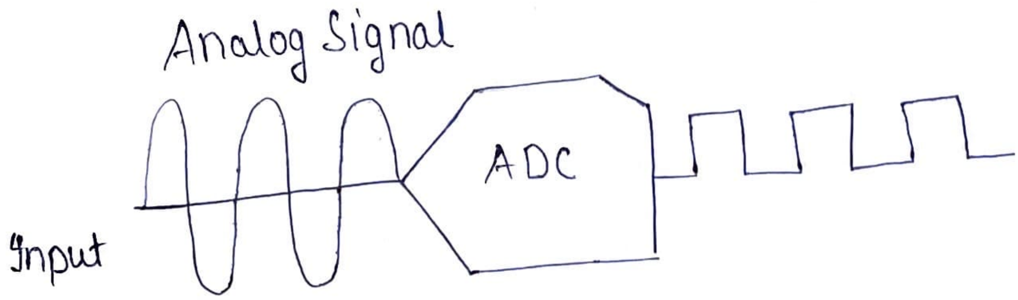
It is called as bistable latch of flip-flops. Schmitt trigger is another bistable circuit important property of a bistable multivibrator is that it maintains a given output voltage level unless an external signal is applied. Application of external signal causes a change of state and this o/p level is maintained indefinitely until a second trigger is applied. Thus a bistable multivibrator requires two external trigger before it returns to its initial state.

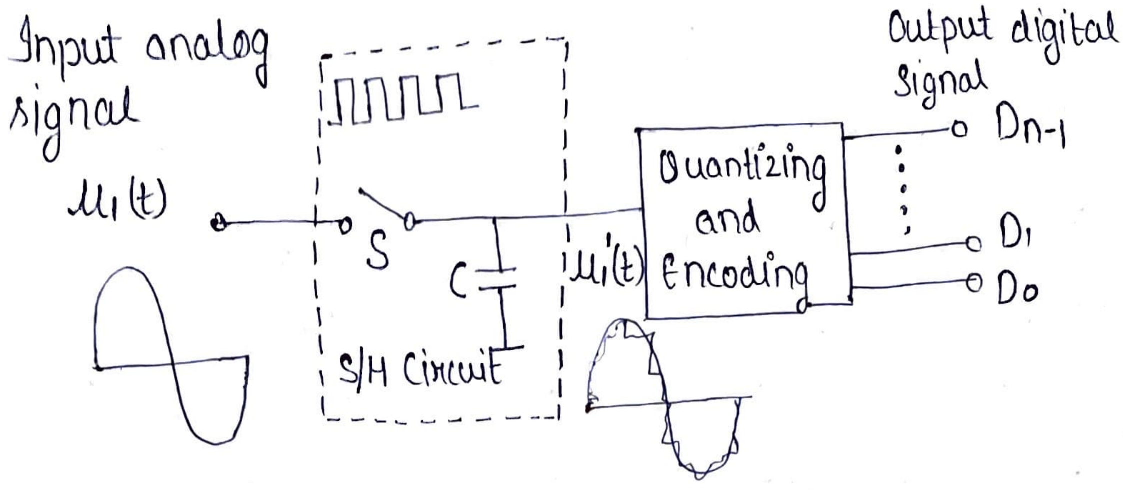
Analog To Digital Converter (ADC)

ADCs are used for data acquisition. Digital Computers use binary (discrete) values, physical world is analog (continuous). Physical quantities dealt in every day life are temperature, heat, light, pressure (wind or liquid), humidity, flow rate and velocity. A physical quantity is converted to electrical (voltage, current) signals using a device called a transducer (sensor). ADC are required to convert real world physical quantities in to digital numbers so that microcontrollers (computers) can read, process and store them.







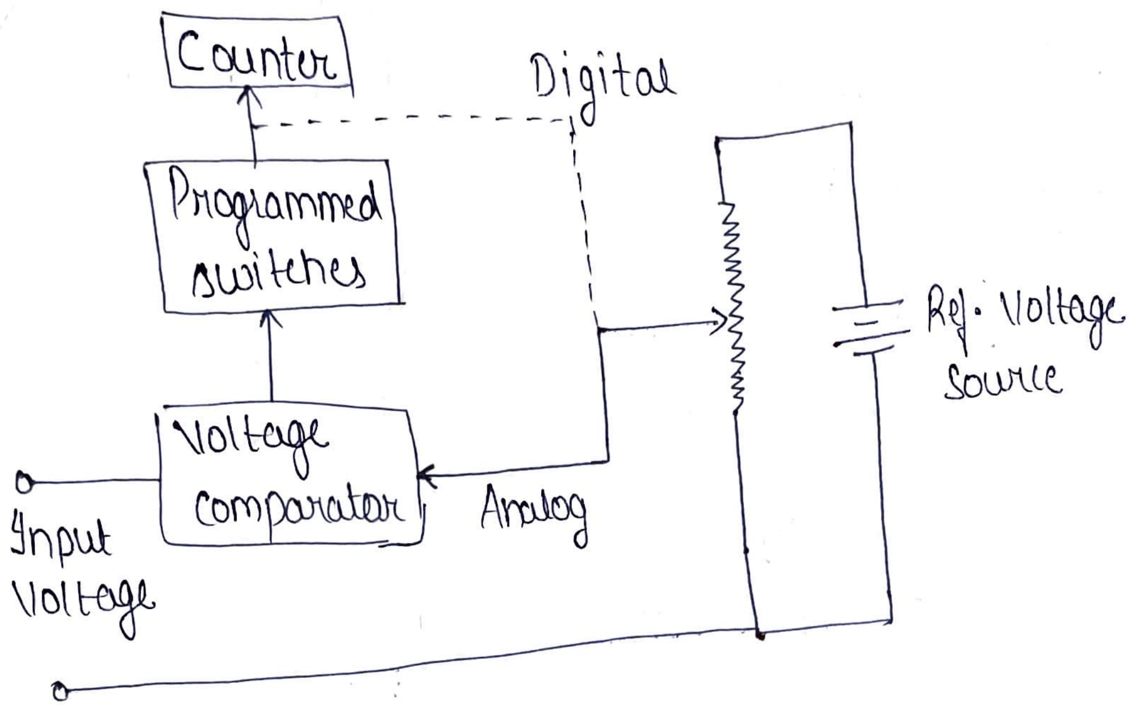


Input
↓
S/H Circuit
↓
$\boxed{\text{Quantizing}}$ (rounding off)
↓
Digitization (Encoding)

<u>Successive Approximation ADC</u> → It is also known as Potentiometric type ADC

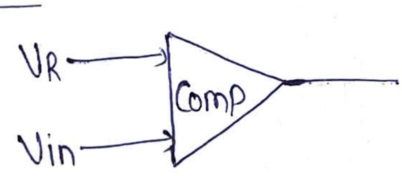
<u>Potentiometric type ADC</u>

It contains voltage divider network with coarse and fine steps. The divider network is connected through electronic switches to a voltage comperator which compares an internal voltage provided by a reference source with an unknown voltage.



Principle: It works on the principle of successive approximation. It compares analog input to a Decade assembly counter reference voltage which is repeatedly divided in to half.

Comparater



$V_R > V_{in}$

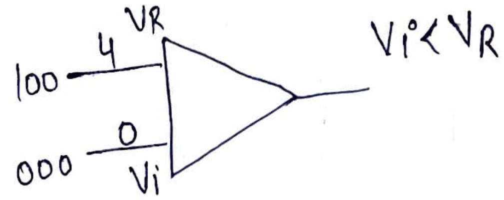
$V_R < V_{in}$

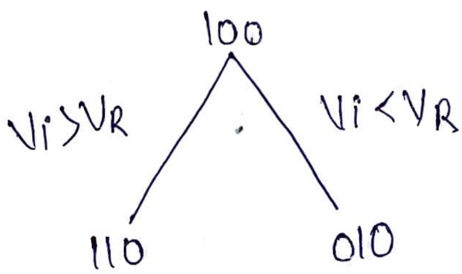
$V_R = V_{in}$

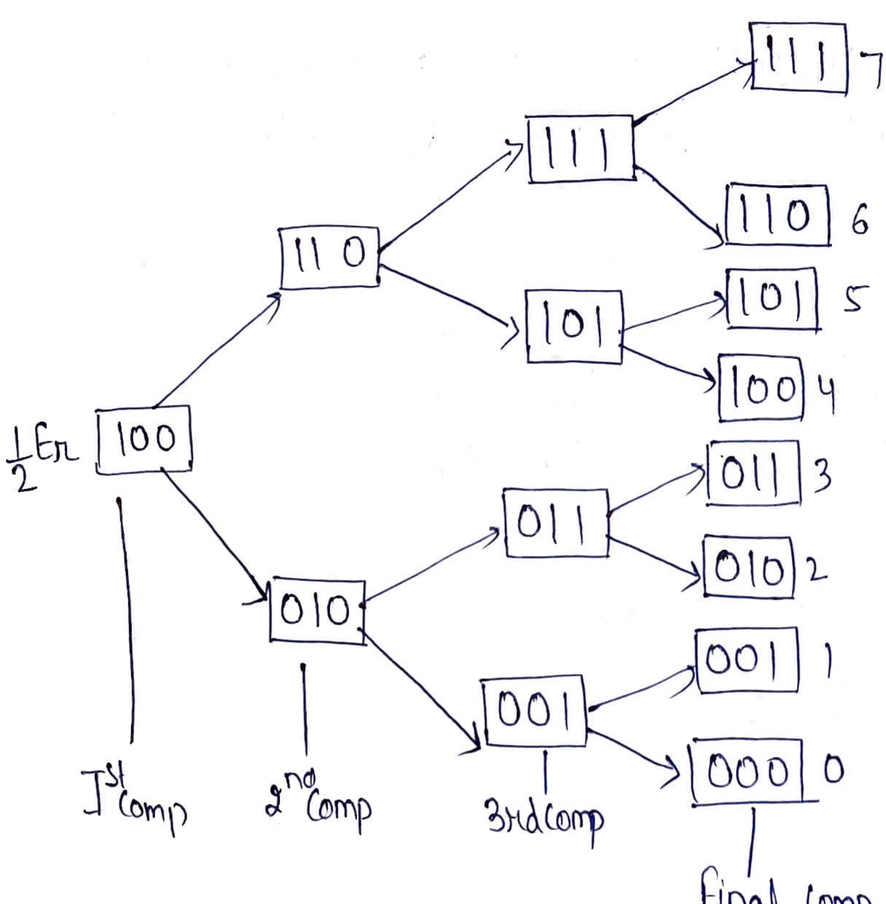
Here V_R → Reference voltage (potentiometer)

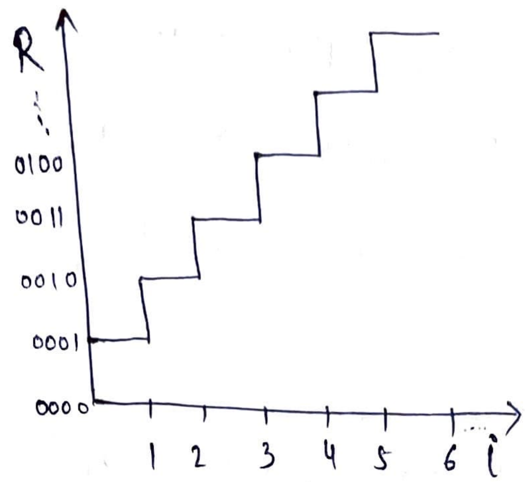
V_{in} → Input voltage

Consider a four digit binary voltage 1000, In the first comparison, it is divided in to its half and correspondingly Er is also halfed i.e Er/2









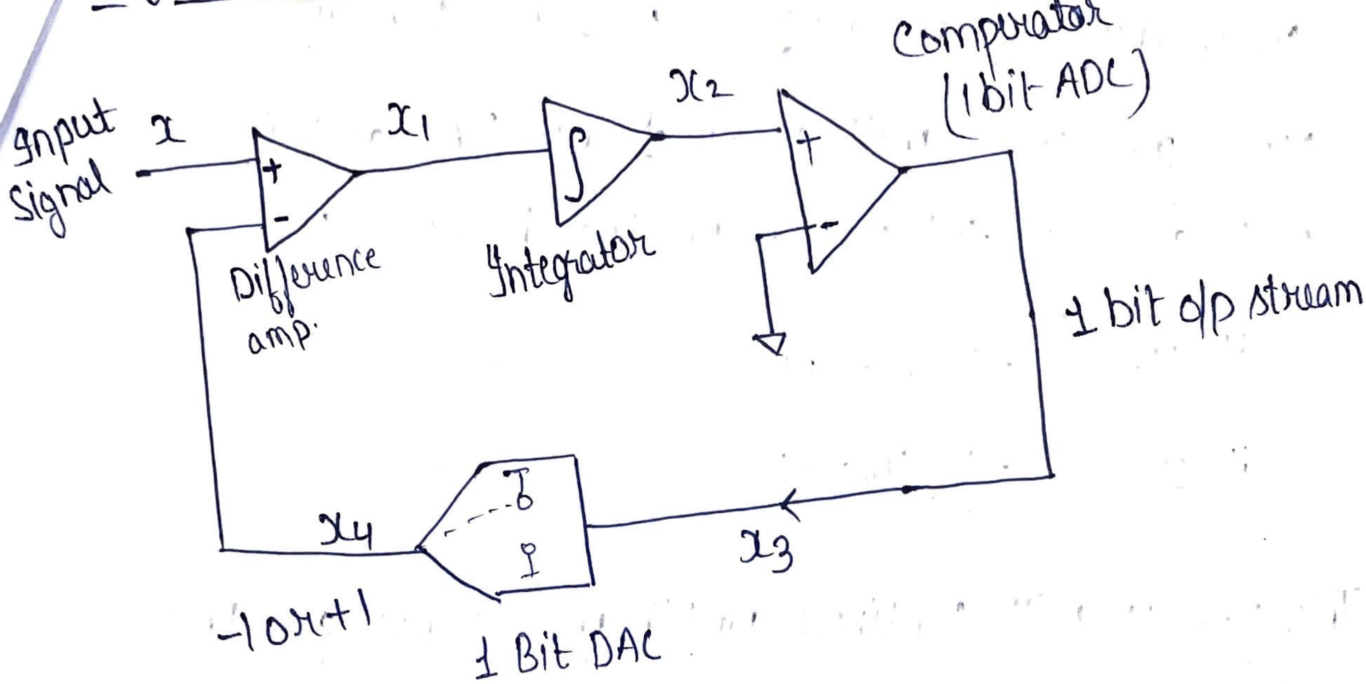
Advantages

* Capable of high speed and reliable
* Medium accuracy compared to other ADC types
* Good tradeoff between speed and cost.
* Capable of outputting the binary number in serial (one bit at a time) format.

Disadvantages

* Higher resolution successive approximation ADC's will be slower.

Sigma Delta ADC



Why we are calling it Sigma (Σ) Delta (Δ) -

* We are using integrator here (which is nothing else Σ)

and

* We are using comperator here which is nothing, a small amount $\frac{\Delta d}{d}$
difference

Working

* x_1 is calculated with the help of difference amplifier.
* Now x_1 transfers to integrator circuit. This integrator add the x_1 value with previous value of integrator.
* Now after integrator o/p (x_2) goes to comperator circuit. Comperator circuit compare the x_2 with zero volt (0V)
* if difference is +ve, the comprator output will be one (1).

* If difference is -ve, comprator o/p will be 0. So in this way we recieved a 1-bit stream.

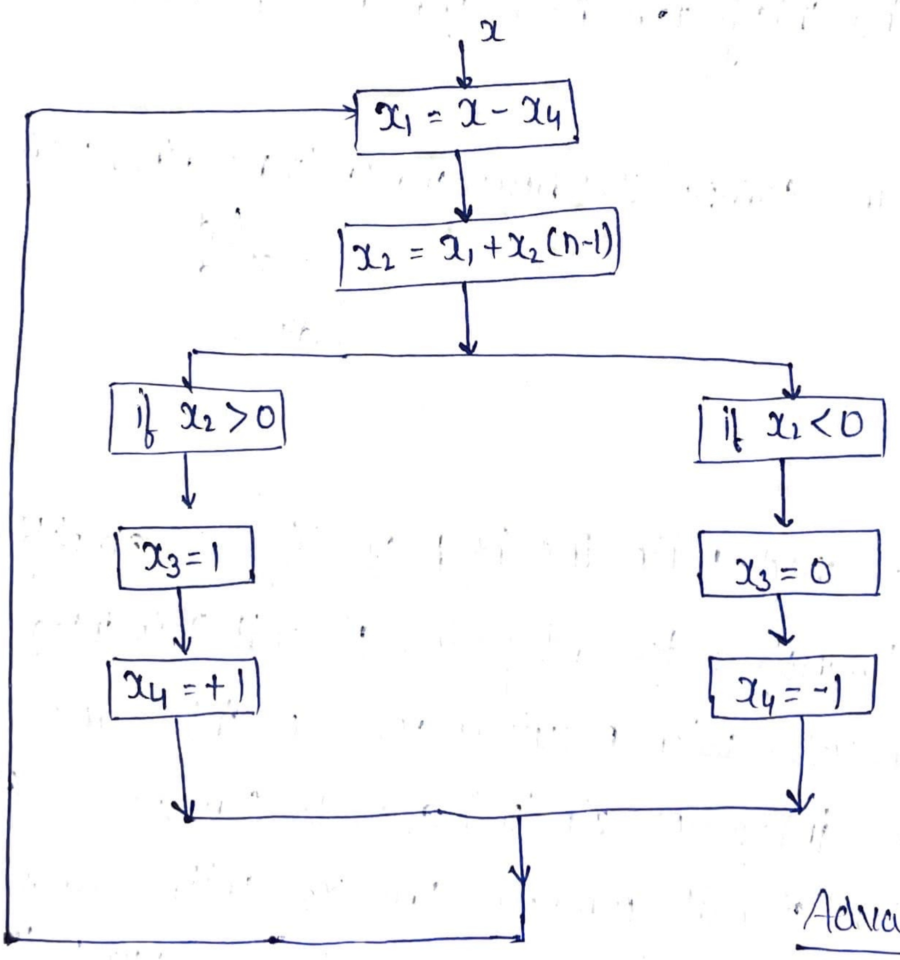
Now x_3 value will go to 1-bit DAC and it will give a +1 or -1 on the basis of:

if $x_3 = 1 \Rightarrow x_4 = +1$

if $x_3 = 0 \Rightarrow x_4 = -1$

This process will continue until we do not get the desired o/p.

Funtional Flow Chart

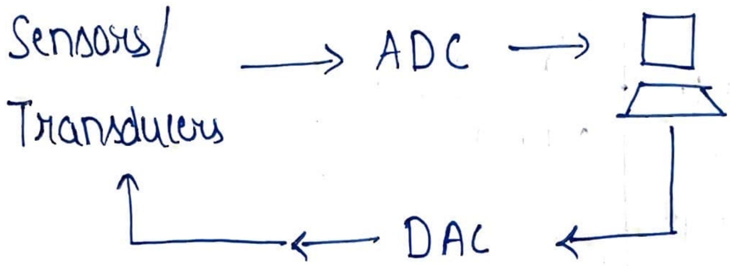


Advantages

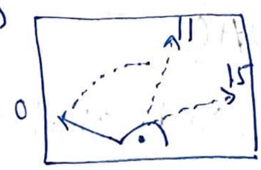
1. High resolution
2. Low cost

igital to Analog Converter (DAC)

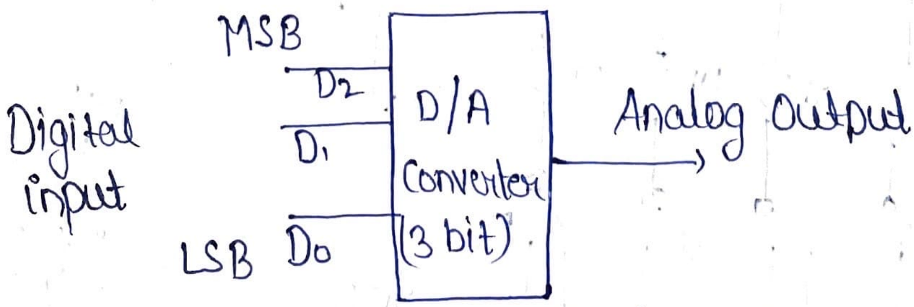
A DAC is a Digital to Analog converter. It converts a binary digital number in to an analog representation, most commonly voltage though current is also used sometimes.



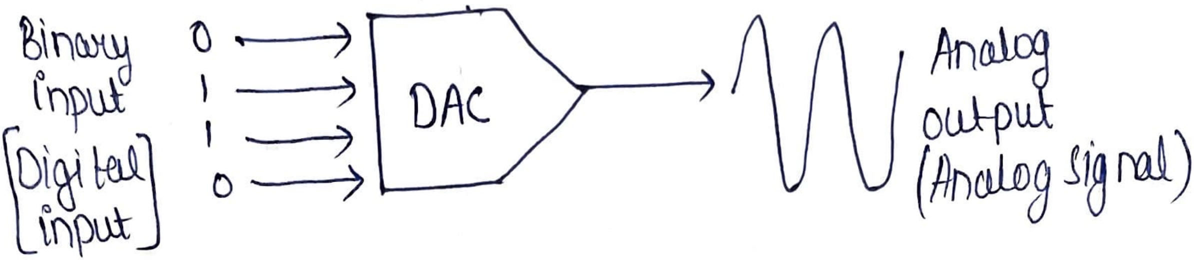
eg 4-bit → 1011 (11)

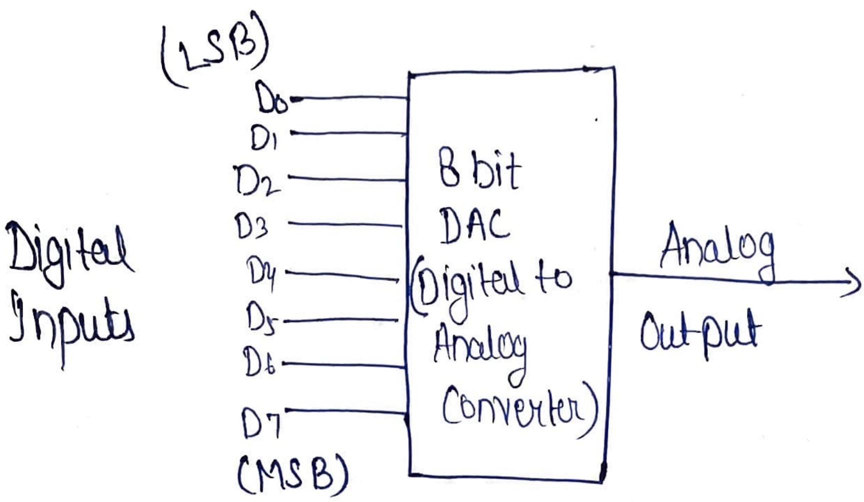


* Digital to analog converter translates a digital signal into an analog signal to represent a physical quantity.



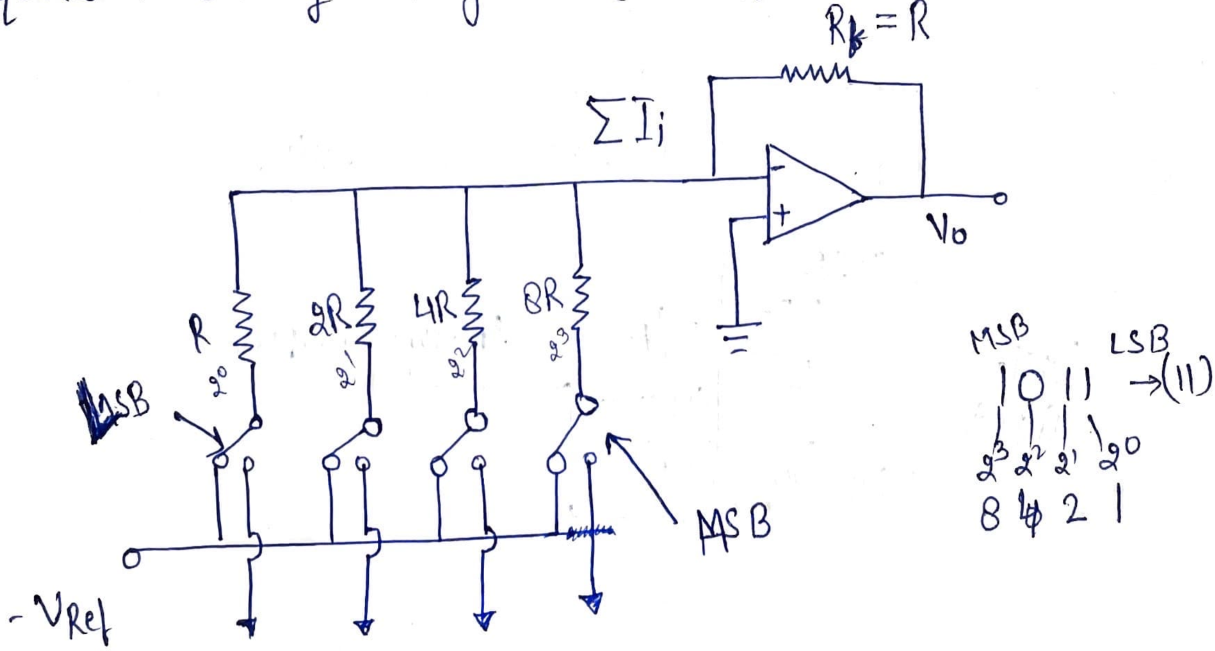
* A n-bit DAC has n input lines to have 2^n input combination and an analog output line.





Weighted Resistor DAC

In this type of DAC, each digital level is converted in to an equivalent analog voltage or current.



Considering a 4-bit DAC which accepts 0000 - 1111 fifteen discrete signals levels.

Here, we have to divide the output signal in to 15 different levels.

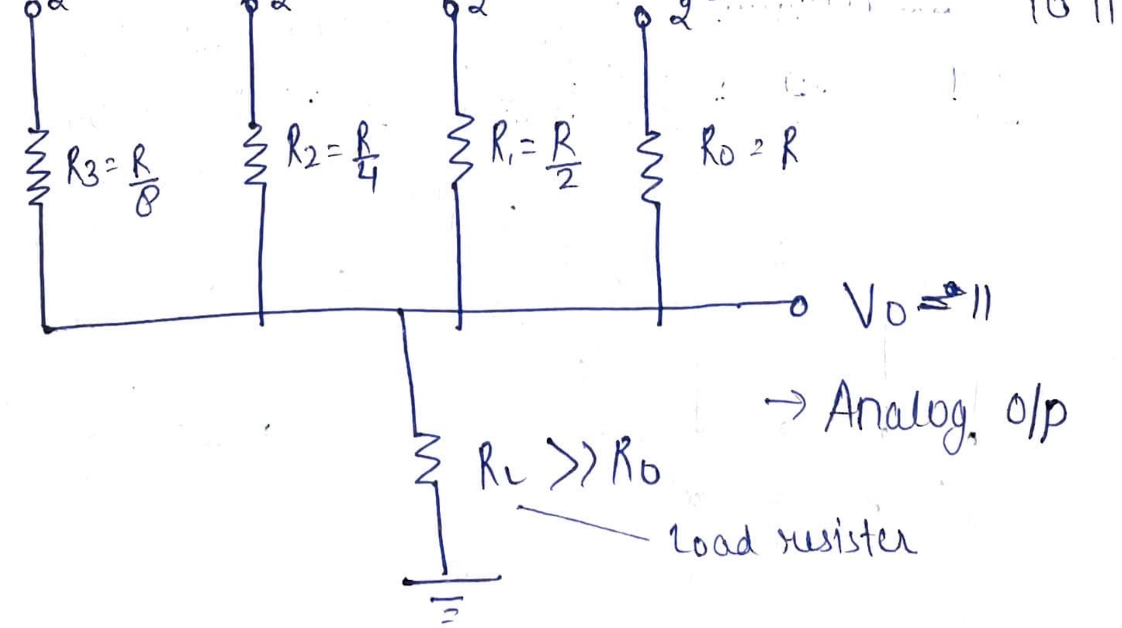
∴ The weighted resistor network is designed in such a way that a 1 in LSB (2^0) position results is $V_R \times \frac{1}{15}$ at the output.

$2^0 \rightarrow \frac{V_R}{15} = \frac{1}{15}$

$2^1 \rightarrow \frac{2}{15}$

$2^2 \rightarrow \frac{4}{15}$

$2^3 \rightarrow \frac{8}{15}$



Four bit DAC

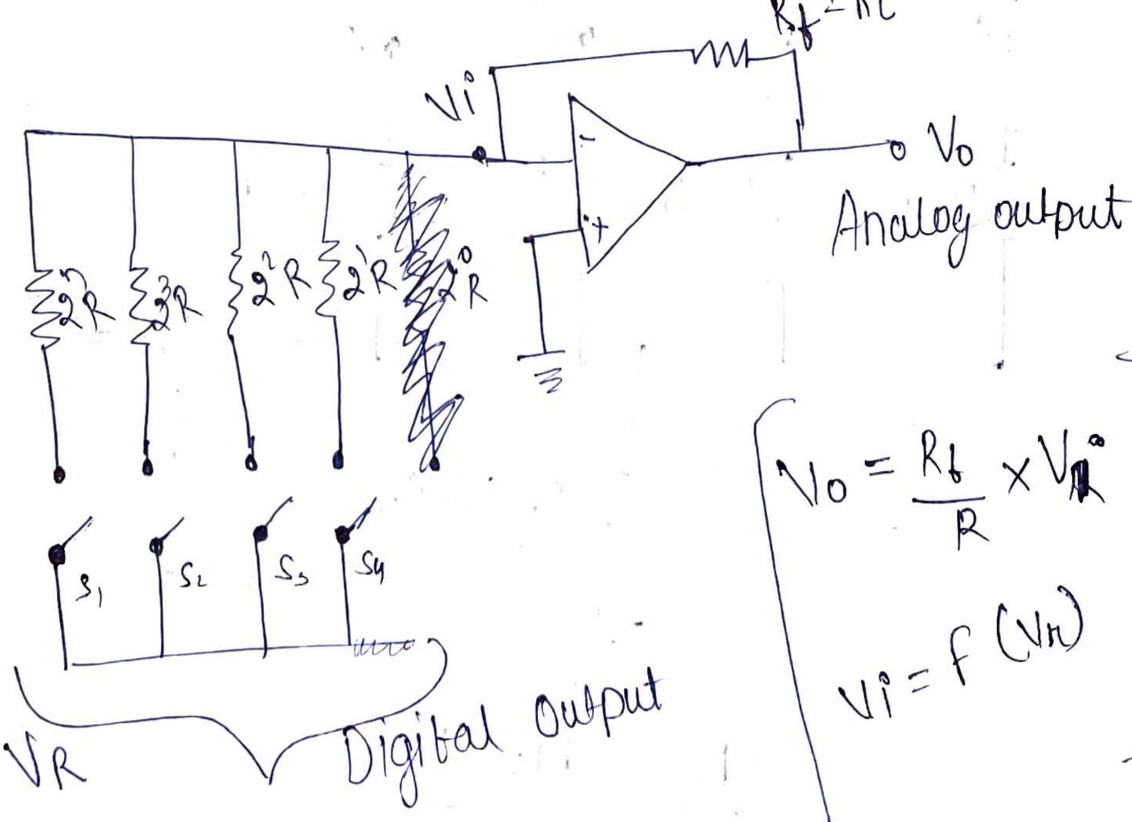
The DAC shown in figure on previous page

1) The 2^0 bit is changed to $\frac{1}{15}$th V_R, 2^1 bit to $\frac{2}{15}$th V_R, the weigh... ampli...
2^2 bit to $\frac{4}{15}$th V_R and 2^3 bit to $\frac{8}{15}$th V_R.

2) These four voltages are added together to form the analog o/p voltage using op-amp summing circuit where R_0, R_1, R_2, and R_3 form a voltage divider n/w connected with op-amp and R_L is the load resis...

$$V_o = \frac{\frac{V_R}{R_1} + \frac{V_R}{R_2} + \frac{V_R}{R_3} + \frac{V_R}{R_4}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4}}$$

$$V_o = \frac{\frac{V_R}{R} + \frac{V_R}{R/2} + \frac{V_R}{R/4} + \frac{V_R}{R/8}}{\frac{1}{R_1} + \frac{1}{R/2} + \frac{1}{R/4} + \frac{1}{R/8}}$$



$$V_o = \frac{R_f}{R} \times V_i \quad (V_i)$$

$$V_i = f(V_R)$$

The weighted resistor arrangement is used with an operational amplifier to amplify and quantize the output voltage in accordance with the range and resolution.

* For input of digital data, digital on/off switches are used.

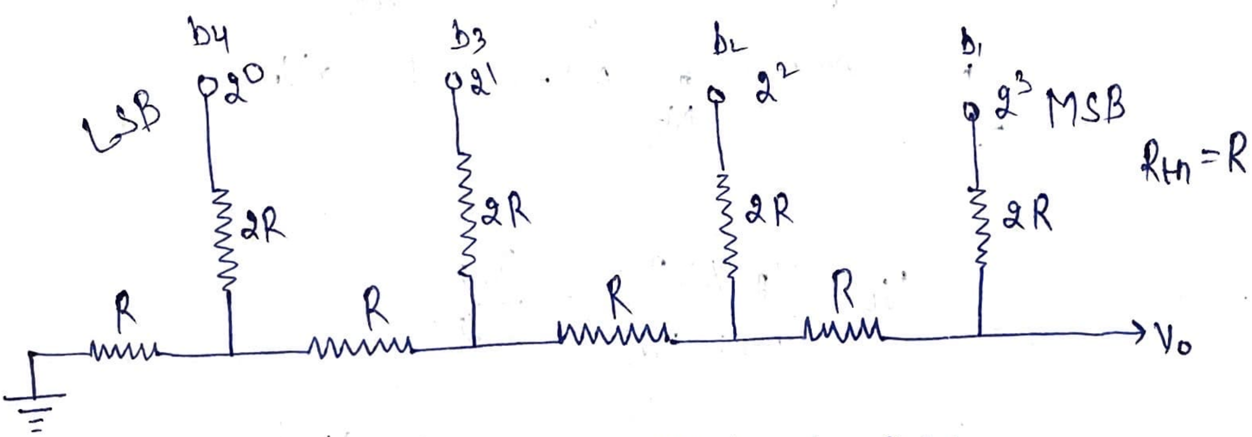
* The main drawback of this converter is the use of large resistance. eg In a 4 bit DAC the maximum value of resistance will be 16 which is very high. It makes power consumption to be increased.

R-2R Ladder type DAC

A wide range of resistor values is required in binary weighted resister by DAC.

In this type, only two value resistors are required i.e value R and 2R, which shows its suitability towards its fabrication.

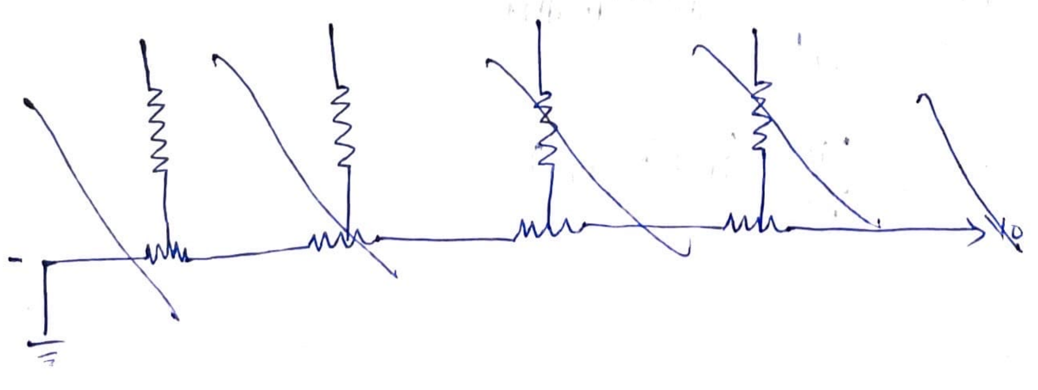
Considering 4-bit binary input data $b_1\ b_2\ b_3\ b_4$

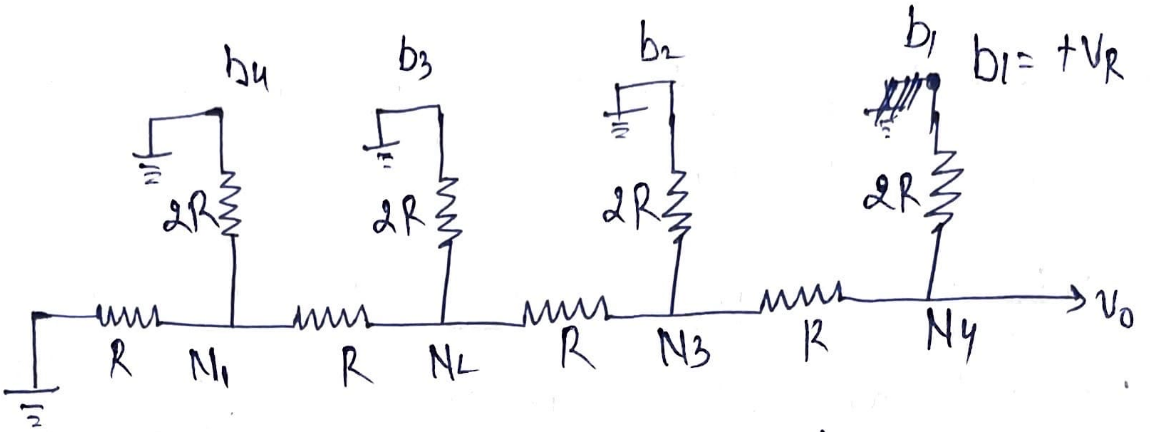


4- bit R- RR Ladder DAC

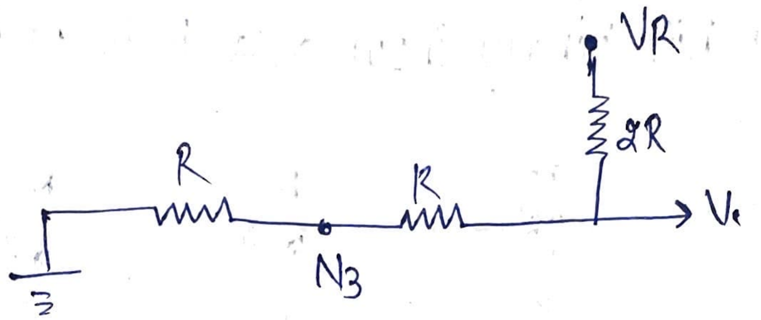
In this circuit, the o/p voltage is a weight sum of digital inputs.

for example $b_1, b_2, b_3, b_4 = 1000$





Equivalent ckt for 1000



$$V_O = \frac{V_R \times 2R}{R + R + 2R} = \frac{V_R}{2}$$

Thus for digital i/p 1000, the $V_O = V_R/2$

Similarly for 0100 → $V_R/4$

0010 → $V_R/8$

0001 → $V_R/16$

0011 → $\frac{V_R}{8} + \frac{V_R}{16}$

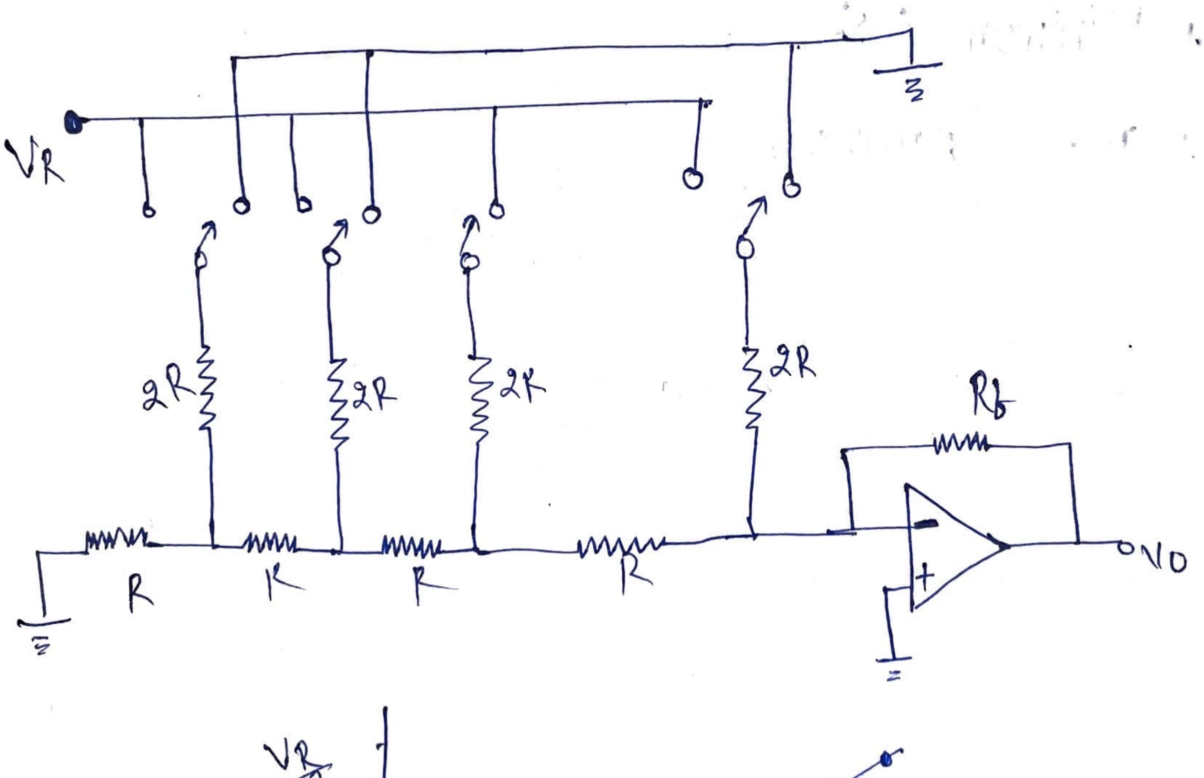
it means $\frac{V_R}{2^1}$ (maximum)

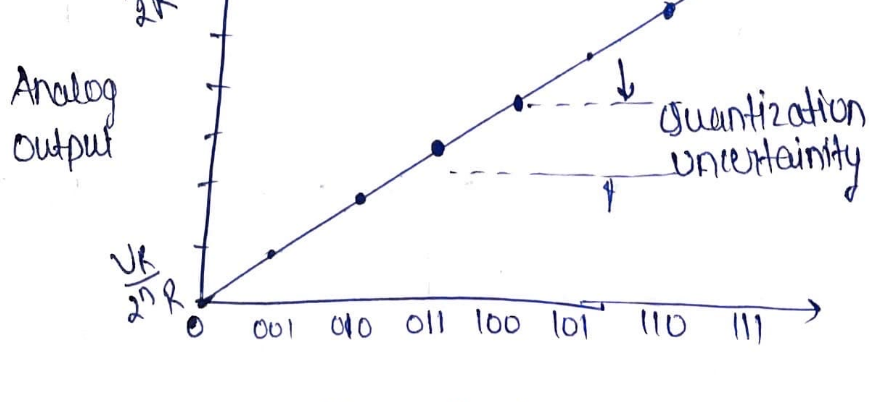
$\frac{V_R}{2^n}$ (minimum)

Hence

$$V_o = \frac{V_R}{2^1} + \frac{V_R}{2^2} + \frac{V_R}{2^3} + \cdots \frac{V_R}{2^n}$$

$$\boxed{\begin{array}{l} \text{Resolution, } I = \frac{1}{2^n} \times \frac{V_R}{R} \\ V = \frac{1}{2^n} \frac{V_R}{R} R_f \end{array}}$$





Advantages

* R-2R ladder DAC contains only two values of resistor. R and 2R. So, it is easy to select and design more accurate resistors.

* If more number of bits are present in the digital input, then we have to include required number of R-2R sections additionally.

* Simple in design

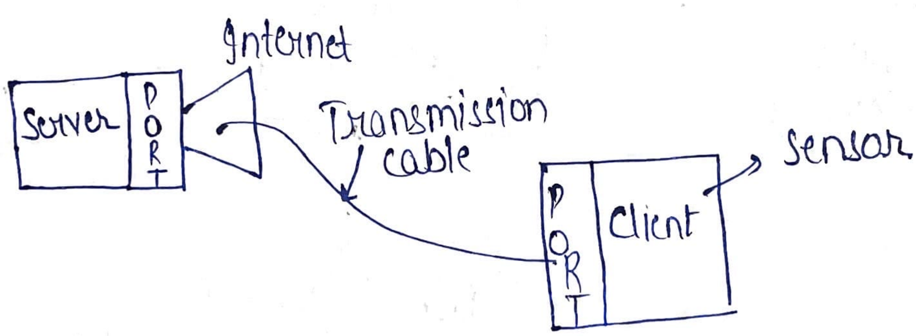
* Minimum cost

* More Accurate

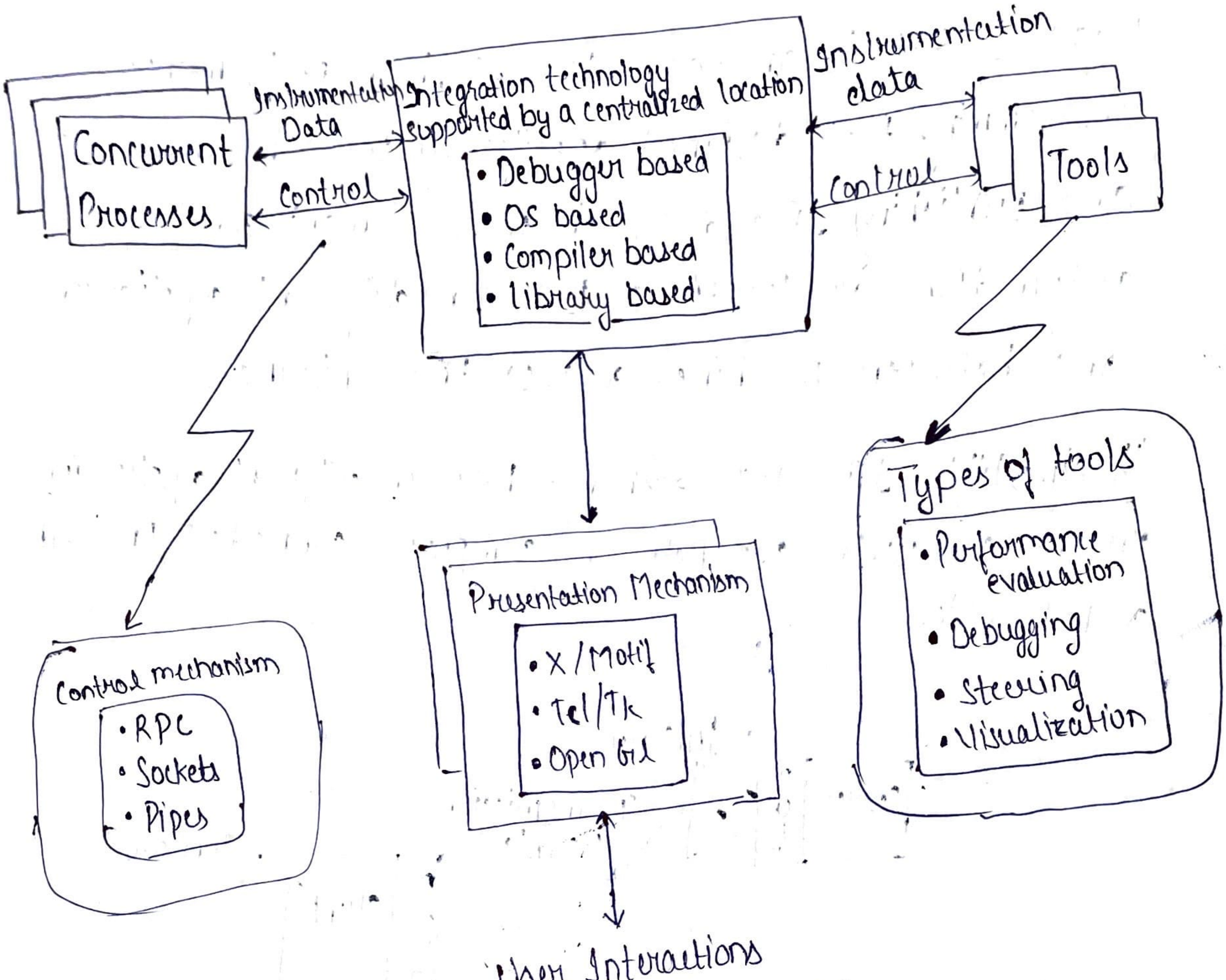
Data Sockets

Data Socket is an easy-to use, high performance programming tool designed specifically for sharing and publishing live data in measurement and automation applications between different applications and between machines across the internet.

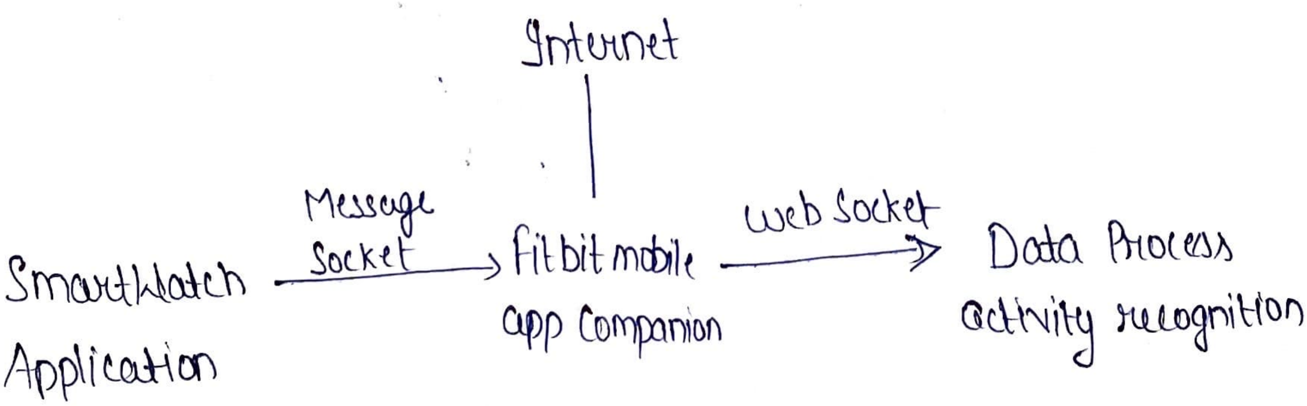
It simplifies live data exchange between different applications on one computer or between computers connected through a network.



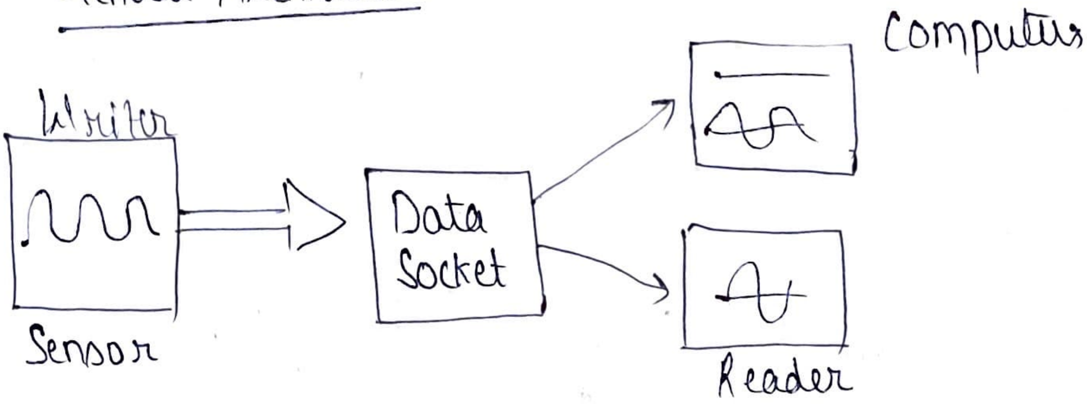
Data Sockets in DAC



Basic diagram of Instrumentation



General Architecture

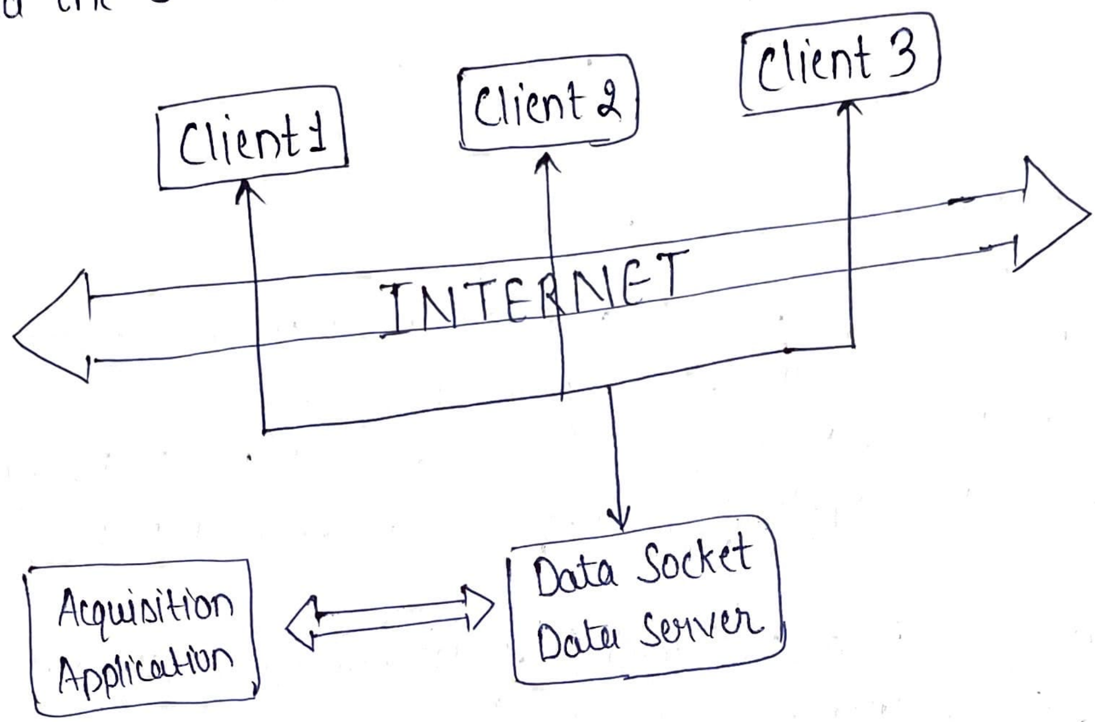


A socket is one end-point of a two way communication link between two programs running on the network.
A socket is bound to a port number so that the TCP layer can identify the application that data is destined to be sent

An end-point is a combination of IP address and a port number. Every TCP connection can be uniquely identified by its two end points. In that ~~way~~

Data Socket Transfer Protocol (DSTP) is a convenient mechanism to monitor the most recent values of measurement data distributed over the internet. This document describes DSTP, the component essential to this protocol, and why dSTP is such an efficient data-sharing protocol.

We can have multiple connections between host and the server.



Data Socket Sharing

→ Data sockets are used in
- → Measurement
- → Calibration
- → Moniter
- → Data sharing
- → Storage
- → Communication