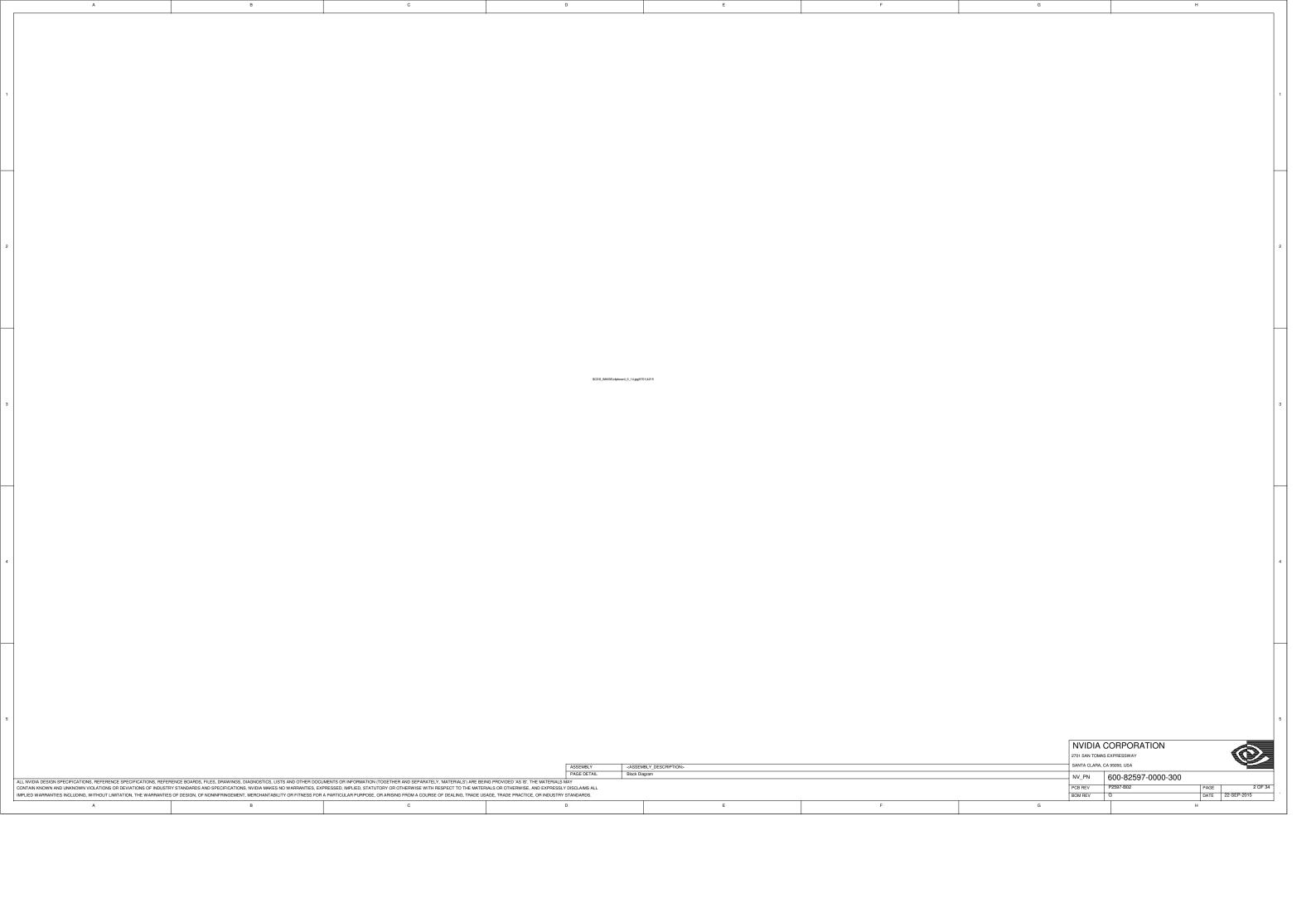
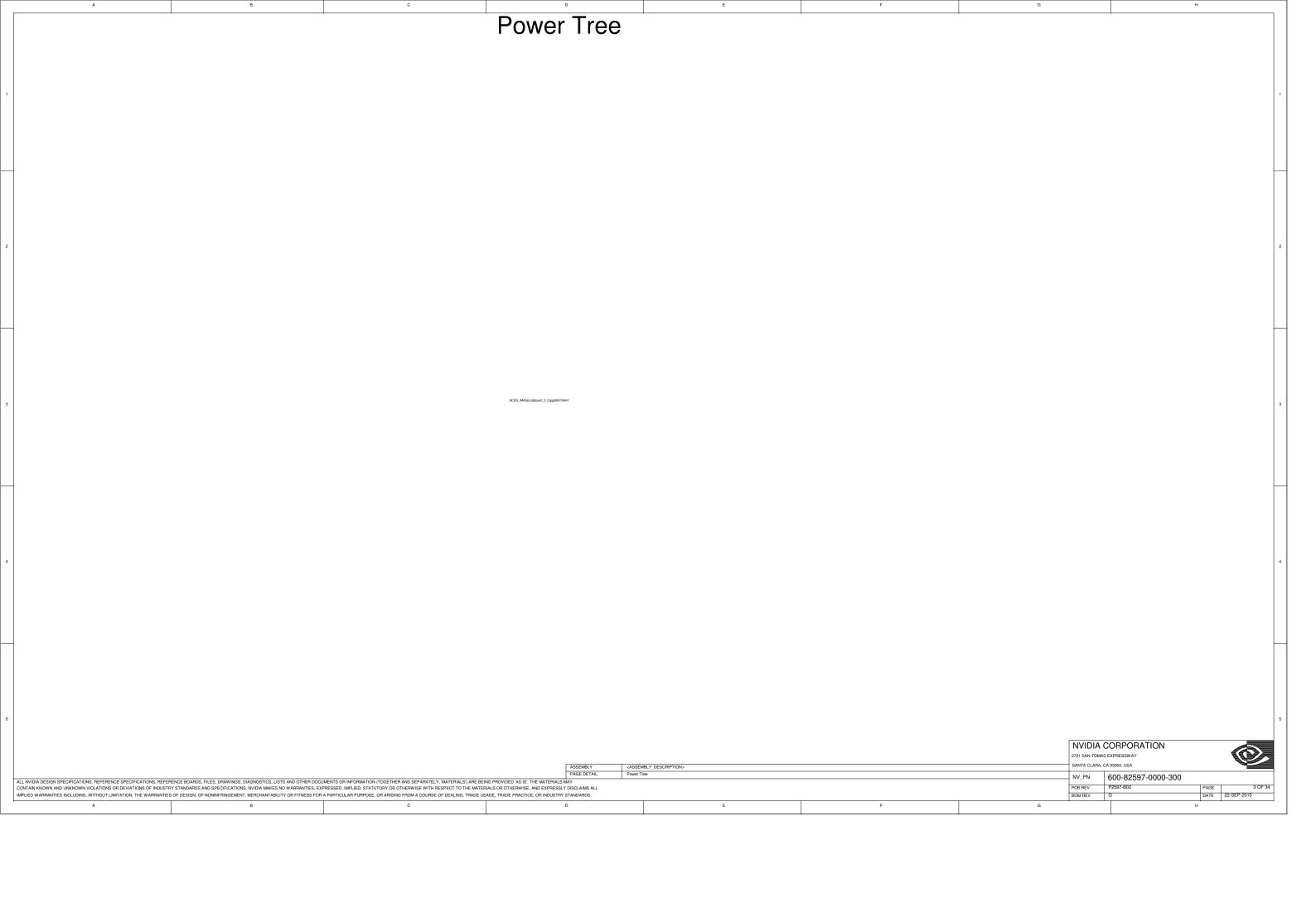
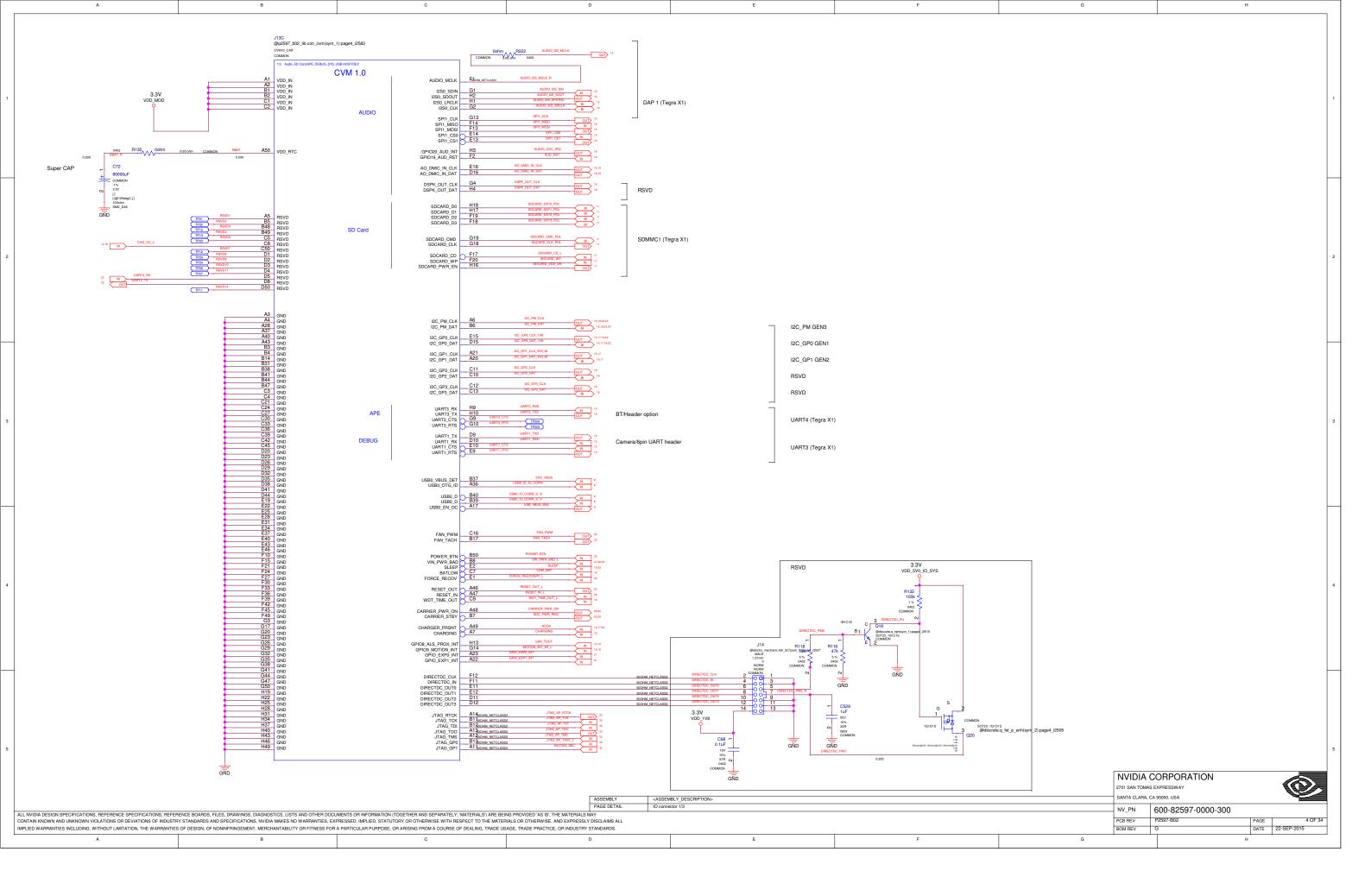
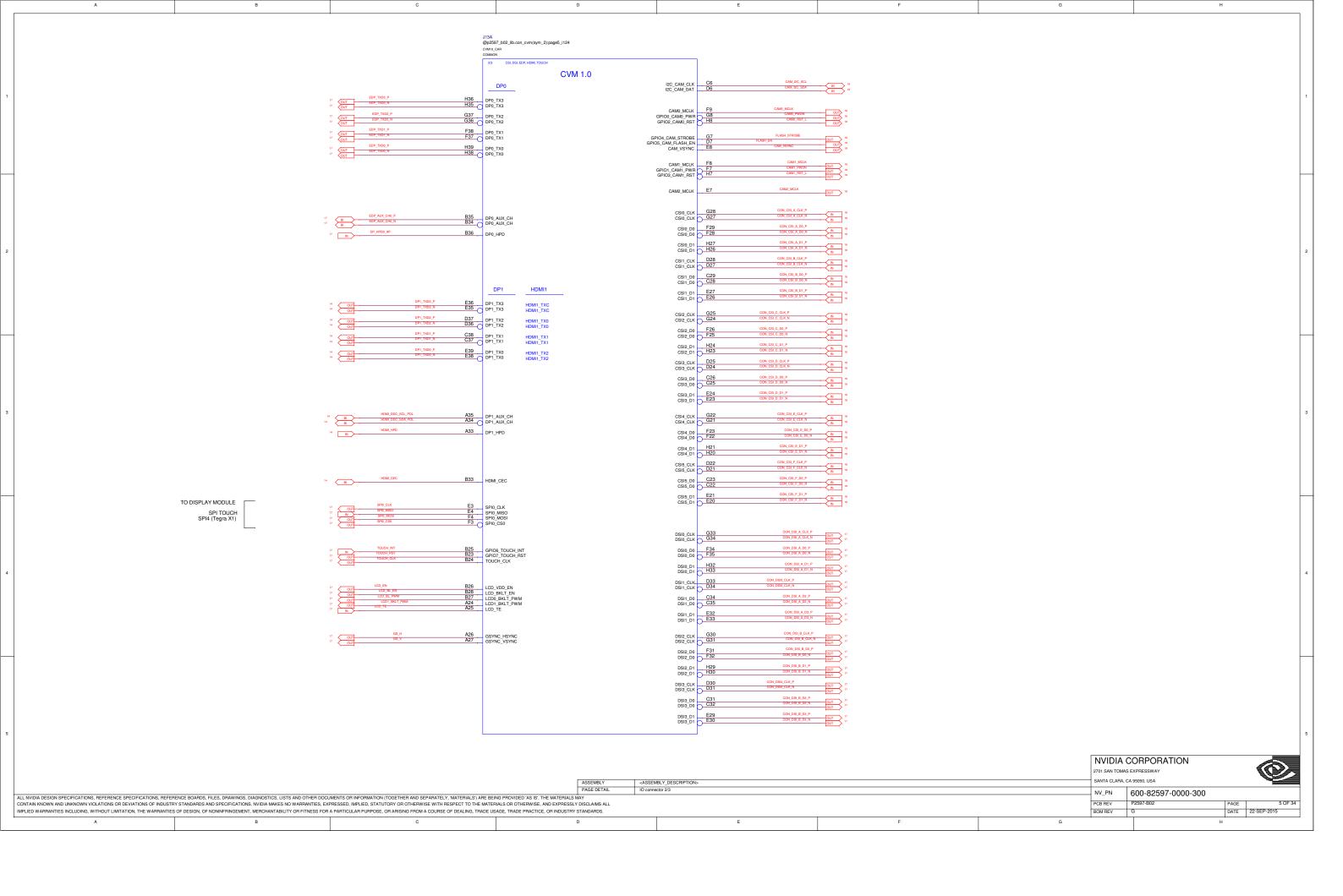
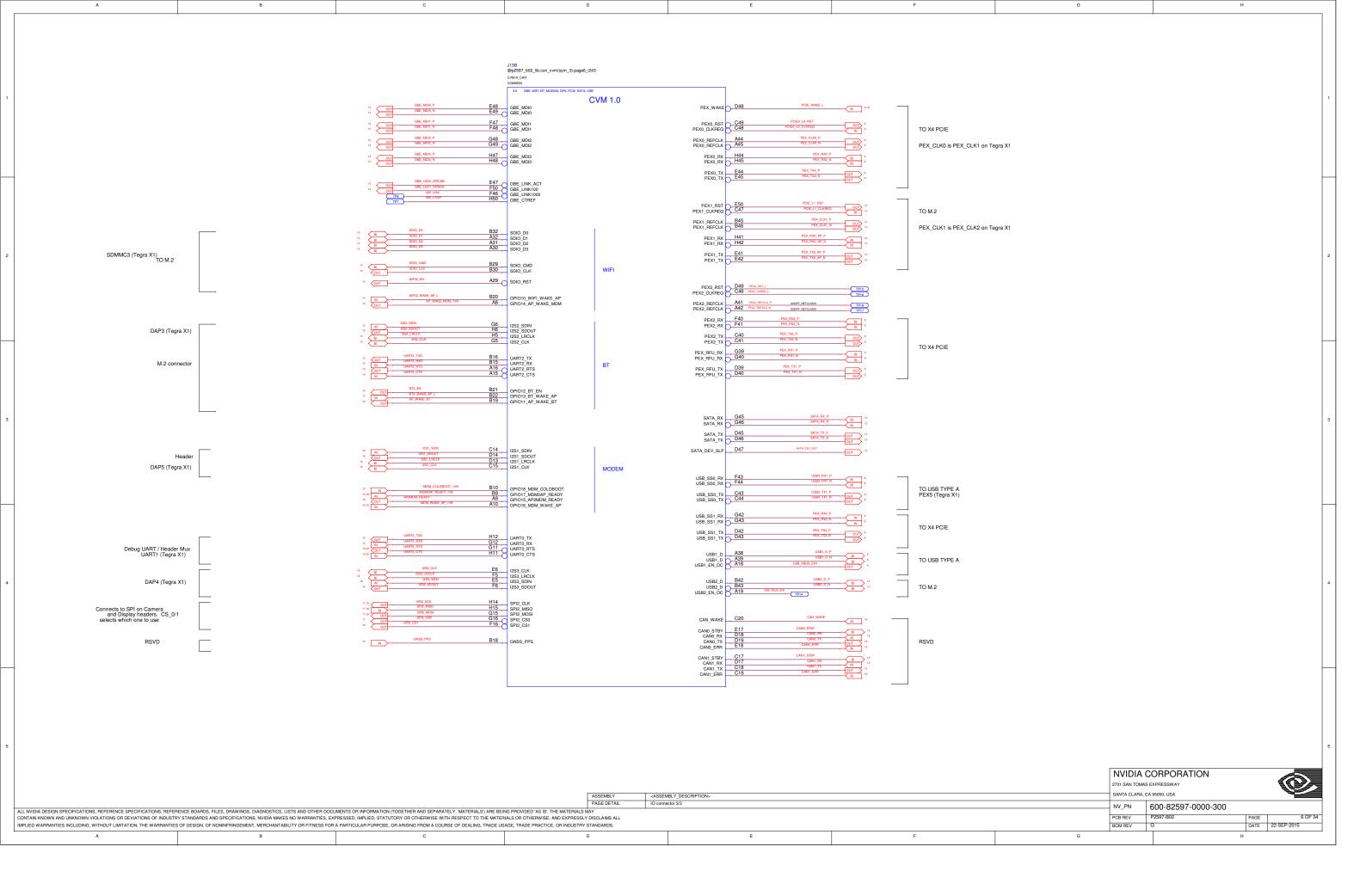
P2597-B02 Tegra X1 Jetson CV-B HDMI, USB, PCIe, SATA, Gbe TABLE OF CONTENTS Page Description Page Description Table of Contents BLANK 26 Block Diagram 27 DC Jack Power Tree 5V & 3V3 Vregs 3V3 SLP AND 1.8V Vregs IO connector 1/3 29 IO connector 2/3 30 Rail Discharge IO connector 3/3 Power Monitor I 31 **BLANK** 32 Power Monitor II USB3.0 type A and USB2.0 micro 33 **Buttons and Mechanical** PCIe x4 Connector **REVISION HISTORY** M.2 KEY E 10 11 SDcard Slot 12 SATA 13 Gigabit Ethernet 14 HDMI 15 Serial port and JTAG **IO Expansion Connector** 17 **DSI** Connector 18 CSI Connector 19 BLANK 20 **BLANK** 21 **GPIO** Expanders 22 FAN AND DEBUG 23 12V BOOST **EEPROM** 24 P2597 I2C Port Assignments 25 BLANK BUS:Device address Slave Device | NA3221 (Power measurement) | I2C Gen 2 : 7*h42 | NA3221 (Power measurement) | I2C Gen 2 : 7*h43 | TCA9539 (GPIO Expander) | I2C Gen 2 : 7*h74 | TCA9539 (GPIO Expander) | I2C Gen 2 : 7*h77 | BOARDID EEPROM | I2C Gen 3 : 7*57h | P2180 I2C Port Assignments Slave Device BUS:Device address NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWA <ASSEMBLY_DESCRIPTION
Table of Contents SANTA CLARA, CA 95050, USA ASSEMBLY PAGE DETAIL NV_PN 600-82597-0000-300 ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED 'AS IS: THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS. PCB REV DATE 22-SEP-2015 BOM REV

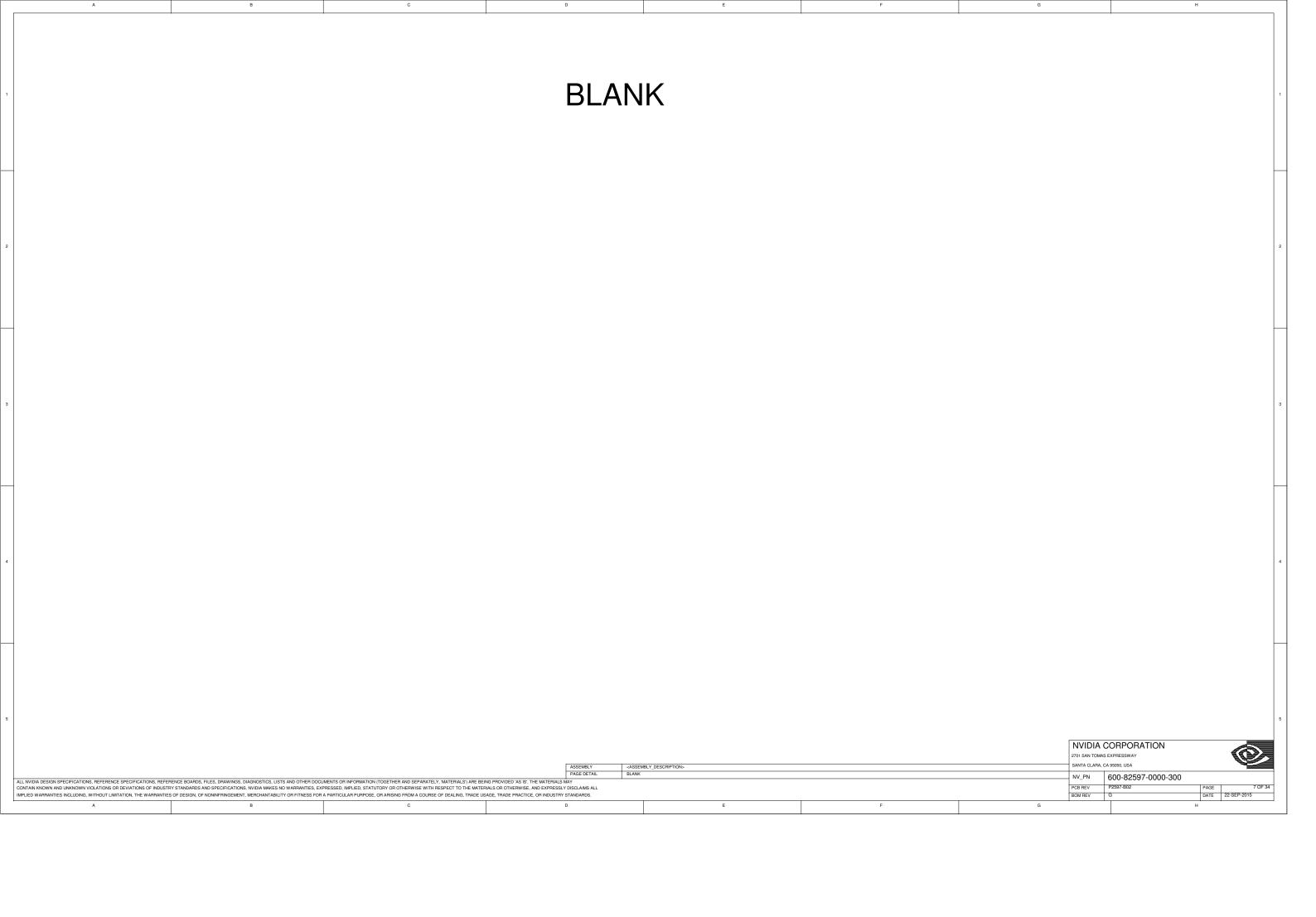


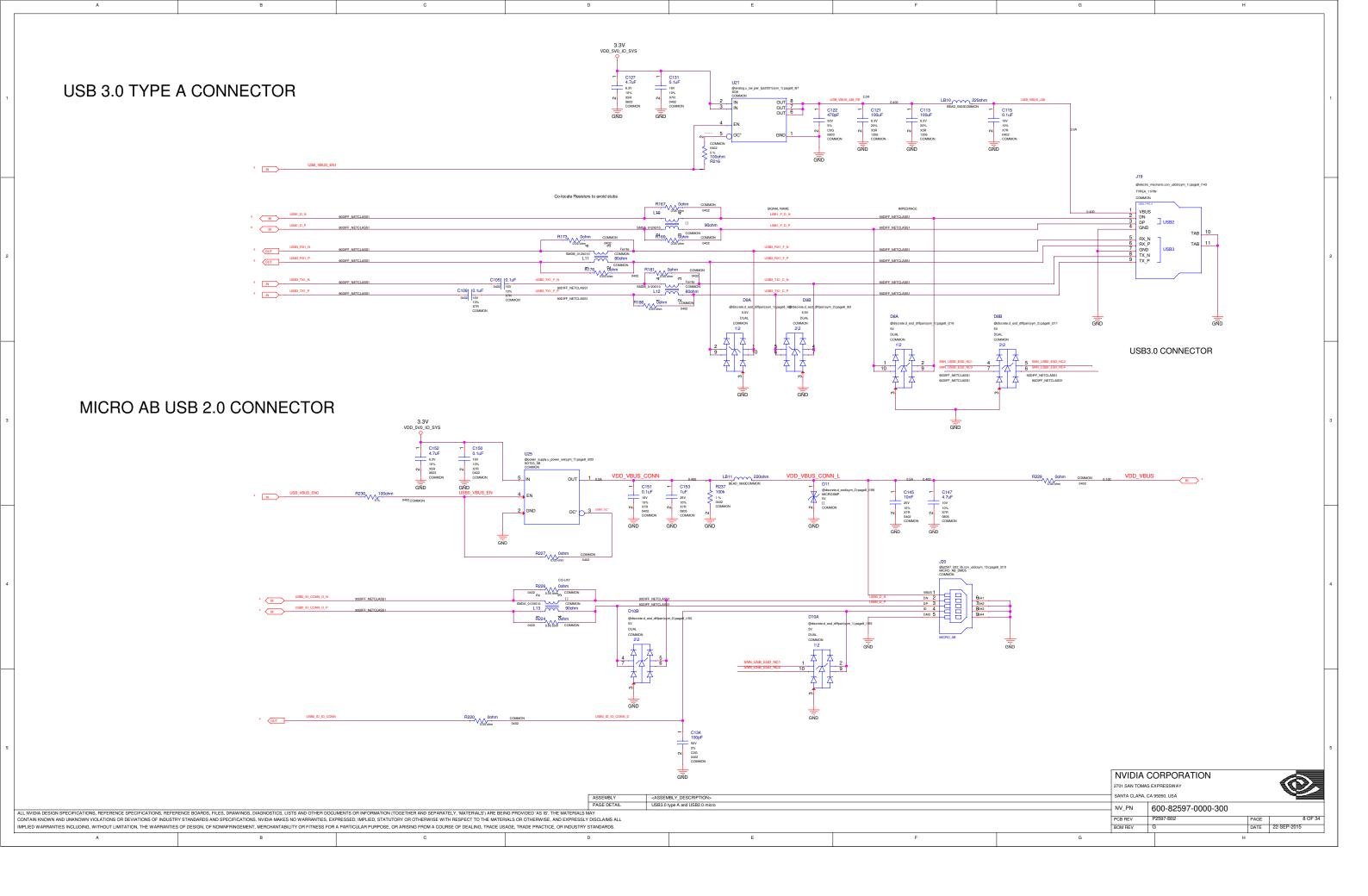


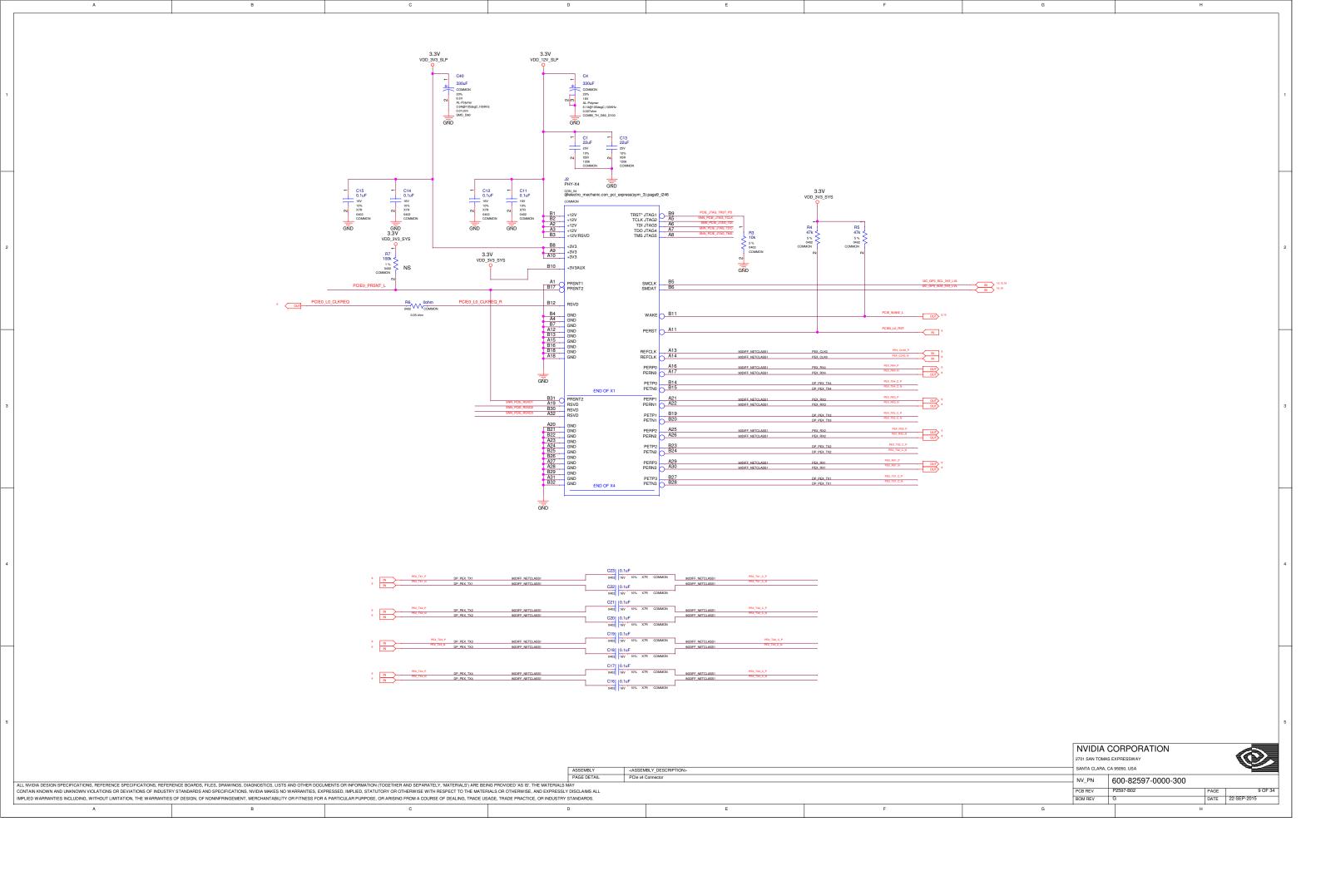


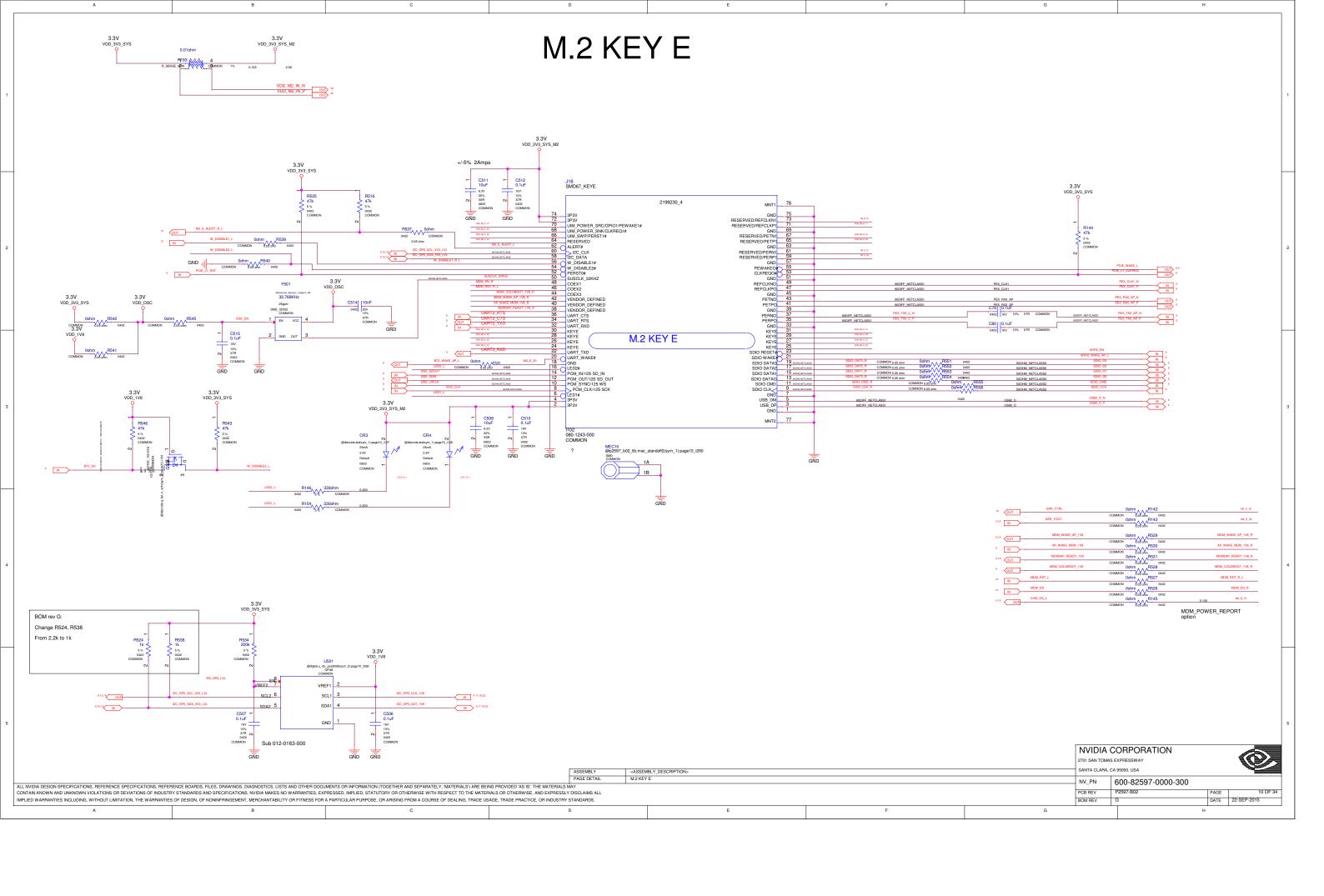


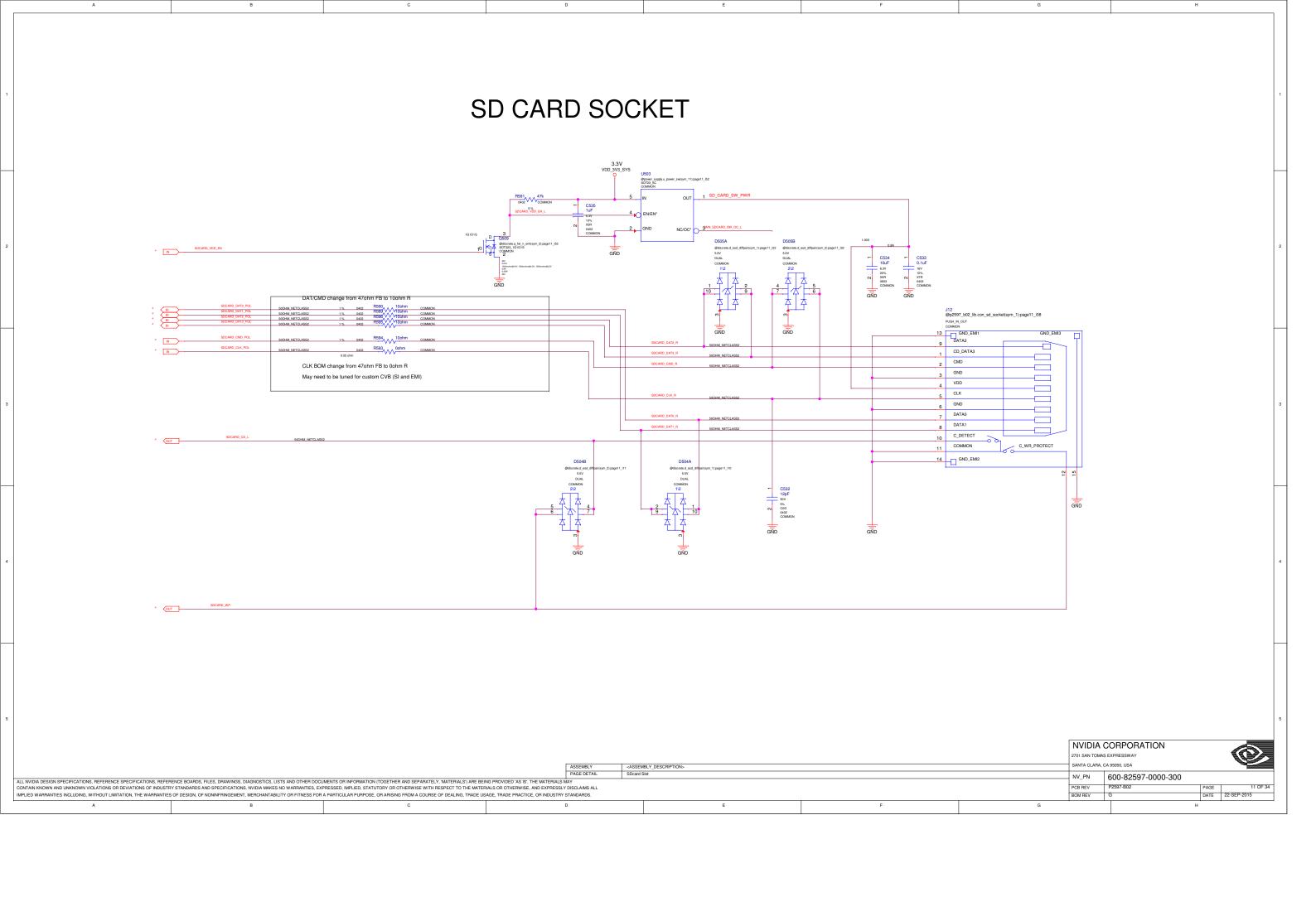


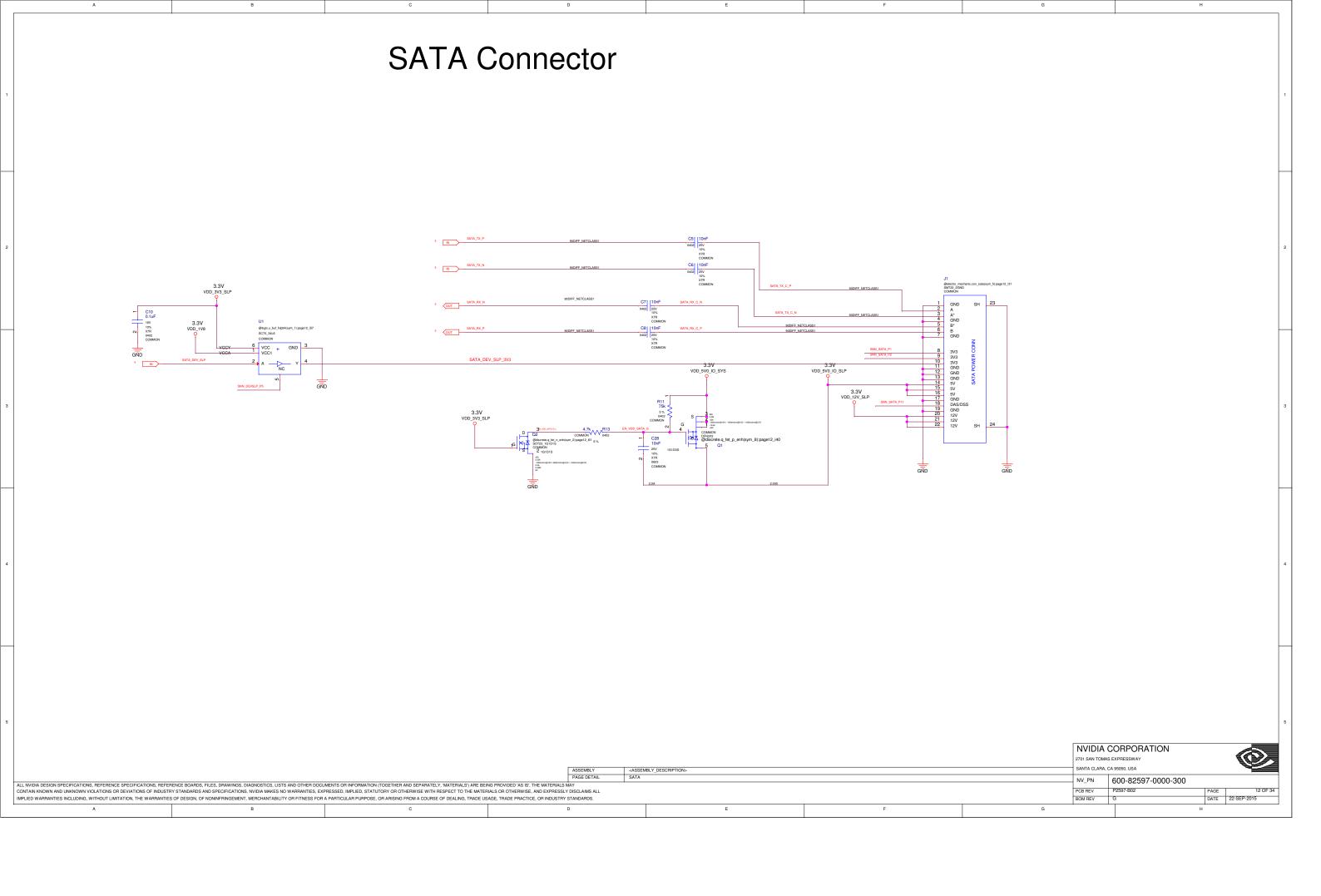


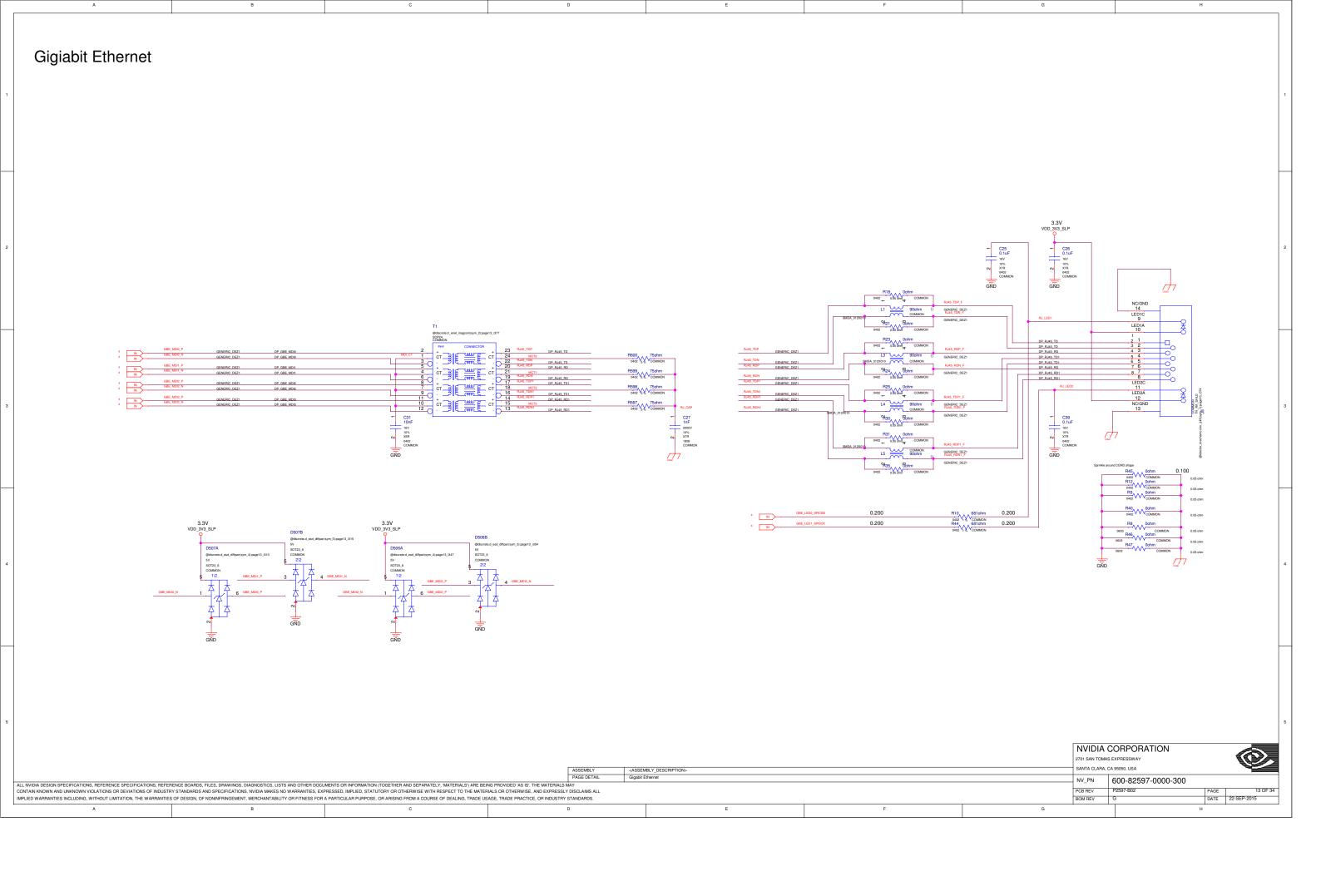


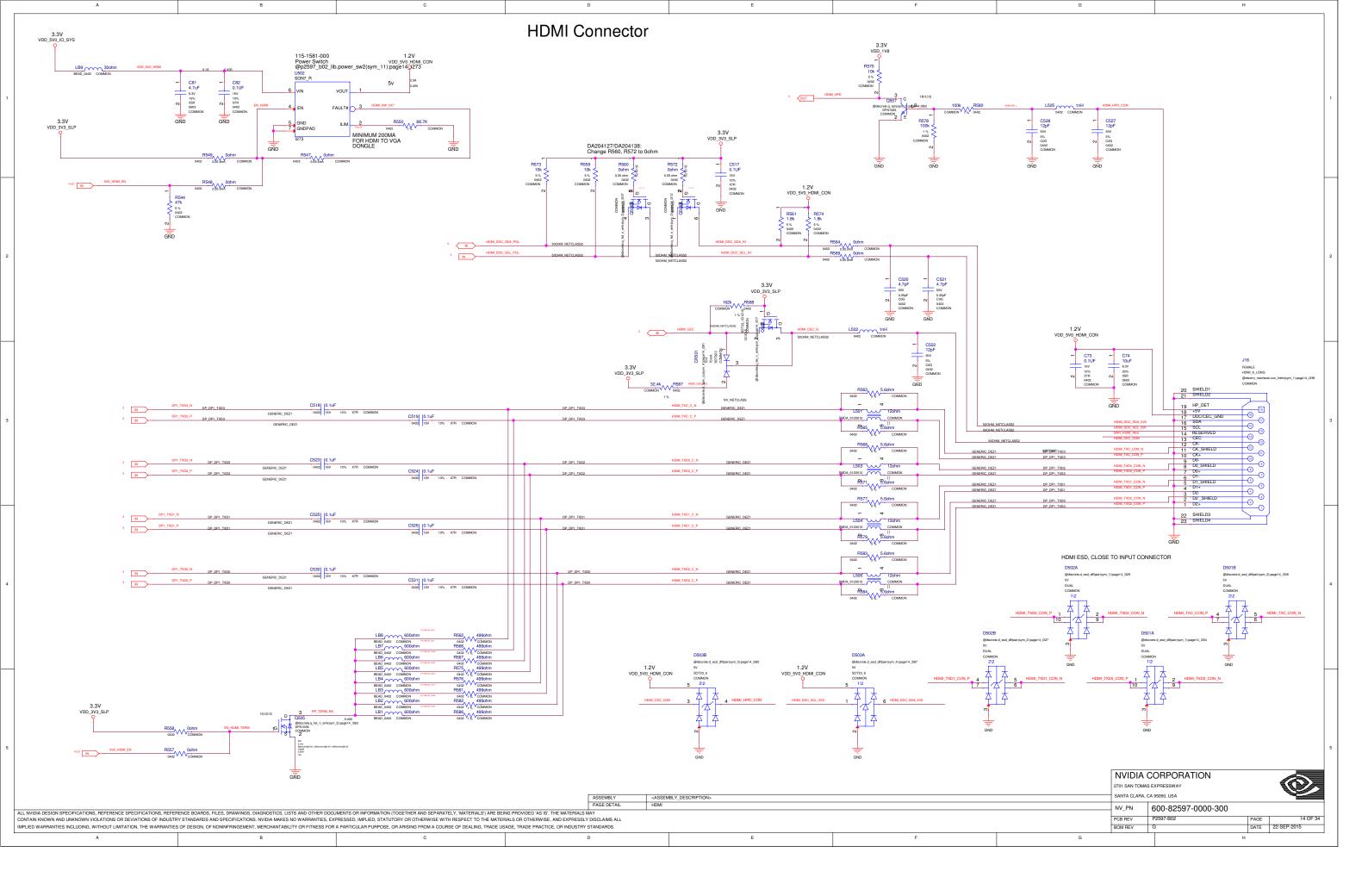


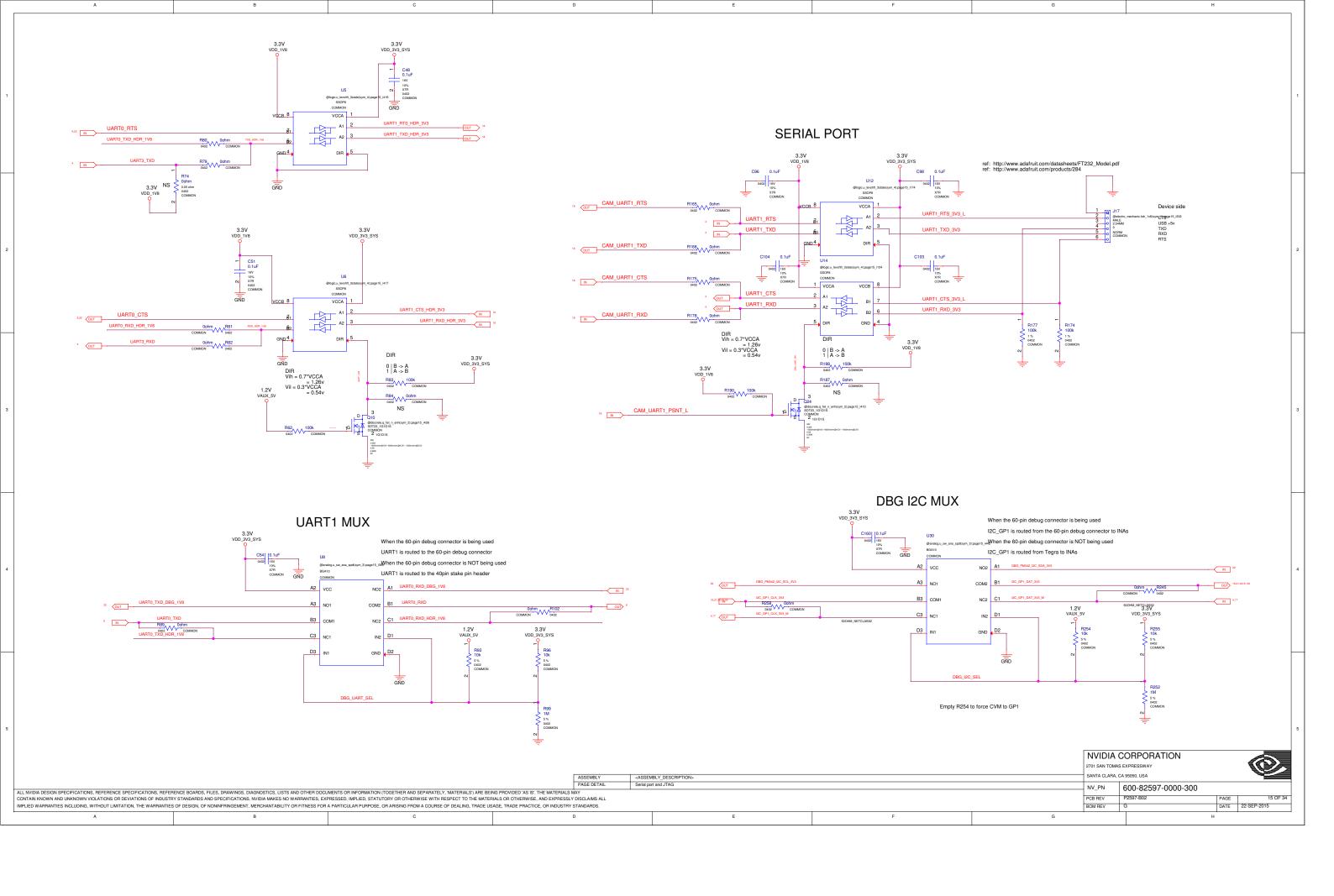


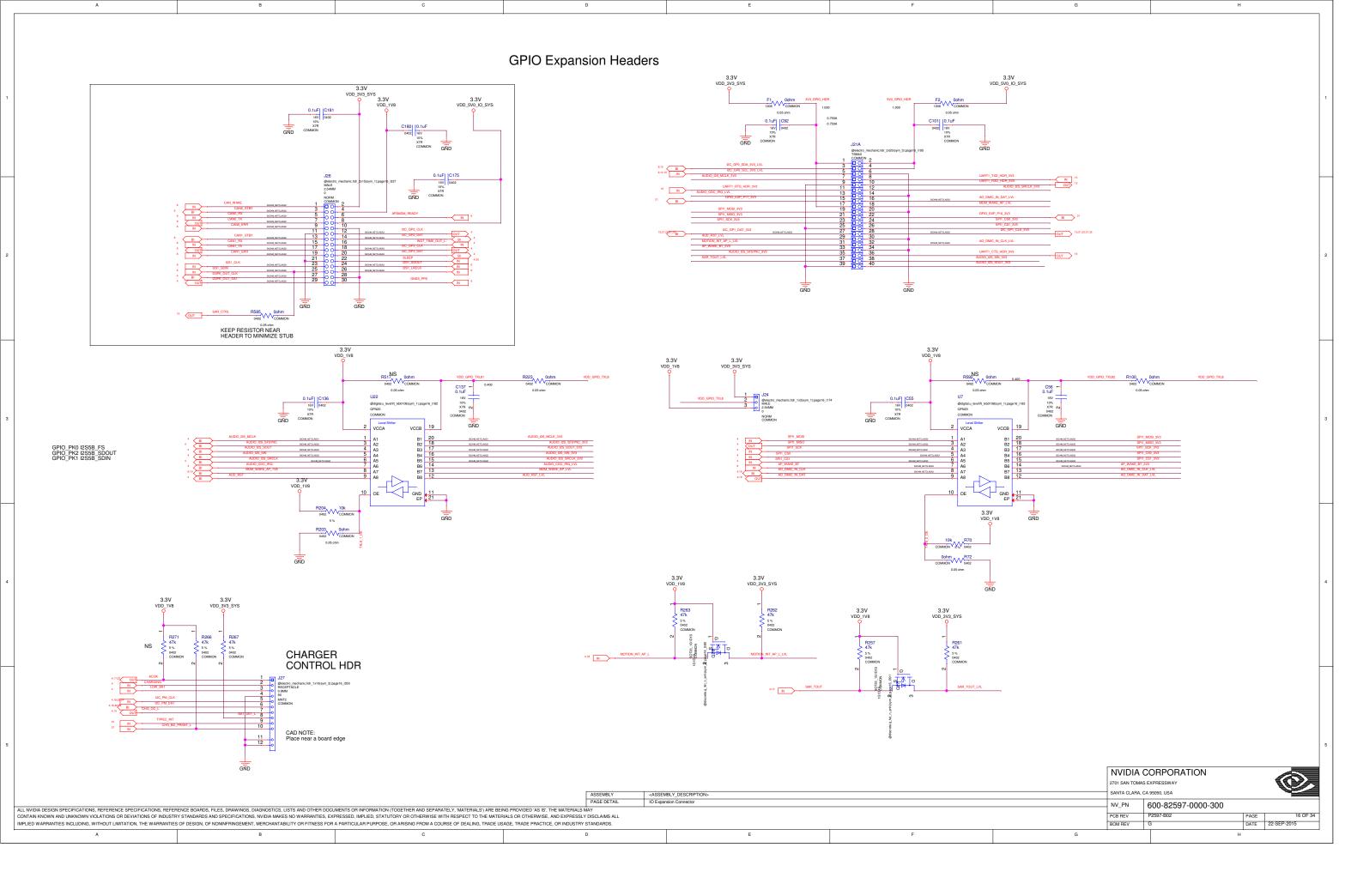


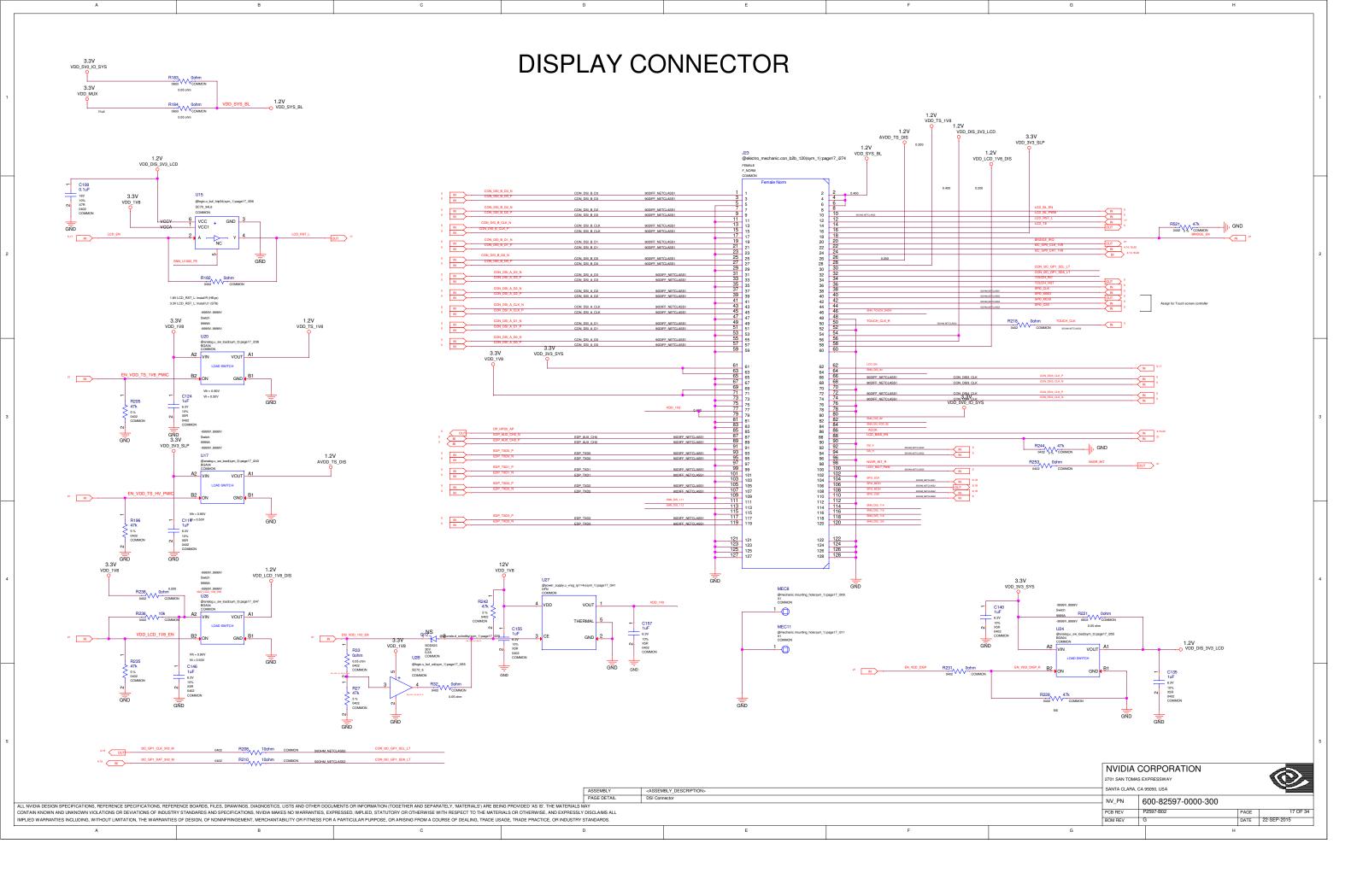


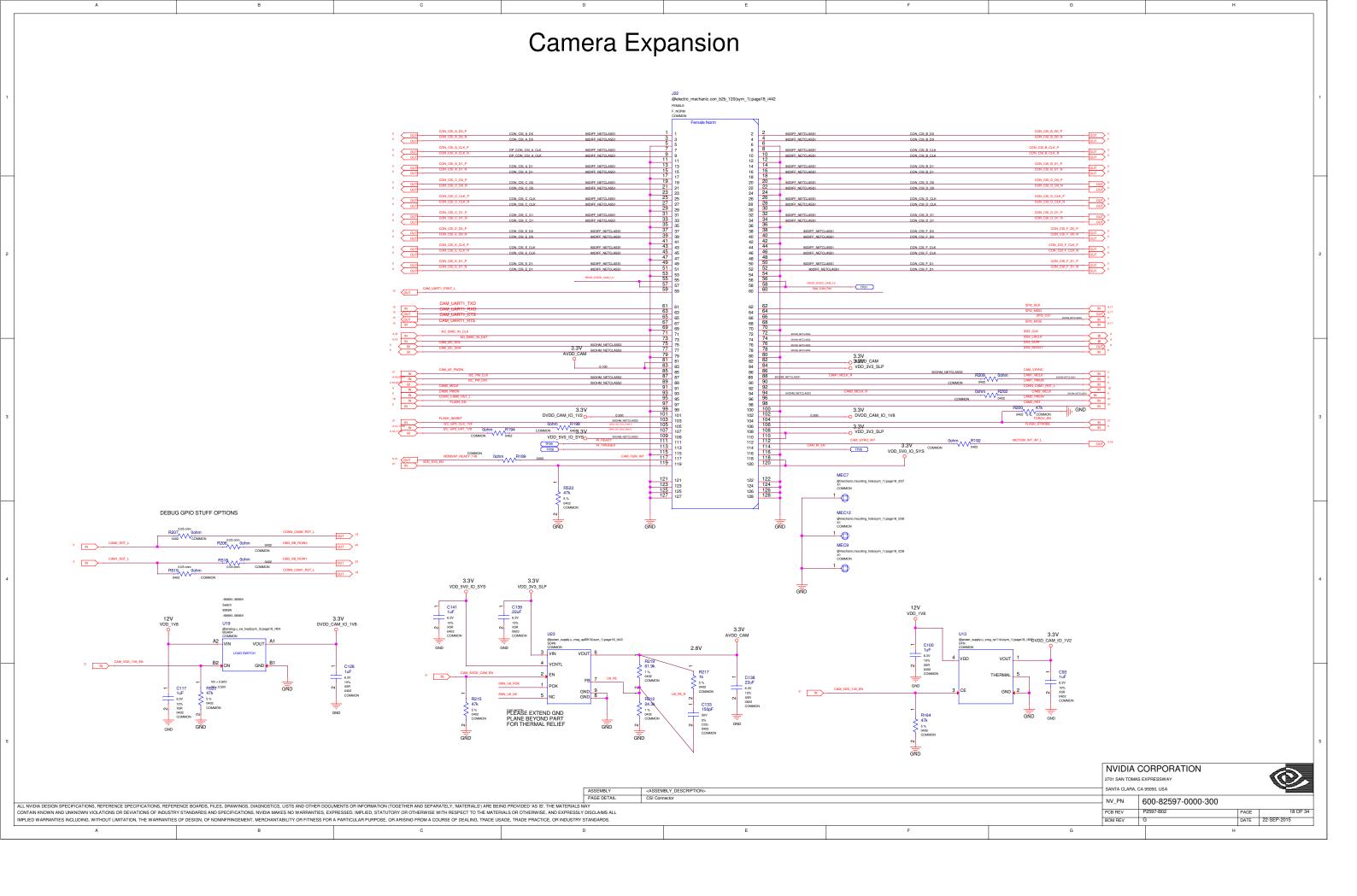


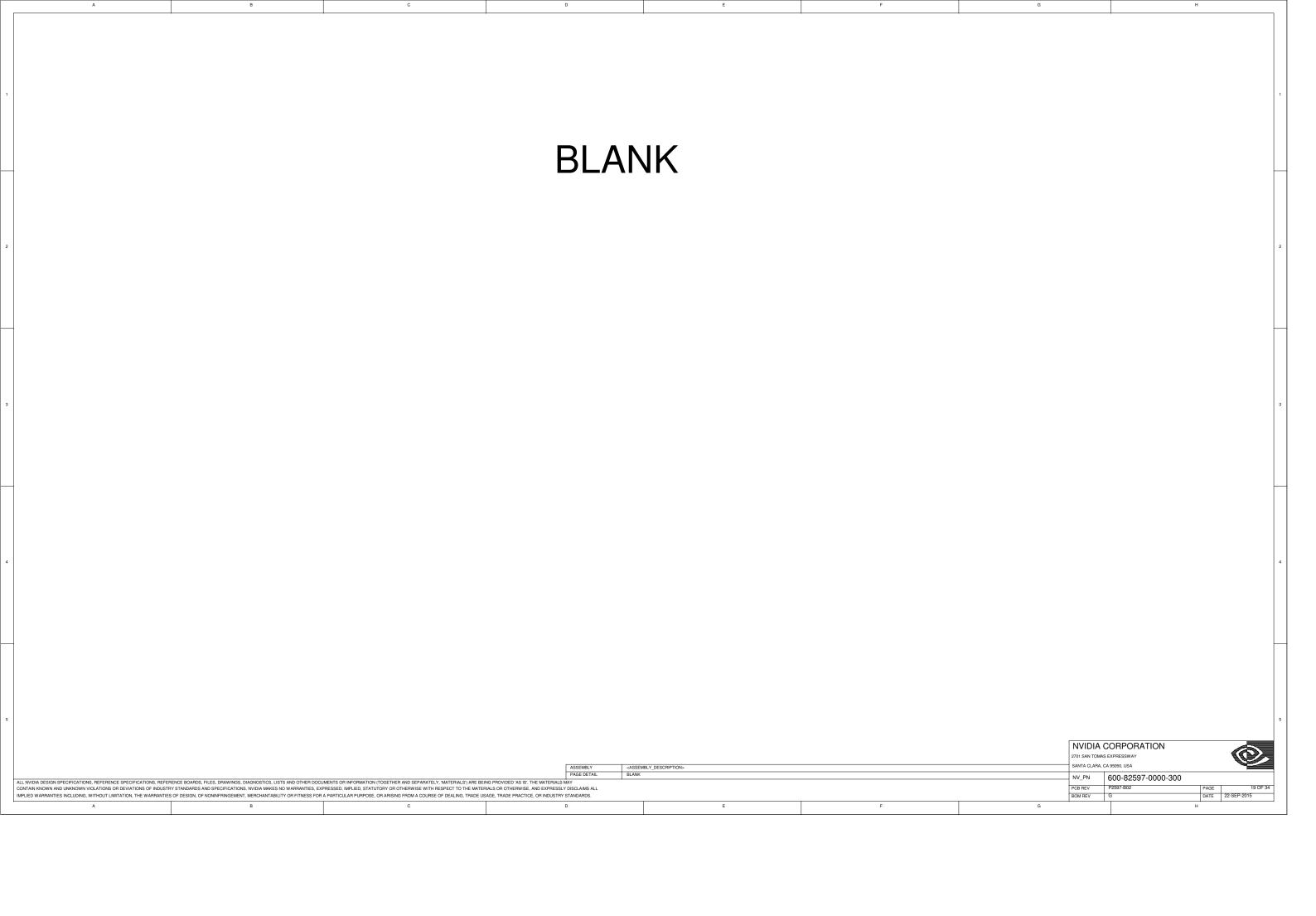


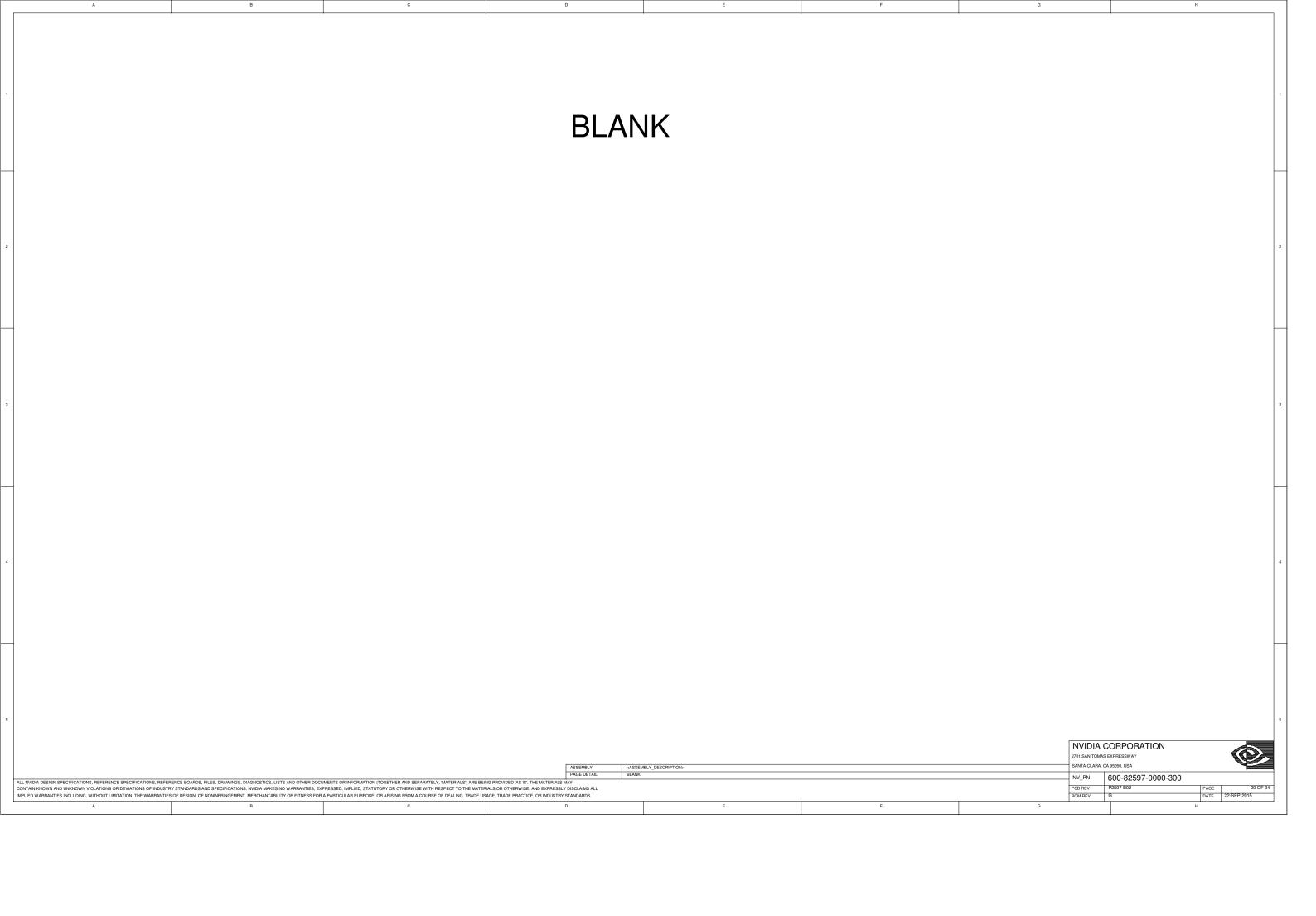


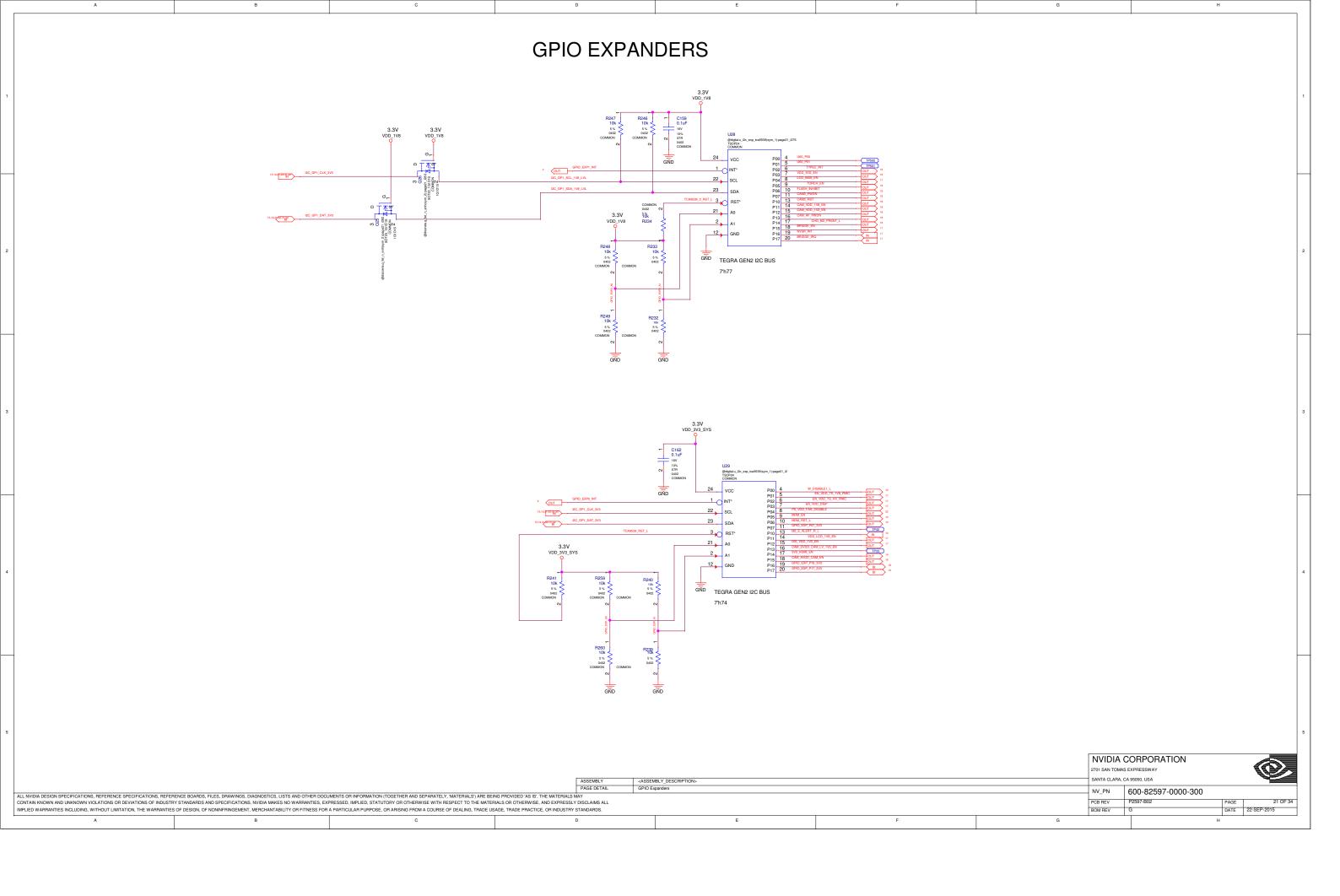


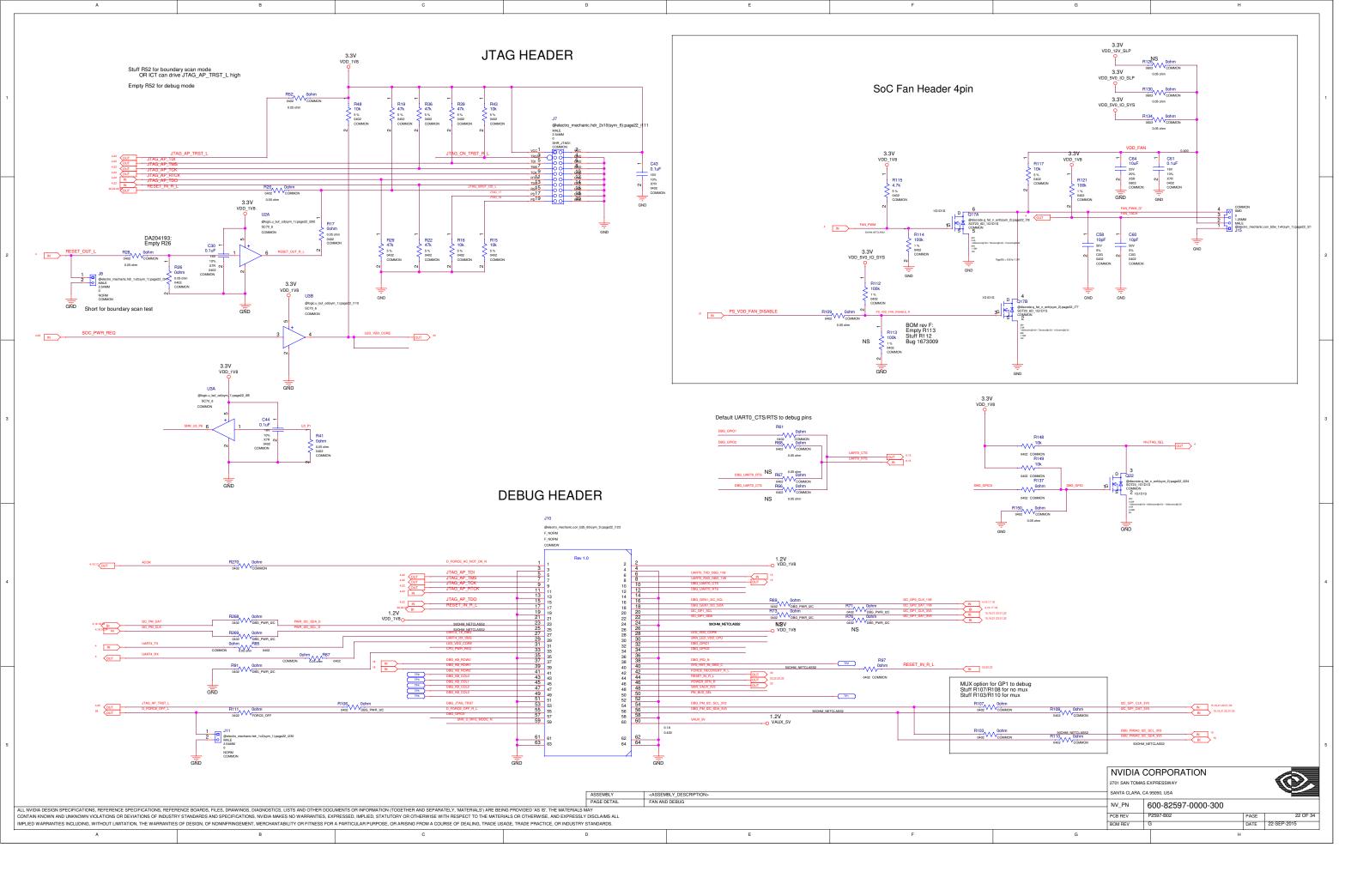


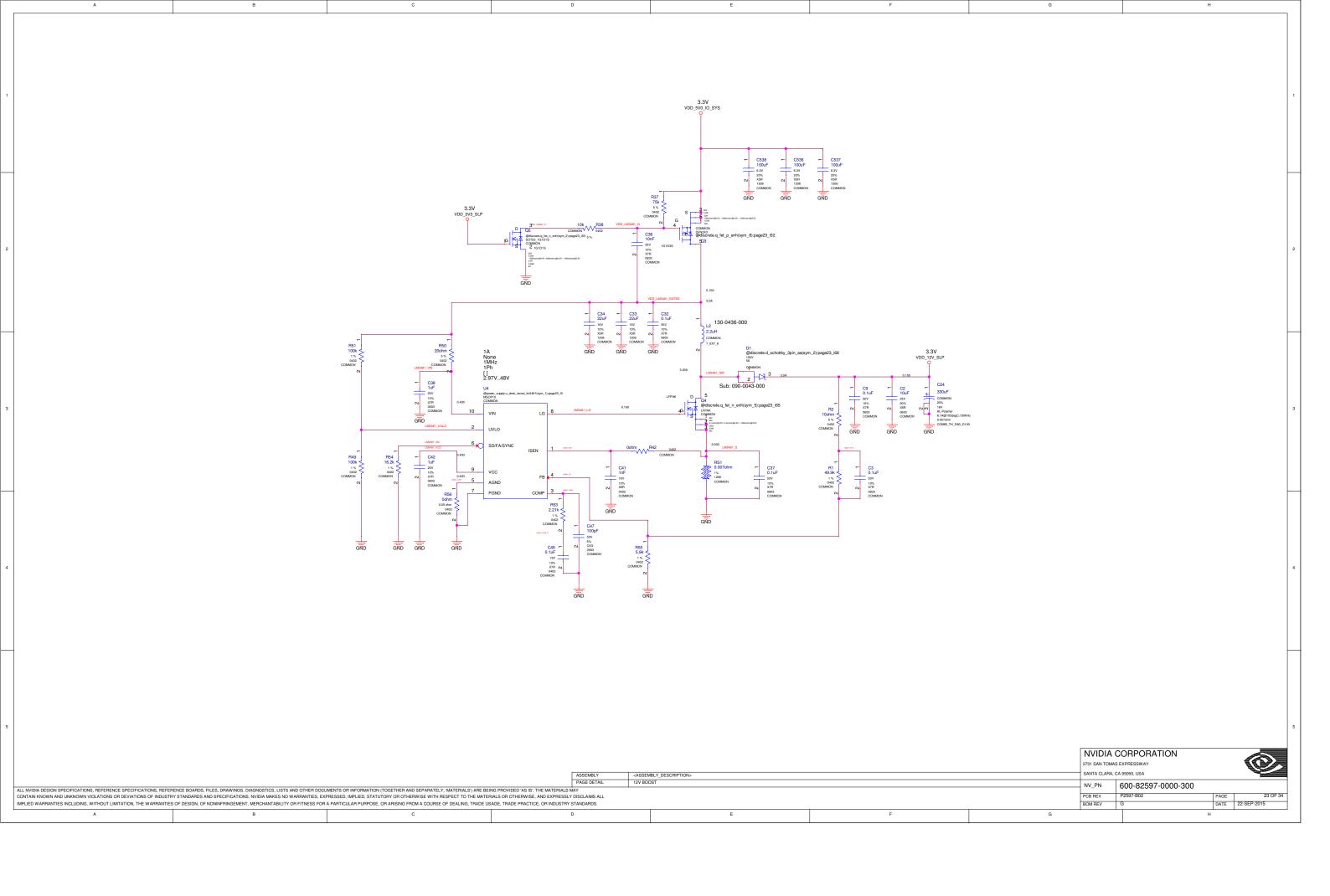


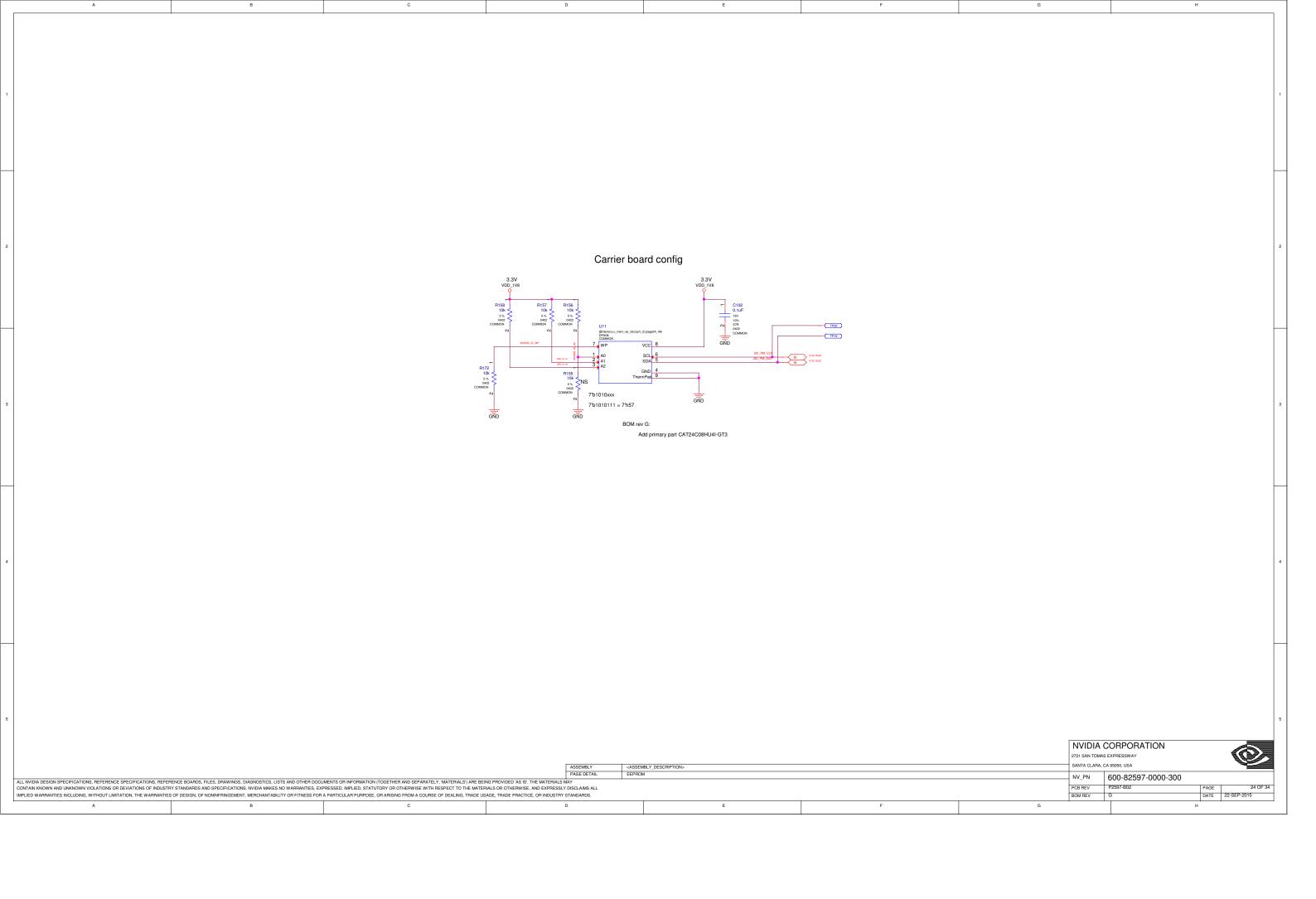


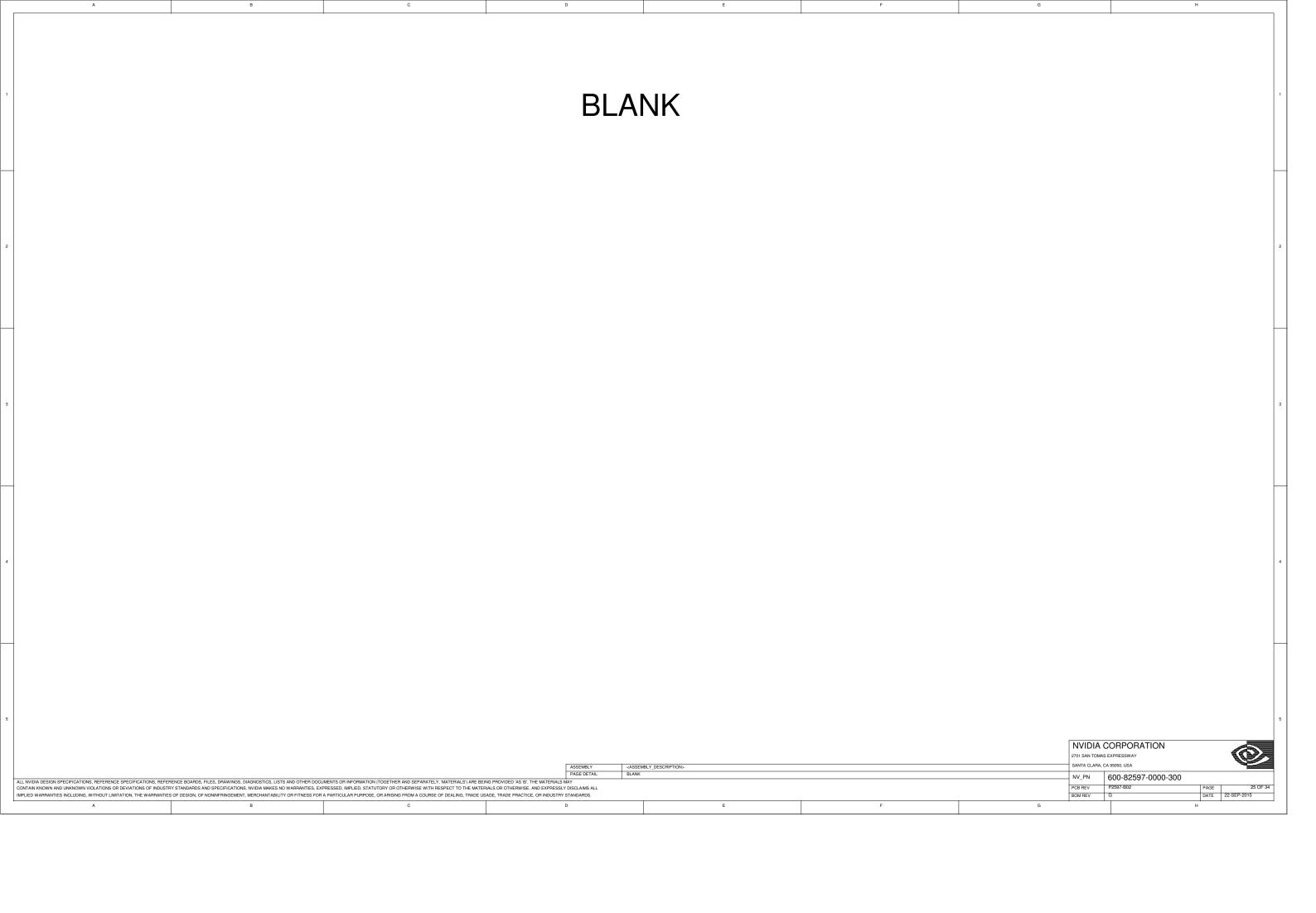


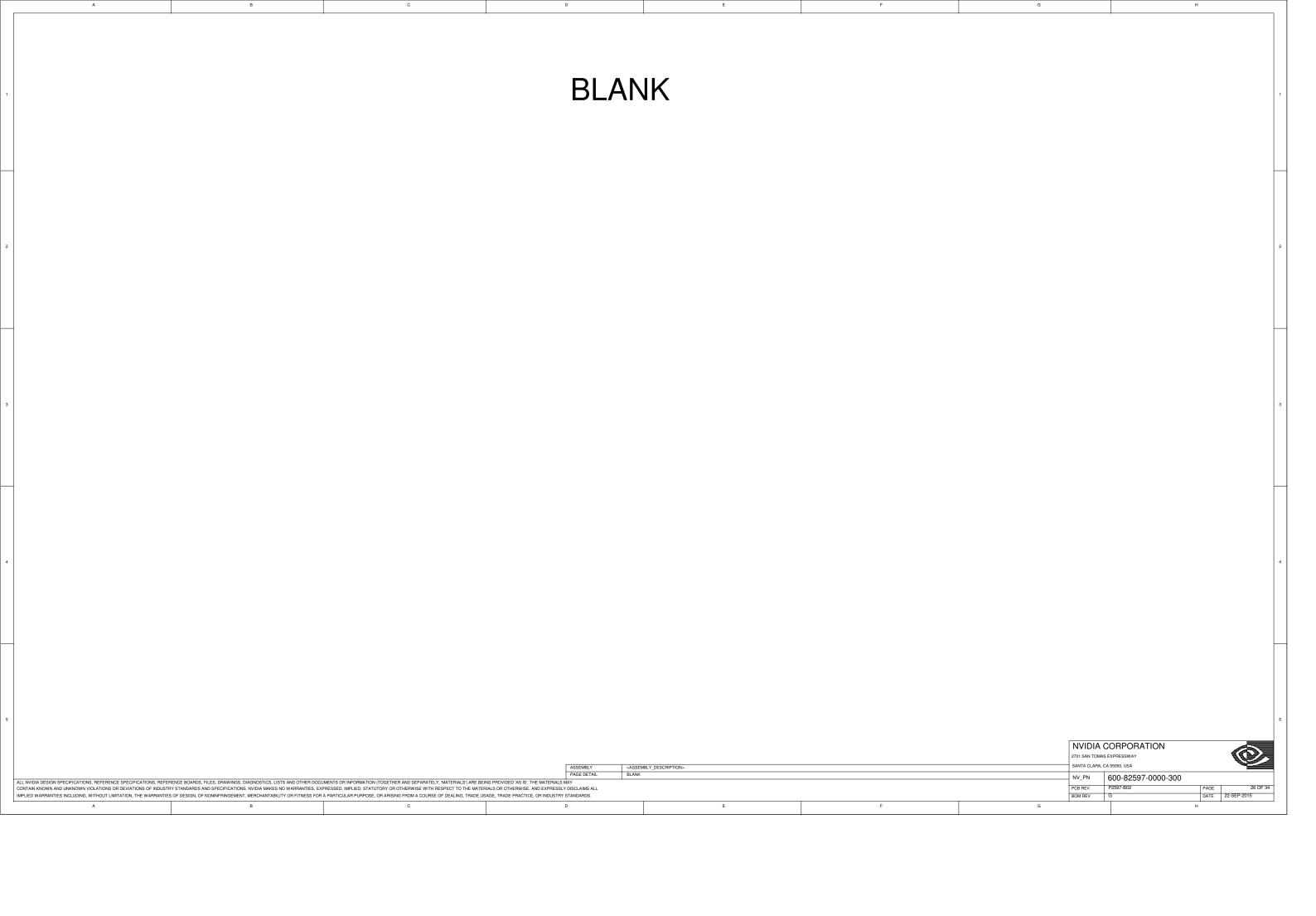


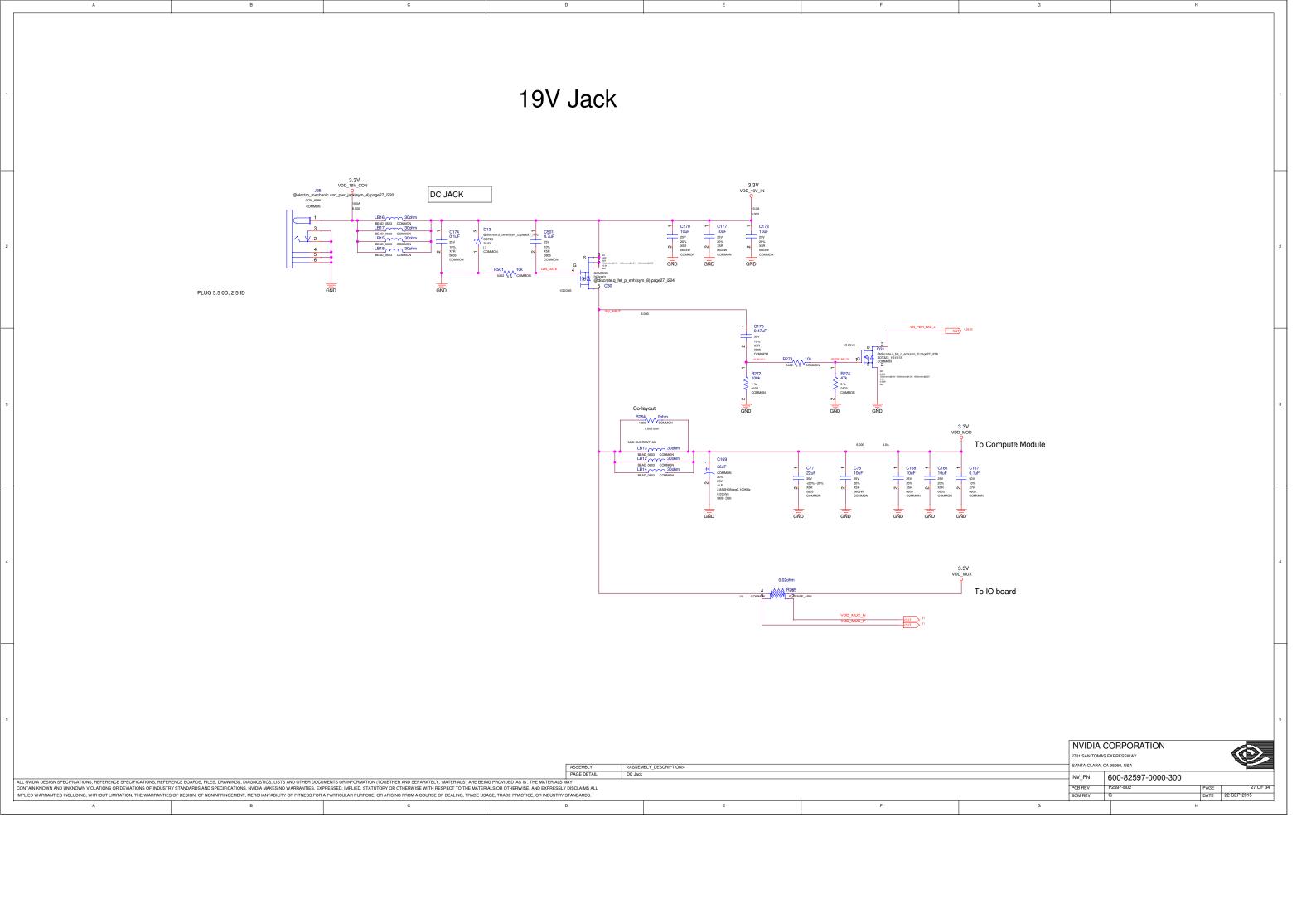


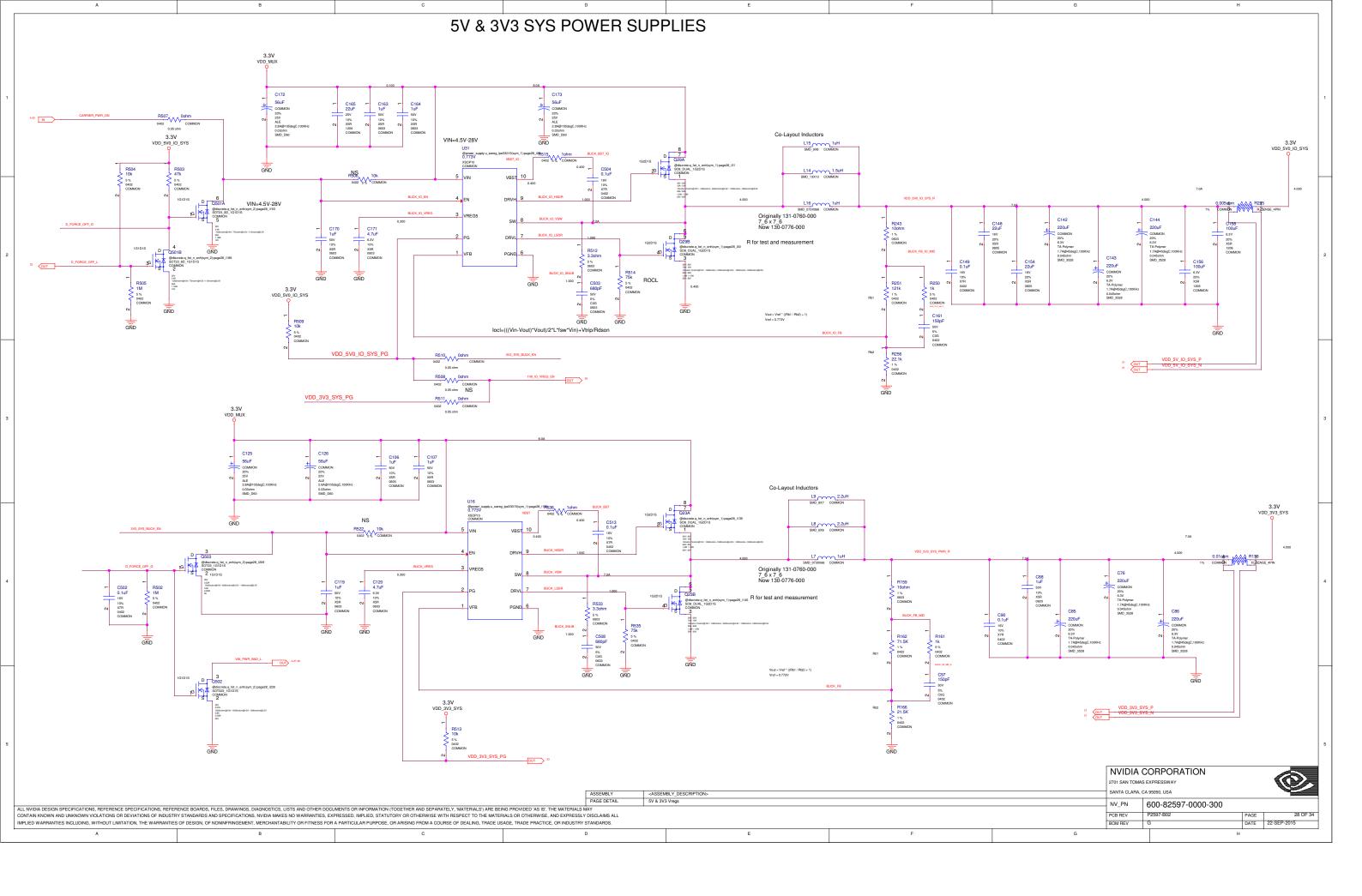


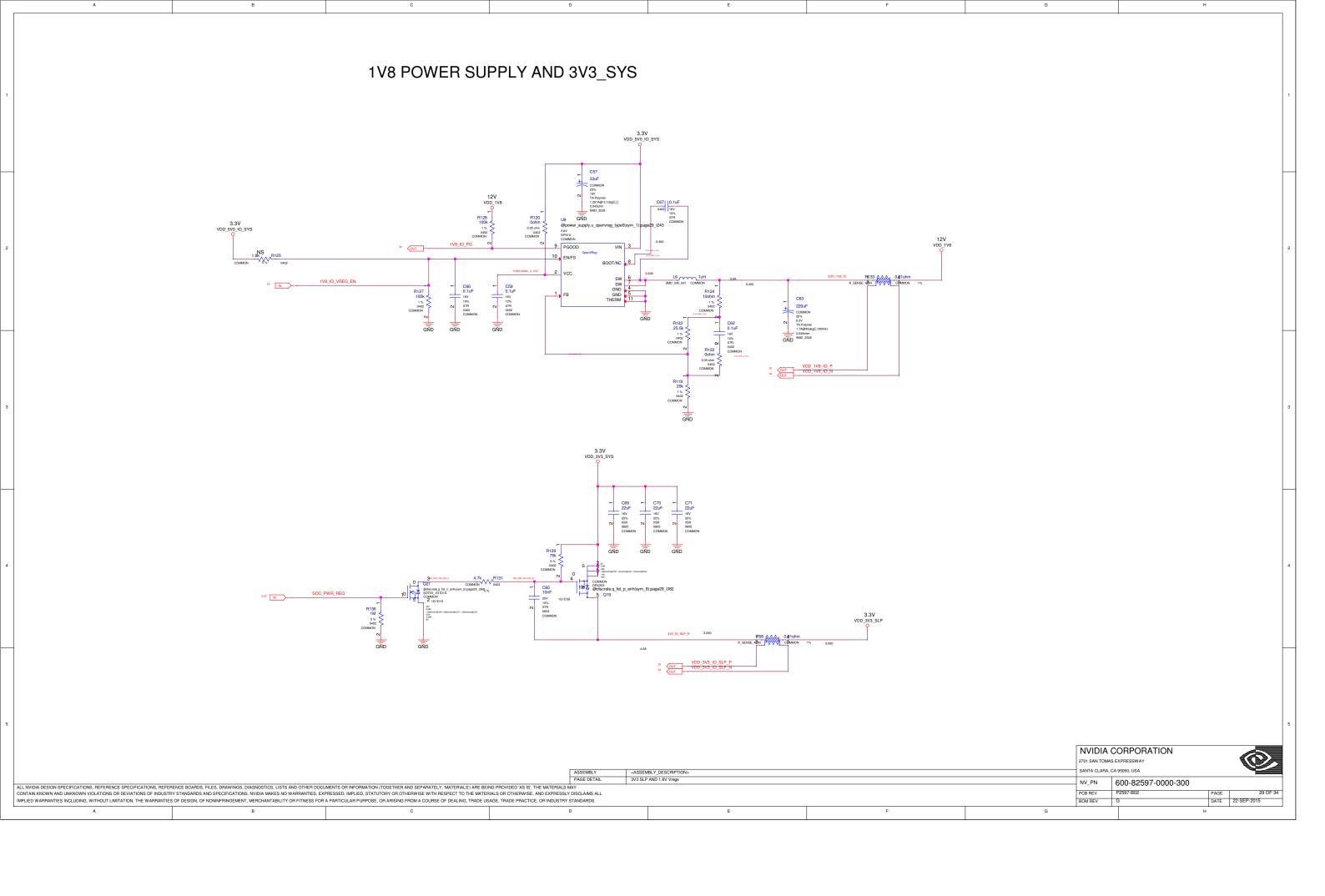


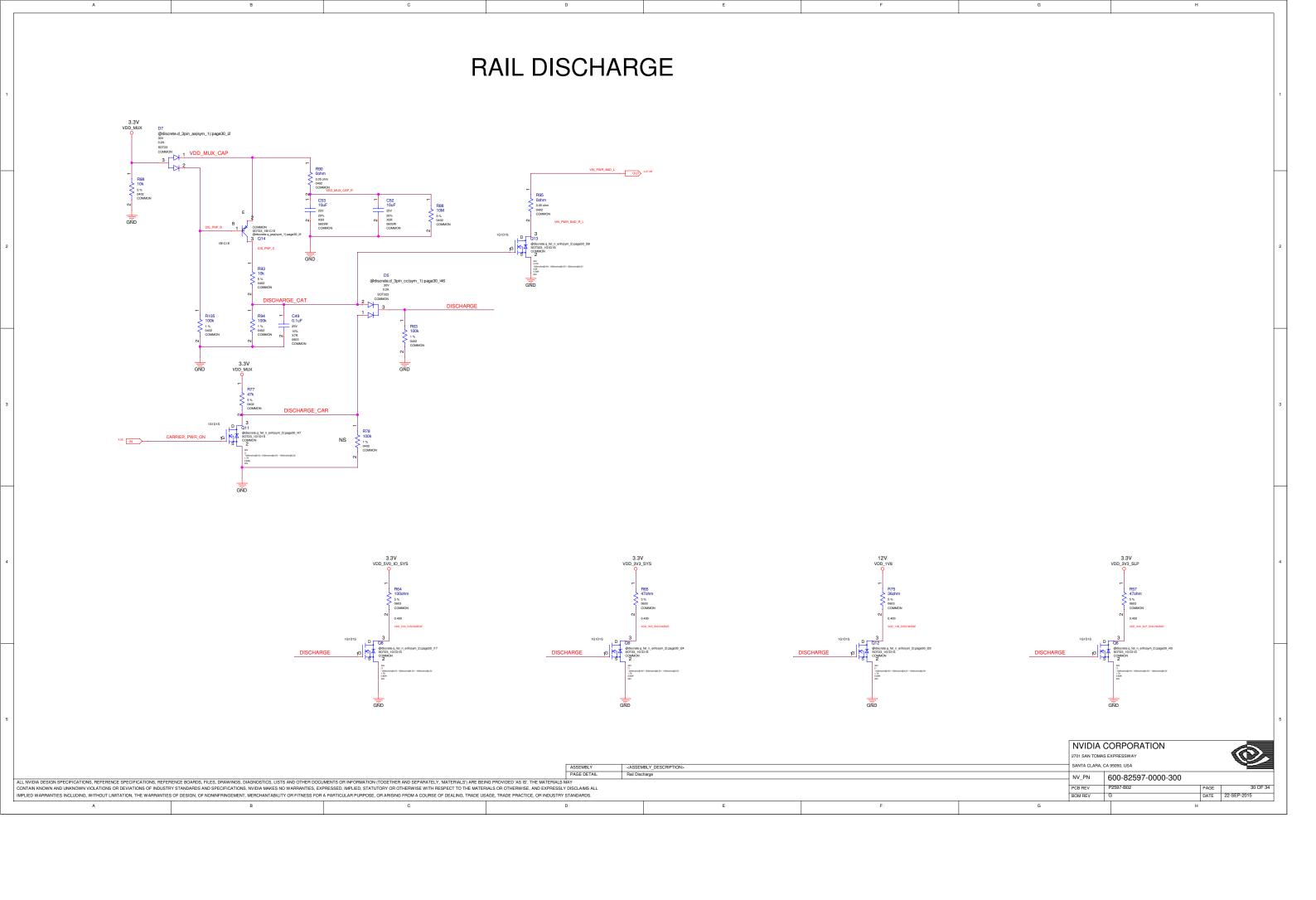


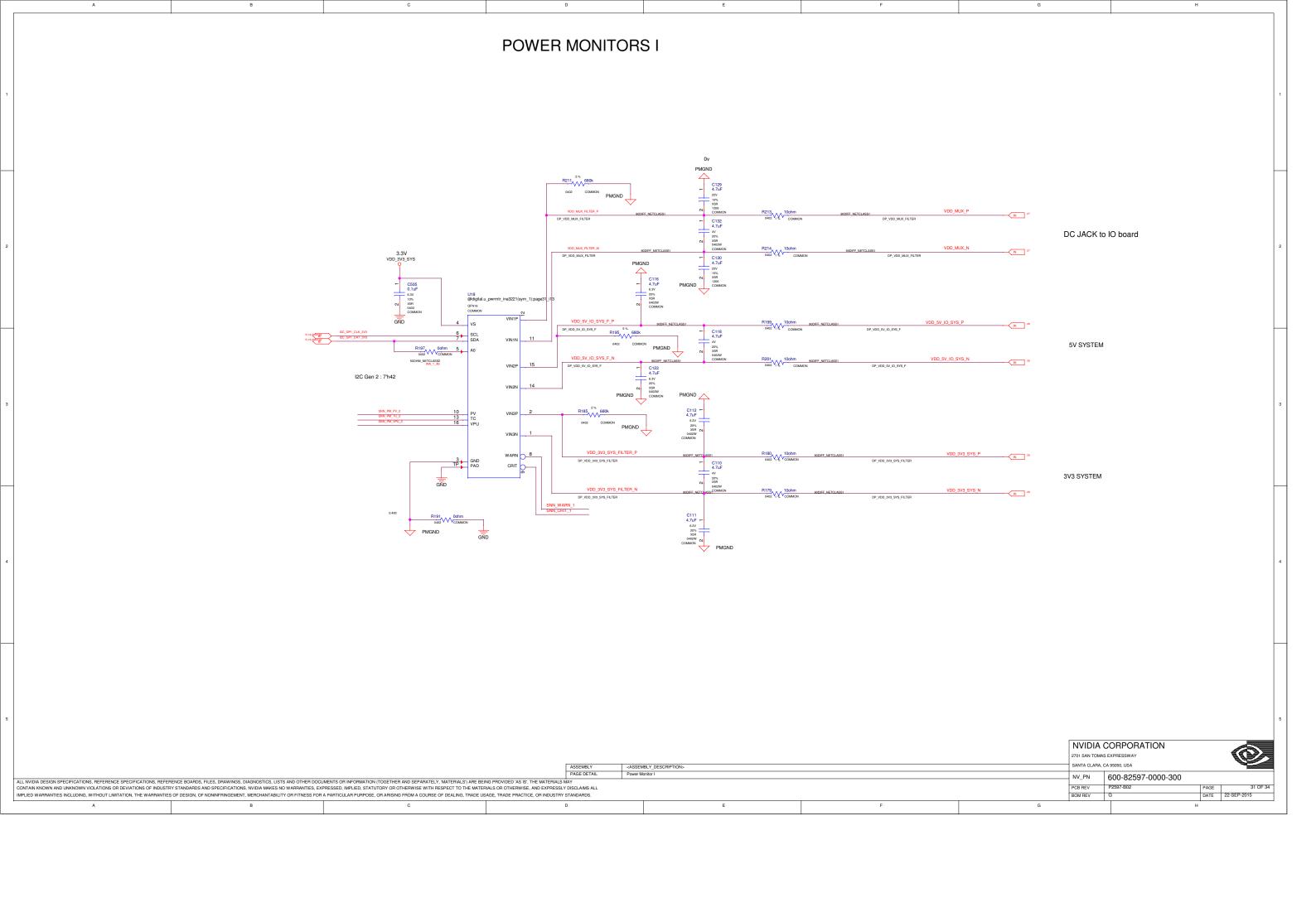


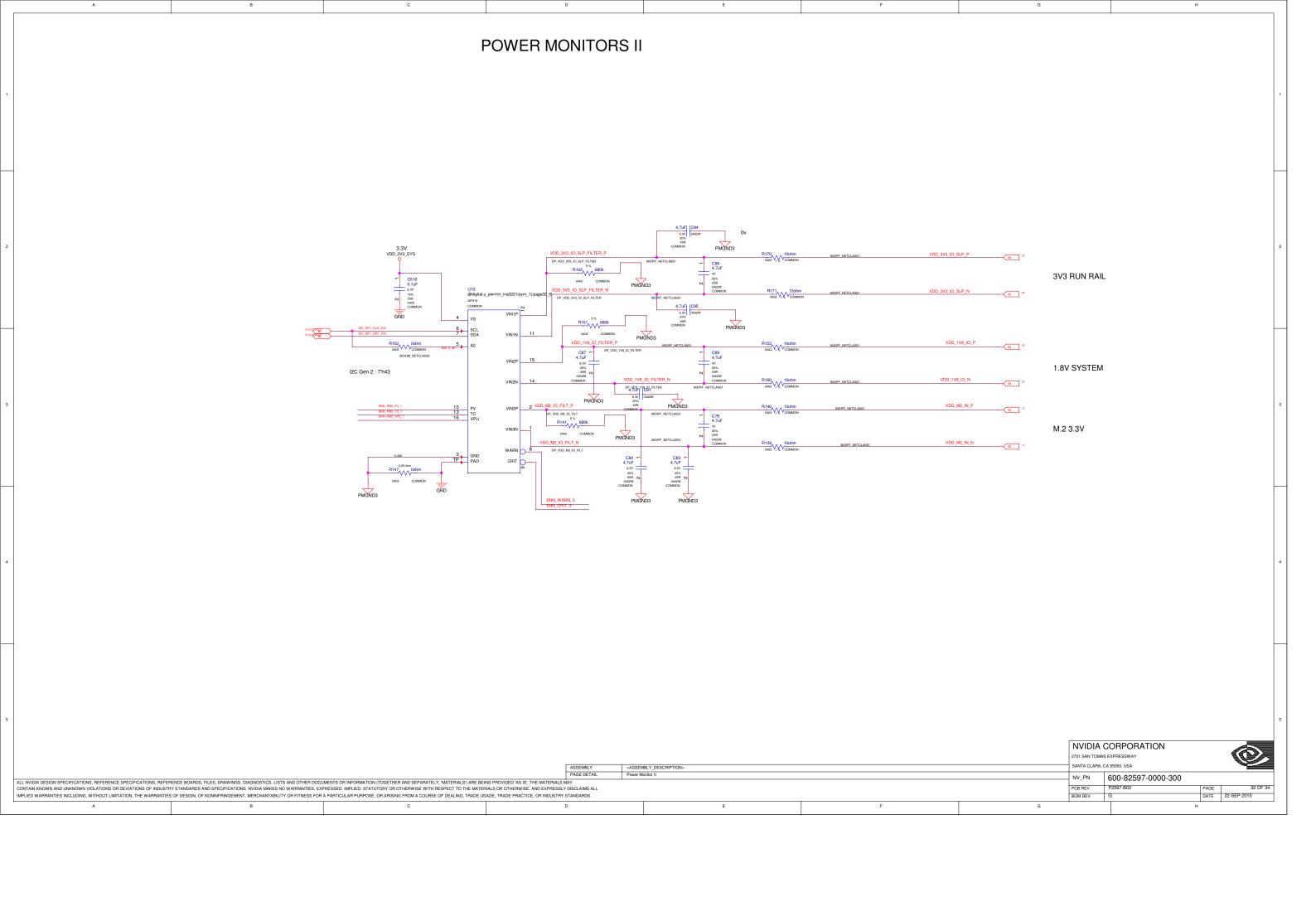


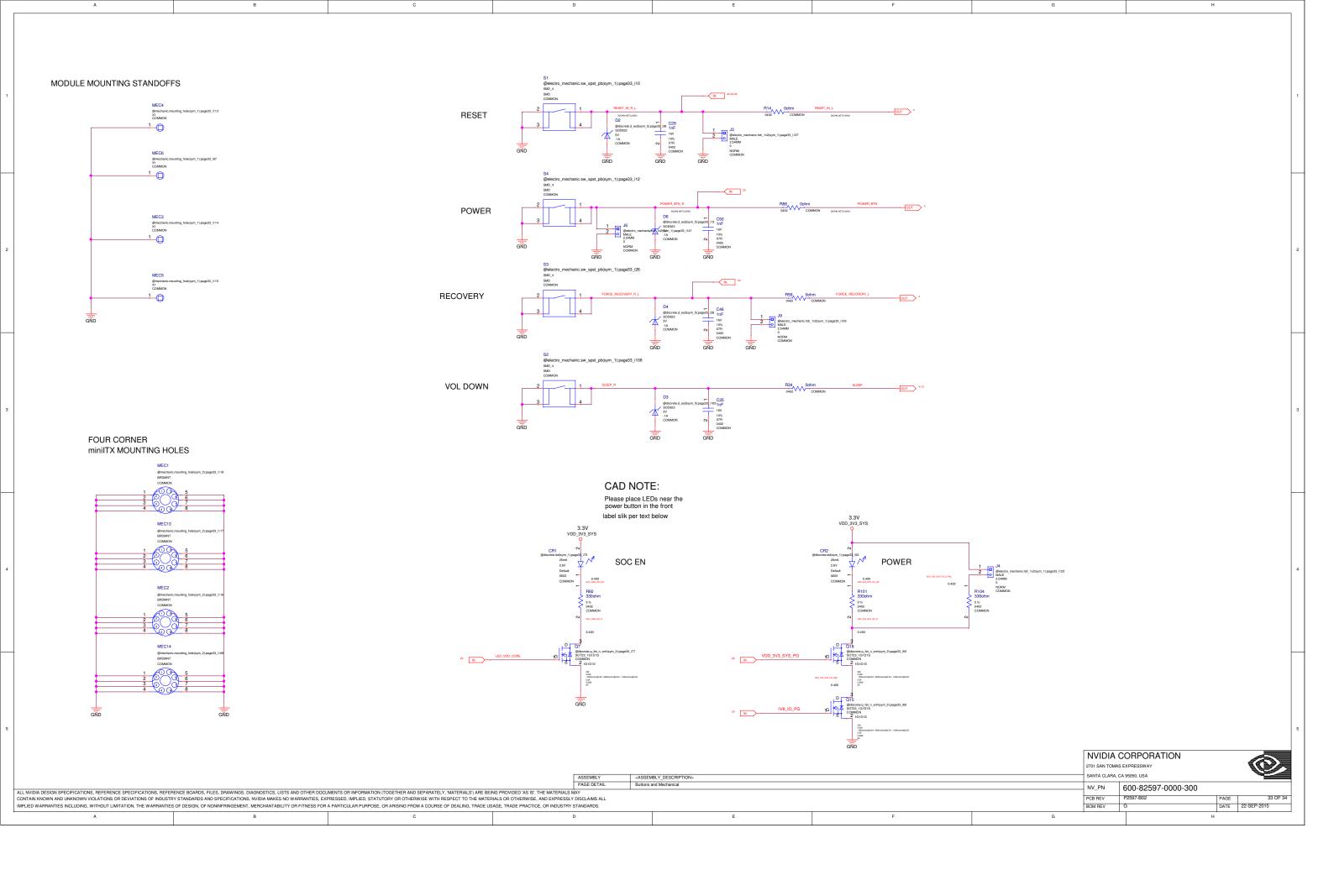












Revision History P2597-B00 BOM rev B Validation Released 5/19 BOM rev C P2597-B02 Page 12: Changed Q1 to MDV3604URH, R11 75K, R12 4.7K, C26 10nf Page 17: Stuffed U18 and emptied R200 for ST8 panel BOM rev E (DA204193) (DA203081) Page 21: Corrected text - GPIO Expanders Page 22: Empty R26 Page 22: Emptied U2, R25, R26, and C31 Page 23: Changed Q3 to MDV3604URH, R34 75K, R35 10K, C37 10nf Page 27: Changed Q28 to MDV3604URH BOM rev F Page 29: Changed Q20 to AM7321P, R132 75K, R135 4.7K, C76 10nf Page 22: Empty R113, stuff R112 (bug 1673009) Page 30: Stuffed R92 P2597-B01 BOM rev G BOM rev A Page 4: Added UART4 TX/RX to CVM connector pins D5 and D8 Page 10: Change R524 and R538 to 1k (improve margin) Page 10: Corrected PCIe RX and TX connection to M.2 connector Page 24: Add primary EEPROM (CAT24C08HU4I-GT3) Page 12: Changed Q2 to single pack FET Page 14: Added pull down to 5V0_HDMI_EN Page 15: Added a pullup option on UART3_TXD Page 16: Extensive changes to J18 and J22 Changed I2C resistor R220 and R221 to 10 ohm per EMI recommendation Page 17: Added pull down to LCD_BIAS_EN and BRIDGE_EN VDD_LCD_1V8_EN, EN_VDD_TS_HV_PMIC, EN_VDD_TS_1V8_PMIC Added pull down and buffer option to DIS_VDD_1V2_EN Page 18: Added pull down to CAM_AVDD_CAM_EN, TORCH_EN, VDD_SYS_EN CAM_VDD_1V8_EN, CAM_VDD_1V2_EN. Changed R237 to 47k stuffed Added 0 ohm stuff option to connect debug header KB ROW0 and KB ROW1 to CAM0 RST and CAM1 RST. Page 22: Added inverter and option to use DBG GPIO1 or DBG GPIO3 for NVJTAG SEL Added R354 to disconnect U2 output from RESET Page 22: Changed pins 27/29 to UART4 Page 22: Added 2pin header on FORCE OFF Page 28: populated snubber (3.3ohm/680pf cap) on 3.3V_SYS and 5V0_SYS regulators to reduce ringing Page 33: Added 2pin headers on RECOVERY and RESET BOM rev B Page 23: Changed R48 to 2.21k, C45 to 0.1uf, and C47 to 100pf (12v BOOST VR COMP) BOM DA203849 Page 27: Changed R274 to 20mohm (INA sense resistor) P2597-B02 Reference designators were resequenced Page 10: Removed unconnected backup 3.8v VR Added a pullup to M2_E_ALERT_L Page 11: Changed SDcard 47ohm FB to 10ohm for CMD/DAT and 0ohm for CLK Page 13: Changed Ethernet MDI route to 95ohm Page 14: Changed R560, R572 to 0ohm (DA204127/DA204138, bug 200128580) Page 15: Added a mux on I2C_GEN1 for PM342 DBG_I2C Page 19: Removed empty sensors Page 22: Added a header on RESET_OUT_L for bug 1651476 Added debug option (default) to route DBG_GPIO1 to UART0_CTS and DBG_GPIO2 to UART0_RTS at debug header per bug 1664555 Changed R109 PU to VDD_5V0_IO_SLP. Added option to run the fan from always on 5v Page 24: Removed empty proximity sensor Page 28: Changed 5v and 3.3v VR input and output MLCC caps to OS CONs and tantalums to reduce audible noise Changed FORCE_OFF implementation to work without PM342. Added 0.1uf on D_FORCE_OFF_G. Connected R505 and R503 to VDD_5V0_IO_SYS. Changed R503 to 47k and added 0.1uf on D_FORCE_OFF_G. Page 29: Changed 1.8v VR input and output caps to tantalums to reduce audible noise Page 31: Changed all INA series resistors to 10ohm, added 680k PD on _P to compensate for _N leakage Page 32: Changed all INA series resistors to 10ohm, added 680k PD on _P to compensate for _N leakage PAGE DETAIL REVISION HISTORY ALL INVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY
CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL
MPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWA SANTA CLARA CA 95050 LISA 600-82597-0000-300 NV PN

PCB REV DATE 22-SEP-2015 BOM REV