SPECIFICATION

NVIDIA Jetson TX1 Developer Kit Carrier Board Specification

Abstract

This document contains recommendations and guidelines for Engineers to follow to create modules for the expansion connectors on the Jetson TX1 carrier board as well as understand the capabilities of the other dedicated interface connectors and associated power solutions on the platform.

Document Change History

Date	Description
NOV, 2015	Release

NVIDIA

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1.0 INTRODUCTION

The NVIDIA® Jetson TX1 carrier board is ideal for software development within the Linux environment. Standard connectors are used to access Jetson TX1 features and interfaces, enabling a highly flexible and extensible development platform. Go to http://developer.nvidia.com/jetson-tx1 or contact your NVIDIA representative for access to software updates and the developer SDK supporting the OS image and host development platform that you want to use. The developer SDK includes an OS image that you will load onto your Jetson TX1 device, supporting documentation, and code samples to help you get started.

1.1 JETSON TX1 Feature List

CPU/GPU
- Quad-core Cortex-A57 complex
- NVIDIA Maxwell architecture GPU

Memory
- 4GB LPDDR4-3200
- 16GB eMMC 5.1

Multimedia
- Ultra low-power audio processor
- Multi-standard Video/JPEG Decoder/Encoder

Image-signal processor

Connectivity
- BCM4354 w/ dual U.FL RF connectors: Connects to 802.11ac Wi-Fi and Bluetooth enabled devices.

Network
- 10/100/1000BASE-T Ethernet

Advanced power management
- Dynamic voltage and frequency scaling
- Multiple clock and power domains
- Thermal Transfer Plate & optional Fan/Heatsink

1.2 Carrier Board Feature List

Connection to Jetson TX1
- 400-pin (8x50) Board-Board Connector

Storage
- Full Size SD Card Slot
- SATA Connector (Power & TX/RX)

USB
- USB 3.0 Type A + USB 2.0 Micro AB

Network
- Gigabit Ethernet (RJ45 Connector w/LEDs)

PCIe
- Standard PCIe x4 connector

Display/Touch Expansion Header
- DSI (2x4 lanes), eDP x4 Lanes
- Backlight PWM/Control
- Touch: SPI/I2C

HDMI Type A

Camera Expansion Header
- CSI: 6, x2 – 3, x4
- Camera CLK, I2C & Control
- I2S, UART, SPI

M.2 Key E Connector
- PCIe x1 Lane, SDIO, USB 2.0
- I2S, UART, I2C
- Control

Expansion Header
- I2C, SPI, UART
- I2S, D-MIC, Audio Clock & Control

UI & Indicators
- Power, Reset & Force Recovery Buttons
- Power & SOC Enable LEDs

Debug/Serial
- JTAG Connector (Standard 20-pin header)
- Debug Connector (60-pin Board-Board)
  - JTAG, UART, I2C
  - Power, Reset & Force Recovery
- Serial Port Signals (1x6 header)

Miscellaneous
- Fan Connector: 5V, PWM & Tach

Power
- DC Jack: 5.5V-19.6V
- Main 3.3V/5V Supplies: 2xTPS53015
- Main 1.8V Supply: APW8805
- USB VBUS Supplies: RT9715 & APL3511
- 12V for PCIe & SATA: LM3481
- Load Switches/LDOs
- Charge Control Header: 10-pin Flex Receptacle

1.3 Jetson TX1 Carrier Board Block Diagram

Figure 1. Jetson TX1 Block Diagram

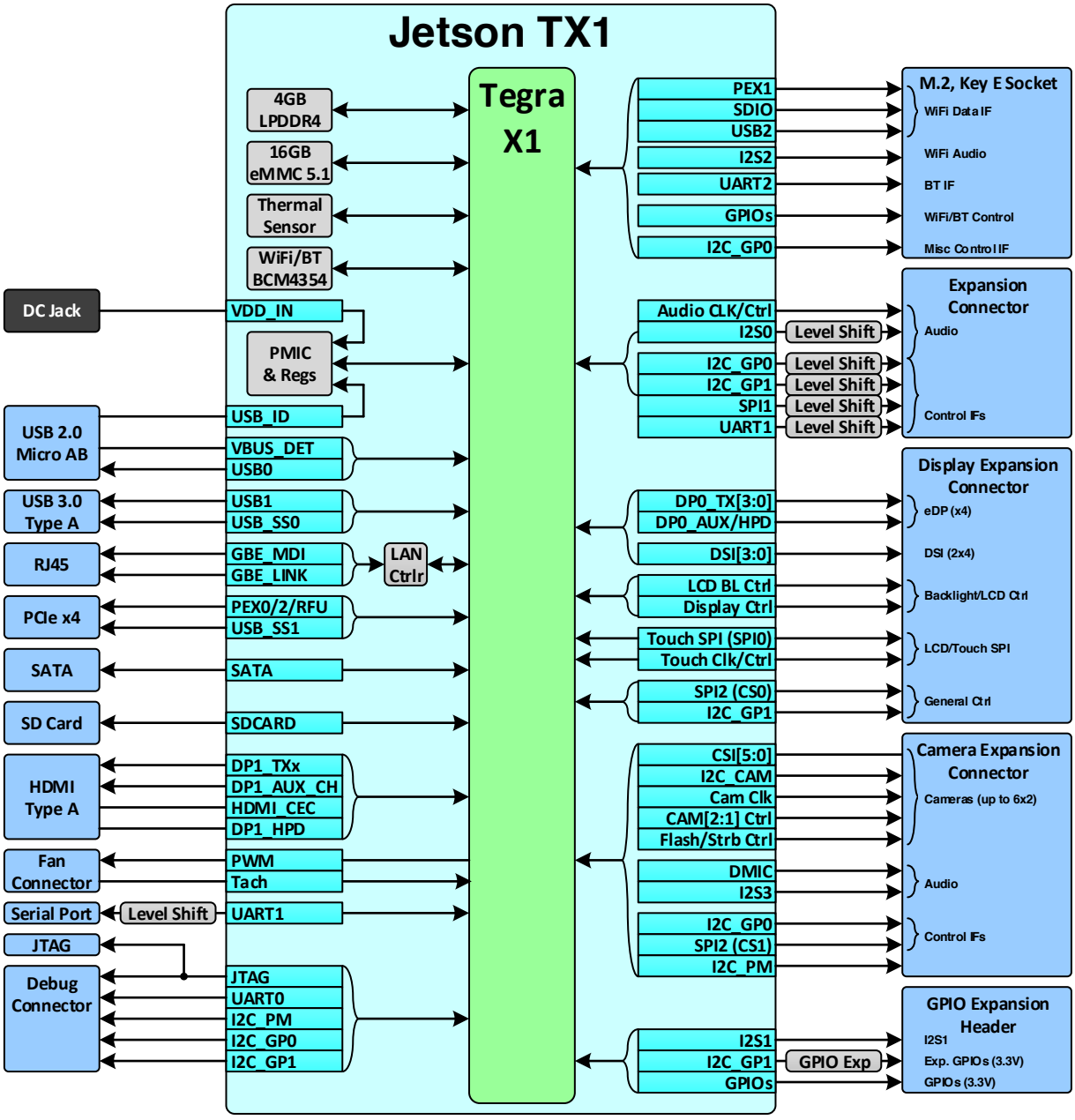


Figure 2. Jetson TX1 Placement (Top View)

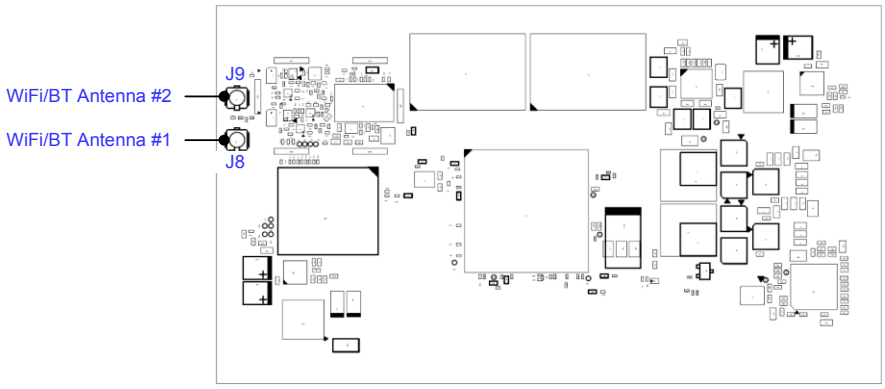
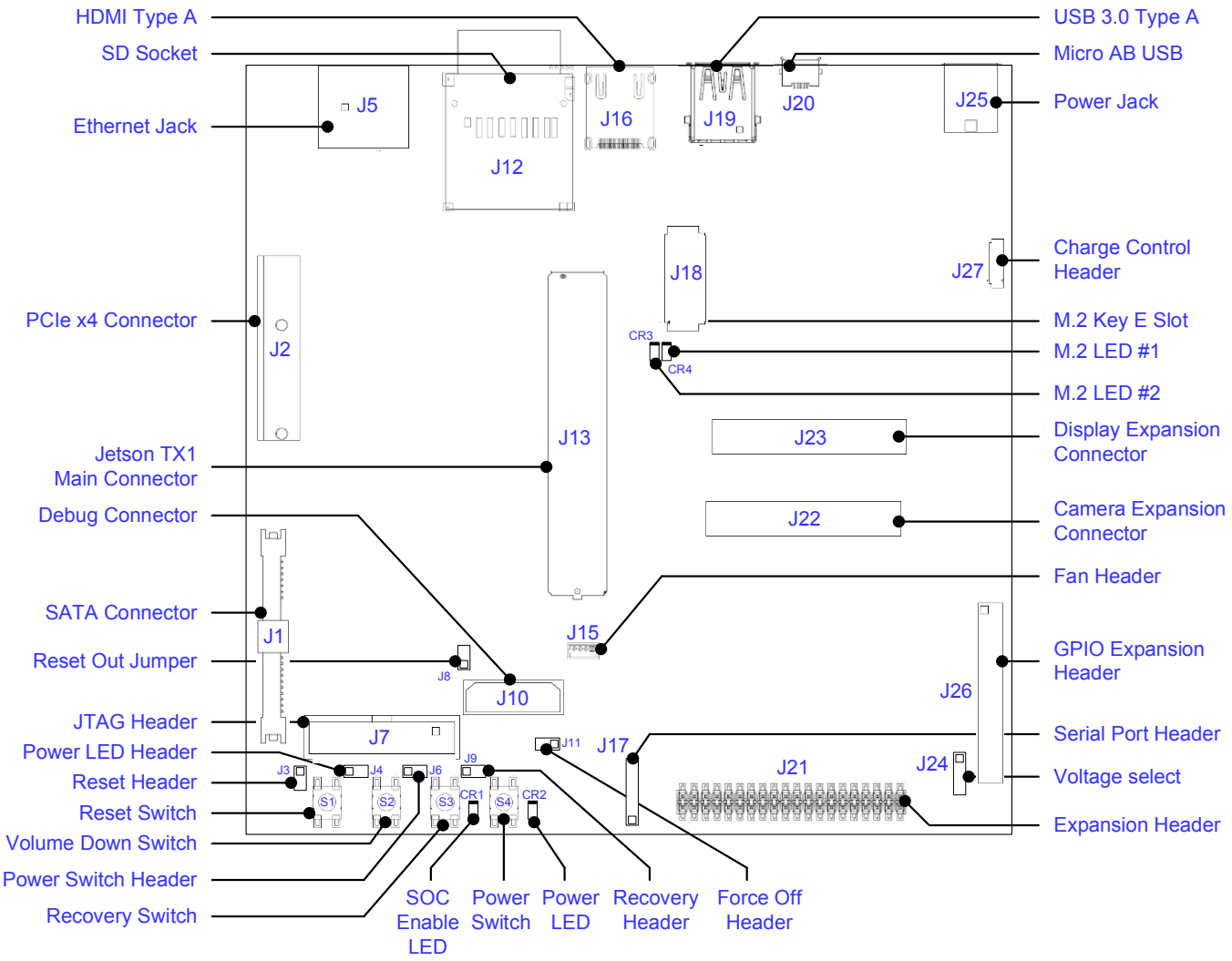


Figure 3. Jetson TX1 Carrier Board Placement (Top View)



J1	SATA Connector (22-pin Including Power)
J2	PCIe x4 Connector
J3	Reset Switch Header (1x2, 2.54mm pitch)
J4	Power LED Header (1x2, 2.54mm pitch)
J5	RJ45 Ethernet Jack
J6	Power Switch Header (1x2, 2.54mm pitch)
J7	JTAG Header (2x10, 2.54mm pitch)
J8	Reset Out Header (1x2, 2.54mm pitch)
J9	Force Recovery Header (1x2, 2.54mm pitch)
J10	Debug Connector (2x30, 0.5mm pitch)
J11	Force Off Header (1x2, 2.54mm pitch)
J12	SD Socket (Full Size)
J13	Jetson TX1 Connector (8x50, 1.27mm pitch)
J14	Reserved
J15	Fan Header (4-pin, 1.25mm pitch)
J16	HDMI Type A
J17	Serial Port Header (1x6, 2.54mm pitch)
J18	M.2 Key E Connectivity Socket (75-pin)
J19	USB 3.0 Type A
J20	Micro AB USB
J21	Expansion Header (2x20, 2.54mm pitch)
J22	Camera Expansion Connector (2x60, 0.5mm pitch)
J23	Display Expansion Connector (2x60, 0.5mm pitch)
J24	Voltage select for SPI1/I2C_GP0 Level Shifter
J25	Power Jack
J26	GPIO Expansion Header (2x15, 2.54mm pitch)
J27	Charge Control Header (10-pin Flex Recep., 0.8mm pitch)
S1	Reset Switch
S2	Volume Down Switch
S3	Recovery Switch
S4	Power Switch
CR1	SOC Enable LED (Green)
CR2	Power LED (Green)
CR3	M.2 LED #2 (Green)
CR4	M.2 LED #1 (Green)

2.0 JETSON TX1 CARRIER BOARD STANDARD CONNECTORS

The Jetson TX1 carrier board provides a number of connectors with industry standard pinouts to support additional functionality beyond what is integrated on the main platform board. This includes:

- USB 2.0: Micro AB Connector
- USB 3.0: Type A Connector
- Gigabit Ethernet: RJ45 Connector
- SATA: Standard SATA Connector, 22-pin including power
- SD Card (Full size) Connector/Cage
- HDMI: Type A Connector
- M.2, Key E Socket
- PCIe x4 Connector
- JTAG header, 2x10, 2.54mm pitch

2.1 USB Ports

The carrier board supports two USB Connectors. One is a USB 2.0 Micro AB connector (J20) supporting Device/Host modes as well as USB Recovery mode. The other is a USB 3.0 Type A connector (J19) supporting Host mode only.

Figure 4. USB Port Connections

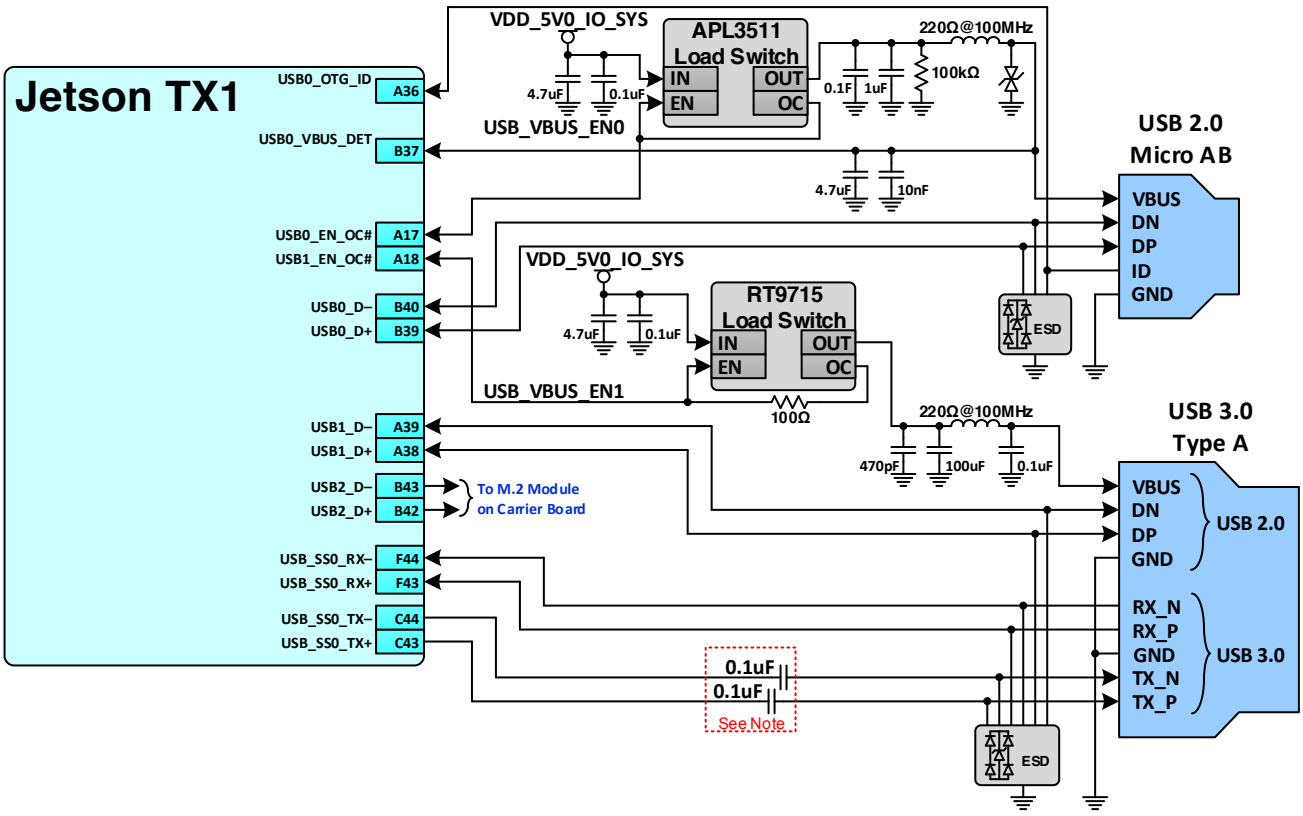


Table 1. USB 2.0 Micro AB & USB 3.0 Type A Connector Pin Descriptions

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default
USB 2.0 Micro AB				
1	VBUS	–	VBUS Supply	Power
2	USB0_IO_CONN_D_N	USB0_D–	USB 2.0 #0 Data -	Bidir
3	USB0_IO_CONN_D_P	USB0_D+	USB 2.0 #0 Data +	Bidir
4	USB0_ID_IO_CONN	USB0_OTG_ID	USB 2.0 #0 Identification	Input
5	GND	–	Ground	Ground
USB 3.0 Type A				
1	VBUS	–	VBUS Supply	Power
2	USB1_D_N	USB1_D–	USB 2.0 #1 Data -	Bidir
3	USB1_D_P	USB1_D+	USB 2.0 #1 Data +	Bidir
4	GND	–	Ground	Ground
5	USB3_RX1_N	USB_SS0_RX–	USB 3.0 #0 Receive -	Input
6	USB3_RX1_P	USB_SS0_RX+	USB 3.0 #0 Receive +	Input
7	GND	–	Ground	Ground
8	USB3_TX1_N	USB_SS0_TX–	USB 3.0 #0 Transmit -	Output
9	USB3_TX1_P	USB_SS0_TX+	USB 3.0 #0 Transmit +	Output

Notes: In the Type/Dir column, Output is to USB Connectors. Input is from USB Connectors. Bidir is for Bidirectional signals.

2.2 Gigabit Ethernet

The carrier board implements an RJ45 connector (J5) along with the necessary magnetics device.

Figure 5. Gigabit Ethernet Connections

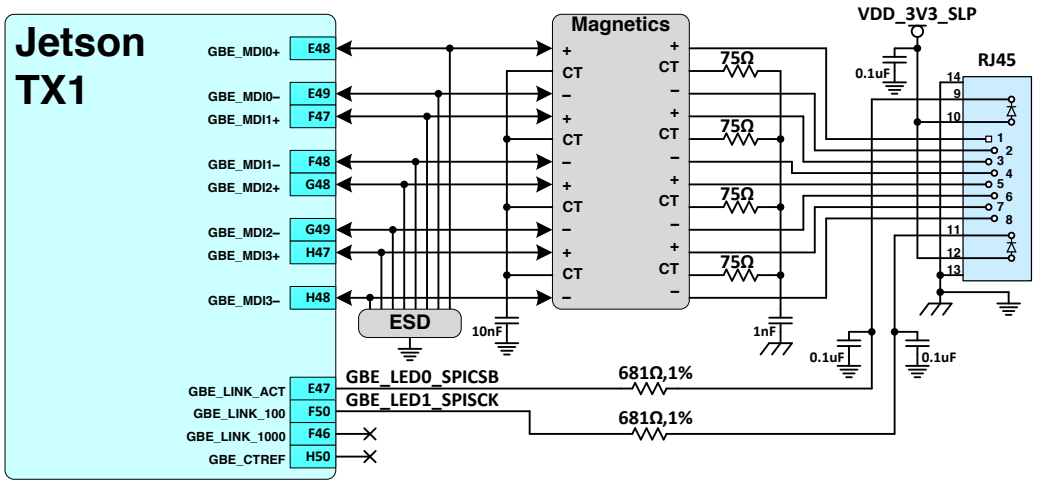


Table 2. Ethernet RJ45 Connector Pin Descriptions

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default
1	RJ45_TDP	GPE_MDI0+	Gigabit Ethernet MDI 0+	Bidir
2	RJ45_TDN	GPE_MDI0–	Gigabit Ethernet MDI 0-	Bidir
3	RJ45_RDP	GPE_MDI1+	Gigabit Ethernet MDI 1+	Bidir
4	RJ45_RDN	GPE_MDI1–	Gigabit Ethernet MDI 1-	Bidir
5	RJ45_TDP1	GPE_MDI2+	Gigabit Ethernet MDI 2+	Bidir
6	RJ45_TDN1	GPE_MDI2–	Gigabit Ethernet MDI 2-	Bidir
7	RJ45_RDP1	GPE_MDI3+	Gigabit Ethernet MDI 3+	Bidir
8	RJ45_RDN1	GPE_MDI3–	Gigabit Ethernet MDI 3-	Bidir

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default
9	GBE_LED0_SPICSB	GBE_LINK_ACT	Connected to LED #1 through resistor	Output OD
10	LED1A	–	Connected to VDD_3V3_SYS	–
11	GBE_LED1_SPISCK	GBE_LINK100	Connected to LED #2 through resistor	Output OD
12	LED2A	–	Connected to VDD_3V3_SYS	–
13	NC/GND	–	Ground	Ground
14	NC/GND	–	Ground	Ground

Notes: In the Type/Dir column, Output is to RJ45 Connector. Input is from RJ45 Connector. Bidir is for Bidirectional signals.

2.3 SATA

The Jetson TX1 carrier board has a standard SATA connector (J1 - both Data & Power) as shown below.

Figure 6. SATA Connections

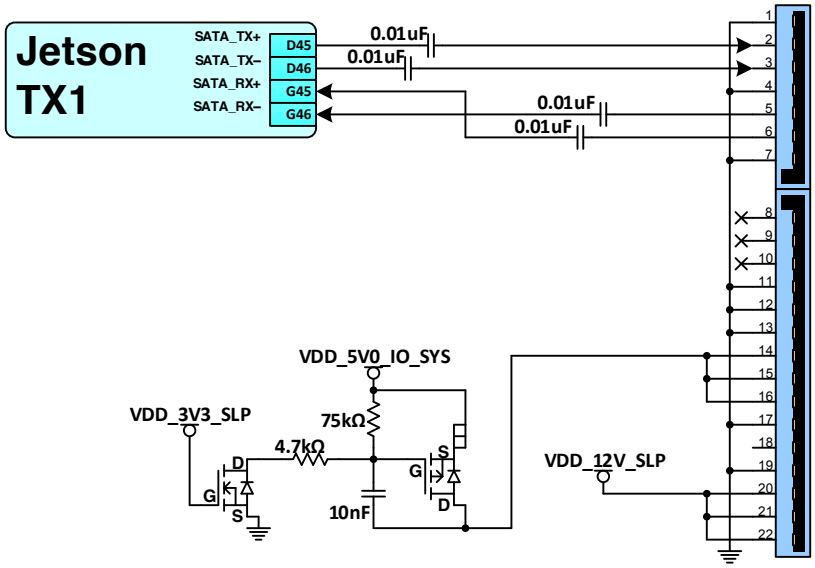


Table 3. SATA Connector Pin Descriptions

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir	Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir
1	GND	–	Ground	Ground	8	NC	–	Unused	Unused
2	SATA_TX_C_P	SATA_TX+	SATA Transmit+	Output	9	NC	–	Unused	Unused
3	SATA_TX_C_N	SATA_TX–	SATA Transmit–	Output	10	NC	–	Unused	Unused
4	GND	–	Ground	Ground	11	GND	–	Ground	Ground
5	SATA_RX_C_N	SATA_RX–	SATA Receive–	Input	12	GND	–	Ground	Ground
6	SATA_RX_C_P	SATA_RX+	SATA Receive+	Input	13	GND	–	Ground	Ground
7	GND	–	Ground	Ground	14	VDD_5V0_IO_SLP	–	Gated version of Main 5.0V Supply	Power
					15	VDD_5V0_IO_SLP	–		Power
					16	VDD_5V0_IO_SLP	–		Power
					17	GND	–	Ground	Ground
					18	NC	–	Unused	Unused
					19	GND	–	Ground	Ground
					20	VDD_12V_SLP	–	12V Supply (From Boost on carrier board)	Power
					21	VDD_12V_SLP	–		Power
					22	VDD_12V_SLP	–		Power

Notes: In the Type/Dir column, Output is to SATA Connector. Input is from SATA Connector. Bidir is for Bidirectional signals.

2.4 SD Card

A full size SD Card (J12) is implemented, supporting up to SDR104 mode (UHS-1).

Figure 7. SD Card Connections

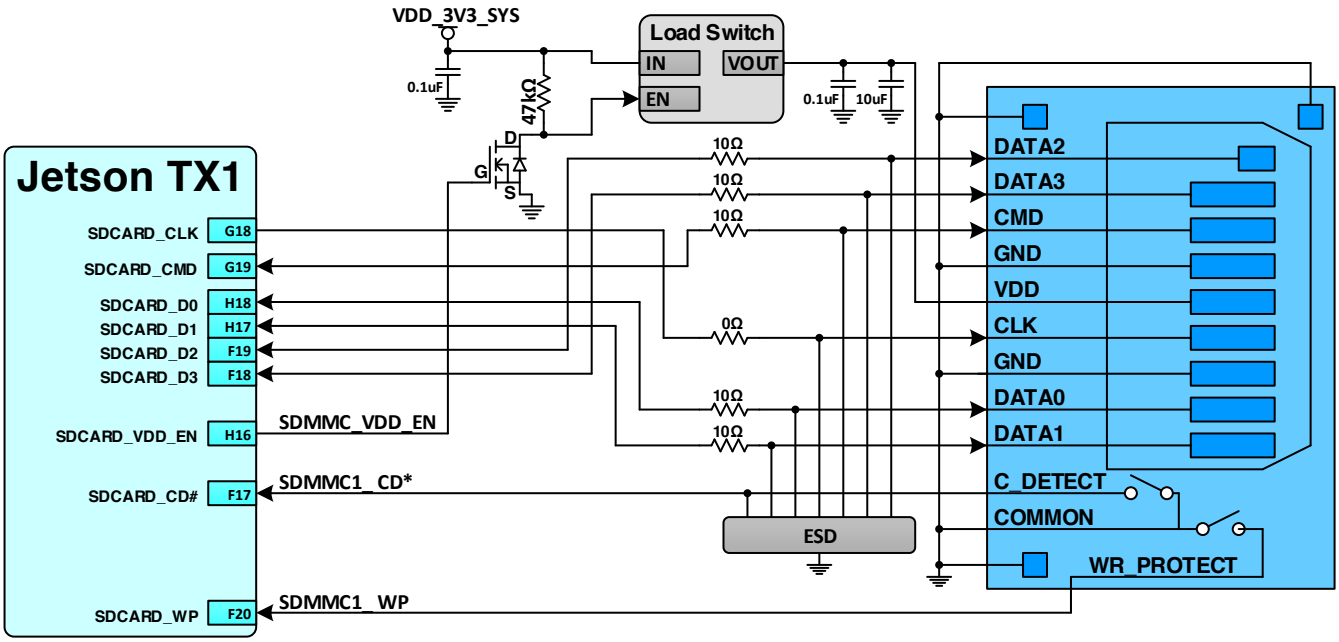


Table 4. SD Card Socket Pin Descriptions

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default
1	SDCARD_DAT3	SDCARD_D3	SD Card Data #3	Bidir
2	SDCARD_CMD	SDCARD_CMD	SD Card Command	Bidir
3	GND	–	Ground	Ground
4	SD_CARD_SW_PWR	–	SD Card Power	Power
5	SDCARD_CLK	SDCARD_CLK	SD Card Clock	Output
6	GND	–	Ground	Ground
7	SDCARD_DAT0	SDCARD_D0	SD Card Data #0	Bidir
8	SDCARD_DAT1	SDCARD_D1	SD Card Data #1	Bidir
9	SDCARD_DAT2	SDCARD_D2	SD Card Data #2	Bidir
10	SDCARD_CD*	SDCARD_CD#	SD Card, Card Detect	Input
11	GND	–	Ground	Ground
12	SDCARD_WP	SDCARD_WP	SD Card Write Protect	Input
13	GND	–	Ground	Ground
14	GND	–	Ground	Ground
15	GND	–	Ground	Ground

Notes: In the Type/Dir column, Output is to SD Card Socket. Input is from SD Card Socket. Bidir is for Bidirectional signals.

2.5 HDMI

A standard HDMI type A connector (J16) is supported.

Figure 8. HDMI Connections

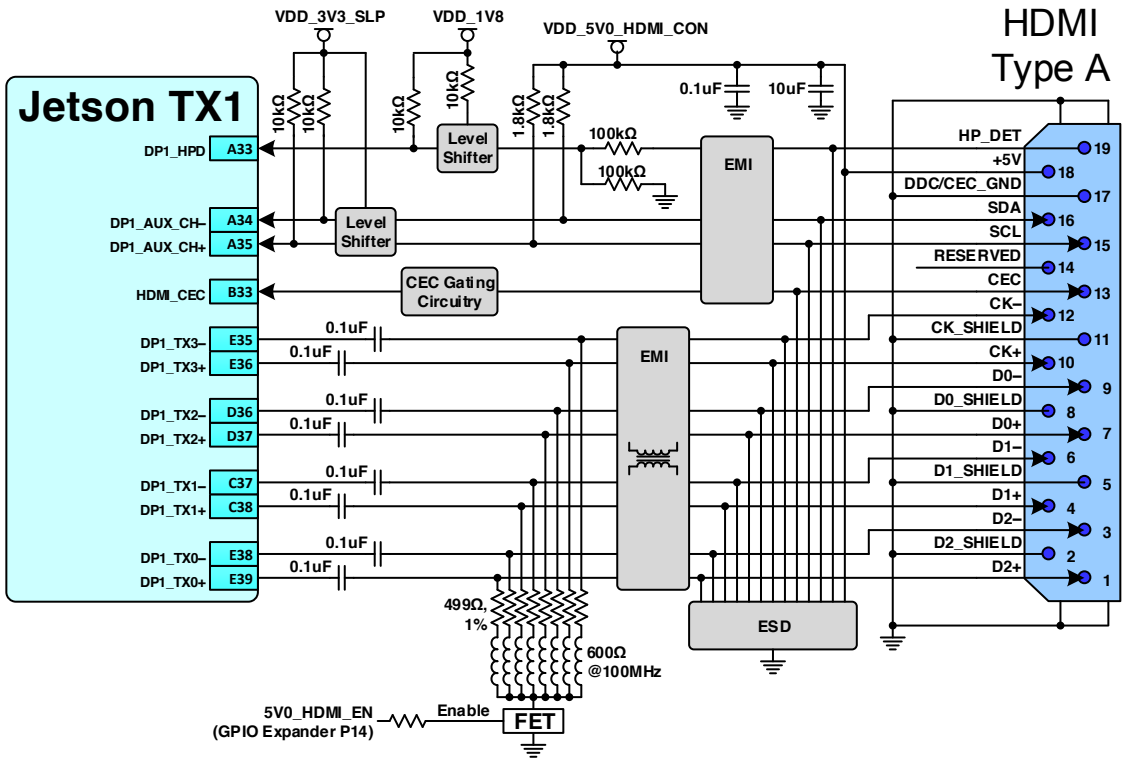


Table 5. HDMI Connector Pin Descriptions

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default
1	HDMI_TXD2_CON_P	DP1_TXD0+	HDMI Transmit Data 2+	Output
2	SHIELD/GND	–	Ground	Ground
3	HDMI_TXD2_CON_N	DP1_TXD0–	HDMI Transmit Data 2–	Output
4	HDMI_TXD1_CON_P	DP1_TXD1+	HDMI Transmit Data 1+	Output
5	SHIELD/GND	–	Ground	Ground
6	HDMI_TXD1_CON_N	DP1_TXD1–	HDMI Transmit Data 1–	Output
7	HDMI_TXD0_CON_P	DP1_TXD2+	HDMI Transmit Data 0+	Output
8	SHIELD/GND	–	Ground	Ground
9	HDMI_TXD0_CON_N	DP1_TXD2–	HDMI Transmit Data 0–	Output
10	HDMI_TXC_CON_P	DP1_TXD3+	HDMI Transmit Clock+	Output
11	SHIELD/GND			
12	HDMI_TXC_CON_N	DP1_TXD3–	HDMI Transmit Clock–	Output
13	HDMI_CEC_CON	HDMI_CEC	HDMI CEC	Bidir
14	RESERVED	–	Unused	Unused
15	HDMI_DDC_SCL_5V0	DP1_AUX_CH+	HDMI DDC Clock	Output /OD
16	HDMI_DDC_SDA_5V0	DP1_AUX_CH–	HDMI DDC Data	Bidir/OD
17	GND	–	Ground	Ground
18	VDD_5V0_HDMI_CON	–	HDMI 5V Power	Power
19	HDMI_HPD_CON	DP1_HPD		Input

Notes: In the Type/Dir column, Output is to HDMI Connector. Input is from HDMI Connector. Bidir is for Bidirectional signals.

2.6 M.2, Key E Expansion Slot

The Jetson TX1 carrier board includes a M.2, Key E Slot Mini-PCIe Expansion slot (J18). This includes interface options for WiFi/Bt including:

- PCIe (x1)
- SDIO (4-bit)
- USB 2.0
- I2S
- I2C

The connections & power rails associated with the connector are shown in the figure below.

Table 6. M.2, Key E Expansion Slot Pin Descriptions

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default
1	GND	–	Ground	Ground		–	–	–	–
3	USB2_D_P	USB2_D+	USB 2.0 Data +	Bidir	2	VDD_3V3_SYS	–	Main 3.3V Supply	Power
5	USB2_D_N	USB2_D–	USB 2.0 Data -	Bidir	4	VDD_3V3_SYS			
7	GND	–	Ground	Ground	6	LED1_L	–	LED #1 (CR4 – Green)Enable	Output
9	SDIO_CLK	SDIO_CLK	SDIO Clock	Output	8	I2S2_CLK	I2S2_CLK	I2S #2 Clock	Bidir
11	SDIO_CMD	SDIO_CMD	SDIO Command	Bidir	10	I2S2_LRCLK	I2S2_LRCLK	I2S #2 Left/Right Clock	Bidir
13	SDIO_DAT0	SDIO_D0	SDIO Data 0	Bidir	12	I2S2_SDIN	I2S2_SDIN	I2S #2 Data In	Input
15	SDIO_DAT1	SDIO_D1	SDIO Data 1	Bidir	14	I2S2_SDOUT	I2S2_SDOUT	I2S #2 Data Out	Bidir
17	SDIO_DAT2	SDIO_D2	SDIO Data 2	Bidir	16	LED2_L	–	LED #2 (CR3 – Green) Enable	Output
19	SDIO_DAT3	SDIO_D3	SDIO Data 3	Bidir	18	GND	–	Ground	Ground
21	WIFI2_EN	SDIO_RST	WiFi #2 Enable	Output	20	BT2_WAKE_AP_L	GPIO13_BT_ WAKE_AP	Bluetooth #2 Wake AP	Input
23	WIFI2_WAKE_AP_L	GPIO10_WIFI_ WAKE_AP	WiFi #2 Wake AP	Input	22	UART2_RXD	UART2_RX	UART #2 Receive	Input
25	NC (Key)	–	Unused	Unused	24	NC (Key)	–	Unused	Unused
27	NC (Key)				26	NC (Key)			
29	NC (Key)				28	NC (Key)			
31	NC (Key)				30	NC (Key)			
33	GND	–	Ground	Ground	32	UART2_TXD	UART2_TX	UART #2 Transmit	Output
35	PEX_TX0_AP_P	PEX1_TX+	PCIe #1 Transmit +	Output	34	UART2_CTS_N	UART2_CTS#	UART #2 Clear to Send	Input
37	PEX_TX0_AP_N	PEX1_TX–	PCIe #1 Transmit -	Output	36	UART2_RTS_N	UART2_RTS#	UART #2 Request to Send	Output
39	GND	–	Ground	Ground	38	NC	–	Unused	Unused
41	PEX_RX0_AP_P	PEX1_RX+	PCIe #1 Receive +	Input	40	NC			
43	PEX_RX0_AP_N	PEX1_RX–	PCIe #1 Receive -	Input	42	NC			
45	GND	–	Ground	Ground	44	NC			
47	PEX_CLK1_P	PEX1_REFCLK+	PCIe #1 Reference clock +	Output	46	NC			
49	PEX_CLK_N	PEX1_REFCLK–	PCIe #1 Reference clock -	Output	48	NC			
51	GND	–	Ground	Ground	50	SUSCLK_32KHZ	–	Suspend Clock (32KHz)	Output
53	PCIE_L1_CLKREQ	PEX1_CLKREQ#	PCIe #1 Clock Request	Bidir	52	PCIE_L1_RST	–	PCIe Reset	Output
55	PCIE_WAKE_L	PEX_WAKE#	PCIe Wake	Input	54	W_DISABLE2_L	–	Wifi Disable #2	Output
57	GND	–	Ground	Ground	56	W_DISABLE1_L	–	Wifi Disable #1	Output
59	NC	–	Unused	Unused	58	GEN1_I2C_SDA_ 3V3_LVL	I2C_GP0_DAT	General I2C Interface #0 Data	Bidir/OD
61	NC				60	GEN1_I2C_SCL_ 3V3_LVL	I2C_GP0_CLK	General I2C Interface #0 Clock	Bidir/OD
63	GND	–	Ground	Ground	62	M2_E_ALERT_L	–	M.2, Key E Connector Alert	Input
65	NC	–	Unused	Unused	64	NC	–	Unused	Unused
67	NC				66	NC			
69	GND	–	Ground	Ground	68	NC			
71	NC	–	Unused	Unused	70	NC			
73	NC				72	VDD_3V3_SYS	–	Main 3.3V Supply	Power
75	GND	–	Ground	Ground	74	VDD_3V3_SYS			

Notes: In the Type/Dir column, Output is to M.2 Module. Input is from M.2 Module. Bidir is for Bidirectional signals.

Table 7. M.2 Related TX1 Carrier PCB Trace Delays

Jetson TX1 Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for M.2 Module (ps)		Jetson TX1 Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)		Max Delay for M.2 Module (ps)	
PCIe					**SDIO**		**≤ SDR50**	**>SDR50**	**≤ SDR50**	**>SDR50**
PEX1_RX+	539	880	341		SDIO_CLK	230	876	521	646	291
PEX1_RX–	539	880	342		SDIO_CMD	223	876	521	653	298
PEX1_TX+	518	880	362		SDIO_D0	222	876	521	654	299
PEX1_TX–	519	880	361		SDIO_D1	222	876	521	654	299
PEX1_REFCLK+	178	880	702		SDIO_D2	225	876	521	651	296
PEX1_REFCLK–	178	880	702		SDIO_D3	240	876	521	636	281
USB					**I2S**		**All**	**na**	**All**	**na**
USB2_D+	171	960	789		I2S2_CLK	970	3600		2630	
USB2_D–	172	960	788		I2S2_LRCLK	967	3600		2633	
					I2S2_SDIN	931	3600		2669	
					I2S2_SDOUT	924	3600		2676	

2.7 PCIe x4 Connector

The Jetson TX1 carrier board includes a standard 4-lane PCIe connector (J2).

Figure 9. PCIe 4-lane Connector Connections

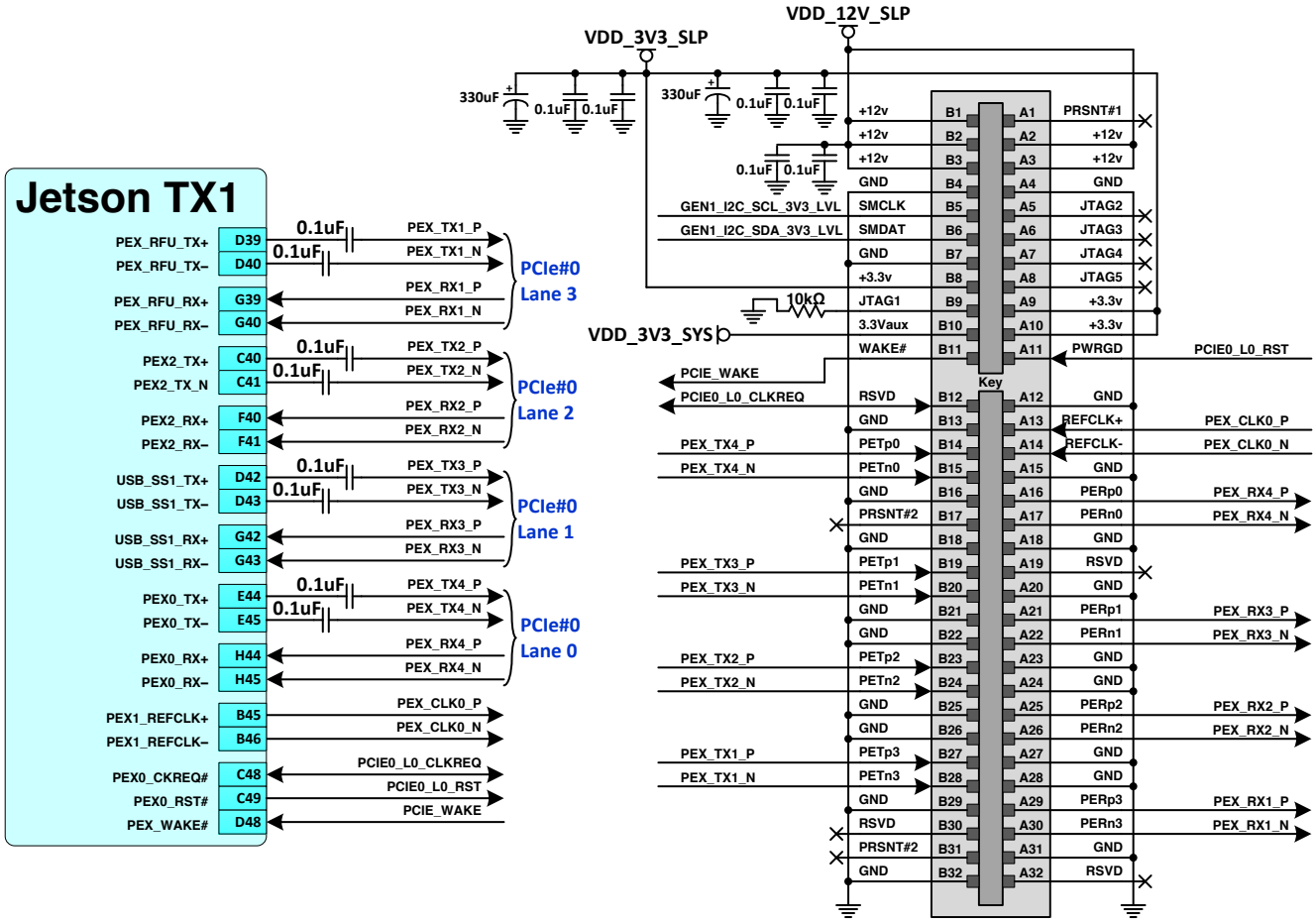


Table 8. PCIe 4-lane Connector Pin Descriptions

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/ Direction	Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/ Direction
A1	GND (PRSNT1)	–	Ground	Ground	B1	VDD_12V_SLP	–	12V Supply	Power
A2	VDD_12V_SLP	–	12V Supply (Boost)	Power	B2	VDD_12V_SLP			
A3	VDD_12V_SLP				B3	VDD_12V_SLP			
A4	GND	–	Ground	Ground	B4	GND	–	Ground	Ground
A5	NC	–	Unused	Unused	B5	GEN1_I2C_SCL_3V3_LVL	I2C_GP0_CLK	General I2C #0 Clock	Bidir/OD
A6	NC				B6	GEN1_I2C_SDA_3V3_LVL	I2C_GP0_DAT	General I2C #0 Data	Bidir/OD
A7	NC				B7	GND	–	Ground	Ground
A8	NC				B8	VDD_3V3_SLP	–	3.3V supply – off in Deep Slp	Power
A9	VDD_3V3_SLP	–	3.3V supply - off in Deep Slp	Power	B9	PCIE_JTAG_TRST_PD	–	Pulled to GND	–
A10	VDD_3V3_SLP				B10	VDD_3V3_SYS	–	Main 3.3V Supply	Power
A11	PCIE0_L0_RST	PEX0_RST#	PCIe Lane 0 Reset	Output	B11	PCIE_WAKE	PEX_WAKE#	PCIe Wake (Shared)	Input
A12	GND	–	Ground	Ground	B12	PCIE0_L0_CLKREQ	PEX0_CLKREQ#	PCIe Ctlr 0 Clock Req.	Bidir
A13	PEX_CLK0_P	PEX0_REFCLK+	PCIe Ctlr 0 Reference Clock +	Output	B13	GND	–	Ground	Ground
A14	PEX_CLK0_N	PEX0_REFCLK–	PCIe Ctlr 0 Reference Clock –	Output	B14	PEX_TX4_C_P	PEX0_TX+	PCIe Ctlr 0 Lane 0 Transmit +	Output
A15	GND	–	Ground	Ground	B15	PEX_TX4_C_N	PEX0_TX–	PCIe Ctlr 0 Lane 0 Transmit –	Output
A16	PEX_RX4_P	PEX0_RX_P	PCIe Ctlr 0 Lane 0 Receive +	Input	B16	GND	–	Ground	Ground
A17	PEX_RX4_N	PEX0_RX–	PCIe Ctlr 0 Lane 0 Receive –	Input	B17	NC	–	Unused	Unused
A18	GND	–	Ground	Ground	B18	GND	–	Ground	Ground
A19	NC	–	Unused	Unused	B19	PEX_TX3_C_P	USB_SS1_TX+	PCIe Ctlr r 0 Lane 3 Transmit +	Output
A20	GND	–	Ground	Ground	B20	PEX_TX3_C_N	USB_SS1_TX–	PCIe Ctlr 0 Lane 3 Transmit –	Output
A21	PEX_RX3_P	USB_SS1_RX+	PCIe Ctlr 0 Lane 3 Receive +	Input	B21	GND	–	Ground	Ground
A22	PEX_RX3_N	USB_SS1_RX–	PCIe Ctlr 0 Lane 3 Receive –	Input	B22	GND			
A23	GND	–	Ground	Ground	B23	PEX_TX2_C_P	PEX2_TX+	PCIe Ctlr 0 Lane 2 Transmit +	Output
A24	GND				B24	PEX_TX2_C_N	PEX2_TX–	PCIe Ctlr 0 Lane 2 Transmit –	Output
A25	PEX_RX2_P	PEX2_RX+	PCIe Ctlr 0 Lane 2 Receive +	Input	B25	GND	–	Ground	Ground
A26	PEX_RX2_N	PEX2_RX–	PCIe Ctlr 0 Lane 2 Receive –	Input	B26	GND			
A27	GND	–	Ground	Ground	B27	PEX_TX1_C_P	PEX_RFU_TX+	PCIe Ctlr 0 Lane 1 Transmit +	Output
A28	GND				B28	PEX_TX1_C_N	PEX_RFU_TX–	PCIe Ctlr 0 Lane 1 Transmit –	Output
A29	PEX_RX1_P	PEX_RFU_RX+	PCIe Ctlr 0 Lane 1 Receive +	Input	B29	GND	–	Ground	Ground
A30	PEX_RX1_N	PEX_RFU_RX–	PCIe Ctlr 0 Lane 1 Receive –	Input	B30	NC	–	Unused	Unused
A31	GND	–	Ground	Ground	B31	NC			
A32	NC	–	Unused	Unused	B32	GND	–	Ground	Ground

Notes: In the Type/Dir column, Output is to the PCIe Connector. Input is from the PCIe Connector. Bidir is for Bidirectional signals.

Table 9. PCIe x4 Related TX1 Carrier PCB Trace Delays

Jetson TX1 Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for PCIe Board (ps)		Jetson TX1 Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for PCIe Board (ps)
PCIe					PEX2_RX+	540	880	340
PEX0_RX+	502	880	378		PEX2_RX–	539	880	341
PEX0_RX–	502	880	378		PEX2_TX+	521	880	359
PEX0_TX+	505	880	375		PEX2_TX–	522	880	358
PEX0_TX–	504	880	376		PEX_RFU_RX+	539	880	341
USB_SS1_RX+	528	880	352		PEX_RFU_RX–	539	880	342
USB_SS1_RX–	527	880	353		PEX_RFU_TX+	518	880	362
USB_SS1_TX+	522	880	358		PEX_RFU_TX–	519	880	361
USB_SS1_TX–	522	880	358		PEX0_REFCLK+	521	880	359
					PEX0_REFCLK–	520	880	360

2.8 JTAG

The Jetson TX1 carrier board has a standard 20-pin (2x10, 2.54mm pitch) JTAG header (J7).

Figure 10. JTAG Header Connections

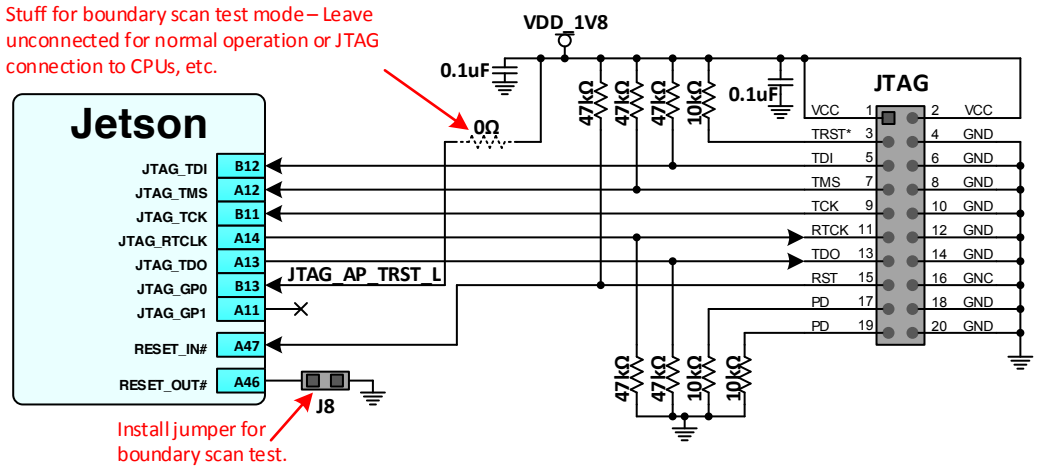


Table 10. JTAG Header Descriptions

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/ Direction	Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/ Direction
1	VDD_1V8	–	Main 1.8V Supply	Power	2	VDD_1V8	–	Main 1.8V Supply	Power
3	TRST*	–	JTAG Test Reset	–	4	GND	–	Ground	Ground
5	JTAG_AP_TDI	JTAG_TDI	JTAG Test Data In	Input	6	GND			
7	JTAG_AP_TMS	JTAG_TMS	JTAG Test Mode Select	Input	8	GND			
9	JTAG_AP_TCK	JTAG_TCK	JTAG Test Clock	Input	10	GND			
11	JTAG_AP_RTCK	JTAG_RTCK	JTAG Test Return clock	Output	12	GND			
13	JTAG_AP_TDO	JTAG_TDO	JTAG Test Data out	Output	14	GND			
15	RESET_IN_L	RESET_IN#	Main carrier board Reset	Input	16	GND			
17	PD	–	Pull-down	–	18	GND			
19	PD	–	Pull-down	–	20	GND			

Notes: In the Type/Dir column, Output is to JTAG header. Input is from JTAG header. Bidir is for Bidirectional signals.

3.0 CARRIER BOARD CUSTOM EXPANSION IF CONNECTIONS

The Jetson TX1 carrier board supports a number of expansion headers/connectors that have custom pinouts. These are listed below:

- Jetson TX1 Module Connector, 8x50, 1.27mm pitch
- Display Expansion Header, 2x60, 0.5mm pitch
- Camera Expansion Header, 2x60, 0.5mm pitch
- Expansion Header, 2x20, 2.54mm pitch
- Debug Connector, 2x30, 0.5mm pitch
- GPIO Expansion Header, 2x15, 2.54mm pitch
- Serial Port Header, 1x6, 2.54mm pitch
- Charge Control Header, 10-pin Flex Receptacle, 0.8mm pitch
- Fan Connector, 4-pin, 1.25mm pitch
- DC Power Jack

The Routing Guidelines for the interfaces supported on the expansion connectors can be found in the Jetson TX1 OEM Product DG. Those guidelines cover the PCB routing from Jetson TX1 to the peripheral device or actual device connector. When designing modules for one of the Jetson TX1 Expansion connectors, the routing on the Carrier board must be accounted for. Tables are be provided for the critical interfaces that provide the PCB delays on the Carrier board. These delays are subtracted from the delays allowed in the Jetson TX1 OEM Product DG routing guidelines. The tables also include the max trace guidelines and remaining max trace delay allowed on the peripheral modules. See the Jetson TX1 OEM Product DG for other requirements (Impedance, trace spacing, skews between signals, etc.).

3.1 Jetson TX1 Module Connector

The carrier board interfaces to the Jetson TX1 module using a 400-pin Samtec connector (J13). The carrier board has a Samtec REF-186138-01 connector. This interfaces with the Jetson TX1 which has a Samtec REF-186137-01 connector. The connector pinout can be found in the Jetson TX1 OEM Product DG.

3.2 Display Expansion Connector

The Jetson TX1 carrier board includes a 120-pin (2x60, 0.5mm pitch) Display Expansion Connector (J23). The connector used on the Carrier board is a Samtec QSH-060-01-H-D-A. The mating connector is a Samtec QTH-060-01-H-D-A. The display expansion connector includes interface options for an embedded display and touch controller including:

- DSI 2 x4
- eDP
- eDP HPD
- eDP AUX
- LCD BL EN/PWM
- LCD EN/TE/BIAS EN
- SPI0, SPI2
- I2C_GP1
- Touch INT/RST/CLK
- Display control

Table 11. Display Expansion Connector Pin Descriptions

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default
1	CON_DSI_B_D3_N	DSI3_D1–	DSI B Data 3-	Output	2	VDD_SYS_BL	–	Main DC supply power	Power
3	CON_DSI_B_D3_P	DSI3_D1+	DSI B Data 3+	Output	4	VDD_SYS_BL			
5	GND	–	Ground	Ground	6	VDD_SYS_BL			
7	CON_DSI_B_D2_N	DSI3_D0–	DSI B Data 2-	Output	8	LCD_BL_EN	LCD_BKLT_EN	Backlight Enable	Output
9	CON_DSI_B_D2_P	DSI3_D0+	DSI B Data 2+	Output	10	LCD_BL_PWM	LCD_BKLT_PWM	Backlight PWM	Output
11	GND	–	Ground	Ground	12	LCD_RST_L	LCD_EN	LCD Enable	Output
13	CON_DSI_B_CLK_N	DSI2_CLK–	DSI B Clock-	Output	14	LCD_TE	LCD_TE	LCD Tearing Effect	Input

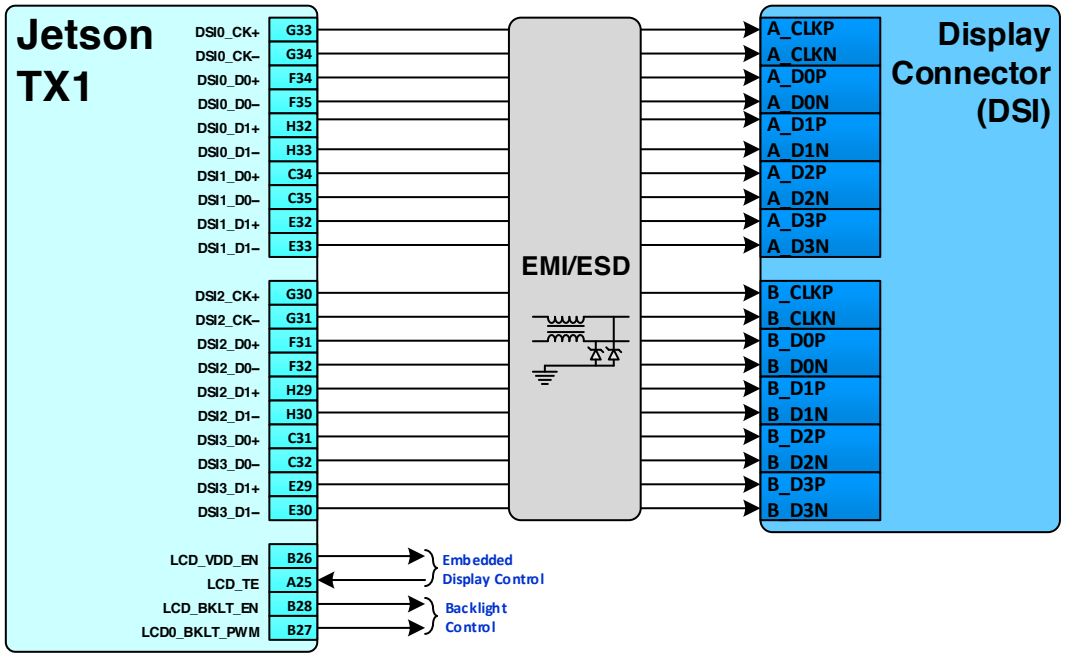
Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default
15	CON_DSI_B_CLK_P	DSI2_CLK+	DSI B Clock+	Output	16	VDD_3V3_SLP	–	3.3V supply - off in Deep Slp	Power
17	GND	–	Ground	Ground	18	BRIDGE_EN	–	Bridge Enable	Output
19	CON_DSI_B_D1_N	DSI2_D1–	DSI B Data 1-	Output	20	BRIDGE_IRQ	–	Bridge Interrupt	Output
21	CON_DSI_B_D1_P	DSI2_D1+	DSI B Data 1+	Output	22	I2C_GP0_CLK_1V8	I2C_GP0_CLK	General I2C #0 Clock	Bidir/OD
23	GND	–	Ground	Ground	24	I2C_GP0_DAT_1V8	I2C_GP0_DAT	General I2C #0 Data	Bidir/OD
25	CON_DSI_B_D0_N	DSI2_D0–	DSI B Data 0-	Output	26	AVDD_TS_DIS	–	3.3V supply for touchscreen	Power
27	CON_DSI_B_D0_P	DSI2_D0+	DSI B Data 0+	Output	28	VDD_TS_1V8		1.8V supply for touchscreen	
29	GND	–	Ground	Ground	30	CON_GEN2_I2C_SCL_LT	I2C_GP1_CLK	General I2C #1 Clock	Bidir/OD
31	CON_DSI_A_D3_N	DSI1_D1–	DSI A Data 3-	Output	32	CON_GEN2_I2C_SDA_LT	I2C_GP1_DAT	General I2C #1 Data	Bidir/OD
33	CON_DSI_A_D3_P	DSI1_D1+	DSI A Data 3+	Output	34	TOUCH_INT	GPIO6_TOUCH_INT	Touchscreen Interrupt	Input
35	GND	–	Ground	Ground	36	TOUCH_RST	GPIO7_TOUCH_RST	Touchscreen controller Reset	Output
37	CON_DSI_A_D2_N	DSI1_D0–	DSI A Data 2-	Output	38	SPI0_CLK	SPI0_CLK	Touchscreen SPI Clock	Bidir
39	CON_DSI_A_D2_P	DSI1_D0+	DSI A Data 2+	Output	40	SPI0_MISO	SPI0_MISO	Touchscreen SPI MISO	Bidir
41	GND	–	Ground	Ground	42	SPI0_MOSI	SPI0_MOSI	Touchscreen SPI MOSI	Bidir
43	CON_DSI_A_CLK_N	DSI0_CLK–	DSI A Clock-	Output	44	SPI0_CS0	SPI0_CS0#	Touchscreen SPI Chip Select	Bidir
45	CON_DSI_A_CLK_P	DSI0_CLK+	DSI A Clock+	Output	46	NC	–	Unused	Unused
47	GND	–	Ground	Ground	48	GND	–	Ground	Ground
49	CON_DSI_A_D1_N	DSI0_D1–	DSI A Data 1-	Output	50	TOUCH_CLK	TOUCH_CLK	Touchscreen Controller Clock	Output
51	CON_DSI_A_D1_P	DSI0_D1+	DSI A Data 1+	Output	52	GND	–		Ground
53	GND	–	Ground	Ground	54	VDD_DIS_3V3_LCD	–	Gated 3.3V analog supply	Power
55	CON_DSI_A_D0_N	DSI0_D0–	DSI A Data 0-	Output	56	VDD_DIS_3V3_LCD	–		Power
57	CON_DSI_A_D0_P	DSI0_D0+	DSI A Data 0+	Output	58	VDD_LCD_1V8_DIS		Gated 1.8V supply	
59	GND	–	Ground	Ground	60	GND	–	Ground	Ground
61	VDD_3V3_SYS	–	Main 3.3V Supply (Switcher)	Power	62	LCD_EN	LCD_VDD_EN	LCD Power Enable	Output
63	VDD_3V3_SYS				64	NC	–	Unused	Unused
65	GND	–	Ground	Ground	66	CON_DSI3_CLK_P			
67	GND				68	CON_DSI3_CLK_N			
69	VDD_1V8	–	Main 1.8V Supply (Switcher)	Power	70	GND	–	Ground	Ground
71	VDD_1V8				72	CON_DSI4_CLK_P	–	Unused	Input
73	GND	–	Ground	Ground	74	CON_DSI4_CLK_N			
75	GND				76	GND	–	Ground	Ground
77	VDD_1V2	–	1.2V Display Supply (LDO)	Power	78	GND			
79	VDD_1V2				80	VDD_5V0_IO_SYS	–	Main 5.0V Supply (Switcher)	Power
81	GND	–	Ground	Ground	82	NC	–	Unused	Unused
83	GND				84	NC			
85	DP_HPD0_AP	DP_HPD	Display Port 0 Hot Plug Det.	Input	86	ACOK	CHARGER_PRSNT	AC OK	Output
87	EDP_AUX_CH0_N	DP0_AUX_CH–	Display Port 0 Aux Channel-	Bidir	88	LCD_BIAS_EN	–	LCD BIAS Enable	Output
89	EDP_AUX_CH0_P	DP0_AUX_CH+	Display Port 0 Aux Channel+	Bidir	90	GND	–	Ground	Ground
91	GND	–	Ground	Ground	92	GS_V	–	Unused	Unused
93	EDP_TXD0_P	DP0_TX0+	Display Port 0 Data Lane 0-	Output	94	GS_H			
95	EDP_TXD0_N	DP0_TX0–	Display Port Data Lane 0+	Output	96	GND	–	Ground	Ground
97	GND	–	Ground	Ground	98	NVSR_INT	–	NV Sensor Interrupt	Input
99	EDP_TXD1_P	DP0_TX1+	Display Port 0 Data Lane 1-	Output	100	LCD1_BKLT_PWM	–	unused	Input
101	EDP_TXD1_N	DP0_TX1–	Display Port 0 Data Lane 1+	Output	102	GND	–	Ground	Ground
103	GND	–	Ground	Ground	104	SPI2_SCK	SPI2_SCK	SPI #2 Clock	Bidir
105	EDP_TXD2_P	DP0_TX2+	Display Port 0 Data Lane 2-	Output	106	SPI2_MISO	SPI2_MISO	SPI #2 Master In, Slave Out	Bidir
107	EDP_TXD2_N	DP0_TX2–	Display Port 0 Data Lane 2+	Output	108	SPI2_MOSI	SPI2_MOSI	SPI #2 Master Out, Slave In	Bidir
109	GND	–	Ground	Ground	110	SPI2_CS0	SPI2_CS0#	SPI #2 Chip Select	Bidir
111	nc	–	Unused	Unused	112	GND	–	Ground	Ground
113	nc				114	NC	–	Unused	Unused
115	GND	–	Ground	Ground	116	NC			
117	EDP_TXD3_P	DP0_TX3+	Display Port 0 Data Lane 3-	Output	118	NC			
119	EDP_TXD3_N	DP0_TX3–	Display Port 0 Data Lane 3+	Output	120	NC			

Notes: In the Type/Dir column, Output is to Display Module. Input is from Display Module. Bidir is for Bidirectional signals.

DSI Guidelines

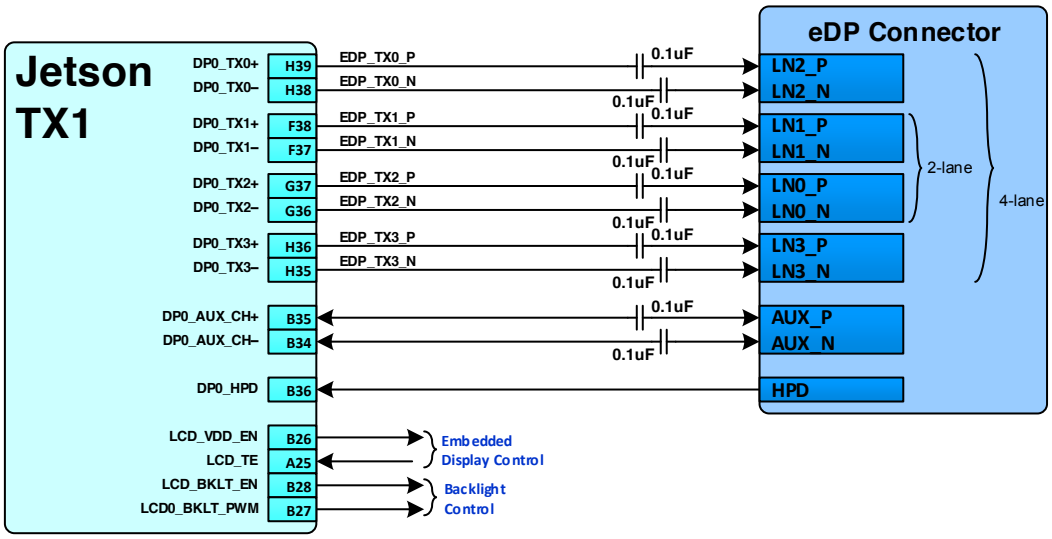
Tegra supports eight total MIPI DSI data lanes and two clock lanes, allowing up to two 4-lane interfaces. These can be be used for two separate displays, or together for a single display (clock lane per 4 data lanes still applies for the single display case. Each data channel has peak bandwidth up to 1.5Gbps.

Figure 11: DSI 2 x 4-Lane Connection Example



Note: If EMI/ESD devices are necessary, they must be tuned to minimize impact to signal quality, which must meet the DSI spec. requirements for the frequencies supported by the design.

Figure 12: eDP 4-Lane Connection Example



See the Jetson TX1 OEM Product DG for Routing Guidelines. Include the Carrier board PCB trace delays in the following table when calculating max trace length & for skew matching.

Table 12. Display Connector Interface Related TX1 Carrier PCB Trace Delays (DSI & SPI)

Jetson TX1 Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for Display Module (ps)		Jetson TX1 Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for Display Module (ps)
DSI					DSI2_D0+	491.32	1050	559
DSI0_CK+	494.07	1050	556		DSI2_D0–	491.24	1050	559
DSI0_CK–	493.22	1050	557		DSI2_D1+	492.98	1050	557
DSI0_D0+	495.21	1050	555		DSI2_D1–	492	1050	558
DSI0_D0–	495.92	1050	554		DSI3_D0+	495.72	1050	554
DSI0_D1+	490.3	1050	560		DSI3_D0–	496.48	1050	554
DSI0_D1–	489.32	1050	561		**SPI**			
DSI1_D0+	491.84	1050	558		SPI0_CLK	750	1865	1115
DSI1_D0–	492.8	1050	557		SPI0_MISO	740	1865	1125
DSI1_D1+	495.04	1050	555		SPI0_MOSI	743	1865	1122
DSI1_D1–	495.98	1050	554		SPI0_CS0#	758	1865	1107
DSI2_CK+	492.54	1050	557		SPI2_SCK	373	1865	1492
DSI2_CK–	491.63	1050	558		SPI2_MISO	650	1865	1215
					SPI2_MOSI	649	1865	1216
					SPI2_CS0#	643	1865	1222

Table 13. Display Connector Interface Related TX1 Carrier PCB Trace Delays (DP0)

Jetson TX1 Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)		Max Delay for Display Module (ps)	
		RBR/HBR Stripline	RBR/HBR uStrip	RBR/HBR Stripline	RBR/HBR uStrip
DP0_TX0+	609	1138	975	529	366
DP0_TX0–	608	1138	975	529	367
DP0_TX1+	608	1138	975	529	367
DP0_TX1–	609	1138	975	529	366
DP0_TX2+	623	1138	975	514	352
DP0_TX2–	624	1138	975	513	351
DP0_TX3+	658	1138	975	479	317
DP0_TX3–	659	1138	975	478	316
DP0_AUX_CH+	529	1138	975	608	446
DP0_AUX_CH–	529	1138	975	609	446

3.3 Camera Expansion Connector

The Jetson TX1 carrier board includes a 120-pin (2x60, 0.5mm pitch) Camera Expansion Connector (J22). The connector used on the Carrier board is a Samtec QSH-060-01-H-D-A. . The mating connector is a Samtec QTH-060-01-H-D-A. The camera expansion connector includes interface options for multiple cameras as well as some for audio (I2S & DMIC):

- CSI up to 6x2 lane
- CAM_I2C, Clock & Control GPIOs for the Cameras
- Digital Microphone IF
- I2S
- SPI
- I2C
- UART

Table 14. Camera Expansion Connector Pin Descriptions

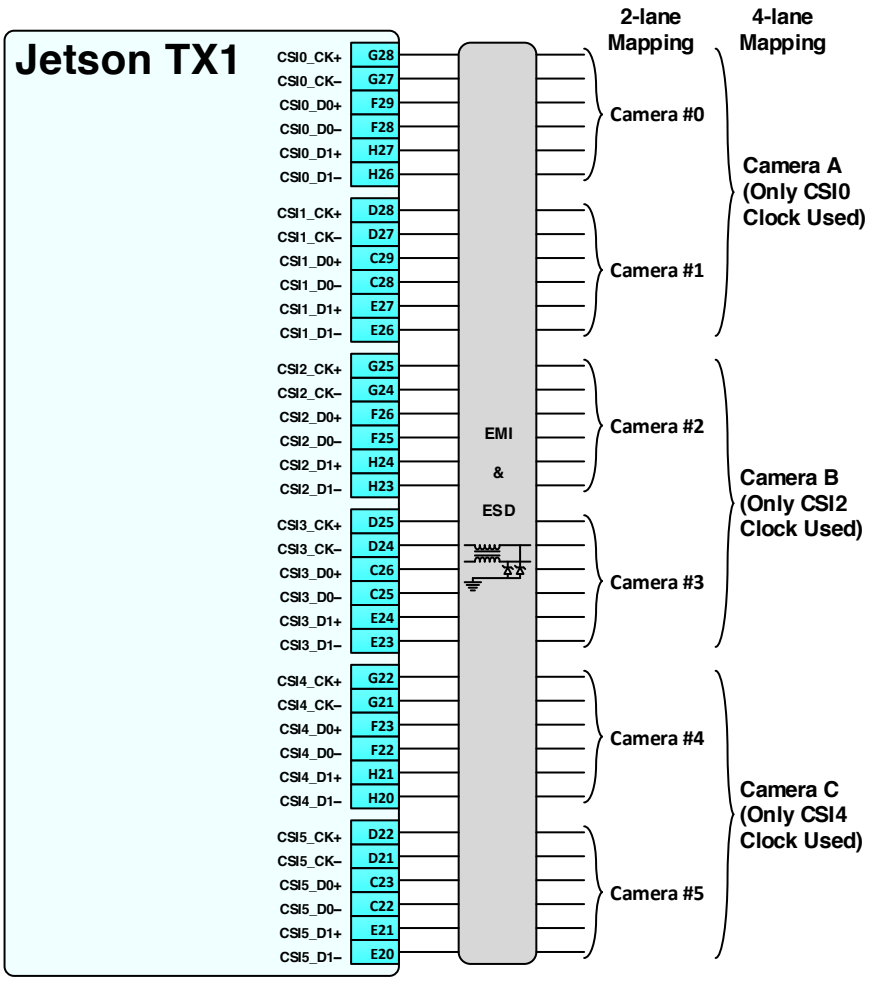
Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default
1	CON_CSI_A_D0_P	CSI0_D0+	CSI A Data 0+	Input	2	CON_CSI_B_D0_P	CSI1_D0_P	CSI B Data 0+	Input
3	CON_CSI_A_D0_N	CSI0_D0–	CSI A Data 0-	Input	4	CON_CSI_B_D0_N	CSI1_D0_N	CSI B Data 0-	Input
5	GND	–	Ground	Ground	6	GND	–	Ground	Ground
7	CON_CSI_A_CLK_P	CSI0_CLK+	CSI A Clock+	Input	8	CON_CSI_B_CLK_P	CSI1_CLK_P	CSI B Clock+	Input
9	CON_CSI_A_CLK_N	CSI0_CLK–	CSI A Clock-	Input	10	CON_CSI_B_CLK_N	CSI1_CLK_N	CSI B Clock-	Input
11	GND	–	Ground	Ground	12	GND	–	Ground	Ground
13	CON_CSI_A_D1_P	CSI0_D1+	CSI A Data 1+	Input	14	CON_CSI_B_D1_P	CSI1_D1_P	CSI B Data 1+	Input

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default
15	CON_CSI_A_D1_N	CSI0_D1–	CSI A Data 1-	Input	16	CON_CSI_B_D1_N	CSI1_D1–	CSI B Data 1-	Input
17	GND	–	Ground	Ground	18	GND	–	Ground	Ground
19	CON_CSI_C_D0_P	CSI2_D0+	CSI C Data 0+	Input	20	CON_CSI_D_D0_P	CSI3_D0+	CSI D Data 0+	Input
21	CON_CSI_C_D0_N	CSI2_D0–	CSI C Data 0-	Input	22	CON_CSI_D_D0_N	CSI3_D0–	CSI D Data 0-	Input
23	GND	–	Ground	Ground	24	GND	–	Ground	Ground
25	CON_CSI_C_CLK_P	CSI2_CLK+	CSI C Clock+	Input	26	CON_CSI_D_CLK_P	CSI3_CLK+	CSI D Clock+	Input
27	CON_CSI_C_CLK_N	CSI2_CLK–	CSI C Clock-	Input	28	CON_CSI_D_CLK_N	CSI3_CLK–	CSI D Clock-	Input
29	GND	–	Ground	Ground	30	GND	–	Ground	Ground
31	CON_CSI_C_D1_P	CSI2_D1+	CSI C Data 1+	Input	32	CON_CSI_D_D1_P	CSI3_D1+	CSI D Data 1+	Input
33	CON_CSI_C_D1_N	CSI2_D1–	CSI C Data 1-	Input	34	CON_CSI_D_D1_N	CSI3_D1–	CSI D Data 1-	Input
35	GND	–	Ground	Ground	36	GND	–	Ground	Ground
37	CON_CSI_E_D0_P	CSI4_D0+	CSI E Data 0+	Input	38	CON_CSI_F_D0_P	CSI5_D0+	CSI F Data 0+	Input
39	CON_CSI_E_D0_N	CSI4_D0–	CSI E Data 0-	Input	40	CON_CSI_F_D0_N	CSI5_D0–	CSI F Data 0-	Input
41	GND	–	Ground	Ground	42	GND	–	Ground	Ground
43	CON_CSI_E_CLK_P	CSI4_CLK+	CSI E Clock+	Input	44	CON_CSI_F_CLK_P	CSI5_CLK+	CSI F Clock+	Input
45	CON_CSI_E_CLK_N	CSI4_CLK–	CSI E Clock-	Input	46	CON_CSI_F_CLK_N	CSI5_CLK–	CSI F Clock-	Input
47	GND	–	Ground	Ground	48	GND	–	Ground	Ground
49	CON_CSI_E_D1_P	CSI4_D1+	CSI E Data 1+	Input	50	CON_CSI_F_D1_P	CSI5_D1+	CSI F Data 1+	Input
51	CON_CSI_E_D1_N	CSI4_D1–	CSI E Data 1-	Input	52	CON_CSI_F_D1_N	CSI5_D1–	CSI F Data 1-	Input
53	GND	–	Ground	Ground	54	GND	–	Ground	Ground
55	RSVD	–	Unused	Unused	56	RSVD	–	Unused	Unused
57	RSVD				58	RSVD			
59	CAM_UART3_PSNT_L	–	Camera UART Present – Direction control for level shifter to prevent contention.	–	60	NC			
61	CAM_UART3_TXD	–	Camera UART Transmit, Receive, Clear-to-Send & Request to Send – Can optionally be brought to Serial port connector (J13).	Output	62	SPI2_SCK	SPI2_CLK	SPI #2 Clock	Bidir
63	CAM_UART3_RXD	–		Input	64	SPI2_MISO	SPI2_MISO	SPI #2 MISO	Bidir
65	CAM_UART3_CTS	–		Input	66	SPI2_CS1	SPI2_CS1#	SPI #2 Chip Select	Bidir
67	CAM_UART3_RTS	–		Output	68	SPI2_MOSI	SPI2_MOSI	SPI #2 MOSI	Bidir
69	GND	–	Ground	Ground	70	GND	–	Ground	Ground
71	AO_DMIC_IN_CLK	–	Unused	Unused	72	I2S3_CLK	I2S3_CLK	I2S #3 Clock	Bidir
73	AO_DMIC_IN_DAT				74	I2S3_LRCLK	I2S3_LRCLK	I2S #3 Left/Right Clock	Bidir
75	CAM_I2C_SCL	I2C_CAM_CLK	Camera I2C clock	Bidir	76	I2S3_SDIN	I2S3_SDIN	I2S #3 Serial Data In	Input
77	CAM_I2C_SDA	I2C_CAM_DAT	Camera I2C data	Bidir	78	I2S3_SDOUT	I2S3_SDOUT	I2S #3 Serial Data Out	Bidir
79	GND	–	Ground	Ground	80	GND	–	Ground	Ground
81	AVDD_CAM	–	2.8V Camera supply (LDO)	Power	82	AVDD_CAM	–	2.8V Camera supply (LDO)	Power
83	AVDD_CAM				84	VDD_3V3_SLP	–	3.3V rail - off in Deep Sleep	Power
85	CAM_AF_PWDN	–	Camera auto-focus powerdn	Output	86	RSVD	–	Unused	Unused
87	I2C_PM_CLK	I2C_PM_CLK	Power Monitor I2C Clock	Bidir/OD	88	CAM1_MCLK	CAM1_MCLK	Camera #1 Master Clock	Output
89	I2C_PM_DAT	I2C_PM_DAT	Power Monitor I2C Data	Bidir/OD	90	CAM1_PWDN	GPIO1_CAM1_PWR	Camera #1 Powerdown	Output
91	CAM0_MCLK	CAM0_MCLK	Camera #0 Master Clock	Output	92	CAM1_RST_L	GPIO3_CAM1_RST	Camera #1 Reset	Output
93	CAM0_PWDN	GPIO0_CAM0_PWR	Camera #0 Powerdown	Output	94	RSVD	–	Unused	Unused
95	CAM0_RST_L	GPIO2_CAM0_RST	Camera #0 Reset	Output	96	CAM2_PWDN	–	Camera #2 Powerdown	Output
97	FLASH_EN	GPIO5_CAM_FLASH_EN	Flash Enable	Output	98	CAM2_RST	–	Camera #2 Reset	Output
99	GND	–	Ground	Ground	100	GND	–	Ground	Ground
101	DVDD_CAM_IO_1V2	–	1.2V digital Camera supply	Input	102	DVDD_CAM_IO_1V8	–	Switched 1.8V Camera supply.	Power
103	FLASH_INHIBIT	–	Flash Inhibit	Output	104	TORCH_EN	–	Torch Enable (GPIO exp. P05)	Output
105	I2C_GP0_CLK_1V8	I2C_GP0_CLK	General I2C #0 Clock	Bidir/OD	106	FLASH_STROBE	GPIO4_CAM_STROBE	Flash Strobe	Output
107	I2C_GP0_DAT_1V8	I2C_GP0_DAT	General I2C #0 Data	Bidir/OD	108	VDD_3V3_SLP	–	3.3V supply – off in Deep Slp	Power
109	VDD_5V0_IO_SYS	–	Main 5.0V Supply (Switcher)	Power	110	VDD_3V3_SLP	–	3.3V supply – off in Deep Slp	Power
111	NC	–	Unused	Unused	112	MOTION_INT_AP_L	GPIO9_MOTION_INT	Motion Sensor Interrupt	Input
113	NC				114	NC	–	Unused	Unused
115	GND	–	Ground	Ground	116	GND	–	Ground	Ground
117	MDM2AP_READY_1V8	–	Modem to Tegra Ready	Input	118	VDD_5V0_IO_SYS	–	Main 5.0V Supply (Switcher)	Power
119	VDD_SYS_EN	–	System power enable	Output	120	VDD_5V0_IO_SYS			

Notes: In the Type/Dir column, Output is to Camera Module. Input is from Camera Module. Bidir is for Bidirectional signals.

Camera/CSI Guidelines

Figure 13: Camera CSI Connections



Note: Any EMI/ESD devices must be tuned to minimize impact to signal quality and meet the timing & Vil/Vih requirements at the receiver & maintain signal quality and meet requirements for the frequencies supported by the design.

See the Jetson TX1 OEM Product DG for Routing Guidelines. Include the Carrier board PCB trace delays in the following table when calculating max trace length & for skew matching.

Table 15. Camera Expansion Connector Related TX1 Carrier PCB Trace Delays

Jetson TX1 Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for Camera Module (ps)		Jetson TX1 Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for Camera Module (ps)
CSI					CSI4_CK+	540	1050	510
CSI0_CK+	626	1050	424		CSI4_CK–	539	1050	511
CSI0_CK–	626	1050	424		CSI4_D0+	540	1050	510
CSI0_D0+	627	1050	423		CSI4_D0–	540	1050	510
CSI0_D0–	627	1050	423		CSI4_D1+	541	1050	509
CSI0_D1+	627	1050	423		CSI4_D1–	540	1050	510
CSI0_D1–	626	1050	424		CSI5_CK+	540	1050	510
CSI1_CK+	626	1050	424		CSI5_CK–	539	1050	511
CSI1_CK–	625	1050	425		CSI5_D0+	541	1050	509
CSI1_D0+	627	1050	423		CSI5_D0–	540	1050	510
CSI1_D0–	626	1050	424		CSI5_D1+	541	1050	509

CSI1_D1+	627	1050	423		CSI5_D1–	540	1050	510
CSI1_D1–	626	1050	424		**I2S**			
CSI2_CK+	587	1050	463		I2S3_CLK	472	3600	3128
CSI2_CK–	586	1050	464		I2S3_LRCLK	485	3600	3115
CSI2_D0+	586	1050	464		I2S3_SDIN	497	3600	3103
CSI2_D0–	585	1050	465		I2S3_SDOUT	457	3600	3143
CSI2_D1+	588	1050	462		**SPI**			
CSI2_D1–	587	1050	463		SPI2_SCK	373	1865	1492
CSI3_CK+	587	1050	463		SPI2_MISO	650	1865	1215
CSI3_CK–	586	1050	464		SPI2_CS1#	513	1865	1352
CSI3_D0+	588	1050	462		SPI2_MOSI	649	1865	1216
CSI3_D0–	587	1050	463					
CSI3_D1+	588	1050	462					
CSI3_D1–	587	1050	463					

3.4 Expansion Header

The Jetson TX1 carrier board includes a 40-pin (2x20, 2.54mm pitch) Expansion Header (J21). The connector used on the Carrier board is a Samtec TSM-120-01-S-DV-TR. The expansion connector includes various audio & control interfaces including:

- I2S(See Note)
- Audio Clock/Control
- I2C (x2) (See Note)
- SPI (See Note)
- UART (See Note)

Note: Some of these interfaces can be 1.8V or 3.3V. J14 is a 3-pin header that is used to control the voltage of the level shifter these interfaces pass through. If J14 pin 1-2 are shorted, the interfaces are level shifted to 3.3V. If pins 2-3 are shorted, the interfaces are 1.8V. The 3.3V only interfaces/signals are:

- I2C_GP0_x_3V3_LVL
- I2C_GP1_x_3V3
- UART1_x_HDR_3V3
- GPIO_EXP_P[17:16]_3V3
- MOTION_INT_AP_L_LVL
- SAR_TOUT_LVL

Table 16. Expansion Header Pin Descriptions

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/ Direction	Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/ Direction
1	VDD_3V3_SYS	–	Main 3.3V Supply	Power	2	VDD_5V0_IO_SYS	–	Main 5.0V Supply	Power
3	I2C_GP0_DAT_3V3	I2C_GP0_DAT	General I2C #0 Data (3.3V)	Bidir/OD	4	VDD_5V0_IO_SYS			
5	I2C_GP0_CLK_3V3	I2C_GP0_CLK	General I2C #0 Clock (3.3V)	Bidir/OD	6	GND	–	Ground	Ground
7	AUDIO_I2S_MCLK_3V3	AUDIO_MCLK	Audio Master Clock (1.8/3.3V)	Bidir	8	UART1_TXD_HDR_3V3	UART0_TX	UART #0 Transmit	Output
9	GND	–	Ground	Ground	10	UART1_RXD_HDR_3V3	UART0_RX	UART #0 Receive	Input
11	UART1_RTS_HDR_3V3	UART0_RTS#	UART #0 Request to Send	Output	12	AUDIO_I2S_SRCLK_3V3	I2S0_SCLK	Audio I2S #0 Clock	Bidir
13	AUDIO_CDC_IRQ	GPIO_PE6	Audio Codec Interrupt	Bidir	14	GND	–	Ground	Ground
15	GPIO_EXP_P17_3V3	–	From GPIO Expander (P17)	Bidir	16	AO_DMIC_IN_DAT_LVL	–	Unused	Unused
17	VDD_3V3_SYS	–	Main 3.3V Supply	Power	18	MDM_WAKE_AP_LVL	GPIO16_MDM_WAKE_AP	Modem Wake AP GPIO	Input
19	SPI1_MOSI_3V3	SPI1_MOSI	SPI #1 Master Out/Slave In (1.8/3.3V)	Bidir	20	GND	–	Ground	Ground
21	SPI1_MISO_3V3	SPI1_MISO	SPI #1 Master In/Slave Out (1.8/3.3V)	Bidir	22	GPIO_EXP_P16_3V3	–	From GPIO Expander (P16)	Bidir
23	SPI1_SCK_3V3	SPI1_CLK	SPI #1 Shift Clock (1.8/3.3V)	Bidir	24	SPI1_CS0_3V3	SPI1_CS0#	SPI #1 Chip Select #0 (1.8/3.3V)	Bidir
25	GND	–	Ground	Ground	26	SPI1_CS1_3V3	SPI1_CS1#	SPI #1 Chip Select #1 (1.8/3.3V)	Bidir
27	I2C_GP1_DAT_3V3	I2C_GP1_DAT	General I2C #1 Data (3.3V)	Bidir/OD	28	I2C_GP1_CLK_3V3	I2C_GP1_CLK	General I2C #1 Clock (3.3V)	Bidir/OD
29	AUD_RST	GPIO19_AUD_RST	Audio Reset (1.8/3.3V)	Output	30	GND	–	Ground	Ground
31	MOTION_INT_AP_L	GPIO9_MOTION_INT	Motion Interrupt (3.3V)	Input	32	AO_DMIC_IN_CLK	–	Unused	Unused
33	AP_WAKE_BT_3V3	GPIO11_AP_WAKE_BT	AP Wake Bt GPIO	Bidir	34	GND	–	Ground	Ground
35	AUDIO_I2S_SFSYNC_3V3	I2S0_LRCLK	AUDIO I2S #0 Left/Right Clock	Bidir	36	UART1_CTS_HDR_3V3	UART0_CTS#	UART #0 Clear to Send	Input
37	SAR_TOUT	GPIO8_ALS_PROX_INT	(3.3V)	Output	38	AUDIO_I2S_SIN_3V3	I2S0_SDIN	Audio I2S #0 Data in	Input

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/ Direction	Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/ Direction
39	GND	–	Ground	Ground	40	AUDIO_I2S_SOUT_3V3	I2S0_SDOUT	Audio I2S #0 Data Out	Output

Notes: - In the Type/Dir column, Output is to Expansion Module. Input is from Expansion Module. Bidir is for Bidirectional signals.

Expansion Header Interface Guidelines

See the Jetson TX1 OEM Product DG for Routing Guidelines. Include the Carrier board PCB trace delays in the following table when calculating max trace length & for skew matching.

Table 17. Expansion Header Related TX1 Carrier PCB Trace Delays

Jetson TX1 Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for Expansion Module (ps)		Jetson TX1 Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for Expansion Module (ps)
I2S					**SPI**			
I2S0_CLK	69	3600	3531		SPI1_SCK	791	1865	1074
I2S0_LRCLK	150	3600	3450		SPI1_MISO	782	1865	1083
I2S0_SDIN	60	3600	3540		SPI1_MOSI	783	1865	1082
I2S0_SDOUT	127	3600	3473		SPI1_CS0#	786	1865	1079
					SPI1_CS1#	791	1865	1074

3.5 Debug Connector

The carrier board includes a 60-pin (2x30, 0.5mm pitch) Debug Connector (J10). The connector used on the Carrier board is a Samtec QSH-30-01-L-D-A-TR. The debug connector includes the following interfaces/functions:

- JTAG
- UART
- I2C (x3) (See Note)
- Power, Force Recovery & Reset Control
- GPIOs

Table 18. Debug Connector Pin Descriptions

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default
1	ACOK	CHARGER_PRSNT#	AC power OK	Input	2	VDD_1V8	–	Main 1.8V Supply	Power
3	GND	–	Ground	Ground	4	GND	–	Ground	Ground
5	JTAG_AP_TDI	JTAG_TDI	JTAG Test Data In	Input	6	UART1_TXD_DBG_1V8	UART0_TX	UART #0 Transmit	Output
7	JTAG_AP_TMS	JTAG_TMS	JTAG Test Mode Select	Input	8	UART1_RXD_DBG_1V8	UART0_RX	UART #0 Receive	Input
9	JTAG_AP_TCK	JTAG_TCK	JTAG Test Clock	Input	10	UART1_CTS	UART0_CTS#	UART #0 Clear to Send	Input
11	JTAG_AP_RTCK	JTAG_RTCK	JTAG Return Clock	Output	12	UART1_RTS	UART0_RTS#	UART #0 Request to Send	Output
13	GND	–	Ground	Ground	14	GND	–	Ground	Ground
15	JTAG_AP_TDO	JTAG_TDO	JTAG Test Data Out	Output	16	I2C_GP0_CLK_1V8	I2C_GP0_CLK	General I2C #0 Clock	Bidir/OD
17	RESET_IN_R_L	–	Reset Input	Bidir	18	I2C_GP0_DAT_1V8	I2C_GP0_DAT	General I2C #0 Data	Bidir/OD
19	GND	–	Ground	Ground	20	NC	–	Unused	Unused
21	VDD_1V8	–	Main 1.8V Supply	Power	22	NC			
23	I2C_PM_DAT	I2C_PM_DAT	I2C Interface (PM) Data	Bidir/OD	24	GND	–	Ground	Ground
25	I2C_PM_CLK	I2C_PM_CLK	I2C Interface (PM) Clock	Bidir/OD	26	VDD_1V8	–	Main 1.8V Supply	Power
27	UART2_TXD_DBG	UART2_TX	UART #2 Transmit	Output	28	LED_VDD_CORE	–	Enable for SOC EN LED	Output
29	UART2_RXD_DBG	UART2_RX	UART #2 Receive	Input	30	NC	–		Unused
31	LED_VDD_CORE	–	Enable for SOC Enable LED	Output	32	DBG_GPIO1	UART0_CTS	UART #0 Clear to send	Input
33	CPU_PWR_REQ	–	Tied to GND	na	34	DBG_GPIO2	UART0_RTS	UART #0 Request to send	Output
35	GND	–	Ground	Ground	36	GND	–	Ground	Ground
37	NC				38	NC	–	Unused	Unused
39	NC				40	RESET_IN_R_L	RESET_IN#	From Reset Button/JTAG Conn.	Input
41	NC	–	Unused	Unused	42	FORCE_RECOVERY_R_L	FORCE_RECOV#	From Recovery button	Input
43	NC				44	RESET_IN_R_L	RESET_IN#	From Reset Button/JTAG Conn.	Input
45	NC				46	POWER_BTN_R	POWER_BTN#	From Power Button	Input

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default
47	NC				48	NC	–	Unused	Unused
49	NC				50	NC			
51	GND	–	Ground	Ground	52	GND	–	Ground	Ground
53	JTAG_AP_TRST_L	JTAG_GP0	Debug GPIO #0	Input	54	I2C_GP1_CLK_3V3	I2C_GP1_CLK	General I2C #1 Clock	Bidir/OD
55	D_FORCE_OFF_L	–	Force Off	Input	56	I2C_GP1_DAT_3V3	I2C_GP1_DAT	General I2C #1 Data	Bidir/OD
57	NC	–	Unused	Unused	58	GND	–	Ground	Ground
59	NC				60	VAUX_5V	–	5V Supply from Debug Conn.	Power

Notes: In the Type/Dir column, Output is to Debug Module. Input is from Debug Module. Bidir is for Bidirectional signals.

Debug Connector Interface Guidelines

See the Jetson TX1 OEM Product DG for Routing Guidelines. Include the Carrier board PCB trace delays when calculating max trace length & for skew matching.

3.6 GPIO Expansion Header

The carrier board includes a 30-pin (2x15, 2.54mm pitch) GPIO Expansion Header (J26) including an I2S IF and several GPIOs.

Table 19. GPIO Expansion Header Pin Descriptions

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default
1	NC	–	Unused	Unused	2	VDD_3V3_SYS	–	Main 3.3V Supply	Power
3	NC				4	VDD_1V8		Main 1.8V Supply	
5	NC				6	AP2MDM_READY	GPIO15_AP2MDM_READY	AP to Modem Ready GPIO	Bidir
7	NC				8	VDD_5V0_IO_SYS	–	Main 5.0V Supply	Power
9	NC				10	GND	–	Ground	Ground
11	GND	–	Ground	Ground	12	NC	–	Unused	Unused
13	NC	–	Unused	Unused	14	NC			
15	NC				16	NC			
17	NC				18	NC			
19	NC				20	NC			
21	GND	–	Ground	Ground	22	SLEEP	SLEEP#	Sleep Indicator	Output
23	I2S1_CLK	I2S1_CLK	I2S #1 Clock	Bidir	24	I2S1_SDOUT	I2S1_SDOUT	I2S #1 Data Out	Bidir
25	I2S1_SDIN	I2S1_SDIN	I2S #1 Data In	Input	26	I2S1_LRCLK	I2S1_LRCLK	I2S #1 Left/Right Clock	Bidir
27	DSPK_OUT_CLK	–	Unused	Unused	28	GND	–	Ground	Ground
29	DSPK_OUT_DAT	–	Unused	Unused	30	GNSS_PPS	–	Unused	Unused

Notes: In the Type/Dir column, Output is from GPIO Module. Input is to GPIO Module. Bidir is for Bidirectional signals.

GPIO Header Interface Guidelines

See the Jetson TX1 OEM Product DG for Routing Guidelines. Include the Carrier board PCB trace delays in the following table when calculating max trace length & for skew matching.

Table 20. GPIO Header Related TX1 Carrier PCB Trace Delays

Jetson TX1 Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Avail. Trace Delay for GPIO Module (ps)
I2S			
I2S1_CLK	900	3600	2700
I2S1_SDIN	893	3600	2707
I2S1_SDOUT	916	3600	2684
I2S1_LRCLK	911	3600	2689

3.7 Serial Port

UART1 from Jetson TX1 is routed through level shifters to a 6-pin, 2.54mm pitch male Serial Port header (J17). The connector used on the carrier board is a Samtec HTSW-106-07-FM-S.

Figure 14. Serial Port Header Connections

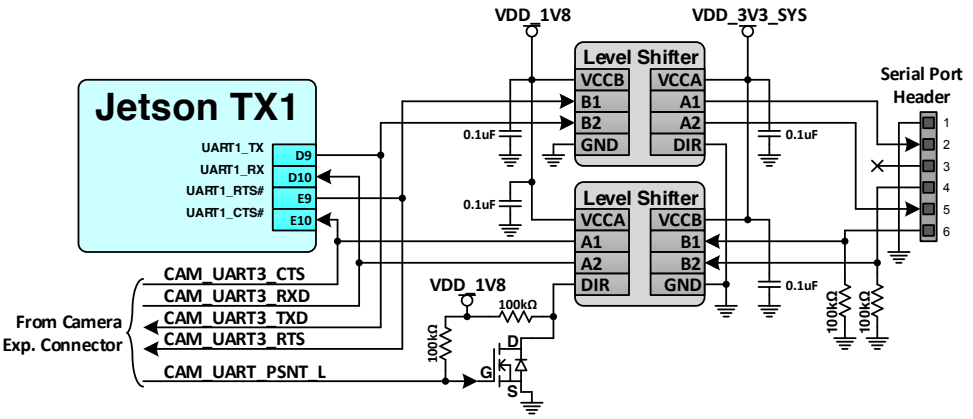


Table 21. Serial Port Header Descriptions

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default
1	SHIELD/GND	–	Ground	Ground
2	UART3_RTS_3V3_L	UART1_RTS#	UART Return to Send	Output
3	NC	–	Unused	Unused
4	UART3_RXD_3V3	UART1_RX	UART Receive	Input
5	UART3_TXD_3V3	UART1_TX	UART Transmit	Output
6	UART3_CTS_3V3_L	UART1_CTS#	UART Clear to Send	Input

Notes: In the Type/Dir column, Output is to Serial Port header. Input is from Serial Port header. Bidir is for Bidirectional signals.

3.8 Charge Control Receptacle

The Jetson TX1 carrier board includes a 10-pin Flex Receptacle (J27) including an I2C IF & charge control/status signals.

Table 22. Charge Control Receptacle Pin Descriptions

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default
1	ACOK	CHARGER_PRSNT#	AC power OK	Input	6	I2C_PM_DAT	I2C_PM_DAT	I2C (Power Monitor) Data	Bidir/OD
2	CHARGING	CHARGING#	Charging indicator	Input	7	NC	–	Unused	Unused
3	LOW_BAT	BATLOW#	Low Battery indicator	Input	8	BAT_DET_L	–	Pulled up to VDD_3V3_SYS	Na
4	GND	–	Ground	Ground	9	TYPEC_INT	–	From GPIO Expander (P02)	Output
5	I2C_PM_CLK	I2C_PM_CLK	I2C (Power Monitor) Clock	Bidir/OD	10	CHG_BD_PRSNT_L	–	From GPIO Expander (P14)	Output

Notes: In the Type/Dir column, Output is to Charger Ctrl board. Input is from Charger Ctrl board. Bidir is for Bidirectional signals.

Charge Receptacle Interface Guidelines

See the Jetson TX1 OEM Product DG for Routing Guidelines. Include the Carrier board PCB trace delays when calculating max trace length & for skew matching.

3.9 Fan Connector

The Jetson TX1 carrier board includes a 4-pin Fan Header (J15).

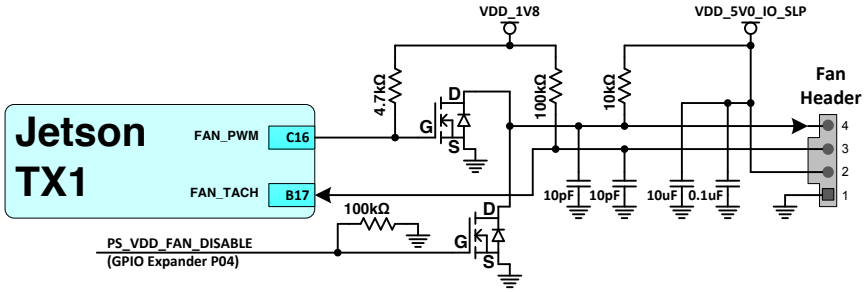


Table 23. Fan Connector Pin Descriptions

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default
1	GND	–	Ground	Ground
2	VDD_5V0_IO_SLP	–	Gated version of Main 5.0V Supply (Enabled by VDD_3V3_SLP)	Power
3	FAN_TACH	FAN_TACH	Fan Tachometer signal	Input
4	FAN_PWM_Q*	FAN_PWM	Fan Pulse Width Modulation signal	Output

Notes: In the Type/Dir column, Output is to Fan Connector. Input is from Fan Connector. Bidir is for Bidirectional signals.

3.10 DC Power Jack

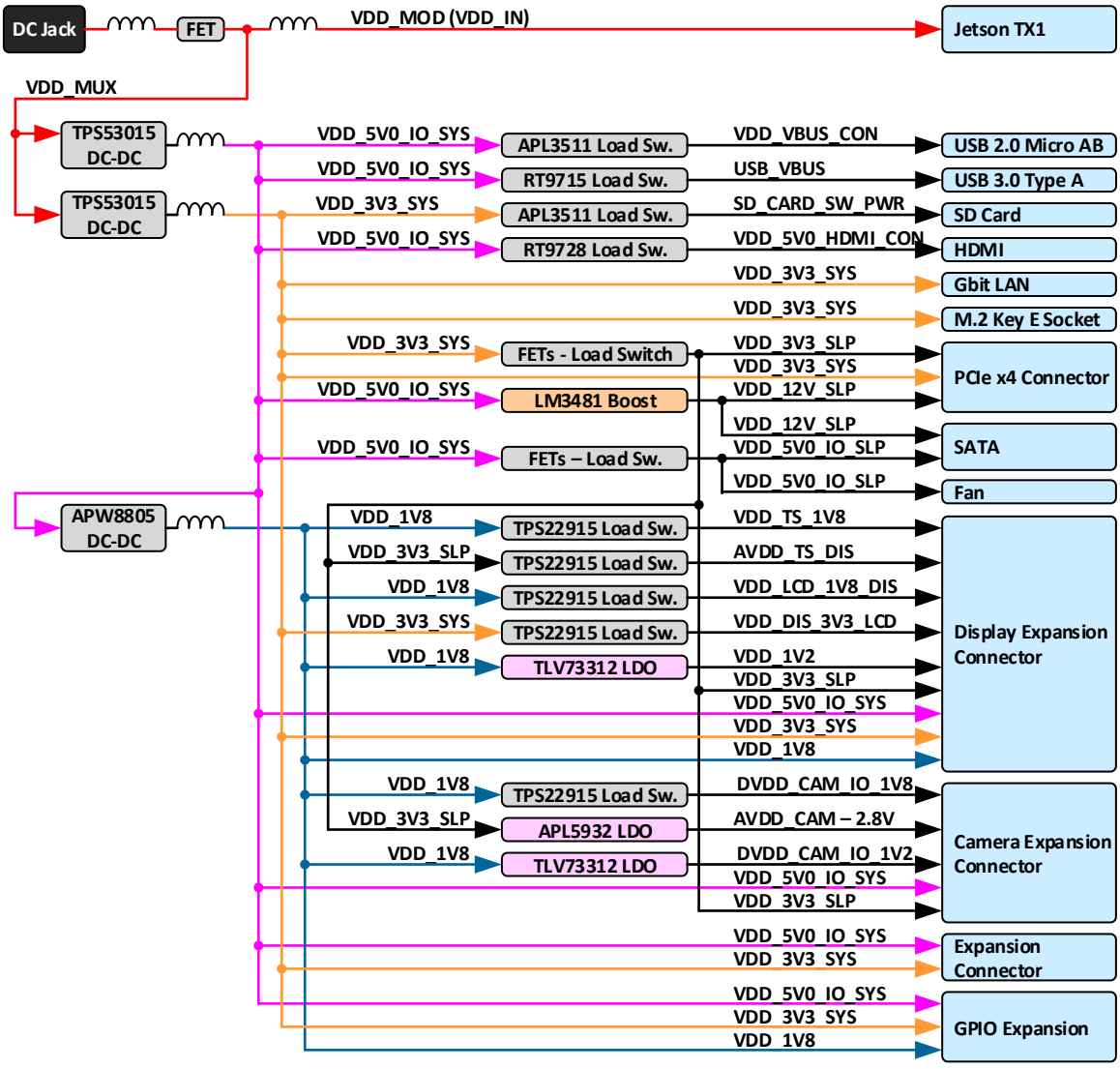
The Jetson TX1 carrier board uses a DC power jack (J25) to bring in the power from the included DC power supply. The jack used on the Carrier board is a Singatron Enterprise 2DC-213-B51. The mating plug is the Singatron Enterprise 2DP-313-B01.

Table 24. DC Jack Pin Descriptions

Pin #	Signal Name	Jetson TX1 Pin Name	Usage/Description	Type/Dir Default
1	VDD_19V_CON	–	Main DC input supplying VDD_IN/VDD_MOD	Power
2	GND	–	Ground	Ground
3	GND	–	Ground	Ground
4	GND	–	Ground	Ground
5	GND	–	Ground	Ground
6	GND	–	Ground	Ground

4.0 INTERFACE POWER

Figure 15. Interface Connector Power Diagram



The table below shows the allocation of supplies to the connectors on the Jetson TX1 carrier board.

Table 25 Interface Power Supply Allocation

#	Power Rails	Usage	(V)	Power Supply or Gate	Source	Enable	Max Current (mA)
1	**VDD_IN/VDD_MUX**	Main power input from DC Adapter	5.5-19.6	FETs	**DC Adapter**		~4000
2	**VDD_5V0_IO_SYS**	Main 5V supply	5.0	TPS53015	**VDD_MUX**	CARRIER_PWR_ON	7000
3	**VDD_3V3_SYS**	Main 3.3V supply	3.3	TPS53015	**VDD_MUX**	3V3_SYS_BUCK_EN	7000
4	**VDD_1V8**	Main 1.8V supply	1.8	APW8805	**VDD_5V0_IO_SYS**	1V8_IO_VREG_EN (VDD_3V3_SYS_PG)	2000
5	**VDD_3V3_SLP**	3.3V rail, off in Deep Sleep (various)	3.3	FETs	**VDD_3V3_SYS**	SOC_PWR_REQ	
6	**VDD_5V0_IO_SLP**	5V rail, off in Deep Sleep, for SATA/FAN	5.0	FETs	**VDD_5V0_IO_SYS**	SOC_PWR_REQ	
7	**VDD_12V_SLP**	12V rail for PCIe x4 & SATA	12.0	LM3481MMX Boost	**VDD_5V0_IO_SYS**	VDD_3V3_SLP	2300
8	**VDD_VBUS_CON**	5V VBUS for USB 2.0 Type AB conn.	5.0	APL3511CBI Load Switch	**VDD_5V0_IO_SYS**	USB_VBUS_EN0	
9	**USB_VBUS**	5V VBUS for USB 3.0 Type A conn.	5.0	RT9715 Load Switch	**VDD_5V0_IO_SYS**	USB_VBUS_EN1	
10	**SD_CARD_SW_PWR**	SD Card power rail	3.3	APL3511DBI Load Switch	**VDD_3V3_SYS**	SDCARD_VDD_EN	
11	**VDD_5V0_HDMI_CON**	5V rail for HDMI connector		RT9728 Load Switch	**VDD_5V0_IO_SYS**	5V0_HDMI_EN (GPIO Expander U32, P14)	
12	**VDD_TS_1V8**	1.8V rail for touch screen		TPS22915 Load Switch	**VDD_1V8**	EN_VDD_TS_1V8_PMIC (GPIO Expander U32, P01)	
13	**AVDD_TS_DIS**	High voltage rail for touch screen	3.3	TPS22915 Load Switch	**VDD_3V3_SLP**	EN_VDD_TS_HV_PMIC (GPIO Expander U32, P02)	
14	**VDD_LCD_1V8_DIS**	1.8V rail for panel		TPS22915 Load Switch	**VDD_1V8**	VDD_LCD_1V8_EN (GPIO Expander U32, P11)	
15	**VDD_DIS_3V3_LCD**	High voltage rail for panel		TPS22915 Load Switch	**VDD_3V3_SYS**	EN_VDD_DISP (GPIO Expander U32, P03)	
16	**VDD_1V2**	Generic 1.2V display rail	1.2	TLV73312 LDO	**VDD_1V8**	DIS_VDD_1V2_EN (GPIO Expander U32, P12)	
17	**VDD_SYS_BL**	Rail to LCD backlight driver	Device Depend.	Stuffing option Resistors	**VDD_MUX VDD_5V0_IO_SYS**	Na	
18	**DVDD_CAM_IO_1V8**	1.8V rail for camera I/O	1.8	TPS22915 Load Switch	**VDD_1V8**	CAM_VDD_1V8_EN (GPIO Expander U31, P11)	1000
19	**AVDD_CAM**	High voltage rail for cameras	2.8	APL5932	**VDD_3V3_SLP**	CAM_AVDD_CAM_EN (GPIO Expander U32, P15)	1000
20	**DVDD_CAM_IO_1V2**	1.2V rail for camera I/O	1.2	TLV73312	**VDD_1V8**	CAM_VDD_1V2_EN (GPIO Expander U31, P12)	200

Note:
1. When operated near the minimum voltage, the power supported by some of the supplies may be reduced.
2. The supplied power adapter is rated to 90W.
3. The values shown in the “Supported Current” column indicate the total power available on the expansion connectors (not per pin).
4. If a given voltage rail cannot provide enough current, a possible solution is for the user to use a regulator from VDD_5V0_IO_SYS, VDD_3V3_SYS or VDD_1V8 to generate the desired rail.

5.0 QUICK-START GUIDE

Introduction

The NVIDIA Jetson TX1 Developer Kit is a full-featured development platform for visual computing. It is ideal for applications requiring high computational performance in a low power envelope. The Jetson TX1 Developer kit is designed to get you up and running quickly: It comes pre-flashed with a Linux environment, includes support for many common APIs, and is supported by NVIDIAs complete development tool chain. The board exposes many standard hardware interfaces, enabling a highly flexible and extensible platform.

Go to http://developer.nvidia.com/jetson-tx1 for access to software updates and the developer SDK supporting the OS image and host development platform that you want to use. The SDK includes an OS image that you will load onto your device, developer tools, supporting documentation, and code samples to help you get started.

Getting Started

Individual development efforts will vary and may result in modifications to the system configuration. It is recommended that you begin with the basic system configuration (as shipped) to ensure proper system operation prior to any further development

CAUTION: The NVIDIA® Jetson TX1 developer board contains ESD-sensitive parts. Always use appropriate anti-static and grounding techniques when working with the system. Failure to do so can result in ESD discharge to sensitive pins, and irreparably damage your Jetson TX1 board. NVIDIA will not replace units that have been damaged due to ESD discharge. Always disconnect any power source prior to adding additional modules or connecting peripheral devices to the developer board. It is important that all modules are properly seated in their connectors to ensure proper operation and to avoid damaging the module or the developer board.

Obtaining Support

The Jetson TX1 Developer Kit is supported via NVIDIA's Embedded Developer Zone at:

https://developer.nvidia.com/embedded-computing

Powering Up the Jetson TX1 Developer Kit

1. Connect a USB keyboard to the USB Type A connector of your device
2. Connect an HDMI-compatible display to the HDMI connector on your device
3. Connect the AC adapter supplied in your kit to the power connector of your device
4. Plug the power adapter into an appropriately rated electrical outlet
5. They system should power on. If not, press and release the power button on the device

Login Credentials

Username: ubuntu

Password: ubuntu

Notes: Note: Login is not required on the serial console. Please plan physical security accordingly.

Force Recovery Mode

To update your system, you will need to be in Force USB Recovery Mode so you can transfer system software to the developer board. When in Force USB Recovery Mode, you are able to update system software and write the boot loader, boot configuration table (BCT), and partition configuration to the device.

See the Platform Software documentation for OS specific instructions when updating system software on your developer board.

CAUTION: ALWAYS CONNECT ALL EXTERNAL PERIPHERAL DEVICES BEFORE CONNECTING THE POWER SUPPLY TO THE AC/DC JACK. Connecting a device while powered on may damage the developer board or peripheral device.

To place system in Force USB Recovery Mode:

1. Power down the device. If connected, remove the AC adapter from the device. The device MUST be powered OFF, not in a suspend or sleep state.
2. Connect the Micro-B plug on the USB cable to the Recovery (USB Micro-B) Port on the device and the other end to an available USB port on the host PC.
3. Connect the power adapter to the device.
4. Press and release the POWER button, if necessary; press and hold the RECOVERY FORCE button; while depressing the RECOVERY FORCE button, press and release the RESET button; wait two seconds and release the RECOVERY FORCE button.

Notes: When in Force USB Recovery Mode, the development system will not boot up (nothing appears on display or serial port).

After successfully updating the system software and restarting your developer board, the system will continue through the boot up process.

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