DESIGN GUIDE

NVIDIA Jetson TX1 Product OEM Design Guide

Abstract

This document contains recommendations and guidelines for Engineers to follow to create a product that is optimized to achieve the best performance from the common interfaces supported by the NVIDIA® Jetson TX1.

This document provides detailed information on the capabilities of the hardware module, which may differ from supported configurations by provided software. Refer to software release documentation for information on supported capabilities.

Document Change History

Date	Description
NOV, 2015	Release
JAN, 2016	**Section 2.1: Overview** - Updated table to correct sharing between USB 3.0 & PCIe. - Removed redundant mention of PCIe WAKE **Section 3.0: Jetson TX1 Pin Descriptions** - Highlighted VDD_RTC (A50) in red to indicate power rail **Section 4.0: Power** - Added caution that Jetson TX1 is not hot-pluggable - Corrected Jetson TX1 pin # swap for RESET_IN# & RESET_OUT# **Section 4.1: Jetson TX1 Power & Control** - Updated VIN_PWR_BAD# usage description in table **Section 4.3: Power Sequence** - Added earlier timeslot for VDD_IN & shifted other timings over one slot. - Show POWER_BTN# as low then indeterminate before VIN_PWR_BAD# goes inactive. - Power Discharge figure: Updated components/values/tolerances to match latest reference design. **Section 6.0: USB, PCIe & SATA** - Corrected Jetson TX1 module pin name for Lane 1 to PEX_RFU in USB 3.0, PCIe, & SATA lane mapping table - Swapped to have Jetson TX1 names in first row & Tegra X1 Lanes below - Added note that x4/x2 lane interfaces can be used instead as single x2 or x1 interfaces - Added forward compatible USB 3.0, PCIe & SATA lane mapping table - Moved notes below both mapping tables. **Section 6.1: USB** - Updated figure to show 100ohm series resistor on USB_VBUS_EN[1:0] between EN & OC - Updated USB 3.0 Routing Requirements o Tightened intra-pair skew & intra-pair matching between subsequent discontinuities requirements o Added location requirement for AC cap o Removed requirements for number of vias & signal to reference o Added ESD layout recommendations o Added additional Serpentine parameters/details o Removed additional requirements table (combined into single table) o Removed separate ESD & CMC requirements tables as these are included in main table. **Section 6.2: Gigabit Ethernet** - Added example connections for Magnetics & RJ45 connector. **Section 6.3: PCIe** - Updated routing requirements o Reorganized requirements into different groups & combined main & additional requirement tables o Removed Connector Breakout area requirement o Tightened intra-pair skew & intra-pair matching between subsequent discontinuities requirements o Updated requirement for location of AC cap **Section 6.4: SATA** - Added discharge circuitry to connections figure for VDD_5V0_IO_SLP & VDD_12V_SLP rails - Added note to ensure customers not only meet routing requirements, but do not use different UPHY settings - Reorganized requirements into different groups & added Serpentine rules - Tightened intra-pair skew & intra-pair matching between subsequent discontinuities requirements **Section 7.3: HDMI/DP** - Corrected swapped pin assignments for DP1_TX[3:0]+/- (Separated +/- into different rows for clarity) **Section 9.0: SDIO/SDCARD/EMMC** - Updated in Interface Mapping table to change the way SDMMC2 & SDMMC4 on-module usage is indicated - Updated note under Connections table to match what is done on latest carrier board **Section 10.0: Audio** - Updated Interface Mapping table to Add Tegra X1 functions & changed the way the on-module I2S is described - Corrected pin names for Reset & Interrupt in connections table **Section 12.1: I2C** - Corrected pin # swap (+ & -) for DP0_AUX_CH & DP1_AUX_CH in figure **Section 12.3: UART** - Corrected pin # for UART1_RX in figure **Section 12.5: Strapping Pins** - Renamed Buttons & Strapping section to just Strapping Pins - Updated figure to show all Tegra strapping pin connections & which are brought out on Jetson TX1 - Updated table to include all Tegra strapping pins - Added notes with restrictions for using any of the Tegra strap pins that are brought out on Jetson TX1 in a design **Section 13: Pads** - Added note related to possible glitches on GPIOs used as output when associated power rail enabled

Date	Description
MAR, 2016	**Section 3.0: Jetson TX1 Pin Descriptions** - Added optional USB options on SATA & PEX1 pins. - Corrected USB controller option for USB_SS1 & changed PCIe to indicate controller lane **Section 4.0: Power** - Updated caution related to no hot-plug support to include recommended minimum time after power-off before installing/removing module - Updated "Power Block Diagram" & "Power & Power Control" table to include CHARGER_PRSNT# which is optionally used for Auto-Power-On support. **Section 4.1: Jetson TX1 Power & Control** - Updated usage for POWER_BTN# & SLEEP# to remove mention of driver on carrier board **Section 4.2: Supply Allocation** - Corrected Usage for VDD_5V0_SYS & VDD_3V3_SYS to indicate supplies for Jetson TX1, not carrier board - Updated VDD_RTC voltage to include Var (variable) **Section 4.4: Power Discharge** - Moved power discharge for VDD_12V_SLP & VDD_5V0_IO_SLP from SATA section to Power Discharge figure **Section 4.4.4: Power & Voltage Monitoring** - Updated resistor values on VDD_IN & VDD_1V8 inputs to voltage monitor & added note with threshold. **Section 4.7: Optional Auto-Power-On Support** - Added new section describing optional circuit options for auto-power-on **Section 6.0: USB, PCIE & SATA** - Changed heading to PCIe - Added intro paragraph explaining what tables show - Changed from Use Cases to Configs in mapping tables - Removed incorrect note references in Forward Compatible table - Updated configurations in note 1 to match updated Config #s in table Forward Compatible table **Section 6.3: PCIe** - Corrected swap between lanes 2 & 3 for x4 configuration in connection table **Section 6.4: SATA** - Removed VDD_5V0_IO_SLP & VDD_12V_SLP discharge circuitry (moved to power discharge section) - Removed gating used to create VDD_5V0_IO_SLP - Added max # through-hole vias & GND via placement requirements **Section 9.1: SD Card** - Corrected Tegra data order to match Jetson TX1 order in figure. - Removed pull-down on SDCARD_CLK on Jetson TX1 **Section 10.0: Audio** - Added I2S3 to connection figure - Removed beads from clocks in figure & connection table to match Jetson TX1 design **Section 12.4: Debug** - Updated figure & moved before JTAG & new Debug UART sections. - Level shifter shown on UART along with note requiring pull-ups on inputs - RST pin of JTAG shown driving to Jetson TX1 for system reset - Optional pull-ups on UART TXD/RTS lines shown for RAM Code strapping along with note - Added Debug UART section with connection table **Section 12.5: Strapping** - Added note below Strapping Breakdown table describing eMMC boot mechanism **Section 16.0: Design Checklist** - - Updated Jetson TX1 Signal Terminations section o Added I2C_CAM_CLK/DAT, SPI2_MOSI/MISO/CLK rows o Changed parallel termination for SPI2_CS[1:0] to external 100kohm pull-ups o Changed value of pull-down on JTAG_GP0 - Updated Carrier Board Signal Terminations section o * Added parallel terminations & resistor in series terminations for DP[1:0] in DP[1:0] for DP/eDP section o * Added resistor in series terminations for HDMI_HPD in DP1 for HDMI section - Updated Carrier Board Supplies section o * Corrected enable for VDD_5V0_IO_SLP o * corrected GPIO Expander device reference numbers - Corrected ball names for RX pins in PCIe section in Unused Special Function Interface Pins table - Corrected pin names for SDCARD_WP, DP[1:0]_TX, GPIO4_CAM_STROBE, GPIO3_CAM1_RST# - Corrected I2S to include I2S3 in Audio section - Reworded check item in Strapping section

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1.0 INTRODUCTION

1.1 References

Refer to the documents or models listed in Table 1 for more information. Use the latest revision of all documents at all times.

Table 1. List of Related Documents

Document
Jetson TX1 Data Sheet
Jetson TX1 PinMux

1.2 Abbreviations and Definitions

Table 2 lists abbreviations that may be used throughout this document and their definitions.

Table 2. Abbreviations and Definitions

Abbreviation	Definition
BT	Bluetooth
CEC	Consumer Electronic Control
DP	Display Port
DTV	Digital Television
eDP	Embedded Display Port
eMMC	Embedded MMC
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
HDMI	High Definition Multimedia Interface
I2C	Inter IC
I2S	Inter IC Sound Interface
LCD	Liquid Crystal Display
LDO	Low Dropout (voltage regulator)
LPDDR4	Low Power Double Data Rate DRAM, Fourth-generation
PCIe (PEX)	Peripheral Component Interconnect Express interface
PCM	Pulse Code Modulation
PHY	Physical Interface (i.e. USB PHY)
PMC	Power Management Controller
PMU	Power Management Unit
RF	Radio Frequency
RTC	Real Time Clock
SATA	Serial "AT" Attachment interface
SDIO	Secure Digital I/O Interface
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
Wi-Fi (WLAN)	Wireless Local Area Network

2.0 JETSON TX1

2.1 Overview

The Jetson TX1 resides at the center of the embedded system solution and includes:

- Power (PMIC/Regulators, etc.)
- DRAM (LPDDR4)
- eMMC
- Connects to 802.11ac Wi-Fi and Bluetooth enabled devices
- Gigabit Ethernet Controller
- Power Monitor
- Thermal Sensor

In addition, a wide range of interfaces are available at the main connector for use on the carrier board as shown below.

Table 3. Jetson TX1 Interfaces

Category	Function		Category	Function
USB	USB 2.0 Interface [x3]		**SD Card**	SD Card Interface
	USB 3.0 (up to x3 – two shared w/PCIe or SATA)		**LAN**	Gigabit Ethernet
PCIe	Control [x2]		**I2C**	3x
	Wake (shared)		**UART**	3, x4-pin
	PCIe (1x1 + 1x1/2/4, shared w/USB 3.0)		**SPI**	3x
Camera	CSI (6 x2 or 3 x4)		**SATA**	SATA
	Control, Clock		**Wi-Fi/BT/Modem**	SDIO/PEX/UART/I2S
Display	eDP/DP Interface			Control/handshake
	HDMI/DP Interface (w/CEC)		**Touch**	Touch Clock, Interrupt & Reset
	DSI (2, x4)		**Sensor**	Control & Interrupt
	Display/Backlight Control		**Fan**	FAN PWM & Tach Input
Audio	I2S Interface (x4)		**Debug**	JTAG, UART
	Control & Clock		**System**	Power Control, Reset, alerts
			Power	Main Input

Figure 1. Jetson TX1 Block Diagram

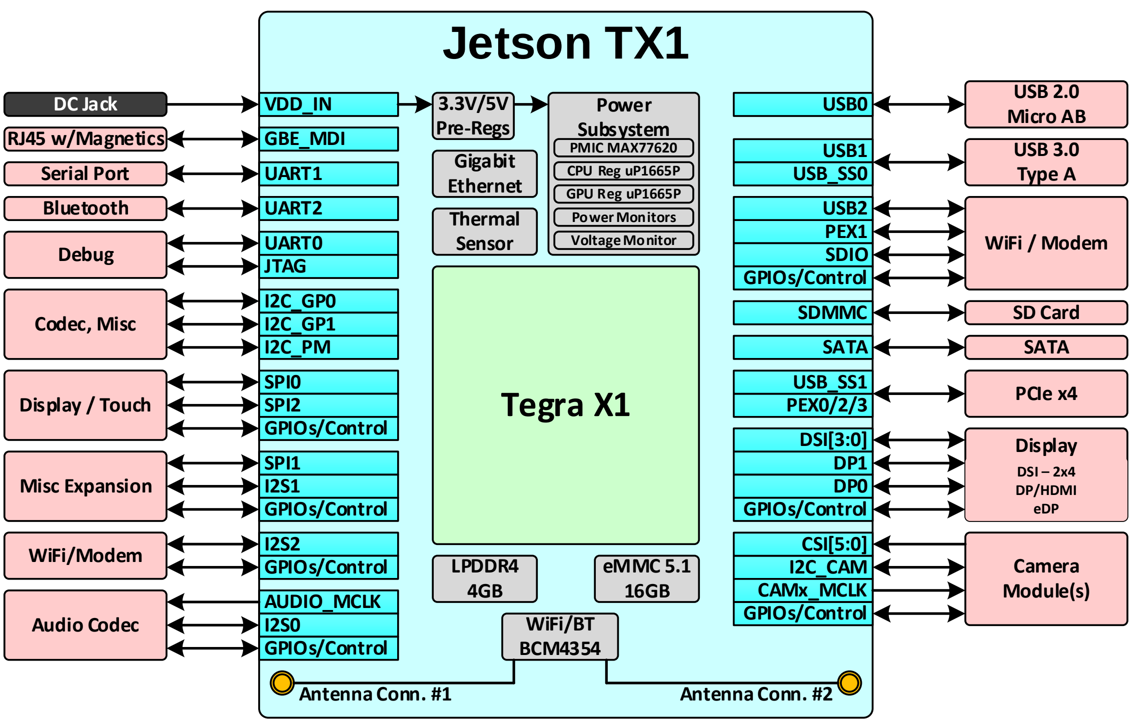


Table 4. Jetson TX1 Connector (8x50) Pin Out Matrix

	A	B	C	D	E	F	G	H
1	VDD_IN	VDD_IN	VDD_IN	RSVD	FORCE_RECOV#	AUDIO_MCLK	I2S0_SDIN	I2S0_LRCLK
2	VDD_IN	VDD_IN	VDD_IN	RSVD	SLEEP#	GPIO19_AUD_RST	I2S0_CLK	I2S0_SDOUT
3	GND	GND	GND	RSVD	SPI0_CLK	SPI0_CS0#	GND	GPIO20_AUD_INT
4	GND	GND	GND	RSVD	SPI0_MISO	SPI0_MOSI	RSVD	RSVD
5	RSVD	RSVD	RSVD	RSVD	I2S3_SDIN	I2S3_LRCLK	I2S2_CLK	I2S2_LRCLK
6	I2C_PM_CLK	I2C_PM_DAT	I2C_CAM_CLK	I2C_CAM_DAT	I2S3_CLK	I2S3_SDOUT	I2S2_SDIN	I2S2_SDOUT
7	CHARGING#	CARRIER_STBY#	BATLOW#	GPIO5_CAM_FLASH_EN	RSVD	GPIO1_CAM1_PWR#	GPIO4_CAM_STROBE	GPIO3_CAM1_RST#
8	GPIO14_AP_WAKE_MDM	VIN_PWR_BAD#	RSVD	RSVD	RSVD	CAM1_MCLK	GPIO0_CAM0_PWR#	GPIO2_CAM0_RST#
9	GPIO15_AP2MDM_READY	GPIO17_MDM2AP_READY	RSVD	UART1_TX	UART1_RTS#	CAM0_MCLK	UART3_CTS#	UART3_RX
10	GPIO16_MDM_WAKE_AP	GPIO18_MDM_COLDBOOT	RSVD	UART1_RX	UART1_CTS#	GND	UART3_RTS#	UART3_TX
11	RSVD	JTAG_TCK	RSVD	RSVD	RSVD	RSVD	UART0_RTS#	UART0_CTS#
12	JTAG_TMS	JTAG_TDI	RSVD	RSVD	RSVD	RSVD	UART0_RX	UART0_TX
13	JTAG_TDO	JTAG_GP0	RSVD	I2S1_LRCLK	SPI1_CS1#	SPI1_MOSI	SPI1_CLK	GPIO8_ALS_PROX_INT
14	JTAG_RTCK	GND	I2S1_SDIN	I2S1_SDOUT	SPI1_CS0#	SPI1_MISO	GPIO9_MOTION_INT	SPI2_CLK
15	UART2_CTS#	UART2_RX	I2S1_CLK	I2C_GP0_DAT	I2C_GP0_CLK	GND	SPI2_MOSI	SPI2_MISO
16	UART2_RTS#	UART2_TX	FAN_PWM	RSVD	RSVD	SPI2_CS1#	SPI2_CS0#	SDCARD_PWR_EN
17	USB0_EN_OC#	FAN_TACH	RSVD	RSVD	RSVD	SDCARD_CD#	GND	SDCARD_D1
18	USB1_EN_OC#	RSVD	RSVD	RSVD	RSVD	SDCARD_D3	SDCARD_CLK	SDCARD_D0
19	RSVD	GPIO11_AP_WAKE_BT	RSVD	RSVD	GND	SDCARD_D2	SDCARD_CMD	GND
20	I2C_GP1_DAT	GPIO10_WIFI_WAKE_AP	RSVD	GND	CSI5_D1-	SDCARD_WP	GND	CSI4_D1-
21	I2C_GP1_CLK	GPIO12_BT_EN	GND	CSI5_CLK-	CSI5_D1+	GND	CSI4_CLK-	CSI4_D1+
22	GPIO_EXP1_INT	GPIO13_BT_WAKE_AP	CSI5_D0-	CSI5_CLK+	GND	CSI4_D0-	CSI4_CLK+	GND
23	GPIO_EXP0_INT	GPIO7_TOUCH_RST	CSI5_D0+	GND	CSI3_D1-	CSI4_D0+	GND	CSI2_D1-
24	RSVD	TOUCH_CLK	GND	CSI3_CLK-	CSI3_D1+	GND	CSI2_CLK-	CSI2_D1+
25	LCD_TE	GPIO6_TOUCH_INT	CSI3_D0-	CSI3_CLK+	GND	CSI2_D0-	CSI2_CLK+	GND
26	RSVD	LCD_VDD_EN	CSI3_D0+	GND	CSI1_D1-	CSI2_D0+	GND	CSI0_D1-
27	RSVD	LCD0_BKLT_PWM	GND	CSI1_CLK-	CSI1_D1+	GND	CSI0_CLK-	CSI0_D1+
28	GND	LCD_BKLT_EN	CSI1_D0-	CSI1_CLK+	GND	CSI0_D0-	CSI0_CLK+	GND
29	SDIO_RST#	SDIO_CMD	CSI1_D0+	GND	DSI3_D1+	CSI0_D0+	GND	DSI2_D1+
30	SDIO_D3	SDIO_CLK	GND	RSVD	DSI3_D1-	GND	DSI2_CLK+	DSI2_D1-
31	SDIO_D2	GND	DSI3_D0+	RSVD	GND	DSI2_D0+	DSI2_CLK-	GND
32	SDIO_D1	SDIO_D0	DSI3_D0-	GND	DSI1_D1+	DSI2_D0-	GND	DSI0_D1+
33	DP1_HPD	HDMI_CEC	GND	RSVD	DSI1_D1-	GND	DSI0_CLK+	DSI0_D1-
34	DP1_AUX_CH-	DP0_AUX_CH-	DSI1_D0+	RSVD	GND	DSI0_D0+	DSI0_CLK-	GND
35	DP1_AUX_CH+	DP0_AUX_CH+	DSI1_D0-	GND	DP1_TX3-	DSI0_D0-	GND	DP0_TX3-
36	USB0_OTG_ID	DP0_HPD	GND	DP1_TX2-	DP1_TX3+	GND	DP0_TX2-	DP0_TX3+
37	GND	USB0_VBUS_DET	DP1_TX1-	DP1_TX2+	GND	DP0_TX1-	DP0_TX2+	GND
38	USB1_D+	GND	DP1_TX1+	GND	DP1_TX0-	DP0_TX1+	GND	DP0_TX0-
39	USB1_D-	USB0_D+	GND	PEX_RFU_TX+	DP1_TX0+	GND	PEX_RFU_RX+	DP0_TX0+
40	GND	USB0_D-	PEX2_TX+	PEX_RFU_TX-	GND	PEX2_RX+	PEX_RFU_RX-	GND
41	RSVD	GND	PEX2_TX-	GND	PEX1_TX+	PEX2_RX-	GND	PEX1_RX+
42	RSVD	USB2_D+	GND	USB_SS1_TX+	PEX1_TX-	GND	USB_SS1_RX+	PEX1_RX-
43	GND	USB2_D-	USB_SS0_TX+	USB_SS1_TX-	GND	USB_SS0_RX+	USB_SS1_RX-	GND
44	PEX0_REFCLK+	GND	USB_SS0_TX-	GND	PEX0_TX+	USB_SS0_RX-	GND	PEX0_RX+
45	PEX0_REFCLK-	PEX1_REFCLK+	GND	SATA_TX+	PEX0_TX-	GND	SATA_RX+	PEX0_RX-
46	RESET_OUT#	PEX1_REFCLK-	RSVD	SATA_TX-	GND	GBE_LINK1000#	SATA_RX-	GND
47	RESET_IN#	GND	PEX1_CLKREQ#	RSVD	GBE_LINK_ACT#	GBE_MDI1+	GND	GBE_MDI3+
48	CARRIER_PWR_ON	RSVD	PEX0_CLKREQ#	PEX_WAKE#	GBE_MDI0+	GBE_MDI1-	GBE_MDI2+	GBE_MDI3-
49	CHARGER_PRSNT#	RSVD	PEX0_RST#	RSVD	GBE_MDI0-	GND	GBE_MDI2-	GND
50	VDD_RTC	POWER_BTN#	RSVD	RSVD	PEX1_RST#	GBE_LINK100#	GND	RSVD

Legend

Ground	Power	Reserved on Jetson TX1	Unassigned on Carrier

Notes:
- RSVD (Reserved) pins on Jetson TX1 must be left unconnected.
- Signals starting with "GPIO_" are standard GPIOs that have been assigned recommended usages. If the assigned usage is required in a design it is recommended the matching GPIO be used. If the assigned usage is not required, the pins may be used as GPIOs for other purposes.

3.0 JETSON TX1 PIN DESCRIPTIONS

Table 5. Jetson TX1 Connector (8x50) Pin Descriptions

Pin #	Jetson TX1 Pin Name	Tegra X1 Signal	Usage/Description	Usage on Jetson TX1 Carrier Board	Direction	Pin Type
A1	VDD_IN	–	Main VDD Input	Main DC input	Input	5.5V-19.6V
A2	VDD_IN	–	Main VDD Input	Main DC input	Input	5.5V-19.6V
A3	GND	–	GND	GND	–	GND
A4	GND	–	GND	GND	–	GND
A5	RSVD	–	Not used	–	–	–
A6	I2C_PM_CLK	GEN3_I2C_SCL	PM I2C Bus Clock	ID EEPROM	Bidir	Open Drain – 1.8V
A7	CHARGING#	BUTTON_VOL_DOWN	Charger Interrupt	System	Input	CMOS – 1.8V
A8	GPIO14/AP_WAKE_MODEM	GPIO_PK5	AP (Tegra) Wake Modem	Modem	Output	CMOS – 1.8V
A9	GPIO15/AP2MDM_READY	AP_READY	AP (Tegra) to Modem Ready	Modem	Input	CMOS – 1.8V
A10	GPIO16/MODEM_WAKE_AP	MODEM_WAKE_AP	Modem Wake AP	Modem	Input	CMOS – 1.8V
A11	RSVD	–	Not used	–	–	–
A12	JTAG_TMS	JTAG_TMS	JTAG Test Mode Select	JTAG	Input	CMOS – 1.8V
A13	JTAG_TDO	JTAG_TDO	JTAG Test Data Out	JTAG	Output	CMOS – 1.8V
A14	JTAG_RTCLK	JTAG_RTCK	JTAG Return Clock	JTAG	Output	CMOS – 1.8V
A15	UART2_CTS#	UART2_CTS	UART 2 Clear to Send	BT	Input	CMOS – 1.8V
A16	UART2_RTS#	UART2_RTS	UART 2 Request to Send	BT	Output	CMOS – 1.8V
A17	USB0_EN_OC#	USB_VBUS_EN0	Micro USB VBUS Enable 0	USB 2.0 (Power)	Bidir	Open Drain – 3.3V
A18	USB1_EN_OC#	USB_VBUS_EN1	USB 3.0 Type A, USB Enable 1	USB 3.0 (Power)	Bidir	Open Drain – 3.3V
A19	RSVD	–	Not used	–	–	–
A20	I2C_GP1_DAT	GEN2_I2C_SDA	General I2C Bus #1 Data	I2C (General)	Bidir	Open Drain – 3.3V
A21	I2C_GP1_CLK	GEN2_I2C_SCL	General I2C Bus #1 Clock	I2C (General)	Bidir	Open Drain – 3.3V
A22	GPIO_EXP1_INT	GPIO_PZ2	GPIO Expander 1 Interrupt	GPIO Expander	Input	CMOS – 1.8V
A23	GPIO_EXP0_INT	GPIO_PL1	GPIO expander 0 Interrupt	GPIO Expander	Input	CMOS – 1.8V
A24	RSVD	–	Not used	–		–
A25	LCD_TE	LCD_TE	Display Tearing Effect	Display (Control)	Input	CMOS – 1.8V
A26	RSVD	–	Not used	–	–	–
A27	RSVD	–	Not used	–	–	–
A28	GND	–	GND	GND	–	GND
A29	SDIO_RST#	NFC_EN	SDIO Reset	SDIO	Output	CMOS – 1.8V
A30	SDIO_D3	SDMMC3_DAT3	SDIO Data 3	SDIO	Bidir	CMOS – 1.8V
A31	SDIO_D2	SDMMC3_DAT2	SDIO Data 2	SDIO	Bidir	CMOS – 1.8V
A32	SDIO_D1	SDMMC3_DAT1	SDIO Data 1	SDIO	Bidir	CMOS – 1.8V
A33	DP1_HPD	HDMI_INT_DP_HPD	Display Port 1 Hot Plug Detect	Display (DP/HDMI)	Input	CMOS – 1.8V
A34	DP1_AUX_CH-	DP_AUX_CH1_N	Display Port 1 Aux- or HDMI DDC SDA	Display (DP/HDMI)	Bidir	AC-Coupled on carrier board
A35	DP1_AUX_CH+	DP_AUX_CH1_P	Display Port 1 Aux+ or HDMI DDC SCL	Display (DP/HDMI)	Bidir	
A36	USB0_OTG_ID	–	USB0 ID / VBUS EN	USB 2.0	Input	Analog
A37	GND	–	GND	GND	–	GND
A38	USB1_D+	USB2_DP	USB 2.0, Port 1 Data+	USB 3.0 Type A	Bidir	USB PHY
A39	USB1_D-	USB2_DN	USB 2.0, Port 1 Data+	USB 3.0 Type A	Bidir	
A40	GND	–	GND	GND	–	GND
A41	RSVD	–	Not used	–	–	–
A42	RSVD	–	Not used	–	–	–
A43	GND	–	GND	GND	–	GND
A44	PEX0_REFCLK+	PEX_CLK1P	PCIe Reference Clock 0+	PCIe	Output	PCIe PHY
A45	PEX0_REFCLK-	PEX_CLK1N	PCIe Reference Clock 0-	PCIe	Output	
A46	RESET_OUT#	–	Reset from carrier board to Tegra & eMMC	System Control	Output	CMOS – 1.8V
A47	RESET_IN#	SYS_RESET_IN_N	System Reset output from Quill & input to initiate full PMIC reset	System Control	Input	Open Drain, 1.8V
A48	CARRIER_PWR_ON	–	Carrier Power On	System Control	Output	CMOS, 3.3V
A49	CHARGER_PRSNT#	–	PMIC AC OK	System	Input	Open Drain, 1.8V
A50	VDD_RTC	VDD_RTC	Tegra Real Time Clock block power	System Control	Bidir	Power In/Power Out
B1	VDD_IN	–	Main VDD Input	Main DC input	Input	5.5V-19.6V
B2	VDD_IN	–	Main VDD Input	Main DC input	Input	5.5V-19.6V
B3	GND	–	GND	GND	–	GND
B4	GND	–	GND	GND	–	GND
B5	RSVD	–	Not used	–	–	–

Pin #	Jetson TX1 Pin Name	Tegra X1 Signal	Usage/Description	Usage on Jetson TX1 Carrier Board	Direction	Pin Type
B6	I2C_PM_DAT	GEN3_I2C_SDA	PM I2C Bus Data	I2C	Bidir	Open Drain – 1.8V
B7	CARRIER_STBY#	SOC_PWR_REQ	SOC Power Request	System Control	Output	CMOS – 1.8V
B8	VIN_PWR_BAD#	–	Input Power Bad	System Control	Input	Open Drain – 5V
B9	GPIO17/MDM2AP_READY	GPIO_PK4	Modem to AP (Tegra) Ready	Modem	Input	CMOS – 1.8V
B10	GPIO18/MODEM_COLDBOOT	GPIO_PK6	Modem Cold Boot	Modem	Input	CMOS – 1.8V
B11	JTAG_TCLK	JTAG_TCK	JTAG Test Clock	JTAG	Input	CMOS – 1.8V
B12	JTAG_TDI	JTAG_TDI	JTAG Test Data In	JTAG	Input	CMOS – 1.8V
B13	JTAG_GP0	JTAG_TRST_N	JTAG Test Reset	JTAG	Input	CMOS – 1.8V
B14	GND	–	GND	GND	–	GND
B15	UART2_RX	UART2_RX	UART 2 Receive	BT	Input	CMOS – 1.8V
B16	UART2_TX	UART2_TX	UART 2 Transmit	BT	Output	CMOS – 1.8V
B17	FAN_TACH	GPIO_PK7	Fan Tach	Fan Control	Input	CMOS – 1.8V
B18	RSVD	–	Not used	–	–	–
B19	GPIO11/AP_WAKE_BT	AP_WAKE_NFC	LCD Enable	Display (Control)	Output	CMOS – 1.8V
B20	GPIO10/WIFI_WAKE_AP	NFC_INT	Wi-Fi 2 Wake AP (Tegra)	2nd Wi-Fi/BT	Input	CMOS – 1.8V
B21	GPIO12/BT_EN	GPS_EN	BT 2 Enable	BT	Output	CMOS – 1.8V
B22	GPIO13/BT_WAKE_AP	GPIO_PH6	BT 2 Wake AP (Tegra)	BT	Input	CMOS – 1.8V
B23	GPIO7/TOUCH_RST	TOUCH_RST	Touch Reset	Touch	Output	CMOS – 1.8V
B24	TOUCH_CLK	TOUCH_CLK	Touch Clock	Touch	Output	CMOS – 1.8V
B25	GPIO6/TOUCH_INT	TOUCH_INT	Touch Interrupt	Touch	Input	CMOS – 1.8V
B26	LCD_VDD_EN	LCD_RST	Display Reset	Display (Control)	Output	CMOS – 1.8V
B27	LCD0_BKLT_PWM	LCD_BL_PWM	Display Backlight PWM	Display (Backlight)	Output	CMOS – 1.8V
B28	LCD_BKLT_EN	LCD_BL_EN	Display Backlight Enable	Display (Backlight)	Output	CMOS – 1.8V
B29	SDIO_CMD	SDMMC3_CMD	SDIO Command	SDIO	Bidir	CMOS – 1.8V
B30	SDIO_CLK	SDMMC3_CLK	SDIO Clock	SDIO	Output	CMOS – 1.8V
B31	GND	–	GND	GND	–	GND
B32	SDIO_D0	SDMMC3_DAT0	SDIO Data 0	SDIO	Bidir	CMOS – 1.8V
B33	HDMI_CEC	HDMI_CEC	HDMI CEC	Display (DP/HDMI)	Bidir	Open Drain, 1.8V
B34	DP0_AUX_CH-	DP_AUX_CH0_N	Display Port 0 Auxiliary Channel-	Display (eDP/DP)	Bidir	AC-Coupled on carrier board
B35	DP0_AUX_CH+	DP_AUX_CH0_P	Display Port 0 Auxiliary Channel+	Display (eDP/DP)	Bidir	
B36	DP0_HPD	DP_HPD0	Display Port 0 Hot Plug Detect	Display (eDP/DP)	Input	CMOS – 1.8V
B37	USB0_VBUS_DET	GPIO_PZ0	USB0 VBUS	USB VBUS Supply en.	Input	USB VBUS, 5V
B38	GND	–	GND	GND	–	GND
B39	USB0_D+	USB0_DP	Micro USB Data+	USB 2.0 Micro AB	Bidir	USB PHY
B40	USB0_D-	USB0_DN	Micro USB Data-	USB 2.0 Micro AB	Bidir	
B41	GND	–	GND	GND	–	GND
B42	USB2_D+	USB3_DP	USB 2.0, Port 2 Data+	2nd Wi-Fi/BT, Modem	Bidir	USB PHY
B43	USB2_D-	USB3_DN	USB 2.0, Port 2 Data+	2nd Wi-Fi/BT, Modem	Bidir	
B44	GND	–	GND	GND	–	GND
B45	PEX1_REFCLK+	PEX_CLK2P	PCIe Reference Clock 1+	PCIe	Output	PCIe PHY
B46	PEX1_REFCLK-	PEX_CLK2N	PCIe Reference Clock 1-	PCIe	Output	
B47	GND	–	GND		–	GND
B48	RSVD	–	Not used	–	–	–
B49	RSVD	–	Not used	–	–	–
B50	POWER_BTN#	BUTTON_PWR_ON	Power on	System Control	Input	Open Drain, 1.8V
C1	VDD_IN	–	Main VDD Input	Main DC input	Input	5.5V-19.6V
C2	VDD_IN	–	Main VDD Input	Main VDD Input	Input	5.5V-19.6V
C3	GND	–	GND	GND	–	GND
C4	GND	–	GND	GND	–	GND
C5	RSVD	–	Not used	–	–	–
C6	I2C_CAM_CLK	CAM_I2C_SCL	Camera I2C Clock	Camera	Bidir	Open Drain – 1.8V
C7	BATLOW#	LCD_GPIO1	GPIO – Low Battery	System	Input	CMOS – 1.8V
C8	RSVD	–	Not used	–	–	–
C9	RSVD	–	Not used	–	–	–
C10	RSVD	–	Not used	–	–	–
C11	RSVD	–	Not used	–	–	–
C12	RSVD	–	Not used	–	–	–
C13	RSVD	–	Not used	–	–	–
C14	I2S1_SDIN	GPIO_PK1	I2S Audio Port 1 Data In	Audio	Input	CMOS – 1.8V
C15	I2S1_CLK	GPIO_PK3	I2S Audio Port 1 Clock	Audio	Bidir	CMOS – 1.8V
C16	FAN_PWM	GPIO_PE7	Fan PWM	Fan Control	Output	CMOS – 1.8V
C17	RSVD	–	Not used	–		–

Pin #	Jetson TX1 Pin Name	Tegra X1 Signal	Usage/Description	Usage on Jetson TX1 Carrier Board	Direction	Pin Type
C18	RSVD	–	Not used	–		–
C19	RSVD	–	Not used	–		–
C20	RSVD	–	Not used	–		–
C21	GND	–	GND	GND	–	GND
C22	CSI5_D0-	CSI_F_D0_N	Camera, CSI 5 Data 0-	Camera	Input	MIPI D-PHY
C23	CSI5_D0+	CSI_F_D0_P	Camera, CSI 5 Data 0+	Camera	Input	
C24	GND	–	GND	GND	–	GND
C25	CSI3_D0-	CSI_D_D0_N	Camera, CSI 3 Data 0-	Camera	Input	MIPI D-PHY
C26	CSI3_D0+	CSI_D_D0_P	Camera, CSI 3 Data 0+	Camera	Input	
C27	GND	–	GND	GND	–	GND
C28	CSI1_D0-	CSI_B_D0_N	Camera, CSI 1 Data 0-	Camera	Input	MIPI D-PHY
C29	CSI1_D0+	CSI_B_D0_P	Camera, CSI 1 Data 0+	Camera	Input	
C30	GND	–	GND	GND	–	GND
C31	DSI3_D0+	DSI_B_D2_P	Display, DSI 3 Data 2+	Display (DSI)	Output	MIPI D-PHY
C32	DSI3_D0-	DSI_B_D2_N	Display, DSI 3 Data 2-	Display (DSI)	Output	
C33	GND	–	GND	GND	–	GND
C34	DSI1_D0+	DSI_A_D2_P	Display, DSI 1 Data 2+	Display (DSI)	Output	MIPI D-PHY
C35	DSI1_D0-	DSI_A_D2_N	Display, DSI 1 Data 2-	Display (DSI)	Output	
C36	GND	–	GND	GND	–	GND
C37	DP1_TX1-	HDMI_DP_TXDN1	DisplayPort 1 Lane 1- / HDMI Lane 1-	Display (DP/HDMI)	Output	AC-Coupled on carrier board
C38	DP1_TX1+	HDMI_DP_TXDP1	DisplayPort 1 Lane 1+ / HDMI Lane 1+	Display (DP/HDMI)	Output	
C39	GND	–	GND	GND	–	GND
C40	PEX2_TX+	PEX_TX2P	PCIe Lane 2 Transmit+	PCIe	Output	PCIe PHY, AC-Coupled on carrier board
C41	PEX2_TX-	PEX_TX2N	PCIe Lane 2 Transmit -	PCIe	Output	
C42	GND	–	GND	GND	–	GND
C43	USB_SS0_TX+	PEX_TX5P	USB 3.0 #0 Transmit+ (PCIe Lane 5)	USB 3.0	Output	USB SS PHY, AC-Coupled on carrier board
C44	USB_SS0_TX-	PEX_TX5N	USB 3.0 #0 Transmit- (PCIe Lane 5)	USB 3.0	Output	
C45	GND	–	GND	GND	–	GND
C46	RSVD	–	Not used	–	–	–
C47	PEX1_CLKREQ#	PEX_L1_CLKREQ_N	PCIE 1 Clock Request	PCIe	Bidir	Open Drain 3.3V, Pull-up on Jetson TX1
C48	PEX0_CLKREQ#	PEX_L0_CLKREQ_N	PCIE 0 Clock Request	PCIe	Bidir	
C49	PEX0_RST#	PEX_L0_RST_N	PCIe Reset 0	PCIe	Output	
C50	RSVD	–	Not used	–	–	–
D1	RSVD	–	Not used	–	–	–
D2	RSVD	–	Not used	–	–	–
D3	RSVD	–	Not used	–	–	–
D4	RSVD	–	Not used	–	–	–
D5	RSVD	–	Not used	–	–	–
D6	I2C_CAM_DAT	CAM_I2C_SDA	Camera I2C Data	Camera	Bidir	Open Drain – 1.8V
D7	GPIO5/CAM_FLASH_EN	CAM_FLASH_EN	Camera Flash Enable	Cameras	Output	CMOS – 1.8V
D8	RSVD	–	Not used	–	–	–
D9	UART1_TX	UART3_TX	UART 1 Transmit	Serial Port	Output	CMOS – 1.8V
D10	UART1_RX	UART3_RX	UART 1 Receive	Serial Port	Input	CMOS – 1.8V
D11	RSVD	–	Not used	–		–
D12	RSVD	–	Not used	–		–
D13	I2S1_LRCLK	GPIO_PK0	I2S Audio Port 1 Field Select	Audio	Bidir	CMOS – 1.8V
D14	I2S1_SDOUT	GPIO_PK2	I2S Audio Port 1 Data Out	Audio	Bidir	CMOS – 1.8V
D15	I2C_GP0_DAT	GEN1_I2C_SDA	General I2C Bus #1 Data	I2C (General)	Bidir	Open Drain – 1.8V
D16	RSVD	–	Not used	–	–	–
D17	RSVD	–	Not used	–	–	–
D18	RSVD	–	Not used	–	–	–
D19	RSVD	–	Not used	–	–	–
D20	GND	–	GND	GND	–	GND
D21	CSI5_CLK-	CSI_F_CLK_N	Camera, CSI 5 Clock-	Camera	Input	MIPI D-PHY
D22	CSI5_CLK+	CSI_F_CLK_P	Camera, CSI 5 Clock+	Camera	Input	
D23	GND	–	GND	GND	–	GND
D24	CSI3_CLK-	CSI_D_CLK_N	Camera, CSI 3 Clock-	Camera	Input	MIPI D-PHY
D25	CSI3_CLK+	CSI_D_CLK_P	Camera, CSI 3 Clock+	Camera	Input	
D26	GND	–	GND	GND	–	GND
D27	CSI1_CLK-	CSI_B_CLK_N	Camera, CSI 1 Clock-	Camera	Input	MIPI D-PHY
D28	CSI1_CLK+	CSI_B_CLK_P	Camera, CSI 1 Clock+	Camera	Input	
D29	GND	–	GND	GND	–	GND

Pin #	Jetson TX1 Pin Name	Tegra X1 Signal	Usage/Description	Usage on Jetson TX1 Carrier Board	Direction	Pin Type
D30	RSVD	–	Not used	–	–	–
D31	RSVD	–	Not used	–	–	–
D32	GND	–	GND	GND	–	GND
D33	RSVD	–	Not used	–	–	–
D34	RSVD	–	Not used	–	–	–
D35	GND	–	GND	GND	–	GND
D36	DP1_TX2-	HDMI_DP_TXDN2	DisplayPort 1 Lane 2- / HDMI Lane 0-	Display (DP/HDMI)	Output	AC-Coupled on carrier board
D37	DP1_TX2+	HDMI_DP_TXDP2	DisplayPort 1 Lane 2+ / HDMI Lane 0+	Display (DP/HDMI)	Output	
D38	GND	–	GND	GND	–	GND
D39	PEX_RFU_TX+	PEX_TX1P	PCIe Lane RFU Transmit+	PCIe	Output	PCIe PHY, AC-Coupled on carrier board
D40	PEX_RFU_TX-	PEX_TX1N	PCIe Lane RFU Transmit-	PCIe	Output	
D41	GND	–	GND	GND	–	GND
D42	USB_SS1_TX+	PEX_TX3P	USB 3.0 #2 or PCIe #0_1 Transmit+	PCIe / USB 3.0	Output	USB SS PHY, AC-Coupled on carrier board
D43	USB_SS1_TX-	PEX_TX3N	USB 3.0 #2 or PCIe #0_1 Transmit-	PCIe / USB 3.0	Output	
D44	GND	–	GND	GND	–	GND
D45	SATA_TX+	SATA_L0_TXP	SATA or USB 3.0 #3 Transmit+	SATA	Output	SATA PHY, AC-Coupled on carrier board
D46	SATA_TX-	SATA_L0_TXN	SATA or USB 3.0 #3 Transmit-	SATA	Output	
D47	RSVD	–	Not used	–	–	–
D48	PEX_WAKE*	PEX_WAKE_N	PCIe Wake	PCIe	Input	Open Drain 3.3V, Pull-up on Jetson TX1
D49	RSVD	–	Not used	–	–	–
D50	RSVD	–	Not used	–	–	–
E1	FORCE_RECOV#	BUTTON_VOL_UP	Force Recovery strap pin	System Control	Input	CMOS – 1.8V
E2	SLEEP*	POWER_SLIDE_SW	Sleep input	Sleep (VOL DOWN) button	Input	Open Drain, 1.8V
E3	SPI0_CLK	SPI4_SCK	SPI 0 Clock	Not used	Bidir	CMOS – 1.8V
E4	SPI0_MISO	SPI4_MISO	SPI 0 MISO	Not used	Bidir	CMOS – 1.8V
E5	I2S3_SDIN	DAP4_DIN	I2S Audio Port 3 Data In	Audio	Input	CMOS – 1.8V
E6	I2S3_CLK	DAP4_SCLK	I2S Audio Port 3 Clock	Audio	Bidir	CMOS – 1.8V
E7	RSVD	–	Not used	–	–	–
E8	RSVD	–	Not used	–	–	–
E9	UART1_RTS#	UART3_TX	UART 1 Transmit	Serial Port	Output	CMOS – 1.8V
E10	UART1_CTS#	UART3_RX	UART 1 Receive	Serial Port	Input	CMOS – 1.8V
E11	RSVD	–	Not used	–	–	–
E12	RSVD	–	Not used	–	–	–
E13	SPI1_CS1#	SPI1_CS1	SPI 1 Chip Select 1	Audio Expansion	Bidir	CMOS – 1.8V
E14	SPI1_CS0#	SPI1_CS0	SPI 1 Chip Select 0	Audio (Control)	Bidir	CMOS – 1.8V
E15	I2C_GP0_CLK	GEN1_I2C_SCL	General I2C Bus #0 Clock	I2C (General)	Bidir	Open Drain – 1.8V
E16	RSVD	–	Not used	–	–	–
E17	RSVD	–	Not used	–	–	–
E18	RSVD	–	Not used	–	–	–
E19	GND	–	GND	GND	–	GND
E20	CSI5_D1-	CSI_F_D1_N	Camera, CSI 5 Data 1-	Camera	Input	MIPI D-PHY
E21	CSI5_D1+	CSI_F_D1_P	Camera, CSI 5 Data 1+	Camera	Input	
E22	GND	–	GND	GND	–	GND
E23	CSI3_D1-	CSI_D_D1_N	Camera, CSI 3 Data 1-	Camera	Input	MIPI D-PHY
E24	CSI3_D1+	CSI_D_D1_P	Camera, CSI 3 Data 1+	Camera	Input	
E25	GND	–	GND	GND	–	GND
E26	CSI1_D1-	CSI_B_D1_N	Camera, CSI 1 Data 1-	Camera	Input	MIPI D-PHY
E27	CSI1_D1+	CSI_B_D1_P	Camera, CSI 1 Data 1+	Camera	Input	
E28	GND	–	GND	GND	–	GND
E29	DSI3_D1+	DSI_B_D3_P	Display, DSI 3 Data 3+	Display (DSI)	Output	MIPI D-PHY
E30	DSI3_D1-	DSI_B_D3_N	Display, DSI 3 Data 3-	Display (DSI)	Output	
E31	GND	–	GND	GND	–	GND
E32	DSI1_D1+	DSI_A_D3_P	Display, DSI 1 Data 3+	Display (DSI)	Output	MIPI D-PHY
E33	DSI1_D1-	DSI_A_D3_N	Display, DSI 1 Data 3-	Display (DSI)	Output	
E34	GND	–	GND	GND	–	GND
E35	DP1_TX3-	HDMI_DP_TXDN3	DisplayPort 1 Lane 3- / HDMI Clk Lane-	Display (DP/HDMI)	Output	AC-Coupled on carrier board
E36	DP1_TX3+	HDMI_DP_TXDP3	DisplayPort 1 Lane 3+ / HDMI Clk Lane+	Display (DP/HDMI)	Output	
E37	GND	–	GND	GND	–	GND
E38	DP1_TX0-	HDMI_DP_TXDN0	DisplayPort 1 Lane 0- / HDMI Lane 2-	Display (DP/HDMI)	Output	AC-Coupled on carrier board
E39	DP1_TX0+	HDMI_DP_TXDP0	DisplayPort 1 Lane 0+ / HDMI Lane 2+	Display (DP/HDMI)	Output	
E40	GND	–	GND	GND	–	GND

Pin #	Jetson TX1 Pin Name	Tegra X1 Signal	Usage/Description	Usage on Jetson TX1 Carrier Board	Direction	Pin Type
E41	PEX1_TX+	PEX_TX0P	PCIe Lane 1 or USB 3.0 #2 Transmit+	PCIe	Output	PCIe PHY, AC-Coupled on carrier board
E42	PEX1_TX-	PEX_TX0N	PCIe Lane 1 or USB 3.0 #2 Transmit -	PCIe	Output	
E43	GND	–	GND	GND	–	GND
E44	PEX0_TX+	PEX_TX4P	PCIe Lane 0 Transmit+	PCIe	Output	PCIe PHY, AC-Coupled on carrier board
E45	PEX0_TX-	PEX_TX4N	PCIe Lane 0 Transmit-	PCIe	Output	
E46	GND	–	GND	GND	–	GND
E47	GBE_LINK_ACT#	–	GbE RJ45 connector Link ACT LED0	LAN	Output	CMOS – 3.3V tolerant
E48	GBE_MDI0+	–	GbE Transformer Data 0+	LAN	Bidir	MDI
E49	GBE_MDI0-	–	GbE Transformer Data 0-	LAN	Bidir	
E50	PEX1_RST#	PEX_L1_RST_N	PCIe 1 Reset	2nd Wi-Fi/BT, Modem	Output	Open Drain 3.3V, Pull-up on Jetson TX1
F1	AUDIO_MCLK	AUD_MCLK	Audio Codec Master Clock	Audio	Output	CMOS – 1.8V
F2	GPIO19/AUD_RST	GPIO_X1_AUD	Audio Codec Reset	Audio	Output	CMOS – 1.8V
F3	SPI0_CS0#	SPI4_CS0	SPI 0 Chip Select 0	Not used	Bidir	CMOS – 1.8V
F4	SPI0_MOSI	SPI4_MOSI	SPI 0 MOSI	Not used	Bidir	CMOS – 1.8V
F5	I2S3_LRCLK	DAP4_FS	I2S Audio Port 3 Field Select	Audio	Bidir	CMOS – 1.8V
F6	I2S3_SDOUT	DAP4_DOUT	I2S Audio Port 3 Data Out	Audio	Bidir	CMOS – 1.8V
F7	GPIO1/CAM1_PWR#	CAM1_PWDN	Camera 1 Power Down	Camera	Output	CMOS – 1.8V
F8	CAM1_MCLK	CAM1_MCLK	Camera 1 Reference Clock	Camera	Output	CMOS – 1.8V
F9	CAM0_MCLK	CAM0_MCLK	Camera 0 Reference Clock	Camera	Output	CMOS – 1.8V
F10	GND	–	GND	GND	–	GND
F11	RSVD	–	Not used	–	–	–
F12	RSVD	–	Not used	–	–	–
F13	SPI1_MOSI	SPI1_MOSI	SPI 1 MOSI	Audio (Control)	Bidir	CMOS – 1.8V
F14	SPI1_MISO	SPI1_MISO	SPI 1 MISO	Audio (Control)	Bidir	CMOS – 1.8V
F15	GND	–	GND	GND	–	GND
F16	SPI2_CS1#	SPI2_CS1	SPI 2 Chip Select 1	Display/Touch	Bidir	CMOS – 1.8V
F17	SDCARD_CD#	GPIO_PZ1	SD Card Card Detect	SD Card	Input	CMOS – 1.8V
F18	SDCARD_D3	SDMMC1_DAT3	SD Card Data 3	SD Card	Bidir	CMOS – 3.3/1.8V
F19	SDCARD_D2	SDMMC1_DAT2	SD Card Data 2	SD Card	Bidir	CMOS – 3.3/1.8V
F20	SDCARD_WP	GPIO_PZ4	SD Card Write Protect	SD Card	Input	CMOS – 1.8V
F21	GND	–	GND	GND	–	GND
F22	CSI4_D0-	CSI_E_D0_N	Camera, CSI 4 Clock-	Camera	Input	MIPI D-PHY
F23	CSI4_D0+	CSI_E_D0_P	Camera, CSI 4 Clock+	Camera	Input	
F24	GND	–	GND	GND	–	GND
F25	CSI2_D0-	CSI_C_D0_N	Camera, CSI 2 Data 0-	Camera	Input	MIPI D-PHY
F26	CSI2_D0+	CSI_C_D0_P	Camera, CSI 2 Data 0+	Cameras	Input	
F27	GND	–	GND	GND	–	GND
F28	CSI0_D0-	CSI_A_D0_N	Camera, CSI 0 Data 0-	Camera	Input	MIPI D-PHY
F29	CSI0_D0+	CSI_A_D0_P	Camera, CSI 0 Data 0+	Camera	Input	
F30	GND	–	GND	GND	–	GND
F31	DSI2_D0+	DSI_B_D0_P	Display, DSI 2 Data 0+	Display (DSI)	Output	MIPI D-PHY
F32	DSI2_D0-	DSI_B_D0_N	Display, DSI 2 Data 0-	Display (DSI)	Output	
F33	GND	–	GND	GND	–	GND
F34	DSI0_D0+	DSI_A_D0_P	Display, DSI 0 Data 0+	Display (DSI)	Output	MIPI D-PHY
F35	DSI0_D0-	DSI_A_D0_N	Display, DSI 0 Data 0-	Display (DSI)	Output	
F36	GND	–	GND	GND	–	GND
F37	DP0_TX1-	EDP_TXD1_N	Display Port 0 Data Lane 1-	Display (eDP/DP)	Output	AC-Coupled on carrier board
F38	DP0_TX1+	EDP_TXD1_P	Display Port 0 Data Lane 1+	Display (eDP/DP)	Output	
F39	GND	–	GND	GND	–	GND
F40	PEX2_RX+	PEX_RX2P	PCIe Lane 2 Receive+	PCIe	Input	PCIe PHY, AC-Coupled on carrier board
F41	PEX2_RX-	PEX_RX2N	PCIe Lane 2 Receive-	PCIe	Input	
F42	GND	–	GND	GND	–	GND
F43	USB_SS0_RX+	PEX_RX5P	USB 3.0 #0 Receive + (PCIe Lane 5)	USB 3.0	Input	USB SS PHY, AC-Coupled (off Jetson TX1)
F44	USB_SS0_RX-	PEX_RX5N	USB 3.0 #0 Receive - (PCIe Lane 5)	USB 3.0	Input	
F45	GND	–	GND	GND	–	GND
F46	GBE_LINK1000#	–	GbE RJ45 connector Link 1000 LED2	LAN	Output	CMOS – 3.3V Tolerant
F47	GBE_MDI1+	–	GbE Transformer Data 1+	LAN	Bidir	MDI
F48	GBE_MDI1-	–	GbE Transformer Data 1-	LAN	Bidir	
F49	GND	–	GND	GND	–	GND
F50	GBE_LINK100#	–	GbE RJ45 connector Link 100 LED1	LAN	Output	CMOS – 3.3V Tolerant
G1	I2S0_SDIN	DAP1_DIN	Digital Audio Port 1 Data In	Audio	Input	CMOS – 1.8V

Pin #	Jetson TX1 Pin Name	Tegra X1 Signal	Usage/Description	Usage on Jetson TX1 Carrier Board	Direction	Pin Type
G2	I2S0_CLK	DAP1_SCLK	Digital Audio Port 1 Clock	Audio	Bidir	CMOS – 1.8V
G3	GND	–	GND	GND	–	GND
G4	RSVD	–	Not used	–	–	–
G5	I2S2_CLK	DMIC2_DAT	Digital Audio Port 3 Clock	Audio	Bidir	CMOS – 1.8V
G6	I2S2_SDIN	DMIC1_DAT	Digital Audio Port 3 Data In	Audio	Input	CMOS – 1.8V
G7	GPIO4/CAM_STROBE	CAM1_STROBE	Camera 1 Strobe	Camera	Output	CMOS – 1.8V
G8	GPIO0/CAM0_PWR#	CAM1_PWDN	Camera 1 Power Down	Camera	Output	CMOS – 1.8V
G9	UART3_CTS#	–	Not used	–	–	–
G10	UART3_RTS#	–	Not used	–	–	–
G11	UART0_RTS#	UART1_RTS_N	UART 1 Return to Send	Debug	–	CMOS – 1.8V
G12	UART0_RX	UART1_RX	UART 1 Receive	Debug	Input	CMOS – 1.8V
G13	SPI1_CLK	SPI1_SCK	SPI 1 Clock	Audio (Control)	Bidir	CMOS – 1.8V
G14	GPIO9/MOTION_INT	MOTION_INT	ICM20628 Gyro/Accel	Sensors	Input	CMOS – 1.8V
G15	SPI2_MOSI	SPI2_MOSI	SPI 2 MOSI	Display/Touch	Bidir	CMOS – 1.8V
G16	SPI2_CS0#	SPI2_CS0	SPI 2 Chip Select 0	Display/Touch	Bidir	CMOS – 1.8V
G17	GND	–	GND	GND	–	GND
G18	SDCARD_CLK	SDMMC1_CLK	SD Card Clock	SD Card	Output	CMOS – 3.3/1.8V
G19	SDCARD_CMD	SDMMC1_CMD	SD Card Command	SD Card	Bidir	CMOS – 3.3/1.8V
G20	GND	–	GND	GND	–	GND
G21	CSI4_CLK-	CSI_E_CLK_N	Camera, CSI 4 Clock-	Cameras	Input	MIPI D-PHY
G22	CSI4_CLK+	CSI_E_CLK_P	Camera CSI 4 Clock+	Camera	Input	
G23	GND	–	GND	GND	–	GND
G24	CSI2_CLK-	CSI_C_CLK_N	Camera, CSI 2 Clock-	Camera	Input	MIPI D-PHY
G25	CSI2_CLK+	CSI_C_CLK_P	Camera, CSI 2 Clock+	Camera	Input	
G26	GND	–	GND	GND	–	GND
G27	CSI0_CLK-	CSI_A_CLK_N	Camera, CSI 0 Clock-	Cameras	Input	MIPI D-PHY
G28	CSI0_CLK+	CSI_A_CLK_P	Camera, CSI 0 Clock+	Camera	Input	
G29	GND	–	GND	GND	–	GND
G30	DSI2_CLK+	DSI_B_CLK_P	Display DSI 2 Clock+	Display (DSI)	Output	MIPI D-PHY
G31	DSI2_CLK-	DSI_B_CLK_N	Display DSI 2 Clock-	Display (DSI)	Output	
G32	GND	–	GND	GND	–	GND
G33	DSI0_CLK+	DSI_A_CLK_P	Display, DSI 0 Clock+	Display (DSI)	Output	MIPI D-PHY
G34	DSI0_CLK-	DSI_A_CLK_N	Display, DSI 0 Clock-	Display (DSI)	Output	
G35	GND	–	GND	GND	–	GND
G36	DP0_TX2-	EDP_TXD2_N	Display Port 0 Data Lane 2-	Display (eDP/DP)	Output	AC-Coupled on carrier board
G37	DP0_TX2+	EDP_TXD2_P	Display Port 0 Data Lane 2+	Display (eDP/DP)	Output	
G38	GND	–	GND	GND	–	GND
G39	PEX_RFU_RX+	PEX_RX1P	PCIe Lane RFU Receive+	PCIe	Input	PCIe PHY, AC-Coupled on carrier board
G40	PEX_RFU_RX-	PEX_RX1N	PCIe Lane RFU Receive+	PCIe	Input	
G41	GND	–	GND	GND	–	GND
G42	USB_SS1_RX+	PEX_RX3P	USB 3.0 #1 or PCIe Lane 3 Receive+	PCIe / USB 3.0	Input	USB SS PHY, AC-Coupled (off Jetson TX1)
G43	USB_SS1_RX-	PEX_RX3N	USB 3.0 #1 or PCIe Lane 3 Receive-	PCIe / USB 3.0	Input	
G44	GND	–	GND	GND	–	GND
G45	SATA_RX+	SATA_L0_RXP	SATA or USB 3.0 #3 Receive+	SATA	Input	SATA PHY, AC-Coupled on carrier board
G46	SATA_RX-	SATA_L0_RXN	SATA or USB 3.0 #3 Receive-	SATA	Input	
G47	GND	–	GND	GND	–	GND
G48	GBE_MDI2+	–	GbE Transformer Data 2+	LAN	Bidir	MDI
G49	GBE_MDI2-	–	GbE Transformer Data 2-	LAN	Bidir	
G50	GND	–	GND	GND	–	GND
H1	I2S0_LRCLK	DAP1_FS	I2S Audio Port 0 Field Select	Audio	Bidir	CMOS – 1.8V
H2	I2S0_SDOUT	DAP1_DOUT	I2S Audio Port 0 Data Out	Audio	Bidir	CMOS – 1.8V
H3	GPIO20/AUD_INT	GPIO_PE6	Audio Codec Interrupt	Audio	Input	CMOS – 1.8V
H4	RSVD	–	Not used	–	–	–
H5	I2S2_LRCLK	DMIC1_CLK	I2S Audio Port 2 Field Select	Audio	Bidir	CMOS – 1.8V
H6	I2S2_SDOUT	DMIC2_CLK	I2S Audio Port 2 Data Out	Audio	Bidir	CMOS – 1.8V
H7	GPIO3/CAM1_RST#	CAM_AF_EN	Camera Autofocus Enable	Camera	Output	CMOS – 1.8V
H8	GPIO2/CAM0_RST#	CAM_RST	Camera Reset	Camera	Output	CMOS – 1.8V
H9	UART3_RX	–	Not used	–	–	–
H10	UART3_TX	–	Not used	–	–	–
H11	UART0_CTS#	UART1_CTS	UART 0 Clear to Send	Debug	Input	CMOS – 1.8V
H12	UART0_TX	UART1_TX	UART 0 Transmit	Debug	Output	CMOS – 1.8V
H13	GPIO8/ALS_PROX_INT	ALS_PROX_INT	Proximity sensor Interrupt	Sensor	Input	CMOS – 1.8V

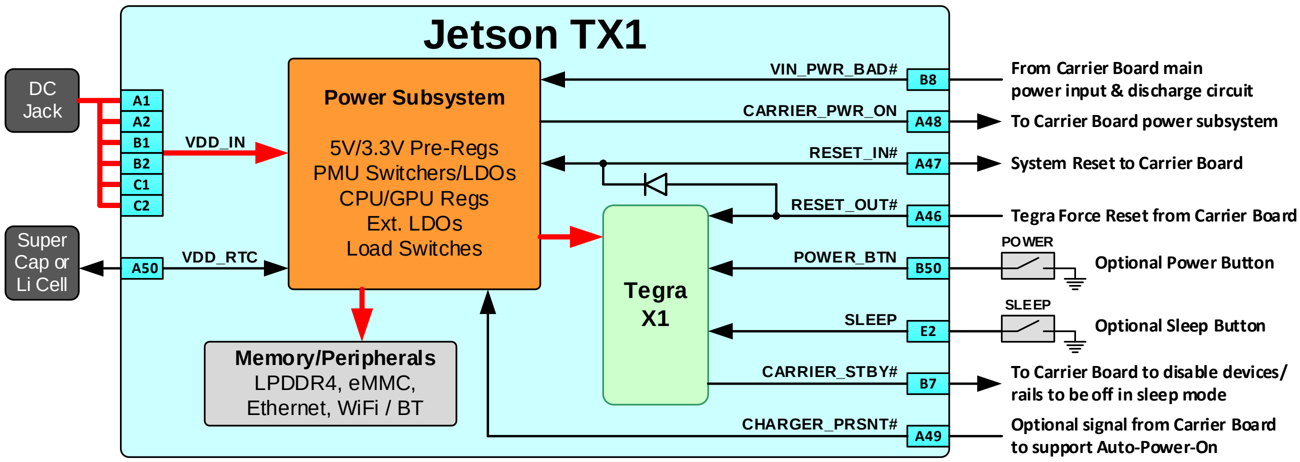
Pin #	Jetson TX1 Pin Name	Tegra X1 Signal	Usage/Description	Usage on Jetson TX1 Carrier Board	Direction	Pin Type
H14	SPI2_CLK	SPI2_SCK	SPI 2 Clock	Display/Touch	Bidir	CMOS – 1.8V
H15	SPI2_MISO	SPI2_MISO	SPI 2 MISO	Display/Touch	Bidir	CMOS – 1.8V
H16	SDCARD_PWR_EN	GPIO_PZ3	SD Card power switch Enable	SD Card	Output	CMOS – 1.8V
H17	SDCARD_D1	SDMMC1_DAT1	SD Card Data 1	SD Card	Bidir	CMOS – 3.3V/1.8V
H18	SDCARD_D0	SDMMC1_DAT0	SD Card Data 0	SD Card	Bidir	CMOS – 3.3V/1.8V
H19	GND	–	GND	GND	–	GND
H20	CSI4_D1-	CSI_E_D1_N	Camera, CSI 4 Data 1-	Camera	Input	MIPI D-PHY
H21	CSI4_D1+	CSI_E_D1_P	Camera, CSI 4 Data 1+	Camera	Input	
H22	GND	–	GND	GND	–	GND
H23	CSI2_D1-	CSI_C_D1_N	Camera, CSI 2 Data 1-	Camera	Input	MIPI D-PHY
H24	CSI2_D1+	CSI_C_D1_P	Camera, CSI 2 Data 1+	Cameras	Input	
H25	GND	–	GND	GND	–	GND
H26	CSI0_D1-	CSI_A_D1_N	Camera, CSI 0 Data 1-	Camera	Input	MIPI D-PHY
H27	CSI0_D1+	CSI_A_D1_P	Camera, CSI 0 Data 1+	Camera	Input	
H28	GND	–	GND	GND	–	GND
H29	DSI2_D1+	DSI_B_D1_P	Display, DSI 2 Data 1+	Display (DSI)	Output	MIPI D-PHY
H30	DSI2_D1-	DSI_B_D1_N	Display, DSI 2 Data 1-	Display (DSI)	Output	
H31	GND	–	GND	GND	–	GND
H32	DSI0_D1+	DSI_A_D1_P	Display, DSI 0 Data 1+	Display (DSI)	Output	MIPI D-PHY
H33	DSI0_D1-	DSI_A_D1_N	Display, DSI 0 Data 1-	Display (DSI)	Output	
H34	GND	–	GND	GND	–	GND
H35	DP0_TX3-	EDP_TXD3_N	Display Port 0 Data Lane 3-	Display (eDP/DP)	Output	AC-Coupled on carrier board
H36	DP0_TX3+	EDP_TXD3_P	Display Port 0 Data Lane 3+	Display (eDP/DP)	Output	
H37	GND	–	GND	GND	–	GND
H38	DP0_TX0-	EDP_TXD0_N	Display Port 0 Data Lane 0-	Display (eDP/DP)	Output	AC-Coupled on carrier board
H39	DP0_TX0+	EDP_TXD0_P	Display Port 0 Data Lane 0+	Display (eDP/DP)	Output	
H40	GND	–	GND	GND	–	GND
H41	PEX1_RX+	PEX_RX0P	PCIe Lane 1 or USB 3.0 #2 Receive+	PCIe	Input	PCIe PHY, AC-Coupled on carrier board
H42	PEX1_RX-	PEX_RX0N	PCIe Lane 1 or USB 3.0 #2 Receive-	PCIe	Input	
H43	GND	–	GND	GND	–	GND
H44	PEX0_RX+	PEX_RX4P	PCIe Lane 0 Receive+	PCIe	Input	PCIe PHY, AC-Coupled on carrier board
H45	PEX0_RX-	PEX_RX4N	PCIe Lane 0 Receive+	PCIe	Input	
H46	GND	–	GND	GND	–	GND
H47	GBE_MDI3+	–	GbE Transformer Data 3+	LAN	Bidir	MDI
H48	GBE_MDI3-	–	GbE Transformer Data 3-	LAN	Bidir	
H49	GND	–	GND	GND	–	GND
H50	RSVD	–	Not used	–	–	–

Notes:
- The Usage/Description column uses the Jetson TX1 port/lane/interface references.
- In the Type/Dir column, Output is from Jetson TX1. Input is to Jetson TX1. Bidir is for Bidirectional signals.
- See Section 12.0 for details on the CMOS & Open-drain Pad Types

4.0 POWER

Caution *Jetson TX1 is not hot-pluggable. Before installing or removing the module, the main power supply (to VDD_IN pins) must be disconnected and adequate time (recommended > 1 minute) allowed for the various power rails to fully discharge.*

Figure 2. Power Block Diagram



4.1 Jetson TX1 Power & Control

Table 6 Jetson TX1 Power & Power Control (Visible at Jetson TX1 Pins)

Power Rails	Usage	(V)	Power Supply	Source
VDD_IN (VDD_MUX)	Main power – Supplies PMU & external supplies	5.5-19.6	External	Carrier board Supply
VDD_RTC	Back-up Real-Time-Clock rail (connects to Lithium Cell or super capacitor on carrier board)	1.65-5.5	PMIC is supply when charging cap or coin cell	Super cap or coin cell is source when system is disconnected from power
Control			**Direction**	**Pin Type**
VIN_PWR_BAD#	Carrier board indication to Jetson TX1 that the VDD_VIN power is good. Carrier board should assert this high only when VIN has reached its required voltage level and is stable. This prevents Jetson TX1 from powering up until the VIN power is stable.		Input	**CMOS VDD_IN**
CARRIER_PWR_ON	Used as part of the power up sequence. Jetson TX1 asserts this signal when it is safe for the carrier board to power up.		Output	**CMOS, 3.3V**
RESET_IN#	General purpose reset output from Jetson TX1 to the carrier board. Also can be driven from carrier board to initiate a full system reset including the PMIC.		Bidirectional	**Open Drain, 1.8V**
RESET_OUT#	Optional forced reset to Jetson TX1 from the carrier board to enter Boundary Scan test mode.		Input	**CMOS, 1.8V**
POWER_BTN#	Power button input to Jetson TX1 from the carrier board. This signal is pulled up on Jetson TX1.		Input	**Open Drain, 1.8V**
SLEEP#	Sleep Request to Jetson TX1 from carrier board. A pull-up is present on Jetson TX1.		Input	**Open Drain, 1.8V**
CARRIER_STBY#	Jetson TX1 drives this signal low when it is in the standby power state.		Output	**CMOS, 1.8V**
CHARGER_PRSNT#	Can optionally be used to support auto-power-on where the Jetson TX1 platform will power-on when the main power source is connected instead of waiting for a power button press.		Input	**Open Drain, 1.8V**

Note: When operated near the minimum voltage, the power supported by some of the supplies may be reduced.

4.2 Supply Allocation

Table 7 Jetson TX1 Internal Power Subsystem Allocation

Power Rails	Usage	(V)	Power Supply	Source
VDD_5V0_SYS	Supplies various switchers & load switches that in turn power the various circuits & peripherals on Jetson TX1.	5.0	5V DC-DC	**VDD_IN**
VDD_3V3_SYS	Supplies various LDOs & load switches that in turn power the various circuits & peripherals on Jetson TX1.	3.3	3.3V DC-DC	**VDD_IN**
VDD_CPU	Tegra CPU	1.0 (Var)	OpenVREG	**VDD_5V0_SYS**
VDD_GPU	Tegra GPU	1.0 (Var)	OpenVREG	**VDD_5V0_SYS**
VDD_SOC (CORE)	Tegra SOC	1.1 (Var)	PMU Switcher 0	**VDD_5V0_SYS**
VDD_DDR_1V1	LPDDR4	1.1	PMU Switcher 1	**VDD_5V0_SYS**
VDD_PRE_REG_1V35	Source for some PMU LDO inputs	1.35	PMU Switcher 2	**VDD_5V0_SYS**
VDD_1V8	Tegra, eMMC, Wi-Fi	1.8	PMU Switcher 3	**VDD_5V0_SYS**
AVDD_DSI_CSI_1V2	Tegra CSI & DSI	1.2	PMU LDO 0	**VDD_PRE_REG_1V35**
VDDIO_SDMMC_AP	Tegra SDMMC	1.8/2.8	PMU LDO 2	**VDD_3V3_SYS**
VDD_RTC (See note)	Tegra Real Time Clock/Always-on Rail	0.9 (Var)	PMU LDO 4	**VDD_5V0_SYS**
AVDD_1V05_PLL	Tegra PLLs	1.05	PMU LDO 7	**VDD_PRE_REG_1V35**
AVDD_SATA_HDMI_DP_1V05	Tegra SATA & HDMI	1.05	PMU LDO 8	**VDD_PRE_REG_1V35**
VDD_PEX_1V05	Tegra PEX / USB 3.0	1.05	LDO	**VDD_1V8**
VDD_1V8_PLL_UTMIP	Tegra USB PLL	1.8	Load Switch	**VDD_1V8**
AVDD_IO_EDP_1V05	Tegra EDP	1.05	Load Switch	**AVDD_1V05_PLL**
VDD_3V3_SLP	3.3V peripheral rail – Off in Deep Sleep	3.3	Load Switch	**VDD_3V3_SYS**
VDD_1V8_COM	Wi-Fi/BT	1.8	Load Switch	**VDD_1V8**

Note: This is the Tegra X1 supply, and should not be confused with the Jetson TX1 VDD_RTC pin which is the supply that connects to the PMIC BBATT pin to keep the Real-Time Clock powered.

4.3 Power Sequencing

In order to ensure reliable and consistent power up sequencing, VIN_PWR_BAD#, CARRIER_PWR_ON, and RESET_OUT# are implemented on the Jetson TX1 connector. The VIN_PWR_BAD# signal is generated by the carrier board and passed to Jetson TX1 to keep it powered off until the VDD_IN supply is stable and it is possible to power up any standby circuits on the Jetson TX1. This signal prevents the Jetson TX1 from powering up prematurely before the carrier board has charged up its decoupling capacitors and power to the Jetson TX1 is stable.

As can be seen in the power up sequence below, the Jetson TX1 is powered before the main carrier board circuits. The CARRIER_PWR_ON signal is generated by Jetson TX1 and passed to the carrier board to indicate that the Jetson TX1 is powered up and that the power up sequence for the carrier board circuits can begin.

After a period sufficient to allow the carrier board circuits to power up, the RESET_OUT# is de-asserted.

Figure 3. Power Up Sequence

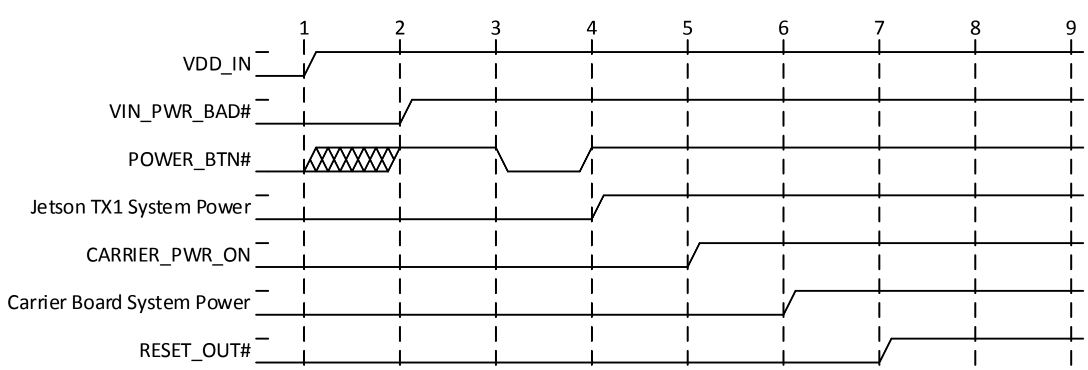
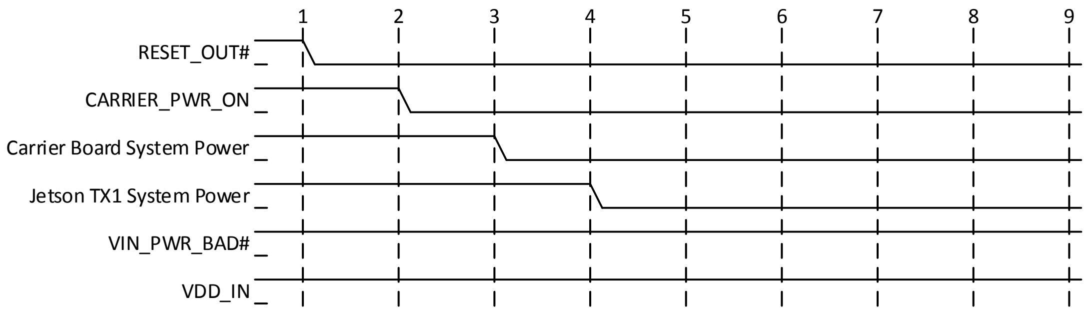


Figure 4. Power Down Sequence



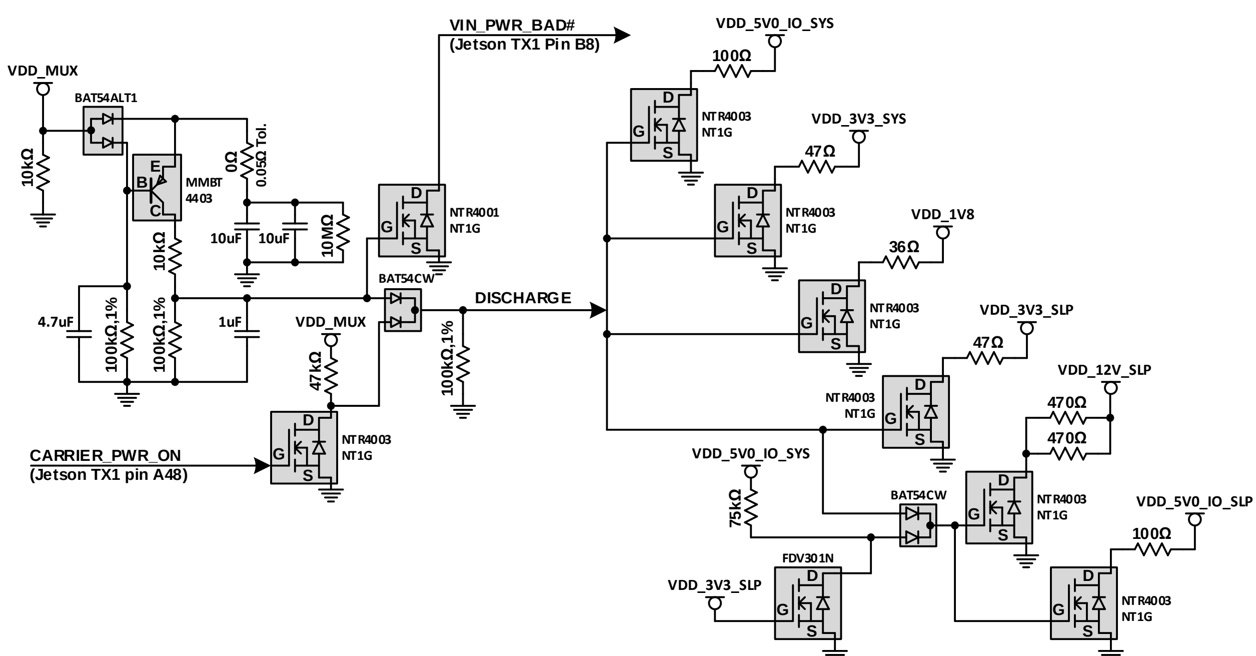
Note: During run time if any I/O rail is switched OFF or ON, the following sequences should be performed. Violating these sequences will result in extra in-rush current during the rail transition.

- OFF Sequence
  - NO_IOPOWER is enable by configuring appropriate bit in the PMC register APBDEV_PMC_NO_IOPOWER_0
  - Rail powered OFF
- ON Sequence
  - Rail powered ON
  - NO_IOPOWER is disable by configuring appropriate bit in the PMC register APBDEV_PMC_NO_IOPOWER_0

4.4 Power Discharge

In order to meet the Power Down requirements, discharge circuitry is required. In the figure below the DISCHARGE signal is generated, based on a transition of the CARRIER_POWER_ON signal or the removal of the main supply (VDD_MUX/VDD_IN). When DISCHARGE is asserted, VDD_5V0_IO_SYS, VDD_3V3_SYS, VDD_1V8 and VDD_3V3_SLP are forced to GND in a controlled manner. Removal of the VDD_MUX supply also causes VIN_PWR_BAD# to go active which controls the main 5V supply on Jetson TX1.

Figure 5. Power Discharge

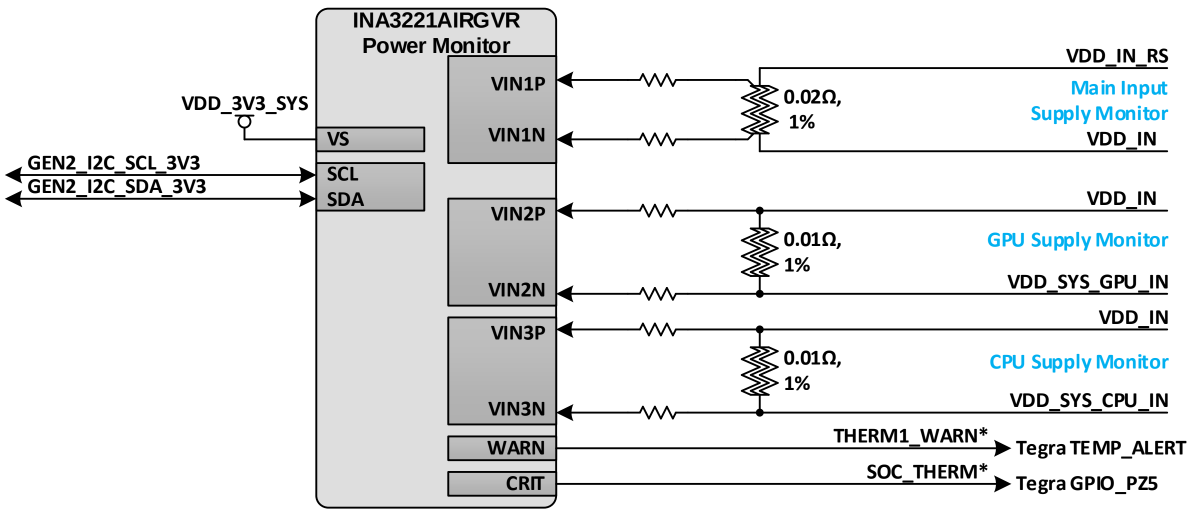


4.5 Power & Voltage Monitoring

4.5.1 Power Monitor

A Power monitor is provided on the Jetson TX1. This device monitors the main DC, GPU & CPU supplies. The monitor will toggle a WARN (warning) output, or a CRIT (critical) output, depending on the power "seen" at the sense resistors and the thresholds set for each supply.

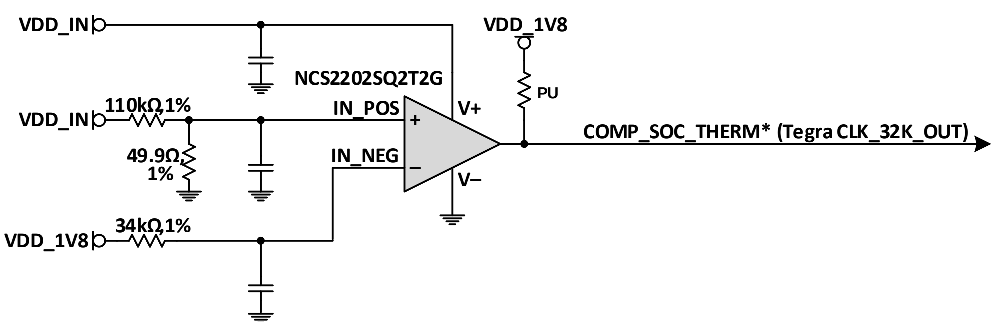
Figure 6. Main DC, GPU & CPU Supply Power Monitor



4.5.2 Voltage Monitor

A voltage monitor circuit is implemented on the Jetson TX1 to indicate if the main DC input rail, VDD_IN, "droops" below an acceptable level. The device used will react quickly and generate an alert to one of the Tegra SOC_THERM capable pins (CLK_32K_OUT). The voltage monitor circuit is implemented with a fast voltage comparator supplied by VDD_IN with a 1.8V (VDD_1V8) reference common with the Tegra IO domain that receives the output signal. This device has an open drain active low output which is pulled low when the VDD_IN voltage drops below the selected threshold.

Figure 7. Voltage Monitor Connections



Note: The threshold for VDD_IN, determined by the voltage divider components used in the circuit above is 5.78V.

4.6 Deep Sleep Wake Considerations

Certain events are required to generate a wake condition. This can vary depending on Operation System. Check platform design guide and reference schematics for specific connections by platform type.

Table 8. Jetson TX1 Signal Wake Events

Potential Wake Event	Jetson TX1 Pin Assigned	Wake #
Audio interrupt	**GPIO20_AUD_INT**	4
External BT wake request to AP	**GPIO13_BT_WAKE_AP**	10
External Wi-Fi wake request to AP	**GPIO10_WIFI_WAKE_AP**	11
Modem to AP ready	**GPIO17_MDM2AP_READY**	14
Modem cold boot alert	**GPIO18_MDM_COLDBOOT**	15
HDMI CEC	**HDMI_CEC**	19
GPIO expander 0 Interrupt	**GPIO_EXP0_INT**	21
Power ON button	**POWER_BTN#**	24
Charging interrupt	**CHARGING#**	26
Sleep request from carrier board	**SLEEP#**	27
Ambient/proximity interrupt	**GPIO8_ALS_PROX_INT**	32
HDMI Hot Plug Detect	**DP1_HPD**	53
Battery low warning	**BATLOW#**	57
Primary modem wake request to AP	**GPIO16_MDM_WAKE_AP**	61
Touch controller interrupt	**GPIO6_TOUCH_INT**	62
Motion sensor interrupt	**GPIO9_MOTION_INT**	63

4.7 Optional Auto-Power-On Support

This section provides guidance for modifying a carrier board design to power the platform on when VDD_IN is first powered, instead of waiting for a power button press. In order to power the system on without a power button, a specific sequence is required between the time the VDD_IN power (5.5V-19.6V) is connected and the CHARGER_PRSNT# pin on Jetson TX1 is driven high. The CHARGER_PRSNT# pin connects to the Jetson TX1 PMIC and requires a minimum delay of 300ms from the point VDD_IN reaches its minimum level (5.5V) before it can be driven low. Three options to meet this requirement and allow Auto-Power-On are described:

- Microcontroller: Recommended if a microcontroller is already being used to control power-on.
- Supervisor IC: Using a supervisor IC and related discrete devices to meet the sequencing requirements.
- Discrete Circuit: Circuit using only discrete devices to meet the sequencing requirements

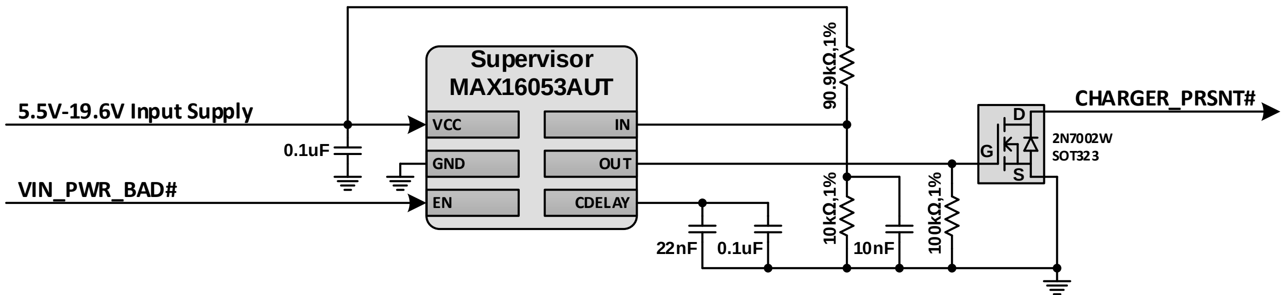
Microcontroller

If a microcontroller is already present on the carrier board and is used to power the system on when the main power source is connected, then it can be used to support Auto-Power-On with the following conditions:

- After the microcontroller is out of reset wait 300ms before pulsing CHARGER_PRSNT# or POWER_BTN# low
- If the POWER_BTN# pin is used, it should be held low for a time period between 40ms & 5sec.
- If the CHARGER_PRSNT# pin is used, it should be held low for >200us

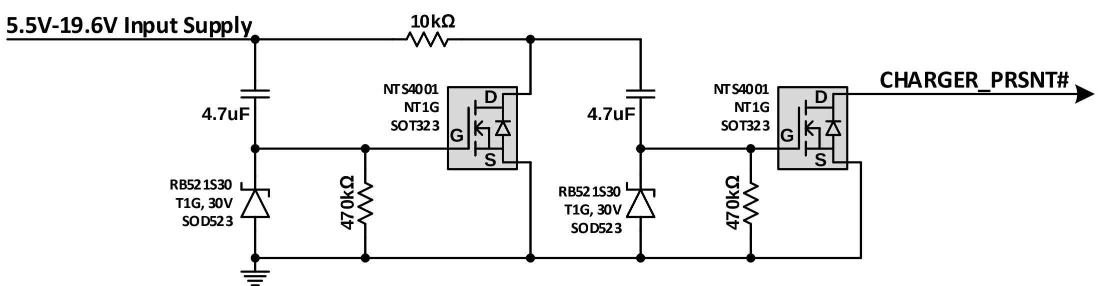
Supervisor IC

The figure below shows a circuit that includes a supervisor IC. This circuit meets the sequence requirement to keep CHARGER_PRSNT# low until VDD_IN is on plus the delay mentioned above (>300ms). The circuit works across the full range of VDD_IN (5.5V to 19.6V).



Discrete Circuit

The figure below shows a circuit using only discrete components. This circuit also meets the sequence requirement to keep CHARGER_PRSNT# low until VDD_IN is on plus the delay mentioned above (>300ms). The circuit assumes the VDD_IN ramp time from 0V-5.5V is > 7 V/S. In order to meet the full supported range for VDD_IN (5.5V to 19.6V), the turn-on delay can be as long as 4sec. For a narrower VDD_IN range, the delay can be optimized (reduced).



5.0 GENERAL ROUTING GUIDELINES

Signal Name Conventions

The following conventions are used in describing the signals for Tegra:

- Signal names use a mnemonic to represent the function of the signal. For example, Secure Digital Interface #3 Command signal is represented as **SDMMC3_CMD**, written in bold to distinguish it from other text. All active low signals are identified by a # or an underscore followed by capital N (_N) after the signal name. For example, **SYS_RESET_N** indicates an active low signal. Active high signals do not have the underscore-N (_N) after the signal names. For example, **SDMMCx_CMD** indicates an active high signal. Differential signals are identified as a pair with the same names that end with _P & _N, just P & N or + & - (for positive and negative, respectively). For example, **USB1_DP** and **USB1_DN** indicate a differential signal pair.
- I/O Type The signal I/O type is represented as a code to indicate the operational characteristics of the signal. The table below lists the I/O codes used in the signal description tables.

Table 9. Signal Type Codes

Code	Definition
A	Analog
DIFF I/O	Bidirectional Differential Input/Output
DIFF IN	Differential Input
DIFF OUT	Differential Output
I/O	Bidirectional Input/Output
I	Input
O	Output
OD	Open Drain Output
I/OD	Bidirectional Input / Open Drain Output
P	Power

Routing Guideline Format

The routing guidelines have the following format to specify how a signal should be routed. Refer to the applicable Tegra platform specific Design Guides for nominal impedance values for some sample board stack-ups.

- Breakout traces are traces routed from BGA ball either to a point beyond the ball array, or to another layer where full normal spacing guidelines can be met. Breakout trace delay limited to 500 mils unless otherwise specified.
- After breakout, signal should be routed according to specified impedance for differential, single-ended, or both (for example: HDMI). Trace spacing to other signals also specified.
- Follow max & min trace delays where specified. Trace delays are typically shown in mm or in terms of signal delay in pico-seconds (ps) or both.
  - For differential signals, trace spacing to other signals must be larger of specified × dielectric height or inter-pair spacing
  - Spacing to other signals/pairs cannot be smaller than spacing between complementary signals (intra-pair).
  - Total trace delay depends on signal velocity which is different between outer (microstrip) & inner (stripline) layers of a PCB.

Signal Routing Conventions

Throughout this document, the following signal routing conventions are used:

SE Impedance (/ Diff Impedance) at x Dielectric Height Spacing

- Single-ended (SE) impedance of trace (along with differential impedance for diff pairs) is achieved by spacing requirement. Spacing is multiple of dielectric height. Dielectric height is typically different for microstrip & stripline. Note: 1 mil = 1/1000th of an inch.

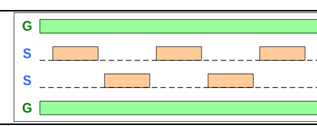
Note: Trace spacing requirement applies to SE traces or differential pairs to other SE traces or differential pairs. It does not apply to traces making up a differential pair. For this case, spacing/trace widths are chosen to meet differential impedance requirement.

General Routing Guidelines

Pay close attention when routing high speed interfaces, such as HDMI/DP, USB 3.0, PCIe or DSI/CSI. Each of these interfaces has strict routing rules for the trace impedance, width, spacing, total delay, and delay/flight time matching. The following guidelines provide an overview of the routing guidelines and notations used in this document.

- **Controlled Impedance**
  Each interface has different trace impedance requirements & spacing to other traces. It is up to designer to calculate trace width & spacing required to achieve specified single-ended (SE) & differential (Diff) impedances. Unless otherwise noted, trace impedance values are ±15%.
- **Max Trace Lengths/Delays**
  Trace lengths/delays should include the carrier board PCB routing (where the Jetson TX1 mating connector resides) and any additional routing on a Flex/ secondary PCB segment connected to main PCB. The max length/delay should be from Jetson TX1 to the actual connector (i.e. USB, HDMI, SD Card, etc.) or device (i.e. onboard USB device, Display driver IC, camera imager IC, etc.)
- **Trace Delay/Flight Time Matching**
  Signal flight time is the time it takes for a signal to propagate from one end (driver) to other end (receiver). One way to get same flight time for signal within signal group is to match trace lengths within specified delay in the signal group.
  - Total trace delay = Carrier PCB trace delay only. Do not exceed maximum trace delay specified.
  - For six layers or more, it is recommended to match trace delays based on flight time of signals. For example, outer-layer signal velocity could be 150psi (ps/inch) & inner-layer 180psi. If one signal is routed 10 inches on outer layer & second signal is routed 10 inches in inner layer, difference in flight time between two signals will be 300ps! That is a big difference if required matching is 15ps (trace delay matching). To fix this, inner trace needs to be 1.7 inches shorter or outer trace needs to be 2 inches longer.
  - In this design guide, terms such as intra-pair & inter-pair are used when describing differential pair delays. Intra-pair refers to matching traces within differential pair (for example, true to complement trace matching). Inter-pair matching refers to matching differential pairs average delays to other differential pair average delays.

General PCB Routing Guidelines

For GSSG stack-up to minimize crosstalk, signal should be routed in such a way that they are not on top of each other in two routing layers (see diagram to right)	
Do not route other signals or power traces/areas directly under or over critical high-speed interface signals.	

Note: *The requirements detailed in the Interface Signal Routing Requirements tables must be met for all interfaces implemented or proper operation cannot be guaranteed.*

6.0 USB, PCIE & SATA

Jetson TX1 allows multiple USB 3.0 & PCIe interfaces, and a single SATA interface to be brought out on the module. In some cases, these interfaces are multiplexed on some of the module pins. The tables below show several ways to bring out as many of the USB 3.0 or PCIe interfaces as possible to meet different design requirements. The first table covers many of the combinations possible on designs built around the Jetson TX1 only. The second table covers the combinations possible for both Jetson TX1 and future pin compatible modules.

Table 10. Jetson TX1 USB 3.0, PCIe & SATA Lane Mapping Configurations

	Jetson TX1 Pin Names			PEX1	PEX_RFU	PEX2	USB_SS1	PEX0	USB_SS0	na	SATA
	Tegra X1 Lanes			**Lane 0**	**Lane 1**	**Lane 2**	**Lane 3**	**Lane 4**	**Lane 5**	**Lane 6**	**SATA**
	Avail. Outputs from Jetson TX1										
Configs	**USB 3.0**	**PCIe**	**SATA**								
1(Carrier)	1	1x1 + 1x4	1	PCIe#1_0	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0	USB_SS#1	USB_SS#0 On-Jetson TX1 For Gigabit Ethernet	SATA
2	2	1x1 + 1x4	0	PCIe#1_0	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0	USB_SS#1		USB_SS#3
3	2	1x4	1	USB_SS#2	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0	USB_SS#1		SATA
4	2	2x1	1	PCIe#1_0			USB_SS#2	PCIe#0_0	USB_SS#1		SATA
5	3	2x1	0	PCIe#1_0			USB_SS#2	PCIe#0_0	USB_SS#1		USB_SS#3

Table 11. Forward Compatible USB 3.0, PCIe & SATA Lane Mapping Configurations

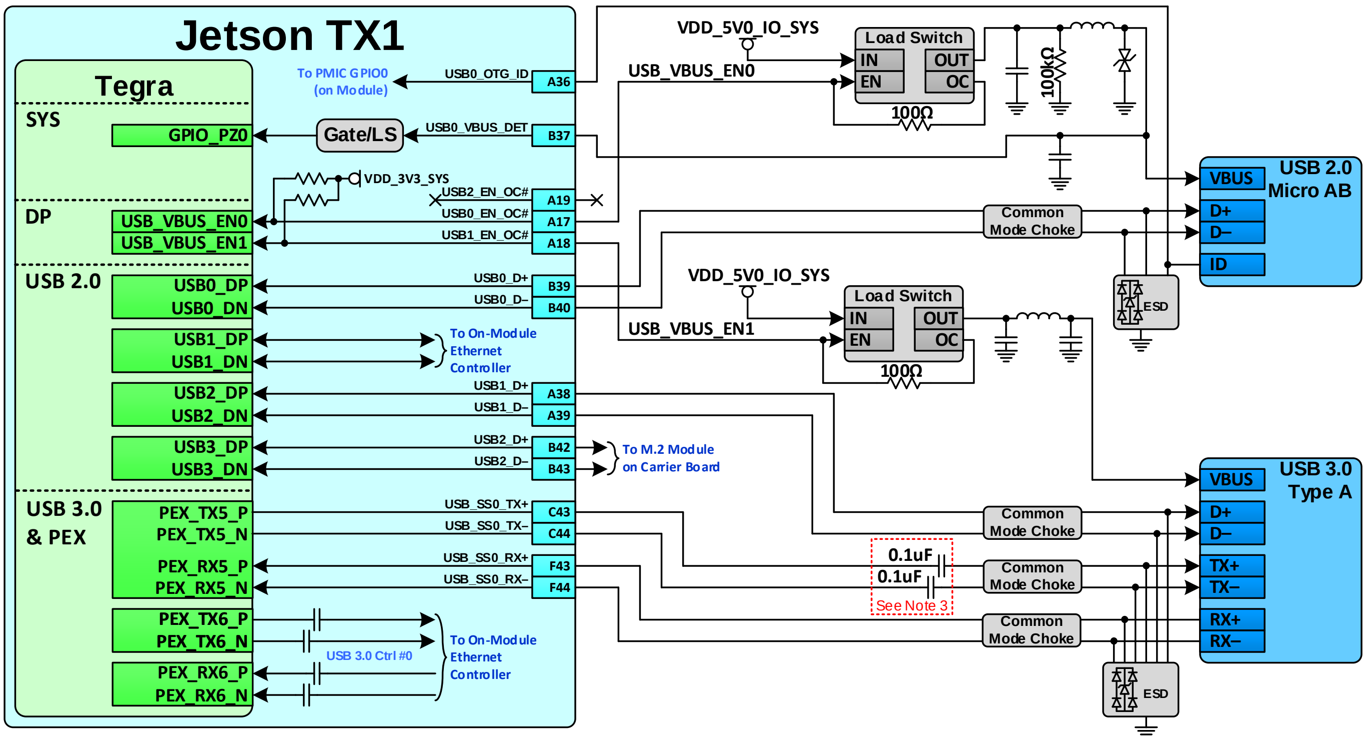
	Module Pin Names			PEX1	PEX_RFU	PEX2	USB_SS1	PEX0	USB_SS0	SATA
	Avail. Outputs from Module									
Configs	**USB 3.0**	**PCIe**	**SATA**							
6	0	1x1 + 1x4	1	PCIe#1_0	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0		SATA
7	1	1x4	1	USB_SS#2	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0		SATA
8	1	1x1, 1x2	1	PCIe#1_0			PCIe#0_1	PCIe#0_0	USB_SS#1	SATA
9	2	1x2	1	USB_SS#2			PCIe#0_1	PCIe#0_0	USB_SS#1	SATA
10	2	2x1	1	PCIe#1_0			USB_SS#2	PCIe#0_0	USB_SS#1	SATA

Note:

1. The Jetson TX1 Module has been designed to enable use cases listed in the table above. However, released Software does not support all configurations, nor has every configuration been validated.
   - Configuration 1 in Table 10 or 6 & 8 in Table 11 represent supported and validated Jetson TX1 Developer Kit configurations. That configuration is supported by the released Software, and the PCIe, USB 3.0, and SATA interfaces have been verified on the carrier board.
   - The USB 3.0 controller #2 interface can optionally be brought out on the PEX1 or USB_SS1 pins, and has been verified on the module. However, that configuration may not be supported/tested with the released Software.
   - The USB 3.0 controller #3 on the SATA pins has been verified at the chip level, but not on the module, and is not supported with the released Software.
2. The cell colors highlight the different PCIe and USB 3.0 controllers. Light and Medium green are used for PCIe controllers #0 and #1. Four shades of blue are used for USB 3.0 controllers #[0:3]. SATA is highlighted in orange.
3. Any x4 configuration can be used as a single x2 using only lanes 0 & 1 or a single x1 using only lane 0. Any x2 configuration can be used as a single x1 using only lane 0.
4. In order to ease routing, the order of lanes for PCIe #0 can either be as shown above, or the reverse (I.e., PCIE#0_3 on lane 4, PCIE#0_2 on lane 3, etc.).

6.1 USB

Figure 8 USB Connection Example



Note:
1. AC capacitors should be located close to either the USB connector, or the Jetson TX1 pins.
2. Common mode filters on USB 2.0 & 3.0 interfaces are optional. If placed, they must be selected to meet USB spec. requirements. For USB 3.0, see the "USB 3.0 Common Mode Choke Requirements" table near the end of this section.
3. For USB 3.0 IF shown above (USB_SS0_TX/RX), AC caps are required on the TX lines. If routed directly to a peripheral, AC caps are needed on the peripheral TX lines as well. The AC caps are recommended to be located near the Jetson TX1 connector pins, although locating the caps near the peripheral RX pins is acceptable.
4. USB0 must be available to use as USB Device for USB Recovery Mode.
5. Connector used must be USB-IF certified if USB 3.0 implemented.
6. Unused **PCIe RX** signals should be tied to **GND**

USB 2.0 Design Guidelines

These requirements apply to the USB 2.0 controller PHY interfaces: **USB[2:0]_D–/D+**

Table 12. USB 2.0 Interface Signal Routing Requirements

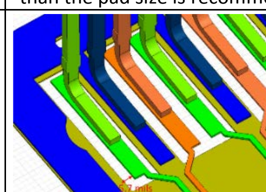
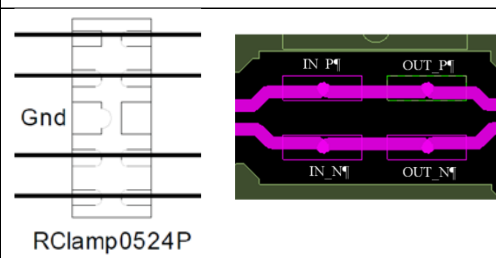
Parameter		Requirement	Units	Notes
Max Frequency (High Speed)	Bit Rate/UI period/Frequency	480/2.083/240	Mbps/ns/MHz	
Max Loading	High Speed / Full Speed / Low Speed	10 / 150 / 600	pF	
Reference plane		**GND**		
Trace Impedance	Diff pair / Single Ended	90 / 50	Ω	±15%
Via proximity (Signal to reference)		< 3.8 (24)	mm (ps)	See Note 1
Max Trace Delay	Microstrip / Stripline	6 (960)	In (ps)	
Max Intra-Pair Skew between **USBx_D+** & **USBx_D–**		7.5	ps	

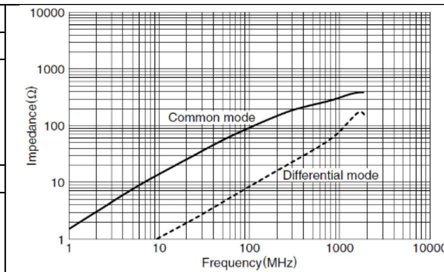
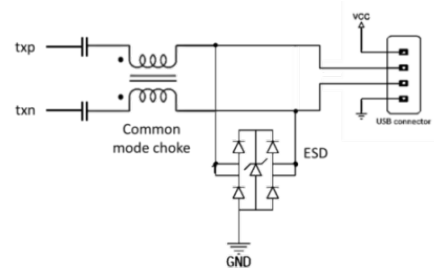
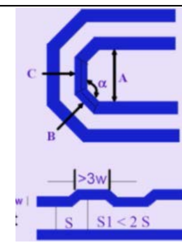
Note:
1. Up to 4 signal Vias can share a single **GND** return Via.
2. Adjustments to the USB drive strength, slew rate, termination value settings should not be necessary, but if any are made, they MUST be done as an offset to default values instead of overwriting those values.

USB 3.0 Design Guidelines

The requirements following apply to the USB 3.0 controller PHY interfaces

Table 13. USB 3.0 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI period	5.0 / 200	Gbps / ps	
Max Number of Loads	1	load	
Termination	90 differential	Ω	On-die termination at TX & RX
Reference plane	**GND**		
Trace Impedance			
Trace Impedance — Diff pair / Single Ended	85 / 45-55	Ω	±15%
Trace Spacing Pair-Pair (inter-pair) — Microstrip / Stripline To plane & capacitor pad — Microstrip / Stripline To unrelated high-speed signals — Microstrip / Stripline	 4x / 3x 4x / 3x 4x / 3x	 dielectric	
Trace Length/Skew			
Breakout Region — Max trace delay Trace width/spacing	41.9 Minimum	ps	 4x or wider dielectric height spacing is preferred
Max Trace Length	76.2 (480)	mm (ps)	Max length assumes USB3 Tx voltage swing set at 0.8V MIN, length can increase if Tx swing is increased.
Max PCB Via distance from pin	6.29 (41.9)	mm (ps)	
Max Within Pair (Intra-Pair) Skew	0.15 (0.5)	mm (ps)	
Intra-pair matching between subsequent discontinuities	0.15 (0.5)	mm (ps)	Do trace length matching before hitting discontinuities
Differential pair uncoupled length	6.29 (41.9)	mm (ps)	
AC Cap			
Value	0.1	uF	Smallest size preferred (i.e. 0201). See note under USB Connection Diagrams for details on when AC capacitors are required
Location (max distance to adjacent discontinuities)	8 (53.22)	mm (ps)	The AC cap location should be located as close as possible to nearby discontinuities
Via			
Max Via Stub Length	0.4	mm	long via stub requires review (IL & resonance dip check)
Voiding			
AC cap pad voiding			Voiding the plane directly under the pad 3-4 mils larger than the pad size is recommended
Connector voiding			 Voiding the ground below the footprint of signal lanes. 5.7mils larger than the print is suggested.
ESD			
Preferred device			Type: SEMTECH RClamp0524p. Optional. Place ESD component near connector
Max Junction capacitance (IO to GND)	0.8	pF	
Location (Max distance to Connector)	8 (53)	mm (ps)	
Layout recommendations			
Common-mode Choke			
Preferred device			Type: TDK ACM2012D-900-2P. Only if needed. Place near connector. Refer to Common Mode Choke Requirement section.
Location - Max distance from to adjacent discontinuities – ex, connector, AC cap)	8 (53)	mm (ps)	TDK ACM2012D-900-2P

Common-mode impedance @ 100MHz Min/Max	65/90	Ω	
Max Rdc	0.3	Ω	
Differential TDR impedance	90	Ω @T_R-200ps (10%-90%)	
Min Sdd21 @ 2.5GHz	2.22	dB	
Max Scc21 @ 2.5GHz	19.2	dB	
Component Order			
Component order			Chip – AC capacitor (TX only) – common mode choke – ESD – Connector: 
Serpentine			
Min spacing between each turn Microstrip / Stripline	4x / 3x	diff pair pitch	S1 must be taken care in order to consider Xtalk to adjacent pair 
Min bend angle	135	deg (α)	
Dimension Min A Spacing / Min B, C Length / Min Jog Width	4x / 1.5x / 3x	Trace width	

Common USB Routing Guidelines

Guideline
If routing to USB device or USB connector includes a flex or 2nd PCB, the total routing including all PCBs/flexes must be used for the max trace & skew calculations.
Keep critical USB related traces away from other signal traces or unrelated power traces/areas or power supply components

Table 14. Tegra USB 2.0 Signal Connections

Jetson TX1 Ball Name	Type	Termination	Description
USB[2:0]_D+ **USB[2:0]_D–**	DIFF I/O	90Ω common-mode chokes close to connector. ESD Protection between choke & connector on each line to GND	**USB Differential Data Pair:** Connect to USB connector, Mini-Card Socket, Hub or other device on the PCB.

Table 15. Miscellaneous USB 2.0 Signal Connections

Jetson TX1 Pin Name	Type	Termination	Description
USB0_VBUS_DET	A	100kΩ resistor to GND. See reference design for VBUS power filtering.	**USB0 VBus Detect:** Connect to VBUS pin of USB connector receiving USB0_+/– interface. Also connects to VBUS power supply if host mode supported.
USB0_OTG_ID	A		**USB Identification:** Connect to ID pin of USB OTG connector receiving USB0_P/M interface.

Table 16. Tegra USB 3.0 Signal Connections

Jetson TX1 Pin Name	Type	Termination	Description
USB_SS0_TX+/– (USB 3.0 Ctrl #1) **PEX1_TX+/– (USB 3.0 Ctrl #2)** **USB_SS1_TX+/– (USB 3.0 Ctrl #2)**	DIFF Out	Series 0.1uF caps. Common-mode chokes & ESD Protection near connector if these are	**USB 3.0 Differential Transmit Data Pairs:** Connect to USB 3.0 connectors, Hubs or other devices on the PCB.

SATA_TX+/–	**(USB 3.0 Ctrl #3)**		used.	
USB_SS0_RX+/– **PEX1_RX+/–** **USB_SS1_RX+/–** **SATA_RX+/–**	**(USB 3.0 Ctrl #1)** **(USB 3.0 Ctrl #2)** **(USB 3.0 Ctrl #2)** **(USB 3.0 Ctrl #3)**	DIFF In	If routed directly to a peripheral on the board, AC caps are needed for the peripheral TX lines. Common-mode chokes & ESD Protection near connector if these are used.	**USB 3.0 Differential Receive Data Pairs:** Connect to USB 3.0 connectors, Hubs or other devices on the PCB.

6.2 Gigabit Ethernet

The Jetson TX1 integrates a Realtek RTL8153AI-VB-CG Gigabit Ethernet controller. The magnetics & RJ45 connector would be implemented on the Carrier board. Contact Realtek for guidelines for the Carrier board placement/routing.

Figure 9. Jetson TX1 Ethernet Connections

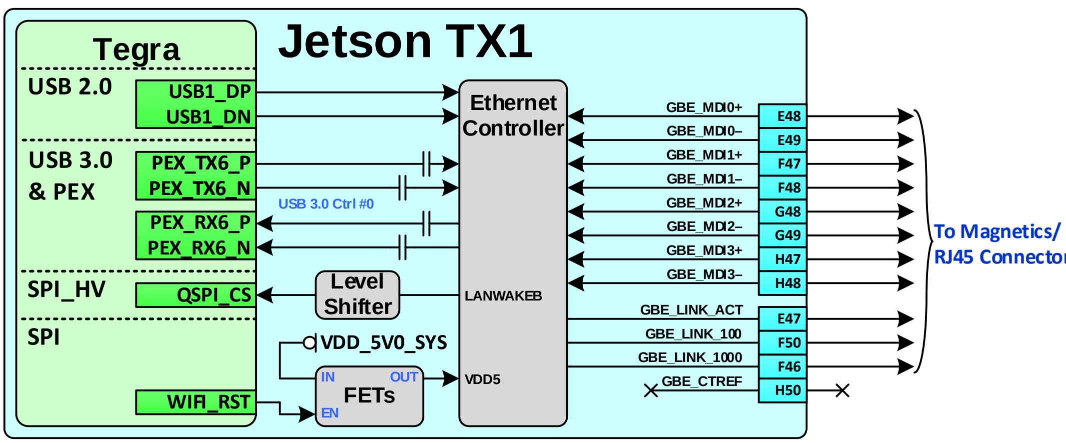
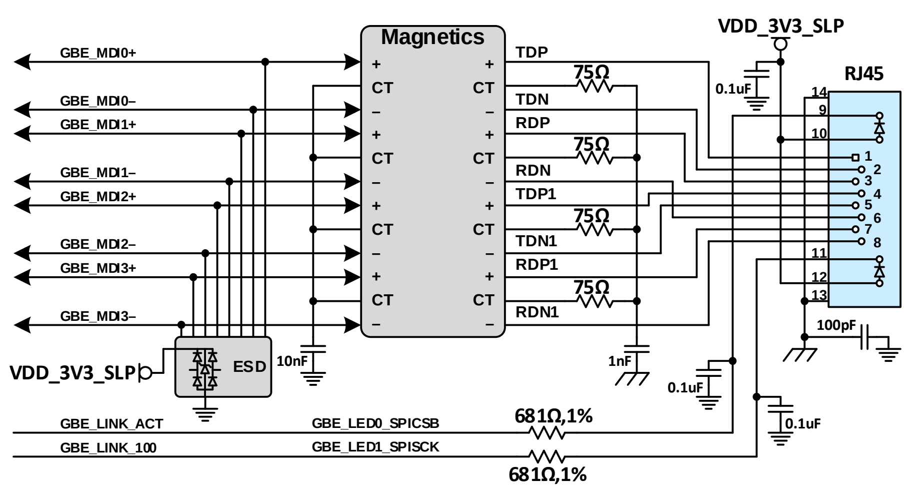


Figure 10. Gigabit Ethernet Magnetics & RJ45 Connections



Note: The connections above match those used on the Jetson TX1 carrier board and are shown for reference.

Table 17. Ethernet MDI Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Reference plane		**GND**		
Trace Impedance	Diff pair / Single End	100 / 50	Ω	±15%. Differential impedance target is 100Ω. 90Ω can be used if 100Ω is not achievable
Min Trace Spacing (Pair-Pair)		0.763	mm	

Max Trace Length	120 (755)	mm (ps)	This includes routing on Jetson TX1 & carrier board. The routing on Jetson TX1 is <10mm on any trace. The signals go through the main 400-pin board-board connector, so the max length should be kept as short as possible.
Max Within Pair (Intra-Pair) Skew	0.15 (1)	mm (ps)	
Number of Vias	minimum		Ideally there should be no vias, but if required for breakout to Ethernet controller or magnetics, keep very close to either device.

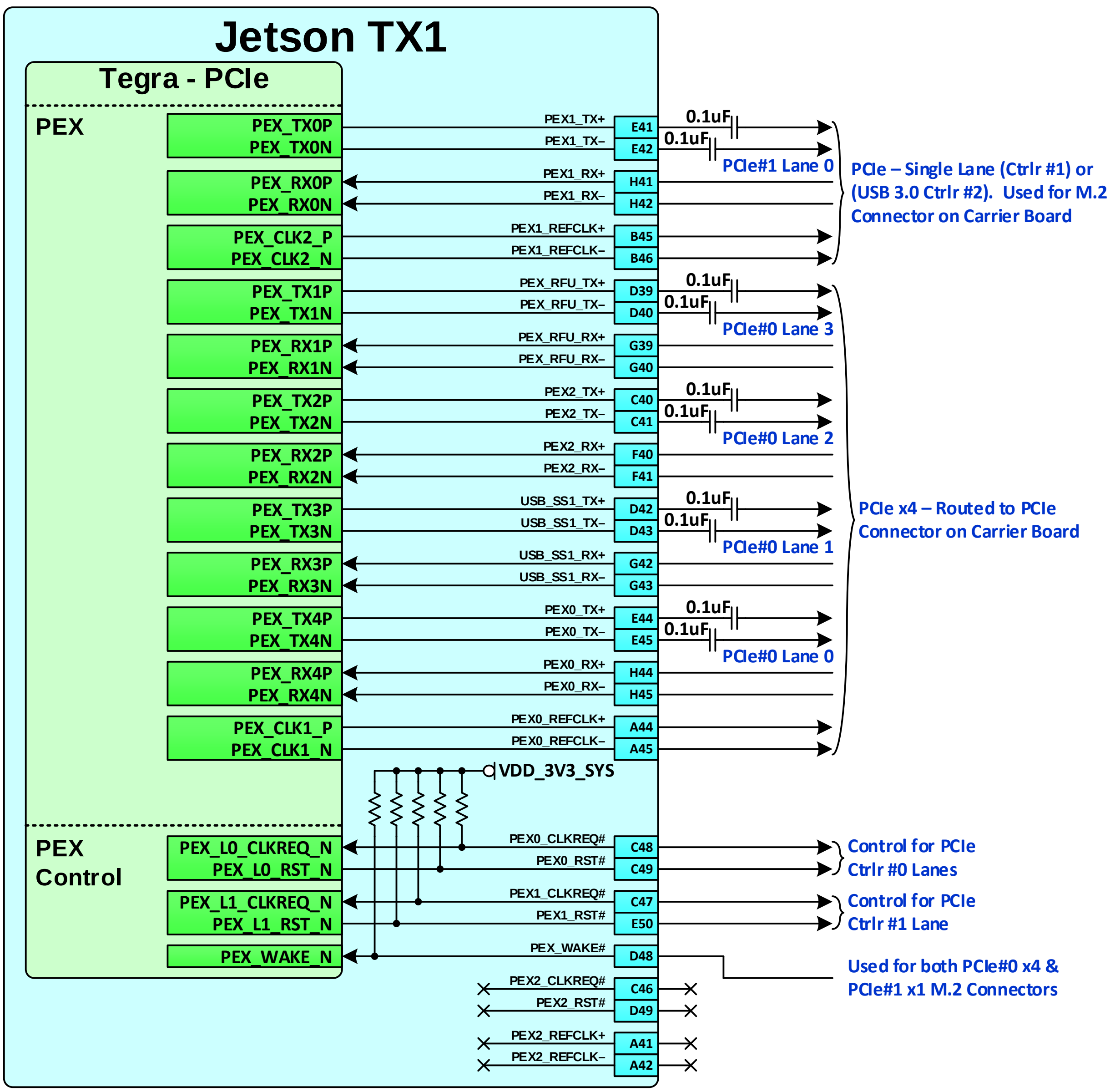
Table 18. Ethernet Signal Connections

Jetson TX1 Pin Name	Type	Termination	Description
GBE_MDI[3:0]+/–	DIFF I/O	ESD device to GND per signal	**Gigabit Ethernet MDI IF Pairs:** Connect to Magnetics +/– pins
GBE_LINK_ACT	O	681Ω series resistor & 0.1uF capacitor to **GND**	**Gigabit Ethernet ACT :** Connect to ACK LED on connector.
GBE_LINK100	O	681Ω series resistor & 0.1uF capacitor to **GND**	**Gigabit Ethernet Link 100 :** Connect to Link 100 LED on conn.
GBE_LINK1000	O	681Ω series resistor & 0.1uF capacitor to **GND**	**Gigabit Ethernet Link 1000 :** Connect to Link 1000 LED on conn.
GBE_CTREF	na		**Not used**

6.3 PEX (PCIe)

Tegra contains a PEX (PCIe) controller that supports up to 5 lanes, and 2 separate interfaces. This narrow, high-speed interface can be used to connect to a variety of high bandwidth devices.

Figure 11. Example Connections for a PCIe x1 Interface & a PCIe x4 Interface



PCIE Design Guidelines

Table 19. PCIE Interface Signal Routing Requirements

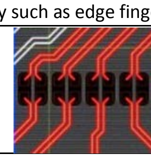
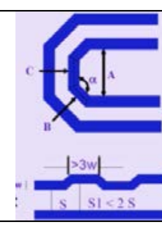
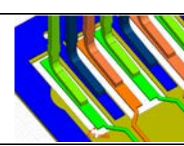
Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI Period	5.0 / 200	Gbps / ps	2.5GHz, half-rate architecture
Configuration / Device Organization	1	Load	
Topology	Point-point		Unidirectional, differential
Termination	50	Ω	To **GND** Single Ended for P & N
Impedance			
Trace Impedance differential / Single Ended	85 / 50	Ω	±15%. See note 1
Reference plane	**GND**		
Spacing			
Trace Spacing (Stripline/Microstrip) Pair – Pair To plane & capacitor pad To unrelated high-speed signals	3x / 4x 3x / 4x 3x / 4x	Dielectric	
Length/Skew			
Breakout region (Max Length)	41.9	ps	Minimum width and spacing. 4x or wider dielectric height spacing is preferred
Max trace length	5.5 (880)	in (ps)	
Max PCB via distance from the BGA	41.9	ps	Max distance from BGA ball to first PCB via.
PCB within pair (intra-pair) skew	0.15 (0.5)	mm (ps)	Do trace length matching before hitting discontinuities
Within pair (intra-pair) matching between subsequent discontinuities	0.15 (0.5)	mm (ps)	
Differential pair uncoupled length	41.9	ps	
Via			
Via placement	Place **GND** vias as symmetrically as possible to data pair vias. **GND** via distance should be placed less than 1x the diff pair via pitch		
Max # of Vias PTH Vias Micro-Vias	2 for TX traces & 2 for RX trace No requirement		
Max Via stub length	0.4	mm	Longer via stubs would require review
Routing signals over antipads	Not allowed		
AC Cap			
Value Min/Max	0.075 / 0.2	uF	Only required for TX pair when routed to connector
Location (max length to adjacent discontinuity)	8	mm	Discontinuity such as edge finger, component pad
Voiding	Voiding the plane directly under the pad 3-4 mils larger than the pad size is recommended.		
Serpentine			
Min spacing between each turn Microstrip Stripline	4x 3x	diff pair pitch	
Min bend angle	135	deg (a)	
Dimension Min A Spacing Min B, C Length Min Jog Width	4x 1.5x 3x	Trace width	S1 must be taken care in order to consider Xtalk to adjacent pair 
MIsc.			
Routing signals over antipads	Not allowed		
Routing over voids	When signal pair approaches Vias, the maximal trace length across the void on the plane is 50mil.		
Connector			
Voiding	Voiding the plane directly under the pad 5.7 mils larger than the pad size is recommended.		
Keep critical PCIe traces such as PEX_TX/RX, TERMP etc. away from other signal traces or unrelated power traces/areas or power supply components			

Table 20. PCIE Signal Connections

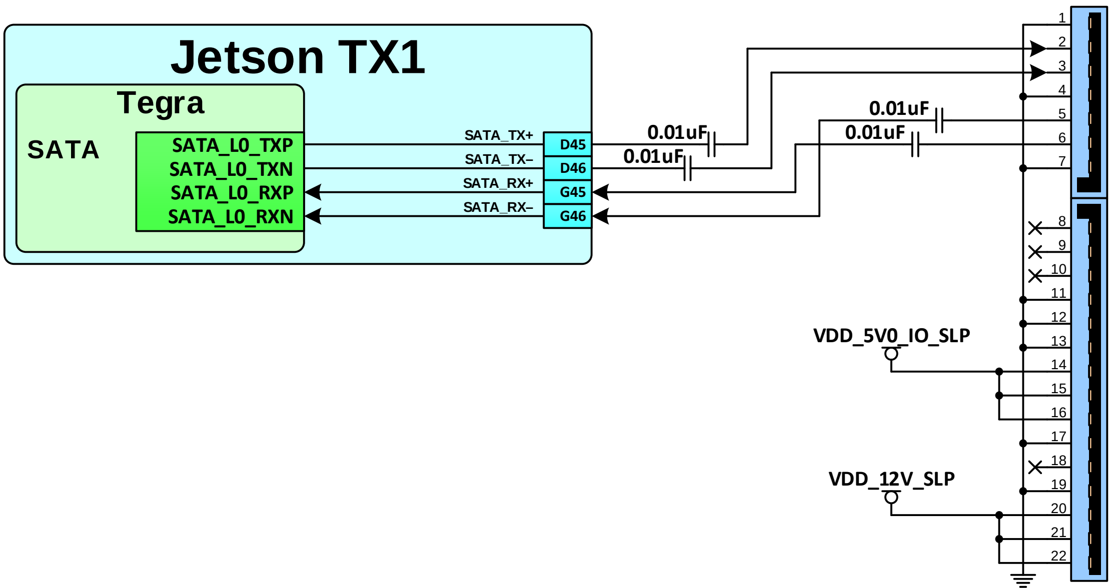
Jetson TX1 Pin Name	Type	Termination	Description
PCIe Controller #0 (x4)			
PEX_RFU_TX+/– (Lane 3) **PEX2_TX+/– (Lane 2)** **USB_SS1_TX+/– (Lane 1)** **PEX0_TX+/– (Lane 0)**	DIFF OUT	Series 0.1uF Capacitor	**Differential Transmit Data Pairs:** Connect to **TX_P/N** pins of PCIe connector or **RX_P/N** pin of PCIe device through AC cap according to supported configuration.
PEX_RFU_RX+/– (Lane 3) **PEX2_RX+/– (Lane 2)** **USB_SS1_RX+/– (Lane 1)** **PEX0_RX_+/– (Lane 0)**	DIFF IN	Series 0.1uF capacitors near Jetson TX1 pins or device if device on main PCB.	**Differential Receive Data Pairs:** Connect to **RX_P/N** pins of PCIe connector or **TX_P/N** pin of PCIe device through AC cap according to supported configuration.
PEX0_REFCLK+/–	DIFF OUT		**Differential Reference Clock Output:** Connect to **REFCLK_P/N** pins of PCIe device/connector
PEX0_CLKREQ#	I/O	47KΩ pull-up to **VDD_3V3_SYS** on each line (exists on Jetson TX1)	**PEX Clock Request for PEX0_REFCLK:** Connect to **CLKREQ** pins on device/connector(s)
PEX0_RST#	O		**PEX Reset:** Connect to **PERST** pins on device/connector(s)
PCIe Controller #1 (x1)			
PEX1_TX+/–	DIFF OUT	Series 0.1uF Capacitor	**Differential Transmit Data Pairs:** Connect to **TX+/–** pins of PCIe connector or **RX_+/–** pin of PCIe device through AC cap according to supported configuration.
PEX1_RX+/–	DIFF IN	Series 0.1uF capacitors near Jetson TX1 pins or device if device on main PCB.	**Differential Receive Data Pairs:** Connect to **RX_+/–** pins of PCIe connector or **TX_+/–** pin of PCIe device through AC cap according to supported configuration.
PEX1_REFCLK+/–	DIFF OUT		**Differential Reference Clock Output:** Connect to **REFCLK_**+/– pins of PCIe device/connector
PEX1_CLKREQ#	I/O	47KΩ pull-up to **VDD_3V3_SYS** on each line (exists on Jetson TX1)	**PEX Clock Request for PEX1_REFCLK:** Connect to **CLKREQ** pins on device/connector(s)
PEX1_RST#	O		**PEX Reset:** Connect to **PERST** pins on device/connector(s)
Common			
PEX_WAKE#	I	47KΩ pull-up to **VDD_3V3_SYS** (exists on Jetson TX1)	**PEX Wake:** Connect to **WAKE** pins on device or connector

Note: Check "Supported USB 3.0, PEX & SATA Interface Mappings" tables earlier in this section for PCIE IF mapping options.

6.4 SATA

A Gen 2 SATA controller is implemented on Tegra. The interface is brought to the Jetson TX1 edge connector as shown in the figure below.

Figure 12. Example Connections for SATA Connector



SATA Design Guidelines

Note: For proper operation, the requirements below must be met in full, and the programming of the UPHY pads (used for SATA) should match the Nvidia software default settings.

Table 21. SATA Signal Routing Requirements

Parameter		Requirement	Units	Notes
Specification				
Max Frequency	Bit Rate / UI	3.0 / 333.3	Gbps / ps	1.5GHz
Topology		Point to point		Unidirectional, differential
Configuration / Device Organization		1	load	
Max Load (per pin)		0.5	pf	
Termination		100	Ω	On die termination
Impedance				
Reference plane		**GND**		
Trace Impedance	Differential Pair / Single Ended	95 / 45-55	Ω	±15%
Spacing				
Trace Spacing Pair-to-pair (inter-pair) To plane & capacitor pad To unrelated high-speed signals	 Stripline / Microstrip Stripline / Microstrip Stripline / Microstrip	 3x / 4x 3x / 4x 3x / 4x	 Dielectric	
Length/Skew				
Breakout region	Max Length Spacing	41.9 Min width/spacing	ps	4x or wider dielectric height spacing is preferred
Max Trace Length/Delay		76.2 (480)	Mm (ps)	
Max PCB Via distance from pin		6.29 (41.9)	mm (ps)	
Max Within Pair (Intra-Pair) Skew		0.15 (0.5)	mm (ps)	
Intra-pair matching between subsequent discontinuities		0.15 (0.5)	mm (ps)	Do trace length matching before hitting discontinuities
Differential pair uncoupled length		6.29 (41.9)	mm (ps)	
AC Cap				
AC Cap Value	typical (max)	0.01 (0.012)	uF	

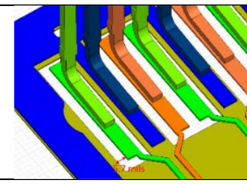
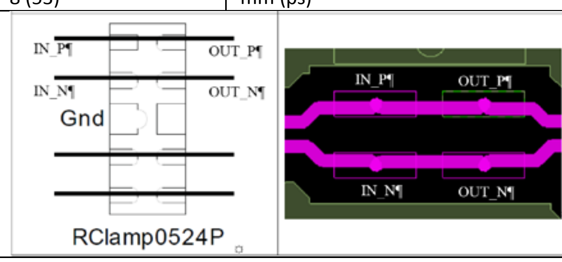
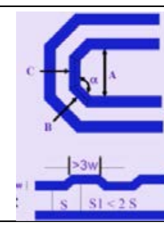
Parameter	Requirement	Units	Notes
AC Cap Location (max distance from adjacent discontinuities)	8 (53.22)	mm (ps)	The AC cap location should be located as close as possible to nearby discontinuities.
Via			
GND Via Placement	Place ground vias as symmetrically as possible to data pair vias GND via distance should be placed less than 1x the diff pair via pitch		
Max # of vias	3		If all are through-hole
Via stub length	< 0.4	mm	
Voiding			
AC cap pad voiding	Voiding the plane directly under the pad 3-4 mils larger than the pad size is recommended		
Connector voiding (Required)	The size of voiding can be same as the size of pin pad		
ESD			
ESD protection device (Optional)	Type: SEMTECH RClamp0524p. Place ESD component near connector. A design may include the footprints for ESD as a stuffing option. The junction capacitance in ESD may cause effect on signal integrity, so it's important to choose an ESD component with low capacitance and whose package design is optimized for high speed links. The SEMTECH ESD Rclamp0524p has been well verified with its 0.3pF capacitance.		
Max distance from ESD Device to Connector	8 (53)	mm (ps)	
Recommended ESD layout			
Choke			
Common mode choke	Type: TDK ACM2012D-900-2P. Only if needed. Place near connector. Refer to Common Mode Choke Requirement section.		
Max distance from common mode choke to adjacent discontinuities (ex, connector, AC cap)	8 (53)	mm (ps)	
Serpentine			
Min spacing between each turn Microstrip Stripline	4x 3x	diff pair pitch	S1 must be taken care in order to consider Xtalk to adjacent pair 
Min bend angle	135	deg (a)	
Dimension Min A Spacing Min B, C Length Min Jog Width	4x 1.5x 3x	Trace width	

Table 22. SATA Signal Connections

Jetson TX1 Pin Name	Type	Termination	Description
SATA_TX+/–	DIFF OUT	Series 0.01uF Capacitor	**Differential Transmit Data Pair:** Connect to **SATA+/–** pins of SATA device/connector through termination (capacitor)
SATA_RX+/–	DIFF IN	Series 0.01uF Capacitor near connector or near device if device on main PCB	**Differential Receive Data Pair:** Connect to **SATA+/–** pins of SATA device/connector through termination (capacitor)

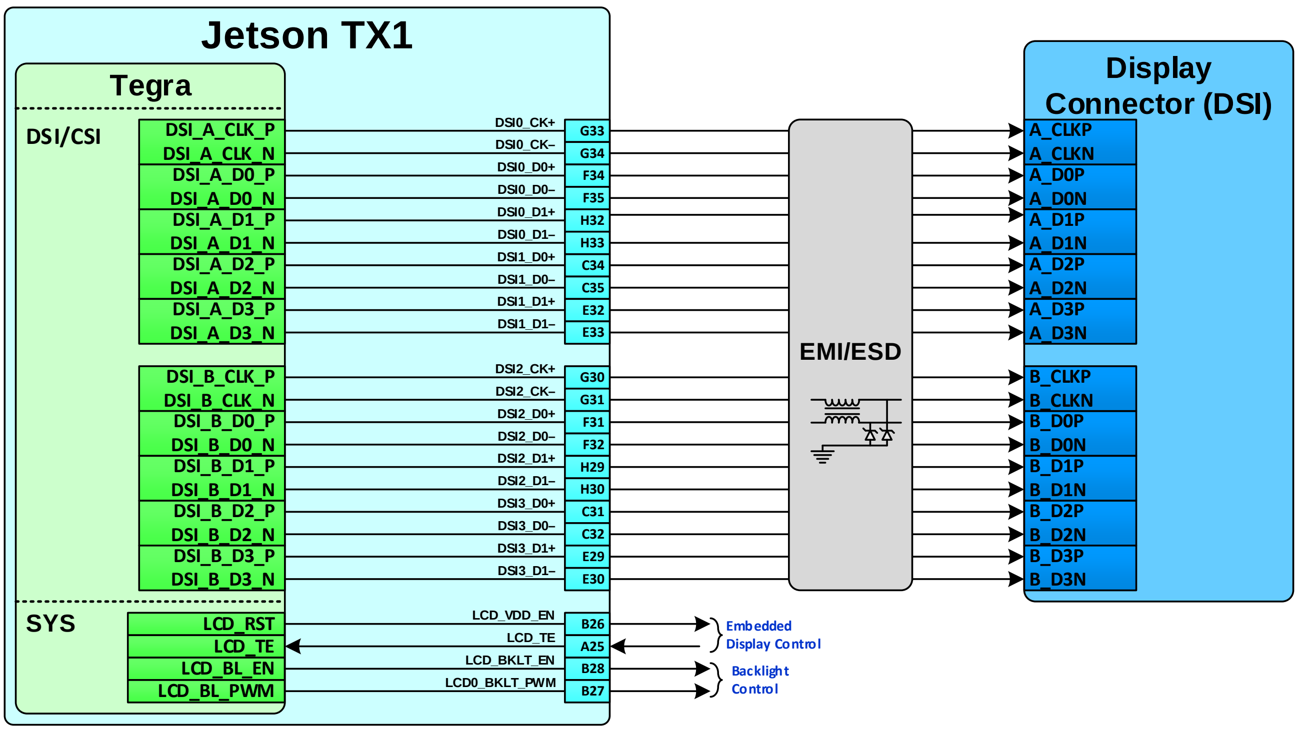
7.0 DISPLAY

Tegra X1 Embedded designs can select from several display options including MIPI DSI & eDP for embedded displays, and HDMI or DP for external displays.

7.1 MIPI DSI

Tegra supports eight total MIPI DSI data lanes and two clock lanes, allowing up to two 4-lane interfaces. These can be used for two separate displays, or together for a single display (clock lane per 4 data lanes still applies for the single display case. Each data channel has peak bandwidth up to 1.5Gbps.

Figure 13: DSI 2 x 4-Lane Connection Example



Note: If EMI/ESD devices are necessary, they must be tuned to minimize impact to signal quality, which must meet the DSI spec. requirements for the frequencies supported by the design.

MIPI DSI / CSI Design Guidelines

Table 23. MIPI DSI & CSI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency/Data Rate (per data lane)	750 / 1500	MHz/Mbps	
Number of Loads	1	load	
Reference plane	**GND**		
Trace Impedance — Diff pair / Single Ended	90-100 / 45-50	Ω	±10%
Via proximity (Signal to reference)	< 0.65 (3.8)	mm (ps)	
Intra-pair Trace Spacing	0.15mm	mm	Can be adjusted to meet Differential Impedance. Loosely Coupled Diff. Pair recommended by Spec.
Inter-pair Trace Spacing — Microstrip / Stripline	4x / 3x	dielectric	
Max PCB Breakout length	5	mm	
Max Trace Length/Delay	186 (1100)	mm (ps)	
Max Intra-pair Skew	1	ps	

Parameter	Requirement	Units	Notes
Max Trace Delay Skew between **DQ** & **CLK**	5	ps	**DQ** includes all the data lines associated with a single clock. This may be 2 differential data lanes for a x2 interface, or 4 differential data lanes for a x4 interface.
Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components			

MIPI DSI / CSI Connection Guidelines

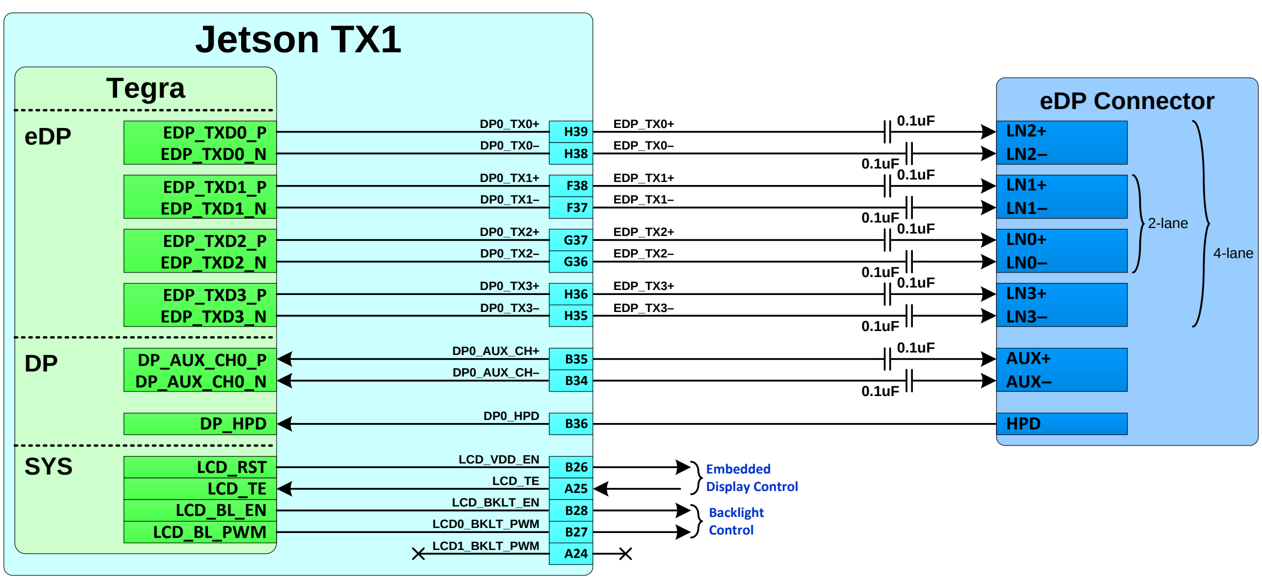
Table 24. MIPI DSI Signal Connections

Jetson TX1 Pin Name	Type	Termination	Description
DSI0_CK+/–	DIFF OUT		**DSI 0 Differential Clock:** Connect to **CLKn & CLKp** pins of the primary DSI display
DSI0_D[1:0]+/–	DIFF OUT		**DSI 0 Differential Data Lanes 1:0:** Connect to lower 2 lanes of the primary DSI display.
DSI1_D[1:0]+/–	DIFF OUT		**DSI 1 Differential Data Lanes 1:0:** Connect to upper two lanes of the primary 4 lane DSI display.
DSI2_CK+/–	DIFF OUT		**DSI 2 Differential Clock:** Connect to **CLKn & CLKp** pins of either the primary DSI display if it supports a 2 x4 lane interface, or a secondary DSI display
DSI2_D[1:0]+/–	DIFF OUT		**DSI 2 Differential Data Lanes 1:0:** Connect to lower 2 lanes of a secondary DSI display or lower 2 lanes of the upper 4 lanes of the primary DSI display supporting a 2 x4 lane interface.
DSI3_D[1:0]+/–	DIFF OUT		**DSI 3 Differential Data Lanes 1:0:** Connect to upper 2 lanes of a secondary DSI display or upper 2 lanes of upper 4 lanes of the primary DSI display supporting a 2 x4 lane interface.
LCD_RST	O		**LCD Reset Input:** Connect to LCD reset pin if supported
LCD_TE	I		**LCD Tearing Effect:** Connect to LCD Tearing Effect pin if supported
LCD_BL_EN	O		**LCD Backlight Enable:** Connect to LCD backlight solution enable if supported
LCD0_BKLT_PWM	O		**LCD Backlight Pulse Width Modulation:** Connect to LCD backlight solution PWM input if supported

7.2 eDP

Tegra supports an eDP interface. See the Tegra X1 Series Data Sheet for the maximum resolution supported. The eDP interface can also be used for DP – see the DP section for connections.

Figure 14: eDP Connection Example



Note:
- HPD only applicable if interface used for DP instead of eDP. See DP section for additional DP_AUX connection details.
- If eDP interface used for DP, note that HDCP is not supported.

eDP Routing Guidelines

Figure 15: eDP (Differential Main Link) Topology

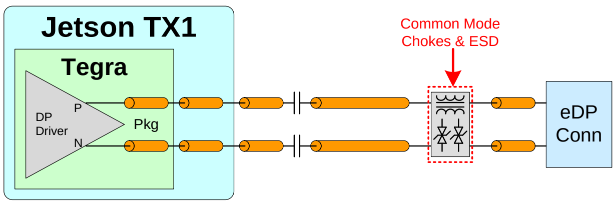


Table 25. eDP Main Link Signal Routing Requirements (Including DP_AUX)

Parameter	Requirement	**Units**	**Notes**
Max Data Rate (per data lane)	5.4	Gbps	
Min UI	185	ps	
Number of Loads	1	load	
Topology			Point-Point, Differential, Unidirectional
Termination	100	**Ω**	On die at TX/RX
Reference plane	GND		
Trace Impedance Differential pair Single Ended	100 95 85 45	Ω (±10%)	- 100Ω by spec. 95Ω/85Ω are options for implementation - intrinsic Zdiff does not account for trace coupling - 95Ω is to account for DP-HDMI co-layout - 85Ω is to account for low-loss profile
Trace loss characteristic:	< 0.8	dB/in @ 2.7GHz	The following max length is derived based on this characteristic. The length constraint must be re-defined if the loss characteristic is changed
Max Total Delay (Jetson TX1 pin to connector) **RBR/HBR** Stripline Microstrip **HBR2** Stripline Microstrip (w/5x dielectric height spacing) Microstrip (w/7x dielectric height spacing)	 215 (1137.5) 215 (975) 101.6 (700) 89 (525) 101.6 (600ps)	 mm (ps)	Stripline is preferred. 175ps/inch delay for stripline & 150ps/inch delay for microstrip used for delay calculations.
Pair-to-pair spacing Stripline Microstrip (HBR & RBR) Microstrip (HBR2)	3x 4x 5x to 7x	dielectric	Stripline: 3x of the thinner of above and below
PCB main link to AUX Spacing Stripline Microstrip	3x 5x	dielectric	Stripline: 3x of the thinner of above & below
Max Intra-Pair (within pair) Skew	0.15 (1)	mm (ps)	Do not perform length matching within breakout region. Do trace length matching before hitting discontinuity (i.e. matching to <1ps before the vias or any discontinuity to minimize common mode conversion.) (.
Max Inter-Pair (pair to pair) Skew	150	ps	
GND transition Via	< 1x	diff pair pitch	For signals switching reference layers, add symmetrical ground stitching Via near signal Vias. GND Via distance should be < 1X diff pair Via pitch
Max signal transition Vias PTH vias HDI (micro) vias	2 Not limited		 If total channel loss meets IL spec
Max Via stub length	1	mm	
AC coupling cap	100	nF	Discrete 0402
Max Dist. from AC cap to conn. **RBR/HBR** **HBR2**	No requirement 0.5	 in	
AC cap pad voiding **RBR/HBR** **HBR2**	No voiding required		**HBR2**: Voiding the plane directly under the pad 3-4 mils larger than the pad size is recommended.

Table 26. Additional eDP Requirements/Recommendations

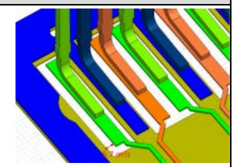
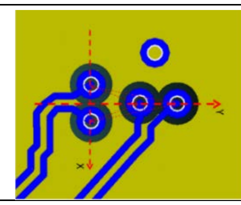
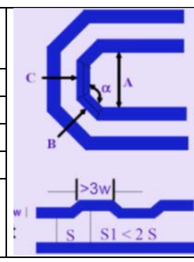
Parameter	Specification	Notes
Connector voiding RBR/ H	No voiding required Voiding required	**HBR2:** Standard DP Connector: Voiding requirement is stack-up dependent. For typical stack-ups, voiding on the layer under the connector pad is required to be 5.7mil larger than the connector pad. 
Via Structure	Y-pattern is recommended. keep symmetry"	Xtalk suppression is the best by Y-pattern. Also it can reduce the limit of pair-pair distance. 
GND via	- Place GND via as symmetrically as possible to the data pair vias - Up to 4 signal vias (2 diff pairs) can share a single GND return via"	GND via is used to maintain return path, while its Xtalk suppression is limited
Serpentine		
Spacing between each turn	Microstrip >= 4x dielectric height Stripline >= 3x dielectric height"	
Bend angle	No 90deg bends; >=135deg (a)	
Dimension	A >= 4x trace width	
	Length of B, C >= 1.5x trace width	
	Jog > 3x trace width	
	S1 must be taken care in order to consider Xtalk to adjacent pair	
Keep critical eDP related traces including differential clock/data traces & **RSET** trace away from other signal traces or unrelated power traces/areas or power supply components		

Table 27. eDP Signal Connections

Jetson TX1 Pin Name	Type	Termination	Description
DP0_TX[3:0]+/–	O	Series 0.1uF capacitors on all lines	**eDP/DP Differential CLK/Data Lanes:** Connect to matching pins on display connector.
DP0_AUX+/–	I/OD	Series 0.1uF capacitors	**eDP/DP: Auxiliary Channels**: Connect to **AUX_CH**+/– on display connector.
DP0_HPD	I		**eDP/DP: Hot Plug Detect**: Connect to **HPD** pin on display connector.

7.3 HDMI / DP

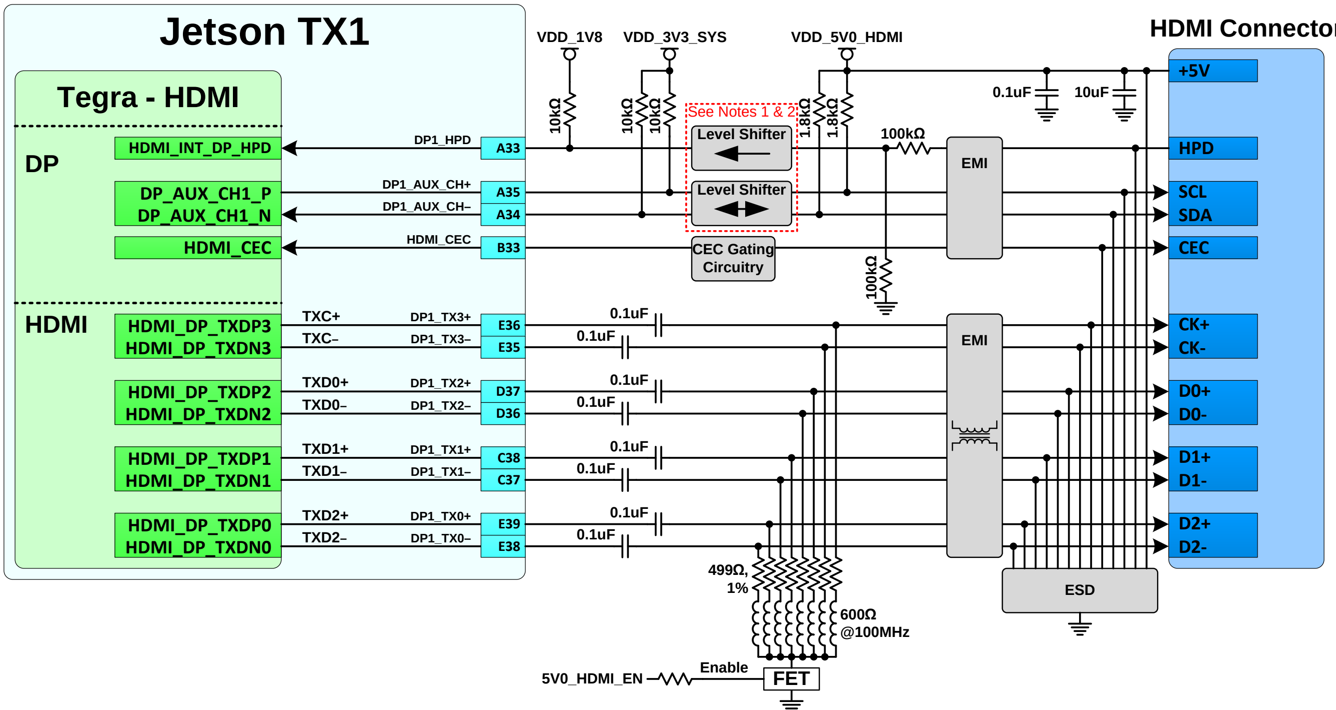
A standard DP 1.2a or HDMI V2.0 interface is supported. These share the same set of interface pins, so either Display Port or HDMI can be supported natively. Dual-Mode DisplayPort(DP++) can be supported, in which the DisplayPort connector logically outputs TMDS signaling to a DP-to-HDMI dongle.

Table 28. DP/HDMI Pin Mapping

Jetson TX1 Pin Name	Pin #s	HDMI	DP
DP1_TX0+ **DP1_TX0–**	**E39** **E38**	**TX2+** **TX2–**	**TX0+** **TX0–**
DP1_TX1+ **DP1_TX1–**	**C38** **C37**	**TX1+** **TX1–**	**TX1+** **TX1–**
DP1_TX2+ **DP1_TX2–**	**D37** **D36**	**TX0+** **TX0–**	**TX2+** **TX2–**
DP1_TX3+ **DP1_TX3–**	**E36** **E35**	**TXC+** **TXC –**	**TX3+** **TX3–**

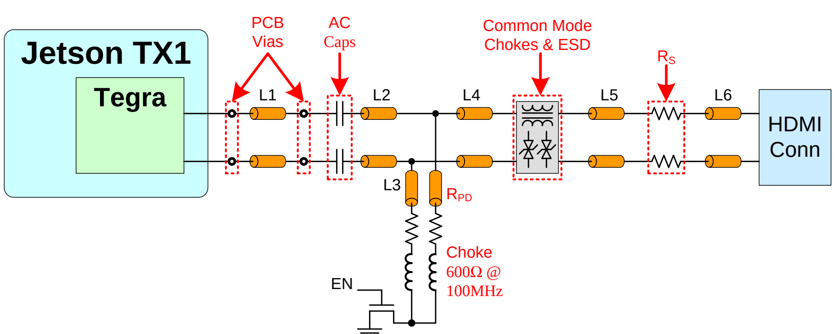
7.3.1 HDMI

Figure 16: HDMI Connection Example



Note: 1. Level shifters required on DDC/HPD. Tegra pads are not 5V tolerant & cannot directly meet HDMI V_{IL}/V_{IH} requirements.
2. HPD level shifter can be non-inverting or inverting.
3. If EMI/ESD devices are necessary, they must be suitable for the frequencies supported by the design.

Figure 17: HDMI Clk/Data Topology



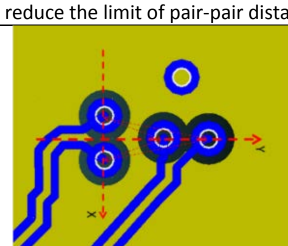
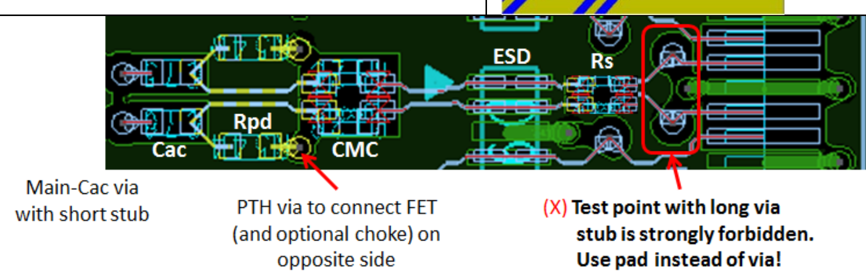
Note: 6Ω, 1% R_S series resistor should be included if differential trace impedance can only hit 95Ω instead of 100Ω target.

Table 29. HDMI Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Max Frequency / UI		5.94 / 168	Gbps / ps	Per lane – not total link bandwidth
Topology		Point to point		Unidirectional, Differential
Termination	At Receiver	100	Ω	Differential To 3.3V at receiver
	On-board	500		To GND near connector
Reference plane		GND		
Trace Impedance	Differential pair	100	Ω	±15%. Differential impedance target is 100Ω. If only 95Ω is achievable, see "Additional HDMI Guidelines" table for RS
	Single Ended	45		

Parameter	Requirement	Units	Notes
			usage guidelines.
trace loss characteristic:	< 0.8 < 0.4	dB/in @ 3GHz dB/in@ 1.5GHz"	the following max length is derived based on this characteristic. The length constraint must be re-defined if the loss characteristic is changed
Max Total Delay (L1+L2+L4+L5+L6 – d HDMI 2.0/1.4b) Stripline Microstrip (w/5x dielectric height spacing) Microstrip (w/7x dielectric height spacing)	 63.5 (1137.5) 50.8 (750) 63.5 (900ps)	 mm/in (ps)	Stripline is preferred. 175ps/inch delay for stripline & 150ps/inch delay for microstrip used for delay calculations.
Pair-to-pair spacing Stripline Microstrip (before 1.4b) Microstrip (1.4b & 2.0)	3x 4x 5x to 7x	dielectric	
Max Intra-Pair (within pair) Skew	0.15 (1)	mm (ps)	Do not perform length matching within breakout region. Do trace length matching before hitting discontinuity (i.e. matching to <1ps before the vias or any discontinuity to minimize common mode conversion.) (.
Max Inter-Pair (pair to pair) Skew	150	ps	
GND transition Via	< 1x	diff pair pitch	For signals switching reference layers, add symmetrical ground stitching Via near signal Vias. GND Via distance should be < 1X diff pair Via pitch
Max signal transition Vias PTH vias HDI (micro) vias	2 Not limited		 If total channel loss meets IL spec
Max Via stub length	0.4	mm	
Max distance from R_{PD} to HDMI connector (L4+L5+L6)	12.7	mm	
Max distance from R_{PD} to main trace (L3)	1	mm	
Max distance from AC_{CAP} to R_{PD} stubbing point (L2)	0	mm	

Table 30. Additional HDMI Guidelines

Parameter	Specification	Notes
Via Structure	Y-pattern is recommended. keep symmetry"	Xtalk suppression is the best by Y-pattern. Also it can reduce the limit of pair-pair distance.
	The impedance dip ≥ 97Ω @200ps ≥ 92Ω @35ps Recommended via dimension for impedance control: - drill/pad = 200um/400um - antipad > 840um - via pitch >= 880um"	
Layout Example		
AC Cap		
Value	0.1uf	
Location	Must be placed before pull-down resistor	Distance between the AC cap and the HDMI connector basically is not restricted.
Placement layer For Standard PCB w/PTH via For HDI PCB	 Place AC cap on bottom if main route above core Place AC cap on top if main route below core No restriction	
Void	GND (or PWR) void under/above cap is preferred	
R_{PD} (Pull-down resistor), Choke & FET		
Value	499Ω, 1%	
Location	- Must be placed after AC cap	

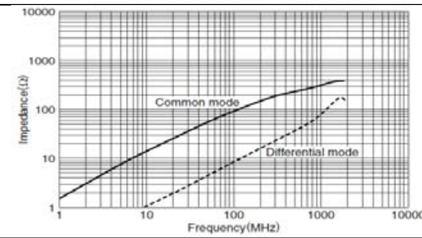
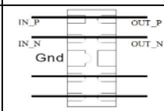
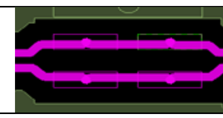
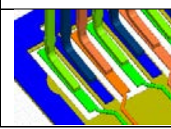
Parameter	Specification	Notes
	- Distance to the main trace, L3 <= 1mm - Distance to the HDMI connector : < 0.5"""	
Placement layer	- On same layer as AC cap - FET & optional choke can be placed on the opposite layer thru a PTH via	
Choke (between R_{PD} & FET)	- Can be choke or trace - Choke: >600 Ω @100MHz or 1uH at DC~100MHz - Trace: max Rdc <= 20mW"	
Void	GND (or PWR) void under/above the cap is preferred	
CMC (Common-Mode Choke)	Stuffing option. Not recommended to be installed unless EMI issues are seen.	
common-mode impedance @ 100MHz	min = 65 Ω ; max = 90 Ω	
R_{DC}	≤0.3Ω	
Differential TDR Impedance	90Ω ±15% @ Tr=200ps (10%-90%)	
Sdd21 @ 2.5GHz	< 2.22dB	
Scc21 @ 2.5GHz	> 19.2dB	
Location	Within 8mm of any adjacent discontinuity (i.e. connector, via, or other added-on components)	
ESD		
Max junction capacitance (IO to GND)	0.35pF	e.g. ON-Semiconductor ESD8040
Footprint	The pad should be on the main trace instead of having a trace stub	 
Location	After R_{PD} & CMC, but before R_S	
Void	GND (or PWR) void under/above the device is preferred	
R_S		
Value	6Ω, ±10%	
Location	After all components – Just before HDMI connector	
Void	GND (or PWR) void under/above the device is preferred	
GND void under connector pins	Voiding the ground below the signal lanes 0.1448(5.7mil) larger than the pin itself	

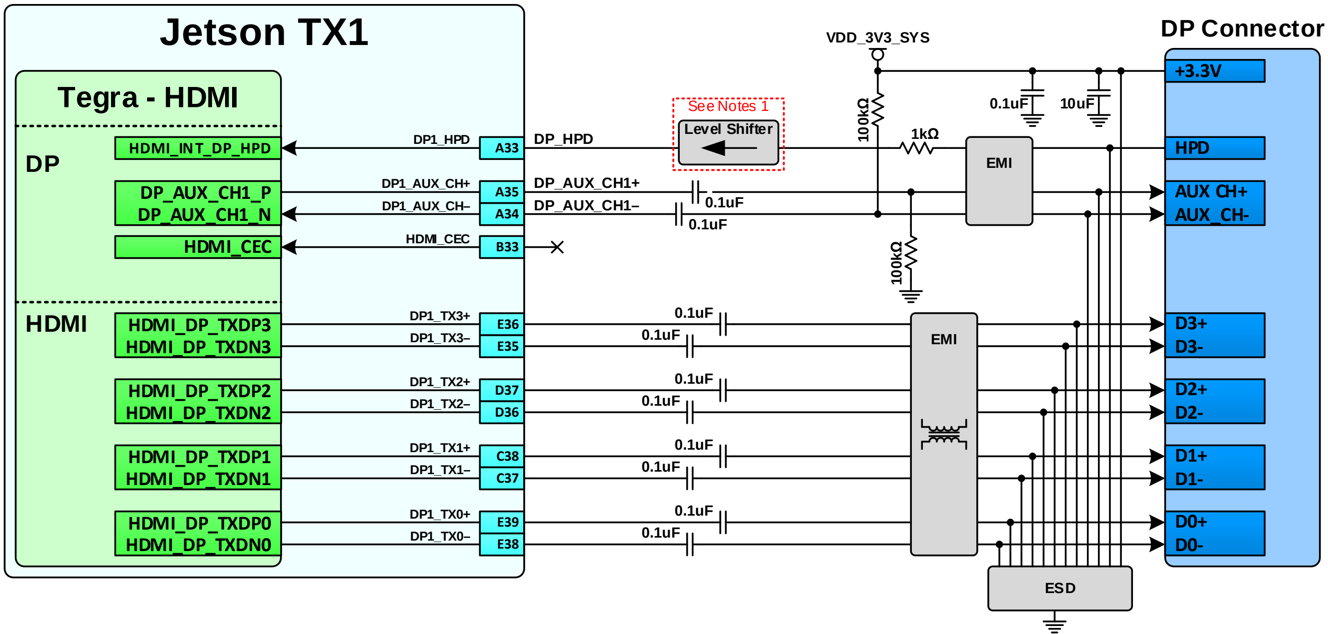
Table 31. HDMI Signal Connections

Jetson TX1 Pin Name	Type	Termination (see note on ESD)	Description
DP1_TX3+/–	DIFF OUT	0.1uF series ACCAP → 500 Ω RPD (controlled by FET) → 6 Ω RS (if required) → EMI/ESD (if required).	**HDMI Differential Clock:** Connect to **C–/C+** & pins on HDMI Connector
DP1_TX[2:0] +/–	DIFF OUT		**HDMI Differential Data:** Connect to **D[0:2]+/–** pins (See DP/HDMI Pin Mapping table)
DP1_HPD	I	Tegra to Connector: 10kΩ PU to 1.8V → level shifter → 100kΩ series resistor. 100kΩ to **GND** on connector side.	**HDMI Hot Plug Detect:** Connect to **HPD** pin on HDMI Connector
HDMI_CEC	I/OD	Gating circuitry, See connection figure or reference schematics for details.	**HDMI Consumer Electronics Control:** Connect to **CEC** on HDMI Connector through circuitry.
DP1_AUX_CH+/–	I/OD	From Tegra to Connector: 10kΩ PU to 3.3V → level shifter → 1.8kΩ PU to 5V → connector pin	**HDMI: DDC Interface – Clock and Data**: Connect **DP1_AUX_CH+** to **SCL** & **DP1_AUX_CH–** to **SDA** on HDMI Connector
HDMI 5V Supply	P	Adequate decoupling (0.1uF & 10uF recommended) on supply near connector.	**HDMI 5V supply to connector:** Connect to **+5V** on HDMI Connector.

Note: Any ESD and/or EMI solutions must support targeted modes (frequencies).

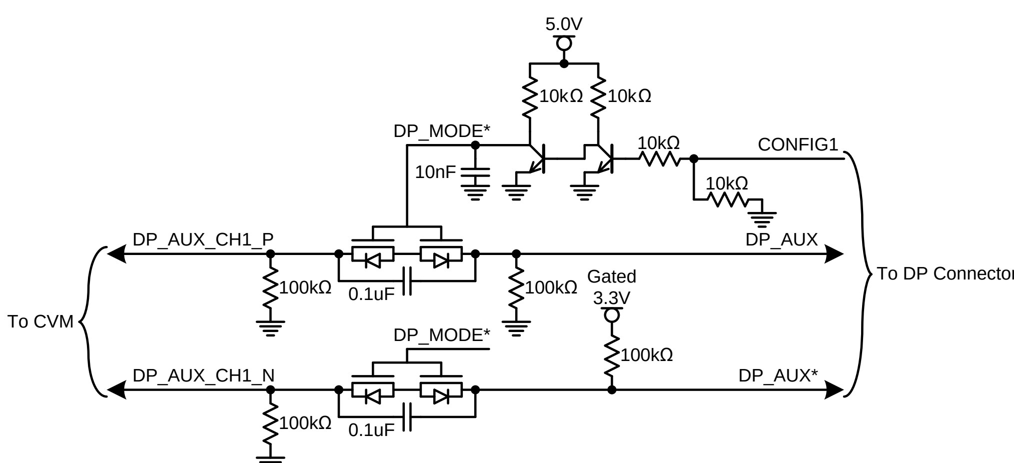
7.3.2 DP

Figure 18: DP Connection Example



Note:
1. Level shifter required on DP1_HPD to avoid the pin from being driven when Tegra is off. The level shifter must be non-inverting (preserve the polarity of the HPD signal from the display).
2. Any EMI/ESD included on the HDMI_DP pins must be suitable for the highest frequency modes supported (<1pf capacitive load recommended).

Figure 19: Optional Circuit for Dual-Mode (DP/HDMI) Support



DP Interface Signal Routing Requirements

See eDP Signal Routing Requirements.

Table 32. DP Signal Connections

Jetson TX1 Pin Name	Type	Termination (see note on ESD)	Description
DP[1:0]_TX[3:0]+/–	O	Series 0.1uF capacitors. EMI/ESD external (if required)	**DP Differential Lanes:** Connect to **D[3:0]+/–**
DP[1:0]_HDP	I	Non-inverting level-shifter → 1kΩ series resistor → EMI/ESD (if required).	**DP Interrupt (Hot Plug Detect):** Connect to **HPD** pin on DP Connector w/termination described.
DP[1:0]_AUX_CH+/–	I/OD	From Tegra-Connector: 100KΩ PD on **+/–** near Tegra, series 0.1uF caps, then 100KΩ PD on **AUX+** & 100KΩ PU to 3.3V on **AUX–** → EMI/ESD (if required).	**DP: Auxiliary Channels**: Connect to **AUX_CH+/–** on DP connector
DP 3.3V Supply	P	Adequate decoupling (0.1uF & 10uF recommended) on supply near connector.	**DP supply to connector:** Connect 3.3V supply pin on DP connector to **VDD_3V3_SYS**.

Note: Any ESD and/or EMI solutions must support targeted modes (frequencies).

8.0 MIPI CSI (VIDEO INPUT)

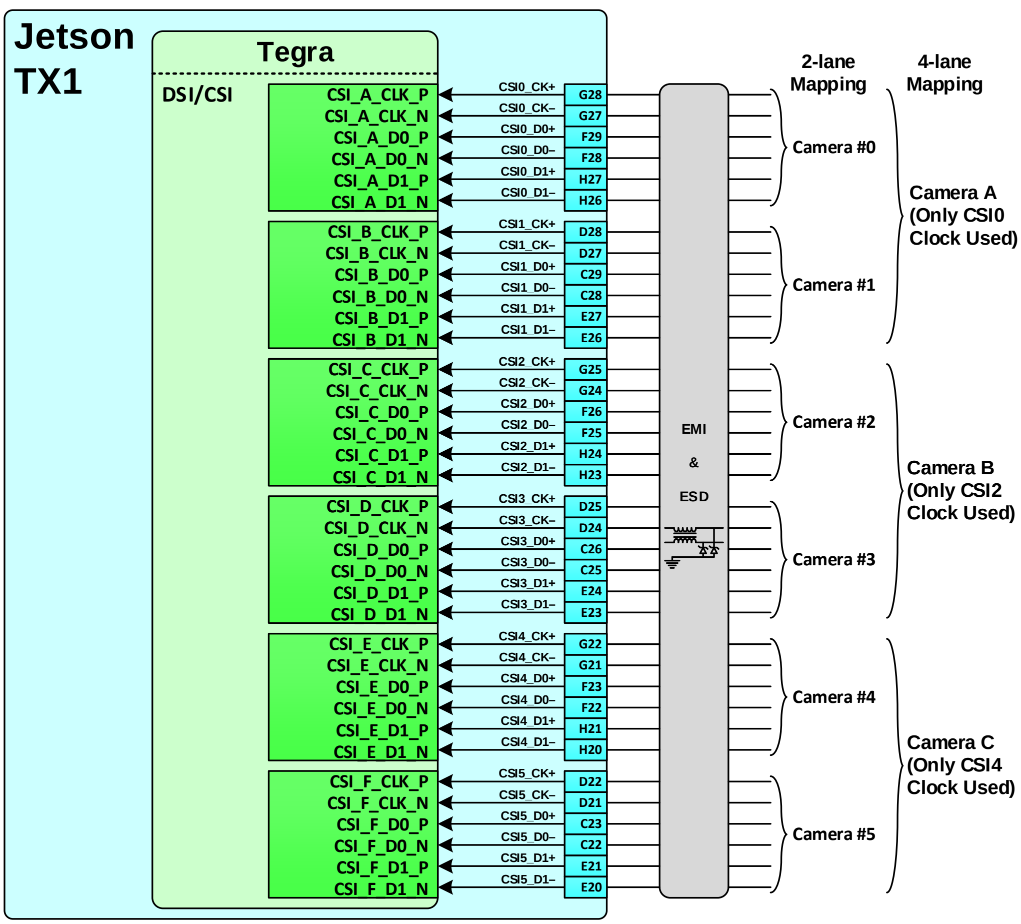
Tegra supports three MIPI CSI x4 bricks, allowing a variety of device types and combinations to be supported. Up to two quad lane stereo cameras or 6 dual lane camera streams are available. Each data channel has peak bandwidth of up to 1.5Gbps.

Table 33. CSI Configurations

Cameras	CSI_A CLK/Data[1:0]	CSI_B CLK	CSI_B Data[1:0]	CSI_C CLK/Data[1:0]	CSI_D CLK	CSI_D Data[1:0]	CSI_E CLK/Data[1:0]	CSI_F CLK	CSI_F Data[1:0]
2-Lanes Each									
1 of 6 Cameras	√								
2 of 6 Cameras		√	√						
3 of 6 Cameras				√					
4 of 6 Cameras					√	√			
5 of 6 Cameras							√		
6 of 6 Cameras								√	√
4-Lanes Each									
1 of 3 Cameras	√		√						
2 of 3 Cameras				√		√			
3 of 3 Cameras							√		√

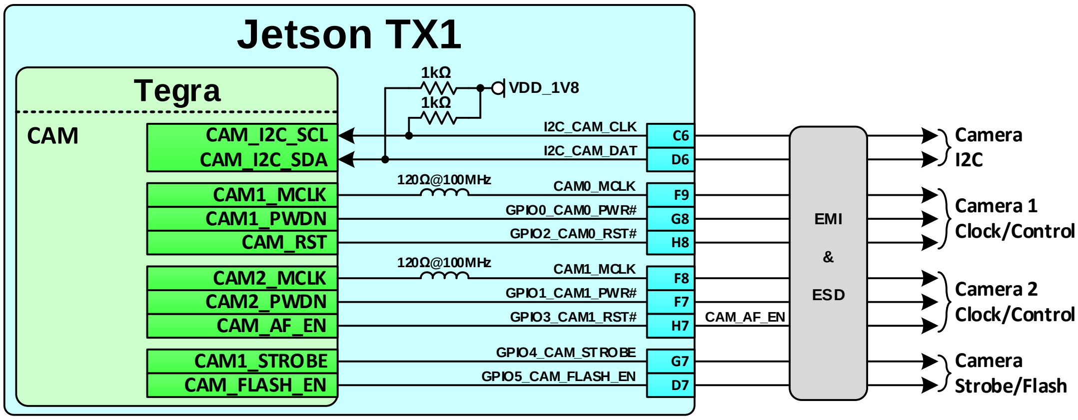
Note:
- Each 2-lane options shown above can also be used for one single lane camera as well
- Combinations of 1, 2 & 4-lane cameras are supported, as long as any 4-lane cameras come from one of the configurations shown above

Figure 20: Camera CSI Connections



Note: Any EMI/ESD devices must be tuned to minimize impact to signal quality and meet the timing & Vil/Vih requirements at the receiver & maintain signal quality and meet requirements for the frequencies supported by the design.

Figure 21: Camera Control Connections



Note:
1. If Tegra is providing flash control (as shown above), **GPIO5_CAM_FLASH_EN** & **GPIO4_CAM_STROBE** must be used.
2. Any EMI/ESD devices must be tuned to minimize impact to signal quality and meet the timing & Vil/Vih requirements at the receiver & maintain signal quality and meet requirements for the frequencies supported by the design.

CSI Design Guidelines

CSI & DSI use the MIPI D-PHY for the physical interface. The routing & connection requirements are found in the DSI section.

Table 34. MIPI CSI Signal Connections

Jetson TX1 Pin Name	Type	Termination	Description
CSI[5:0]_CLK+/–	I	See note	**CSI Differential Clocks:** Connect to clock pins of camera. See the CSI Configurations table for details
CSI[5:0]_D[1:0]+/–	I/O	See note	**CSI Differential Data Lanes:** Connect to data pins of camera. See the CSI Configurations table for details

Note: Depending on the mechanical design of the platform and camera modules, ESD protection may be necessary. In addition, EMI control may be needed. Both are shown in the Camera Connection Example diagram. Any EMI/ESD solution must be compatible with the frequency required by the design.

Table 35. Miscellaneous Camera Connections

Jetson TX1 Pin Name	Type	Termination	Description
I2C_CAM_CLK **I2C_CAM_DAT**	O I/O	1kΩ Pull-ups **VDD_1V8** (on Jetson TX1). See note related to EMI/ESD under MIPI CSI Signal Connections table.	**Camera I2C Interface:** Connect to I2C **SCL & SDA** pins of imager
CAM[1:0]_MCLK	O	120Ω Bead in series (on Jetson TX1) See note related to EMI/ESD under MIPI CSI Signal Connections table.	**Camera Master Clocks:** Connect to Camera reference clock inputs.
GPIO1_CAM1_PWR# **GPIO0_CAM0_PWR#**	I/O	See note related to ESD under MIPI CSI Signal Connections table.	**Camera Power Control signals (or GPIOs [1:0])**: Connect to power down pins on camera(s).
GPIO4_CAM_STROBE			**Camera Strobe Enable (or GPIO 4):** Connect to camera strobe circuit unless strobe control comes from camera module.
GPIO5_CAM_FLASH_EN	O		**Camera Flash Enable:** Connect to enable of flash circuit
GPIO3_CAM1_RST# **GPIO2_CAM0_RST#**	O		**Camera Resets (or GPIO [3:2]):** Connect to reset pin on any cameras with this function. If Auto Focus Enable is required, connect **GPIO3_CAM1_RST#** to **AF_EN** pin on camera module & use **GPIO2_CAM0_RST#** as common reset line.

9.0 SDIO/SDCARD/EMMC

Jetson TX1 has four SD/MMC interfaces. Two are used on the Jetson TX1 for eMMC & Wi-Fi/BT. The other two are brought to the connector pins for SD Card & SDIO use.

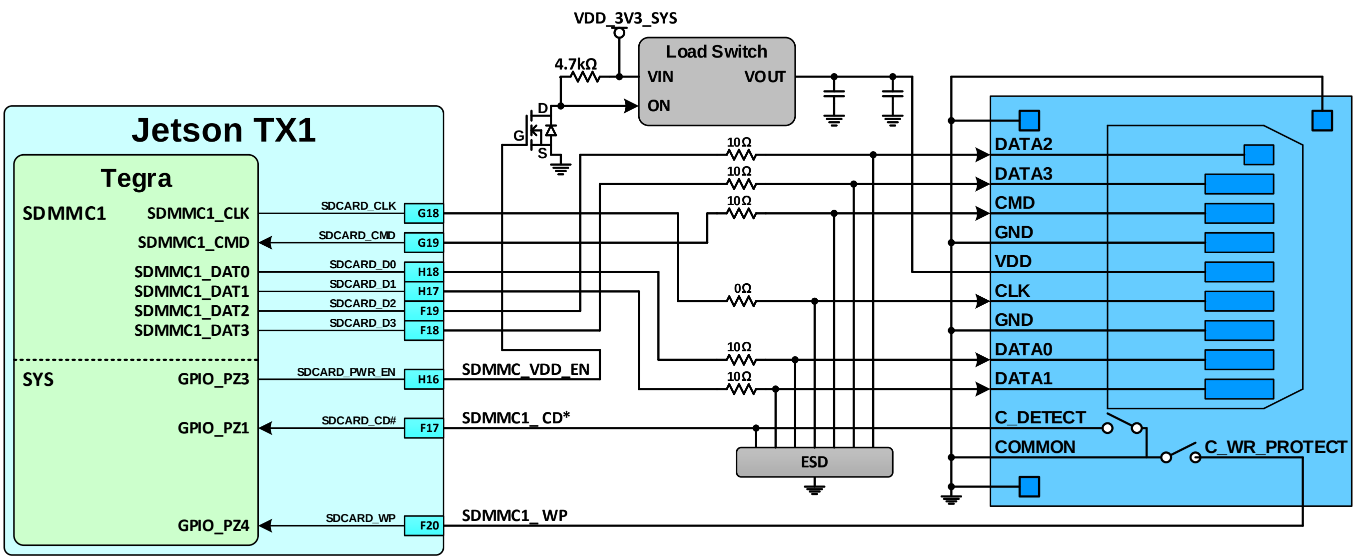
Table 36. SDIO / SD Card / eMMC Interface Mapping

Jetson TX1 Pins	Tegra Interface	Width	Usage
SDCARD	SDMMC1	4-bit	SD (Primary SD Card)
N/A	SDMMC2	4-bit	Used on Jetson TX1 for Primary Wi-Fi
SDIO	SDMMC3	4-bit	SDIO (2nd Wi-Fi, etc.)
N/A	SDMMC4	8-bit	Used on Jetson TX1 for eMMC

9.1 SD Card

The Figure shows a standard SD socket. Internal pull-up resistors are used for SDCARD Data/CMD lines, so external pull-ups are not required.

Figure 22. Tegra SD Card Socket Connection Example



Notes:
1. If EMI and/or ESD devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing & Vil/Vih requirements at the receiver & maintain signal quality and meet requirements for the frequencies supported by the design.
2. Supply (load switch, etc.) used to provide power to the SD Card must be current limited if the supply is shorted to GND.

Table 37. SDIO/SDCARD Interface Signal Routing Requirements

Parameter			Requirement	Units	Notes
Max Frequency	3.3V Signaling	DS	25 (12.5)	MHz (MB/s)	See Note 1
		HS	50 (25)		
	1.8V Signaling	SDR12	25 (12.5)		
		SDR25	50 (25)		
		SDR50	100 (50)		
		SDR104	208 (104)		
		DDR50	50 (50)		
Topology			Point to point		
Reference plane			**GND** or **PWR**		See Note 2
Trace Impedance			50	Ω	±15%. 45Ω optional depending on stack-up
Max Via Count		PTH	**4**		Independent of stack-up layers
		HDI	**10**		Depends on stack-up layers
Via proximity (Signal to reference)			< 3.8 (24)	mm (ps)	Up to 4 signal Vias can share 1 **GND** return Via

Trace spacing	Microstrip / Stripline	4x / 3x	dielectric	
Trace length SDR50 / SDR25 / SDR12 / HS / DS SDR104 / DDR50	 Min Max Min Max	 **16 (100)** **139 (876)** **16 (100)** **83 (521)**	mm (ps)	
Max Trace Delay Skew in/between **CLK** & **CMD/DAT**	SDR50 / SDR25 / SDR12 / HS / DS SDR104 / DDR50	14 (87.5) 2 (12.5)	**Mm (ps)**	**See Note 3**
Keep CLK, CMD & DATA traces away from other signal traces or unrelated power traces/areas or power supply components				

Note:
1. Actual frequencies may be lower due to clock source/divider limitations.
2. If PWR, 0.01uF decoupling cap required for return current
3. If routing to SD Card socket includes a flex or 2nd PCB, max trace & skew calculations must include PCB & flex routing.

Table 38. SD Card Loading vs Drive Type

General SD Card Compliance	Parameter	Value	Units	Notes
C_{CARD} (C_{DIE}+C_{PKG})	Min	5	pF	Spec best case value
	Max	10	pF	Spec worst case value
Drive Type	A	33	Ω	UHS50 Card = optional, UHS104 Card = mandatory
	B	50	Ω	UHS50 Card = mandatory, UHS104 Card = mandatory
	C	66	Ω	UHS50 Card = optional, UHS104 Card = mandatory
	D	100	Ω	UHS50 Card = optional, UHS104 Card = mandatory
F_{MAX} (CLK base frequency)	SDR104	208	MHz	Single data rate up to 104MB/sec
	DDR50	50	MHz	Double data rate up to 50MB/sec
	SDR50	100	MHz	Single data rate up to 50MB/sec
	SDR25	50	MHz	Single data rate up to 25MB/sec
	SDR12	25	MHz	Single data rate up to 12.5MB/sec
	HS	50	MHz	Single data rate up to 25MB/sec
	DS	25	MHz	Single data rate up to 12.5MB/sec
C_{LOAD} (C_{CARD}+C_{EQ}) (CLK freq = 208MHz)	Drive Type = A	21	pF	Total load capacitance supported
	Drive Type = B	15	pF	Total load capacitance supported
	Drive Type = C	11	pF	Total load capacitance supported
	Drive Type = D	22	pF	Possibly 22pF+ depending on host system
C_{LOAD} (C_{CARD}+C_{EQ}) (CLK freq = 100/50/25MHz)	Drive Type = A	43	pF	Total load capacitance supported
	Drive Type = B	30	pF	Total load capacitance supported
	Drive Type = C	23	pF	Total load capacitance supported
	Drive Type = D	22	pF	Possibly 22pF+ depending on host system

Table 39. SDIO/SDCARD Signal Connections

Function Signal Name	Type	Termination	Description
SDIO_CK/SDCARD_CLK	O	0Ω series resistor for SD_CARD_CLK (for possible tuning). See note for EMI/ESD	**SDIO/SDMMC Clock:** Connect to **CLK** pin of device or socket
SDIO_CMD/SDCARD_CMD	I/O	10Ω series resistor for SD_CARD_CMD/D[3:0] See note for EMI/ESD	**SDIO/SDMMC Command:** Connect to **CMD** pin of device/socket
SDIO_D[3:0]/SDCARD_D[3:0]	I/O		**SDIO/SDMMC Data:** Connect to **Data** pins of device or socket
SDCARD_CD#	I		**SDIO Card Detect:** Connect to **CD/C_DETECT** pin on socket if required.
SDCARD_WP	I		**SDIO Write Protect:** Connect to **WP/WR_PROTECT** pin on socket if required.
SDIO_RST#	O		**SDIO Reset:** Connect to reset line on SDIO peripheral/connector.
SDCARD_PWR_EN	O		**SDIO Supply/Load Switch Enable:** Connect to enable of supply/load switch supplying **VDD** on SD Card socket.

Note: EMI/ESD may be required for SDIO when used as the SD Card socket interface. Any EMI/ESD device used must be able to meet signal timing/quality requirements. The Carrier Board implements 10Ω series resistors on the data lines and a 0Ω series resistors on the clock line (for possible tuning if required).

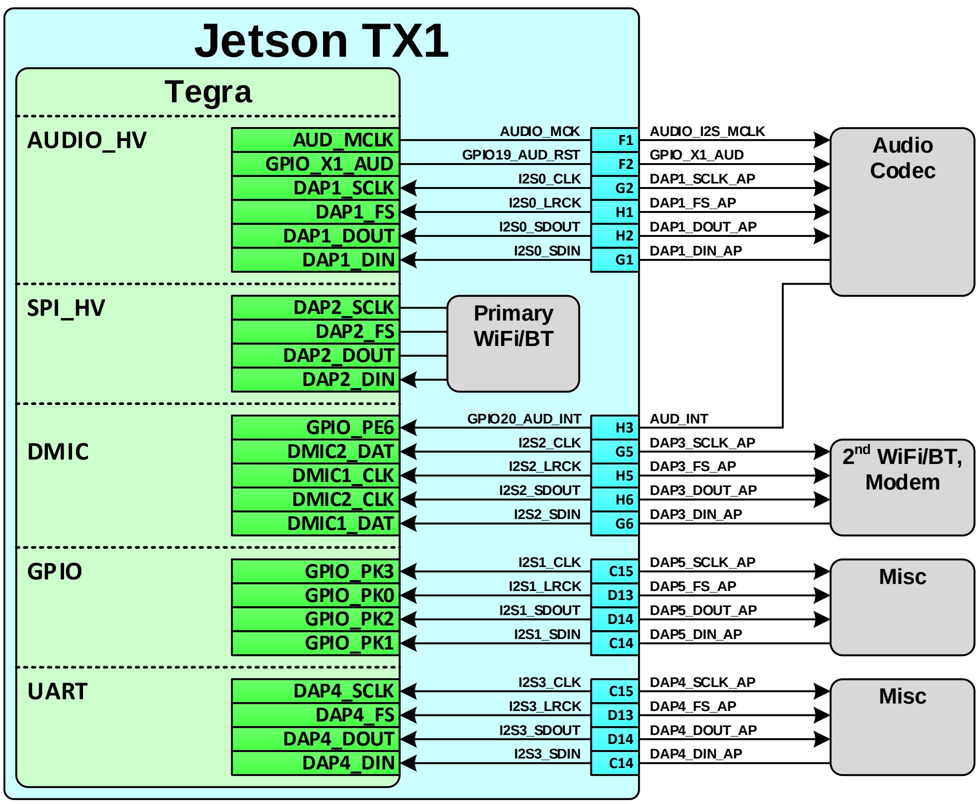
10.0 AUDIO

Tegra supports Multiple PCM/I2S audio interfaces & includes a flexible audio-port switching architecture. The following assignments should be used for the I2Sx interfaces:

Table 40. I2S Interface Mapping

Jetson TX1 Pins (Tegra X1 Functions)	I/O Block	Typical Usage
I2S0 (I2S1)	AUDIO_HV	Available (Codec)
I2S1 (I2S5B)	GPIO	Available (Misc. Expansion)
I2S2 (I2S3)	DMIC	Available (Wi-Fi / BT, Modem)
I2S3 (I2S4B)	UART	Available (Misc.)
N/A (I2S2)	SPI_HV	Used on Jetson TX1 for Wi-Fi / BT

Figure 23. Audio Device Connection Example



Note: The I2S interfaces can be used in either Master or Slave mode.

I2S Design Guidelines

Table 41. I2S Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Configuration / Device Organization		1	load	
Max Loading		8	pF	
Reference plane		**GND**		
Breakout Region Impedance		Min width/spacing		
Trace Impedance		50	Ω	±20%
Via proximity (Signal to reference)		< 3.8 (24)	mm (ps)	See Note 1
Trace spacing	Microstrip or Stripline	2x	dielectric	
Max Trace Delay		3600 (~22)	ps (in)	See Note 2
Max Trace Delay Skew between **SCLK** & **SDATA_OUT/IN**		250 (~1.6”)	ps (in)	See Note 2

Note: Up to 4 signal Vias can share a single GND return Via

Table 42. Audio Signal Connections

Jetson TX1 Pin Name	Type	Termination	Description
I2S[3:0]-SCLK	I/O		**DAP Serial Clock:** Connect to I2S/PCM **CLK** pin of audio device.
I2S[3:0]-LRCK	I/O		**DAP Field Select (Word Select for I2S):** Connect to word/field select pin of audio device.
I2S[3:0]-SDATA_OUT	I/O		**DAP Data Output:** Connect to Data Input pin of audio device.
I2S[3:0]-SDATA_IN	I		**DAP Data Input:** Connect to Data Output pin of audio device.
AUD_MCLK	O		**Audio Codec Master Clock:** Connect to clock pin of Audio Codec.
GPIO19_AUD_RST	O		**Audio Reset:** Connect to reset pin of Audio Codec.
GPIO20_AUD_INT	I		**Audio Interrupt:** Connect to interrupt pin of Audio Codec.

11.0 WI-FI / BT (INTEGRATED)

Jetson TX1 integrates a Broadcom BCM4354XKUBG Wi-Fi / BT solution. This is a IEEE 802.11 ac 2x2. Two Dual-band antenna connectors are located on the module. The requirements are in the Antenna Requirements table below.

Figure 24. Integrated Wi-Fi / BT

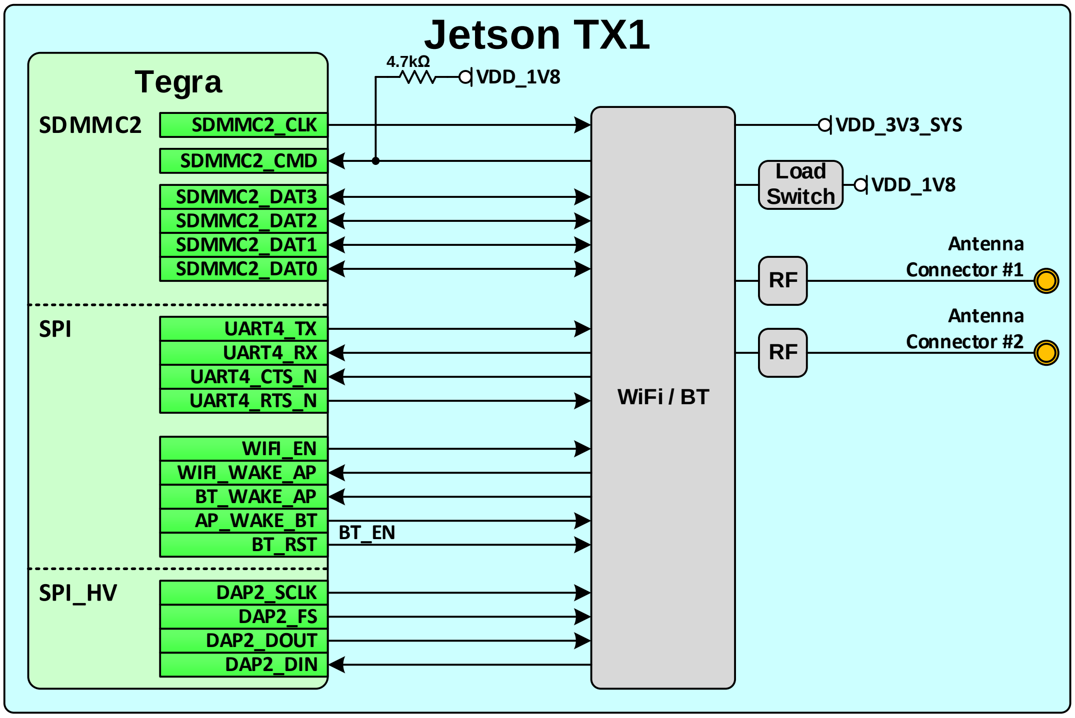


Table 43. Antenna Requirements

Parameter	Requirement	Units	Notes
Type	Dual-Band (x2)		
Frequency Band(s)	2.4 & 5.0	GHz	
Impedance	50	Ω	
Mating Connector	Female I-PEX		2x Male I-PEX on Jetson TX1 module

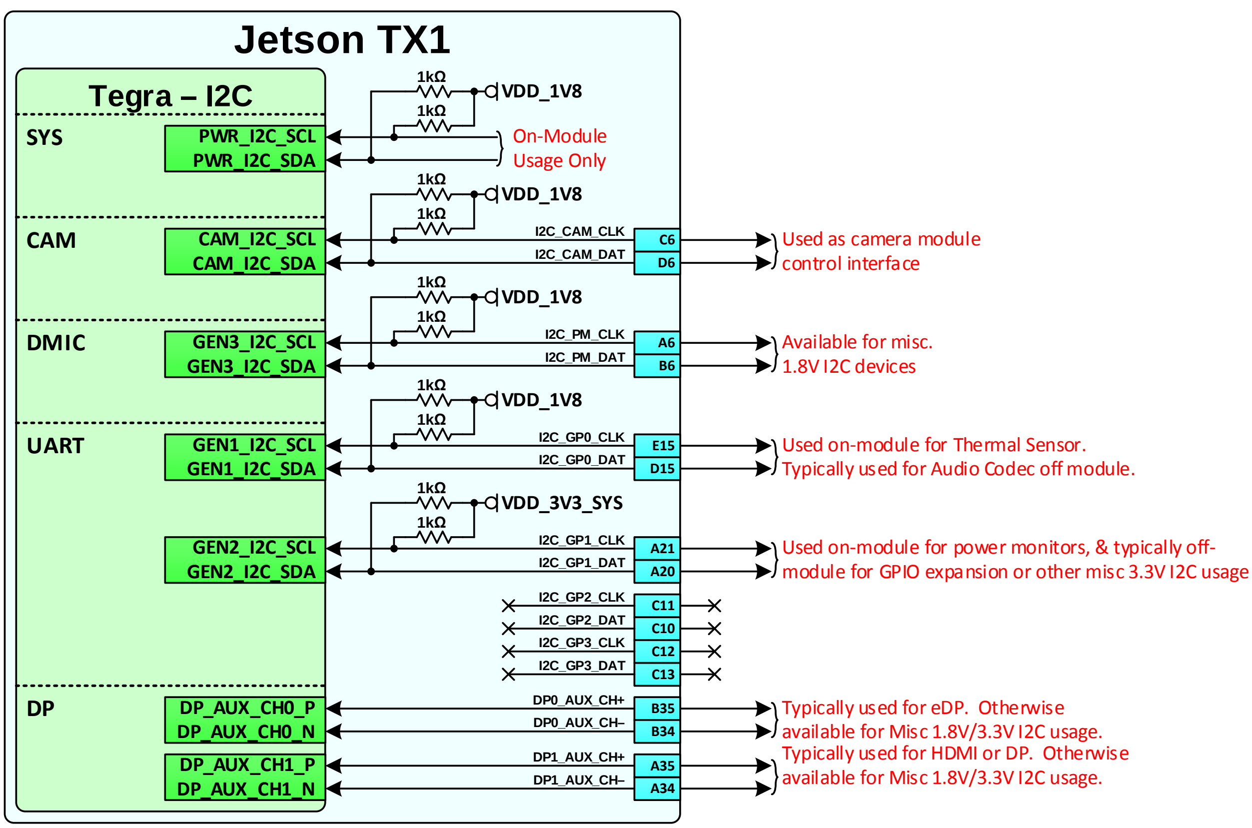
12.0 MISCELLANEOUS INTERFACES

12.1 I2C

Tegra has seven I2C controllers, which are shown in the table below. The assignments in the table should be used for the I2C interfaces:

I2C Controller	Jetson TX1 Pins Names	Usage on Jetson TX1	Typical usage on carrier board	On-Jetson TX1 Pull-up/voltage
I2C1	I2C_GP0_CLK/DAT	Thermal Sensor control	Audio Codec, other general I2C bus usage. Only 1.8V devices supported without level shifter.	1KΩ on Jetson TX1 to 1.8V
I2C2	I2C_GP1_ CLK/DAT	Power monitors	General I2C bus usage. Only 3.3V devices supported without level shifter.	1KΩ on Jetson TX1 to 3.3V
I2C3	I2C_PM_ CLK/DAT		General I2C bus usage. Only 1.8V devices supported without level shifter.	1KΩ on Jetson TX1 to 1.8V
I2C_VI	I2C_CAM_CLK/DAT		Cameras & camera related functions (AF, etc.). Only 1.8V devices supported without level shifter.	1KΩ on Jetson TX1 to 1.8V
I2C6	DP0_AUX_CH_P/N		eDP or other I2C bus usage. 1.8V or 3.3V devices can be supported.	None on Jetson TX1. IF supports pull-up to 1.8V or 3.3V
DDC	DP1_AUX_CH_P/N		HDMI / DP or other I2C bus usage. 1.8V or 3.3V devices can be supported.	None on Jetson TX1. IF supports pull-up to 1.8V or 3.3V
I2CPMU	na	Power control	On-Jetson TX1 use only	1KΩ on Jetson TX1 to 1.8V

Figure 25. I2C Connections



I2C Design Guidelines

Care must be taken to ensure I2C peripherals on same I2C bus connected to Tegra do not have duplicate addresses. Addresses can be in two forms: 7-bit, with the Read/Write bit removed or 8-bit including the Read/Write bit. Be sure to compare I2C device addresses using the same form (all 7-bit or all 8-bit format).

Table 44. I2C Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Max Frequency	Standard-mode / Fm / Fm+ Hs Mode	100 / 400 / 1000 3.4	kHz MHz	See Note 1 & 2
Topology		Single ended, bi-directional, multiple masters/slaves		
Max Loading	Standard-mode / Fm / Fm+ Hs Mode	400 100	pF	Total of all loads
Reference plane		**GND** or **PWR**		
Trace Impedance		50 – 60	Ω	±15%
Trace Spacing		1x	dielectric	
Max Trace Delay	Standard Mode Fm, Fm+ & Hs Modes	3400 (~20) 1700 (~10)	ps (in)	

Note: 1. Fm = Fast-mode, Fm+ = Fast-mode Plus, Hs = High-speed.
2. I2C_GP1 & DP1_AUX (when used for HDMI DDC or I2C) only support up to Fm+ speed.
3. Avoid routing I2C signals near noisy traces, supplies or components such as a switching power regulator.
4. No requirement for decoupling caps for **PWR** reference

Table 45. I2C Signal Connections

Jetson TX1 Pin Name	Type	Termination	Description
I2C_GP0_CLK/DAT	I/OD	1kΩ pull-ups to **VDD_1V8** on Jetson TX1	**General I2C 0 Clock & Data.** Connect to **CLK & Data** pins of any 1.8V devices
I2C_GP1_CLK/DAT	I/OD	1kΩ pull-ups to **VDD_3V3_SYS** on Jetson TX1	**General I2C 1 Clock & Data.** Connect to **CLK & Data** pins of 3.3V devices.
I2C_PM_CLK/DAT	I/OD	1kΩ pull-ups to **VDD_1V8** on Jetson TX1	**Power Measurement I2C Clock & Data.** Connect to **CLK & Data** pins of any 1.8V devices
I2C_CAM_CLK/DAT	I/OD	1kΩ pull-ups to **VDD_1V8** on Jetson TX1	**Camera I2C Clock & Data.** Connect to **CLK & Data** pins of any 1.8V devices
DP0_AUX_CH+/–	I/OD	Include pads for 100kΩ pull-downs to **GND** near Jetson TX1 pins.	**AUX Channel for eDP interface.** Connect to **AUX_CH+/–**
DP1_AUX_CH+/–	I/OD	See HDMI/DP sections for correct termination	**DP_AUX Channel (DP) or DDC I2C 2 Clock & Data (HDMI).** Connect to **AUX_CH+/–** (DP) or **SCL/SDA** (HDMI)

Note: 1. If some devices require a different voltage level than others connected to the same I2C bus, level shifters are required.
2. For I2C interfaces that are pulled up to 1.8V, disable the OD (Open Drain) option for these pads. For I2C interfaces that are pulled up to 3.3V, enable the OD (Open Drain) option. The Open Drain option is selected in the Pinmux registers.

De-bounce

The tables below contain the allowable De-bounce settings for the various I2C Modes.

Table 46. De-bounce Settings (Fast Mode Plus, Fast Mode & Standard Mode)

I2C Mode	Clock Source	Source Clock Freq	I2C Source Divisor	Sm/Fm Divisor	De-bounce Value	I2C SCL Freq
Fm+	PLLP_OUT0	408MHz	5 (0x04)	10 (0x9)	0	1016KHz
					5:1	905.8KHz
					7:6	816KHz
Fm	PLLP_OUT0	408MHz	5 (0x4)	26 (0x19)	7:0	392KHz
Sm	PLLP_OUT0	408MHz	20 (0x13)	26 (0x19)	7:0	98KHz

Note: Sm = Standard Mode.

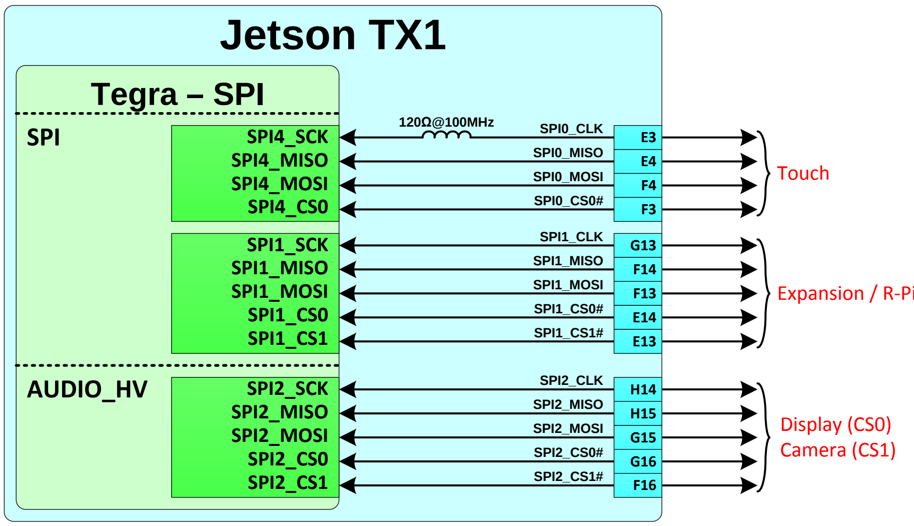
Table 47. Debounce Settings (High-Speed Mode)

Mode	Source	PLLP_OUT0	I2C Source Div	Hs Div	De-bounce	I2C Freq
Hs	PLLP_OUT0	408MHz	3 (0x2)	3 (0x2)	0	3.48MHz
					7:1	Not allowed

12.2 SPI

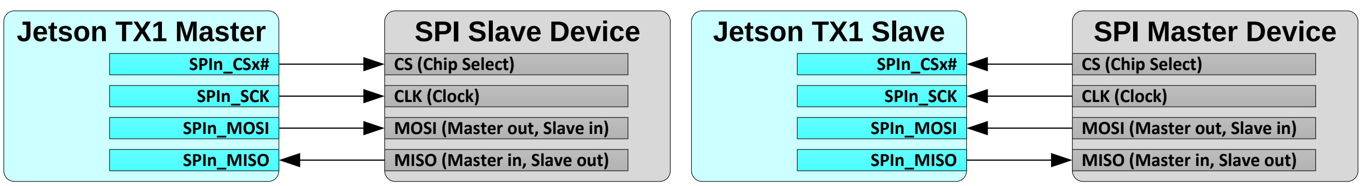
The Jetson TX1 brings out three of the Tegra SPI interfaces. See the Figure below.

Figure 26. SPI Connections



The figure below shows the basic connections used.

Figure 27. Basic SPI Master/Slave Connections



SPI Design Guidelines

Figure 28. SPI Topology

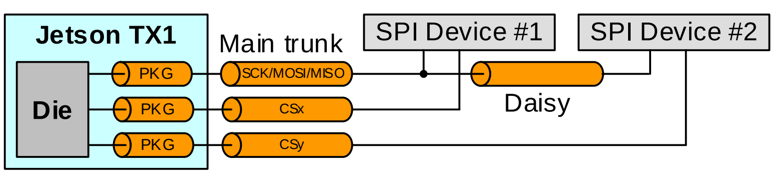


Table 48. SPI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency	65	MHz	
Configuration / Device Organization	4	load	
Max Loading (total of all loads)	15	pF	
Reference plane	**GND**		
Breakout Region Impedance	Minimum width & spacing		
Max PCB breakout delay	75	ps	
Trace Impedance	50 – 60	Ω	±15%
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 1
Trace spacing Microstrip / Stripline	4x / 3x	dielectric	
Max Trace Delay (PCB Main Trunk) Single load case Two load case	1760 (~11) 1280 (~8)	ps (in)	
Max Trace Delay (Daisy)	480 (~3)	ps (in)	
Max Trace Delay Skew between **MOSI** (**DOUT**), **MISO** (**DIN**) & **CS** to **SCK**	50	ps	At any point

Note: Up to 4 signal Vias can share a single GND return Via

Table 49. SPI Signal Connections

Jetson TX1 Pin Names	Type	Termination	Description
SPI[2:0]_CLK	I/O	**SPI0_CLK** has 120Ω Bead in series (on Jetson TX1).	**SPI Clock.:** Connect to Peripheral **CLK** pin(s)
SPI[2:0]_MOSI	I/O		**SPI Data Output:** Connect to Slave Peripheral **MOSI** pin(s)
SPI[2:0]_MISO	I/O		**SPI Data Input:** Connect to Slave Peripheral **MISO** pin(s)
SPI[2:1]_CS[1:0]# **SPI0_CS0#**	I/O		**SPI Chip Selects.:** Connect one **CS_N** pin per SPI IF to each Slave Peripheral **CS** pin on the interface

12.3 UART

The Jetson TX1 brings three UARTs out to the main connector. One of the UARTs is used for the Wi-Fi/BT on the Jetson TX1. See Figure below for typical assignments of the three available UARTs.

Figure 29. Jetson TX1 UART Connections

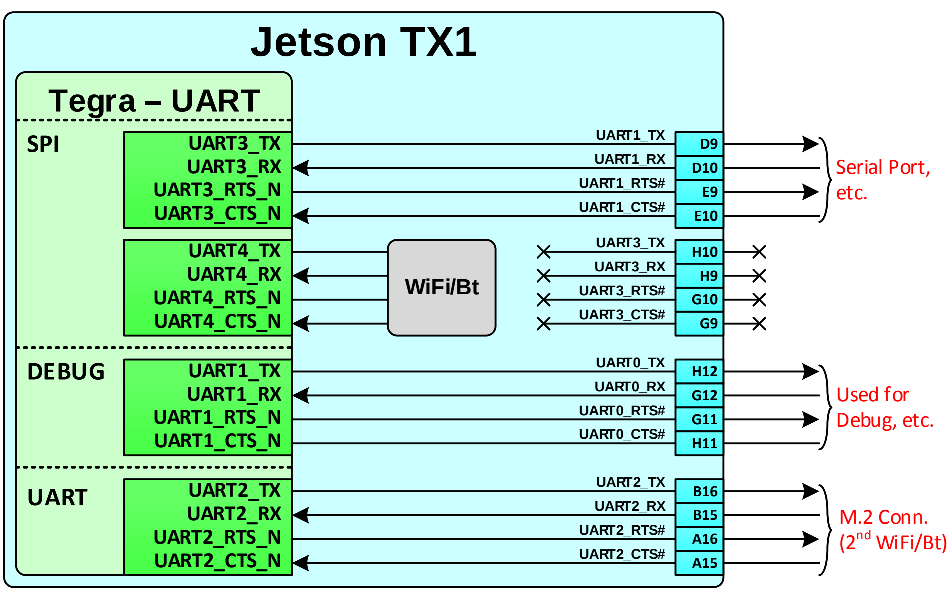
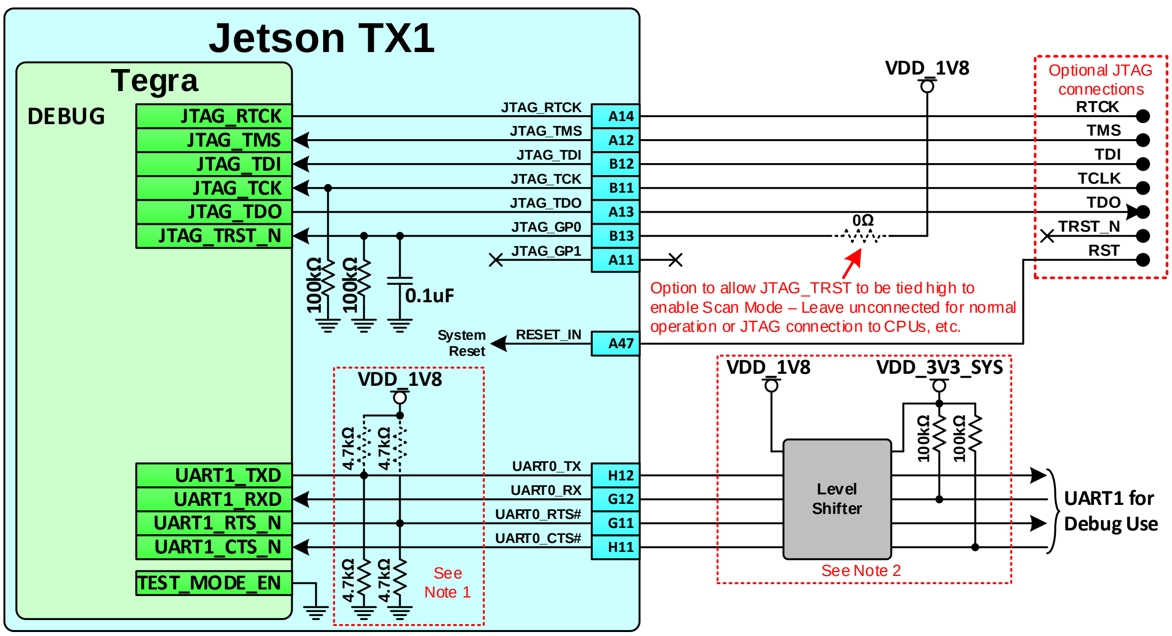


Table 50. UART Signal Connections

Ball Name	Type	Termination	Description
UART[2:0]_TX	O		**UART Transmit:** Connect to Peripheral **RXD** pin of device
UART[2:0]_RX	I		**UART Receive:** Connect to Peripheral **TXD** pin of device
UART[2:0]_CTS#	I		**UART Clear to Send:** Connect to Peripheral **RTS_N** pin of device
UART[2:0]_RTS#	O		**UART Request to Send:** Connect to Peripheral **CTS** pin of device

12.4 Debug & Test

Figure 30. Debug Connections



Note: 1. Pull-ups or Pull-downs are present on the UART TX & RTS lines for RAM Code strapping.
2. If level shifter is implemented, pull-ups are required the RX & CTS lines on the non-Jetson TX1 side of the level shifter. This is required to keep the inputs from floating and toggling when no device is connected to the debug UART.

12.4.1 JTAG

JTAG is not required, but may be useful for new design bring-up. Note that the Tegra **JTAG_TRST_N** pin (JTAG_GP0 on Jetson TX1 connector) is not used as a conventional JTAG reset line. Instead, this pin selects whether JTAG is to be used for communicating with the Tegra CPU complex, or for Test/Scan purposes. When **JTAG_TRST_N** is pulled low, the JTAG interface is enabled for access to the CPU complex. When high, it is in Test/Scan mode. In order to reset the JTAG block, a reset command is used rather than toggling the **JTAG_TRST_N** pin.

Table 51. JTAG Connections

Jetson TX1 Pin Name	Type	Termination	Description
JTAG_TMS	I		**JTAG Mode Select:** Connect to **TMS** pin of connector
JTAG_TCK	I	100kΩ to **GND** (on Jetson TX1)	**JTAG Clock:** Connect to **TCK** pin of connector
JTAG_TDO	O		**JTAG Data Out:** Connect to **TDO** pin of connector
JTAG_TDI	I		**JTAG Data In:** Connect to **TDI** pin of connector
JTAG_RTCLK	I		**JTAG Return Clock:** Connect to **RTCK** pin of connector
JTAG_GP0	I	100kΩ to **GND** & 0.1uF to **GND** (on Jetson TX1)	**JTAG General Purpose Output :** - Normal operation: Leave series resistor from **JTAG_GP0** not stuffed. - Boundary Scan test mode: Connect **JTAG_GP0** to **VDD_1V8** (install 0Ω resistor as shown).

12.4.2 Debug UART

Jetson TX1 provides UART0 for debug purposes. The connections are shown in the Figure 30 and described in the table below.

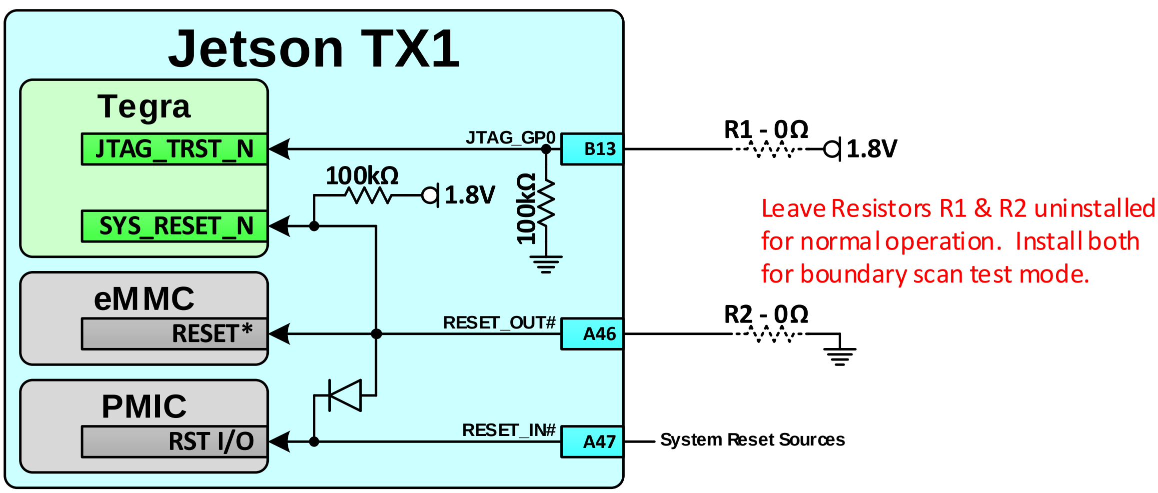
Table 52. Debug UART Connections

Jetson TX1 Pin Name	Type	Termination	Description
UART0_TXD	O	4.7kΩ to **GND** or VDD_1V8 on Jetson TX1 for RAM Code strapping	**UART #0 Transmit:** Connect to **RX** pin of serial device
UART0_RXD	I	If level shifter implemented, 100kΩ to supply on the non-Jetson TX1 side of the device.	**UART #0 Receive:** Connect to **TX** pin of serial device
UART0_RTS#	O	4.7kΩ to **GND** or VDD_1V8 on Jetson TX1 for RAM Code strapping	**UART #0 Request to Send:** Connect to **CTS** pin of serial device
UART0_CTS#	I	If level shifter implemented, 100kΩ to supply on the non-Jetson TX1 side of the device.	**UART #0 Clear to Send:** Connect to **RTS** pin of serial device

12.4.3 Boundary Scan Test Mode

In order to support Boundary Scan Test mode, the Tegra JTAG_TRST_N pin must be pulled high and Tegra must be held in reset without resetting the PMIC. The figure below illustrates this. Other requirements related to supporting Boundary Scan Test mode are described in the "Tegra X1 Series Boundary Scan Requirements & Usage" document.

Figure 31. Boundary Scan Connections



12.5 Strapping Pins

Figure 32. Force Recovery Strap Connections

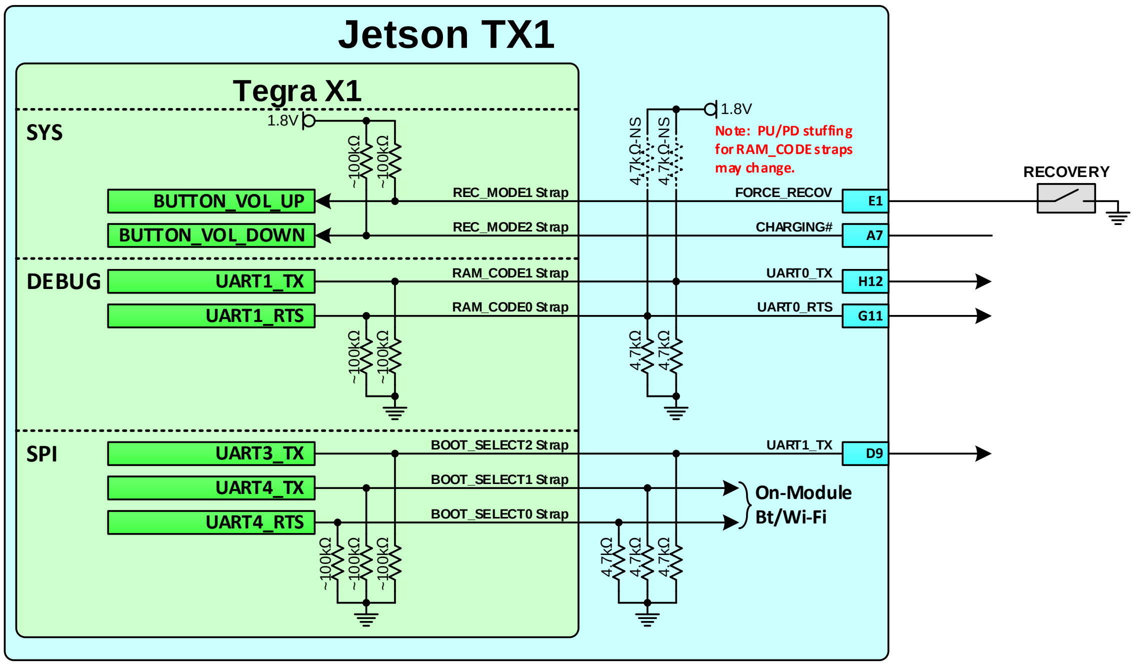


Table 53. Power-on Strapping Breakdown

Jetson TX1 Pin Name	Tegra X1 Ball Name	Strap Options	Tegra X1 Internal PU/PD	Jetson TX1 PU/PD	Description
FORCE_RECOV#	**BUTTON_VOL_UP**	REC_MODE1	~100kΩ PU		Recovery Mode [2:1] x1: Normal boot from secondary device 10: Forced Recovery Mode 00: Reserved ***See critical warning in note 1***
CHARGING#	**BUTTON_VOL_DOWN**	REC_MODE2	~100kΩ PU		
UART0_TX	**UAR1_TX**	RAM_CODE1	~100kΩ PD	4.7kΩ PD or 4.7KΩ PU	Selects one of four DRAM configuration sets within the BCT. For Nvidia use only. ***See critical warning in Note 2***.
UART0_RTS	**UART1_RTS**	RAM_CODE0	~100kΩ PD	4.7kΩ PD or 4.7KΩ PU	
UART1_TX	**UART3_TX**	BOOT_SELECT2	~100kΩ PD	4.7kΩ PD	Software reads value and determines Boot device to be configured and used 000 = eMMC x8 BootModeOFF, 512-byte page. Maps to SDMMC w/config=0x0001 size. 26MHz 001 – 111 Reserved ***See Notes 3 & 4*** ***See critical warning in Note 5.***
NA	**UART4_TX**	BOOT_SELECT1	~100kΩ PD	4.7kΩ PD	
NA	**UART4_RTS**	BOOT_SELECT0	~100kΩ PD	4.7kΩ PD	

Note:

1. If the CHARGING# pin is used in a design, it must not be driven or pulled low during power-on at the same time as FORCE_RECOV# is pulled low for Recovery Mode as this would change the strapping and select a reserved mode. ***Violating this requirement will prevent the system from entering Recovery Mode***.
2. If UART0_TX and/or UART0_RTS are used in a design, they must not be driven or pulled high or low during power-on. ***Violating this requirement can change the RAM_CODE strapping and result in functional failures***.
3. The above BOOT_SELECT option is only in effect in "regular boot" conditions i.e. cold boot. If "Forced Recovery" mode is detected (FORCE_RECOV# low at boot), that mode take precedence over the eMMC boot device choice.
4. eMMC boot does not use either the normal boot mode or alternate boot mode supported by the eMMC spec. The Tegra X1 BootROM uses the Card Identification mode for booting from eMMC.
5. If UART1_TX is used in a design, it must not be driven or pulled high during power-on as this would affect the BOOT_SELECT strapping. ***Violating this requirement will likely prevent the system from booting***.

13.0 PADS

Note: Jetson TX1 signals that come from Tegra X1 may glitch when the associated power rail is enabled. This may affect pins that are used as GPIO outputs. Designers should take this into account. GPIO outputs that must maintain a low state even while the power rail is being ramped up may require special handling.

13.1 Pad Drive Strength

The table below provides estimated output drive values across minimum/maximum DRVUP/DRVDN settings. There are values for 1.8V & 3.3V power rail voltages.

Table 54. Output Drive Current Estimates across Pad Output Control settings

	1.8V			3.3V		
	Drive current (mA)			Drive current (mA)		
DRVUP DRVDN	Min	Typ	Max	Min	Typ	Max
00000	7.2	15.5	23.8	16.5	28.3	40.0
11111	14.7	23.4	32.1	36.5	48.3	60.0

13.2 Pad DC Characteristics

Table 55. CMOS Pad Type DC Characteristics

Symbol	Description	Min	Max	Units
V_{IL}	Input Low Voltage	-0.5	0.25 x VDD	V
V_{IH}	Input High Voltage	0.75 x VDD	0.5 + VDD	V
V_{OL}	Output Low Voltage (I_{OL} = 1mA)	---	0.15 x VDD	V
V_{OH}	Output High Voltage (I_{OH} = -1mA)	0.85 x VDD	---	V

Table 56. Open Drain Pin Type DC Characteristics

Symbol	Description	Min	Max	Units
V_{IL}	Input Low Voltage	-0.5	0.25 x VDD	V
V_{IH}	Input High Voltage	0.75 x VDD		V
V_{OL}	Output Low Voltage (I_{OL} = 1mA)	---	0.15 x VDD	V

Note: Do not drive unpowered signals above 0.5V (when associated power rail is off).

14.0 UNUSED INTERFACE TERMINATIONS

14.1 Unused MPIO (Multi-purpose Standard CMOS Pad) Interfaces

The following Jetson TX1 pins (& groups of pins) are Tegra MPIO pins that support either special function IOs (SFIO) and/or GPIO capabilities. Any unused pins or portions of pin groups listed below that are not used can be left unconnected.

Table 57. Unused MPIO pins / Pin Groups

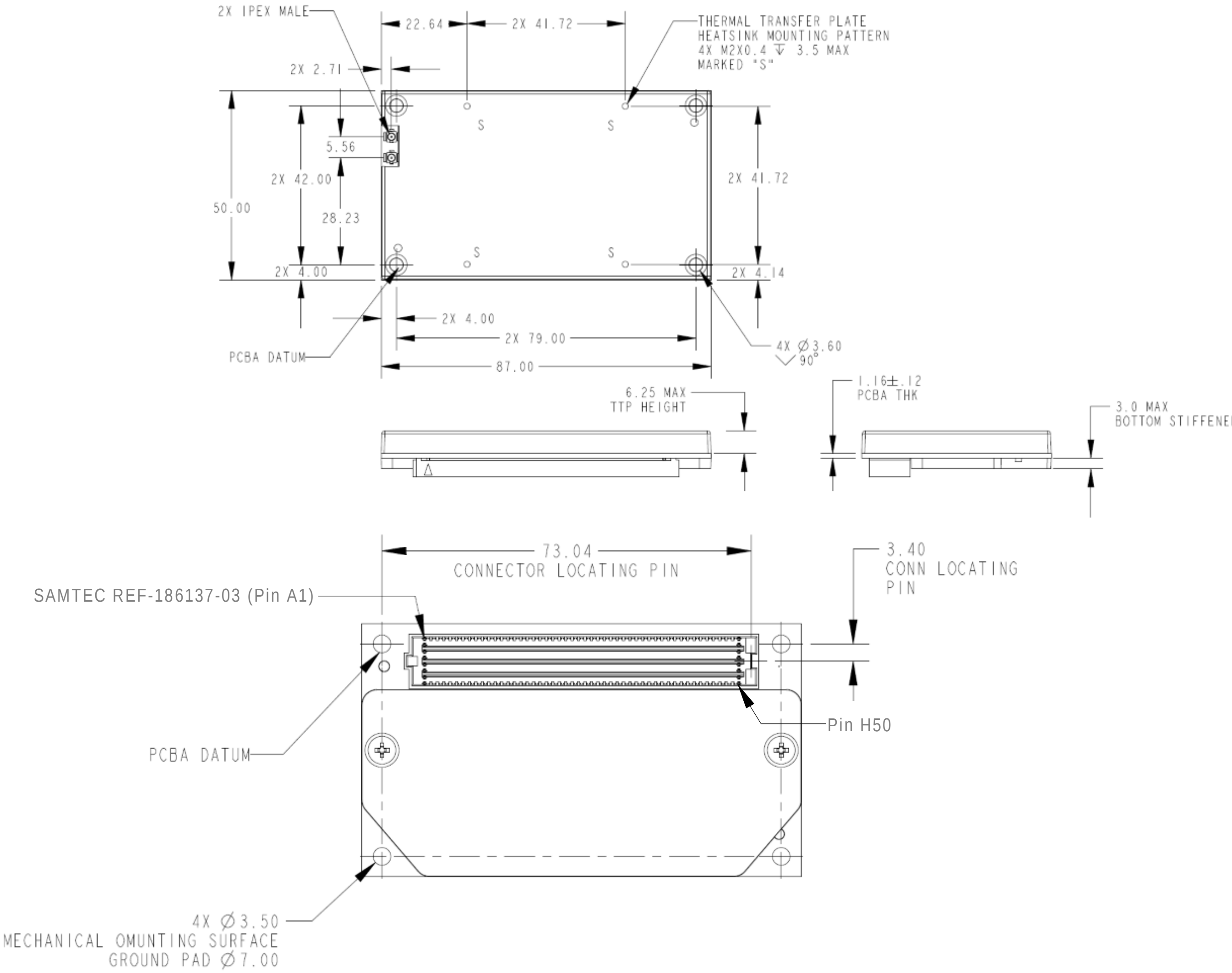
Jetson TX1 Pins / Pin Groups		Jetson TX1 Pins / Pin Groups
SLEEP#		CAM Control, Clock
BATLOW#		SDIO, SDMMC
FORCE_RECOV#		AUDIO_x
RESET_OUT#		I2S
WDT_TIME_OUT#		UART
CARRIER_STBY#		I2C
CHARGER_PRSNT#		SPI
CHARGING#		TOUCH_x
USBx_EN_OC#		WIFI_WAKE_x
PEXx_REFCLK/RST/CLKREQ/WAKE		MODEM_x, MDM2AP_x, AP2MDM_x
LCD0_BKLT_PWM, FAN_PWM		GPIO_EXP[1:0]_INT
LCD_x		ALS_PROX_INT, MOTION_INT
DP0_HPD, DP1_HPD, HDMI_CEC		JTAG

14.2 Unused Special Function Interfaces

See the Unused Special Function Pins section in the Checklist at the end of this document.

15.0 MECHANICAL

Figure 33. Jetson TX1 Dimensions



Notes:

- Carrier board connector location & mounting holes should match the Jetson TX1 dimensions shown in figure above.
- Carrier board components limited to 2.5mm under outline of Jetson TX1. This assumes the use of the mating connector "SAMTEC REF-186138-01" (SEAM-50-02.0-S-08-2-A-K-TR). If the connector used is taller, the max component height would change accordingly.
- The Keep out area on the carrier board for standoffs depends on diameter of standoffs used. Jetson TX1 carrier board uses 6MM diameter round keep out areas surrounding the four mounting holes. These areas on the PCB should be GND with no soldermask. See Jetson TX1 carrier board layout for reference.
- All Dimensions are in "MM" unless otherwise specified
- Tolerances are:
  - . X ± .25
  - .XX ± .13
  - Angles ± 1°
- Mass: 75 Grams, ±2%
- Thermal transfer Plate Finish: Clear Chemfilm per MIL-C-5541-E Class 3

16.0 DESIGN CHECKLIST

The checklist below is intended to help ensure that the correct connections have been made in a design. The check items describe connections for the various interfaces and the "Same/Diff/NA" column is intended to be used to indicate whether the design matches the check item description, is different, or is not applicable to the design.

Table 58. Checklist

Check Item Description			Same/Diff/NA
Jetson TX1 Signal Terminations (shown for reference only)			
	Parallel Termination	**Series Termination**	
USB/PCIe			
USB0_EN_OC#	External 100KΩ Pull Up to 3.3V	–	
USB1_EN_OC#	External 100KΩ Pull Up to 3.3V	–	
USB0_VBUS_DET	External 10KΩ Pull Up to 1.8V	Level shifter between Tegra & Jetson TX1 USB0_VBUS_DET pin	
PEX0_CLKREQ#	External 47KΩ Pull Up to 3.3V	–	
PEX0_RST#	External 47KΩ Pull Up to 3.3V	–	
PEX1_CLKREQ#	External 47KΩ Pull Up to 3.3V	–	
PEX1_RST#	External 47KΩ Pull Up to 3.3V	–	
PEX_WAKE#	External 47KΩ Pull Up to 3.3V	–	
HDMI/DP/eDP			
DP0_HPD	Internal Pull Down	–	
DP1_HPD	Internal Pull Down	–	
I2C			
I2C_GP0_CLK/DAT	External 1KΩ Pull Up to 1.8V	–	
I2C_GP1_CLK/DAT	External 1KΩ Pull Up to 3.3V	–	
I2C_PM_CLK/DAT	External 1KΩ Pull Up to 1.8V	–	
I2C_CAM_CLK/DAT	External 1KΩ Pull Up to 1.8V	–	
SPI			
SPI0_MOSI	Internal Pull Down	–	
SPI0_MISO	Internal Pull Down	–	
SPI0_CLK	Internal Pull Down	–	
SPI0_CS0#	Internal Pull Up to 1.8V	–	
SPI1_MOSI	Internal Pull Down	–	
SPI1_MISO	Internal Pull Down	–	
SPI1_CLK	Internal Pull Down	–	
SPI1_CS0#	Internal Pull Up to 1.8V	–	
SPI1_CS1#	Internal Pull Up to 1.8V	–	
SPI2_MOSI	Internal Pull Down	–	
SPI2_MISO	Internal Pull Down	–	
SPI2_CLK	Internal Pull Down	–	
SPI2_CS0#	External 100KΩ Pull Up to 1.8V	–	
SPI2_CS1#	External 100KΩ Pull Up to 1.8V	–	
SD Card			
SDCARD_CMD	Internal Pull Up to 1.8V/3.3V	–	
SDCARD_D[3:0]	Internal Pull Up to 1.8V/3.3V	–	
SDCARD_CD#	Internal Pull Up to 1.8V	–	
SDCARD_WP	Internal Pull Up to 1.8V	–	
SDIO			
SDIO_CMD	Internal Pull Up to 1.8V	–	
SDIO_D[3:0]	Internal Pull Up to 1.8V	–	
Embedded Display			
LCD_TE	Internal Pull Down	–	
GPIO			
GPIO19/AUD_RST	Internal Pull Up to 1.8V	–	
GPIO6/TOUCH_INT	Internal Pull Up to 1.8V	–	
GPIO8/ALS_PROX_INT	Internal Pull Up to 1.8V	–	

Check Item Description			Same/Diff/NA
GPIO9/MOTION_INT	Internal Pull Up to 1.8V	–	
GPIO10/WIFI_WAKE_AP	Internal Pull Up to 1.8V	–	
GPIO13/BT_WAKE_AP	Internal Pull Up to 1.8V	–	
GPIO16/MDM_WAKE_AP	Internal Pull Up to 1.8V	–	
GPIO17/MDM2AP_READY	Internal Pull Up to 1.8V	–	
GPIO18/MDM_COLDBOOT	Internal Pull Up to 1.8V		
GPIO_EXP0_INT	Internal Pull Up to 1.8V	–	
GPIO_EXP1_INT	Internal Pull Up to 1.8V	–	
System Control			
VIN_PWR_BAD#	External 10KΩ Pull Up to 5.0V	–	
FORCE_RECOV#	Internal Pull Up to 1.8V	–	
SLEEP#	Internal Pull Up to 1.8V	–	
POWER_BTN#	Internal Pull Up to 1.8V	BAT54CW Schottky barrier diodes	
RESET_IN#	External 4.7KΩ Pull Up to 1.8V	–	
FAN_TACH	Internal Pull Up to 1.8V		
Charging			
CHARGER_PRSNT#	Internal Pull Up to 1.8V	–	
CHARGING#	Internal Pull Up to 1.8V	–	
BATLOW#	Internal Pull Up to 1.8V	–	
JTAG			
JTAG_TCLK	External 100KΩ Pull Down to GND	–	
JTAG_GP0	External 100KΩ Pull Down to GND & 0.1uF capacitor to GND	–	
Carrier board Signal Terminations			
	Parallel Termination	**Series Termination**	
USB/PCIe/SATA			
USB_SS0_TX+/-	–	0.1uF capacitors near main connector	
USB_SS1_TX+/-	–	0.1uF capacitors near main connector	
USB_SS0_RX+/-	–	0.1uF capacitors near peripheral if directly connected	
USB_SS1_RX+/-	–	0.1uF capacitors near peripheral if directly connected	
PEX0_TX+/-	–	0.1uF capacitors near main connector	
PEX1_TX+/-	–	0.1uF capacitors near main connector	
PEX2_TX+/-	–	0.1uF capacitors near main connector	
PEX_RFU_TX+/-	–	0.1uF capacitors near main connector	
PEX0_RX+/-	–	0.1uF capacitors near peripheral if directly connected	
PEX1_RX+/-	–	0.1uF capacitors near peripheral if directly connected	
PEX2_RX+/-	–	0.1uF capacitors near peripheral if directly connected	
PEX_RFU_RX+/-	–	0.1uF capacitors near PCIe device/conn.	
SATA_TX+/-	–	0.01uF capacitors near main connector	
SATA_RX+/-	–	0.01uF capacitors near SATA device/conn.	
Ethernet			
GBE_MDI0+/-	–	Magnetics near RJ45 connector	
GBE_MDI1+/-	–	Magnetics near RJ45 connector	
GBE_MDI2+/-	–	Magnetics near RJ45 connector	
GBE_MDI3+/-	–	Magnetics near RJ45 connector	
GBE_LINK100#	–	LED and Pull Up Current Limiting Circuit	
GBE_LINK1000#	–	LED and Pull Up Current Limiting Circuit	
GBE_LINK_ACT#	–	LED and Pull Up Current Limiting Circuit	
DP[1:0] for eDP/DP			
DP0_TX3+/-	–	0.1uF capacitors near main connector	
DP0_TX2+/-	–	0.1uF capacitors near main connector	
DP0_TX1+/-	–	0.1uF capacitors near main connector	
DP0_TX0+/-	–	0.1uF capacitors near main connector	
DP0_AUX_CH+	–	0.1uF capacitors near main connector	

Check Item Description			Same/Diff/NA
DP0_AUX_CH-	–	0.1uF capacitors near main connector	
DP0_HPD	10kΩ Pull-up to 1.8V near main conn. & 100kΩ Pull-down to GND on DP side of level shifter.	Level Shifter (w/output toward main connector) near main connector & 100kΩ resistor to DP connector. Level shifter must be non-inverting.	
DP1_TX3+/-	–	0.1uF capacitors near main connector	
DP1_TX2+/-	–	0.1uF capacitors near main connector	
DP1_TX1+/-	–	0.1uF capacitors near main connector	
DP1_TX0+/-	–	0.1uF capacitors near main connector	
DP1_AUX_CH+	100kΩ Pull-down to GND near connector (DP only)	0.1uF capacitors near main connector	
DP1_AUX_CH-	100kΩ Pull-up to 3.3V near connector (DP only)	0.1uF capacitors near main connector	
DP1_HPD	10kΩ Pull-up to 1.8V near main conn. & 100kΩ Pull-down to GND on DP side of level shifter.	Level Shifter (w/output toward main connector) near main connector & 100kΩ resistor to DP connector. Level shifter must be non-inverting.	
DP1 for HDMI			
HDMI_TXC+/-	499Ω, 1% resistor to 600Ω bead to GND	0.1uF capacitors near HDMI connector	
HDMI_TX0+/-	499Ω, 1% resistor to 600Ω bead to GND	0.1uF capacitors near HDMI connector	
HDMI_TX1+/-	499Ω, 1% resistor to 600Ω bead to GND	0.1uF capacitors near HDMI connector	
HDMI_TX2+/-	499Ω, 1% resistor to 600Ω bead to GND	0.1uF capacitors near HDMI connector	
HDMI_DDC_SCL/SDA	10kΩ Pull-up to 3.3V near main conn. & 1.8kΩ Pull-up to 5V near HDMI conn.	Bidirectional level shifter between Pull-ups in Parallel Termination column	
HDMI_HPD	10kΩ Pull-up to 1.8V near main conn. & 100kΩ Pull-down to GND near HDMI conn.	Level shifter (w/output toward main connector) between Pull-up & Pull-down in Parallel Termination column. Level shifter can be inverting or non-inverting. 100kΩ series resistor between pull-down & HDMI connector.	

Power

Jetson TX1 Power Supplies

Supply (Carrier Board)	Usage	(V)	Supply Type	Source	Enable	
VDD_IN	Main Supply from Adapter	5.5-19.6	Adapter	na	na	
VDD_RTC	Real-time clock supply	2.6-5.5	Jetson TX1 PMIC	VDD_5V0_SYS on Jetson TX1 or carrier board (for charging)	na	

Carrier Board Supplies

Supply (Carrier Board)	Usage	(V)	Supply Type	Source	Enable	
VDD_MUX	Main power input from DC Adapter	5.5-19.6	FETs	DC Adapter		
VDD_5V0_IO_SYS	Main 5V supply	5.0	DC/DC	VDD_MUX	CARRIER_PWR_ON	
VDD_3V3_SYS	Main 3.3V supply	3.3	DC/DC	VDD_MUX	3V3_SYS_BUCK_EN	
VDD_1V8	Main 1.8V supply	1.8	DC/DC	VDD_5V0_IO_SYS	1V8_IO_VREG_EN (VDD_3V3_SYS_PG)	
VDD_3V3_SLP	3.3V rail, off in Sleep (various)	3.3	FETs/Ld Sw	VDD_3V3_SYS	SOC_PWR_REQ	
VDD_5V0_IO_SLP	5V rail, off in Sleep, for SATA/FAN	5	FETs/Ld Sw	VDD_5V0_IO_SYS	VDD_3V3_SLP	
VDD_12V_SLP	PCIe & SATA connectors	12	Boost	VDD_5V0_IO_SYS	VDD_3V3_SLP	
VDD_VBUS_CON	VBUS for USB 2.0 Type AB conn.	5.0	Load Switch	VDD_5V0_IO_SYS	USB_VBUS_EN0	
USB_VBUS	VBUS for USB 3.0 Type A conn.	5.0	Load Switch	VDD_5V0_IO_SYS	USB_VBUS_EN1	
SD_CARD_SW_PWR	SD Card power rail	3.3	Load Switch	VDD_3V3_SYS	SDCARD_VDD_EN	
VDD_5V0_HDMI_CON	5V rail for HDMI connector	5.0	Load Switch	VDD_5V0_IO_SYS	GPIO Expander U29, P14	
VDD_TS_1V8	1.8V rail for touch screen	1.8	Load Switch	VDD_1V8	GPIO Expander U29, P01	
AVDD_TS_DIS	High voltage rail for touch screen	3.3	Load Switch	VDD_3V3_SLP	GPIO Expander U29, P02	
VDD_LCD_1V8_DIS	1.8V rail for panel	1.8	Load Switch	VDD_1V8	GPIO Expander U29, P11	
VDD_DIS_3V3_LCD	High voltage rail for panel	3.3	Load Switch	VDD_3V3_SYS	GPIO Expander U29, P03	
VDD_1V2	Generic 1.2V display rail	1.2	LDO	VDD_1V8	GPIO Expander U29, P12	
DVDD_CAM_IO_1V8	1.8V rail for camera I/O	1.8	Load Switch	VDD_1V8	GPIO Expander U28, P11	
AVDD_CAM	High voltage rail for cameras	2.8	Load Switch	VDD_3V3_SLP	GPIO Expander U28, P15	
DVDD_CAM_IO_1V2	1.2V rail for camera core	1.2	LDO	VDD_1V8	GPIO Expander U28, P12	

Check Item Description	Same/Diff/NA
Power Control	
VIN_PWR_BAD# connects to carrier board main power input & discharge circuit. Inactive when main supply is stable	
CARRIER_PWR_ON used as enable for carrier board main 5V supply & discharge circuit	
RESET_IN# to carrier board connects to system reset source(s) such as reset button, etc.	
RESET_OUT# from Jetson TX1 connects to devices on carrier board that require reset during power-on	
POWER_BTN# connects to button or similar to pull POWER_BTN# to GND when pressed/asserted to power system ON/OFF	
SLEEP# connects to button or similar to pull SLEEP# to GND when pressed/asserted to put system in sleep mode	
CARRIER_STBY# connects to enable of supplies that should be off in Sleep mode such as VDD_3V3_SLP	
Power Discharge	
Discharge circuit is implemented to bring carrier board main 5V, 3.3V, 1.8V & 3.3V Sleep rails low when system is powered off or the main supply is removed. Circuit also asserts VIN_PWR_BAD# when power is removed.	
Wake Event Pins	
If Audio Interrupt required, **GPIO20_AUD_INT** pin is used	
If External BT Wake Request to AP required, **GPIO13_BT_WAKE_AP** pin is used	
If External Wi-Fi Wake Request to AP required, **GPIO10_WIFI_WAKE_AP** pin is used	
If Modem to AP Ready required, **GPIO17_MDM2AP_READY** pin is used	
If Modem Cold Boot Alert required, **GPIO18_MDM_COLDBOOT** pin is used	
If HDMI CEC required, **HDMI_CEC** pin is used	
If GPIO Expander 0 Interrupt required, **GPIO_EXP0_INT** pin is used	
If Power Button On required, **POWER_BTN#** pin is used	
If Charging Interrupt required, **CHARGING#** pin is used	
If Sleep Request from carrier board required, **SLEEP#** pin is used	
If Ambient/Proximity Interrupt required, **GPIO8_ALS_PROX_INT** pin is used	
If HDMI Hot Plug Detect required, **DP1_HPD** pin is used	
If Battery Low Warning required, **BATLOW#** pin is used	
If Primary Modem Wake Request to AP required, **GPIO16_MDM_WAKE_AP** pin is used	
If Touch Controller Interrupt required, **GPIO6_TOUCH_INT** pin is used	
If Motion Sensor Interrupt required, **GPIO9_MOTION_INT** pin is used	
USB/PEX/SATA Connections	
USB 2.0	
USB0 available to be used as device for USB recovery at a minimum	
USB ID from connector, if used, connects to Jetson TX1 USB0_OTG_ID pin	
VBUS from connector connects to load switch (if host supported) and USB0_VBUS_DET pin on Jetson TX1 (100kΩ resistor to GND required)	
Any EMI/ESD devices used are suitable for USB High-speed	
USB 3.0	
USB_SS0_RX+/– connected to RX+/- pins on USB 3.0 connector, Device, Hub, etc.	
USB_SS0_TX+/– connected to TX+/- pins on USB 3.0 connector, Device, Hub, etc. (See Signal Terminations)	
Additional USB 3.0 interfaces taken from USB_SS1_x, PEX1_x or SATA (See Signal Terminations)	
See USB 3.0 section for Common Mode Choke requirements if this is required. TDK ACM2012D-900-2P device is recommended	
See USB 3.0 section for ESD requirements. SEMTECH ESD Rclamp0524p device is recommended	
PCIe	
PCIe Controller #1 (x1)	
PEX1 used for 3.3V single-lane device/connector	
TX+/– connected to corresponding pins on connector, or RX+/– on device on carrier board (See Signal Terminations)	
RX+/– connected to corresponding pins on connector, or TX+/– on device on carrier board	
AC caps are provided for device TX pins (those connected to Jetson TX1 RX+/–) if device is on carrier board (See Signal Terminations)	
Reference clock used for PCIe Controller #1 (single-lane PCIe interface) is PEX1_REFCLK+/–	
Clock Request & Reset for PCIe Controller #1 are PEX1_CLKREQ# & PEX1_RST# (See Signal Terminations)	
PCIe Controller #0 (up to x4)	
PEX0 used for 3.3V single-lane device/connector	
PEX0 & USB_SS1 used for 3.3V 2-lane device/connector	
PEX0, USB_SS1, PEX2 & PEX_RFU used for 3.3V 4-lane device/connector	
TX+/– connected to corresponding pins on connector, or RX+/– on device on carrier board (See Signal Terminations)	
RX+/– connected to corresponding pins on connector, or TX+/– on device on carrier board	
AC caps are provided for device TX pins (those connected to Jetson TX1 RX+/–) if device is on carrier board (See Signal Terminations)	
Reference clock used for PCIe Controller #0 (Up to x4 lane PCIe interface) is PEX0_REFCLK+/–	
Clock Request & Reset for PCIe Controller #0 are PEX0_CLKREQ# & PEX0_RST#	
Common	
PEX_WAKE# connected to WAKE pins on devices/connectors (See Signal Terminations)	

Check Item Description	Same/Diff/NA
SATA	
SATA_TX+/– connected to TX_P/N pins of SATA connector (or RX+/– pins of onboard device) (See Signal Terminations)	
SATA_RX+/– connected to RX_P/N pins of SATA connector (or TX+/– pins of onboard device) (See Signal Terminations)	
See SATA section for Common Mode Choke requirements if they are required. TDK ACM2012D-900-2P device is recommended	
See SATA section for ESD requirements. SEMTECH ESD Rclamp0524p device is recommended	
SDMMC Connections	
SD Card	
SDCARD_CLK connected to CLK pin of socket	
SDCARD_CMD connected to CMD pin of device. (See Signal Terminations)	
SDCARD_D[3:0] connected to DATA[3:0] pins of socket. (See Signal Terminations)	
SDCARD_CD connected to the SD Card Detect pin on socket	
SDCARD_WP connected to the SD Card Write Protect pin on socket (if supported)	
SDCARD_PWR_EN connected to SD Card VDD supply/load switch enable pin	
Adequate bypass caps provided on SD Card VDD rail	
Any EMI/ESD devices used are suitable for highest frequencies supported (low capacitive load: <1pf recommended).	
SDIO	
SDIO_CLK connected to CLK pin of device	
SDIO_CMD connected to CMD pin of device. (See Signal Terminations)	
SDIO_D[3:0] connected to DATA[3:0] pins of device. (See Signal Terminations)	
Any EMI/ESD devices used are suitable for highest frequencies supported (low capacitive load: <1pf recommended).	
Display Connections	
DSI	
DSI0_CK+/– connected to CLKn & CLKp pins of the primary DSI display	
DSI0_D[1:0] +/– connected to lower 2 lanes of the primary DSI display.	
DSI1_D[1:0] +/– connected to upper two lanes of the primary 4 lane DSI display.	
DSI2_CK+/– connected to CLKp/n pins of either the primary DSI display if it supports a 2 x4 lane interface, or a secondary DSI display	
DSI2_D[1:0] +/– connected to lower 2 lanes of a secondary DSI display or lower 2 lanes of the upper 4 lanes of the primary DSI display supporting a 2 x4 lane interface.	
DSI3_D[1:0] +/– connected to upper 2 lanes of a secondary DSI display or upper 2 lanes of upper 4 lanes of the primary DSI display supporting a 2 x4 lane interface.	
LCD_TE (used for Tearing Effect signal from display) connected to matching pin on display connector if supported	
LCD_VDD_EN connected to enable of embedded display related power supply/load switch	
LCD_BKLT_EN connected to enable of backlight solution	
LCD_BKLT_PWM connected to PWM input of backlight solution	
Any EMI/ESD devices used on DSI signals are suitable for highest frequencies supported (low capacitive load: <1pf recommended)	
eDP	
DP0_TX[3:0] +/– connected to eDP panel/connector (See Signal Terminations)	
DP0_AUX_CH+/– connected to Aux Lane of eDP panel/connector (See Signal Terminations)	
DP0_HPD connected to HPD pin of panel/connector (if DP implemented on DP0 pins– not applicable to eDP)	
Any EMI/ESD devices used are suitable for highest frequencies supported (low capacitive load: <1pf recommended)	
Check Item Description	**Same/Diff/NA**
HDMI	
DP1_TX3+/– connected to C–/C+ & pins on HDMI Connector (See Signal Terminations)	
DP1_TX[2:0]+/– connected to D[0:2]+/– pins (See DP/HDMI Pin Mapping table) (See Signal Terminations)	
DP1_HPD connected to HPD pin on HDMI Connector (See Signal Terminations)	
HDMI_CEC connected to CEC on HDMI Connector through gating circuitry.	
DP1_AUX_CH+ connected to SCL & DP1_AUX_CH– to SDA on HDMI Connector (See Signal Terminations)	
HDMI 5V Supply connected to +5V on HDMI Connector.	
See HDMI section for Common Mode Choke requirements if this is required (not recommended unless EMI issues seen)	
See HDMI section for ESD requirements. ON-Semiconductor ESD8040 device is recommended	
DP	
DP1_TX[3:0]+/– connected to D[3:0]+/– on DP Connector. (See Signal Terminations)	
DP1_HDP connected to HPD pin on DP Connector (See Signal Terminations)	
DP1_AUX_CH+/– connected to AUX_CH+/– on DP connector (See Signal Terminations)	
DP 3.3V Supply connected 3.3V supply pin on DP connector to VDD_3V3_SYS with adequate decoupling.	
Any EMI/ESD devices used are suitable for highest frequencies supported (low capacitive load: <1pf recommended)	
Video Input	
Camera (CSI)	

Check Item Description	Same/Diff/NA
CSI[5:0]_CLK+/– connected to clock pins of camera. See the CSI Configurations table for details	
CSI[5:0]_D[1:0]+/– connected to data pins of camera. See the CSI Configurations table for details	
I2C_CAM_CK/DAT connected to I2C SCL & SDA pins of imager (See Signal Terminations).	
CAM[1:0]_MCLK connected to Camera reference clock inputs.	
GPIO1_CAM1_PWR# / GPIO0_CAM0_PWR# connected to power down pins on camera(s).	
GPIO4_CAM_STROBE connected to camera strobe circuit unless strobe control comes from camera module.	
CAM_FLASH_EN connected to enable of flash circuit	
If Jetson TX1 GPIO used for flash control, CAM_FLASH_EN and/or CAMR_STROBE pins are used	
GPIO3_CAM1_RST# / GPIO2_CAM0_RST# connected to reset pin on any cameras with this function.	
If Auto Focus Enable is required, GPIO3_CAM1_RST# connected to AF_EN pin on camera module & GPIO2_CAM0_RST# used as common reset line.	
Any EMI/ESD devices used are suitable for highest frequencies supported (low capacitive load: <1pf recommended)	
Audio	
Codec/DAP/I2S	
I2S0 used for Audio Codec if present in design	
I2S2 used for BT if present in design	
I2S[3:0]-SCLK Connect to I2S/PCM CLK pin of audio device.	
I2S[3:0]-LRCK Connect to word/field select pin of audio device.	
I2S[3:0]-SDATA_OUT Connect to Data Input pin of audio device.	
I2S[3:0]-SDATA_IN Connect to Data Output pin of audio device.	
AUD_MCLK Connect to clock pin of Audio Codec.	
GPIO8_AUD_RST Connect to reset pin of Audio Codec.	
GPIO9_AUD_INT Connect to interrupt pin of Audio Codec.	
I2C/SPI/UART	
I2C	
I2C devices on same I2C interface do not have address conflicts (comparisons are done 7-bit to 7-bit format or 8-bit to 8-bit format)	
I2C_CAM, I2C_GP0 & I2C_PM (See Signal Terminations). Additional external pull-ups are not added & devices on bus are 1.8V or level shifter is used.	
I2C_GP1 (See Signal Terminations). Additional external pull-ups are not added & devices on bus are 3.3V or level shifter is used.	
Pull-up resistors are provided on all I2C I/F segments, including on either side of any level shifters.	
Pull-up resistor values based on frequency/load (check I2C Spec)	
I2C_CAM_CK/DAT, I2C_GP[1:0]_CK/DAT & I2C_PM_CK/DAT connect to SCL/SDA pins of devices	
SPI	
SPI[2:0]_CLK connected to Peripheral CLK pin(s)	
SPI[2:0]_MOSI connected to Slave Peripheral MOSI pin(s)	
SPI[2:0]_MISO connected to Slave Peripheral MISO pin(s)	
SPI[2:1]_CS[1:0]# / SPI0_CS0# connected one CS# pin per SPI IF to each Slave Peripheral CS pin on the interface	
Check Item Description	**Same/Diff/NA**
UART	
UARTx_TX connects to Peripheral RX pin of device	
UARTx_RX connects to Peripheral TX pin of device	
UARTx_CTS# connects to Peripheral RTS# pin of device	
UARTx_RTS# connects to Peripheral CTS# pin of device	
Miscellaneous	
JTAG	
JTAG_TMS Connect to TMS pin of connector	
JTAG_TCK Connect to TCK pin of connector (See Signal Terminations).	
JTAG_TDO Connect to TDO pin of connector	
JTAG_TDI Connect to TDI pin of connector	
JTAG_RTCLK Connect to RTCK pin of connector	
JTAG_TRST#: For Scan test mode, TRST# is connected to JTAG connector by installing series resistor. (See Signal Terminations).	
For normal operation, JTAG_TRST# is pulled down only & series resistor to connector not stuffed.	
Strapping	
FORCE_RECOV#: To enter Forced Recovery mode, pin is connected to GND when system is powered on.	
Pin Selection	
Pinmux completed including GPIO usage (direction, initial state, Ext. PU/PD resistors, Deep Sleep state).	
SFIO usage matches reference platform where possible.	
Each SFIO function assigned to only one pin, even if function selected in Pinmux registers is not used or pin used as GPIO	

Check Item Description		**Same/Diff/NA**
GPIO usage matches reference platform where possible.		
Unused Special Function Interface Pins		
Ball Name	Termination	
USB 2.0		
USB[2:1]+/–	Leave NC any unused pins	
USB 3.0 / PCIe		
PEX_[2:0]_TX+/–, **USB_SS[1:0]_TX**+/–, **PEX_RFU_TX**+/–	Leave NC any unused TX lines	
PEX_[2:0]_RX+/–, **USB_SS[1:0]_RX**+/–, **PEX_RFU_RX**+/–	Connect to **GND** any unused RX lanes	
PEX_[1:0]_REFCLK+/–	Leave NC if not used	
Ball Name	Termination	
SATA		
SATA_TX+/–	Leave NC if not used.	
SATA_RX+/–	Connect to **GND** if SATA IF not used	
DSI		
DSI[2,0]_CK+/–	Leave NC any Clock lane not used.	
DSI[3:0]_D[1:0]+/–	Leave NC any unused DSI Data lanes	
DSI[3,1]_CK+/–	Leave NC - not used on Jetson TX1	
CSI		
CSI[5:0]_CK+/–	Leave NC any unused CSI Clock lanes	
CSI[5:0]_D[1:0] +/–	Leave NC any unused CSI Data lanes	
eDP		
DP0_TX[3:0] +/–	Leave NC any unused lanes	
DP0_AUX_CH+/–	Leave NC if not used	
DP0_HPD	Leave NC if not used	
HDMI/DP		
DP1_TX[3:0] +/–	Leave NC if lanes not used for HDMI or DP	
DP1_AUX_CH+/–	Leave NC if not used	
DP1_HPD	Leave NC if not used	
HDMI_CEC	Leave NC if not used	

17.0 APPENDIX A: GENERAL LAYOUT GUIDELINES

17.1 Overview

Trace and via characteristics play an important role in signal integrity and power distribution on a the Jetson TX1. Vias can have a strong impact on power distribution and signal noise, so careful planning must take place to ensure designs meet NVIDIA's via requirements. Trace length and impedance determine signal propagation time and reflections, both of which can greatly improve or reduce the performance of the Jetson TX1. Trace and via requirements for each signal type can be found in the corresponding chapter; this appendix provides general guidelines for via and trace placement.

17.2 Via Guidelines

The number of vias in the path of a given signal, power supply line, or ground line can greatly affect the performance of the trace. Via placement can make differences in current carrying capability, signal integrity (due to reflections and attenuation), and noise generation, all of which can impact the overall performance of the trace. The following guidelines provide basic advice for proper use of vias.

17.2.1 Via Count and Trace Width

As a general rule, each ampere of current requires at least two micro-vias.

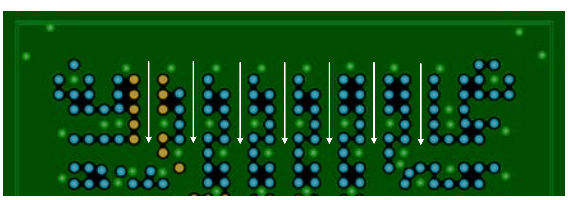
17.2.2 Via Placement

If vias are not placed carefully, they can severely degrade the robustness of a board's power plane. In standard deigns that don't use blind or buried vias, construction of a via entails drilling a hole that cuts into the power and ground planes. Thus, incorrect via placement affects the amount of copper available to carry current to the power balls of the IC. The package pin-out and breakout patterns are designed with via channels in mind.

17.2.3 Via Placement and Power/Ground Corridors

Vias should be placed so that sufficiently wide power corridors are created for good power distribution, as show in Figure 34.

Figure 34. Via Placement for Good Power Distribution



Care should also be taken to avoid use of "thermal spokes" (also referred to as "thermal relief") on power and ground vias. Thermal spokes are not necessary for surface-mount components, and the narrow spoke widths contribute to increased inductance. The metal on the inner layers between vias may not be flooded with copper if sufficient spacing is not provided. The diminished spacing creates a blockage and forces the current to find another path due to lack of copper, as shown in Figure 35 and Figure 36. This leads to power delivery issues and impedance discontinuities when traces are routed over these plane voids.

Figure 35. Good Current Flow Resulting from Correct Via Placement

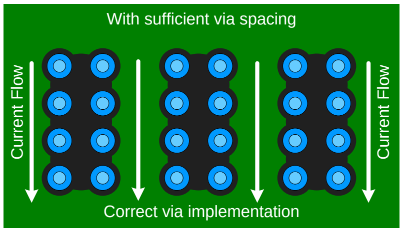
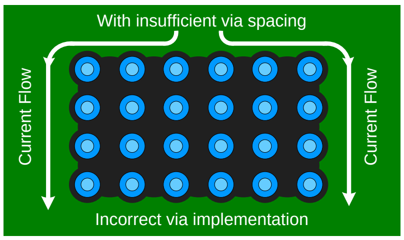


Figure 36. Poor Current Flow Resulting from Incorrect via Placement



In general, a dense via population should be avoided and good PCB design principles and analysis should be applied.

17.3 Connecting Vias

To be effective, vias must be connected properly to the signal and power planes. Poor via connections make the capacitor and power planes less effective, leading to increased cost due to the need for additional capacitors to achieve equivalent performance. This not only impacts the BOM (Bill of Material) cost of the design, but it can greatly impact quality and reliability of the design.

17.4 Trace Guidelines

Trace length and impedance play a critical role in signal integrity between the driver and the receiver on the Jetson TX1. Signal trace requirements are determined by the driver characteristics, source characteristics, and signal frequency of the propagating signal.

17.4.1 Layer Stack-Up

The number of layers required is determined by the number of memory signal layers needed to achieve the desired performance, and the number of power rails required to achieve the optimum power delivery/noise floor. For example, high-performance boards require four memory signal routing layers, with at least two GND planes for reference. This comes to six layers; add another two for power, which gives eight layers minimum. Reduction from eight to six layers starts the trade-off of cost versus performance.

Power and GND planes usually serve two purposes in PCB design: power distribution and providing a signal reference for high-speed signals.

Either the power or the ground planes can be used for high-speed signal reference; this is particularly common for low-cost designs with a low layer count. When both power and GND are used for signal reference, make sure you minimize the reference plane transition for all high-speed signals. Decoupling caps or transition vias should be added close to the reference plane transitions.

17.4.2 Trace Length

The maximum trace length for a given signal is determined by the maximum allowable propagation delay and impedance for the signal. Higher frequency signals must be treated as transmission lines (see “Appendix C – Transmission Line Primer”) to determine proper trace characteristics for a signal.

All signals on the graphics card maintain different trace guidelines; please refer to the corresponding signal chapter in the Design Guide to determine the guidelines for the signal.

18.0 APPENDIX B: STACK-UPS

18.1 Reference Design Stack-Ups

18.1.1 Importance of Stack-Up Definition

Stack-ups define the number and order of Board layers. Stack-up definition is critical to the following design:

- Circuit routability
- Signal quality
- Cost

18.1.2 Impact of Stack-Up Definition on Design

Stack-Up Impact on Circuit Routability

If there are insufficient layers to maintain proper signal spacing, prevent discontinuities in reference planes, obstruct flow of sufficient current, or avoid extra vias, circuit routing can become unnecessarily complex. Layer count must be minimally appropriate for the circuit.

Stack-Up Impact on Signal Quality

Both layer count and layer order impact signal integrity. Proper inter-signal spacing must be achievable. Via count for critical signals must be minimized. Current commensurate with the performance of the board must be carried. Critical signals must be adjacent to major and minor reference planes, and adhere to proximity constraints with respect to those planes. The recommended NVIDIA stack-ups achieve these requirements for the signal speeds supported by the board.

Stack-Up Impact on Cost

While defining extra layers can facilitate excellent signal integrity, current handling capability and routability, extra layers can impede the goal of hitting cost targets. The art of stack-up definition is achieving all technical and reliability circuit requirements in a cost efficient manner. The recommended NVIDIA stack-ups achieve these requirements with efficient use of board layers.

19.0 APPENDIX C: TRANSMISSION LINE PRIMER

19.1 Background

NVIDIA maintains strict guidelines for high-frequency PCB transmission lines to ensure optimal signal integrity for data transmission. This section provides a brief primer into basic board-level transmission line theory.

Characteristics

The most important PCB transmission line characteristics are listed in the following bullets:

- Trace width/height, PCB height and dielectric constant, and layer stack-up affect the characteristic trace impedance of a transmission line.

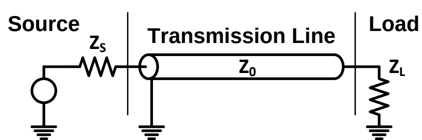
$$Z_0 \cong \left(\frac{L}{C}\right)^{1/2}$$

- Signal rise time is proportional to the transmission line impedance and load capacitance.

$$\text{RiseTime} \cong \left(\frac{Z_0 * R_{Term}}{Z_0 + R_{Term}}\right) * C_{Load}$$

- Real transmission lines (Figure 37) have non-zero resistances that lead to attenuation and distortion, creating signal integrity issues.

Figure 37. Typical Transmission Line Circuit



Transmission lines are used to “transmit” the source signal to the load or destination with as little signal degradation or reflection as possible. For this reason it is important to design the high-speed signal transmission line to fall within characteristic guidelines based on the signal speed and type.

19.2 Physical Transmission Line Types

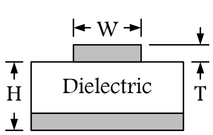
The two primary transmission line types often used for Tegra board designs are

- Microstrip transmission line (Figure 38)
- Stripline transmission line (Figure 39)

The following sections describe each type of transmission.

Microstrip Transmission Line

Figure 38. Microstrip Transmission Line

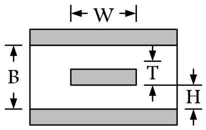


$$Z_0 = \left(\frac{87}{\sqrt{Er + 1.414}}\right) \ln\left(\frac{5.98H}{0.8W + T}\right)$$

- Z_0: Impedance
- W: Trace width (inches)
- T: Trace thickness (inches)
- Er: Dielectric constant of substrate
- H: Distance between signal and reference plane

Stripline Transmission Line

Figure 39. Stripline Transmission Line



$$Z_0 = \left(\frac{60}{\sqrt{Er}}\right)\ln\left(\frac{4H}{0.67\pi W\left(0.8 + \frac{T}{W}\right)}\right)$$

- Z_0: Impedance
- W: Trace width (inches)
- T: Trace thickness (inches)
- Er: Dielectric constant of substrate
- H: Distance between signal and reference plane

19.3 Driver Characteristics

Driver characteristics are important to the integrity and maximum speed of the signal. The following points identify key driver equations and concepts used to improve signal integrity and transmission speed.

- The driver (source) has resistive output impedance Z_S, which causes only a fraction of the signal voltage to propagate down the transmission line to the receiver (load).
  - • Transfer function at source:

    $$T1 = \frac{Z_0}{Z_S + Z_0}$$

  - • Driver strength is inversely proportional to the source impedance, Z_S.
- Z_S also acts as the source termination, which helps dampen reflection.
  - Source reflection coefficient:

    $$R1 = \frac{(Z_S - Z_0)}{(Z_S + Z_0)}$$

19.4 Receiver Characteristics

Receiver characteristics are important to the integrity and detectability of the signal. The following points identify key receiver concepts and equations for optimum signal integrity at the final destination.

- The receiver acts as a capacitive load and often has a high load impedance, Z_L.
- Unterminated transmission lines cause overshoot and reflection at the receiver, which can cause data corruption.
  - Output transfer function at load:

    $$T2 = \frac{2 * Z_L}{Z_L + Z_0}$$

  - Load reflection coefficient:

    $$R2 = \frac{(Z_L - Z_0)}{(Z_L + Z_0)}$$

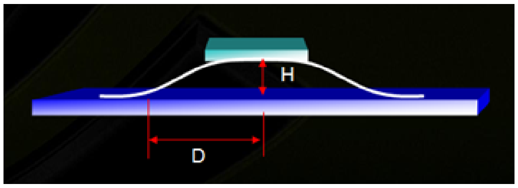
- Load impedance can be lowered with a termination resistor (R_{Term}) placed at the end of the transmission line.
  - Reflection is minimized when Z_L matches Z_0

19.5 Transmission Lines & Reference Planes

Defining an appropriate reference plane is vital to transmission line performance due to crosstalk and EMI issues. The following points explore appropriate reference plane identification and characteristics for optimal signal integrity:

- Transmission line return current (Figure 40)
  - High-speed return current follows the path of least inductance.
  - The lowest inductance path for a transmission line is right underneath the transmission line; i(D) is proportional to:

Figure 40. Transmission Line Height



- Transmission line return current:
  - High-speed return current follows the path of least inductance.
  - The lowest inductance path for a transmission line is the portion of the line closest to the dielectric surface; i(D) is proportional to

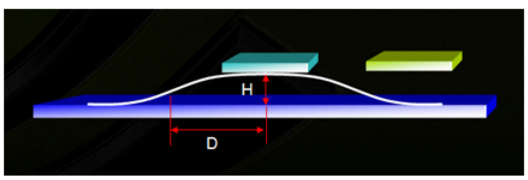
$$\frac{1}{\left(1+\left(\frac{D}{H}\right)^2\right)}$$

- Crosstalk on solid reference plane (Figure 41):
  - Crosstalk is caused by the mutual inductance of two parallel traces.
  - Crosstalk at the second trace is proportional to

$$\frac{1}{\left(1+\left(\frac{D}{H}\right)^2\right)}$$

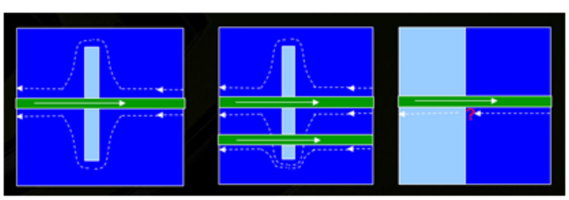
  - The signals need to be properly spaced to minimize crosstalk.

Figure 41. Crosstalk on Reference Plane



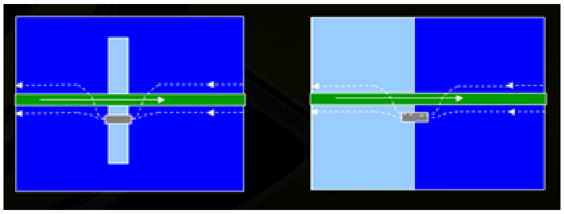
- Reference plane selection
  - Solid ground is preferred as reference plane.
  - Solid power can be used as reference plane with decoupling capacitors near driver and receiver.
  - Reference plane cuts and layer changes need to be avoided.
- Power plane cut example (Figure 42)
  - Power plane cuts will cause EMI issues.
  - Power plane cuts also induce crosstalk to adjacent signals.

Figure 42. Example of Power Plane Cuts



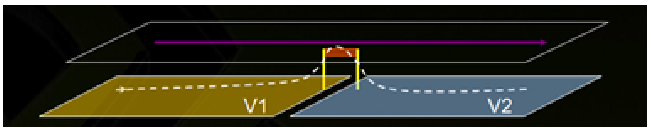
- When cut is unavoidable:
  - • Place decoupling capacitors near transition.
  - • Place transition near source or receiver when decoupling capacitors are abundant (Figure 43).

Figure 43. Another Example of Power Plane Cuts



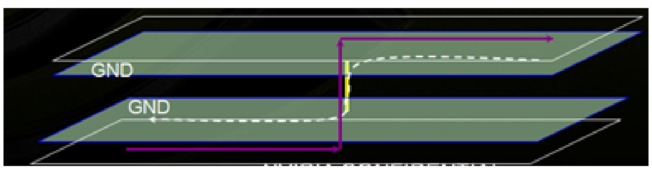
- When signal changes plane:
  - Try not to change the reference plane, if possible.
  - When a reference plane switches to different power rail, a stitching capacitor is required (Figure 44).

Figure 44. Switching Reference Planes



  - When the same ground/power reference plane changes to a different layer, a stitching via is required (Figure 45).

Figure 45. Reference Plane Switch Using VIA



20.0 APPENDIX D: DESIGN GUIDELINE GLOSSARY

The Design Guidelines include various terms. The descriptions in the table below are intended to show what these terms mean and how they should be applied to a design.

Table 59 Layout Guideline Tutorial

Trace Delays
Max Breakout Delay - Routing on Component layer: Maximum Trace Delay from inner ball to point beyond ball array where normal trace spacing/impedance can be met. Routing passes to layer other than Component layer: Trace delay from ball to via + via delay. Beyond this, normal trace spacing/impedance must be met. **Max Total Trace Delay** - Trace from Jetson TX1 pin to Device pin. This must include routing on the main PCB & any other Flex or secondary PCB. Delay is from Jetson TX1 to the final connector/device.
Intra/Inter Pair Skews
Intra Pair Skew (within pair) - Difference in delay between two traces in differential pair: Shorter routes may require indirect path to equalize delays **Inter Pair Skew (pair to pair)** - Difference between two (or possibly more) differential pairs
Impedance/Spacing
Microstrip vs Stripline - Microstrip: Traces next to single ref. plane. Stripline: Traces between two ref planes **Trace Impedance** - Impedance of trace determined by width & height of trace, distance from ref. plane & dielectric constant of PCB material. For differential traces, space between pair of traces is also a factor **Board trace spacing / Spacing to other nets** - Minimum distance between two traces. Usually specified in terms of dielectric height which is distance from trace to reference layers. **Pair to pair spacing** - Spacing between differential traces **Breakout spacing** - Possible exception to board trace spacing above is shown in figure to right where different spacing rules are allowed under Tegra in order to escape from Ball array. - This includes spacing between adjacent traces & between traces/vias or pads under the device in order to escape ball matrix. Outside device boundary, normal spacing rules apply.
Reference Return

Ground Reference Return Via & Via proximity (signal to reference)
- Signals changing layers & reference GND planes need similar return current path
- Accomplished by adding via, tying both GND layers together
Via proximity (sig to ref) is distance between signal & reference return vias
- GND reference via for Differential Pair
- Where a differential pair changes GND reference layers, return via should be placed close to & between signal vias (example to right)
Signal to return via ratio
- Number of Ground Return vias per Signal vias. For critical IFs, ratio is usually 1:1. For less critical IFs, several trace vias can share fewer return vias (i.e. 3:2 – 3 trace vias & 2 return vias).
Slots in Ground Reference Layer
- When traces cross slots in adjacent power or ground plane
- Return current has longer path around slot
- Longer slots result in larger loop areas
- Avoid slots in GND planes or do not route across them
Routing over Split Power Layer Reference Layers
- When traces cross different power areas on power plane
    - Return current must find longer path - usually a distant bypass cap
    - If possible, route traces w/solid plane (GND or PWR) or keep routes across single area
- If traces must cross two or more power areas, use stitching capacitors
    - Placing one cap across two PWR areas near where traces cross area boundaries provides high-frequency path for return current
    - Cap value typically 0.1uF & should ideally be within 0.1" of crossing