Project Examples of Hardware Redesign and Cost Optimization

Amarjit Bhatia

4.3-inch Control Panel Redesign

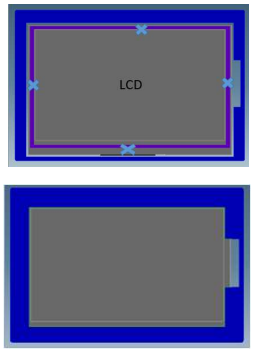
Amarjit Bhatia

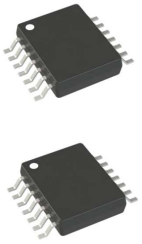
Control Panel touch redesign to low cost | $15M savings

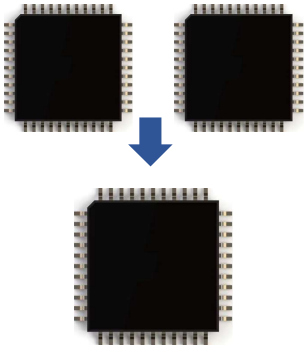
Sustainable solution

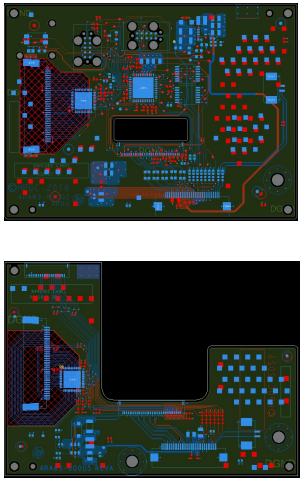
Complexity reduction

Lower cost implementation









Cost reduce Display to ITO Glass attach

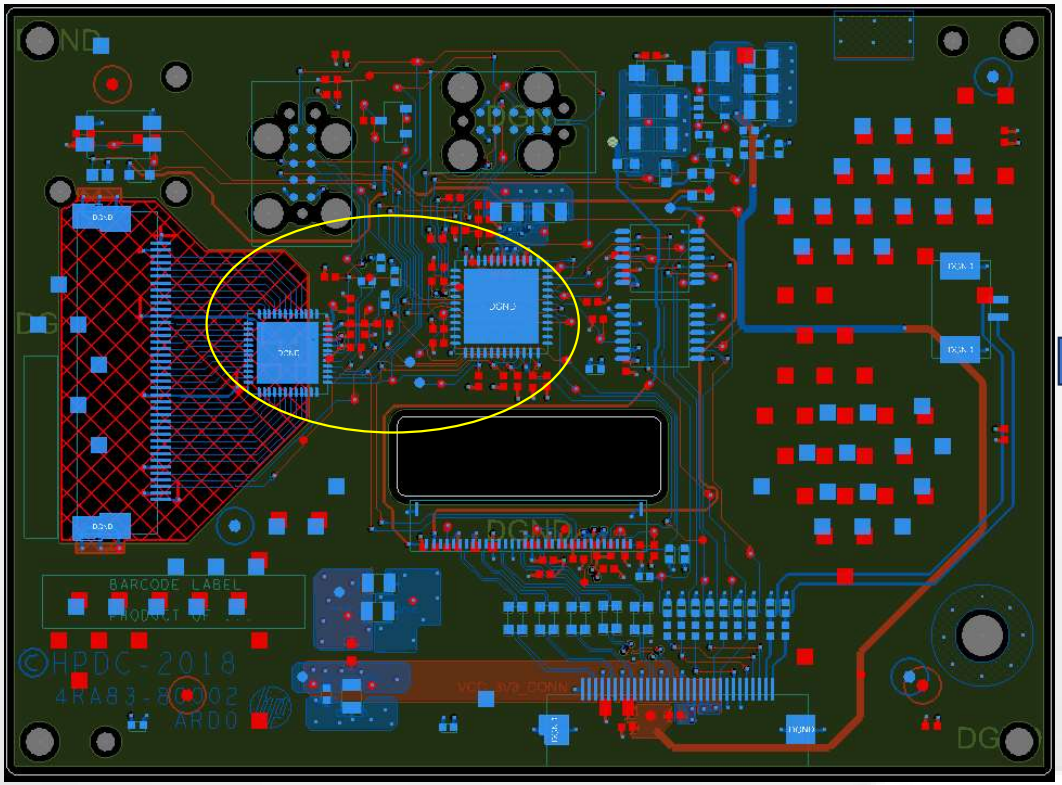
Remove Back bias buffers

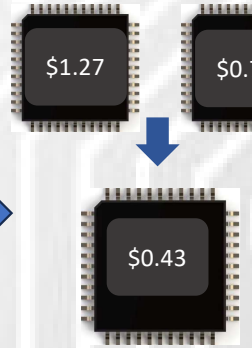
Two chip to single chip Solution Hardware and Firmware redesign

Redesign PCB to smaller size

Qualify lower cost speaker supplier

Capacitive touch 2 microcontroller to Single microcontroller |$1.58/unit savings





$1.27

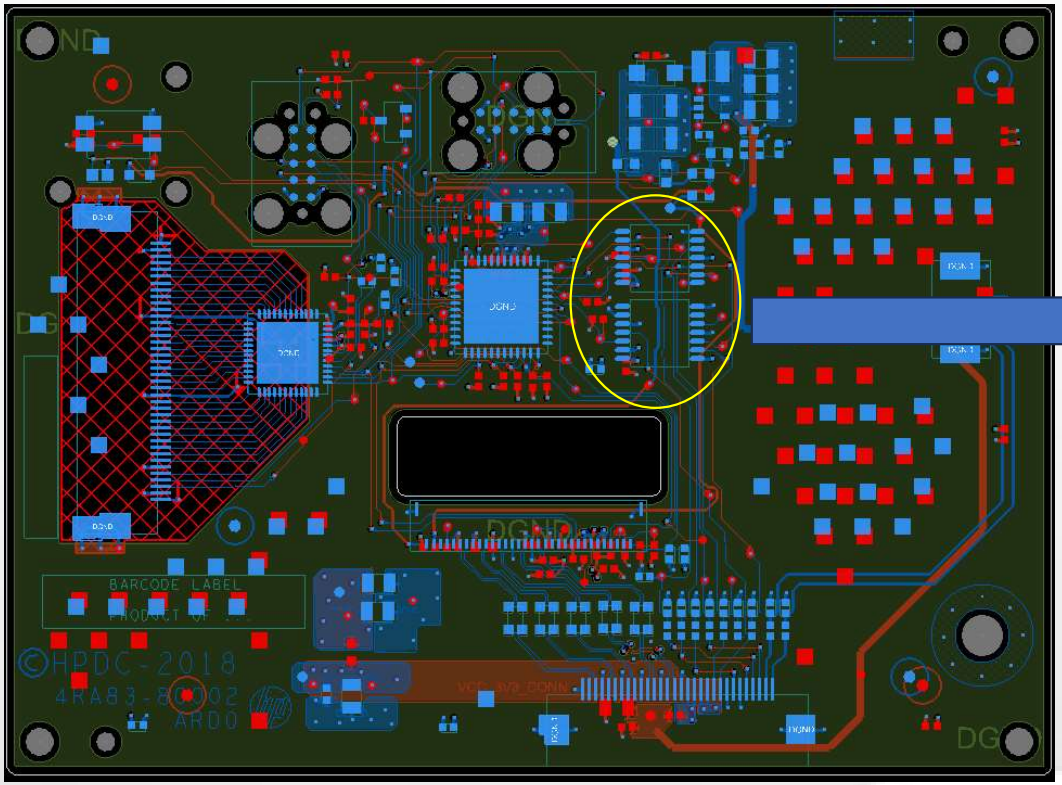
$0.74

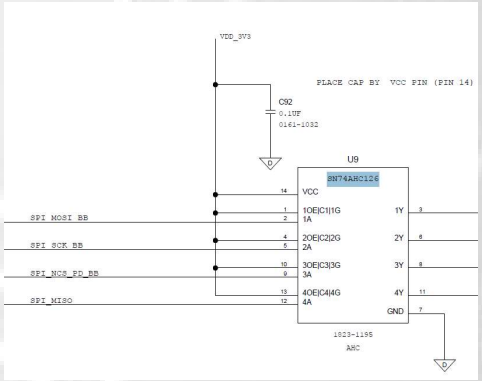
Total cost $2.01

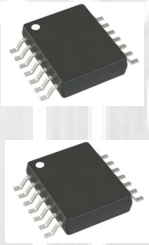
New cost $0.43

Two chip touch sensing to single chip Solution Hardware and Firmware redesign

Remove Back Bias Buffers| $0.20/unit savings

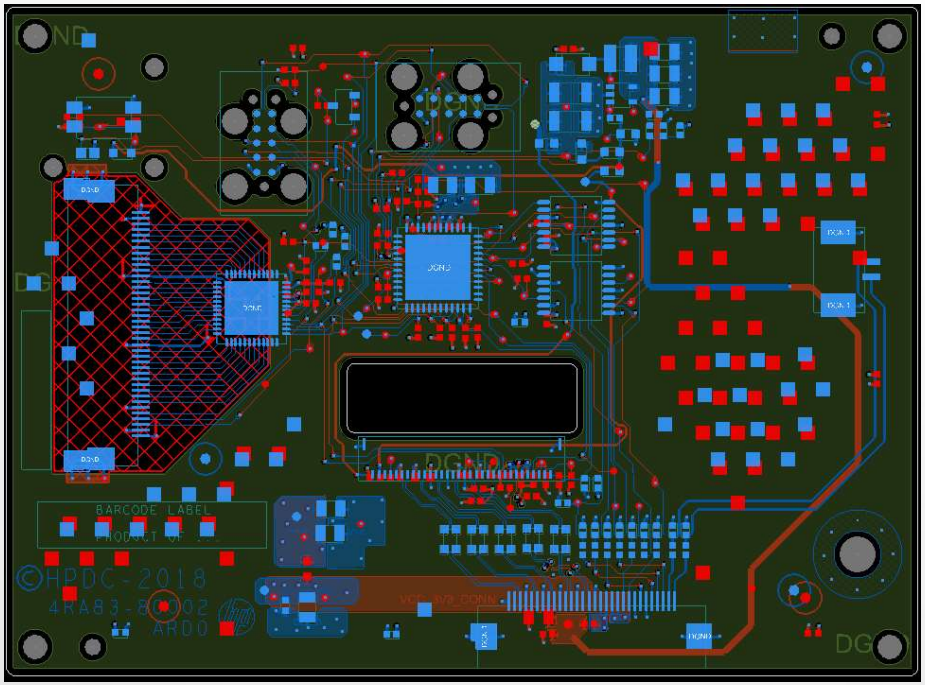


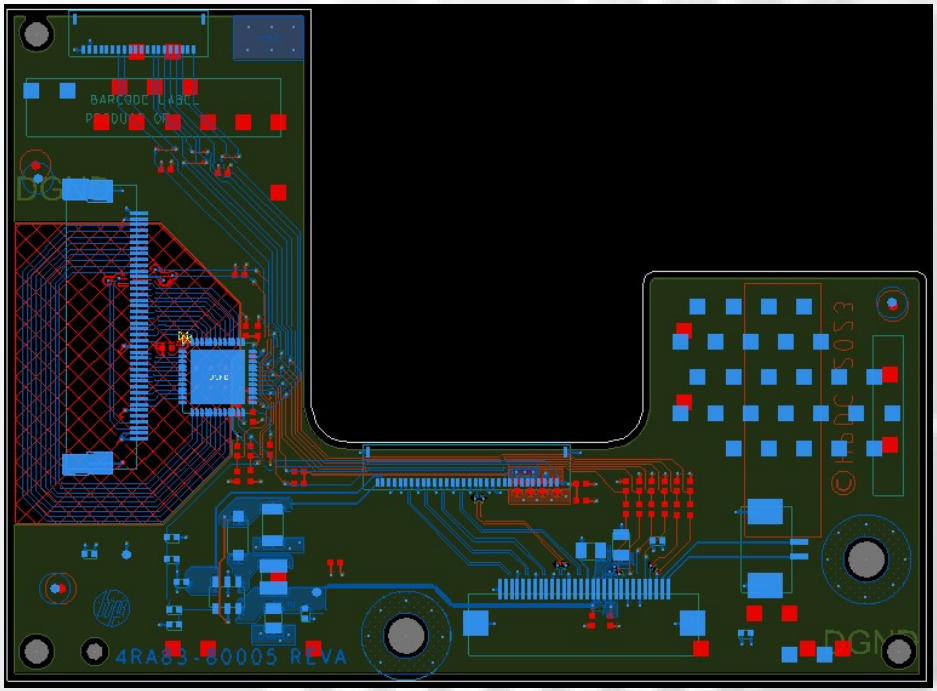




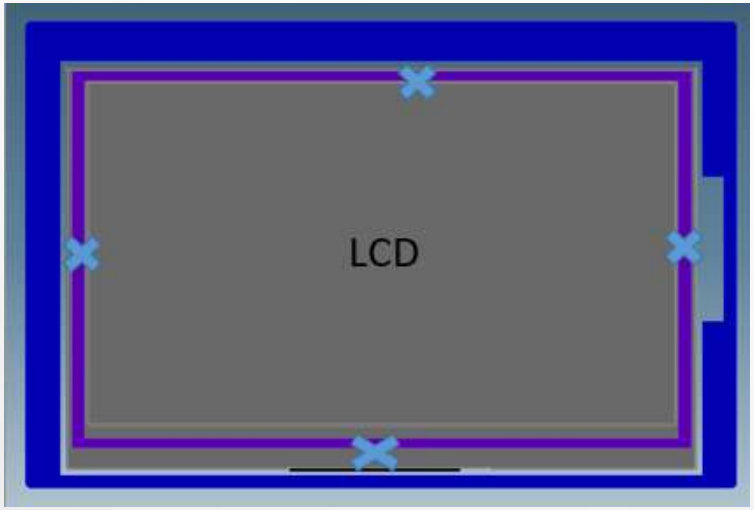
Remove Back Bias buffers while maintaining good signal Integrity

Redesign PCB to smaller nested PCB |Saving $0.38/unit





Use ITO adhesive to attach display | $0.10/unit

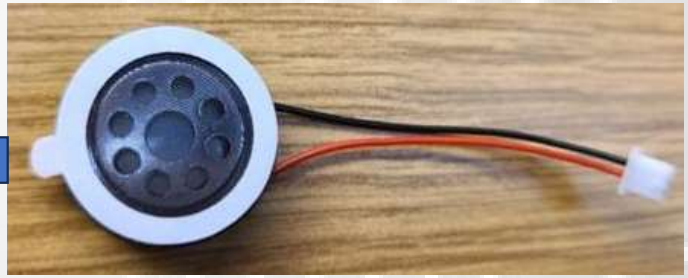


Touchscreen Adhesive enlarged by adding material to the inner dimension

Part Number	Description	unit cost	qty	Ext. cost
3SJ05-00004	Adhesive - LCD	0.034	2	0.069
3SJ05-00005	Adhesive - LCD Side	0.015	2	0.029
			Savings	0.098

Worked with the ITO supplier to grow ITO attach area, removed 4 inner adhesive strips and direct attach the Display to ITO glass

Qualified Lower cost Speaker | $0.14/unit



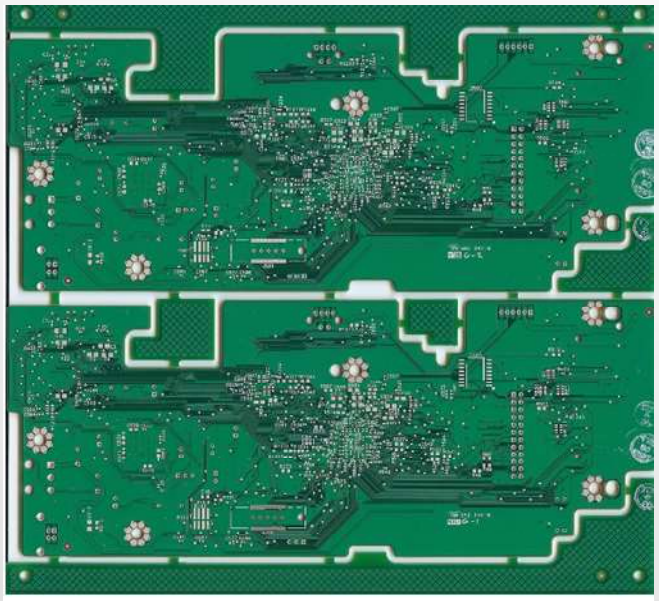
Collaborated with the supplier to design and qualify a speaker at a lower cost, while meeting the audio performance.

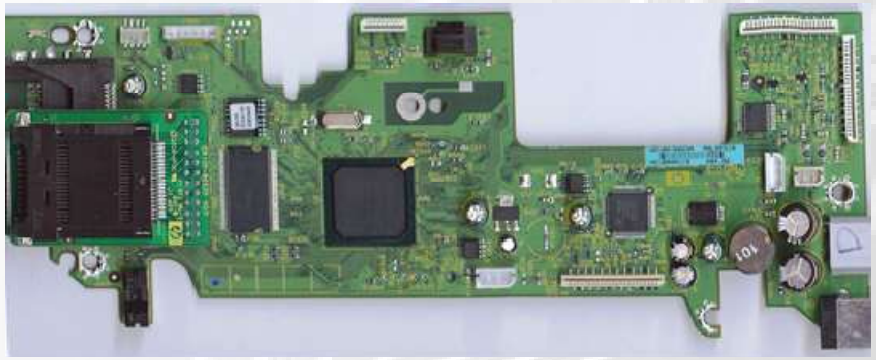
Main Logic board and PCA redesign projects

Amarjit Bhatia

Main Logic PCA redesign nesting of Photo card | $5M in savings

Original design and panel

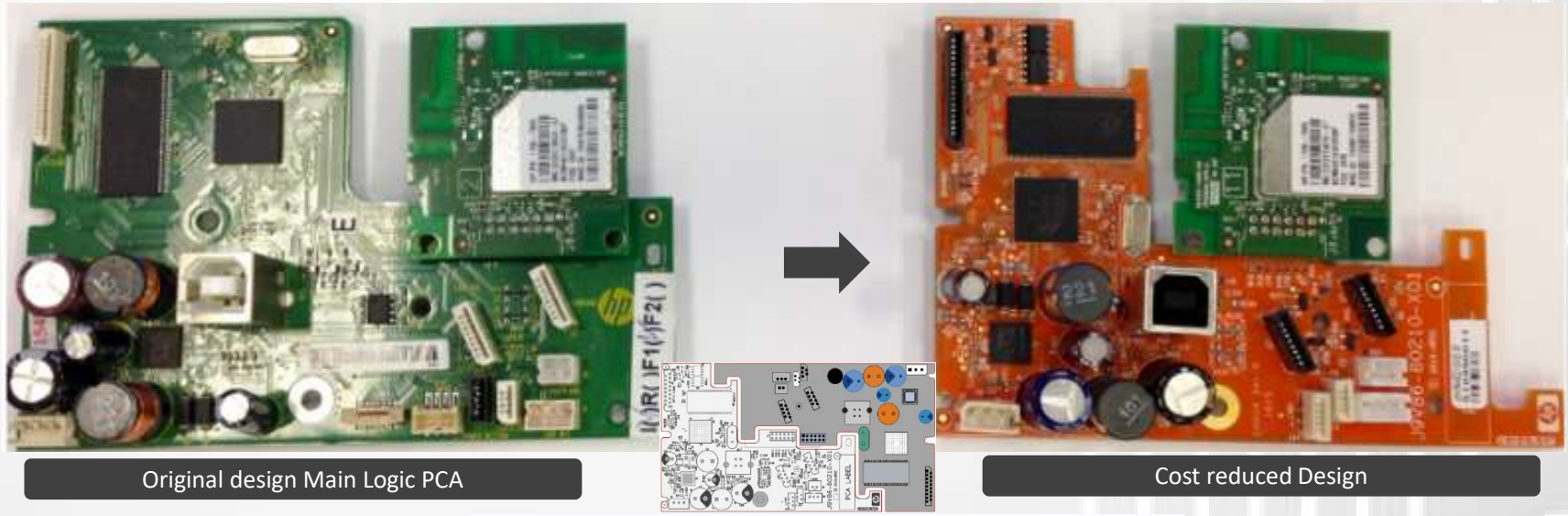




Cost reduced Design and Panel

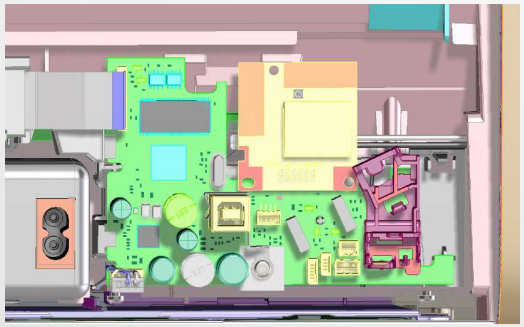
4 layer Photo card PCB nested

High Volume Product Logic PCA redesign to low cost | $1.6 M in savings



Original design Main Logic PCA

Cost reduced Design



Thorough study with Mechanical engineering for cable routing , fire enclosure, final assembly with the reduced cost board

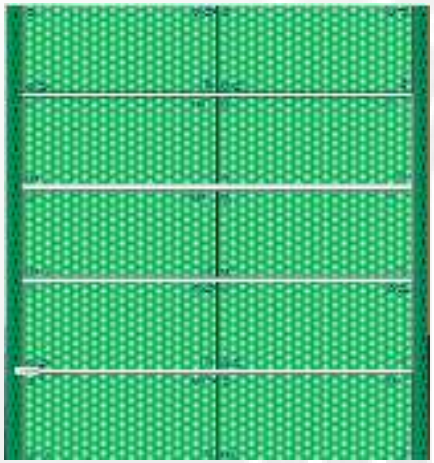
Control panel PCA Redesign | $1.32M in savings

Optimize Control panel PCB | 0.16/unit

Original CP design

Cost reduced Design

PCB Panel produces 16 PCBs compared to 10 before

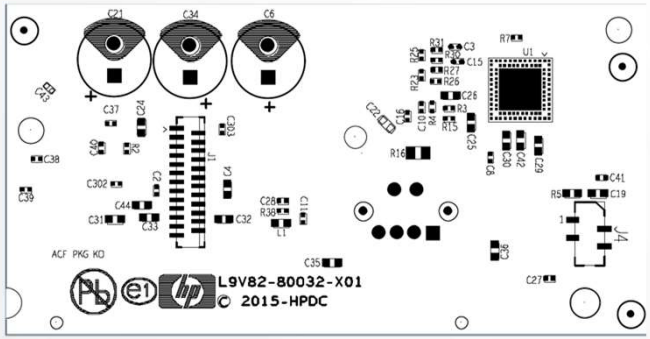


Original Design

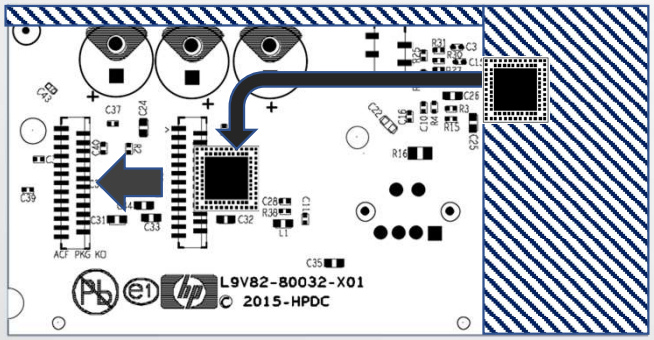
Cost reduced Design

Cost reduced control panel used on multiple programs generating $1.32M in savings

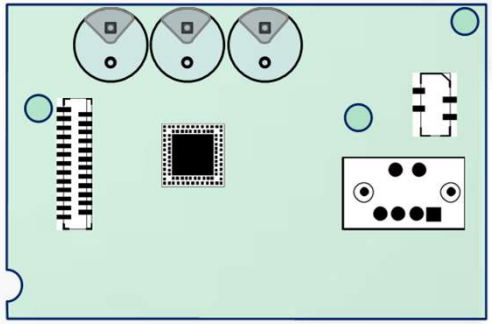
Carriage PCA redesign to smaller size | $2.5M in savings



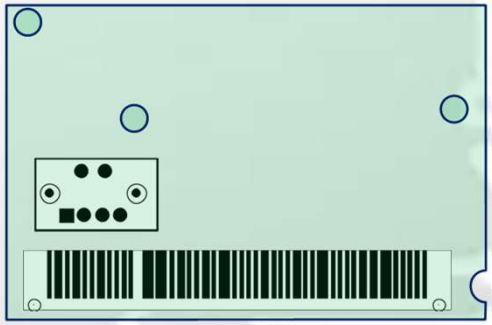
Original CP design

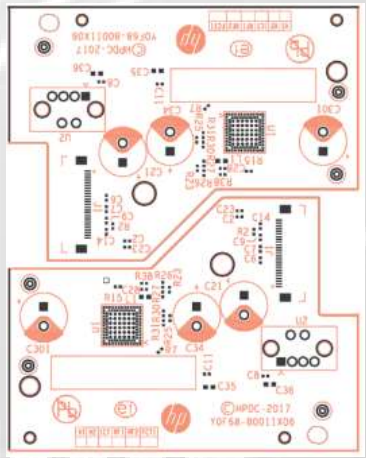


Cost reduction design



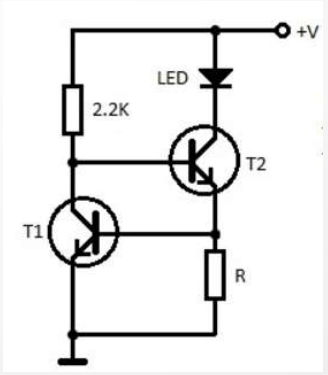
1st Round Cost reduction design

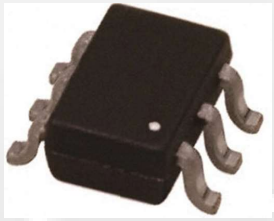




2nd round cost reduction design

Direct Drive Control panel LEDs | $2M savings



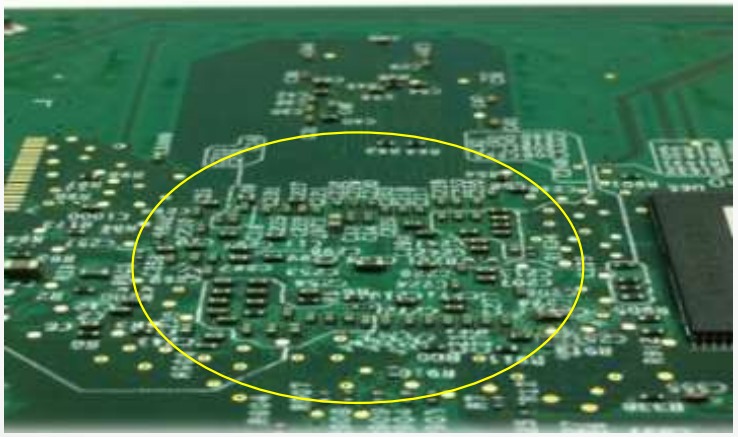


$0.10/unit savings :Remove transistor Drive circuits and directly drive LEDs with microcontroller GPIO

Component savings and optimization for cost

Amarjit Bhatia

Decoupling Capacitor EMC Optimization and Removal | $5M in savings



Pilot Program: Elvis CR

For our pilot program, we chose Elvis CR, of which we plan to build one million starting this summer.

We optimized the 3.3V PDN that started with 62 capacitors loaded.

Technical challenges that we overcame

- Matching simulations to measured results
- Determining the right frequency-dependent target impedance
- Choosing capacitor libraries that match simulations
- Incorporating S-parameter models for ASIC PDN
- Incorporating VRM models
- Defining tests to detect potential side affects of change

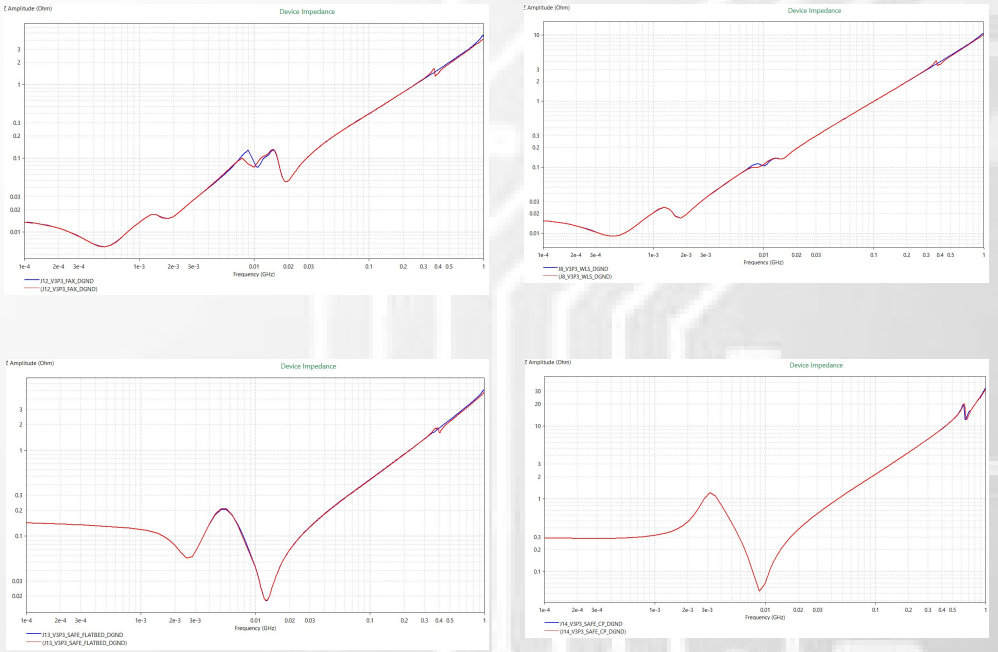
Impedance simulation using cadence Sigerity tools and collaboration with EMC team to optimize and reduce decoupling capacitors

- Elvis
- Chili
- Congo
- Congo Wireless
- Shaolin WL/ IA
- Wudang AIO/IA
- Naples Minus/IA
- Naples
- Naples Plus
- Naples Super
- Corfu/minus
- Corfu Plus

Decoupling Capacitor EMC Optimization and Removal | $5M in savings

Impedance simulation using Cadence Sigerity tool

C299	located along PCB edge
C301	located along PCB edge
C303	located along PCB edge
C304	located along PCB edge
C307	located along PCB edge
C308	located along PCB edge
C335	located along PCB edge
C339	located along PCB edge
C797	Under U101, Impedance plot is quite similar
C24	Under U1, Impedance plot is quite similar

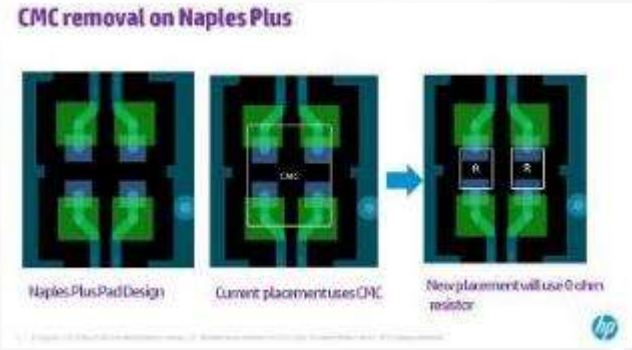


Original Simulation:

Removed caps Simulation:

Design improvement and removal of common mode chokes | $1.03M in savings

Common Mode Choke are noise suppression components used from Legacy designs, removed through design improvement and testing

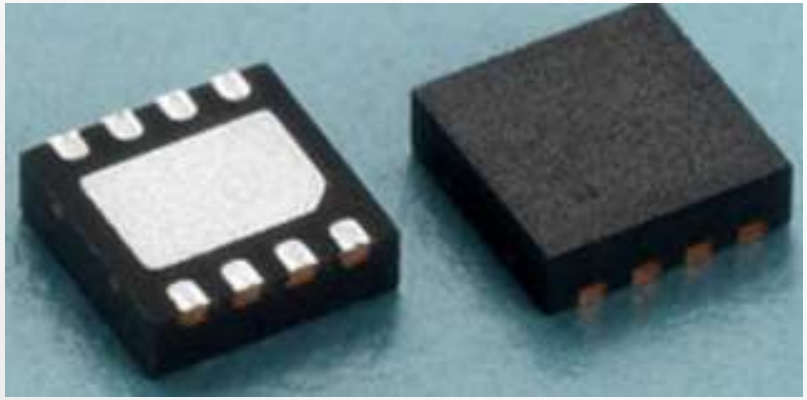


Improve trace routing add 0-ohm resistor overlap to remove common mode chokes

Improve PCB routing to remove Common mode chokes on ethernet and USB ports .

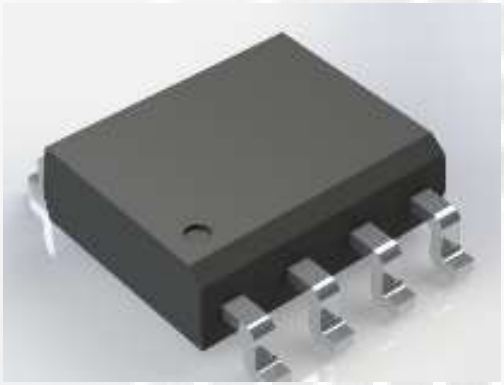
Change package on Pen security chip DFN-8 to SO-8| $2 M in savings

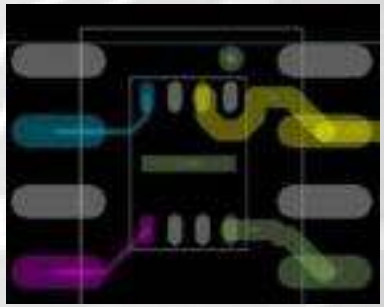
DFN Package Pen Security Acumen Chip



Change DFN to So8

10 cent cheaper : 8 Pin SO-8 package





Overlap nesting DFN to SO8 geometry in Layout on multiple programs, qualified and ECO design change into production

Collaborated with ST to redesign the security chip package, transitioning from DFN8 (Dual Flat No Leads) to SO8 (Small Outline-Leads). Successfully qualified across multiple programs, achieving a cost reduction of $0.10 per unit, resulting in total savings of $2M over two years.

Change MLCC from single to quad Packs | Savings $5M+

Change Individual MLCC capacitors to Quad Pack

Quad Packs MLCC

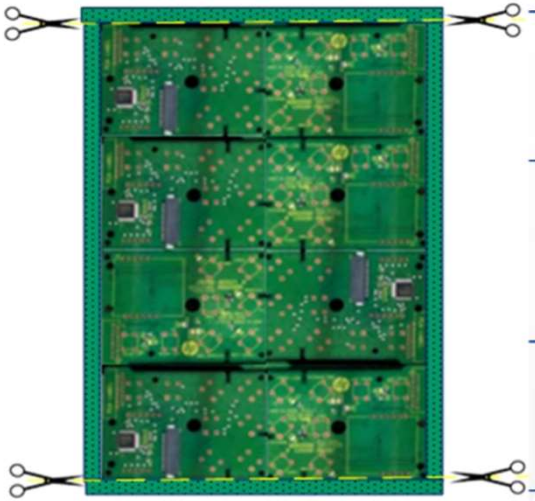
Product	Volume	Placement Cost Saving	Total EOL Saving
Corfu	2440083	$0.203	$494,117
Corfu IA	553222	$0.203	$112,027
Corfu Minus	58240	$0.203	$11,794
Corfu Plus	1466057	$0.243	$356,252
Corfu Plus IA	332082	$0.243	$80,696
Palermo Fast	2000000	$0.421	$842,400
Palermo Minus	3000000	$0.316	$947,700
Palermo Super	1000000	$0.494	$494,100
Verona	4000000	$0.235	$939,600
Verona Plus	2000000	$0.275	$550,800
Weber	2000000	$0.920	$1,840,000
		Total EOL Saving	**$6,669,486**

Serial #	Part Number	Description
1	0161-1032	CAP-FXD 0.1UF +-10% 10 V CER X5R ROHS
2	0161-1057	CAP-FXD 470PF +-10% 50 V CER X7R ROHS
3	0161-1093	CAP-FXD 22PF +-5% 50 V CER C0G ROHS
4	0161-1171	CAP-FXD 0.1uF +-10% 50V CER X7R ROHS
5	0161-1227	CAP-FXD 0.01UF +-10% 25 V CER X7R ROHS
6	0161-2309	CAP-FXD 1000pF +-10% 50V CER X7R
7	0697-1463	RES 16K +-1% .063W TC=0+-200 ROHS
8	0699-7203	RESISTOR 100 +-1% .063W TKF ROHS
9	0699-7215	RESISTOR 10K +-1% .063W TKF ROHS
10	0699-7513	RES 10 OHM 1% .063W TKF TC=0+-200 ROHS

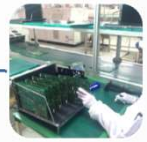
Process improvement for Savings

Amarjit Bhatia

4 Tab to 2 Tab Panel Conversion Factory process change |$1M /year savings

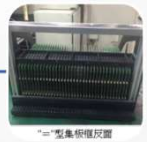


Extra Tabs on PCB's Increase Per PCB cost to HP



"4 side tabs PCBs" used in Production due to Foxconn process and fixture limitations

Design for supply chain team engaged with Foxconn and CDPS to understand their Fixtures and process



Process Improvement and fixture redesign with Foxconn to run production with "2 side tab" PCB's

Estimated minimum $500K+ savings year after year at Foxconn from 2 Tab PCB's

		FY'16	FY'17	FY'18
Weber MPCA		$132,638	$280,373	$101,881
Weber Base CP	$0.027	$30,409	$64,279	$23,358
Weber Mid CP	$0.035	$39,572	$83,648	$30,396
Shaolin WL	$0.027	$37,394	$99,568	$3,803
Lhasa Wl CP	$0.022	$10,611	$36,118	$15,301
	Savings/Year	$250,624	$563,986	$174,739
	Total Savings	**$989,349**		

Remove the high-temperature regulation label and apply direct silkscreen certification on the PCB| $0.5M/year

Remove high temperature Regulatory label

Silkscreen Logos and Regs certification on the PCB

Worked with the Regulatory compliance team and Wifi card supplier to remove the high temperature regs label and directly silkscreen Regs information and logos on the Wifi card