About Me – Amarjit Bhatia

I'd like to give a summary of my professional journey and the diverse roles I've undertaken over the past two decades.

My experience spans the full product lifecycle—from concept and design to manufacturing, quality, and cost optimization—driven by a deep passion for innovation, reliability, and process excellence.

I live in San Diego with my wife, who works for a university and is a health and wellness coach. Outside of work, I enjoy a variety of hobbies that help me unwind and stay creative. I maintain a vegetable and herb garden, which I find to be a meditative and rewarding task. Additionally, I love tinkering with IoT devices and home automation projects, and I'm always eager to dive into home improvement projects as a self-proclaimed handy person.

Career Highlights:

Electrical Hardware Design Engineer: Designed complex multilayer PCBs with digital, analog, and mixed-signal systems; Specialized in getting designs through functional reliability ,EMC/EMI compliance, working experience of rigid-flex PCB design using Altium and Cadence tools.

- **Quality Manager:** Led Quality Assurance & Quality Control functions to ensure robust QMS practices, field failure analysis, and regulatory compliance; drove root cause investigations and 8D/7-step corrective actions across global teams.
- **NPI Manager:** Directed New Product Introduction programs, aligning engineering, manufacturing, and supply chain teams to deliver successful product ramp-ups; ensured smooth transitions from design to high-volume production.
- **Design for Cost and Process Optimization:** Championed cost-saving initiatives through design-driven cost reductions, supplier benchmarking, and material changes; implemented scalable, efficient solutions to improve manufacturability and reduce BOM costs.

This blend of hands-on engineering and cross-functional leadership continues to shape how I approach challenges—with a balance of technical depth, quality mindset, and operational agility.

Global Hardware Quality Manager

Amarjit Bhatia - Quality management leadership overview

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Quality Management Leadership

Amarjit Bhatia
Global Quality manager

Sustaining engineering team
China, USA,
Singapore, Mexico

Quality system work
Factory badge
engineers

[redacted]
Quality Program Lead

Metrics visibility and initiative lead

[redacted]
Quality Program Mgr
QPM Lead
(Flextronics)

[redacted]
Quality Program Mgr
(Flextronics)

[redacted]
Quality Program Mgr
NKG QPM

[redacted]
Quality Program Mgr
(NKG)

[redacted]
Quality Program Mgr
EET PM
Foxconn QPM

[redacted]
Virtual Quality Program Mgr
(Foxconn)

[redacted]
Quality Program Mgr
(Foxconn CQ)

3 engineers engaged in factory Quality team , Full engagement form

[redacted]
Lead Data Analyst

[redacted]
EMEA regional QE

[redacted]
Process engineer

[redacted]
EMEA regional QE

[redacted]
Data Analyst
(Contract)

[redacted]
EMEA regional intern

[redacted]
Quality Program Mgr
(Foxconn LH)

[redacted]
Regional QE Lead
Americas regional QE
Pentane Quality

Flex Quality team

NKG Quality team

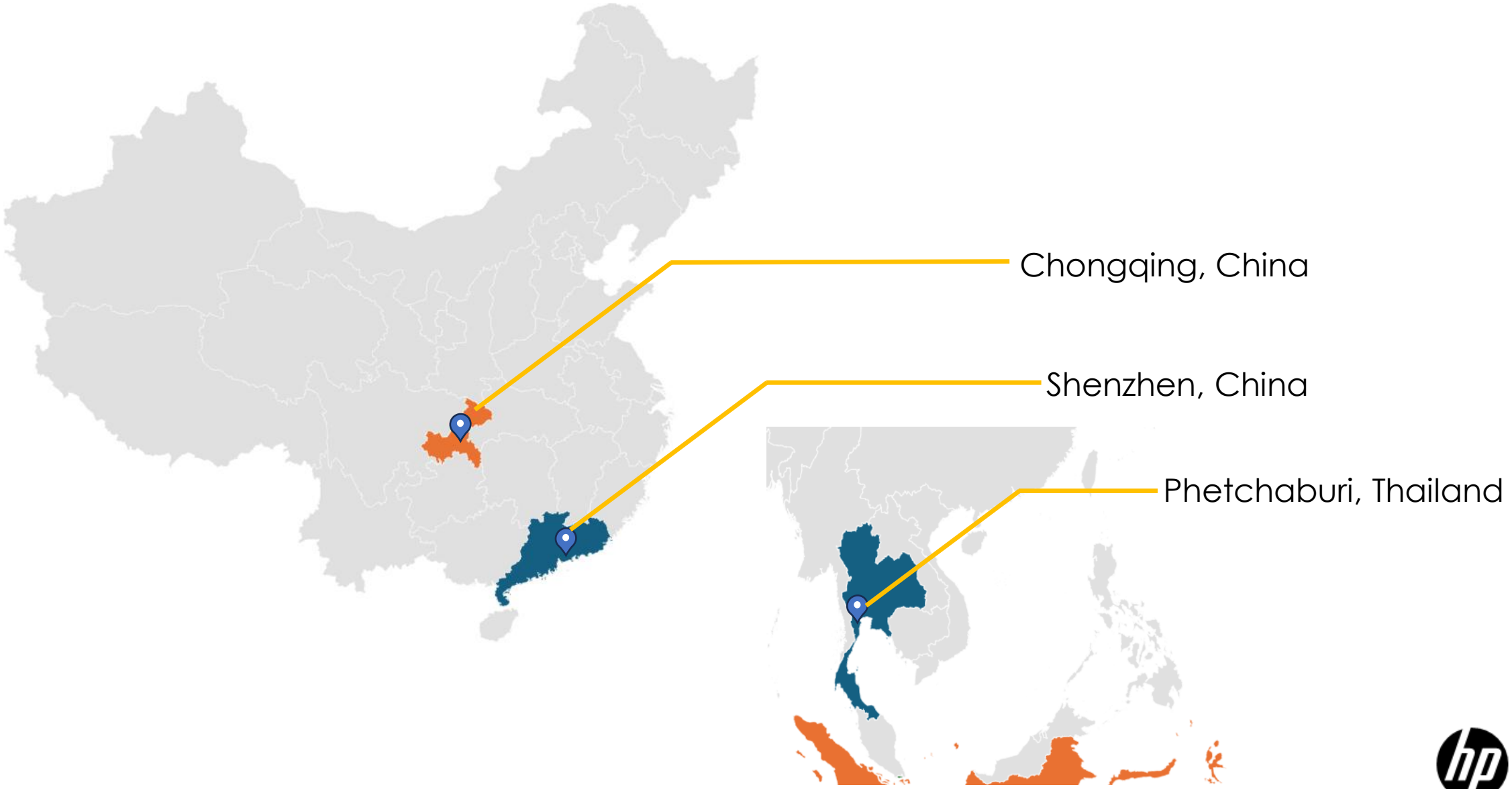
Foxconn Factory Quality team

Data and Process Team	Regional Quality team	Factory Quality team	Virtual Factory Badge Quality team

HP engineers

Factory Badge engineers

Global Supply Chain – Contract manufacturing partner locations



Product Quality & Sustaining management lifecycle

control action

control action

incident

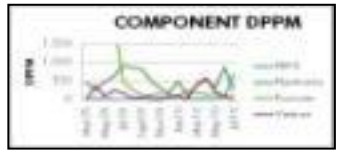
incident/ escalation

incident/ escalation

Product Development

Feedback Loops
- Field failure findings
- Direct Eng discussions
- Program team meetings
- Design reviews
- Pre-test alignment
- CSAT-NPI alignment
- Development test unit teardowns
- Design margin analysis

Component/ subassembly supplier



Feedback Loops
- CM part quality failure feedback

Contract Manufacturer

Feedback Loops
- Field failure findings
- HP audits
- Yield data
- Line issue resolutions

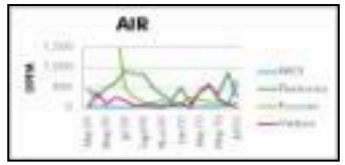
Distribution Center

Feedback Loops
- Post factory issue resolution

Retailer

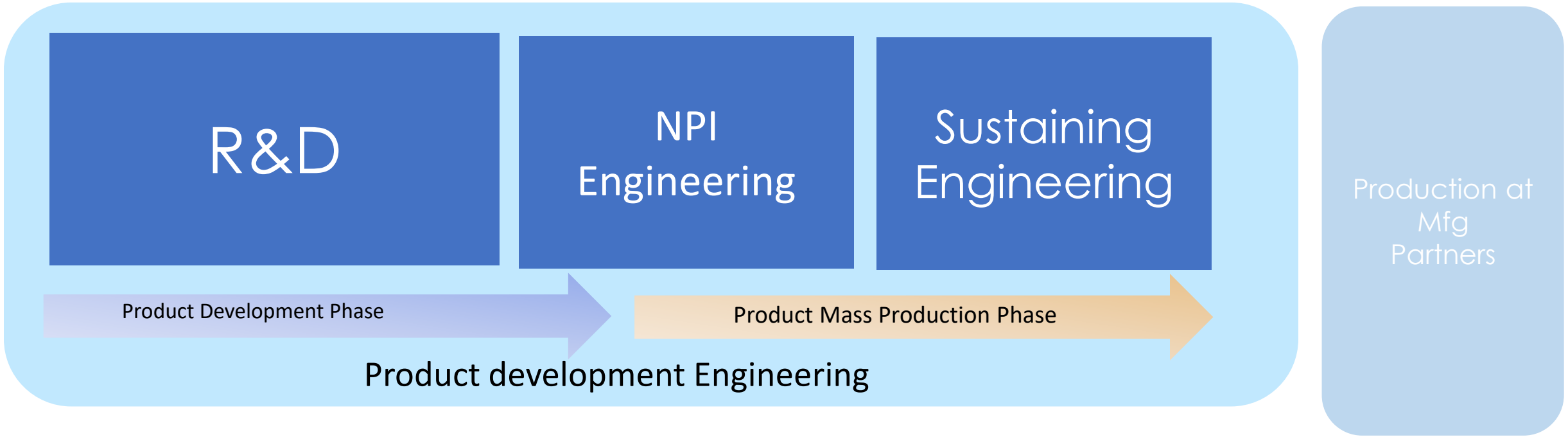
Feedback Loops
- CSAT escalations

End Customer/ Key Account



Feedback Loops
- Call notes analysis
- Field failure analysis
- SASH data
- HP product forums

Development to Manufacturing



Organizational roles from Development to Manufacturing

R&D
- Product knowledge transfer
- Product Issue resolution
- Product design stability
- Critical processes

NPI Engineering

Bring design into mass production
- Stability
- Scalable
- Leverage & Reuse

Engineering collaboration with R&D.
- Design reviews
- Design for Manufacturing
- Development of manufacturability solution
- Drive CM's readiness in delivering on operation-excellence

Capacity mgmt and installation
- Parts & Lines qualification

Sustaining Engineering

Current Product Engineering
- Customer issue identification and resolution
- Factory issue resolution
- Field Failure Analysis data interpretation
- DFX input
- Issue resolution communication to generating organization

Factory/Process Engineering
- Factory support, yields, line stops, process issues
- CM common process setup

Assurance of Supply
- Assurance of Supply qualifications on current products, plans and execution

Budgeting
- Current product tooling and evaluation expense budgeting

PCM-Product Cost Management
- Evaluation & Operating Supply
- Direct Labor /Indirect Labor Head Count validation

Planning
- Scenario planning
- Nominal & strategic capacity plan
- Demand and supply forecasting

New Product Program Management
- NPI program management
- Proto Build/Schedule
- Ramp plan
- PLC build checkpoints

Procurement and Sourcing
- Tool qualification schedule
- Part First Article reporting
- Tooling budget management
- Part tool Capacity installation plan

Manufacturing and Material Ops
- PSL qualification
- AOS strategy
- Proto build material readiness
- Integrated capacity plan

Reliability and compliance Engineering
- Reliability and regulatory qualification and submission

Manufacturing Test Engineering

Manufacturing Test Strategy
- Strategy elaboration
- Manufacturing test plan

Manufacturing Test Engine
- Test engine maintenance and enhancement

NPI Program team support
- Test script generation, a product development tool that evolves into the main manufacturing test

Factory Support
- Test changes for yield improvements and/or new failure mode detection

Asset Support
- Test and development support by asset

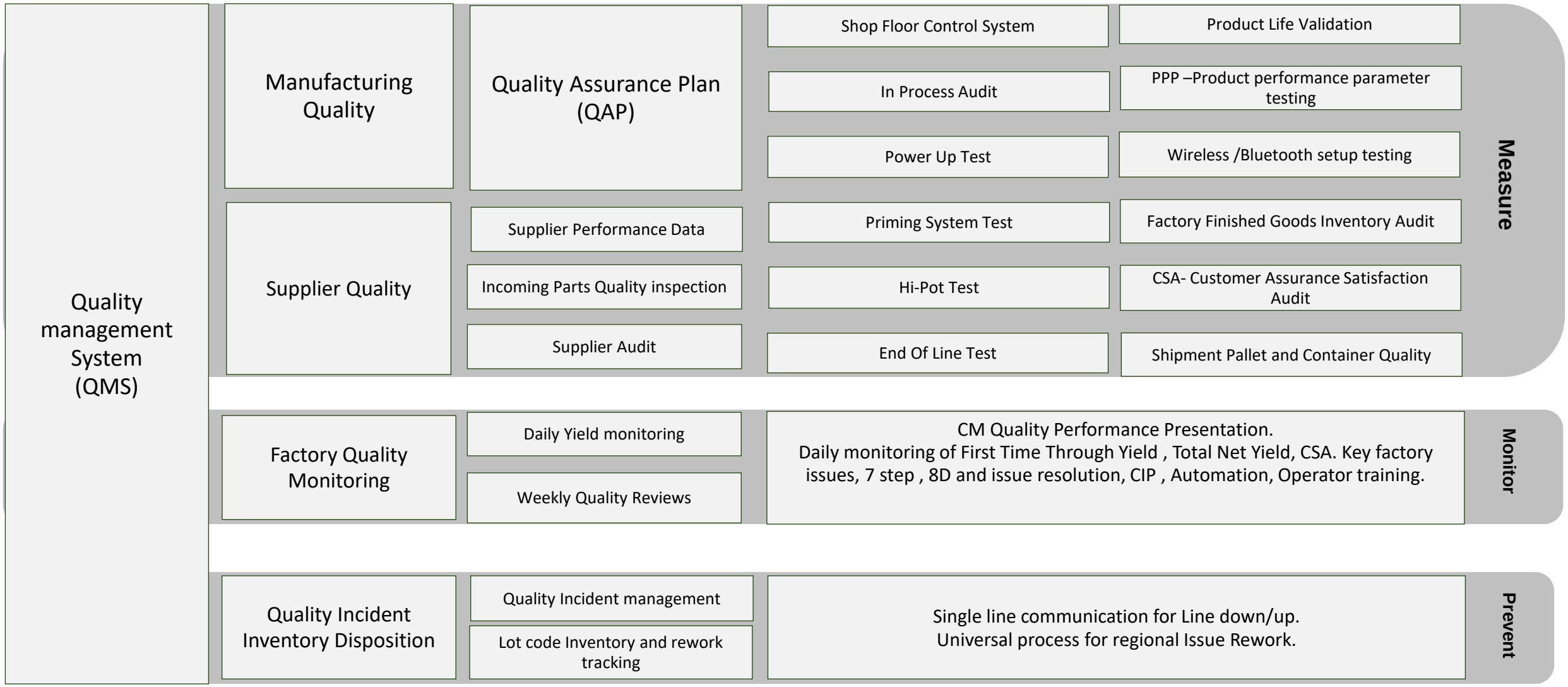
Quality Engineering

Quality System
- Quality Assurance Plans
- Factory Audits
- Quality System monitoring and corrective actions

Regional Retouch
- Rework Procedures
- Technical Management
- Rework monitoring and reporting

Data acquisition & management
- Customer data acquisition and transformation
- Field Failure Analysis data management

Quality System



NPI Manager - New generation product launch management

Amarjit Bhatia

NPI Manager for 5 product launches

ENVY 5020

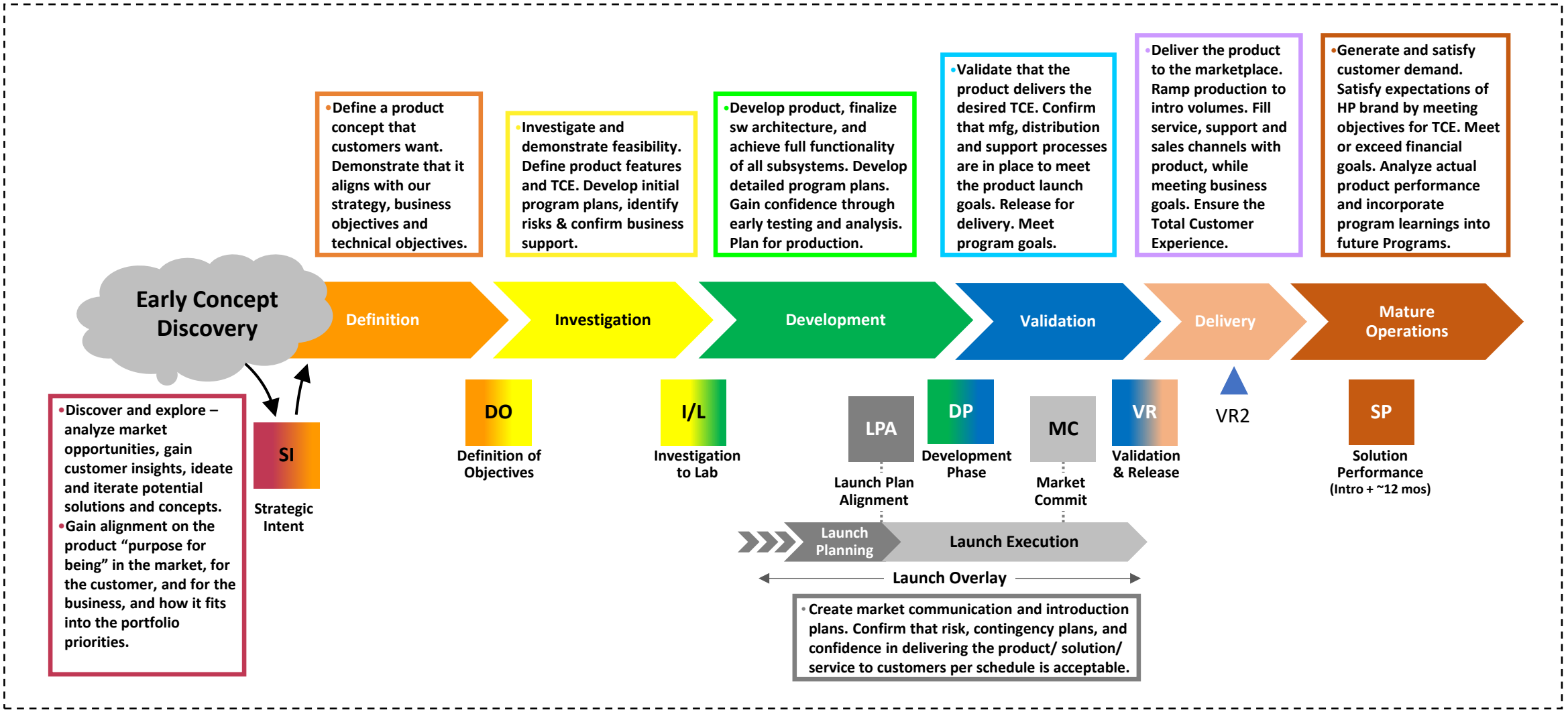
OfficeJet 5220

ENVY 6255

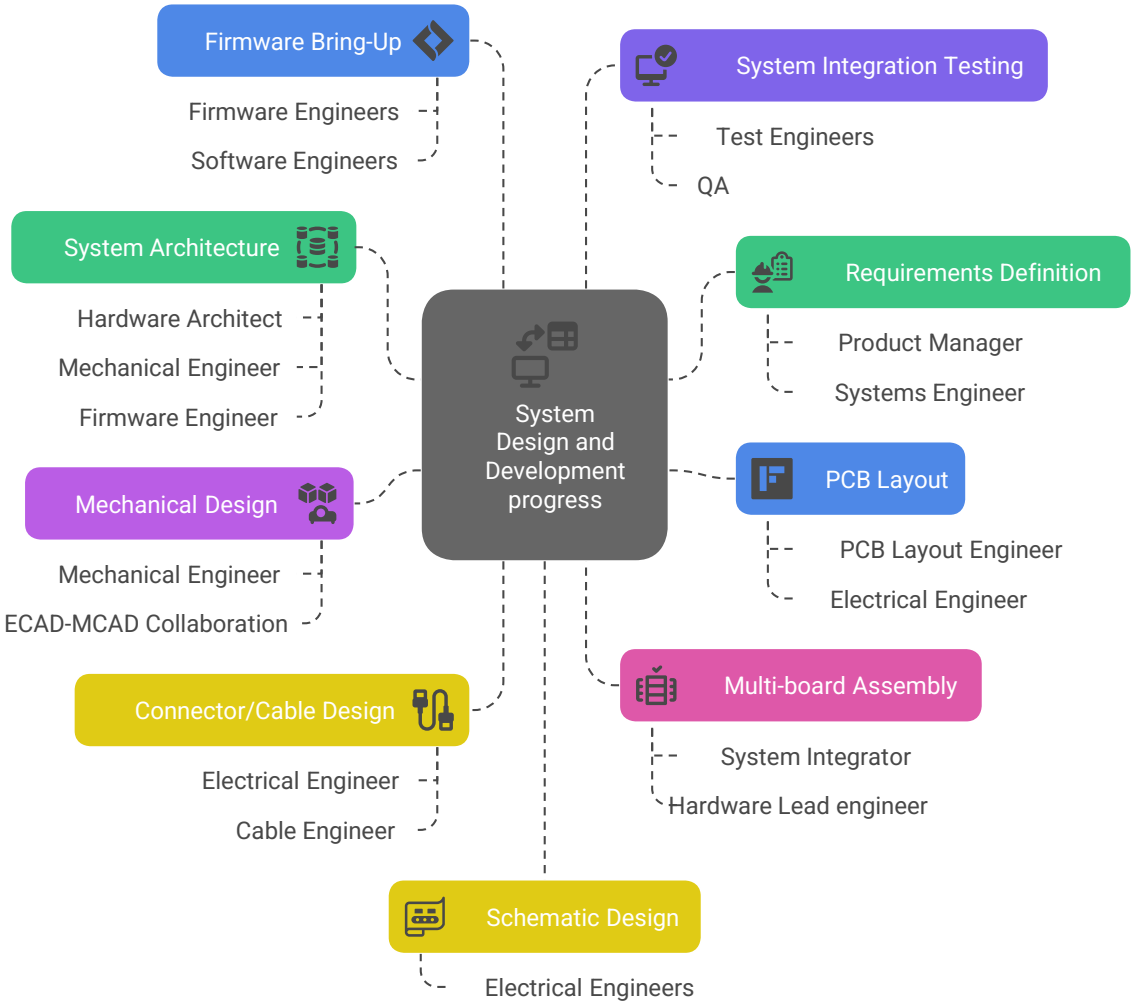
ENVY 7155

ENVY 7855

Leadership in Phase review Management | Ideation to production launch



Managing integrating and reporting development Progress



Tracking and keeping teams moving through development metrics

Demonstrated Technical Program Leadership

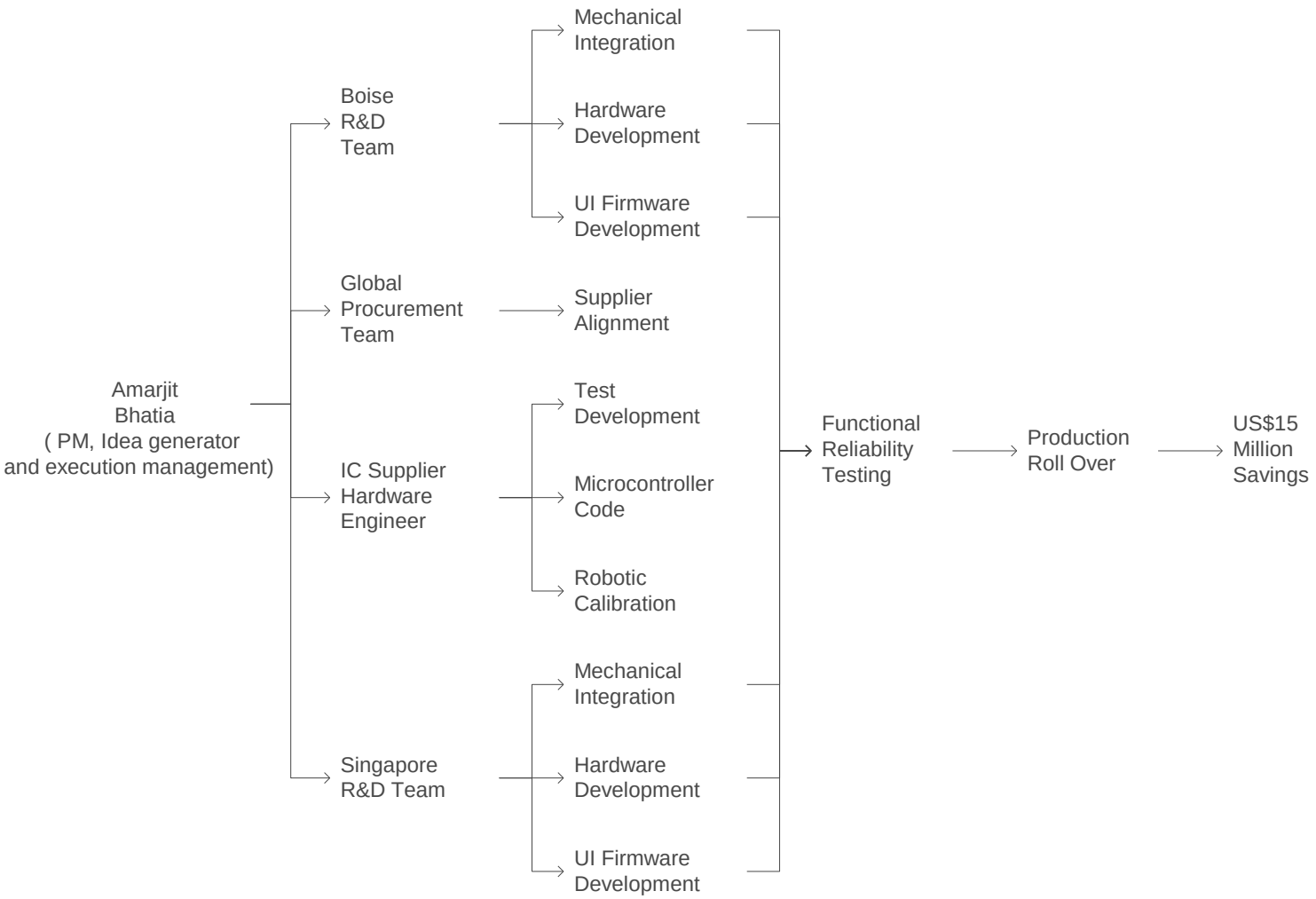
Hardware Redesign and Cost Optimization

Examples of Design for Cost projects executed by Amarjit Bhatia

4.3-inch Control Panel Redesign

Amarjit Bhatia

Amarjit's Project Management Flowchart



Managed global teams to get savings

Amarjit Bhatia
Program manager- Cost reduction Idea generator & Lead engineer

Ken /Cameron
Mechanical integration engineer

Amarjit /George Hardware Co-development (Boise)

Jose Firmware UI Engineer (Boise)

Boise Laserjet Product development team

Functional Reliability and EMC testing Boise products

Production roll over at Cannon and Jabil for Laser jet

mCore new touch IC supplier

Test development robotic calibration and touch firmware

$15M

Amarjit aligned with Global Procurement commodity team

Tiong Chiong
Mechanical integration Singapore

Amarjit /Min Cong Co-development Singapore

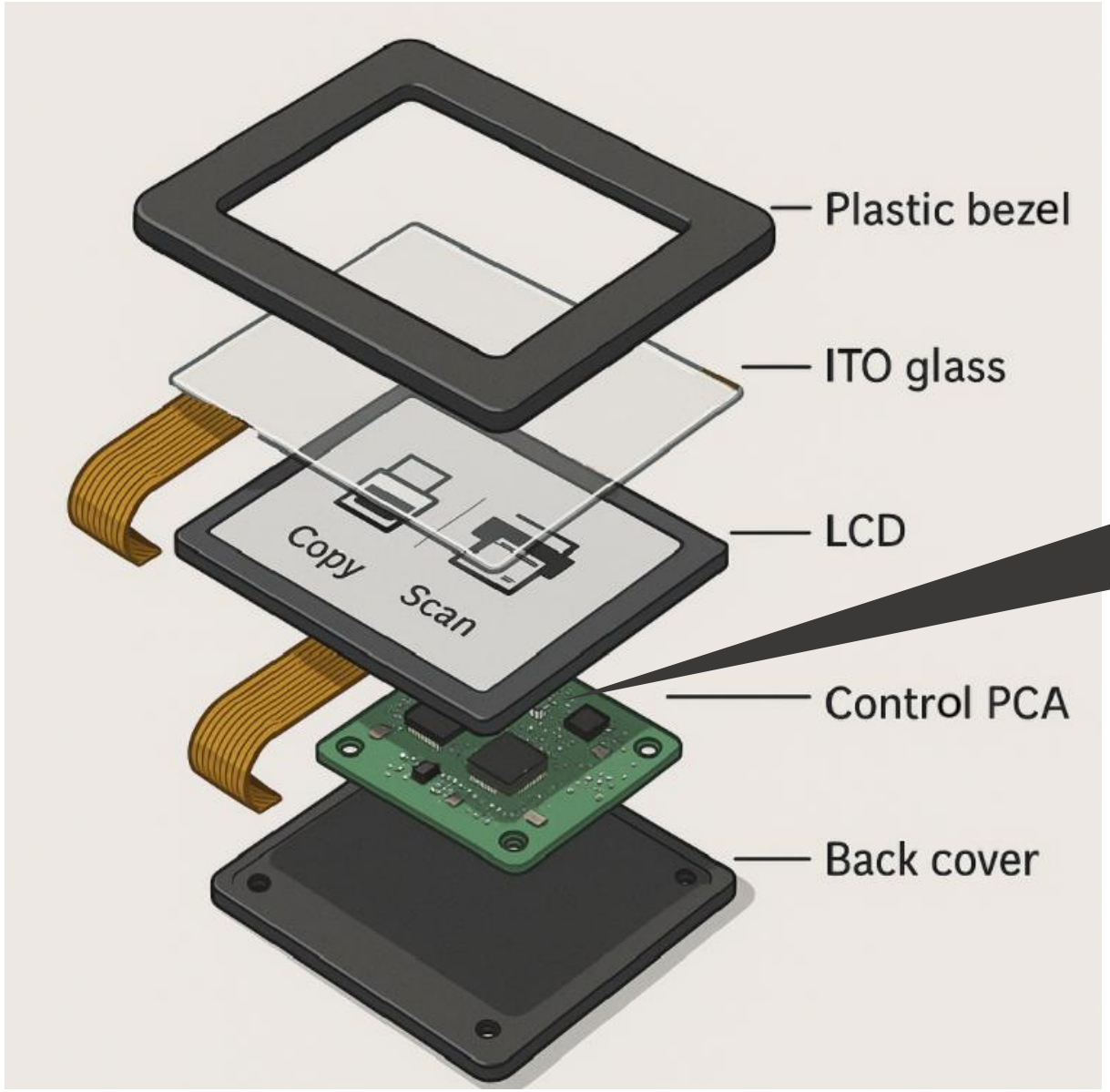
Shia Firmware UI Engineer Singapore

Singapore Inkjet Product development team

Functional Reliability and EMC testing Singapore products

Production roll over at Foxconn and NKG for Inkjet

Control Panel Architecture | Redesign touch to low-cost



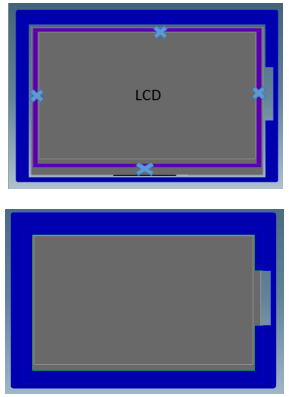
Redesign touch sensing circuit and firmware to lower cost implementation

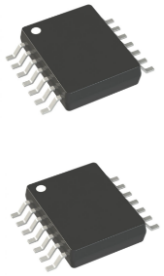
Control Panel touch redesign to low cost | $15M savings

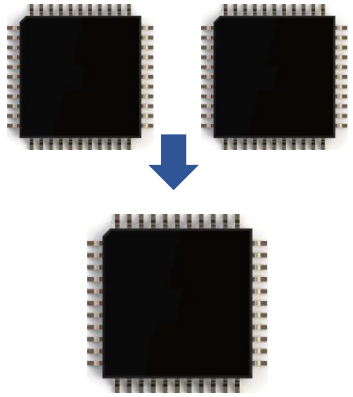
Sustainable solution

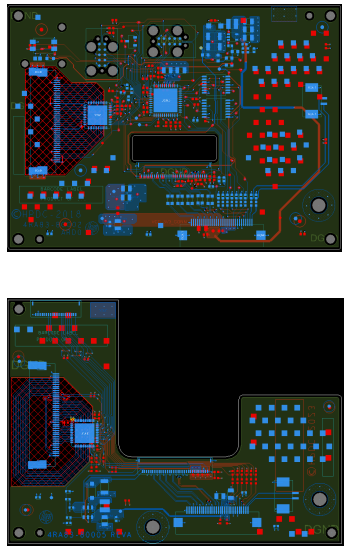
Complexity reduction

Lower cost implementation









Cost reduce Display to ITO Glass attach

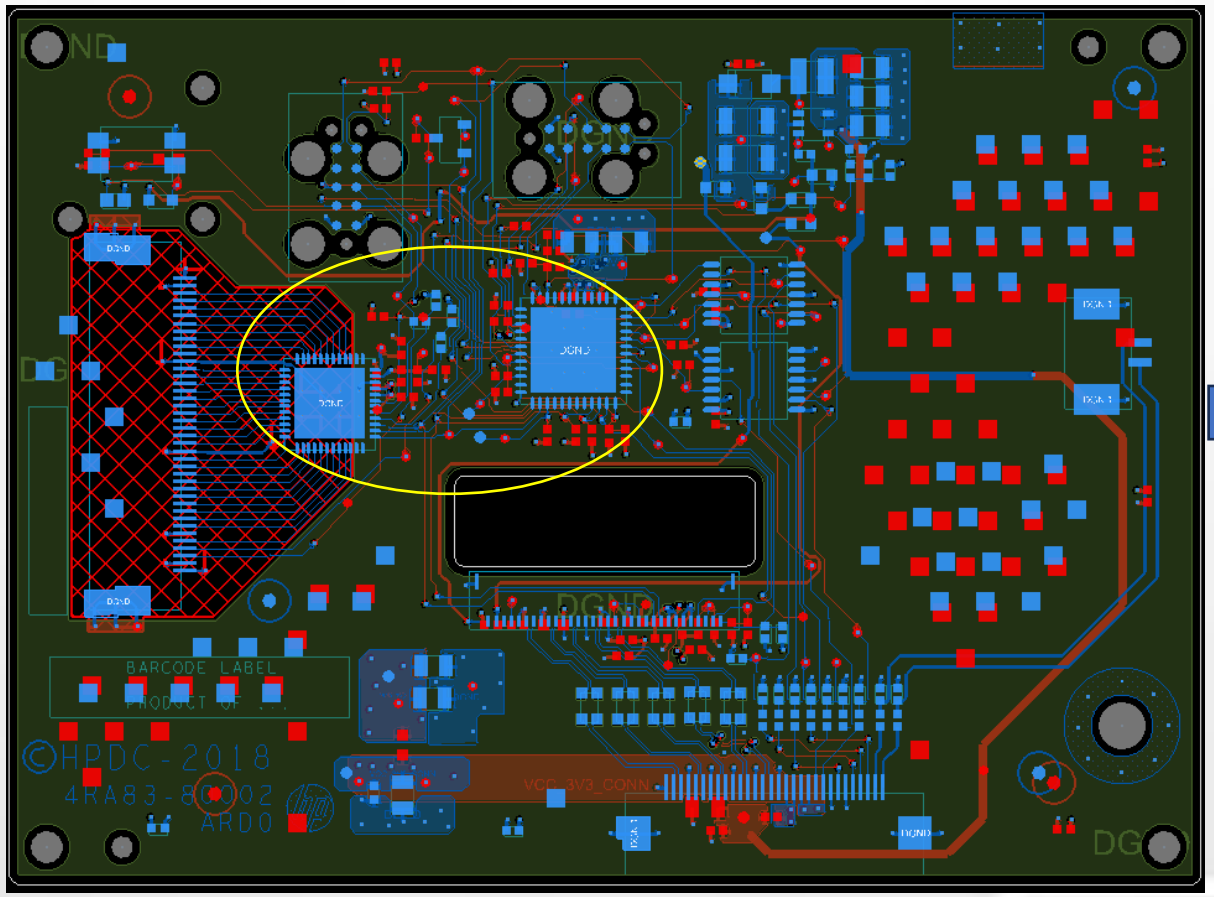
Remove Back bias buffers

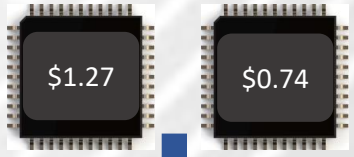
Two chip to single chip Solution Hardware and Firmware redesign

Redesign PCB to smaller size

Qualify lower cost speaker supplier

Capacitive touch 2 microcontroller to Single microcontroller |$1.58/unit savings



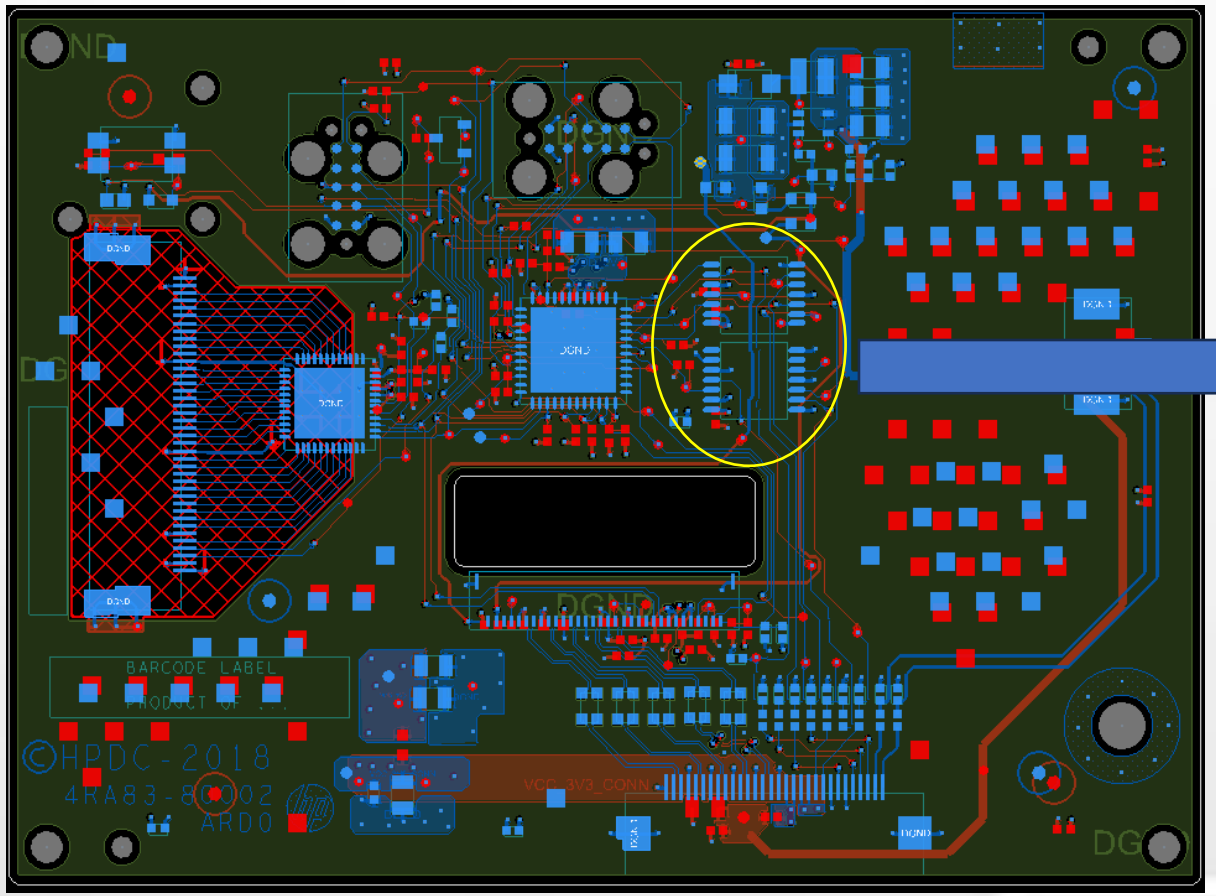


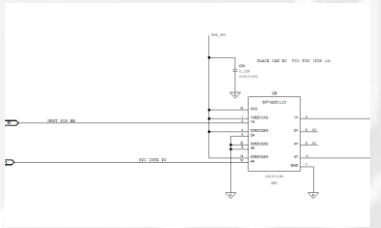
Total cost
$2.01

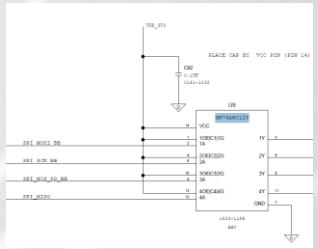
New cost
$0.43

Two chip touch sensing to single chip Solution Hardware and Firmware redesign

Remove Back Bias Buffers| $0.20/unit savings



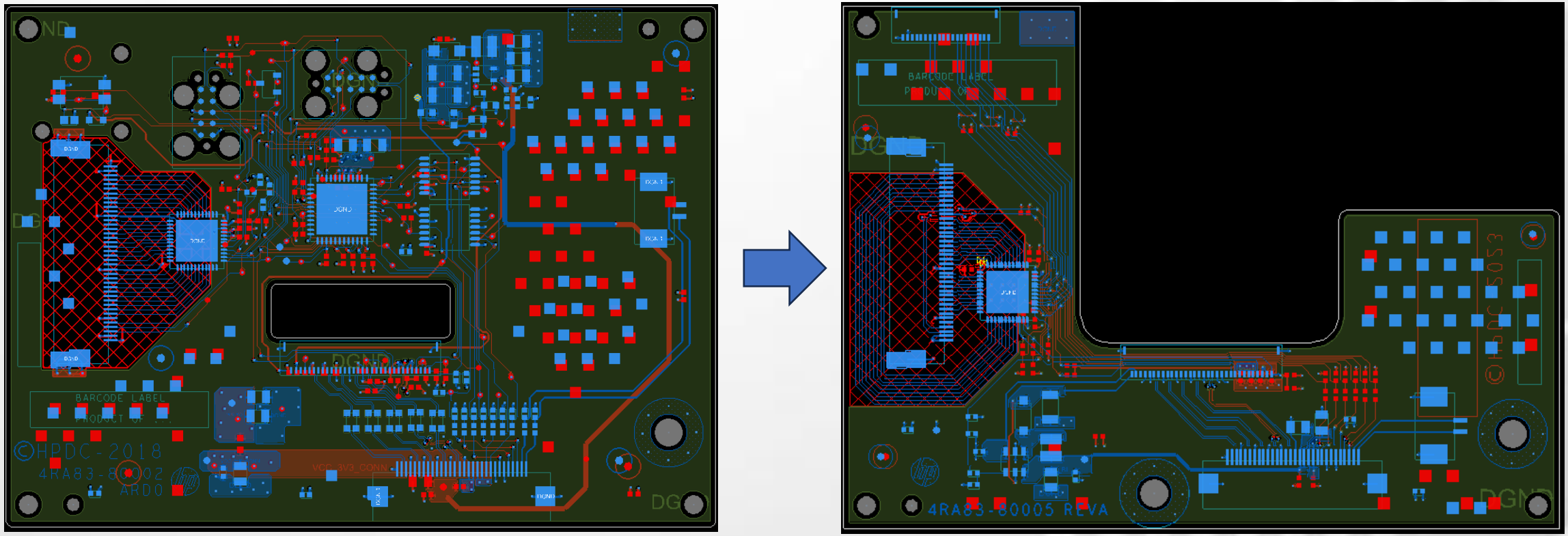




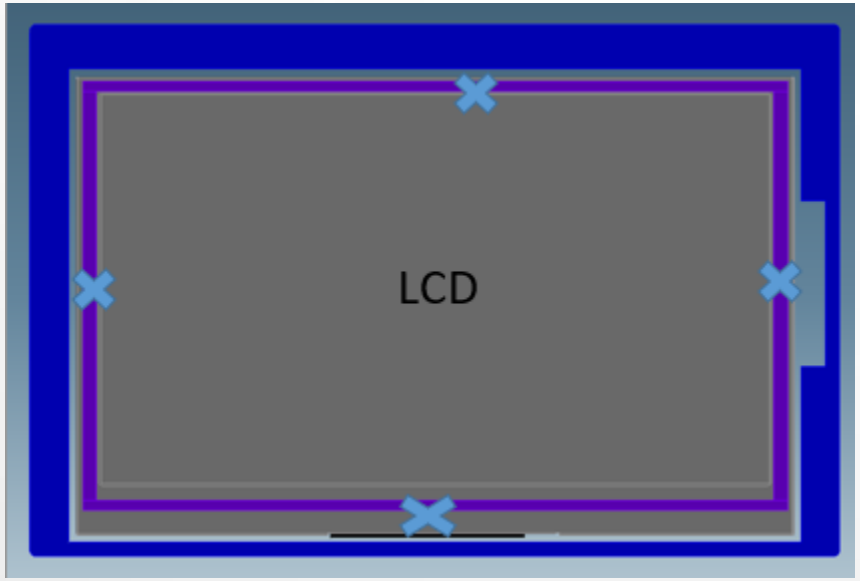
INPUTS		OUTPUT
OE	A	Y
L	X	Z
H	L	L
H	H	H

Remove buffers while maintaining good signal Integrity

Redesign PCB to smaller nested PCB |Saving $0.38/unit



Use ITO adhesive to attach display | $0.10/unit

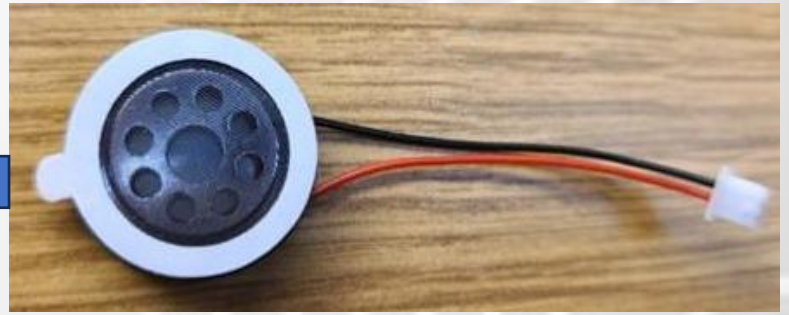


Touchscreen Adhesive enlarged by adding material to the inner dimension

Part Number	Description	unit cost	qty	Ext. cost
3SJ05-00004	Adhesive - LCD	0.034	2	0.069
3SJ05-00005	Adhesive - LCD Side	0.015	2	0.029
			Savings	0.098

Worked with the ITO supplier to grow ITO attach area, removed 4 inner adhesive strips and direct attach the Display to ITO glass

Qualified Lower cost Speaker | $0.14/unit



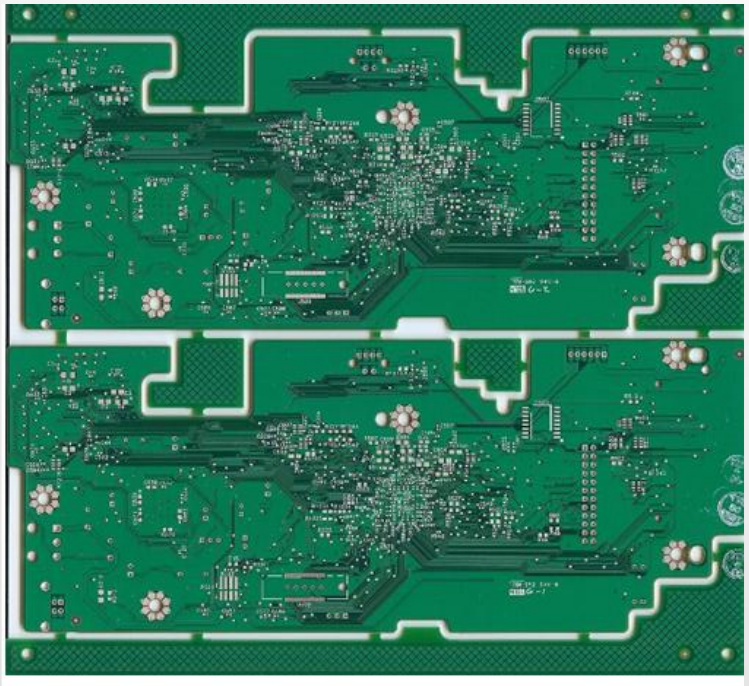
Collaborated with the supplier to design and qualify a speaker at a lower cost, while meeting the audio performance.

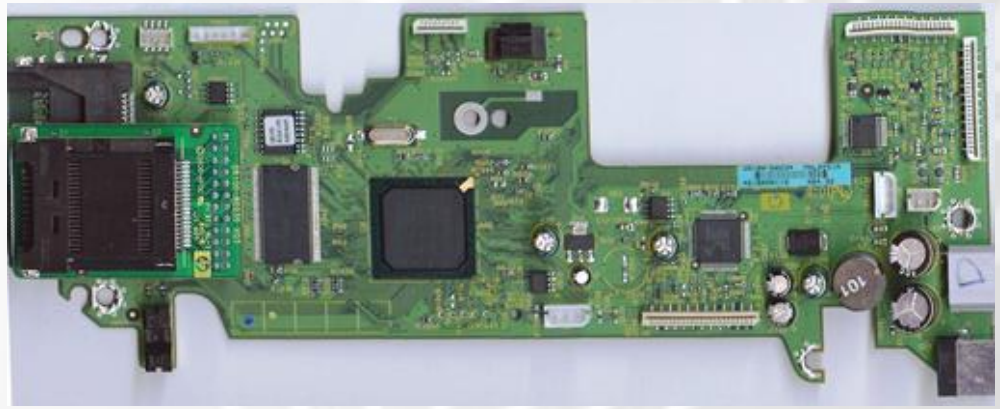
Main Logic board and PCA redesign projects

Amarjit Bhatia

Main Logic PCA redesign nesting of Photo card | $5M in savings

Original design and panel

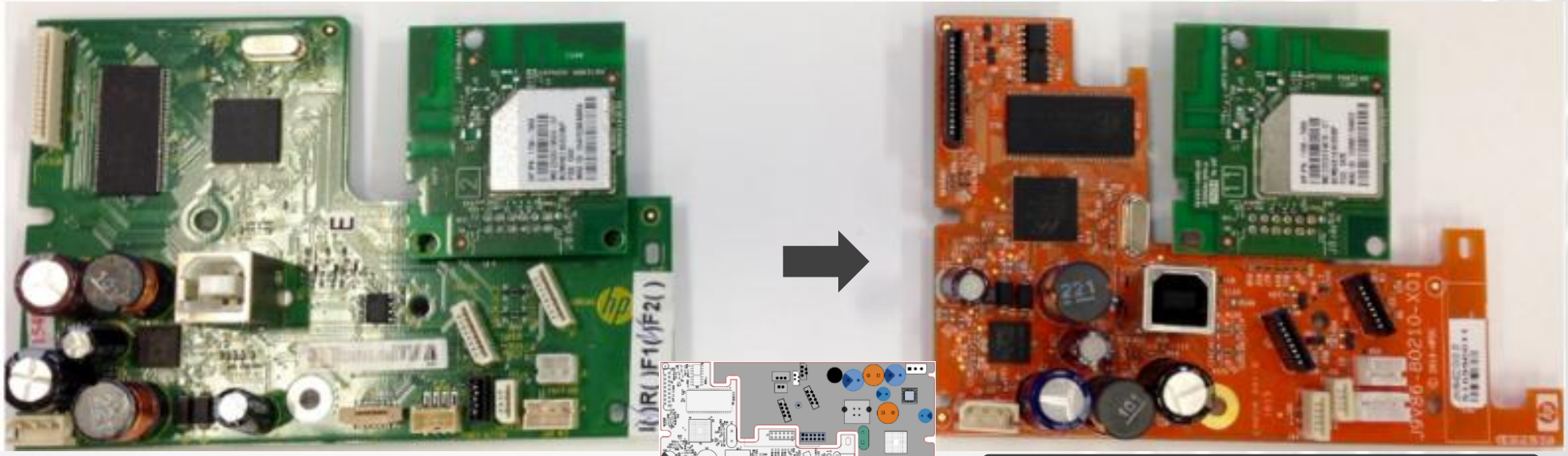




Cost reduced Design and Panel

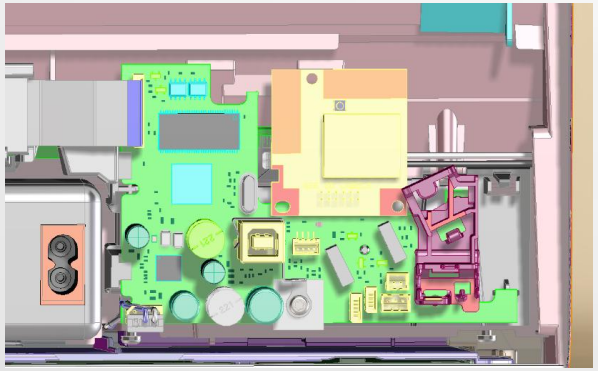
4-layer Photo card PCB nested

High Volume Product Logic PCA redesign to low cost | $1.6 M in savings



Original design Main Logic PCA

Cost reduced Design



Thorough study with Mechanical engineering for cable routing , fire enclosure, final assembly with the reduced cost board

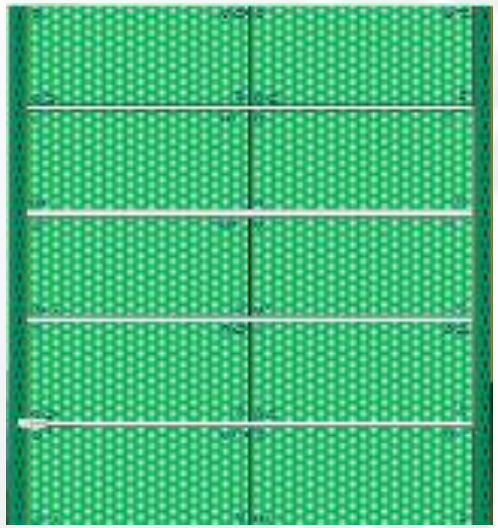
Control panel PCA Redesign | $1.32M in savings

Optimize Control panel PCB | 0.16/unit

Original CP design

Cost reduced Design

PCB Panel produces 16 PCBs coCMred to 10 before

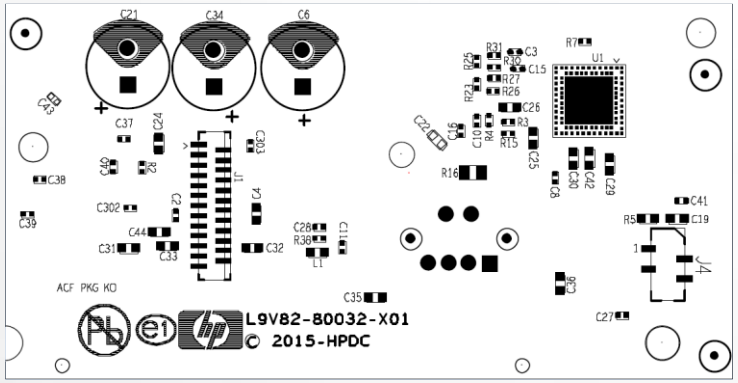


Original Design

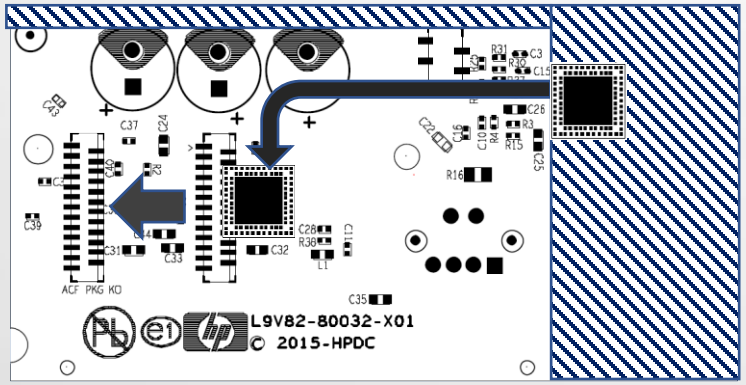
Cost reduced Design

Cost reduced control panel used on multiple programs generating $1.32M in savings

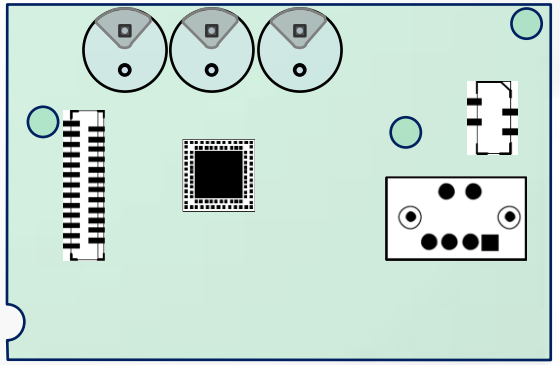
Carriage PCA redesign to smaller size | $2.5M in savings



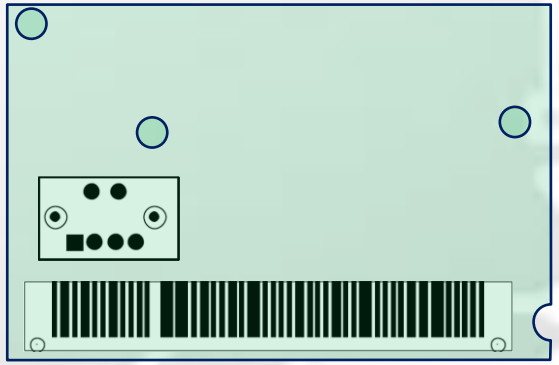
Original CP design

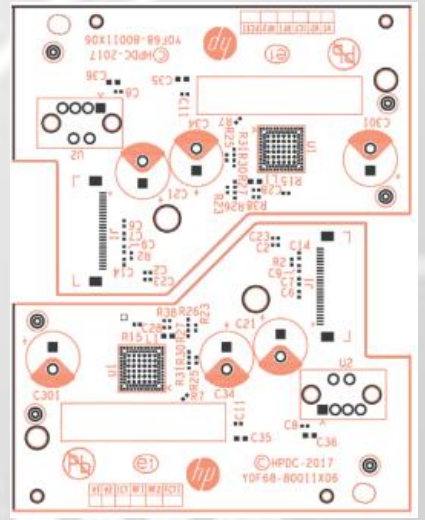


Cost reduction design



1st Round Cost reduction design



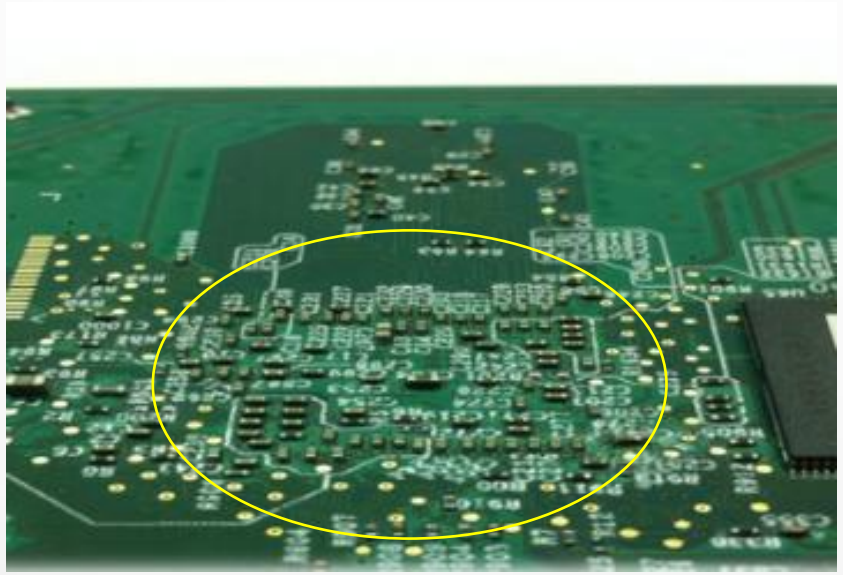


2nd round cost reduction design

Component savings and optimization for cost

Amarjit Bhatia

Decoupling Capacitor EMC Optimization and Removal | $5M in savings



Pilot Program: Elvis CR

For our pilot program, we chose Elvis CR, of which we plan to build one million starting this summer.

We optimized the 3.3V PDN that started with 62 capacitors loaded.

Technical challenges that we overcame

- Matching simulations to measured results
- Determining the right frequency-dependent target impedance
- Choosing capacitor libraries that match simulations
- Incorporating S-parameter models for ASIC PDN
- Incorporating VRM models
- Defining tests to detect potential side affects of change

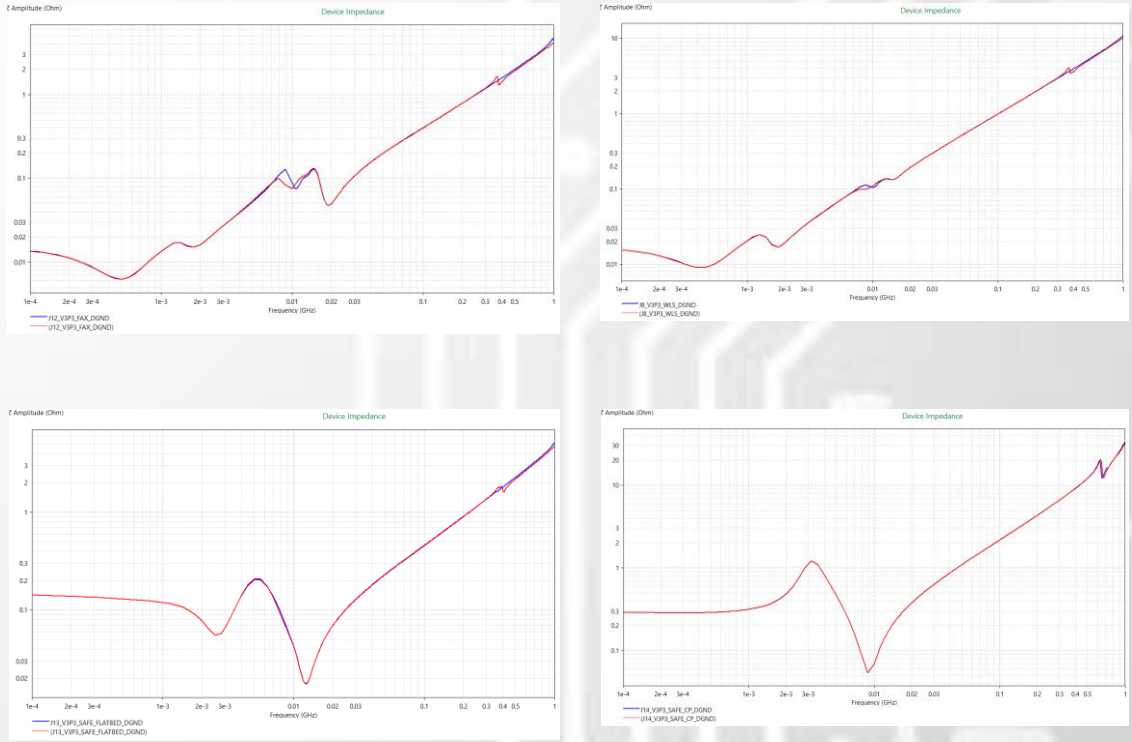
Impedance simulation using cadence Sigerity tools and collaboration with EMC team to optimize and reduce decoupling capacitors

- Elvis
- Chili
- Congo
- Congo Wireless
- Shaolin WL/ IA
- Wudang AIO/IA
- Naples Minus/IA
- Naples
- Naples Plus
- Naples Super
- Corfu/minus
- Corfu Plus

Decoupling Capacitor EMC Optimization and Removal | $5M in savings

Impedance simulation using Cadence Sigerity tool

C299	located along PCB edge
C301	located along PCB edge
C303	located along PCB edge
C304	located along PCB edge
C307	located along PCB edge
C308	located along PCB edge
C335	located along PCB edge
C339	located along PCB edge
C797	Under U101, Impedance plot is quite similar
C24	Under U1, Impedance plot is quite similar

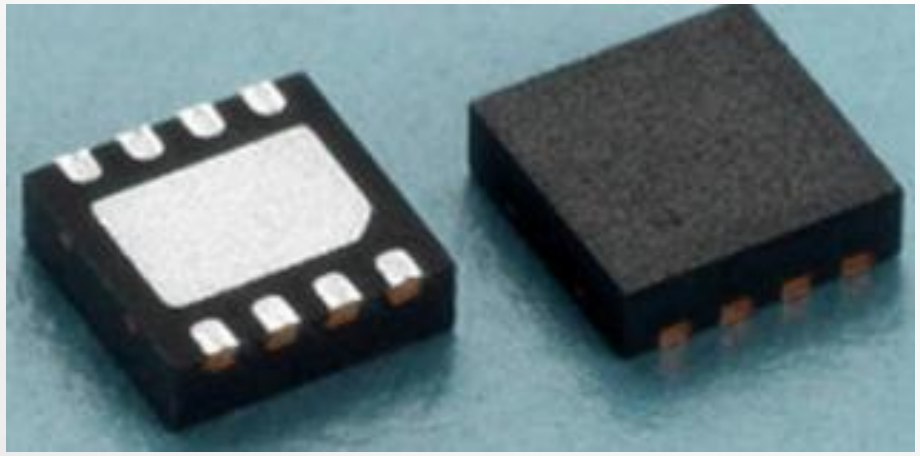


Original Simulation:

Removed caps Simulation:

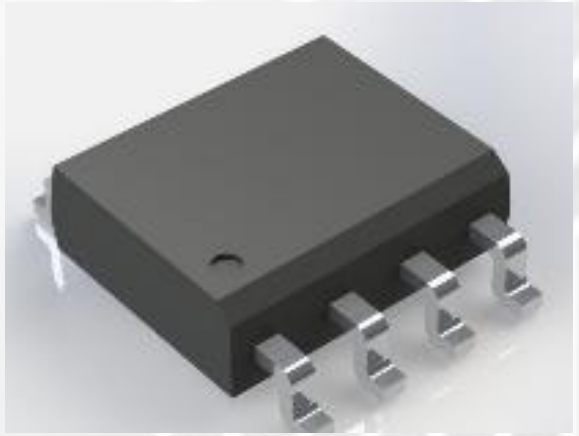
Change package on Pen security chip DFN-8 to SO-8| $2 M in savings

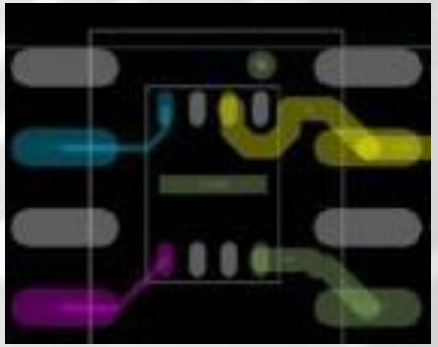
DFN Package Pen Security Acumen Chip



Change DFN to So8

10 cent cheaper : 8 Pin SO-8 package





Overlap nesting DFN to SO8 geometry in Layout on multiple programs, qualified and ECO design change into production

Collaborated with ST to redesign the security chip package, transitioning from DFN8 (Dual Flat No Leads) to SO8 (Small Outline-Leads). Successfully qualified across multiple programs, achieving a cost reduction of $0.10 per unit, resulting in total savings of $2M over two years.

Change MLCC from single to quad Packs | Savings $5M+

Change Individual MLCC capacitors to Quad Pack

Quad Packs MLCC

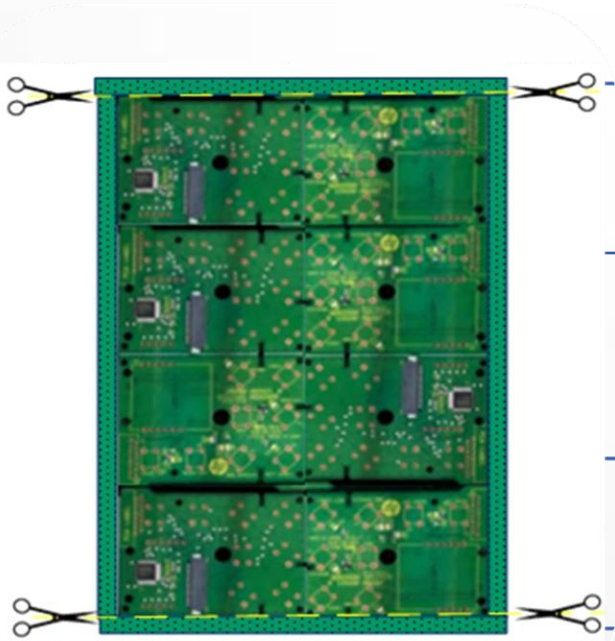
Product	Volume	Placement Cost Saving	Total EOL Saving
Corfu	2440083	$0.203	$494,117
Corfu IA	553222	$0.203	$112,027
Corfu Minus	58240	$0.203	$11,794
Corfu Plus	1466057	$0.243	$356,252
Corfu Plus IA	332082	$0.243	$80,696
Palermo Fast	2000000	$0.421	$842,400
Palermo Minus	3000000	$0.316	$947,700
Palermo Super	1000000	$0.494	$494,100
Verona	4000000	$0.235	$939,600
Verona Plus	2000000	$0.275	$550,800
Weber	2000000	$0.920	$1,840,000
		Total EOL Saving	**$6,669,486**

Serial #	Part Number	Description
1	0161-1032	CAP-FXD 0.1UF +-10% 10 V CER X5R ROHS
2	0161-1057	CAP-FXD 470PF +-10% 50 V CER X7R ROHS
3	0161-1093	CAP-FXD 22PF +-5% 50 V CER C0G ROHS
4	0161-1171	CAP-FXD 0.1uF +-10% 50V CER X7R ROHS
5	0161-1227	CAP-FXD 0.01UF +-10% 25 V CER X7R ROHS
6	0161-2309	CAP-FXD 1000pF +-10% 50V CER X7R
7	0697-1463	RES 16K +-1% .063W TC=0+-200 ROHS
8	0699-7203	RESISTOR 100 +-1% .063W TKF ROHS
9	0699-7215	RESISTOR 10K +-1% .063W TKF ROHS
10	0699-7513	RES 10 OHM 1% .063W TKF TC=0+-200 ROHS

Process improvement for Savings

Amarjit Bhatia

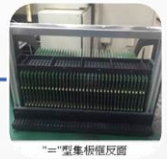
Championed 4 rail to 2 rail PCB panel design Factory process change |$1M /year savings



Extra Tabs on PCB's Increase Per PCB cost to HP

"4 side tabs PCBs" used in Production due to Foxconn process and fixture limitations

Design for supply chain team engaged with Foxconn and CDPS to understand their Fixtures and process



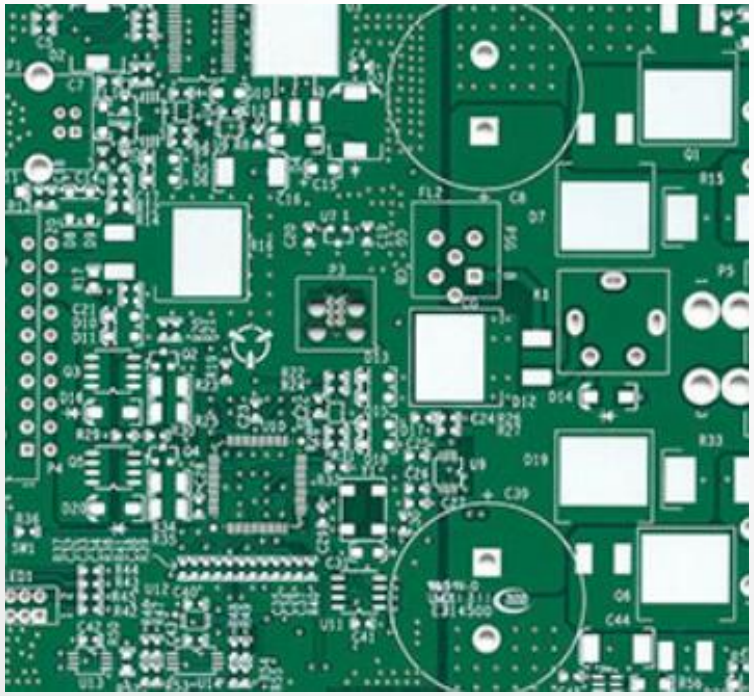
Process Improvement and fixture redesign with Foxconn to run production with "2 side tab" PCB's

Estimated minimum $500K+ savings year after year at Foxconn from 2 Tab PCB's

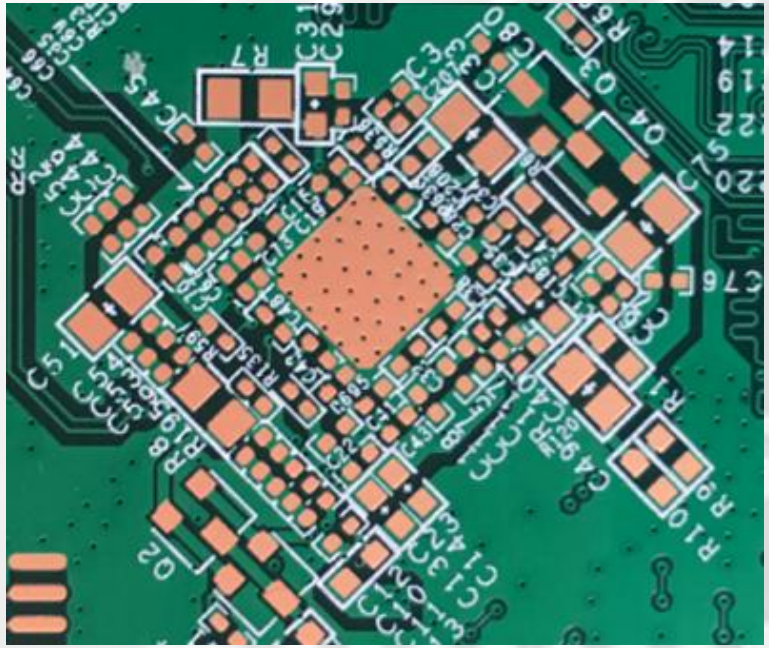
		FY'16	FY'17	FY'18
Weber MPCA		$132,638	$280,373	$101,881
Weber Base CP	$0.027	$30,409	$64,279	$23,358
Weber Mid CP	$0.035	$39,572	$83,648	$30,396
Shaolin WL	$0.027	$37,394	$99,568	$3,803
Lhasa Wl CP	$0.022	$10,611	$36,118	$15,301
	Savings/Year	$250,624	$563,986	$174,739
	Total Savings	**$989,349**		

Championed Surface finish change from Immersion tin to OSP Pan HP project | $1M/year savings

PCB surface finish change to generate 3% cost savings per PCB



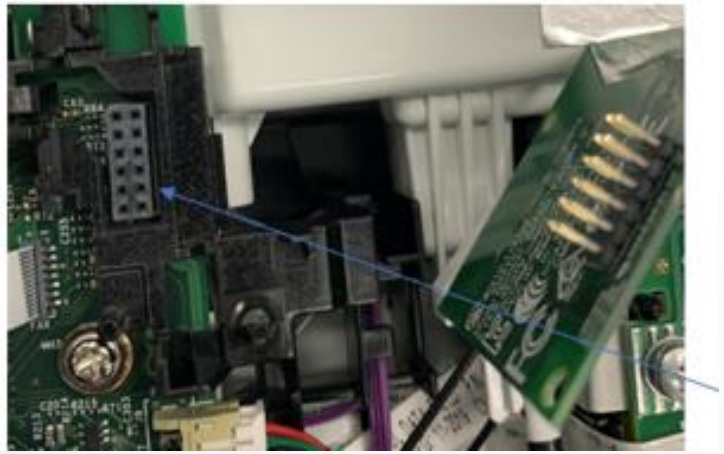
Immersion Tin

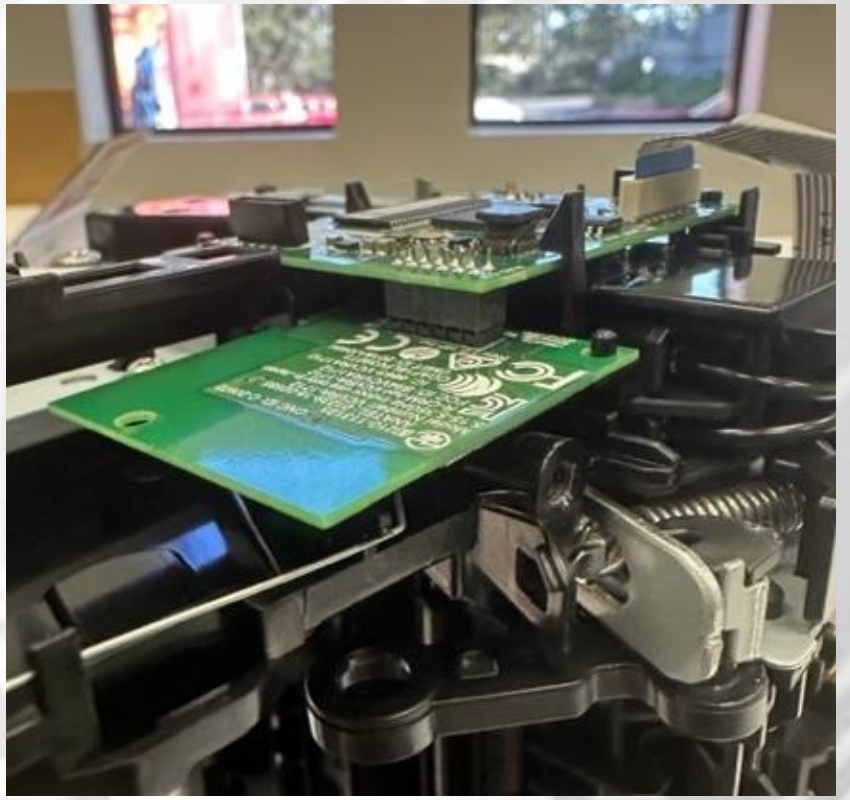


OSP- Organic solderability Preserve

3% cost down

Architected direct solder wifi Card to Main Logic Board Pan HP |$1.2M/year savings





Optimized EMC solution –Compliance to CISPR-35 requirements at lower cost

Use Lower cost DC cable ferrite

Reduce the size of the scanner ferrite

Remove Control panel cable ferrite

Test Type	Description
Electrostatic Discharge (ESD)	Immunity to static discharges (per IEC 61000-4-2)
Radiated RF Immunity	Resistance to radio-frequency fields (IEC 61000-4-3)
Conducted RF Immunity	Immunity via power and signal cables (IEC 61000-4-6)
Electrical Fast Transients (EFT)	Switching transients immunity (IEC 61000-4-4)
Surge Immunity	Protection against voltage surges (IEC 61000-4-5)
Voltage Dips and Interruptions	Power reliability (IEC 61000-4-11)

Use Lower cost DC cable ferrite

Remove metal shielding from CP cable

Pass copy sample

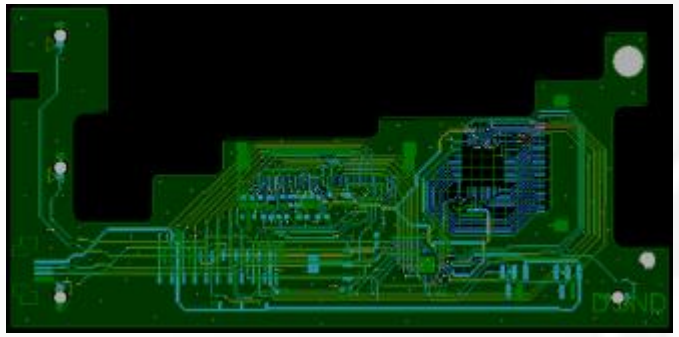
Fail copy sample

Product	Savings/unit	Total savings
Tassel Plus	$0.22	$ 0.6 M
Tassel Base	$0.265	$ 3.2 M
Total savings		$ 3.8 M

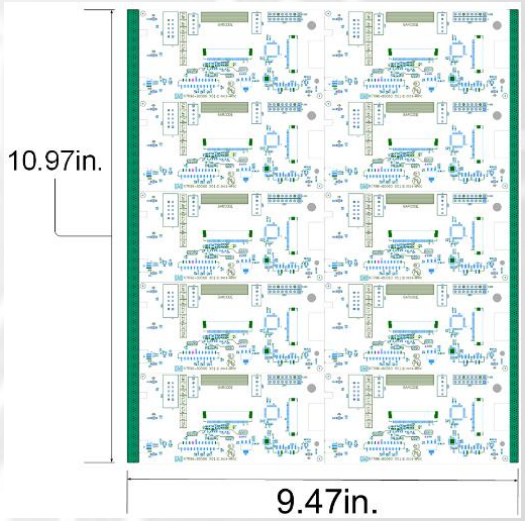
Optimized low-cost solution to meet **CISPR 35** international standard that specifies **immunity requirements** for **multimedia equipment** (MME) regarding electromagnetic disturbances. It is published by **CISPR** (International Special Committee on Radio Interference), which is part of the **IEC** (International Electrotechnical Commission).

Control Panel 34% PCB Size reduction saves $0.27/unit

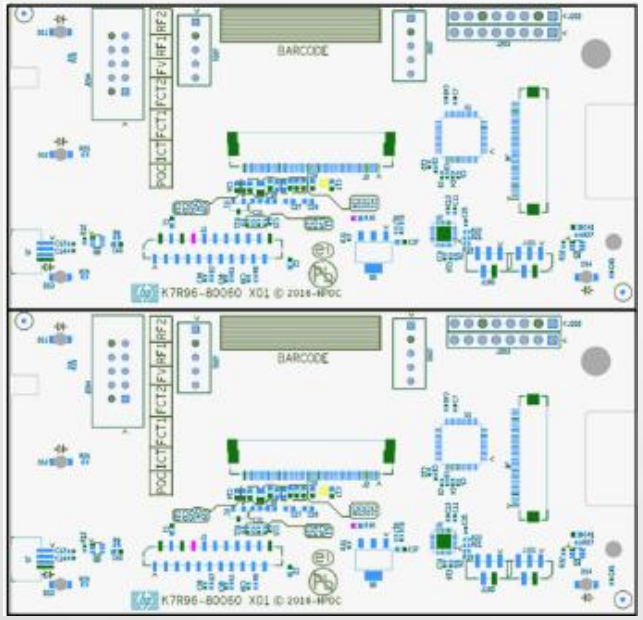
Original Design Control Panel PCA $0.78/PCB



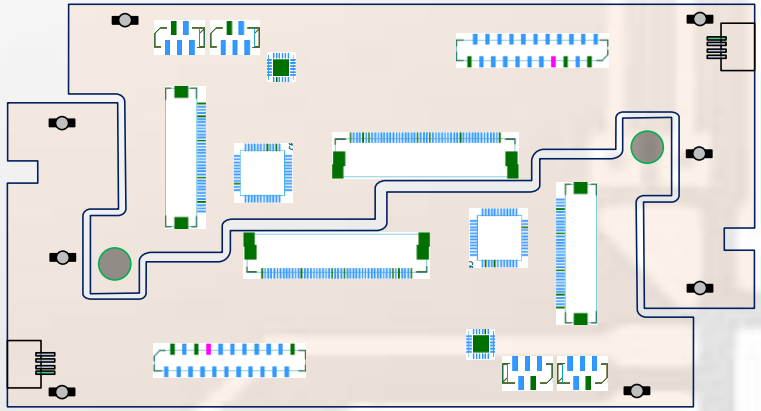
Redesign PCB new cost estimate $0.51/PCB

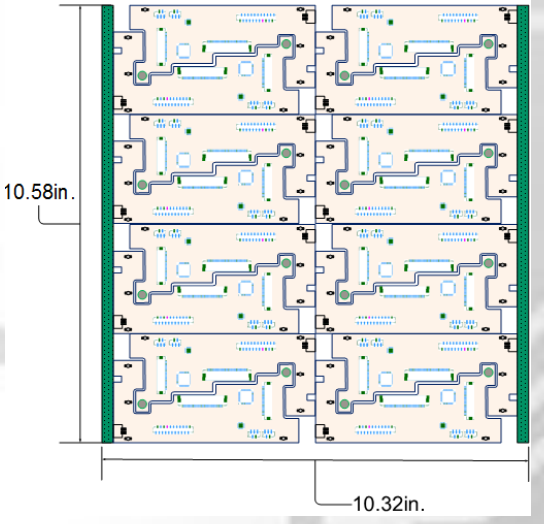


10 boards /panel



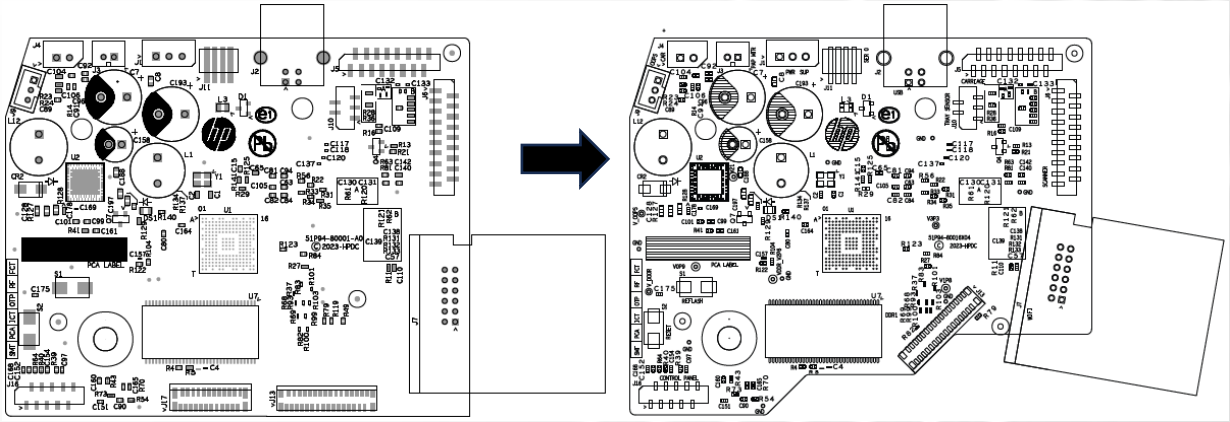
Improved nesting on Panel





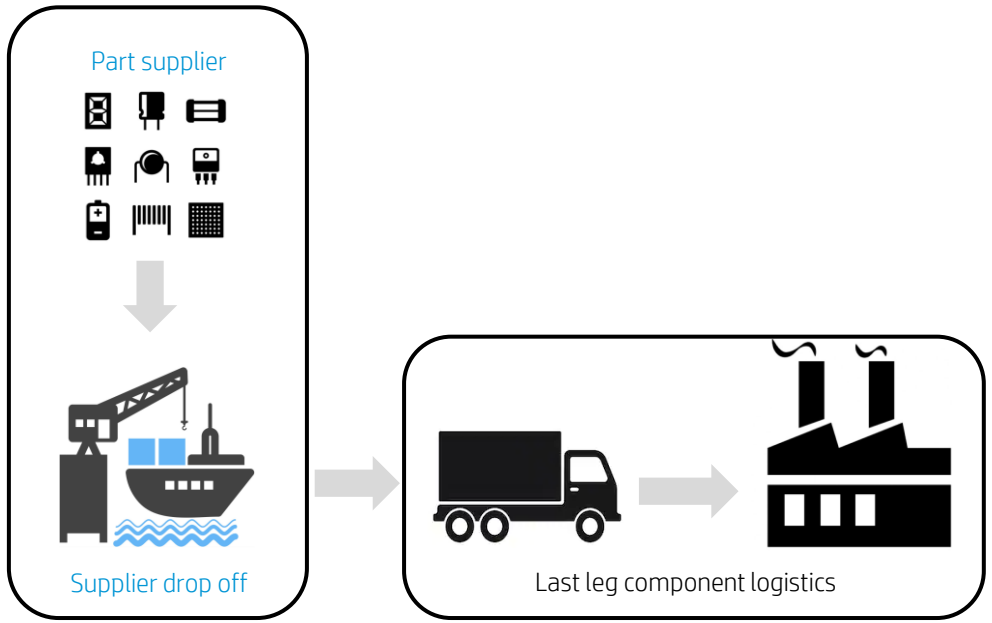
16 boards /panel

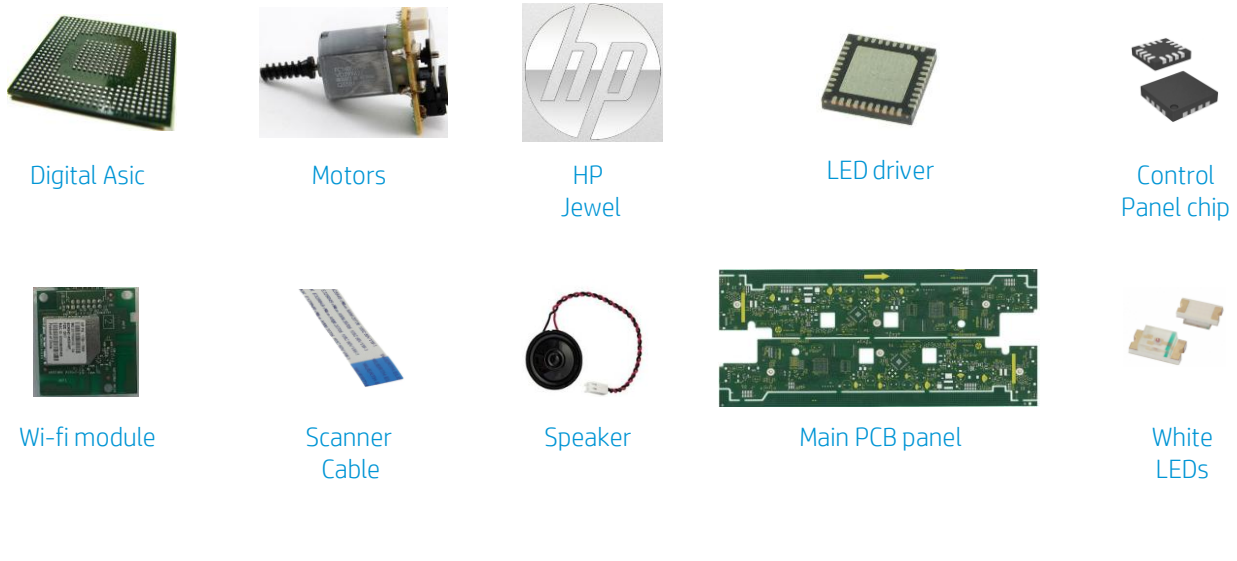
Redesigned Main Logic Board to smaller size | $960K in savings



Product	Savings/unit	Total savings
High-volume low-end product	$0.12	$960K
Total savings		$960K

Align to-should cost with CM for Last leg logistics savings | $400K/year





Logistics-Term	Defination	Explanation
DAP	Delivered at Place	Seller delivers goods ready
FOB	Free on Board-Port of Loading	Seller delivers goods on board at origin port (e.g., FOB Shenzhen)
EXW Ex Works	Buyer picks up goods at seller's facility	Buyer picks up goods at seller's facility
CIF	Cost, Insurance, and Freight	Seller covers cost, insurance, and freight to the destination port
DDP	Delivered Duty Paid	Seller delivers goods including all duties/taxes to buyer's facility

Savings Description	Products	FY21	FY22
Logistics cost alignment GTK parts	Multiple products	$53,138	$0
Asic last leg logistics savings	Multiple products	$100,150	$27,930
Puff Asic last leg logistics savings	Multiple products	$84,677	$38,414
HP jewel last leg logistics savings	Multiple products	$42,034	$17,876
Last leg logistics on TK parts	Multiple products	$92,328	$0
Last leg logistic savings on 10 Vasari parts	Multiple products	$71,986	$273,485
Last leg logistics cost alignment on plastics and cables	Multiple products	$7,432	$26,609
Main PCB logistics alignment	Multiple products	$0	$14,415
	Total yearly savings	**$451,745**	**$398,729**