# Aaron Marlin

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## Education

**Georgia Institute of Technology** — Atlanta, GA
*Bachelor of Science in Computer Engineering* **GPA**: 3.84 — Aug 2023 – Dec 2026

**Georgia Institute of Technology** — Atlanta, GA
*M.S. in Electrical and Computer Engineering* — Jan 2027 – Dec 2027

## Technical Skills

**Programming Languages**: SystemVerilog, C++, C, Python, Bash, Tcl, CUDA, RISC-V Assembly, MIPS Assembly, Java
**Hardware**: RISC-V Architecture, Layout, Digital Design, Design Verification, Computer Architecture, GPU Architecture, FPGA
**Software**: Git, Linux, Cadence Virtuoso, Synopsys VCS, QuestaSim, Vivado, OpenMP, OpenMPI, LabVIEW
**Embedded Systems**: ESP32, Arduino, Raspberry Pi, FreeRTOS, WiFi,, BLE, SPI, UART, I2C, RISC-V, ARM, MIPS

## Experience

**Incoming Design Verification Intern** — May 2026 – Aug 2026
*IBM* — *Austin, TX*

**Digital Design Engineer** — Jan 2024 – Jan 2025
*SiliconJackets — Georgia Institute of Technology* — *Atlanta, GA*

- Collaborated with design team to develop a custom, pipelined RISC-V processor implemented onto club's first SoC
- Implemented 32-bit Dadda Multiplier module in Verilog to accelerate ∼13% compared to previous multiplier
- Coordinated integration of digital design and design verification to fully verify 4 modules before our RTL Freeze

**Design Verification Engineer** — Jan 2025 – Present
*SiliconJackets — Georgia Institute of Technology* — *Atlanta, GA*

- Leading the establishment of an FPGA, validation environment for software testing and emulation of SoC
- Incorporated SystemVerilog constraint randomization in 6 module-level testbenches for 100% functional coverage
- Arranged Python scripts to generate large sequences of test vectors used during module-level simulation

**Software Engineering R&D Intern** — May 2024 – Aug 2024
*Sandia National Laboratories* — *Albuquerque, NM*

- Enhanced GPU performance visibility in distributed systems by creating a lightweight C++/ROCm API that provides developers with over 100 critical hardware metrics
- Streamlined connection between the sampling API and Grafana to efficiently visualize metrics on 20 clusters

**High Performance Computing R&D Intern** — Sep 2024 – Present
*Sandia National Laboratories* — *Remote*

- Scaled a GPU performance analysis tool for the U.S.'s first exascale supercomputers (Frontier, El Capitan), boosting computational efficiency for over 1000 researchers utilizing cutting-edge GPU/APU hardware
- Worked with HPC Tools team to integrate the Lightweight Distributed Metric Service API for low overhead monitoring
- Developed documentation for researchers using the ROCm software stack to develop custom profiling tools

**Digital Twin Research Assistant** — Aug 2024 – Apr 2025
*Georgia Institute of Technology* — *Atlanta, GA*

- Classified structures embedded in LiDAR scans with CNN semantic segmentation to characterize objects efficiently
- Simulated WiFi propagation via raytracing in Python using NVIDIA Sionna API to recreate indoor wireless environments
- Published findings between LiDAR scan fidelity and relative accuracy of simulations to IEEE ORSS 2025

**FPGA Design Verification** — Aug 2024 – Apr 2025
*Configurable Computing and Embedded Systems VIP* — *Atlanta, GA*

- Developed testbench in SystemVerilog to verify one-way communication on PYNQ-Z1 FPGA SPI bus
- Collaborated with FPGA Design members to create seamless hardware interactions for users
- Utilized Vivado Logic Analyzer to ensure expected values of internal connections and monitor FPGA states

## Projects

**TamaGITchi** | *C++, ESP-32, FreeRTOS, Embedded System Design* Oct 2025 – Dec 2025

- Developed task keeping handheld device with ESP-32C6 and C++ to gamify productivity for users
- Utilized BLE to upload custom tasks from phone to device to remind users of important tasks to complete
- Configured memory mapped I/O for SPI communication to LCD and I2S for audio output

**16-bit Pipelined Ripple Carry Adder** | *Cadence Virtuoso, Digital Design, Layout, DRC, LVS, Tcl* Oct 2025 – Nov 2025

- Developed schematics and compact layouts for NOT, NOR, and XOR boolean gate unit cells, passing DRC and LVS
- Organized boolean gates to layout unit cell for 1-bit Adder, and used a mirror cell technique to scale up to a 16-bit RCA
- Optimized to a 1:4, height to width, aspect ratio of 16-bit RCA, improving area to compute ratio and complying with DRC

**Accelerated Rubik's Solver** | *Python, PyTorch, C++, Verilog* Jul 2025 – Present

- Implemented edge and color detection to segment each face and assign positions with color using OpenCV
- Developed Python script to algorithmically predict moves to solve Rubik's Cube based on segmented faces
- Integrating a CNN acceleration module and camera module onto an FPGA to improve computation speed

**Rhythm Master** | *C, ESP-32, Embedded System Design* Jan 2025 – May 2025

- Controlled 8 peripherals and implemented game logic for reading and interpreting user inputs using C
- Designed compact and organized PCB, routing and integrating power and control for all components of the robot
- Debugged faulty GPIO and ADC on ESP-32 using Oscilloscope and Signal Generator to address and iterate designs

**LoRa for Automated, Efficient Vertical Farming** | *C++, Arduino* August 2022 – April 2023

- Reduced initial investment for vertical farms by 15% using LoRa and low-power microcontrollers
- Cut power consumption by 25% compared to current vertical farming solutions
- Hosted a lecture series for cohort of 20 students across multiple teams on programming and building with Arduino
- Led team of 10 students to develop a prototype that placed second in the state for Engineering Design

## Relevant Courses

**Advanced Digital Design & VLSI**: CMOS Design, Cadence Virtuoso, Adder and Multiplier Topology, Timing Analysis
**Embedded Systems Design**: UART, SPI, I2C, I2S, Bluetooth (BLE), WiFi, Real-Time Operating Systems (RTOS), microcontrollers
**Computer Architecture**: 5-Stage Pipelined Processor, Verilog, Memory Hierarchy, Cache Coherency, Virtual Memory, GPU Architecture
**Advanced Programming Techniques**: C++, SFML, OpenMP, OpenMPI, CUDA, OpenGL, Sockets, Multithreading
**Digital Design Laboratory**: HDL, FPGA, Oscilloscope, Logic Analyzer, Quartus Prime