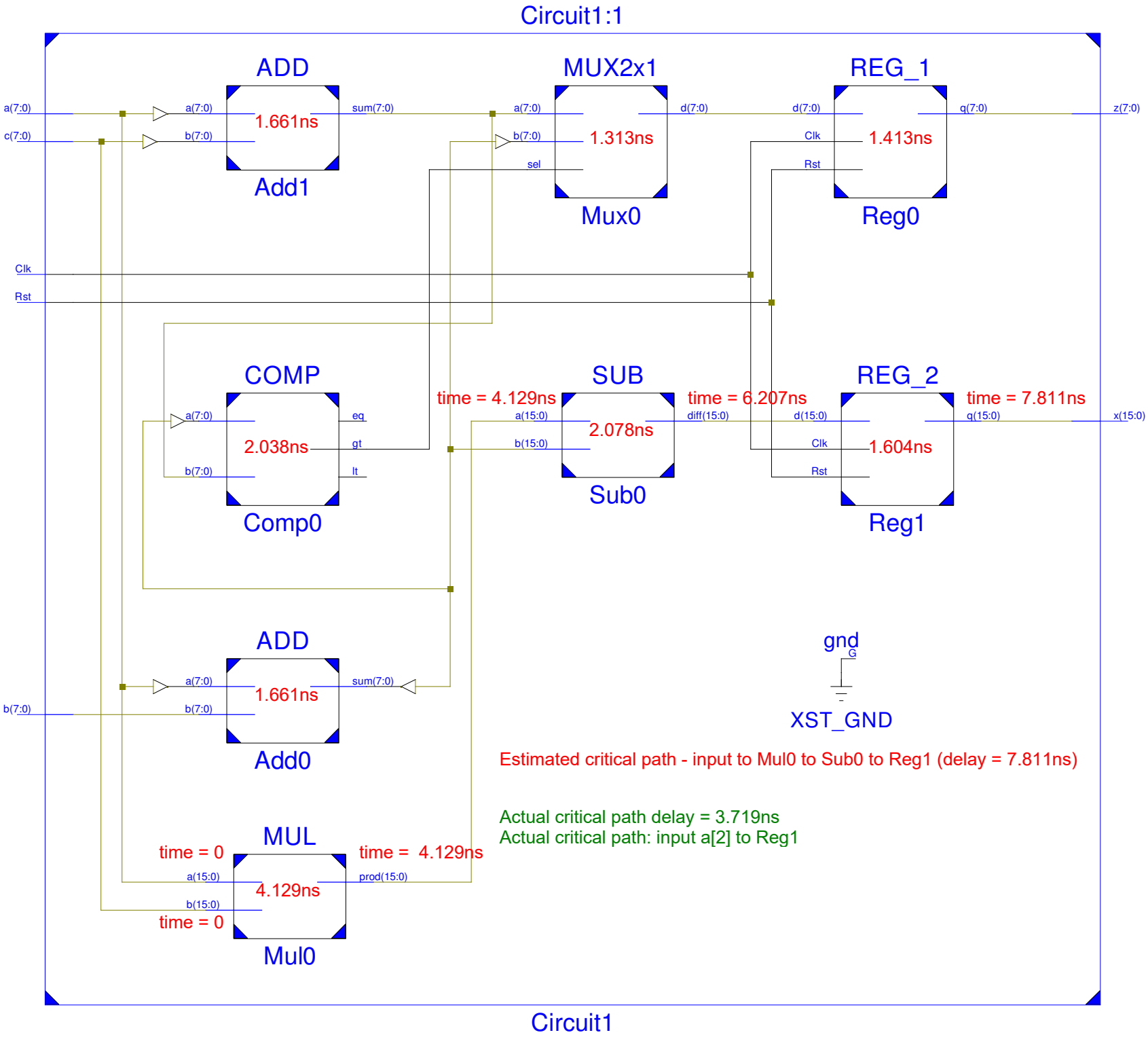
Circuit1:1
ADD
1.661ns
Add1
a(7:0)
b(7:0)
sum(7:0)
MUX2x1
1.313ns
Mux0
sel
d(7:0)
REG_1
1.413ns
Reg0
Clk
Rst
q(7:0)
z(7:0)
c(7:0)
COMP
2.038ns
Comp0
eq
gt
lt
SUB
time = 4.129ns
2.078ns
Sub0
a(15:0)
b(15:0)
diff(15:0)
time = 6.207ns
REG_2
1.604ns
Reg1
d(15:0)
q(15:0)
time = 7.811ns
x(15:0)
ADD
1.661ns
Add0
MUL
time = 0
4.129ns
Mul0
a(15:0)
b(15:0)
prod(15:0)
time = 4.129ns
gnd
XST_GND
Estimated critical path - input to Mul0 to Sub0 to Reg1 (delay = 7.811ns)
Actual critical path delay = 3.719ns
Actual critical path: input a[2] to Reg1
Circuit1