BUG REPORT FOR PHASE – 4

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Bug Number : 1

Line Number : 284 in cache\_block\_0.v

Bug Type : syntax

Test Number : N/A. Syntax checking by just compiling 'cache\_multi\_config\_1.v' with nc-verilog

Bug Description : The equality comparison operator must be '==' and not '=' .

Fix Implemented : Change '=' to '==' at line 284 in cache\_block\_0.v

Bug Number : 2

Line Number : 569 in cache\_block\_0.v

Bug Type : syntax

Test Number : N/A. Syntax checking by just compiling 'cache\_multi\_config\_1.v' with nc-verilog

Bug Description : Net used as an lvalue. CPU\_stall is not declared as a reg.

Fix Implemented : Declare a reg for CPU\_stall as 'reg CPU\_stall'

Bug Number : 3

Line Number : 17 in cache\_def\_0.v

Bug Type : Syntax

Test Number : N/A. Syntax checking by just compiling 'cache\_multi\_config\_1.v' with nc-verilog

Bug Description : Illegal expression in LRU\_size macro definition. Incorrect operator used.

Fix Implemented : Replace '<>' with the correct operator '<<'

Bug Number : 4

Line Number : 69 in cache\_controller\_I\_0.v

Bug Type : Syntax

Test Number : N/A. Syntax checking by just compiling 'cache\_multi\_config\_1.v' with nc-verilog

Bug Description : Macro TAG\_MSB is incorrectly written.

Fix Implemented : Replace TAG\_MSB with `TAG\_MSB

Bug Number : 5

Line Number : 568 in cache\_block\_3.v

Bug Type : Syntax

Test Number : N/A. Syntax checking by just compiling 'cache\_multi\_config\_1.v' with nc-verilog

Bug Description : Cache\_var register size is given incorrectly as CACHE\_DEPTH also Cache\_var array size is incorrectly given as CACHE\_DATA\_SIZE.

Fix Implemented :

define Cache\_var reg as 'reg [`CACHE\_DATA\_SIZE-1 : 0] Cache\_var [0 : `CACHE\_DEPTH-1];'

Bug Number : 6

Line Number : 221, 222 in cache\_block\_3.v

Bug Type : Functionality

Test Number : 1. TopReadMiss .

Bug Description : BusRd and BusRdX assignments are interchanged.

Fix Implemented : assign BusRd to BusRd\_reg and BusRdX to BusRdX\_reg appropriately

Bug Number : 6

Line Number : 771 in cache\_block\_0.v

Bug Type : Functionality

Test Number : 1

Bug Description : Com\_Bus\_Req\_snoop of Proc 1 is asserted while it should remain de-asserted

Bug Number : 7

Line Number : 647 in cache\_block\_1.v

Bug Type : Functionality

Test Number : 3

Bug Description : Core 1 does not send Invalidate signal upon writing to a Shared Block.

Fix Implemented : Add Invalidate logic at 647 in cache\_block\_1.v

Bug Number : 8

Line Number : 470 in cache\_block\_1.v

Bug Type : Functionality

Test Number : 3

Bug Description : Core 1 Invalidates its own block after it sends Invalidate signal out.

Fix Implemented : at 470 in cache\_block\_1.v, remove the ‘Invalidate’ term inside if condition