VERIFICATION ACADEMY

UVM Basics

Monitors and Subscribers

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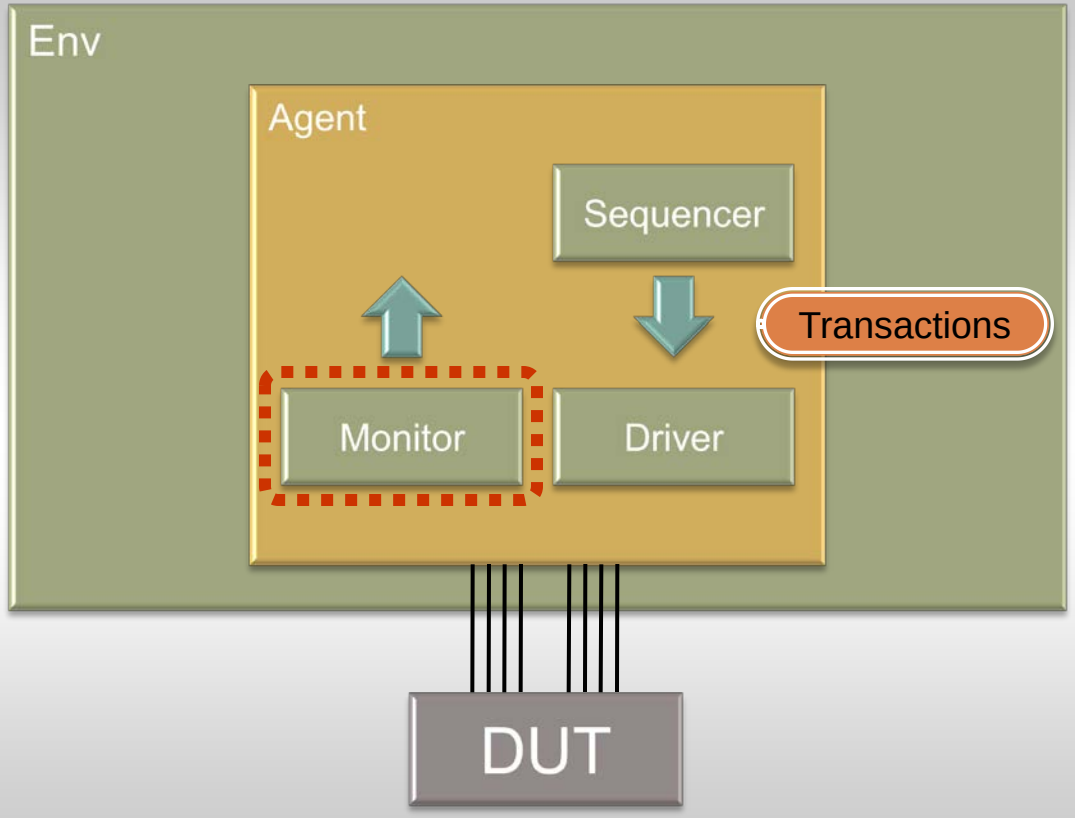
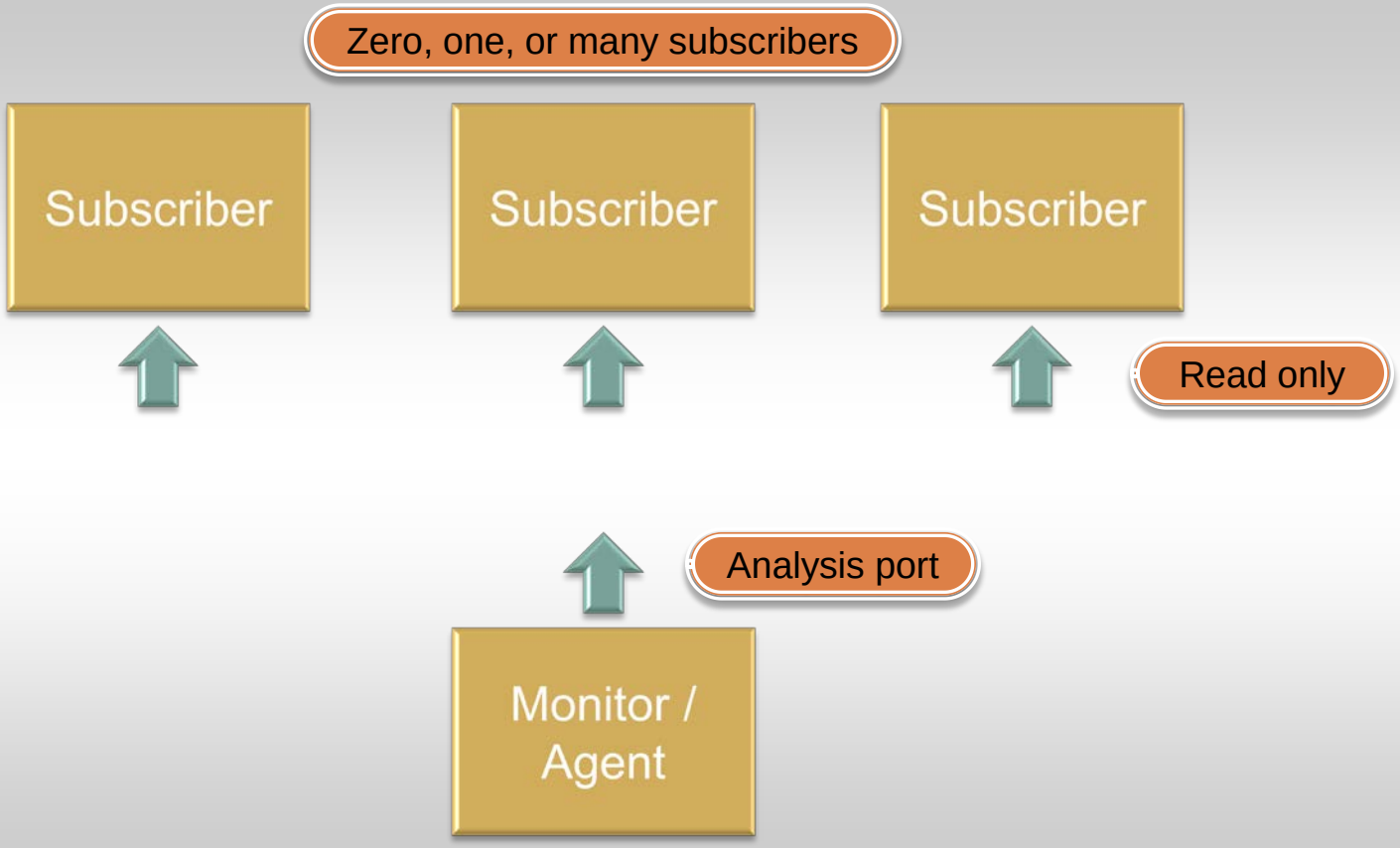
Monitor



Analysis Ports



Monitor

```
class my_monitor extends uvm_monitor;
```

Monitor

```
class my_monitor extends uvm_monitor;

  `uvm_component_utils(my_monitor)

  uvm_analysis_port #(my_transaction) aport;
```

Monitor

```
class my_monitor extends uvm_monitor;

  `uvm_component_utils(my_monitor)

  uvm_analysis_port #(my_transaction) aport;

  virtual dut_if dut_vi;

  function new ...

  function void build_phase(uvm_phase phase);
    super.build_phase(phase);
    aport = new("aport", this);
    ...
```

Monitor

```
class my_monitor extends uvm_monitor;
  ...
  task run_phase(uvm_phase phase);
    forever
    begin
      my_transaction tx;

      @(posedge dut_vi.clock);
      tx = my_transaction::type_id::create("tx");
      tx.cmd  = dut_vi.cmd;
      tx.addr = dut_vi.addr;
      tx.data = dut_vi.data;
```

Monitor

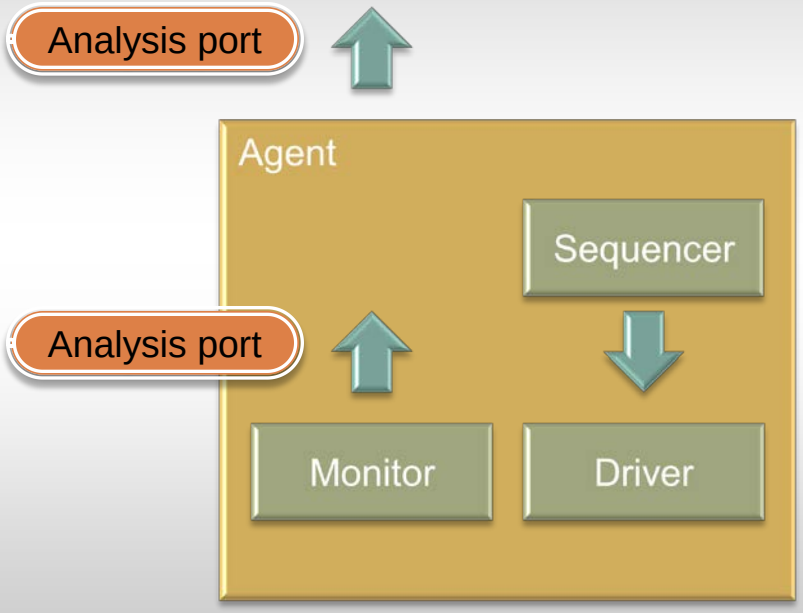
```
class my_monitor extends uvm_monitor;
  ...
  task run_phase(uvm_phase phase);
    forever
    begin
      my_transaction tx;

      @(posedge dut_vi.clock);
      tx = my_transaction::type_id::create("tx");
      tx.cmd  = dut_vi.cmd;
      tx.addr = dut_vi.addr;
      tx.data = dut_vi.data;

      aport.write(tx);
```

Sends tx through analysis port

Agent


Analysis port
Agent
Sequencer
Analysis port
Monitor
Driver

Agent

```
class my_agent extends uvm_agent;
  ...
  uvm_analysis_port #(my_transaction) aport;
```

Agent

```
class my_agent extends uvm_agent;
  ...
  uvm_analysis_port #(my_transaction) aport;
  ...
  function void build_phase(uvm_phase phase);
    super.build_phase(phase);
    aport = new("aport", this);
    my_sequencer_h = my_sequencer::type_id::create ...
    my_driver_h    = my_driver   ::type_id::create ...
    my_monitor_h   = my_monitor  ::type_id::create ...
```

Agent

```
class my_agent extends uvm_agent;
  ...
  uvm_analysis_port #(my_transaction) aport;
  ...
  function void build_phase(uvm_phase phase);
    super.build_phase(phase);
    aport = new("aport", this);
    my_sequencer_h = my_sequencer::type_id::create ...
    my_driver_h    = my_driver   ::type_id::create ...
    my_monitor_h   = my_monitor  ::type_id::create ...
  endfunction: build_phase

  function void connect_phase(uvm_phase phase);
    ...
    my_monitor_h.aport.connect( aport );
```

Port on child

Port on parent

Connecting a Subscriber

```
class my_env extends uvm_env;
  ...
  my_agent      my_agent_h;
  my_subscriber my_subscriber_h;
  ...
  function void build_phase(uvm_phase phase);
    super.build_phase(phase);
    my_agent_h      = my_agent     ::type_id::create ...
    my_subscriber_h = my_subscriber::type_id::create ...
  endfunction: build_phase

  function void connect_phase(uvm_phase phase);
    my_agent_h.aport.connect(
                          my_subscriber_h.analysis_export );
  endfunction: connect_phase
```

Subscriber

```
class my_subscriber extends uvm_subscriber
                            #(my_transaction);
  `uvm_component_utils(my_subscriber)


  ...


  function void write(my_transaction t);
```

Has implicit analysis_export

Coverage and Checking

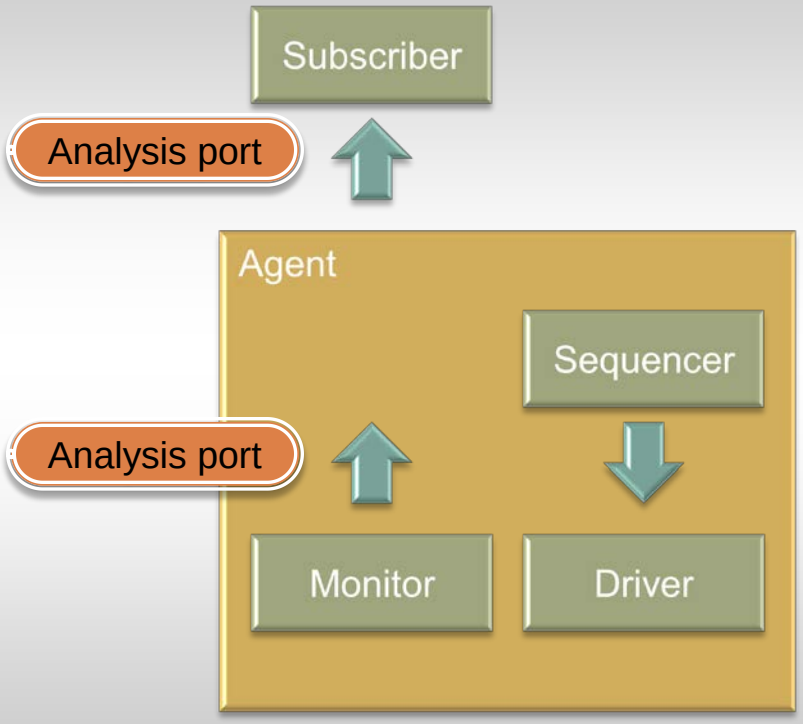
Coverage registers

```
bit cmd;
int addr;
int data;

covergroup cover_bus;
  coverpoint cmd;
  coverpoint addr { bins a[16] = {[0:255]}; }
  coverpoint data { bins d[16] = {[0:255]}; }
endgroup: cover_bus

function void write(my_transaction t);
  ...
  cmd  = t.cmd;
  addr = t.addr;
  data = t.data;
  cover_bus.sample();
```

Summary


Subscriber
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