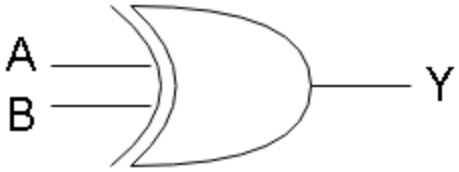
Lab 1 : 2 Input Logic XOR Gate

Due Date : February 16, 2020

2-Input Logic XOR Gate Diagram :



Truth Table :

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Design Verilog Code :

C:/Users/014593967/xor/xor.srcs/sources_1/new/lab2.v

```
1   `timescale 1ns / 1ps
2
3   module lab2(A, B, Y);
4
5       input A;
6       input B;
7       output Y;
8
9       assign Y = (A ^ B);
10  endmodule
```

Simulation/Testbench Verilog Code :

C:/Users/014593967/xor/xor.srcs/sim_1/new/xor_tb01.v

```
1   `timescale 1ns / 1ps
2
3   module xor_tb01;
4
5       reg A;
6       reg B;
7
8       wire Y;
9
10      lab2 UUT ( .A(A), .B(B), .Y(Y) );
11
12      initial begin
13          A = 0; B = 0;
14          #10;
15          A = 0; B = 1;
16          #10;
17          A = 1; B = 0;
18          #10;
19          A = 1; B = 1;
20          #10;
21      end
22
23  endmodule
24
```

Redo (Ctrl+Shift+Z)

Simulation Waveform :