Due Date : February 9, 2020

Lab 0 : Vivado Tutorial using an inverter

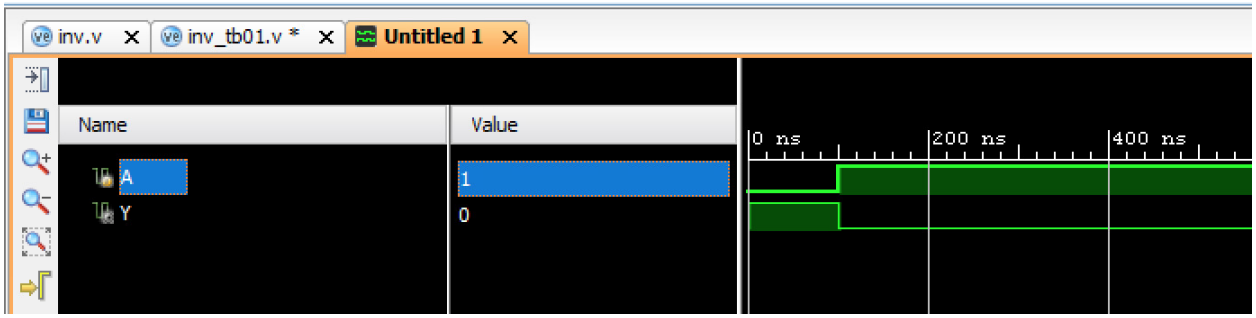
Verilog code for inv.v:

```
module inv(A,Y);

    input A;
    output Y;

    assign Y = ~A;
endmodule
```

Verilog code for inv_tb01.v:

```
////////////////////////////////////
module inv_tb01;

    reg A;
    wire Y;

    inv UUT ( .A(A), .Y(Y) );

    initial begin
        //test case 0
        A = 0;
        #100;
        //test case 1
        A = 1;
        #100;
    end

endmodule
```

Simulation waveform:



Summary of output:

The screenshot provided above proves that the inverter works in this lab. This is proven because when the input(A) is ‘0’, the output(Y) is ‘1’. On the other hand, when the input is ‘1’, the output becomes ‘0’.