CECS225

Lab 4 : Sequential Circuit_DFF

Due Date : May 8, 2020

PART 1 : HalfAdder

Section 1 - Design File

```
`timescale 1ns / 1ps
module HalfAdder(A, B, Cout, S);

    input A, B;
    output Cout, S;

    assign Cout = A & B;
    assign S = A ^ B;

endmodule
```

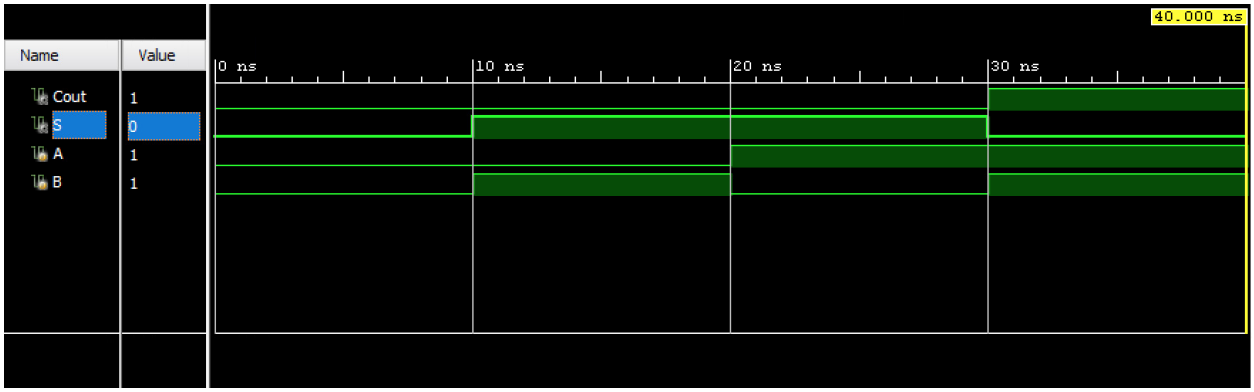
Section 2 - Simulation File

```
`timescale 1ns / 1ps
module HalfAdder_Tester;
    reg A;
    reg B;

    wire Cout;
    wire S;

    HalfAdder uut (.A(A), .B(B), .Cout(Cout), .S(S));
    initial begin
        A = 0;
        B = 0;
        #10;
        A = 0;
        B = 1;
        #10;
        A = 1;
        B = 0;
        #10;
        A = 1;
        B = 1;
        #10;
        $stop;
    end
endmodule
```

Section 3 - Simulation Screenshot



PART 2 : FullAdder

Section 4 - Design File

```
`timescale 1ns / 1ps
module FullAdder(FA_A, FA_B, Cin, FA_S, Cout);
    input FA_A, FA_B, Cin;
    output FA_S, Cout;

    assign FA_S = (FA_A ^ FA_B) ^ Cin;
    assign Cout = ((FA_A & FA_B) | (FA_B & Cin) | (Cin & FA_A));

endmodule
```

Section 5 - Simulation File

```
`timescale 1ns / 1ps
module FullAdder_Tester;
    reg FA_A;
    reg FA_B;
    reg Cin;
    wire FA_S;
    wire Cout;

    FullAdder uut(.FA_A(FA_A), .FA_B(FA_B), .Cin(Cin), .FA_S(FA_S), .Cout(Cout));
    initial begin
        FA_A = 0;
        FA_B = 0;
        Cin = 0;
        #10;
        FA_A = 0;
        FA_B = 0;
        Cin = 1;
        #10;
        FA_A = 0;
        FA_B = 1;
        Cin = 0;
        #10;
        FA_A = 0;
        FA_B = 1;
        Cin = 1;
        #10;
```

```
        FA_A = 1;
        FA_B = 0;
        Cin = 0;
        #10;
        FA_A = 1;
        FA_B = 0;
        Cin = 1;
        #10;
        FA_A = 1;
        FA_B = 1;
        Cin = 0;
        #10;
        FA_A = 1;
        FA_B = 1;
        Cin = 1;
        #10;
        $stop;
    end
endmodule
```

Section 6 -Simulation Screenshot