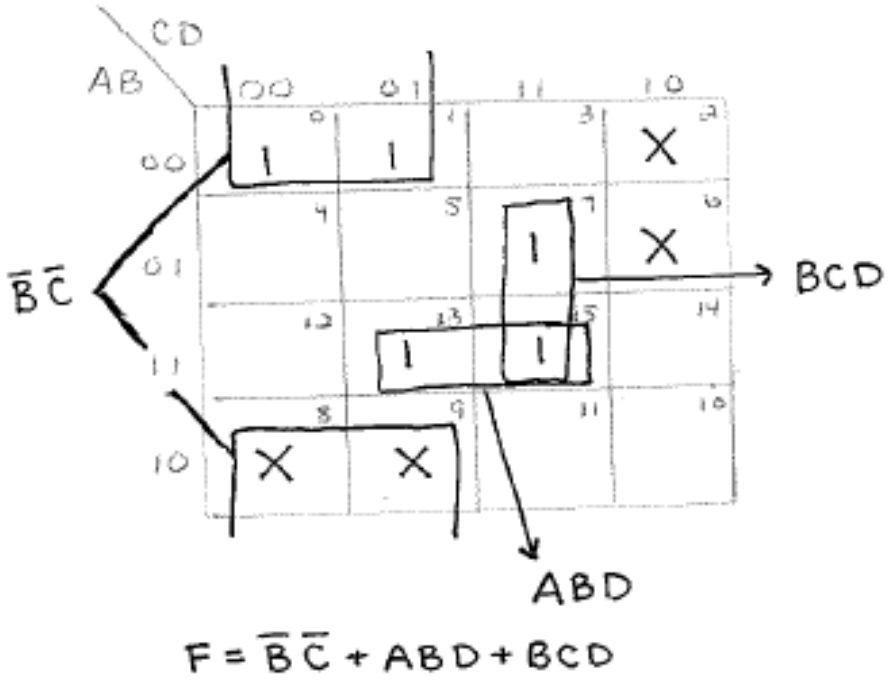
Lab 2 : K-Map

Due Date : April 6, 2020

Truth Table :

A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	X
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	X
0	1	1	1	1
1	0	0	0	X
1	0	0	1	X
1	0	1	0	X
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

K-Map Simplification :



Design Verilog Code :

```
`timescale 1ns / 1ps

module k_map(A, B, C, D, F);

    input A,B,C,D;
    output F;

    assign F = (((~B)&(~C)) | (A & B & D) | (B & C & D));

endmodule
```

Testbench Verilog Code :

```
`timescale 1ns / 1ps
module k_maptb;

    reg A;
    reg B;
    reg C;
    reg D;

    wire F;

    k_map UUT( .A(A), .B(B), .C(C), .D(D), .F(F) );

  initial begin
    // test case 0
    A = 0; B = 0; C = 0; D = 0;
    #10;
    // test case 1
    A = 0; B = 0; C = 0; D = 1;
    #10;
    // test case 2
    A = 0; B = 0; C = 1; D = 0;
    #10;
    // test case 3
    A = 0; B = 0; C = 1; D = 1;
    #10;
```

```
        // test case 4
        A = 0; B = 1; C = 0; D = 0;
        #10;
        // test case 5
        A = 0; B = 1; C = 0; D = 1;
        #10;
        // test case 6
        A = 0; B = 1; C = 1; D = 0;
        #1;
        // test case 7
        A = 0; B = 1; C = 1; D = 1;
        #10;
        // test case 8
        A = 1; B = 0; C = 0; D = 0;
        #10;
        // test case 9
        A = 1; B = 0; C = 0; D = 1;
        #10;
        // test case 10
        A = 1; B = 0; C = 1; D = 0;
        #10;
        // test case 11
        A = 1; B = 0; C = 1; D = 1;
        #10;

      // test case 12
      A = 1; B = 1; C = 0; D = 0;
      #10;
      // test case 13
      A = 1; B = 1; C = 0; D = 1;
      #10;
      // test case 14
      A = 1; B = 1; C = 1; D = 0;
      #10;
      // test case 15
      A = 1; B = 1; C = 1; D = 1;
      #10;
    end
endmodule
```

Simulation Waveform :