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Our testbench runs **all 3 programs continuously**.

To run the project, make project in ModelSim and import alu.sv, definitions.sv, dmem.sv, imem.sv, ls_dec.sv, lut_pc.sv, pc.sv, program_all_tb.sv, rf.sv, top.sv. Compile order by clicking Auto Generate. Start Simulation and select program_all_tb Module when you are prompted which file to simulate then click ok. In Wave - Default select run all. That is how the program is run.

Our modifications to the **program_all_tb.sv** testbench included:

- Replacing **program_all_pa1(.*)** with **top strm(.*)** at the top.
- Add a reset bit at the top only calls it once at the beginning:
    - **reset = 1;**
    - **#20ns reset = 0;**
- Replacing all instances of **pa1.data.ram_all[x]** with **strm.dm1.guts[x]** where x is either a variable or a constant based on the testbench.
- Loaded the following data into registers and memories:
    - Product:

```
strm.dm1.guts[1] = a;
strm.dm1.guts[2] = b;
strm.dm1.guts[3] = c;
strm.rf1.core[0] = 8'd1;
strm.rf1.core[1] = 8'd0;
strm.rf1.core[2] = 8'd0;
strm.rf1.core[3] = 8'd2;
strm.rf1.core[4] = 8'd4;
strm.rf1.core[5] = 8'd0;
strm.rf1.core[6] = 8'd0;
strm.rf1.core[7] = 8'd0;
```

    - String Match

```
strm.dm1.guts[6] = 4'b1101;
strm.rf1.core[0] = 8'd6;
strm.rf1.core[5] = 8'd32;
strm.rf1.core[2] = 8'd0;
```

strm.rf1.core[6] = 8'd7;
strm.rf1.core[3] = 8'd96;

- Closest Pair

strm.rf1.core[4] = 8'd128;
strm.rf1.core[5] = 8'd129;
strm.rf1.core[6] = 8'd255;
strm.rf1.core[7] = 8'd124;
strm.dm1.guts[124] = 8'd147;
strm.dm1.guts[125] = 8'd147;
strm.dm1.guts[126] = 8'd127;

RTL View