KeyStone Architecture Overview

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1 KeyStone Architecture

1.1 C66x CorePac

- 1.25 GhZ clock, 1 to 8 C66x core. C6678 has 8 cores
- Fixed and floating point operations
- 16-/32 bit ISA, doubled MPY

1.2 Memory Subsystem

- 32KB L1 program memory, 32KB L1 data memory
- 1MB L2 cache per cores
- 2MB Multicore Shared Memory (MSM)
- DDR3-1600 Mhz (64-bit)

1.3 Application specific Coprocessors

- 2x TCP3d: Turbo Decoder
- TCP3e: Turbo Encoder
- 2x FFT (FFt/IFFT and DFT/IDFT) Coprocessor
- 4x VCP2 for voide channel decoding
- Security accelerator
- Packet accelerator

40nm High-Performance Process

2 KeyStone Media Applications

- Medical Imaging
  - Digital Ultrasound
  - Optical Coherence Tomography
- Smart Grid
- Media and networking

3 CorePac and Memory Subsystem

3.1 CorePac

- Clocked upto 1.25 GhZ clock, 1 to 8 C66x core. C6678 has 8 cores
- Fixed and floating point operations

3.2 L1 Memory configured as cache

- 32KB L1P per core
- 32KB l1D per core
- Error detection for L1P
- Memory protection

3.3 Dedicated and Shared L2 Memory

- 512KB to 1MB L2 per core
- 2 to 4MB MSM
- Multicore Shared Memory Controller
- Error detection and correction for L2 memory
- MSM available to all cores and can be data or program

Boot ROM

4 Multicore Navigator

- Data movement within the chip
- Effective inter processor communication
- 8KB hardware queues and 64 KB descriptors
- 10 Gbps pre-fetching capability

5 Miscellaneous Elements

- Semaphore2 provides atomic accesses to shared chip-level resources
- Boot ROM
- Power Management

- Eight 64 bit timers
- Three on-chip PLLs: PLL1 for CorePacs, PLL2 for DDR3 and PLL3 for packet Acceleration
- EDMA

6 Application-Specific Coprocessors

- FFTCx2
- TCP3E, TCP3D and 4 Viterbi Coprocessor (4xVCP2) all for wireless application