ECEN2350 – Project 2, Checkpoint Submission 1

Fall, 2020

Due Friday, October 16th, end of day (0 points if late)

15 points

The checkpoint submissions are not very subtle incentive for you to begin work early on your project, and make progress through the project. Please submit only a single .pdf file, by pasting the requested information into this document. Do not submit individual Verilog or simulation output files.

Use this file as a template, and save your final document as a .pdf file, which you will upload to Canvas.

Turn in this checkpoint submission even if you do not have a completed Day of the Year counter.

1. (7 points) Verilog design code for your Day of the Year counter (1 – 99). You may either paste your code into this document or paste a screenshot of your code into this document.

```
module day_counter (ADC_CLK_10, reset, LED0, HEX0, HEX1, HEX2, HEX3, HEX4, HEX5);
    input ADC_CLK_10;
    input reset;
    output wire LED0;
    output [7:0] HEX0, HEX1, HEX2, HEX3, HEX4, HEX5;
    wire [3:0] off = 4'b1111;
    reg [7:0] BCD = 8'b0000_0001;
    wire clk;

    seg7_decoder seg7_decoder_inst_5(.in(BCD[7:4]), .out(HEX5));
    seg7_decoder seg7_decoder_inst_4(.in(BCD[3:0]), .out(HEX4));
    seg7_decoder seg7_decoder_inst_3(.in(off), .out(HEX3));
    seg7_decoder seg7_decoder_inst_2(.in(off), .out(HEX2));
    seg7_decoder seg7_decoder_inst_1(.in(off), .out(HEX1));
    seg7_decoder seg7_decoder_inst_0(.in(off), .out(HEX0));

    //Clock division
    clk_div clk_div_inst (.clk_in(ADC_CLK_10), .clk_out(clk), .led(LED0));

    always @ (posedge clk or negedge reset)
    begin
        if (reset == 0)
        begin
            BCD[3:0] <= 1;
            BCD[7:4] <= 0;
        end
        else if (BCD[3:0] < 9)
            BCD[3:0] <= BCD[3:0] + 1;
        else if (BCD[7:4] == 9 && BCD[3:0] == 9)
        begin
            BCD[3:0] <= 1;
            BCD[7:4] <= 0;
        end
        else
        begin
            BCD[3:0] <= 0;
            BCD[7:4] <= BCD[7:4] + 1;
        end
    end

endmodule
```

```
module clk_div (clk_in, clk_out, led);
    input clk_in;
    output reg clk_out;
    output reg led;
    //parameter div = 5000000;
    parameter div = 2;
    reg [22:0] counter = 23'd1;

    always @ (posedge clk_in)
    begin
        counter <= counter + 23'd1;
        if (counter >= div)
            counter <= 23'd1;
        clk_out <= (counter <= div/2) ? 1'b0 : 1'b1;
        led <= clk_out;
    end
endmodule
```

2. (5 points) Verilog testbench code for you Day of the Year. You may either paste your code into this document or paste a screenshot of your code into this document.

```
1  `timescale 1 ns / 1 ps
2  module tb_day();
3
4      reg [1:0] KEY = 2'b01;
5      reg ADC_CLK_10 = 0;
6      wire LED0 = 0;
7      wire [7:0] HEX0, HEX1, HEX2, HEX3, HEX4, HEX5;
8
9      day_counter U0
10     (
11         .ADC_CLK_10(ADC_CLK_10),
12         .reset(KEY[0]),
13         .LED0(LED0),
14         .HEX0(HEX0),
15         .HEX1(HEX1),
16         .HEX2(HEX2),
17         .HEX3(HEX3),
18         .HEX4(HEX4),
19         .HEX5(HEX5)
20     );
21
22 initial
23     begin
24         $dumpfile("output_day.vcd");
25     $dumpvars;
26             ADC_CLK_10 = ~ADC_CLK_10;
27         #10 ADC_CLK_10 = ~ADC_CLK_10;
28         #10 ADC_CLK_10 = ~ADC_CLK_10;
29         #10 ADC_CLK_10 = ~ADC_CLK_10;
30         #10 ADC_CLK_10 = ~ADC_CLK_10;
31         #10 ADC_CLK_10 = ~ADC_CLK_10;
32         #10 ADC_CLK_10 = ~ADC_CLK_10;
33         #10 ADC_CLK_10 = ~ADC_CLK_10;
34         #10 ADC_CLK_10 = ~ADC_CLK_10;
35         #10 ADC_CLK_10 = ~ADC_CLK_10;
36         #10 ADC_CLK_10 = ~ADC_CLK_10;
37         #10 ADC_CLK_10 = ~ADC_CLK_10;
38         #10 ADC_CLK_10 = ~ADC_CLK_10; KEY[0] = 0;
39     end
40
41 initial
42     begin
43         $monitor($time, " 1-99: %b%b, clock_in: %d, clock_out: %d, reset: %d", HEX5, HEX4, ADC_CLK_10, LED0, KEY[0]);
44     end
45 endmodule
```

3. (3 points) Paste a screenshot of your GTKWave simulation output into this document