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COAL LAB TASK #09

Multiplying Larger Numbers:

When multiplying large numbers, we encounter a limitation due to the fixed register size (16 or 32 bits). Standard shift operations (SHL, SHR) can only manipulate bits within the register size, leading to significant bits being dropped or lost when shifting larger numbers. This results in incorrect products. For instance, multiplying two 16-bit numbers can yield a 32-bit result, but our 16-bit registers can't accommodate this. Therefore, we need to develop a strategy to store and process partial products without overflowing the registers, ensuring accurate multiplication of large numbers.

Extended Shifting

To address the memory limitation, we employ extended shifting techniques, which enable us to manipulate and process larger numbers beyond the standard register size, ensuring accurate calculations and preventing data overflow.

The Algorithm

The extended shifting algorithm utilizes two essential instructions - SHL (Shift Left) and RCL (Rotate Carry Left) - to facilitate the efficient shifting of 32-bit numbers by 16 bits to the left, while meticulously preserving all significant bits and preventing any data loss during the process.

num1: dd 40000

shl word [num1],1

rcl word [num1+2], 1

word [num1+2], 1

In this scenario, num1 is a 32-bit number stored in memory, and we employ the SHL instruction to shift its lower 16 bits to the left, while the most significant bit is captured in the carry. Subsequently, the RCL instruction cleverly inserts this carried bit into the least significant bit position of the adjacent word, effectively concatenating the two 16-bit words and preserving the entire 32-bit value.

Conversely, when shifting right, the process is inverted. The SHR (Shift Right) and RCR (Rotate Carry Right) instructions are employed to guarantee the preservation of all significant bits, preventing any data loss during the rightward shift.

num1: dd 40000 shr word [num1+2], 1 rcr word [num1], 1 word [num1], 1

ADC (Add with Carry):

Adds two numbers and the carry flag.

Code:

[org 0x0100]

imp start

multiplicand: dd 1300

multiplier: dw 500

result: dd 0

start: mov cl, 16

mov dx, [multiplier]

checkbit: shr dx, 1

jnc skip

```
mov ax, [multiplicand]
add [result], ax
mov ax, [multiplicand+2]
adc [result+2], ax
skip: shl word [multiplicand], 1
rcl word [multiplicand+2], 1
dec cl
jnz checkbit
mov ax, 0x4c00
```

Code Explanation:

- **1.** [org 0x0100]: This line specifies the origin of the code, setting the starting address to 0x0100.
- **2. jmp start:** This line jumps to the label "start", which marks the beginning of the main code.
- **3. multiplicand:** dd 1300: This line declares a 32-bit data element named "multiplicand" and initializes it with the value 1300. The "dd" directive stands for "define doubleword".
- **4. multiplier: dw 500:** This line declares a 16-bit data element named "multiplier" and initializes it with the value 500. The "dw" directive stands for "define word".
- **5. result: dd 0:** This line declares a 32-bit data element named "result" and initializes it with the value 0.

- **6. start: mov cl, 16:** This line moves the value 16 into the CL register, which will be used as a bit counter.
- **7. mov dx, [multiplier]:** This line loads the value of the "multiplier" into the DX register.
- **8. checkbit: shr dx**, **1:** This line shifts the contents of the DX register one bit to the right, moving the rightmost bit into the carry flag.
- **9. jnc skip:** This line jumps to the label "skip" if the carry flag is zero (i.e., the rightmost bit was zero).
- **10.** mov ax, [multiplicand]: This line loads the less significant word of the "multiplicand" into the AX register.
- **11.** add [result], ax: This line adds the contents of the AX register to the less significant word of the "result".
- **12.** mov ax, [multiplicand+2]: This line loads the more significant word of the "multiplicand" into the AX register.
- **13.** adc [result+2], ax: This line adds the contents of the AX register to the more significant word of the "result", using the carry from the previous addition.
- **14. skip: shl word [multiplicand], 1:** This line shifts the contents of the "multiplicand" one bit to the left.

15. rcl word [multiplicand+2], 1: This line rotates the contents of the more

significant word of the "multiplicand" one bit to the left, moving the leftmost bit

into the carry flag.

16. dec cl: This line decrements the bit counter in the CL register.

17. jnz checkbit: This line jumps back to the label "checkbit" if the bit counter is

not zero, repeating the process until all bits have been processed.

18. mov ax, 0x4c00: This line moves the value 0x4c00 into the AX register, which

is likely used to terminate the program.

First Iteration:

skip: shl word [multiplicand], 1

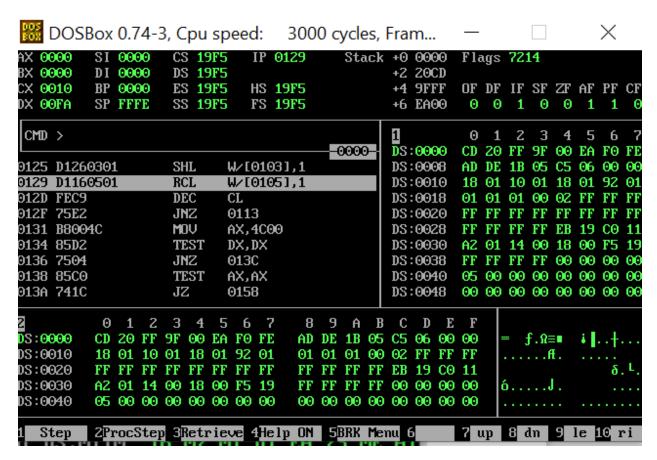
This instruction performs a left shift operation on the lower 16 bits of the multiplicand, effectively moving all bits one position to the left. As a result, the leftmost bit is transferred to the carry flag, while the rightmost bit is replaced

with a zero, effectively multiplying the multiplicand by 2.

Before: 0000010110100100

After: 0000101000101000 (binary representation after shifting left by one) in

hex A28



rcl word [multiplicand+2], 1

This instruction rotates the carry flag into the least significant bit of the upper 16 bits of the multiplicand, effectively inserting the carried bit into the most significant bit position. Since the carry flag was not set by the previous shift operation, the upper 16 bits of the multiplicand remain unchanged:

- Before rotation: 0000000000000000

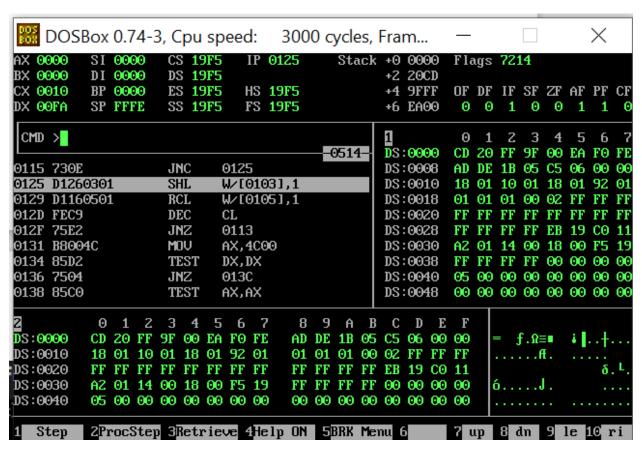
- After rotation: 0000000000000000

dec cl;

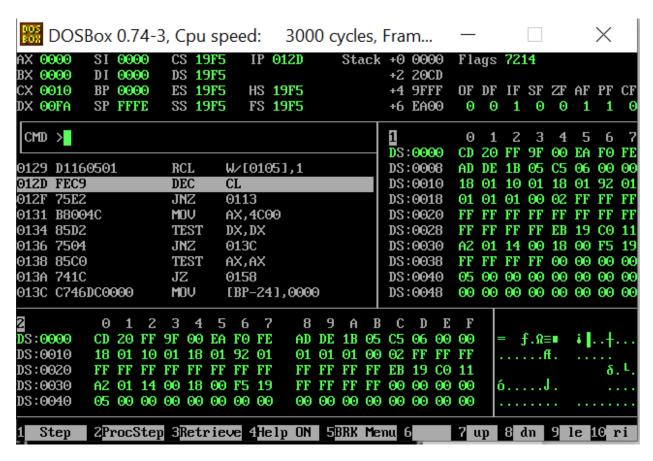
The bit counter is decremented by 1.

jnz checkbit;

If there are still bits left to process (i.e., the bit counter is not zero), the program jumps back to the 'checkbit' label to repeat the process.



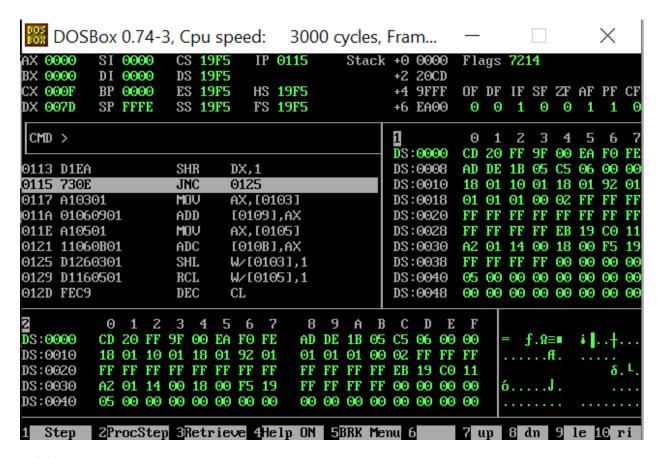
Iteration 2:



Iteration 3:

multiplicand: 000000001111101

After shift right carry flag is set.



Addition:

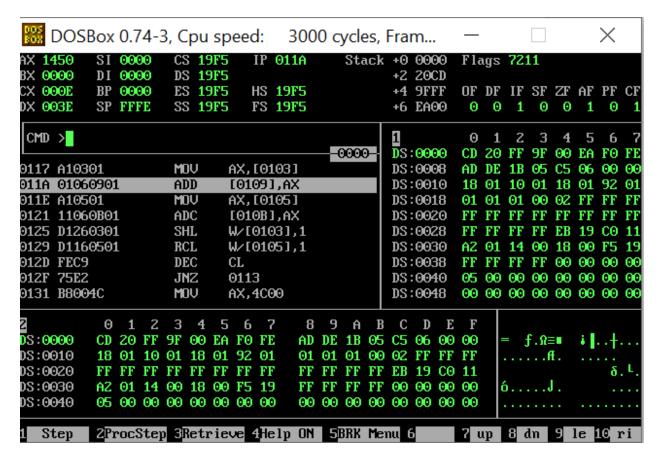
mov ax, [multiplicand]

add [result], ax; add less significant word

mov ax, [multiplicand+2]

adc [result+2], ax; add more significant word

mov the multiplicand to ax

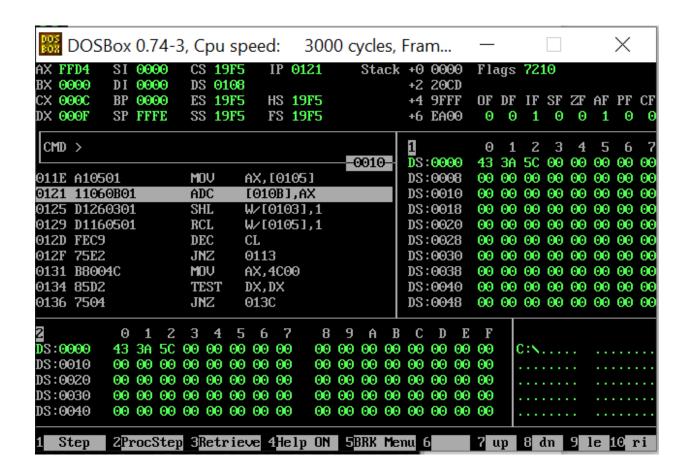


multiplicand 0001010001010000

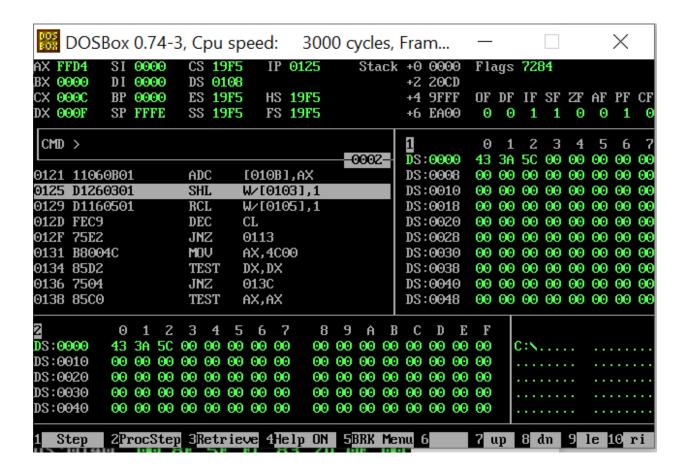
add [result], ax;

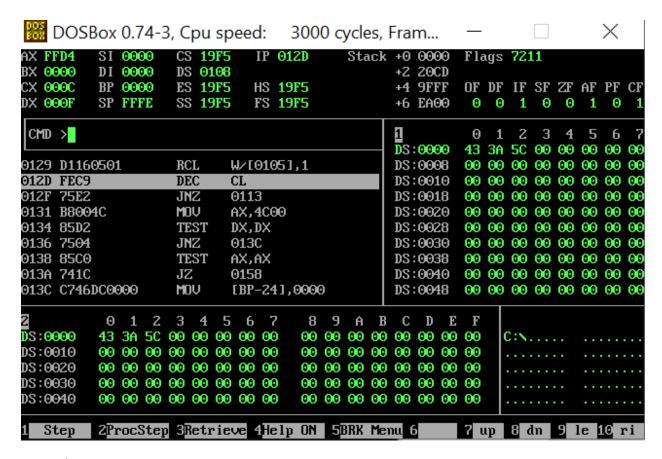
```
2
                       3
                          4
                              5
            0
               1
                                  6
          E9 0A 00 50
DS 0100
                         14
                            00
                                00 F4
             50
                     00
DS:0108
                         00
                                 10 8B
DS:0110
DS:0118
                         09
                             01
                                A1
           03
              Θ1
                 01
                     06
                                    05
DS:0120
           01
              11
                     ΘB
                         01
                             D1
                                26
DS:0128
           01 D1
                 16
                     05
                         01
DS:0130
           EZ
                 \mathbf{00}
                     4C
                             DZ
DS:0138
           85
              co
                             46
                                DC
                      1C
                                    00
DS:0140
                             7D
           00 SE
                  5E
                     FC 83
                                0E
                                    00
DS:0148
           74
              09
                 8B
                     46 F2
                             48
                                3B
```

mov ax, [multiplicand+2]

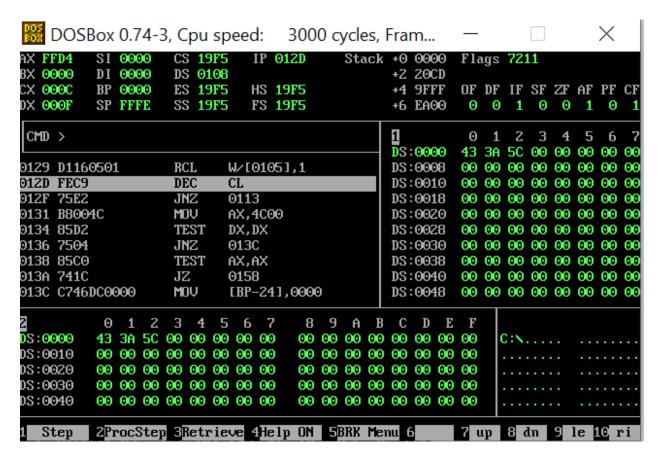


adc [result+2], ax; add more significant word

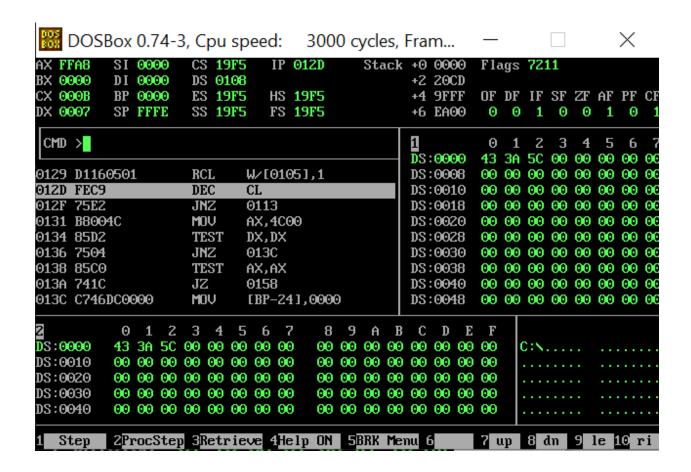




Iteration 4:



Iteration 5:



Iteration 6:

	DOSBox (.74-3, Cpu	ı speed:	3000	cycles, Fra	me	skip 0	, Pro	одга	m:	-	AFD	<u> </u>) (X
AX 0001 BX 0000	SI 000 DI 000			012D	Stack		0000 20CD	Fla	ags	729	94				
CX 000A DX 0003	BP 000 SP FFF			19F5 19F5			9FFF EA00	OF O	DF O	IF 1	SF 1	ZF 0	AF 1	PF 1	CF O
CMD >						1	.0100	0	1	2	3	4	5	6	7
9129 D1:		RCL	W∕[010	95],1		DS	:0100 :0108 :0110	01	0A 10 07	4 D	02		B1	10	8B
912D FE 912F 751 9131 B80	EZ	DEC JNZ MOV	0113	20		DS	:0118 :0120	03	01 11	01	06	09	01	A1	05
9134 851 9136 750	02	TEST	AX,4CC DX,DX			DS	:0128	01	D1	16	05	01	FE	C9	75
9136 730 9138 850 913A 743	00	JNZ TEST JZ	013C AX,AX 0158			DS	:0130 :0138 :0140	85	B8 C0 BE	74	1 C	C7	46	DC	00
	16DC0000	MOV		41,000	10		:0148					FZ			

Iteration 7:

	DOSBox 0.74	-3, Cpu s	peed:	3000	cycles, Fra	me	skip 0,	Pro	одга	m:	-	AFD	9		×
AX 0002 BX 0000		CS 19F5		012D	Stack		0000 20CD	Fla	ıgs	72:	14				
CX 0009 DX 0001	BP 0000 SP FFFE	ES 19F5 SS 19F5	HS.	19F5 19F5			9FFF EAOO	OF O	DF O	IF 1	SF 0	ZF 0	AF 1	PF 1	CF O
CMD >						1	:0100	0 E9	1 0A	2 00		4 14	5 05	6	7 F4
0129 D1:		RCL DEC	W/[010	951,1		DS:	0108	01	10 07	D7	04	00	B1	10	8B
012F 75	EZ	JNZ	0113	~~		DS:	0118	03	01	01	06	09	01	A1	0 5
0131 B80 0134 851	D2	MOV TEST	AX,4CC DX,DX			DS:	0128	01	11 D1	16	05	01	FE	C9	75
0136 75 0138 85	CO	JNZ TEST	013C AX,AX			DS:		85	B8	74	1 C	C7	46	DC	00
013A 74 013C C7	1C 46DC0000	JZ MOV	0158 [BP-24	41,000	Θ		:0140 :0148		8E 09						

Iteration 8:

!	DOSBox 0.74	-3, Cpu s	peed:	3000 cy	/cles, Fr	ame	skip 0,	Рго	одга	m:	-	٩FD			×
AX 0005 BX 0000	SI 0000	CS 19F9		012D	Stack			Fla	ıgs	72:	14				
CX 0008	DI 0000 BP 0000	ES 19F		19F5		_	20CD 9FFF	OF	DF	IF	SF	ΖF	ΑF	PF	CF
DX 0000	SP FFFE	SS 19F	5 FS	19F5		+6	EA00	0	0	1	0	0	1	1	0
CMD >						1		0	1	2			5		
0129 D1:	160501	RCL	W/[010	951,1			:0100 :0108	E9 01	0A 10	00 EB	00 09	28 00	0A B1	00 10	
012D FE		DEC JNZ	CL 0113				0110 0118	16 03		01 01		EA 09			
0131 B8		MOV	AX,4C	90			0120		11						
0134 851 0136 750	_	TEST JNZ	DX,DX 013C				:0128 :0130		D1 B8						
0138 850	CO	TEST	AX,AX			DS	0138	85	CO	74	1 C	C7	46	DC	00
013A 74: 013C C7	1C 46DC0000	JZ MOV	0158 [BP-24	41,0000			:0140 :0148		8E 09						

Iteration 9:

DC	OSBox 0.74	-3, Cpu s	peed:	3000	cycles, Fra	ame	skip 0,	Pro	одга	m:	,	AFD	_		×
	SI 0000 DI 0000	CS 19F5		012D	Stack		0000 20CD	Fla	ıgs	721	14				
CX 0007	BP 0000	ES 19F5	HS	19F5		+4	9FFF			IF		ZF	ΑF		CF
DX 0000	SP FFFE	SS 19F5	61 (19F5		+0	EA00	0	0		0	0		1	
CMD >						1	.0400	0	1		3		5		_
0129 D1160)501	RCL	W/[010	951.1	$\neg \neg$:0100 :0108	E9 01				50 00			
012D FEC9		DEC	CL				:0110					ΕA			
012F 75E2 0131 B8004	c	JNZ MOV	0113 AX,400	90			:0118 :0120					09 01			
0134 85D2		TEST	DX,DX			DS	:0128	01	D1	16	05	01	FΕ	C9	75
0136 7504 0138 8500		JNZ TEST	013C AX,AX				:0130 :0138					85 C7			
0130 03C0 013A 741C		JZ	0158				:0140					83			
013C C746D	C0000	MOV	[BP-24	11,0000		DS	:0148	74	09	8B	46	FZ	48	3B	46

Iteration 10:

AX 0005 SI 0000 BX 0000 DI 0000 CX 0006 BP 0000 DX 0000 SP FFFE	CS 19F5 IP 012D S DS 19F5 ES 19F5 HS 19F5 SS 19F5 FS 19F5	+2 20CD	Flags 7294 OF DF IF SF ZF AF PF CF 0 0 1 1 0 1 1 6
CMD >		DS:0100	0 1 2 3 4 5 6 7 E9 0A 00 00 A0 28 00 F4
0129 D1160501	RCL W/[0105],1		01 10 EB 09 00 B1 10 8H
012D FEC9	DEC CL	DS:0110	16 07 01 D1 EA 73 0E A1
012F 75E2	JNZ 0113	DS:0118	03 01 01 06 09 01 A1 05
0131 B8004C	MOV AX,4COO	DS:0120	01 11 06 0B 01 D1 26 0 3
0134 85D2	TEST DX,DX	DS:0128	01 D1 16 05 01 FE C9 75
0136 7504	JNZ 013C	DS:0130	E2 B8 00 4C 85 D2 75 04
0138 85C0	TEST AX,AX	DS:0138	85 CO 74 1C C7 46 DC 00
013A 741C	JZ 0158	DS:0140	00 8E 5E FC 83 7D 0E 06
013C C746DC0000	MOV [BP-241,0000	DS:0148	74 09 8B 46 F2 48 3B 46

Iteration 11:

AX 0005 SI 0000 BX 0000 DI 0000	CS 19F9		Stack +0 0000 +2 200D	Flags 72	214		
CX 0005 BP 0000 DX 0000 SP FFFE	ES 19F9 SS 19F9		+4 9FFF +6 EA00	OF DF 11 Θ Θ :		7F AF 0 1	PF CF 1 0
CMD >			1 DS:0100	0 1 2 E9 0A 00	_	4 5 10 51	6 7 00 F4
0129 D1160501 012D FEC9	RCL DEC	W/[0105],1 CL	DS:0108 DS:0110	01 10 EI 16 07 0			
012F 75E2	JNZ	0113	DS:0118	03 01 0	06 6	9 01	A1 05
0131 B8004C 0134 85D2	MOV TEST	AX,4C00 DX,DX	DS:0120 DS:0128	01 11 00 01 D1 10			
0136 7504 0138 8500	JNZ TEST	013C AX.AX	DS:0130 DS:0138	E2 B8 00 85 C0 74			
013A 741C 013C C746DC0000	JZ MOV	0158 [BP-24],0000	DS:0140 DS:0148	00 8E 5I	FC 8	3 7D	0E 00

Iteration 12:

AX 0005 SI 0000 BX 0000 DI 0000 CX 0004 BP 0000 DX 0000 SP FFFE	CS 19F! DS 19F! ES 19F! SS 19F!	5 HS 19F5	Stack +0 0000 +2 20CD +4 9FFF +6 EA00	Flags 7		ZF 0	AF 1	PF 1	CF O
CMD > 0129 D1160501 012D FEC9 012F 75E2 0131 B8004C 0134 85D2 0136 7504 0138 85C0 013A 741C 013C C746DC0000	RCL DEC JNZ MOV TEST JNZ TEST JZ MOV	W/[0105],1 CL 0113 AX,4C00 DX,DX 013C AX,AX 0158 [BP-24],0000	DS:0100 DS:0108 DS:0110 DS:0118 DS:0120 DS:0128 DS:0130 DS:0138 DS:0140 DS:0148	E9 0A 0	EB 09 01 D1 01 06 06 0B 16 05 00 4C 74 1C 5E FC	80 00 EA 09 01 01 85 C7 83	B1 73 01 D1 FE D2 46 7D	00 10 0E A1 26 C9 75 DC 0E	8B A1 05 03 75 04 00

Iteration 13:

DOSBox 0.7	4-3, Cpu speed:	3000 cycles, F	rameskip 0	, Program:	AFC) – X
AX 0005 SI 0000 BX 0000 DI 0000	CS 19F5 IP DS 19F5	012D Stac	k +0 0000 +2 20CD	Flags 72	54	
CX 0003 BP 0000 DX 0000 SP FFFE		19F5 19F5	+4 9FFF +6 EA00	0F DF IF 0 0 1	SF ZF 0 1	AF PF CF 1 1 0
CMD >			DS:0100	0 1 2 E9 0A 00		5 6 7 45 01 F4
0129 D1160501 012D FEC9	RCL W/[010	051,1	DS:0108 DS:0110	01 10 EB	09 00	
012F 75E2	JNZ 0113	00	DS:0118	03 01 01	06 09	01 A1 05
0131 B8004C 0134 85D2	MOV AX,4CO TEST DX,DX		DS:0120 DS:0128	01 D1 16	05 01	D1 26 03 FE C9 75
0136 7504 0138 8500	JNZ 013C TEST AX,AX		DS:0130 DS:0138	85 CO 74	1C C7	DZ 75 04 46 DC 00
013A 741C 013C C746DC0000	JZ 0158 MOV [BP-2	41,0000	DS:0140 DS:0148			7D OE 00 48 3B 46

Iteration 14:

AX 0005 SI 0000	CS 19F5 IP 012D	Stack +0 0000	Flags 7254 OF DF IF SF ZF AF PF CF 0 0 1 0 1 1 0
BX 0000 DI 0000	DS 19F5	+2 20CD	
CX 0002 BP 0000	ES 19F5 HS 19F5	+4 9FFF	
DX 0000 SP FFFE	SS 19F5 FS 19F5	+6 EA00	
CMD > 0129 D1160501 0120 FEC9 012F 75E2 0131 B8004C 0134 85D2 0136 7504 0138 85C0 013A 741C 013C C746DC0000	RCL W/[0105],1 DEC CL JNZ 0113 MOU AX,4C00 TEST DX,DX JNZ 013C TEST AX,AX JZ 0158 MOU [BP-24],0000	DS:0100 DS:0108 DS:0110 DS:0118 DS:0120 DS:0128 DS:0130 DS:0138 DS:0140 DS:0148	0 1 2 3 4 5 6 7 E9 0A 00 00 00 8A 02 F4 01 10 EB 09 00 B1 10 8B 16 07 01 D1 EA 73 0E A1 03 01 01 06 09 01 A1 05 01 D1 16 05 01 FE C9 75 E2 B8 00 4C 85 D2 75 04 85 C0 74 1C C7 46 DC 00 00 8E 5E FC 83 7D 0E 00 74 09 8B 46 F2 48 3B 46

Iteration 15:

i [OOSBox 0.74	-3, Cpu s	speed:	3000	cycles, Fr	ame	skip 0	, Pro	одга	m:	-	AFD	<u>_</u>) (×
AX 0005	SI 0000	CS 19F	5 IP	012D	Stack	+0	0000	Fla	ags	725	54				
BX 0000	DI 0000	DS 19F	5			+2	20CD								
CX 0001	BP 0000	ES 19F	5 HS	19F5		+4	9FFF	\mathbf{OF}	DF	\mathbf{IF}	SF	ΖF	ΑF	\mathbf{PF}	CF
DX 0000	SP FFFE	SS 19F	5 FS	19F5		+6	EA00	0	0	1	0	1	1	1	0
CMD >						1		0	1	2	3	4	5	6	7
						DS	0100	E9	ΘA	00			14	05	F4
0129 D116	50501	RCL	W/[010	951,1		DS	:0108	01	10	EB	09	00	B1	10	8B
O1ZD FECS	9	DEC	CL			DS	:0110	16	07	01	D1	ΕA	73	ΘE	A1
012F 75E2	2	JNZ	0113			DS	:0118	03	01	01	06	09	01	A1	0 5
0131 B800	94C	MOV	AX,4C	90		DS	:0120	01	11	06	\mathbf{OB}	01	D1	26	03
0134 85D2	2	TEST	DX,DX			DS	:0128	01	D1	16	05	01	\mathbf{FE}	C9	75
0136 750	1	JNZ	013C			DS	:0130	EZ	B8	00	4 C	85	DZ	75	04
0138 8500		TEST	AX,AX			DS	:0138	85	CO	74	1 C	C7	46	DC	00
013A 7410		JZ	0158			DS	:0140	00	8E	5E	FC	83	7D	ΘE	00
013C C746	5DC0000	MOV	[BP-24	41,0000	9	DS	:0148	74	09	8B	46	FZ	48	3B	46