Chapter 6

- MOSFET Operation
  - Capacitance
    - Accumulation
    - Depletion
    - Inversion
  - IV Characteristics
    - Linear
    - Saturation
    - Spice Models
  - Short Channel
    - LDD
    - Scaling
    - Hot Carriers
    - Oxide Breakdown
    - DIBL
    - Body Effect
    - Gate Tunneling

Capacitance - Accumulation

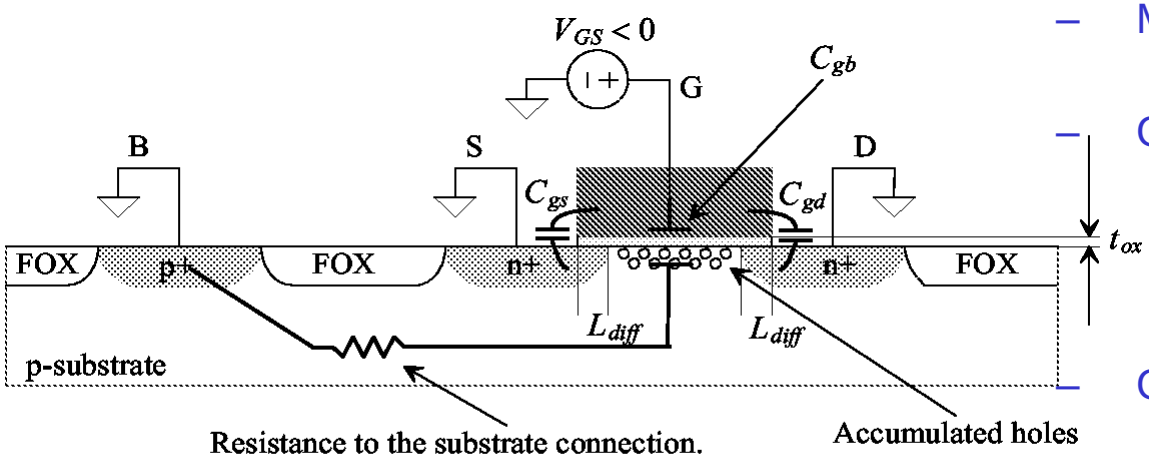


Figure 6.2 Cross-sectional view of a MOSFET operating in accumulation.

DESCRIPTION

- NFET, Vgs<0 ATTRACTS + HOLES
- MAJORITY CARRIERS AT SURFACE
- GATE TO BULK CAPACITANCE
  - POLY GATE
  - P+ HOLES AT SURFACE
  - $C_{GB} = \varepsilon (L_{EFF}) (W_{DRAWN}) / t_{OX}$
- GATE TO SOURCE/DRAIN CAP
  - POLY GATE
  - N- ELECTRONS AT SURFACE
  - $C_{GS} = \varepsilon (L_{DIFF} (W_{DRAWN}) / t_{OX}$
- SUBSTRATE RESISTANCE
  - CANNOT NEGLECT
- WHAT IS NORMAL BIASING?

Capacitance - Depletion

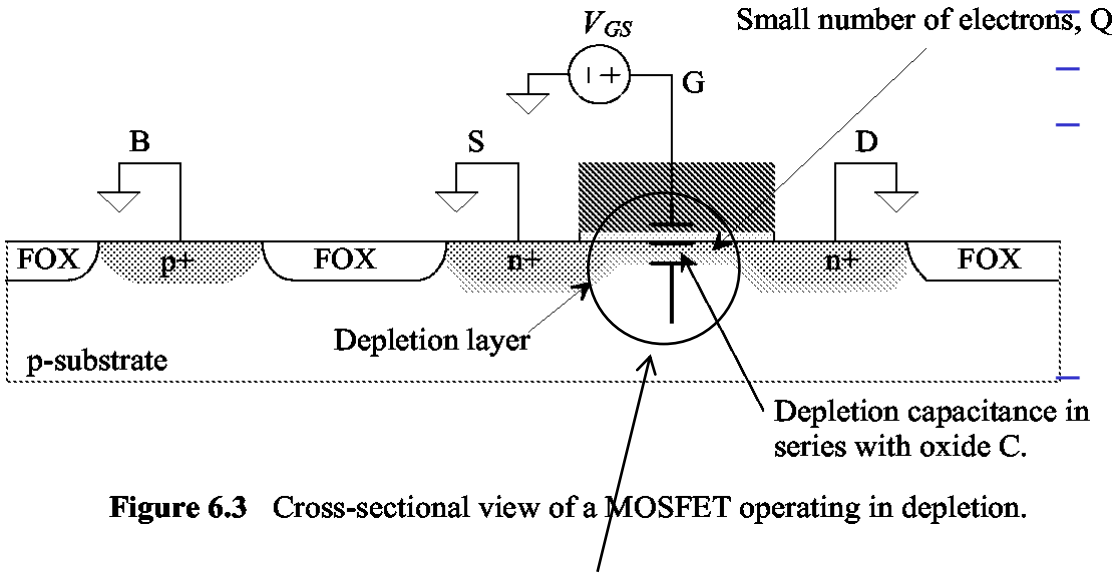


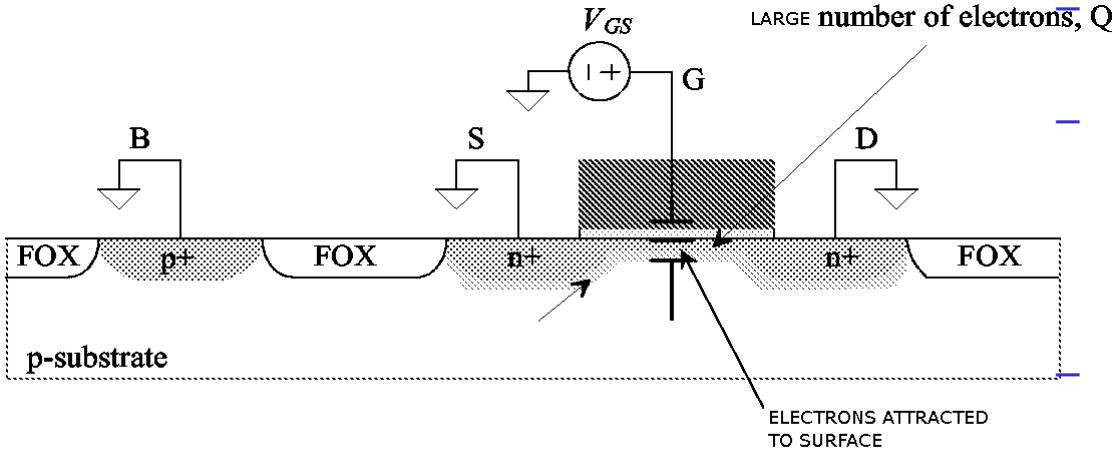
Figure 6.3 Cross-sectional view of a MOSFET operating in depletion.

Bottom Plate of Capacitor is moving "down", further Into the substrate

DESCRIPTION

- NFET, Vgs BETWEEN RANGES
- NEITHER CARRIER AT SURFACE
- IMMOBILE IONS LEFT
- GATE TO CHANNEL CAPACITANCE
  - POLY GATE
  - SOME N- ELECTRONS
  - APPROX $C=\varepsilon A / t_{ox}$
- DEPL TO BULK CAPACITANCE
  - SOME N- ELECTRONS SURFACE
  - NO ANALYTICAL EQUATION
- GATE TO SOURCE/DRAIN CAP
  - POLY GATE
  - N+ ELECTRONS AT SURFACE
  - $C_{GS} = \varepsilon (L_{DIFF} (W_{DRAWN}) / t_{OX}$
- WHAT IS OPERATING POINT?

Capacitance - Inversion



DESCRIPTION

- NFET, Vgs>Vtn
- N- ELECTRONS AT SURFACE
- GATE TO CHANNEL CAPACITANCE
  - POLY GATE
  - N- ELECTRONS
  - $C=\varepsilon A / t_{ox}$
- GATE TO SOURCE/DRAIN CAP
  - POLY GATE
  - N+ ELECTRONS AT SURFACE
  - $C_{GS} = \varepsilon (L_{DIFF} (W_{DRAWN}) / t_{OX}$
- WHAT IS OPERATING POINT?

CV CURVE

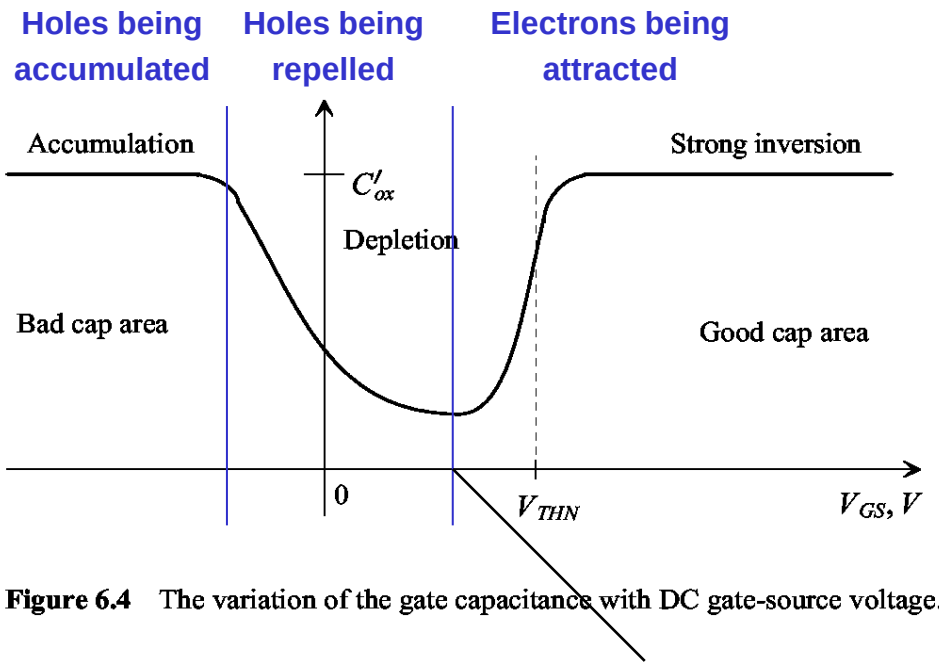


Figure 6.4 The variation of the gate capacitance with DC gate-source voltage.

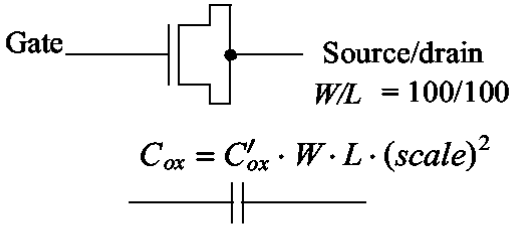


Figure 6.5 Using the MOSFET as a capacitor.

DESCRIPTION

- KEEP IN MIND OPERATING POINT
- ACCUMULATION != GOOD CAP
  - SERIES RESISTANCE TO TAP
- CAN USE MOSFET AS CAP
  - SHORT SOURCE TO DRAIN
  - IF VGATE CHANGES, VARACTOR
- SHOULD UNDERSTAND EACH CAP

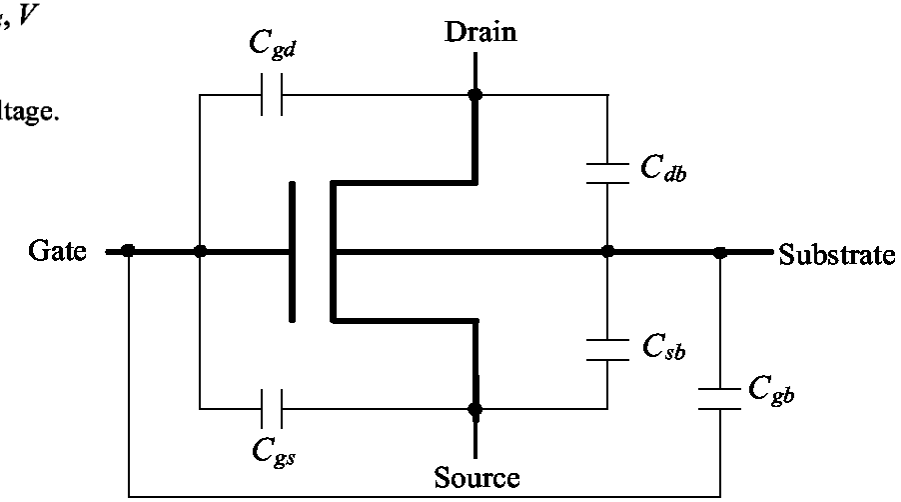


Figure 6.6 MOSFET capacitances.

- IV TERMINLOGY

ID	DRAIN CURRENT → IMPLIES DRAIN TO SOURCE (IDS) WHERE ELSE WOULD CURRENT GO FROM-TO?
IDLIN	IDS IN LINEAR REGION
IDSAT	IDS IN SATURATION REGION
μ_n	MOBILITY OF ELECTRONS
W	WIDTH OF CHANNEL
L	LENGTH OF CHANNEL (CT-CT DIRECTION)
C_{OX}	GATE OXIDE CAPACITANCE
V_{GS}	GATE TO SOURCE POTENTIAL
V_{tn}	TRANSISTOR THRESHOLD FOR NFET
V_{DS}	DRAIN TO SOURCE POTENTIAL
V_{DS-SAT}	SATURATION VDS
V_{EFF}	VGS – VTN, HOW FAR ABOVE THRESHOLD IS THE GATE

IV VS. VDS CURVE

FROM MARTIN

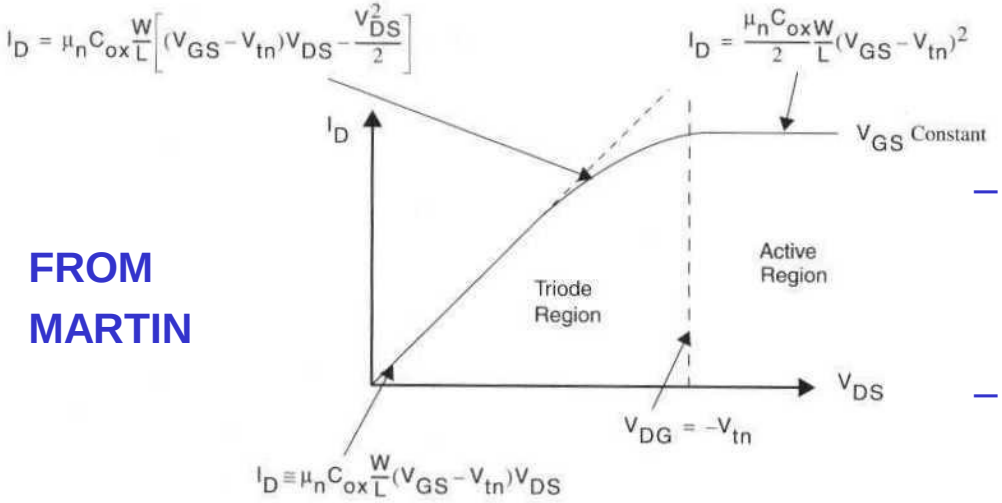


Figure 3.20 The I_D versus V_{DS} curve for an ideal MOS transistor. For $V_{DG} > -V_{tn}$, I_D is approximately constant.

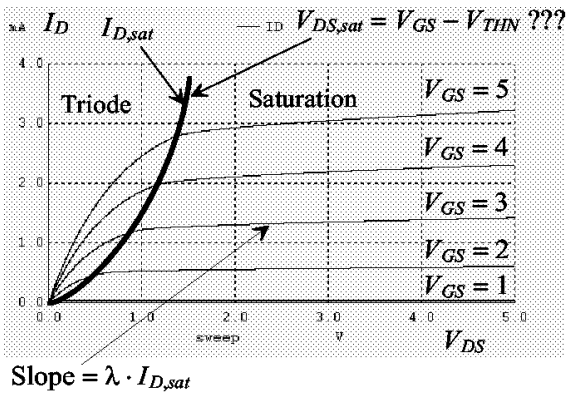
DESCRIPTION

- LINEAR REGION
  - CHANNEL IS INVERTED
  - V=IR IS LINEAR REGION
- SATURATION REGION
  - CURRENT IS CONSTANT
  - NO DEPENDENCE NO VDS
- TRANISTION REGION
  - NEED FULL EQUATION

Three regions of operation:

•Linear or Triode Region	Vds << Veff	channel inverted
•Saturation or Active Region	Vds > Veff	channel pinched off
•Transition region	Vdg ~ Vt or Vds ~ Veff	beginning of pinch off

IDS vs. VDS (SATURATION)



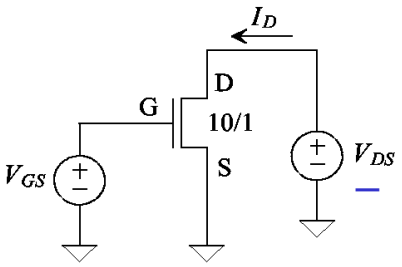


Figure 6.11 Characterisitics of a long-channel NMOS device.

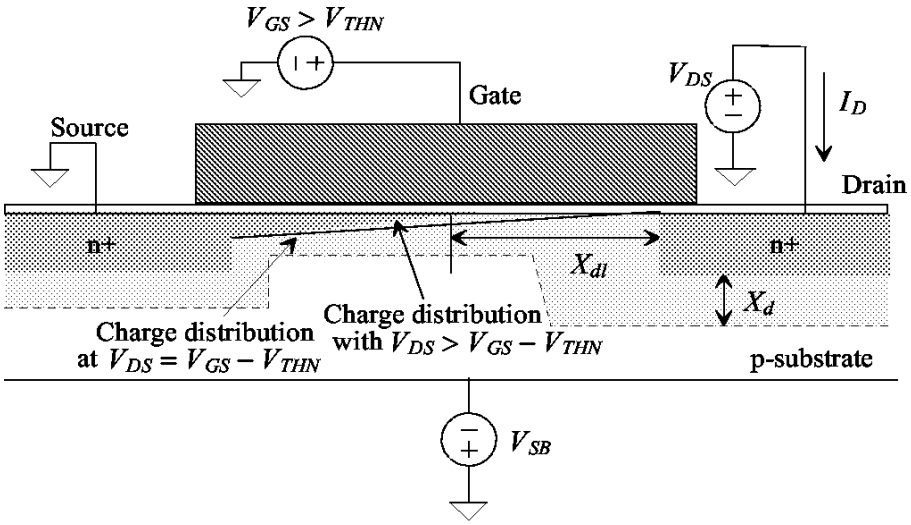


Figure 6.10 The MOSFET in saturation (pinched off).

DESCRIPTION

- IDS vs. VDS, VARY VGS
  - AS VGS INCR, R DECR
  - VDsat, WHERE PINCHOFF OCCURS
  - VGD=VT PINCHOFF
- TRANSCONDUCTANCE PARM
  - $K_{PN}=\mu_N C_{OX}=\mu_N \varepsilon_{OX}/t_{OX} \sim 120uA/V^2$
  - $K_{PP}=\mu_P C_{OX}=\mu_P \varepsilon_{OX}/t_{OX} \sim 40uA/V^2$
- MOBILITY DIFFERENCES
  - $\mu_N=650\ cm^2/\ V\ sec$
  - $\mu_P=250\ cm^2/\ V\ sec$

IDS vs. VGS (BODY EFFECT)

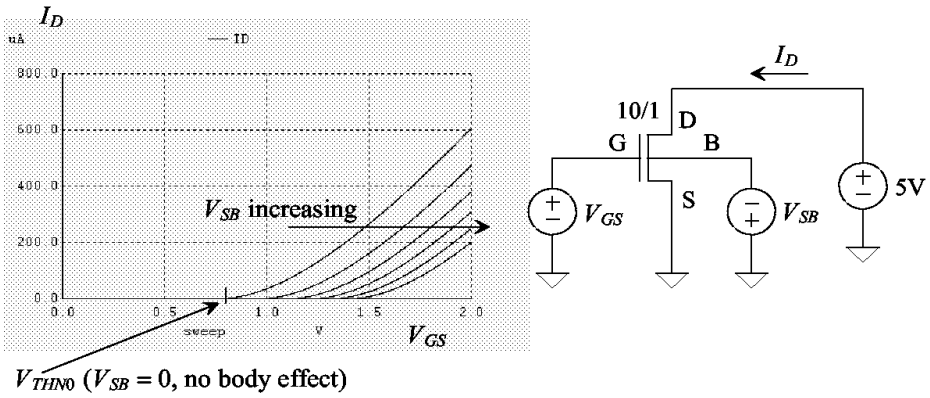


Figure 6.13 Threshold voltage and body effect.

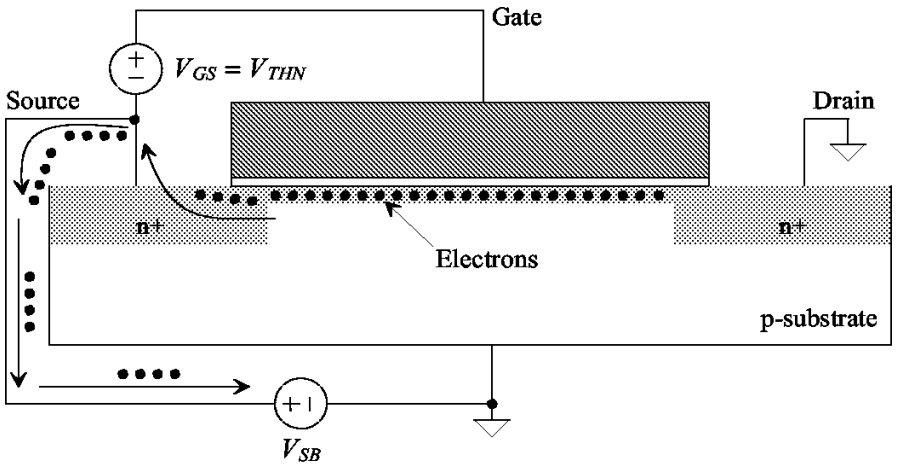


Figure 6.15 Qualitative description of body effect.

DESCRIPTION

- IDS vs. VGS, VARY VSB
  - DETERMINES Vt
  - BODY BIAS EFFECT
- BODY BIAS
  - AS VSB INC, e- GO TO SOURCE
  - DEPL DEPTH INCR
  - HARDER TO INVERT SURFACE
- LOG IDS
  - SHOWS Ioff LEAKAGE

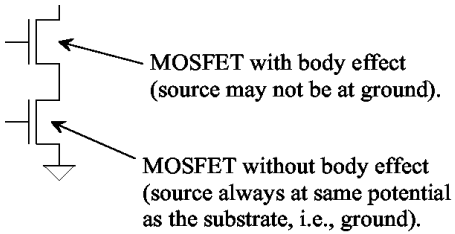


Figure 6.14 How an NMOS can have body effect.

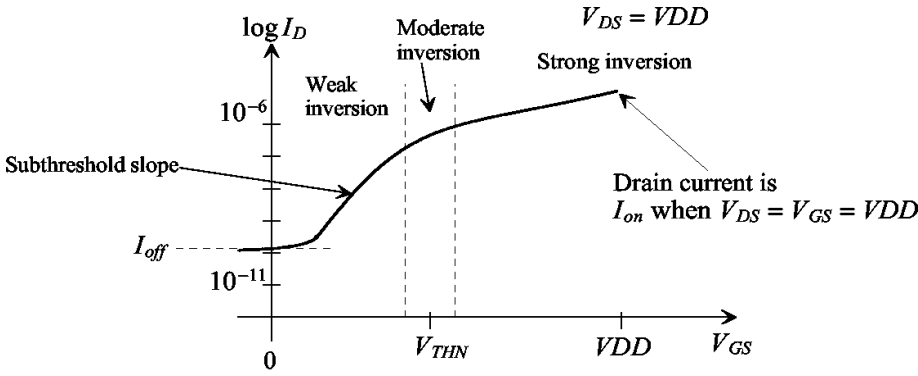


Figure 6.16 Drain current plotted from weak to strong inversion.

IV CURVE SUMMARY

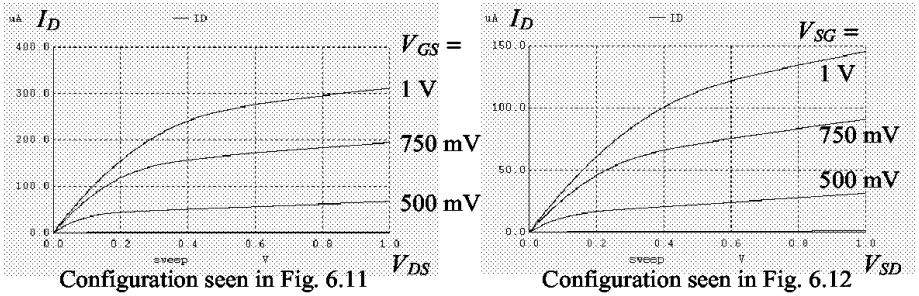


Figure 6.19 Current-voltage characteristics for 50 nm MOSFETs.

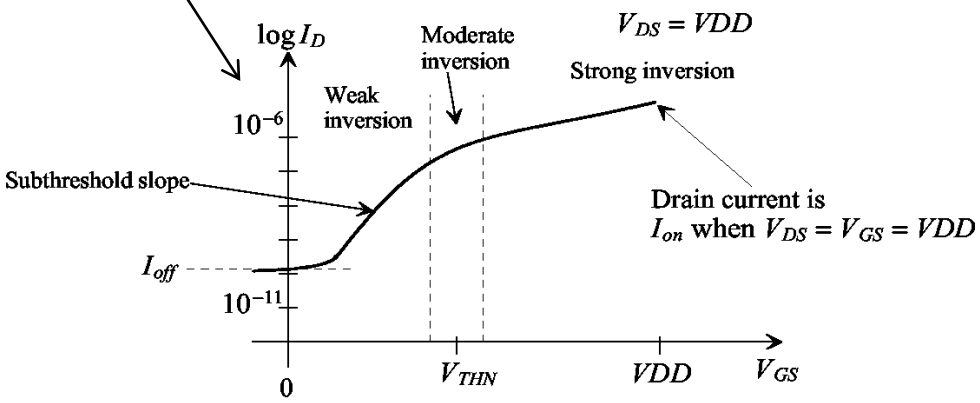


Figure 6.16 Drain current plotted from weak to strong inversion.

DESCRIPTION

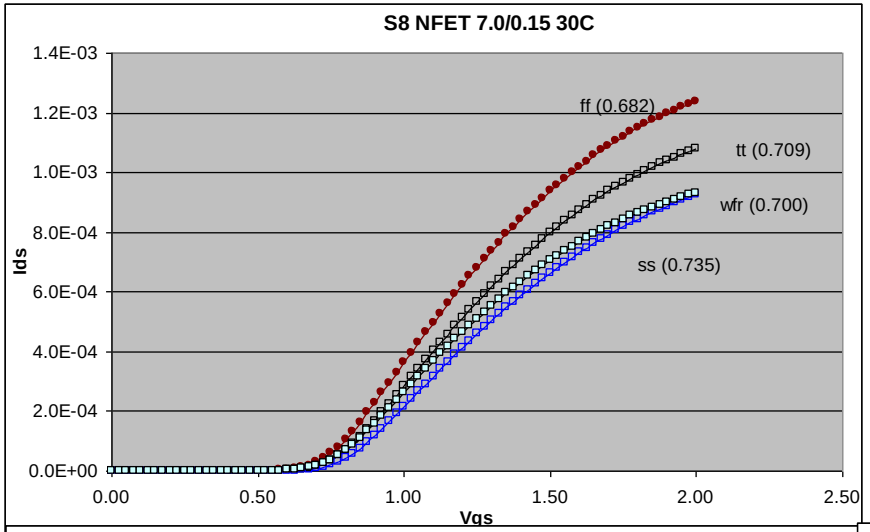
IDS VS. VDS, VARY VGS
- LINEAR, SATURATION REGIONS
- DOES NOT SHOW Vt
- MAY SHOW SHORT CH EFFECTS

IDS VS. VGS, VARY VSB
- SHOWS Vt
- SHOWS BODY EFFECT

IDS VS. VGS, LOG SCALE
- DOES NOT SHOWS Vt
- SHOWS OFF-STATE CURRENT
- SHOWS SSLP

SHORT CHANNEL EFFECTS (SCE)
- Leff IS SMALLER THAN Ldrawn
- USE LDD TO MITIGATE IMPACT
- DRAIN ENGINEERING

IDS vs. VGS EXAMPLES



DESCRIPTION

Vt VARIES WITH PROCESS

- SHAPE OF CURVE CHANGES
- Vt DERIVED AT MAX INFLECTION
  - SMALL OFFSET OF VDS APPLIED

LOG SCALE SHOWS Ioff