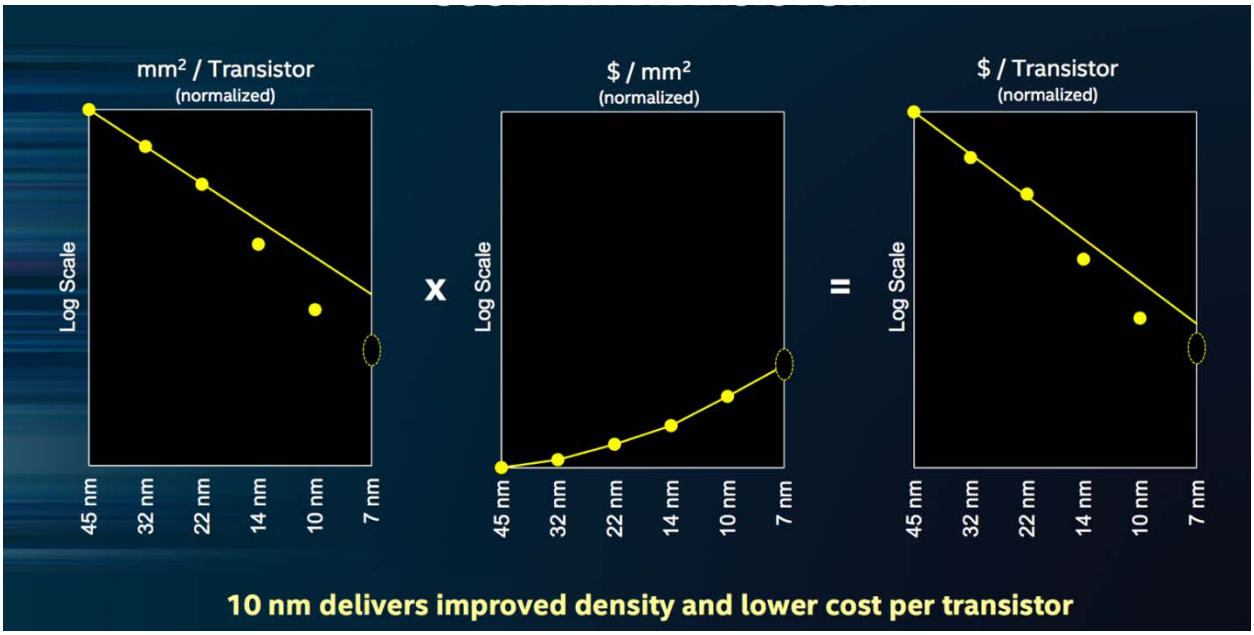
INTEL NEWS FACT SHEET

Intel's 10 nm Technology: Delivering the Highest Logic Transistor Density in the Industry Through the Use of Hyper Scaling

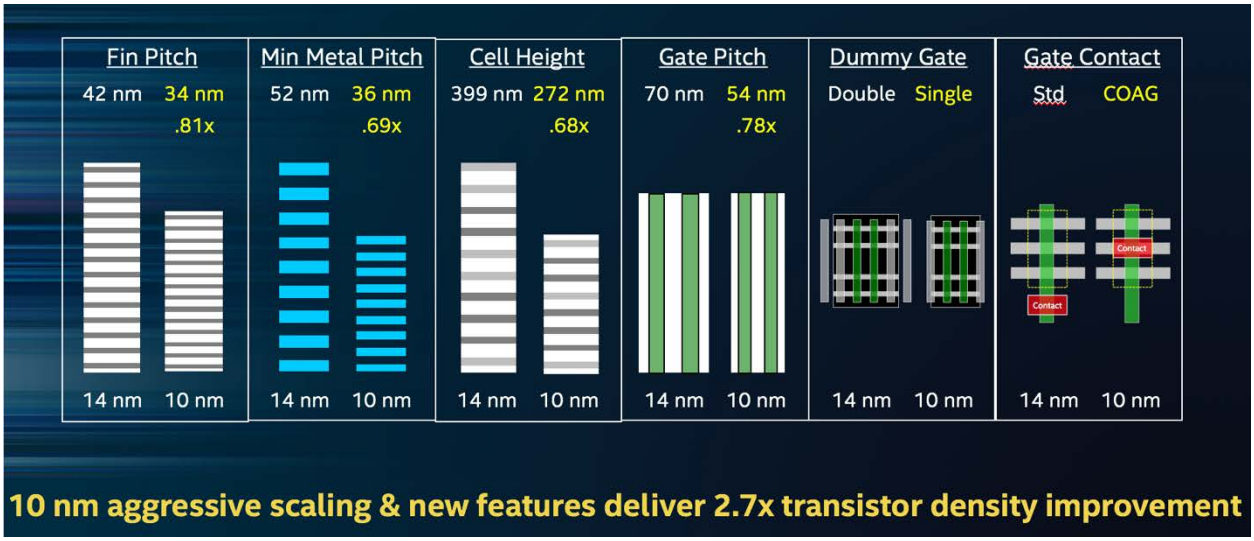
Intel's 10 nm process utilizes third-generation FinFET technology and is estimated to be a full generation ahead of other "10 nm" technologies. The use of hyper scaling on Intel's 10 nm technology extracts the full value of multi-patterning schemes and allows Intel to continue the benefits of Moore's Law economics by delivering transistors that are smaller and have lower cost-per-transistor. Intel's 10 nm process technology will be used to fabricate the full range of Intel products serving the client, server and other market segments.

Cost Per Transistor

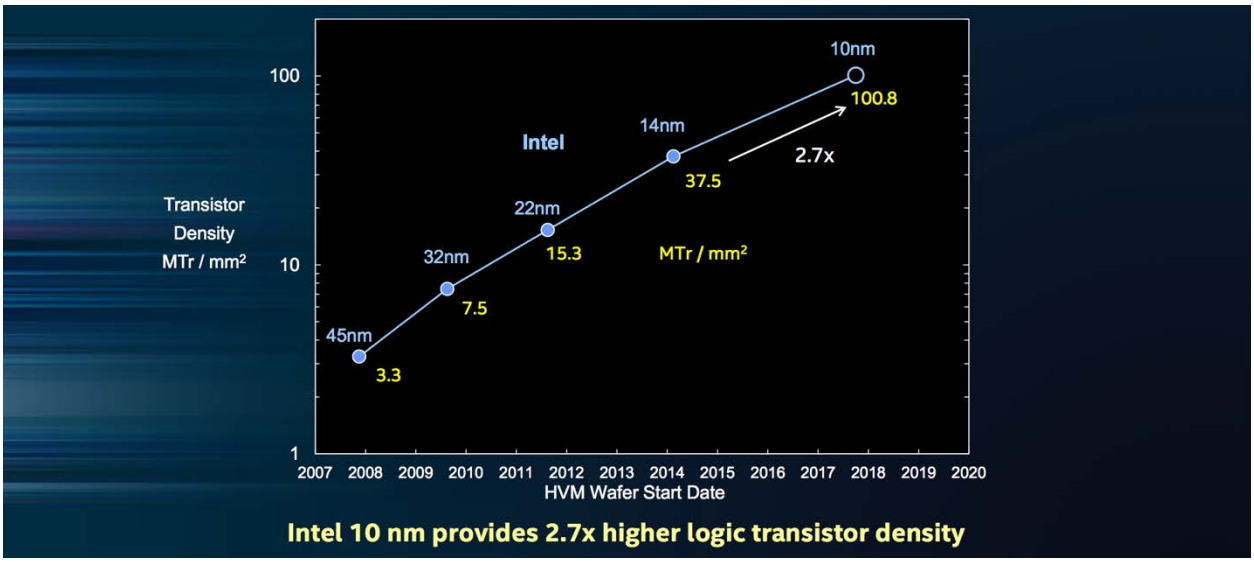


The minimum gate pitch of Intel's 10 nm process shrinks from 70 nm to 54 nm and the minimum metal pitch shrinks from 52 nm to 36 nm. These smaller dimensions enable a logic transistor density of 100.8 mega transistors per mm^2, which is 2.7x higher than Intel's previous 14 nm technology and is expected to be approximately 2x higher than other industry 10 nm technologies.

10 nm Hyper Scaling

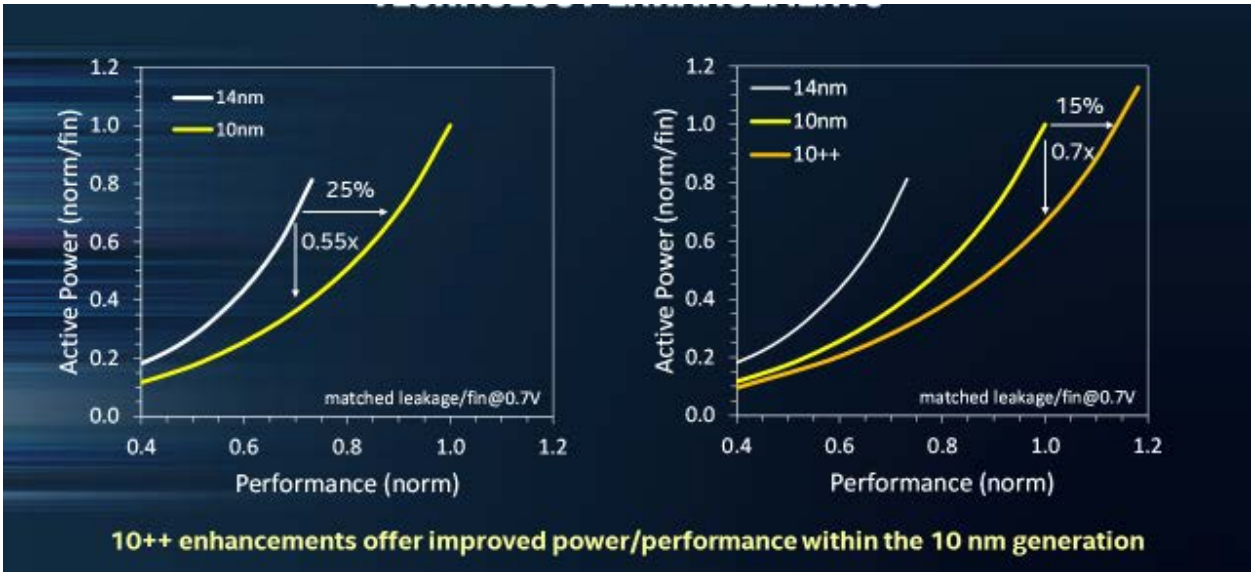


Logic Transistor Density



Intel's 10 nm process delivers up to 25 percent better performance and 45 percent lower power than the previous 14 nm technology. A new, enhanced version of the 10 nm process, called 10++, boosts the performance an additional 15 percent while reducing power by another 30 percent.

Technology Enhancements



Intel Custom Foundry offers the Intel 10 nm process to customers through two design platforms: 10GP (general purpose) and 10HPM (high performance mobile). These platforms include broad silicon-validated IP portfolios, ARM Libraries and POP Kits, and fully integrated turnkey foundry services and support.