INVESTOR MEETING

2015 SANTA CLARA

ADVANCING MOORE'S LAW

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Executive Vice President

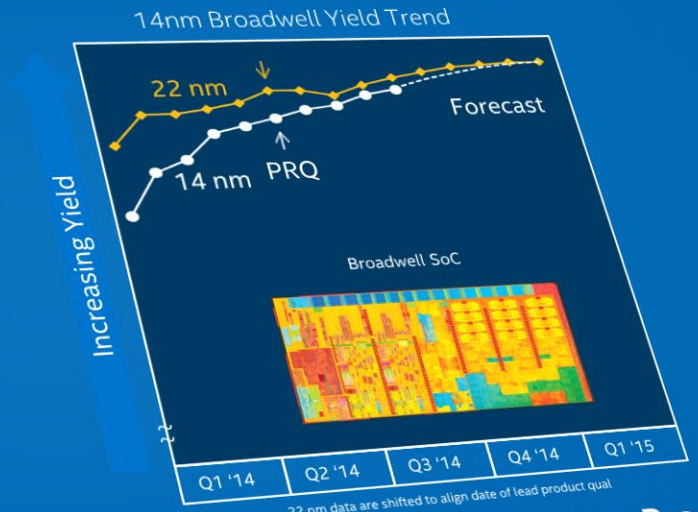
General Manager, Technology and Manufacturing Group

intel INVESTOR MEETING 2015 SANTA CLARA

AGENDA

- Progress
  - 14nm Update
  - Cost per Transistor Trend
- Economics of Moore's Law
  - What does it take to afford to continue?
- Competitiveness
- Forward looking options

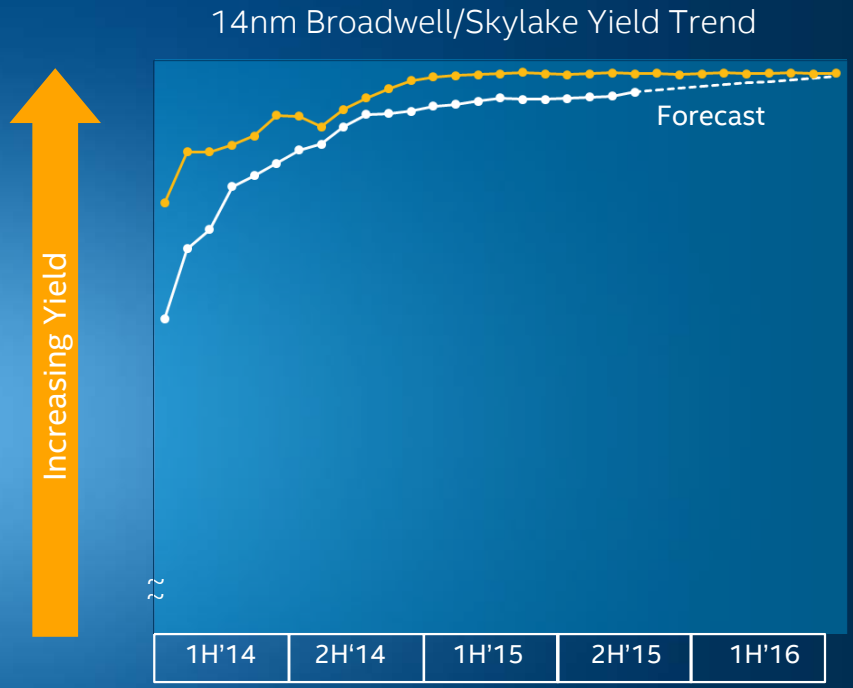
14 NM PRODUCT YIELD IS IN HEALTHY RANGE



22nm Is Intel's Highest Yielding Process Ever

Investor Meeting
2014

14 NM YIELD IS MATURING

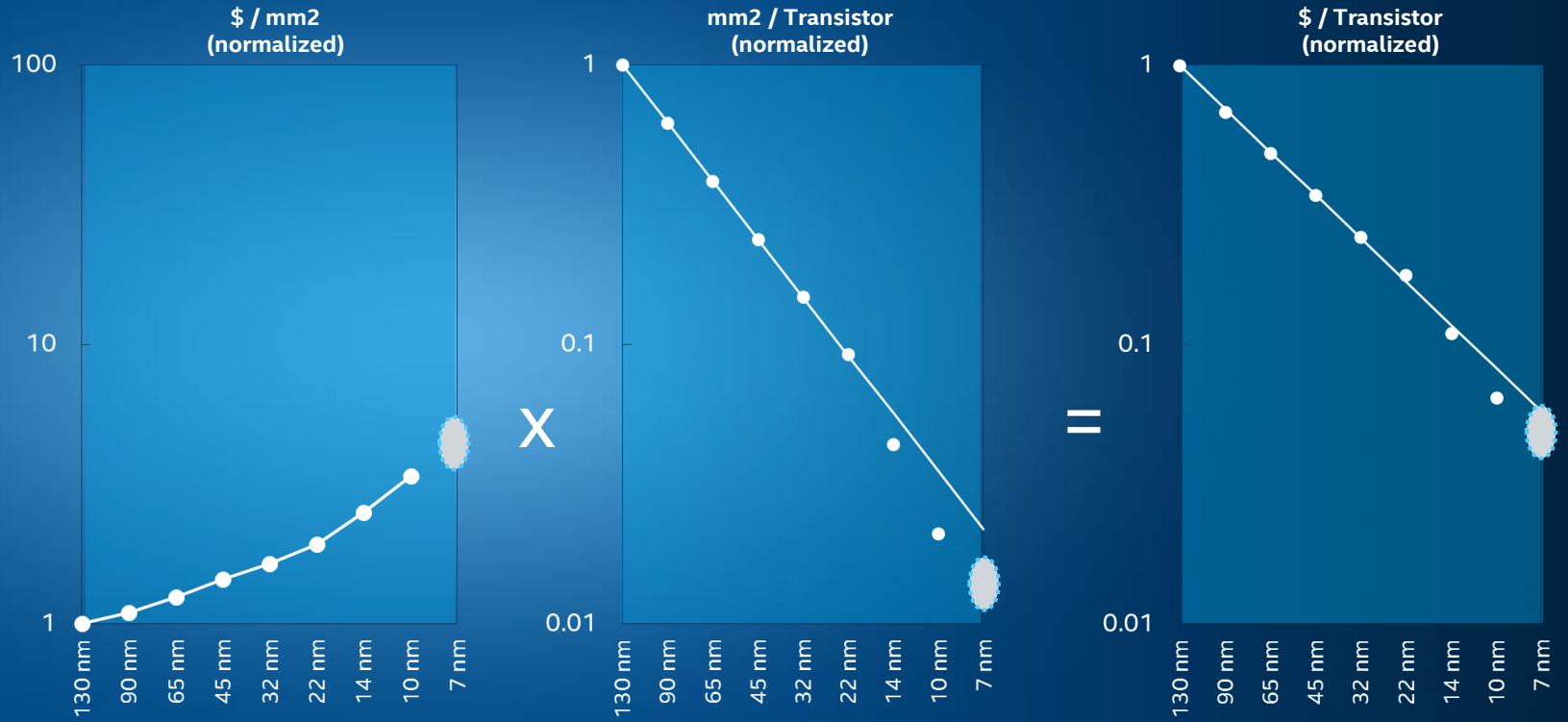


22 nm data are shifted to align date of lead product qual

Trending to match 22nm yields

Source: Intel

COST PER TRANSISTOR TREND



Source: Intel estimate, based upon available information and subject to change

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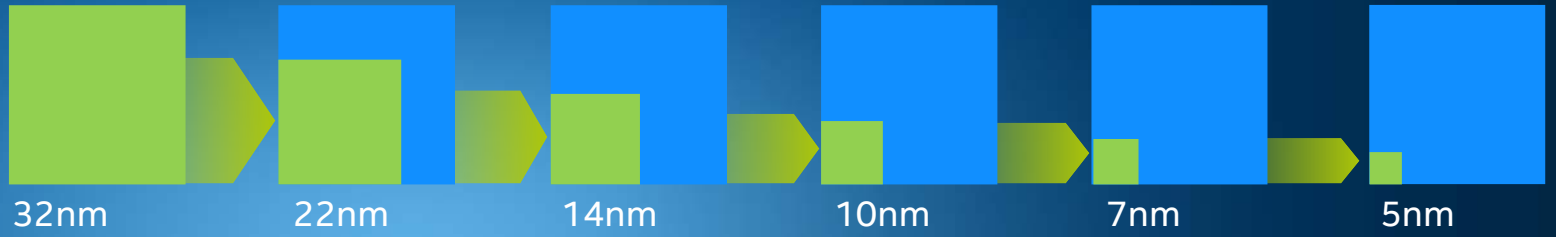
MOORE'S LAW ENABLES INNOVATION AND COST REDUCTIONS



Same circuitry half the space (cost reduction)

OR

Twice the circuitry in the same space (architectural innovation)

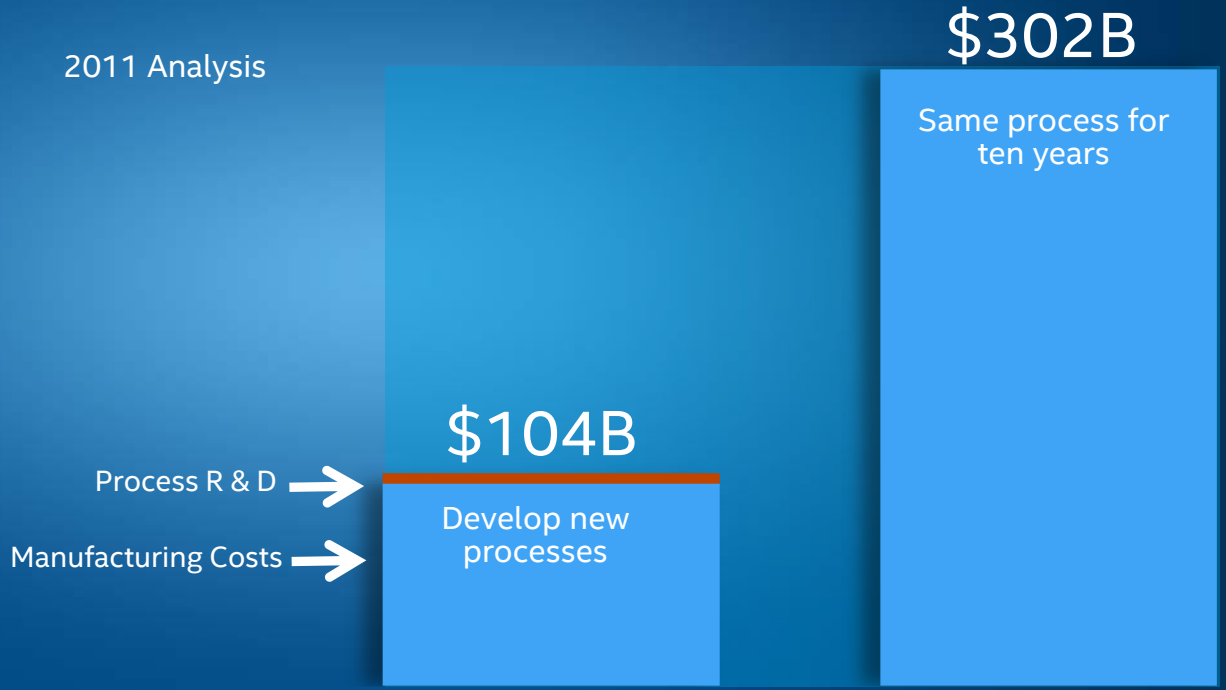
=

Option to design for optimal performance/cost

Source: Intel

ADVANCING PROCESS TECHNOLOGY LOWERS COSTS

Ten Year Model of Manufacturing and Process R & D

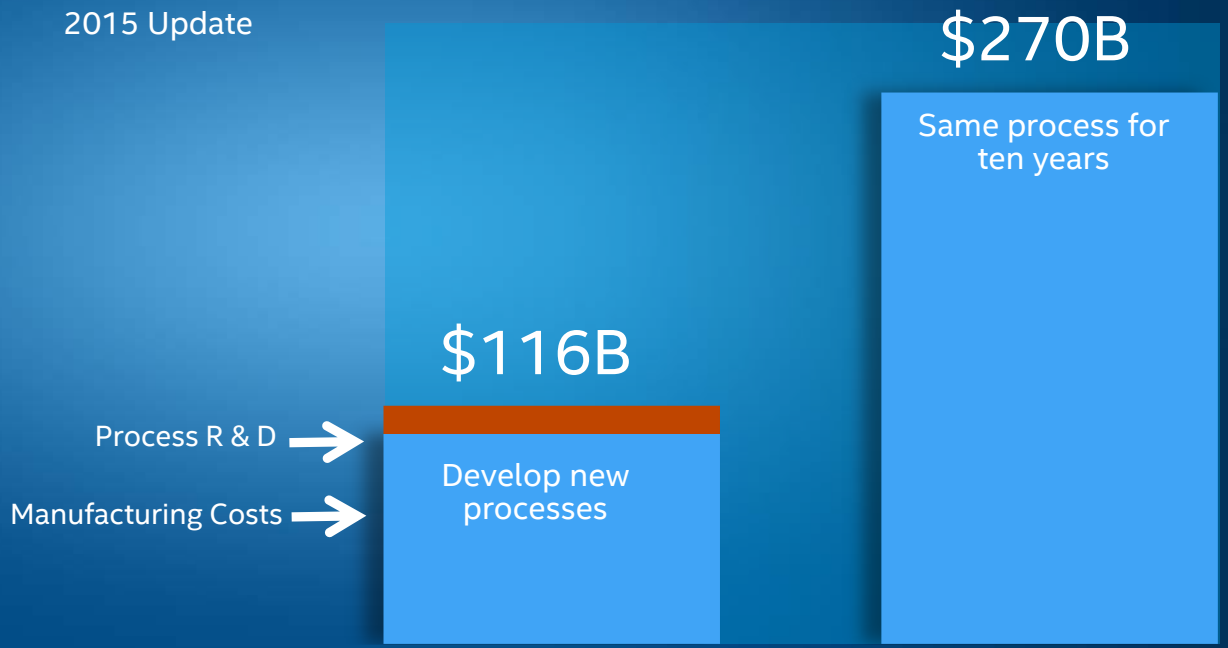


Assumptions are theoretical and not forecasts.

Source: Intel

ADVANCING PROCESS TECHNOLOGY LOWERS COSTS

Ten Year Model of Manufacturing and Process R & D



Assumptions are theoretical and not forecasts.

Source: Intel

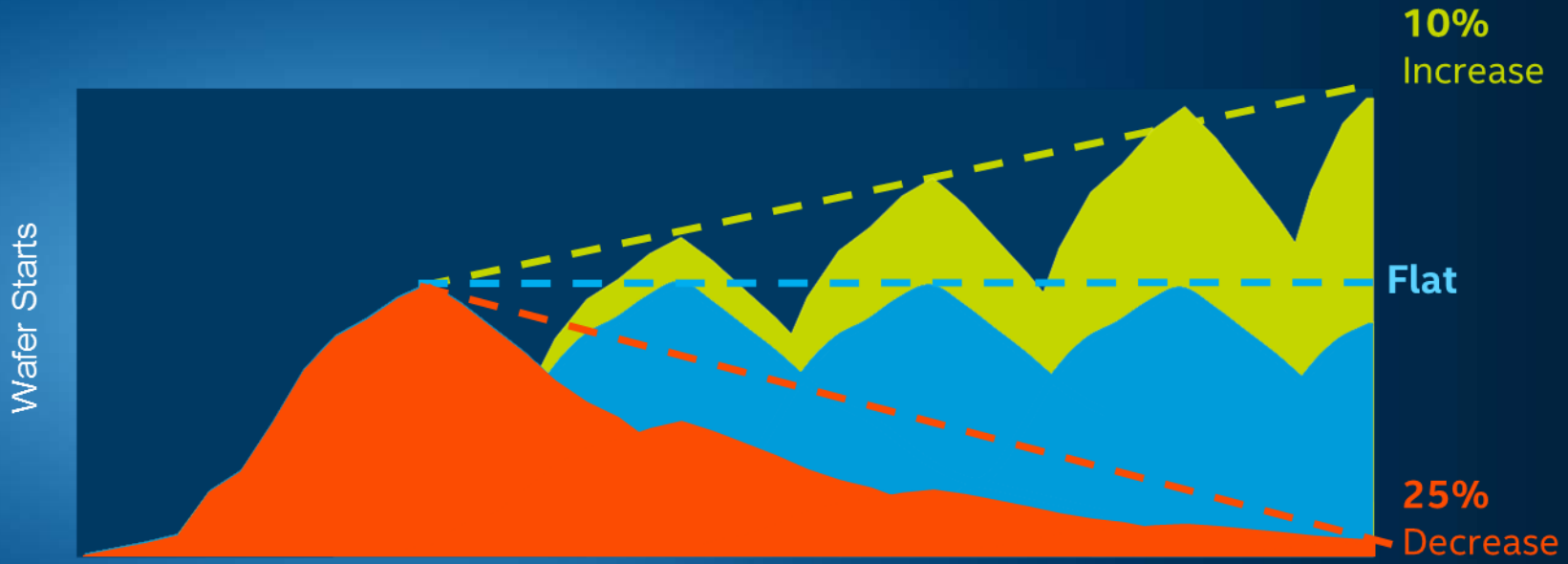
THREE WAYS TO TEST THE MODEL:

Lower unit demand

Higher technology development cost

Reduced cost per transistor improvement

THREE WAYS TO TEST THE MODEL: UNIT DEMAND CHANGES

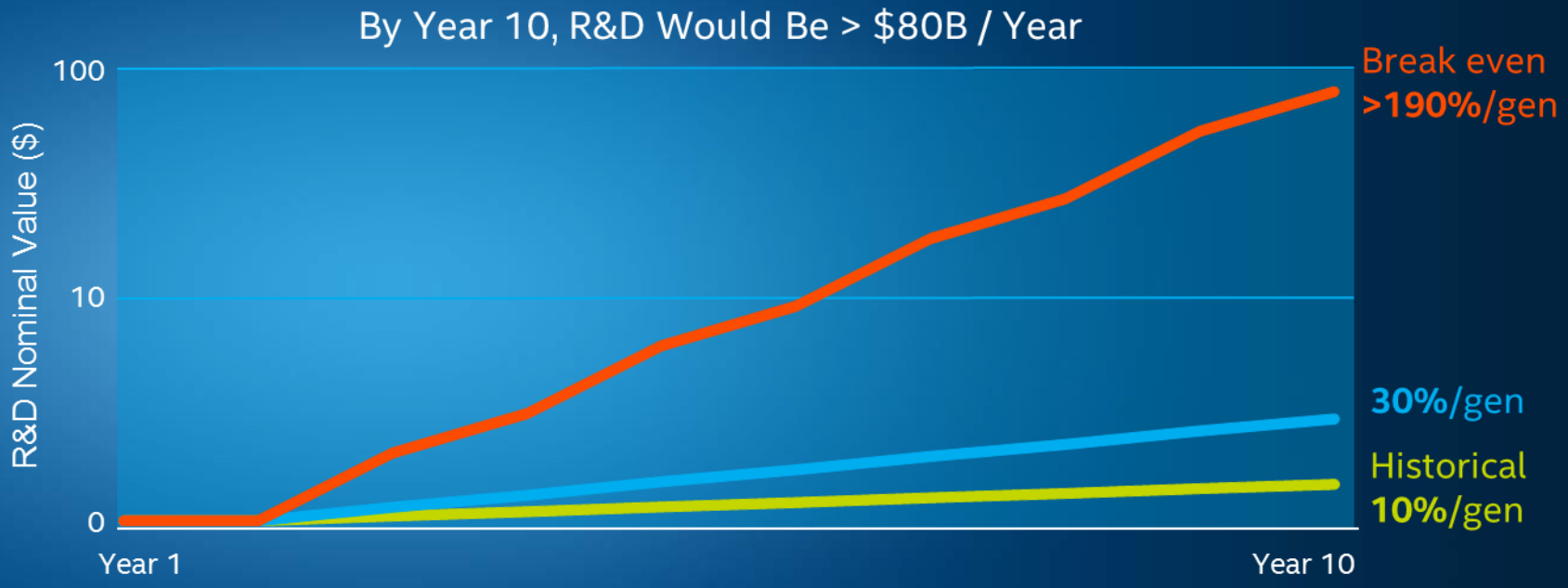


Annual unit demand of -25% over 10 years required to offset economic scaling benefits

Assumptions are theoretical and not forecasts

Source: Intel

THREE WAYS TO TEST THE MODEL: R&D COST INCREASES

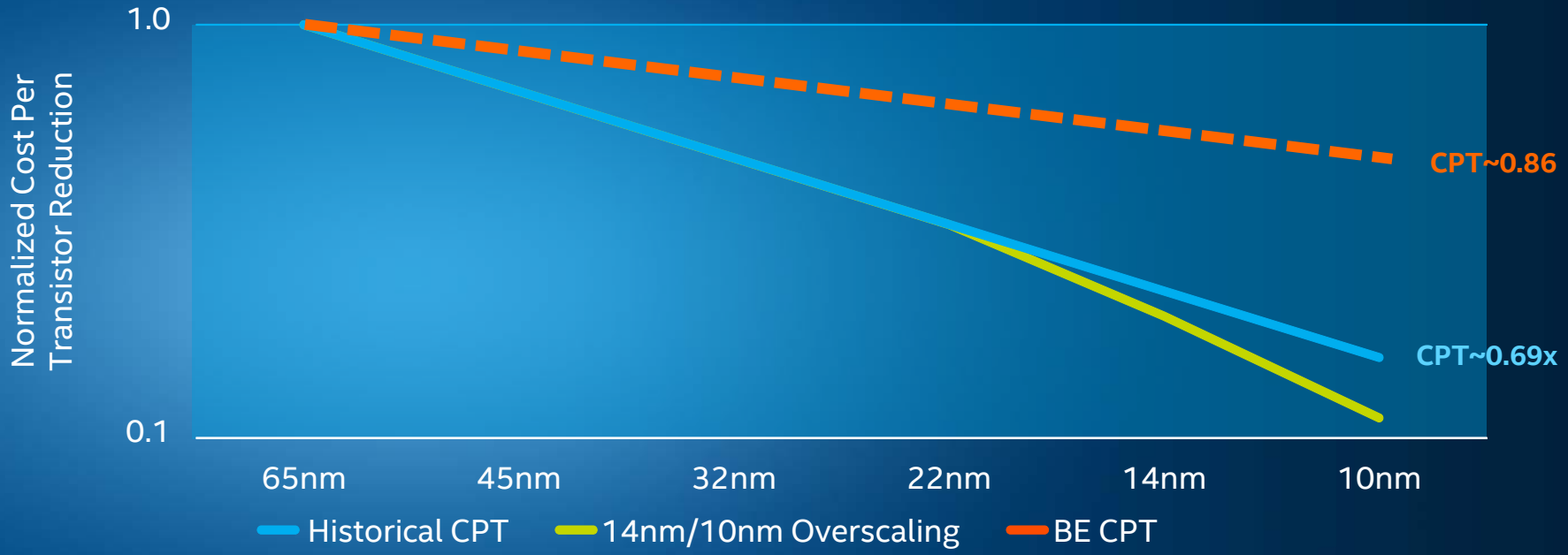


Higher R&D investment growth will NOT limit Moore's Law

Assumptions are theoretical and not forecasts.

Source: Intel

THREE WAYS TO TEST THE MODEL: CPT IMPROVEMENT REDUCES



Poorer CPT scaling could challenge economic benefits

Assumptions are theoretical and not forecasts

Source: Intel

AGENDA

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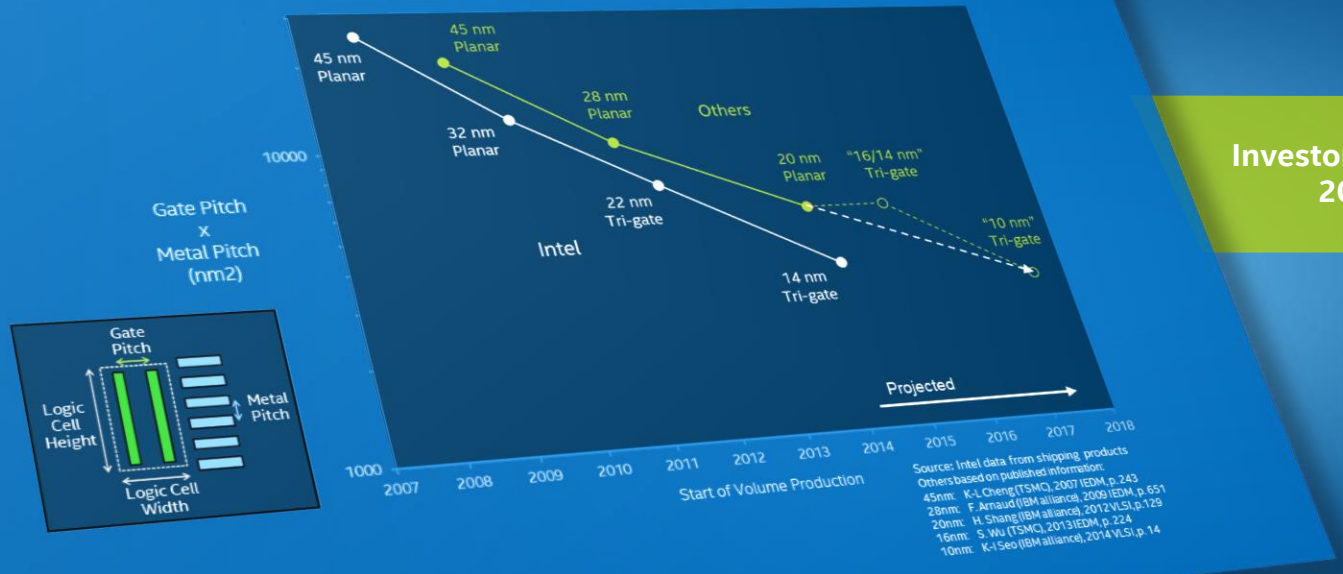
LOGIC AREA SCALING TREND

(Publicly available scaling information)



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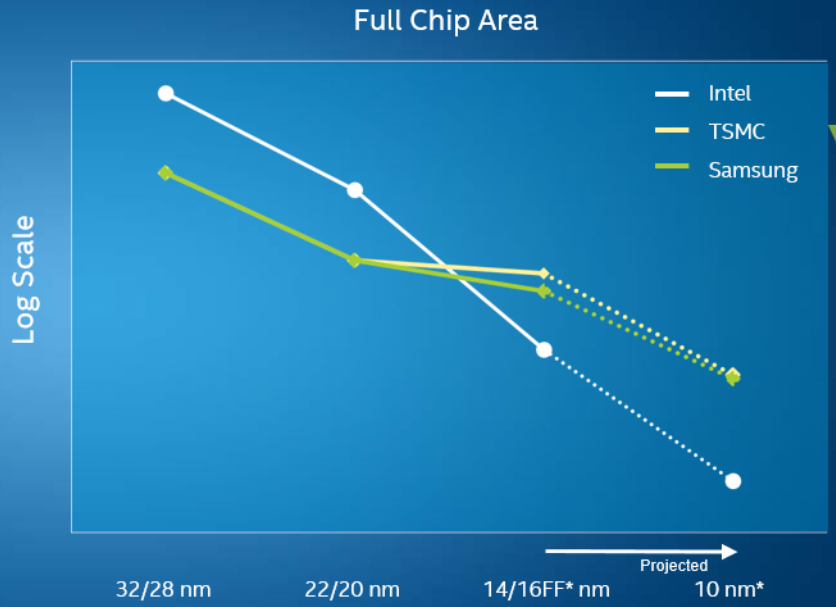
ESTIMATED FULL CHIP SCALING

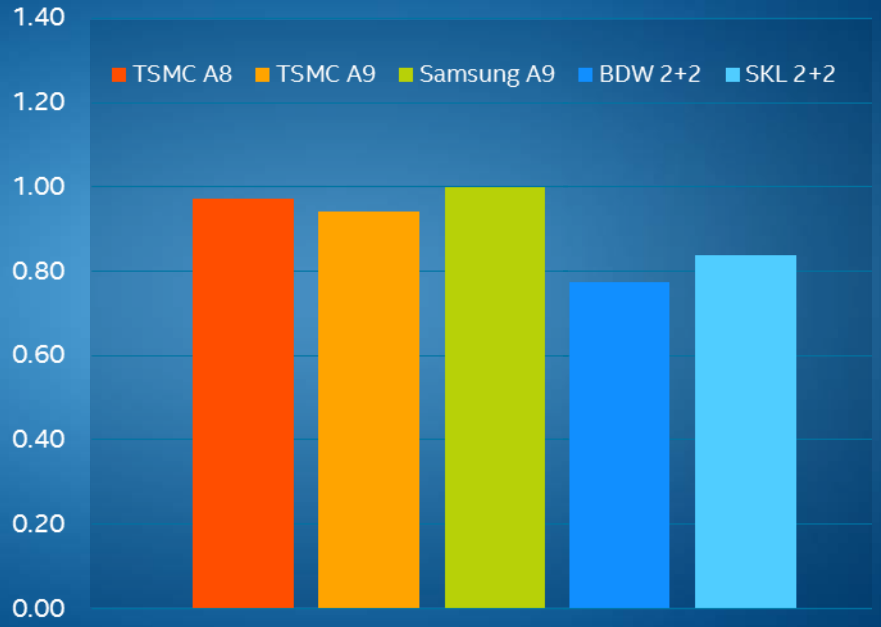


Updated from Investor Meeting 2013

Area scaling estimate includes more of the technology features

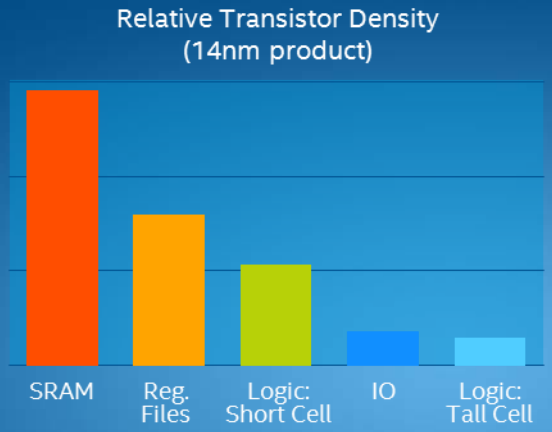
Sources: TSMC keynote, ARM Tech Con 2012, Oct. 30, 2012, 2014 TSMC Technology Symposium, April 22, 2014, *Samsung, Globalfoundries Prep 14nm Process*, EE Times 4/17/2014, 2014. 2014 VLSI Technology Symposium abstract - *A 10nm Platform Technology for Low Power and High Performance Application Featuring FINFET Devices with Multi Workfunction Gate Stack on Bulk and SOI*, Samsung, Global Foundries, et. al. Intel: P1274/P1275 Definition Wrap-up, TMG Technology Density working group, * Projected

TRANSISTOR DENSITY FROM ACTUAL PRODUCTS

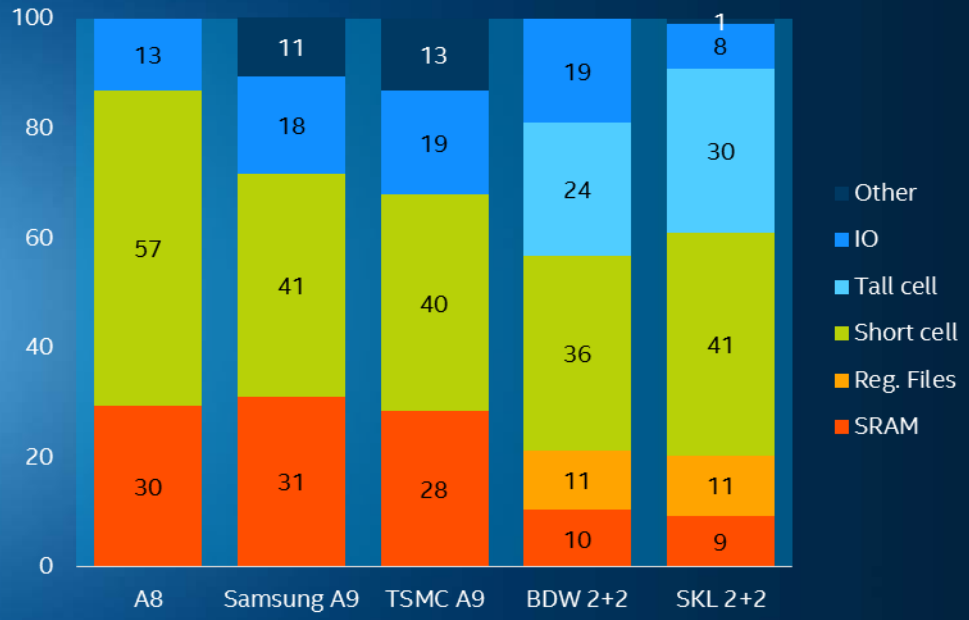


Source: Intel Internal analysis

COMPOSITION MATTERS



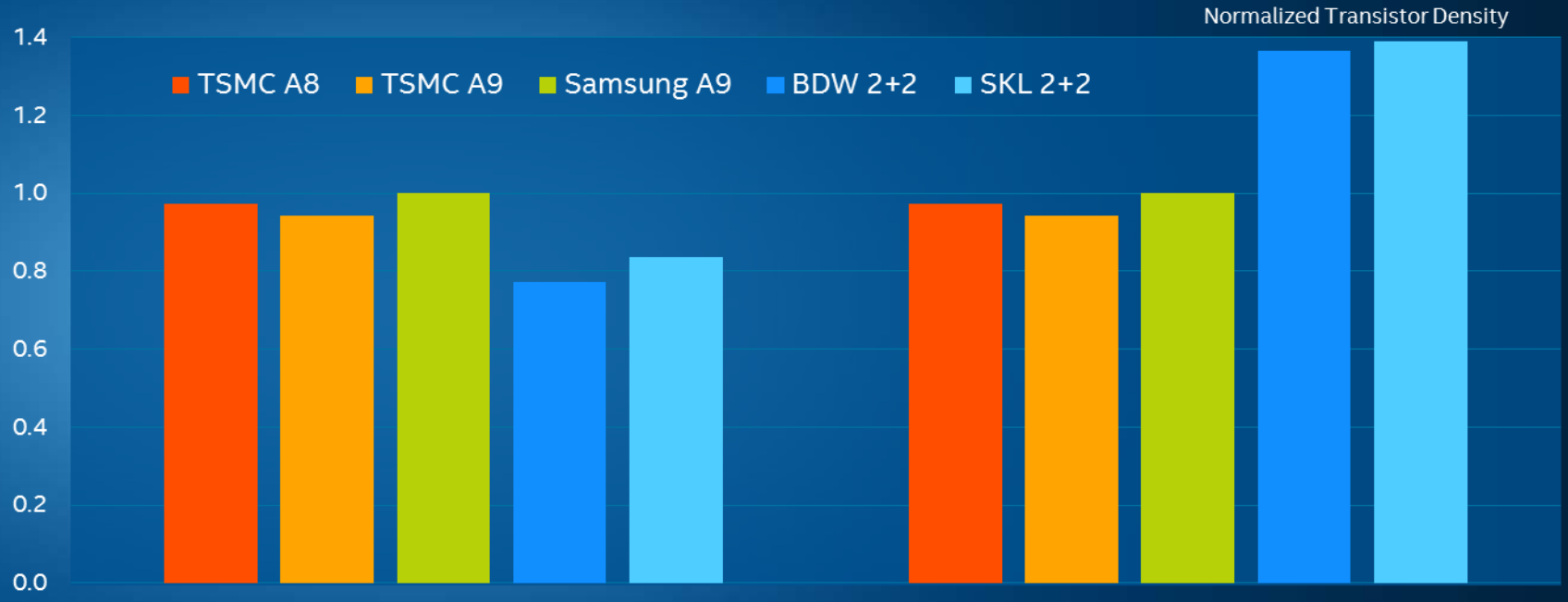
SRAM density = ~ 3X+ of logic
Logic cell choice = ~ 3X



A8/A9 has more inherently dense elements.
Intel has more sparse, higher speed elements.

Source: Intel Internal analysis

TRANSISTOR DENSITY NORMALIZED FOR COMPOSITION

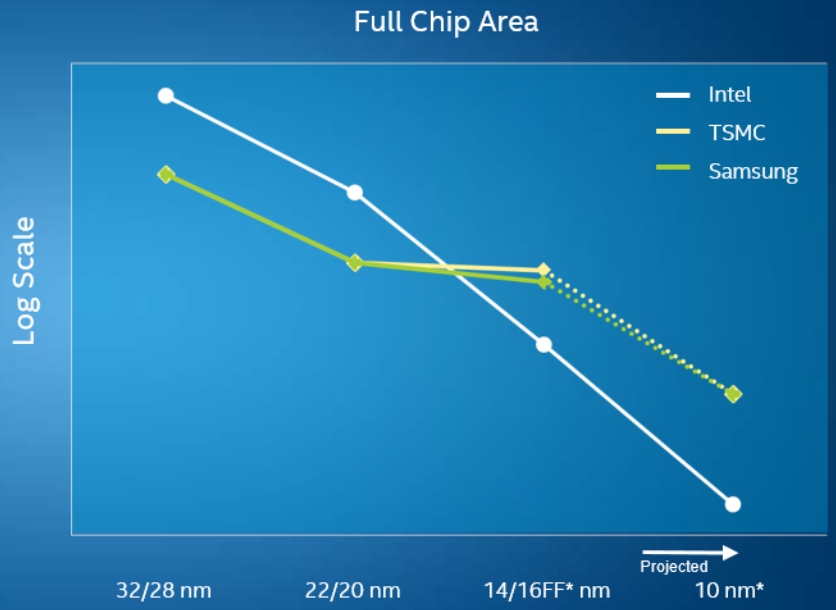


Product data demonstrates Intel 14nm advantage

Source: Intel Internal analysis

Source: Intel internal analysis

FULL CHIP SCALING UPDATED WITH ACTUAL 14/16NM PRODUCTS



Intel 14nm provides significant density advantage

Sources: TSMC keynote, ARM Tech Con 2012, Oct. 30, 2012, 2014 TSMC Technology Symposium, April 22, 2014, *Samsung, Globalfoundries Prep 14nm Process*, EE Times 4/17/2014, 2014. 2014 VLSI Technology Symposium abstract - *A 10nm Platform Technology for Low Power and High Performance Application Featuring FINFET Devices with Multi Workfunction Gate Stack on Bulk and SOI*, Samsung, Global Foundries, et. al. Intel: P1274/P1275 Definition Wrap-up, TMG Technology Density working group, * Projected

FUTURE OPTIONS BEING INVESTIGATED

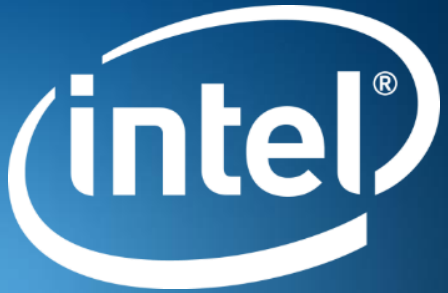
Source: Intel

SUMMARY

- 14nm yields, availability and product portfolio M**ATURING**
- Cost per Transistor is difficult, but progress is **PROMISING**
- Economics of Moore's Law for Intel are **SOLID**
- Our view of competition is **UNCHANGED**
- Innovation and change will be required looking forward

but….

- The research pipeline is challenging but **FULL**



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