Preliminary Information

AMD Athlon™

Processor Module Data Sheet

Publication # **21016** Rev: **M**
Issue Date: **June 2000**

AMD

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Revision History

Date	Rev	Description
June 2000	M	Added information about the AMD Athlon™ processor Model 4 to the following chapters: ■ "About This Data Sheet" on page 1. ■ Chapter 1, "Overview" on page 3. ■ Chapter 6, "Electrical Data" on page 23. ■ Chapter 8, "Ordering Information" on page 53. Revised SADDIN and SADDOUT information in Chapter 3, "Logic Symbol Diagram" on page 11. Added "Signal and Power-Up Requirements" on page 37. Revised Chapter 5, "Thermal Design" on page 21.
May 2000	L	Non-public version
March 2000	K	Added information about the 950-MHz AMD Athlon processor in the following tables: ■ Table 10, "VCC_CORE Power and Current for Model 1, Model 2, and Model 4," on page 30 ■ Table 21, "Valid Ordering Part Number Combinations for Model 2," on page 55 Revised information about the 900-MHz and 1-GHz (1000 MHz) AMD Athlon processor in Table 21, "Valid Ordering Part Number Combinations for Model 2," on page 55.

February 2000	J	Added information about the 900-MHz and 1-GHz (1000 MHz) AMD Athlon processor in the following chapters:
		■ In Chapter 1, "Overview" on page 3.
		■ In Chapter 6, "Electrical Data" on page 23 in the following tables:
		  ■ Table 8, "Operating Ranges," on page 28
		  ■ Table 10, "VCC_CORE Power and Current for Model 1, Model 2, and Model 4," on page 30
		  ■ Table 11, "DC Characteristics," on page 32
		■ Chapter 8, "Ordering Information" on page 53.

February 2000	I	Added information about the 850-MHz AMD Athlon processor in the following chapters:
		■ In Chapter 1, "Overview" on page 3.
		■ In Chapter 6, "Electrical Data" on page 23 in the following tables:
		  ■ Table 8, "Operating Ranges," on page 28
		  ■ Table 10, "Typical and Maximum Power Dissipation for Model 2—Part One," on page 31
		  ■ Table 11, "DC Characteristics," on page 32
		■ Chapter 8, "Ordering Information" on page 53.
		Reorganized entire book by merging Part One and Part Two together to integrate Model 2 and Model 1 information.
		Revised *Power Supply Current* Maximum values for 550-MHz through 800-MHz Model 2 processors in Table 11, "DC Characteristics," on page 32.
		Revised *Power Supply Current* Maximum values Model 1processors in Table 14, "DC Characteristics for Model 1," on page 34.

Date	Rev	Description
January 2000	H	Added information about the 800-MHz AMD Athlon processor in the following chapters: ■ In Chapter 14, "Electrical Data" on page 65 in the following tables: ■ Table 23, "Operating Ranges," on page 68 ■ Table 25, "Typical and Maximum Power Dissipation (Model 2)," on page 69 ■ Table 26, "DC Characteristics (Model 2)," on page 70 ■ In Chapter 16, "Ordering Information" on page 81. Changed the value of pullup resistors from 68-ohms to 47-ohms in the "Termination" section starting on page 24, Table 7, "Signal and Clock Layout and Termination Requirements," on page 24, and Figure 8, "Test Circuit" on page 31. Revised the maximum thermal power values for all Model 2 processors in Table 25, "Typical and Maximum Power Dissipation (Model 2)," on page 69.
December 1999	G	Divided book into Part One and Part Two. Part One provides information about the AMD Athlon™ processor family (Model 1 and Model 2), and Part Two provides information specific to the AMD Athlon processor Model 2 (0.18-micron process technology). **Revisions to Part One:** In Chapter 6, "Electrical Data" on page 21: ■ Expanded information in the "Termination" section starting on page 24, including the addition of Table 7, "Signal and Clock Layout and Termination Requirements". ■ Revised maximum rating in Table 9, "Absolute Ratings," on page 26. ■ Revised Stop Grant values in Table 10, "Typical and Maximum Power Dissipation (Model 1)," on page 27. ■ Added I_{CC} values and notes 7 and 8 to Table 11, "DC Characteristics (Model 1)," on page 28. In Chapter 7, "Mechanical Data" on page 33, added # to SCHECK[2]# and SCHECK[7]# in signal Tables 15, 16, and 17 starting on page 39.
October 1999	F	Added the 700 MHz AMD Athlon™ processor to Table 10, "Typical and Maximum Power Dissipation (Model 1)," on page 27 and Table 18, "Valid Ordering Part Number Combinations," on page 47. Revised Table 11, "DC Characteristics (Model 1)," on page 28 and Table 12, "AC Characteristics," on page 30.
August 1999	E	Revised VCC_CORE minimum value from 1.4V to 1.5V in Table 8, "Operating Ranges," on page 26. Revised information in Table 9, "Absolute Ratings," on page 26. Revised information in Table 10, "Typical and Maximum Power Dissipation (Model 1)," on page 27.
August 1999	D	Initial public release

About This Data Sheet

This AMD Athlon™ processor data sheet describes the technical specifications of the AMD Athlon processor family designed for the Slot A mechanical connector. The processor module may include either the AMD Athlon processor Model 1, Model 2, or Model 4. For more information about determining the Model number and features of an AMD Athlon processor module, see the *AMD Processor Recognition Application Note*, order# 20734 and the *AMD Athlon Processor Revision Guide,* order# 22557.

For information about the PGA versions of the AMD Athlon processor, see the *AMD Athlon™ Processor PGA Data Sheet*, order#23792.

1 Overview

The AMD Athlon™ processor powers the next generation in computing platforms, delivering the ultimate performance for cutting-edge applications and an unprecedented computing experience.

The AMD Athlon™ processor family continues to deliver leading-edge processor performance for high-performance desktop systems, workstations, and servers. The newest member of the AMD Athlon processor family integrates a high-performance, full-speed 256-Kbyte Level-Two (L2) cache. Achieving frequencies of 1-GHz (1000 MHz), the AMD Athlon processor is the world's most powerful x86 processor, delivering the highest integer, floating-point and 3D multimedia performance for applications running on x86 system platforms. All AMD Athlon processors provide industry-leading processing power for cutting-edge software applications, including digital content creation, digital photo editing, digital video, image compression, video encoding for streaming over the internet, soft DVD, commercial 3D modeling, workstation-class computer-aided design (CAD), commercial desktop publishing, and speech recognition. It also offers the scalability and 'peace-of-mind' reliability that IT managers and business users require for enterprise computing.

The AMD Athlon processor family features the industry's first seventh-generation x86 microarchitecture, which is designed to support the growing processor and system bandwidth requirements of emerging software, graphics, I/O, and memory technologies. The AMD Athlon processor's nine-issue superpipelined microarchitecture includes multiple full x86 instruction decoders, a high-performance cache architecture, three independent integer units, three address calculation units, and the x86 industry's first superscalar, fully pipelined, out-of-order, three-way floating-point unit. The floating-point unit is capable of delivering 4 gigaflops (Gflops) of single-precision and more than 2 Gflops of double-precision floating-point results at 1 GHz, for superior performance on numerically complex applications.

Only the AMD Athlon processor microarchitecture incorporates Enhanced 3DNow!™ technology and the industry's first 200-MHz, 1.6-Gigabyte per second front-side bus (FSB)—the fastest system bus for x86 platforms.

AMD's Enhanced 3DNow! technology includes additional instructions to the popular 3DNow! instruction set. It consists of new integer multimedia instructions and software-directed data movement instructions for optimizing such applications as digital content creation and streaming video for the internet, as well as new instructions for digital signal processing (DSP)/communications applications.

Based on the high-performance Alpha™ EV6 interface protocol licensed from Digital Equipment Corporation, the AMD Athlon system bus combines the latest technological advances, such as point-to-point topology, source-synchronous packet-based transfers, and low-voltage signaling, to provide the most powerful, scalable bus available for any x86 processor.

The AMD Athlon processor is binary-compatible with existing x86 software and backwards compatible with applications optimized for MMX™ and 3DNow! instructions. Using a data format and single-instruction multiple-data (SIMD) operations based on the MMX instruction model, the AMD Athlon processor can produce as many as four, 32-bit, single-precision floating-point results per clock cycle, potentially resulting in 4 Gflops at 1 GHz (fully scalable).

The AMD Athlon processors are implemented in AMD's advanced 0.18-micron process technology to achieve maximum performance and scalability.

For information about the PGA versions of the AMD Athlon processor, see the *AMD Athlon™ Processor PGA Data Sheet*, order#23792.

1.1 AMD Athlon™ Processor Microarchitecture Summary

The following features summarize the AMD Athlon processor microarchitecture:

- Nine-issue, superpipelined, superscalar x86 processor microarchitecture designed to achieve high clock frequencies
- Multiple full x86 instruction decoders
- Three out-of-order, superscalar, fully pipelined floating-point execution units, which execute all x87 (floating-point), MMX, 3DNow!, and Enhanced 3DNow! instructions
- Three out-of-order, superscalar, pipelined integer units and and three address calculation units
- 72-entry instruction control unit
- Advanced dynamic branch prediction
- Enhanced 3DNow! technology
- A 200-MHz AMD Athlon system bus (scalable beyond 400 MHz) enabling leading-edge system bandwidth for data movement-intensive applications
- High-performance cache architecture including a split 128-Kbyte L1 cache, an integrated 256-Kbyte L2 cache (external 512-Kbyte L2 cache for Model 1 and Model 2), and a large dual-level, split Translation Look-aside Buffer (TLB)

AMD is committed to delivering reliable, high-performance, and cost-effective solutions to its customers for all applications and configurations. The AMD Athlon processor continues to deliver superior system performance for systems from desktops to servers. Figure 1 on page 6 shows a typical AMD Athlon processor system block diagram.

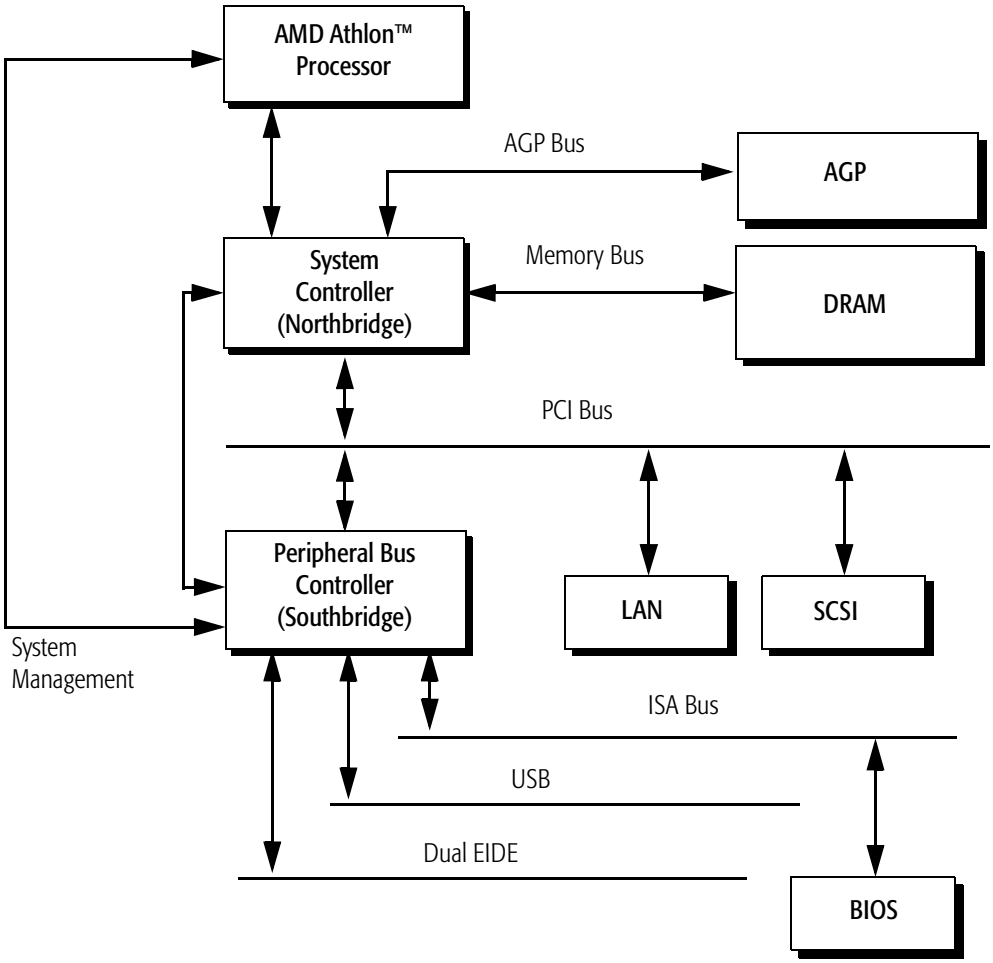


Figure 1. Typical AMD Athlon™ Processor System Block Diagram

2 Interface Signals

2.1 Overview

The AMD Athlon™ system bus architecture is designed to deliver unprecedented data movement bandwidth for next-generation x86 platforms, as well as the high performance required by enterprise-class application software. The system bus architecture consists of three high-speed channels (a unidirectional processor request channel, a unidirectional probe channel, and a 72-bit bidirectional data channel, including 8-bit error code correction [ECC] protection), source-synchronous clocking, and a packet-based protocol. In addition, the system bus supports several control, clock, and legacy signals. The interface signals use a HSTL-like, low-voltage swing signaling technology contained within the Slot A mechanical connector, which is mechanically compatible with the industry-standard SC242 connector.

2.2 Signaling Technology

The AMD Athlon system bus uses a variation of the low-voltage, JEDEC HSTL signaling technology, which has been enhanced to provide larger noise margins, reduced ringing, and variable voltage levels. The signals are open-drained and require termination to a supply that provides the High signal level. The HSTL+ inputs use differential receivers, which require a reference voltage (V_{REF}). The reference signal is used by the receivers to determine if a signal is asserted or deasserted by the source. Termination resistors are placed at both ends of the interface and are used to provide the High signal level and to control reflections on the interface.

2.3 AMD Athlon™ System Bus Signals

Table 2 on page 8 shows the AMD Athlon system bus signals and legacy interface signals. Table 1 shows the pin-type definitions used in the *Type* column of Table 2. Signals with pound signs (#) are active Low.

Table 1. Pin-Type Definitions

Mnemonic	Definition
I	Standard input pin to the processor
O	Standard output pin from the processor
I/O	Bidirectional, three-state input/output pin
OD	Open-drain structure that allows multiple devices to share the pin in a wired-OR configuration
PP	Push/Pull structure driven by a single source

Table 2. AMD Athlon™ System Bus and Legacy Interface Signals

Signal Name	Type	Level	Number of Pins	Description
A20M#	I	OD	1	A20M# is an input from the system used to simulate address wrapping around in the 20-bit 8086.
CLKFWDRST	I	OD	1	CLKFWDRST resets clock-forward circuitry for both the system and processor.
CONNECT	I	OD	1	CONNECT is an input from the system used for power management and clock-forward initialization at reset.
COREFB+ COREFB–	O	PP	2	COREFB+ and COREFB– are outputs to the system that provide AMD Athlon processor core voltage feedback to the system.
FERR	O	OD	1	FERR is an output to the system that is asserted for any unmasked numerical exception independent of the NE bit in CR0.
FID[3:0]	O	OD	4	The FID[3:0] signals are outputs to the system that report the multiplier used on the system clock (SYSCLK) producing the AMD Athlon processor core clock.
IGNNE#	I	OD	1	IGNNE# is an input from the system that tells the processor to ignore numeric errors.
INIT#	I	OD	1	INIT# is an input from the system that resets the integer registers without affecting the floating-point registers or the internal caches. Execution starts at 0FFFF FFF0h.

Note:
* *The industry-standard APIC signals, PICCLK and PICD[1:0]#, are not available on Model 1.*

Table 2. AMD Athlon™ System Bus and Legacy Interface Signals (continued)

Signal Name	Type	Level	Number of Pins	Description
INTR	I	OD	1	INTR is an input from the system that causes the processor to start an interrupt acknowledge transaction that fetches the 8-bit interrupt vector and starts execution at that location.
NMI	I	OD	1	NMI is an input from the system that causes a non-maskable interrupt.
PICCLK*	I	PP	1	PICCLK is an input clock that is required for operation of the APIC bus.
PICD[1:0]#*	I	OD	2	PICD[1:0]# are bidirectional signals that are used by the APIC bus, and must be connected to all APIC data pins on all devices of the APIC bus.
PROCRDY	O	OD	1	PROCRDY is an output to the system and is used for power management and source-synchronous clock initialization at reset.
PWROK	I	OD	1	PWROK is an input from the system indicating that the core power is within specified limits.
RESET#	I	OD	1	RESET# is an input from the system that initializes and resets the processor and invalidates cache blocks.
SADDIN[14:2]#	I	OD	13	SADDIN[14:2]# is the unidirectional system probe and data movement command channel from the system.
SADDINCLK#	I	OD	1	SADDINCLK# is the single-ended source-synchronous clock for SADDIN[14:2]# and is driven by the system.
SADDOUT[14:2]#	O	OD	13	SADDOUT[14:2]# is the unidirectional processor request channel to the system. It is used to transfer processor requests or probe responses to the system.
SADDOUTCLK#	O	OD	1	SADDOUTCLK# is the single-ended source-synchronous clock for SADDOUT[14:2]# driven by the processor.
SCHECK[7:0]#	I/O	OD	8	SCHECK[7:0]# contain the ECC bits for data transfers on SDATA[63:0]#.
SDATA[63:0]#	I/O	OD	64	SDATA[63:0]# is the bidirectional channel between the processor and system for data movement.
SDATAINCLK[3:0]#	I	OD	4	SDATAINCLK[3:0]# is the single-ended forwarded clock driven by the system to transfer data on SDATA[63:0]#. Each 16-bit data word is skewed-aligned with this clock.
SDATAINVAL#	I	OD	1	SDATAINVAL# is driven by the system to pace the data into the processor. SDATAINVAL# can be used to introduce an arbitrary number of cycles between octawords into the processor.

Note:

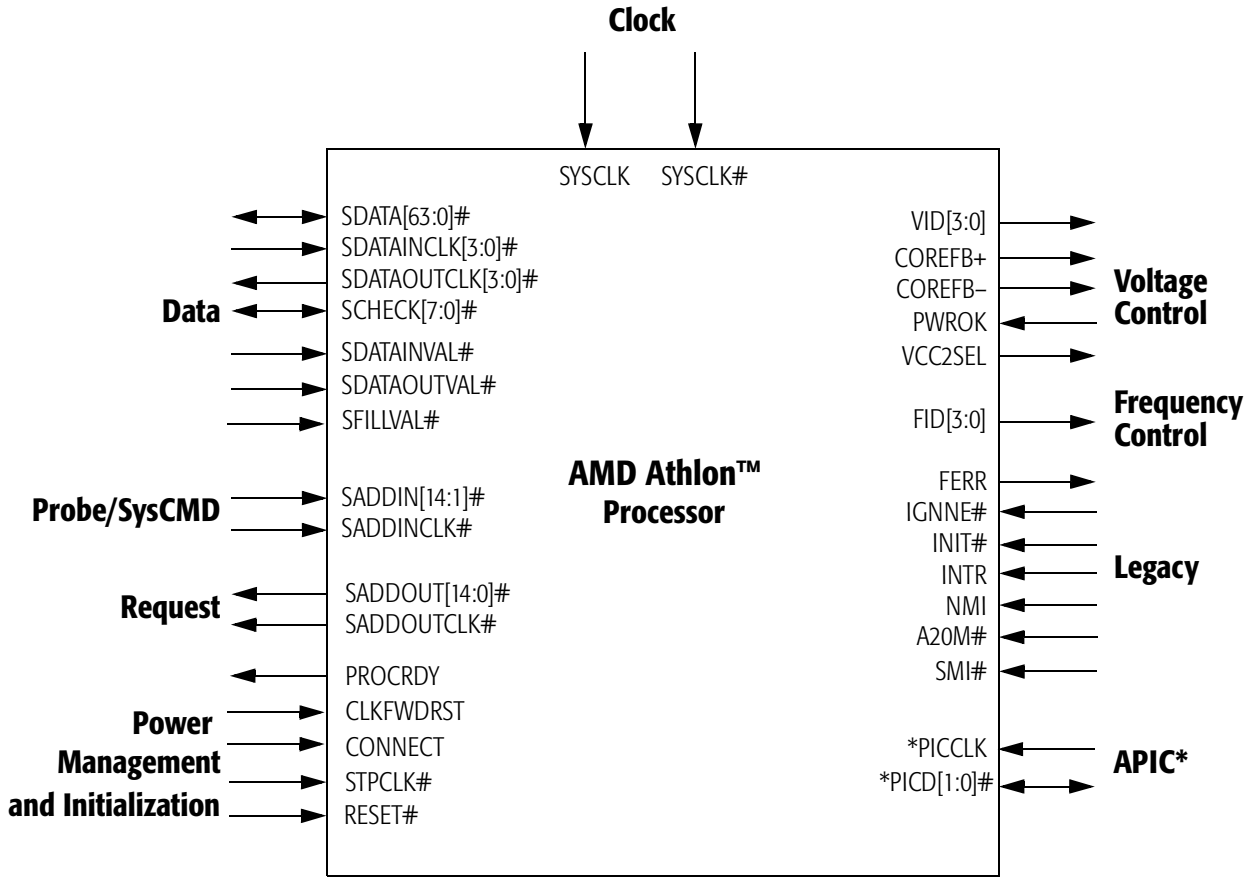
* *The industry-standard APIC signals, PICCLK and PICD[1:0]#, are not available on Model 1.*

Table 2. AMD Athlon™ System Bus and Legacy Interface Signals (continued)

Signal Name	Type	Level	Number of Pins	Description
SDATAOUTCLK[3:0]#	O	OD	4	SDATAOUTCLK[3:0]# is the single-ended source-synchronous clock driven by the processor to transfer data on SDATA[63:0]#. Each 16-bit data word on SDATA[63:0]# is skewed-aligned with this clock.
SDATAOUTVAL#	I	OD	1	SDATAOUTVAL# is driven by the system to pace the data from the processor. SDATAOUTVAL# can be used to introduce an arbitrary number of cycles between quadwords from the processor.
SFILLVAL#	I	OD	1	SFILLVAL# validates a data transfer to the processor. The system may tie this pin to the asserted state (validating all fills). The processor samples SFILLVAL# at the first or second data beat.
SMI#	I	OD	1	SMI# is an input that causes the processor to enter the system management mode.
STPCLK#	I	OD	1	STPCLK# is an input that causes the processor to enter a lower power mode and issue a Stop Grant special cycle.
SYSCLK SYSCLK#	I		2	SYSCLK and SYSCLK# are differential input clock signals provided to the processor's PLL from a system-clock generator.
VCC2SEL	O	OD	1	VCC2SEL is an output to the system that indicates the required core voltage for the L2 SRAM. High=2.5V, Low=3.3V.
VID[3:0]	O	OD	4	The VID[3:0] signals are outputs to the motherboard that indicate the required VCC_CORE voltage for the processor.

Note:
* *The industry-standard APIC signals, PICCLK and PICD[1:0]#, are not available on Model 1.*

3 Logic Symbol Diagram



Note:

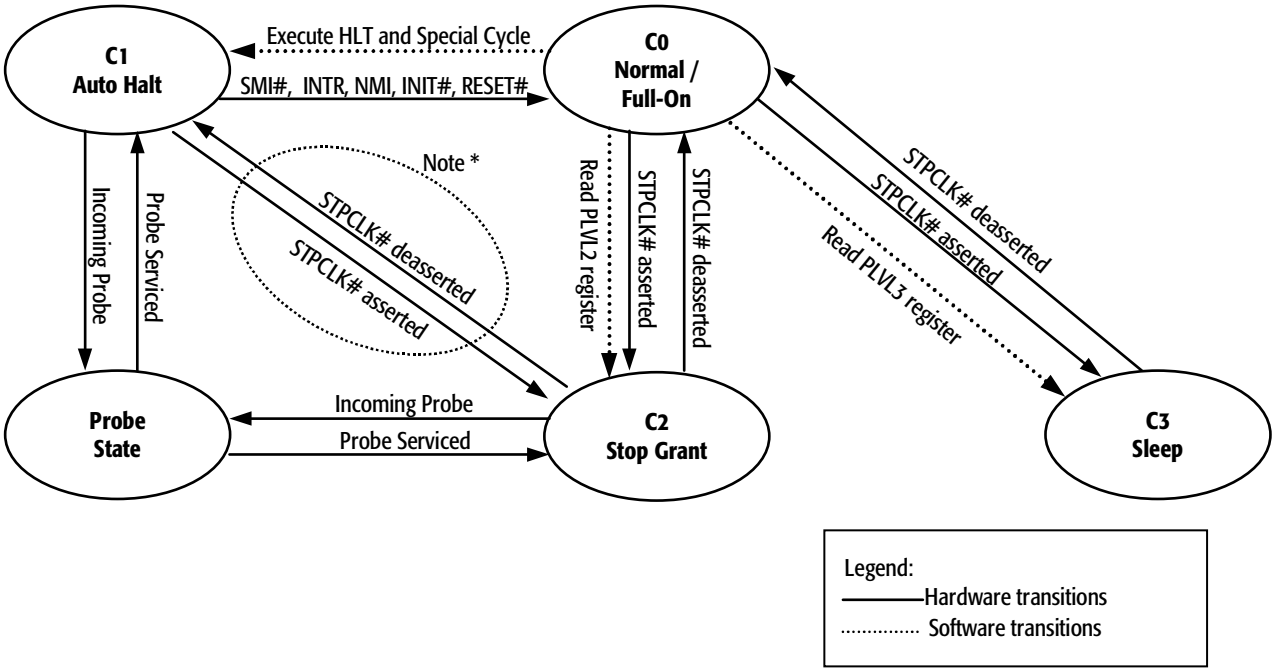
* *The industry-standard APIC signals, PICCLK and PICD[1:0]#, are not available on Model 1.*

Figure 2. Logic Symbol Diagram for AMD Athlon™ Processor

4 Power Management

4.1 Power Management States

The AMD Athlon™ processor uses multiple advanced power states to place the processor in reduced power modes. These power states are used to enhance processor performance, minimize power dissipation, and provide a balance between performance and power (see "Power Dissipation" on page 30 for more information). In addition, these power states conform to the industry-standard Advanced Configuration and Power Interface (ACPI) requirements for processor power states. (ACPI is a specification for system hardware and software to support OS-oriented power management.) Each state has a specific mechanism that allows the processor to enter the respective state. Figure 3 shows the power management states of the AMD Athlon processor. The figure includes the ACPI power states for the processor, labeled as Cx.



Note: *The C1 to C2 transition by way of the STPCLK# assertion/deassertion is not defined for ACPI-compliant systems.*

Figure 3. AMD Athlon™ Processor Power Management States

The following sections describe each of the low-power states.

Note: *In all power management states, the system must not disable the system clock (SYSCLK/SYSCLK#) to the processor.*

Full-On

The Full-on or normal state refers to the default power state and means that all functional units are operating at full processor clock speed.

Halt State

When the AMD Athlon processor executes the HLT instruction, the processor issues a Halt special cycle to the system bus. The phase-lock loop (PLL) continues to run, enabling the processor to monitor bus activity and provide a quick resume from the Halt state. The processor may enter a lower power state.

The Halt state is exited when the processor samples INIT#, INTR (if interrupts are enabled), NMI, RESET#, or SMI#.

Stop Grant and Sleep States

After recognizing the assertion of STPCLK#, the AMD Athlon processor completes all pending and in-progress bus cycles and acknowledges the STPCLK# assertion by issuing a Stop Grant special bus cycle to the system bus. The processor may enter a lower power state.

From a software standpoint, the Sleep/Stop Grant state is entered by reading the PLVL registers located in an ACPI-compliant peripheral bus controller. The difference between the Stop Grant state and the Sleep state is determined by which PLVL register software reads from the peripheral bus controller. If the software reads the PLVL_2 register, the processor enters the Stop Grant state. In this state, probes are allowed, as shown in Figure 3 on page 13. If the software reads the PLVL_3 register, the processor enters the Sleep state, where probes are not allowed. This action is accomplished by disabling snoops within an ACPI-compliant system controller.

The Sleep/Stop Grant state is exited upon the deassertion of STPCLK# or the assertion of RESET#. After the processor enters the Full-on state, it resumes execution at the instruction boundary where STPCLK# was initially recognized.

The processor latches INIT#, INTR (if interrupts are enabled), NMI, and SMI#, if they are asserted during the Stop Grant or Sleep state. However, the processor does not exit this state until the deassertion of STPCLK#. When STPCLK# is deasserted,

any pending interrupts are recognized after returning to the Normal state.

If RESET# is sampled asserted during the Stop Grant or Sleep state, the processor immediately returns to the Full-on state and the reset process begins.

Probe State

The Probe state is entered when the system requires the processor to service a probe. When in the Probe state, the processor responds to a probe cycle in the same manner as when it is in the Full-on state.

When the probe has been serviced, the processor returns to the same state as when it entered the Probe state.

4.2 Connection and Disconnection Protocol

The AMD Athlon processor enhances power savings in each of the power management states when the system logic disconnects the processor from the system bus and slows down the internal clocks. Entering the lowest power state is accomplished with a connection protocol between the processor and system logic. The system can initiate a bus disconnection upon the receipt of a Stop Grant special cycle. If required by the system, the processor disconnects from the system bus and slows down its internal clocks before entering the Stop Grant or Sleep state. If the system requires the processor to service a probe while it is in the Stop Grant state, it must first request that the processor increase its clocks to full speed and reconnect to the system bus. Table 3 on page 16 describes the AMD Athlon processor power states using the connection protocol as described on page 16.

AMD Athlon system bus connections and disconnections are controlled by an enable bit within the system controller.

Table 3. AMD Athlon™ Processor Power Management States

State Name	Entered	Exited
Full-On / Normal	This is the full-on running state of the processor	Initiates either a Halt instruction or STPCLK# assertion.
Halt	Execution of the Halt instruction. A special cycle is issued. The processor may enter a lower power state.	The processor exits and returns to the Run state upon the occurrence of INIT#, INTR, NMI, SMI# or RESET#. The processor transitions to the Stop Grant state if STPCLK# is asserted and returns to the Halt state upon STPCLK# deassertion.
Stop Grant	The processor transitions to the Stop Grant state with the assertion of STPCLK# (as a result of a read to the PLVL_2 register). A Stop Grant special cycle is issued. The processor may enter a lower power state. ***Note:*** While in this state, interrupts are latched and serviced when the processor transitions to the Full-on state.	The processor transitions to the Full-on or Halt state upon STPCLK# deassertion. RESET# asserted initializes the processor but, if STPCLK# is asserted, the processor returns to the Stop Grant state.
Probe	A transition to the Probe state occurs when the system asserts CONNECT. The processor remains in this state until the probe is serviced and any data is transferred.	The processor returns to the Halt or Stop Grant state when the probe has been serviced and the system deasserts CONNECT. If the processor was disconnected from the bus in the previous state, bus disconnection occurs and the internal frequency of the processor is again slowed down.
Sleep	The processor can enter its lowest power state, Sleep, from the Full-on state with the assertion of STPCLK# (as a result of a read to the PLVL_3 register). ***Note:*** While in this state, interrupts are latched and serviced when the processor transitions to the Full-on state.	The processor transitions to the Run state upon STPCLK# deassertion. Asserting RESET# initializes the processor but, if STPCLK# is asserted, the processor returns to the Sleep state.

Connection Protocol

In addition to the legacy STPCLK# signal and the Halt and Stop Grant special cycles, the AMD Athlon system bus connection protocol includes the CONNECT, PROCRDY, and CLKFWDRST signals and a *Connect* special cycle.

AMD Athlon system bus disconnects are initiated by the system controller in response to the receipt of a Stop Grant special cycle. Reconnections are initiated by the processor in response to an interrupt or STPCLK# deassertion, or by the system to service a probe.

A disconnect request is implicit, if enabled, in the processor Stop Grant special cycle request. It is expected that the system controller provides a BIOS-programmable register in which it

can disconnect the processor from the AMD Athlon system bus upon the occurrence of a Stop Grant special cycle. The system receives the special cycle request from the processor and, if there are no outstanding probes or data movements, the system deasserts CONNECT to the processor. The processor detects the deassertion of CONNECT on a rising edge of SYSCLK, and deasserts PROCRDY to the system. In return, the system asserts CLKFWDRST in anticipation of reestablishing a connection at some later point.

Note: *The system must disconnect the processor from the AMD Athlon system bus before issuing the Stop Grant special cycle to the PCI bus.*

The processor can receive an interrupt or STPCLK# deassertion after it sends a Stop Grant special cycle to the system but before the disconnection actually occurs. In this case, the processor sends the Connect special cycle to the system, rather than continuing with the disconnect sequence. The system cancels the disconnection. Figure 4 shows the sequence of events from a system perspective, which leads to disconnecting the processor from the AMD Athlon system bus and placing the processor in the Stop Grant state.

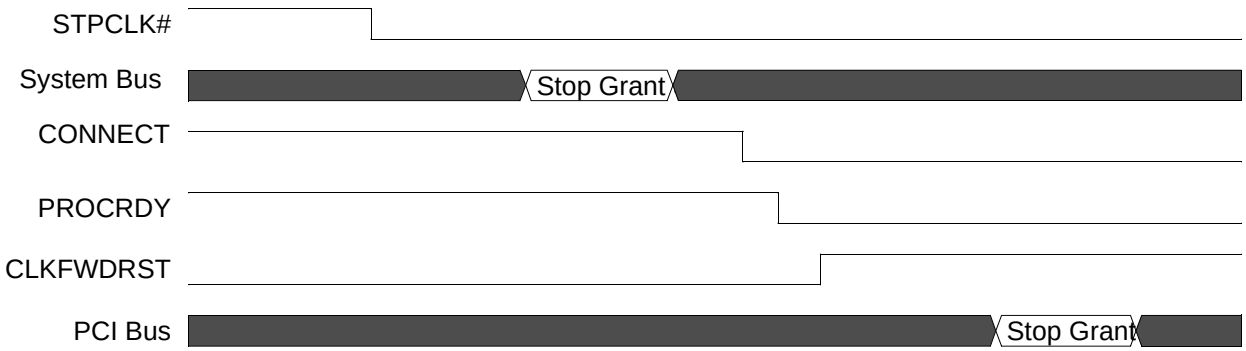


Figure 4. Example System Bus Disconnection Sequence

The following sequence of events describes how the processor is placed in the Stop Grant state when bus disconnection is enabled within the system controller:

1. The peripheral controller asserts STPCLK# to place the processor in the Stop Grant state.
2. When the processor receives STPCLK#, it acknowledges the system by sending out a Stop Grant special bus cycle on the AMD Athlon system bus.

3. When the special cycle is received by the system controller, the system controller deasserts CONNECT, initiating a bus disconnect to the processor.
4. The processor replies to the system controller by deasserting PROCRDY, approving the bus disconnect request.
5. The system controller asserts CLKFWDRST to complete the bus disconnection sequence.
6. After the processor is disconnected from the bus, the system controller passes the Stop Grant special cycle along to the peripheral controller via the PCI bus, notifying it that the processor is in the Stop Grant state.

Figure 5 shows the signal sequence of events that take the processor out of the Stop Grant state, reconnect the processor to the AMD Athlon system bus, and put the processor into the Full-on state.

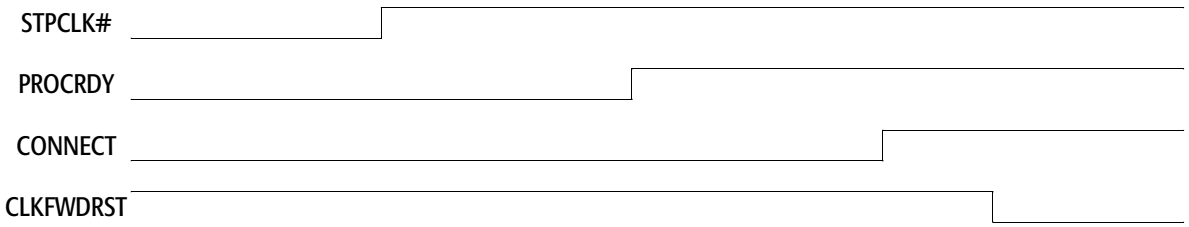


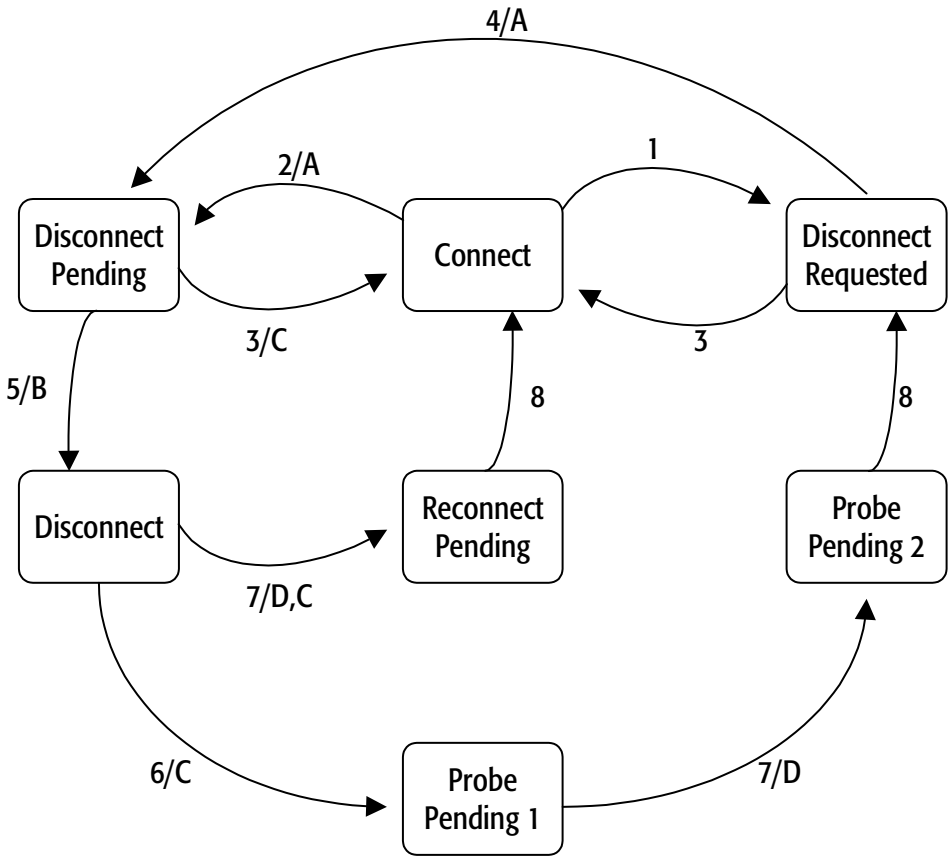
Figure 5. Exiting Stop Grant State/Bus Reconnection Sequence

The following sequence of events removes the processor from the Stop Grant state and reconnects it to the AMD Athlon system bus:

1. The peripheral controller deasserts STPCLK#, informing the processor of a wake event.
2. When the processor receives STPCLK#, it asserts PROCRDY, notifying the system controller to reconnect to the bus.
3. The system controller asserts CONNECT, telling the processor that it is connected to the AMD Athlon system bus.
4. The system controller finally deasserts CLKFWDRST, which synchronizes the forwarded clocks between the processor and the system controller.

Connection State Machines

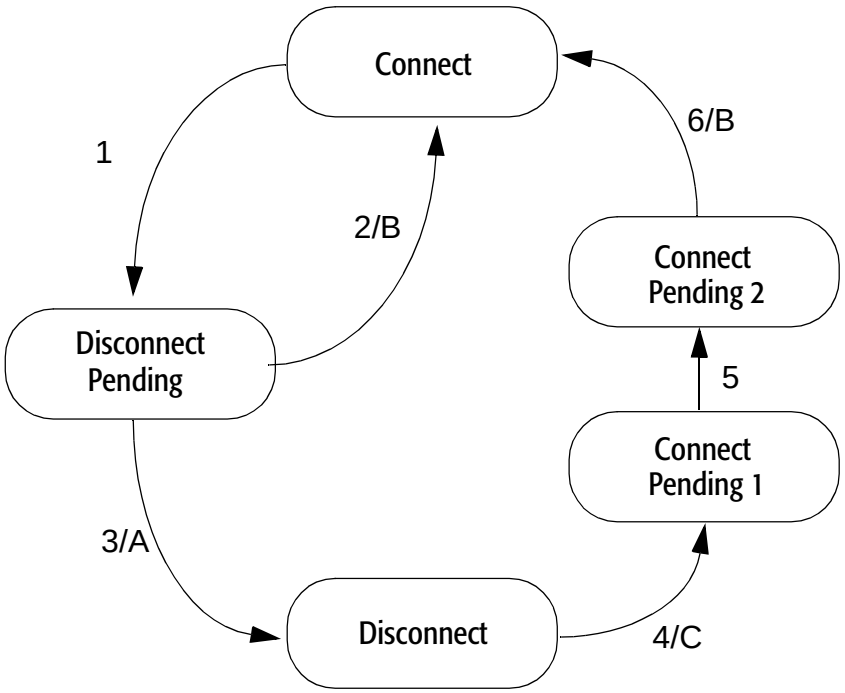
Figure 6 and Figure 7 on page 20 describe the system and processor connection state machines, respectively.



	Condition
1	A disconnect is requested and probes are still pending
2	A disconnect is requested and no probes are pending
3	A CONNECT special cycle from the processor
4	No probes are pending
5	PROCRDY is deasserted
6	A probe needs service
7	PROCRDY is asserted
8	3 SYSCLK periods after CLKFWDRST is deasserted. *Although reconnected to the system interface, the system must not issue any non-NOP SysDC commands for a minimum of four SYSCLK periods after deasserting CLKFWDRST.*

	Action
A	Deassert CONNECT 8 SYSCLK periods after last probe/command sent
B	Assert CLKFWDRST
C	Assert CONNECT
D	Deassert CLKFWDRST

Figure 6. System Connection States



	Condition
1	CONNECT is deasserted by the system (for a previously sent Halt or Stop Grant special cycle).
2	Processor receives a wake-up event and must cancel the disconnect request.
3	Deassert PROCRDY and slow down internal clocks.
4	Processor wake-up event or CONNECT asserted by system.
5	CLKFWDRST is deasserted by the system
6	Forward clocks start 3 SYSCLK periods after CLKFWDRST is deasserted.

	Action
A	CLKFWDRST is asserted by the system.
B	Issue a CONNECT special cycle.
C	Assert PROCRDY and return internal clocks to full speed

Figure 7. Processor Connection States

5 Thermal Design

For information about thermal design for the AMD Athlon™ processor module, including layout and airflow considerations, see the *AMD Thermal, Mechanical, and Chassis Cooling Design Guide*, order# 23794 and the cooling guidelines on www.amd.com.

6 Electrical Data

6.1 The AMD Athlon™ System Bus

The AMD Athlon™ system bus architecture is designed to deliver unprecedented data movement bandwidth for next-generation x86 platforms, as well as the high performance required by enterprise-class application software. The system bus architecture consists of three high-speed channels (a unidirectional processor request channel, a unidirectional snoop channel, and a 72-bit bidirectional data channel, including 8-bit error code correction [ECC] protection), source-synchronous clocking, and a packet-based protocol. In addition, the system bus supports several control, clock, and legacy signals. The interface signals use a HSTL-like, low-voltage swing signaling technology contained within the Slot A mechanical connector, which is mechanically compatible with the industry-standard SC242 connector. For more information on the AMD Athlon system bus, see the *AMD Athlon™ System Bus Specification*, order# 21902.

6.2 Signal Groupings

The AMD Athlon system bus is the processor connection to a memory and I/O controller or a shared multiprocessor controller. The system interface can be categorized into four signal groups plus power and ground connections. These groups are listed in Table 4 on page 24. The first group connects the AMD Athlon processor to the system controller and uses a source-synchronous, or clock-forwarded clocking scheme. Using this technique, the clocks and data travel in the same direction down the transmission line and arrive together. The second group connects the AMD Athlon processor to the peripheral bus controller, but unlike the system controller group, these signals do not use a source-synchronous scheme. The third group is the control group, which contains signals that interface with the power supply of the system. The fourth group contains the system clock. This is the input clock for the AMD Athlon processor and is the source for all other clocks generated by the AMD Athlon processor module.

Table 4. AMD Athlon™ Processor Interface Signal Groupings

Name	Buffer Type	Signals
System Controller (Northbridge)	Open-Drain	SADDIN[14:2]#, SADDOUT[14:2]#, SADDINCLK#, SADDOUTCLK#, SFILLVAL#, SDATAINVAL#, SDATAOUTVAL#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAOUTCLK[3:0]#, SCHECK[7:0]#, FID[3:0], CLKFWDRST, PROCRDY, CONNECT
Peripheral Bus Controller (Southbridge)		RESET#, INTR, NMI, SMI#, INIT#, A20M#, FERR, IGNNE#, STPCLK#, PICD[1:0]#*, PICCLK*
Control		VID[3:0], VCC2SEL, COREFB+, COREFB–, PWROK
Clock		SYSCLK, SYSCLK#
Power		VCC_CORE, VCC_SRAM, GND

Note:
* *The industry-standard APIC signals, PICCLK and PICD[1:0]#, are not available on Model 1.*

Clock Forwarding

The signals in the system controller group can be divided into six source-synchronous groups, as shown in Table 5. Groups that contain two clocks are bidirectional, source-synchronous groups. These groups use a different clock, based on the operation being performed. For example, when data is sent from the AMD Athlon processor to the system controller, SDATAOUTCLK# is used, and when data is sent from the system controller to the AMD Athlon processor, SDATAINCLK# is used. The topology is point-to-point and active terminations.

Table 5. Source-Synchronous Clock Signal Groups

Group	Signals in Group	Clock
SData0	SDATA[15:0]#, SCHECK[0:1]#	SDATAINCLK[0]#, SDATAOUTCLK[0]#
SData1	SDATA[31:16]#, SCHECK[2:3]#	SDATAINCLK[1]#, SDATAOUTCLK[1]#
SData2	SDATA[47:32]#, SCHECK[4:5]#	SDATAINCLK[2]#, SDATAOUTCLK[2]#
SData3	SDATA[63:48]#, SCHECK[6:7]#	SDATAINCLK[3]#, SDATAOUTCLK[3]#
SAddIn	SADDIN[14:2]#, SFILLVAL#, SDATAINVAL#, SDATAOUTVAL#	SADDINCLK#
SAddOut	SADDOUT[14:2]#	SADDOUTCLK#

6.3 Voltage Identification

The AMD Athlon processor provides four voltage ID lines back to the system for proper configuration of the processor core voltage. The processor either connects a VID to VSS, or has an open value. If required by the voltage regulator, the motherboard pulls up these four signals up to TTL levels. The motherboard is required to pull VID[4] Low for the voltage regulator to supply voltage in the appropriate range for the AMD Athlon processor. These voltage ID values are defined in Table 6. The pullup resistors used on the motherboard must have a value of at least 10 kΩ.

Table 6. Voltage ID Values

VID[3]	VID[2]	VID[1]	VID[0]	VCC_CORE (V)
0	0	0	0	2.05
0	0	0	1	2.00
0	0	1	0	1.95
0	0	1	1	1.90
0	1	0	0	1.85
0	1	0	1	1.80
0	1	1	0	1.75
0	1	1	1	1.70
1	0	0	0	1.65
1	0	0	1	1.60
1	0	1	0	1.55
1	0	1	1	1.50
1	1	0	0	1.45
1	1	0	1	1.40
1	1	1	0	1.35
1	1	1	1	1.30

In addition, the AMD Athlon processor provides the VCC2SEL signal to identify the core voltage of the L2 cache SRAMs. Like the VID signals, the AMD Athlon processor either connects the VCC2SEL to VSS or has an open value, with a pullup resistor on the motherboard. An open value indicates that a voltage of 2.5V is required for VCC_SRAM, while a VSS indicates a required voltage of 3.3V.

6.4 Frequency Identification

The AMD Athlon processor provides four frequency ID signals (FID[3:0]) to the system controller to indicate the SYSCLK multiplier at which the processor core operates. This mechanism is automatic, using the system controller and the BIOS without jumpers on the motherboard to set the operating frequency of the AMD Athlon processor.

6.5 Decoupling

See the *AMD Athlon™ Processor Voltage Regulation Design Application Note*, order# 22651, or contact your local AMD office for information about the decoupling required on the motherboard for use with the AMD Athlon processor.

6.6 Termination

Table 7 lists the layout and termination for Slot A signals and clocks. For additional information concerning termination design guidelines for AMD Athlon processor-based systems, contact your local AMD representative to obtain detailed documentation available under a non-disclosure agreement.

Table 7. Signal and Clock Layout and Termination Requirements

Group/Name	Termination Requirements
SYSCLK, SYSCLK#	Differential clock inputs to the system controller (Northbridge) and Slot A. Point-to-point system clocks driven by the central system clock generator. See "SYSCLK, SYSCLK#" on page 27.
SDATA0, SDATA1, SDATA2, SDATA3, SADDIN, SADDOUT[1]	47 ohm pullup resistors must be kept with 1" of Northbridge. See "OD Termination" on page 27.
CLKFWDRST, CONNECT, PROCRDY	
PICCLK[2]	These signals must be pulled to 2.5 V on the motherboard using a 330-ohm resistor to Vcc3 and a 1.0-kohm resistor to VSS.
PICD[1:0][2]	
NMI, INTR, SMI#, INIT#, A20M#, IGNNE#, STPCLK#, CPURESET#	Route to minimum length where possible. HSTL-like inputs. Point-to-point signals driven by the peripheral bus controller (Southbridge) to the Slot A connector. These signals are pulled to VCC_CORE on the Slot A card and do not require termination on the motherboard.

Notes:
1. *See Table 5, "Source-Synchronous Clock Signal Groups," on page 24.*
2. *The industry-standard APIC signals, PICCLK and PICD[1:0]#, are not available on Model 1.*

OD Termination

Both the processor and Northbridge use HSTL-like open-drain outputs and HSTL-like inputs. Therefore, the bus signals must be terminated both at the source and the destination with 47-Ω pullup resistors to VCC_CORE. Pullups at the processor are located on the processor module and need not be considered during motherboard layout. Consequently, the only terminations required on the motherboard are the pullup resistors at the Northbridge. These pullup termination resistors must be located 1 inch from the Northbridge.

For systems that do not support ECC, SCHECK[7:0]# should be tied to VCC_CORE with a 47-ohm pullup, with minimal routing where possible.

CLKFWD Signal Groups

The termination scheme for all clock forward signals, both signal and clock, involves having each end terminated by a 47-ohm pullup resistor located 1 inch from each device. Pullups at the processor are located on the processor module and need not be considered during motherboard layout.

Note: *The data bus, SDATA[63:0], drives in both directions and, therefore, must have a unidirectional clock for each data group travelling each way.*

SYSCLK, SYSCLK#

Each of the two SYSCLK pairs from the clock generator to the processor, SYSCLK and SYSCLK# (true and complimentary), are series terminated at the source with a 47-ohm resistor located a maximum distance of 0.5 inch from the clock generator and parallel terminated at the end with a 47-ohm resistor to VCC_CORE. Parallel termination occurs on the processor module and need not be considered during motherboard layout.

6.7 Operating Ranges

The AMD Athlon processor is designed to provide functional operation if the voltage and temperature parameters are within the limits defined in Table 8.

Table 8. Operating Ranges

Parameter	Description		Min	Nominal	Max	Notes
VCC_CORE	AMD Athlon™ processor **Model 1** core supply	500–700 MHz	1.5 V	1.6 V	1.7 V	1
	AMD Athlon processor **Model 2** core supply	550–750 MHz	1.5 V	1.6 V	1.7 V	
		800–850 MHz	1.6 V	1.7 V	1.8 V	
		900–1000 MHz	1.7 V	1.8 V	1.9 V	
	AMD Athlon processor **Model 4** core supply	650–850 MHz	1.6 V	1.7 V	1.8 V	
		900–1000 MHz	1.65 V	1.75 V	1.85 V	
VCC_CORE_{SLEEP}	AMD Athlon processor core supply in Sleep state		1.2 V	1.3 V	1.4 V	2
VCC_SRAM	2.5 V SRAM core supply		2.475 V	2.5 V	2.625 V	3
	3.3 V SRAM core supply		3.15 V	3.3 V	3.45 V	4
T_{PLATE}	Temperature of thermal plate				70° C	

Notes:

1. *Normal operating conditions*
2. *For Sleep state operating conditions*
3. *Value of VCC_SRAM when VCC2SEL is High*
4. *Value of VCC_SRAM when VCC2SEL is Low*

6.8 Absolute Ratings

The AMD Athlon processor should not be subjected to conditions exceeding the absolute ratings listed in Table 9, as such conditions may adversely affect long term reliability or result in functional damage.

Table 9. Absolute Ratings

Parameter	Description	Min	Max	Notes
VCC_CORE	AMD Athlon™ processor core supply	–0.5 V	nominal + 0.5 V	
VCC_SRAM	2.5 V SRAM core supply	–0.5 V	3.0 V	1
VCC_SRAM	3.3 V SRAM core supply	–0.5 V	4.0 V	2
V_{PIN}	Voltage on any system bus pin	TBD	TBD	
$T_{STORAGE}$	Storage temperature of processor	–40° C	85° C	

Notes:

1. *Value of VCC_SRAM when VCC2SEL is Low*
2. *Value of VCC_SRAM when VCC2SEL is High*

6.9 Power Dissipation

Table 10 shows the power and current of the AMD Athlon processor Model 1, Model 2, and Model 4 during normal and reduced power states.

Table 10. VCC_CORE Power and Current for Model 1, Model 2, and Model 4

Frequency (MHz)	Maximum Thermal Power	Typical Thermal Power	Stop Grant (Maximum)[4]	Maximum I_{CC} (Power Supply Current)	Notes
Model 1					
500	42 W	38 W	6 W	25 A	1, 6
550	46 W	41 W	6 W	30 A	1, 6
600	50 W	45 W	6 W	33 A	1, 6
650	54 W	48 W	6 W	36 A	1, 6
700	50 W	45 W	6 W	33 A	1, 6
Model 2					
550	31 W	28 W	6 W	20 A	1, 6
600	34 W	30 W	6 W	21 A	1, 6
650	36 W	32 W	6 W	22 A	1, 6
700	39 W	34 W	6 W	24 A	1, 6
750	40 W	35 W	7 W	25 A	1, 6
800	48 W	43 W	7 W	29 A	2, 7
850	50 W	45 W	8 W	30 A	2, 7
900	60 W	53 W	9 W	34 A	4, 9
950	62 W	55 W	9 W	35 A	4, 9
1000	65 W	60 W	9 W	37 A	4, 9

Notes:

1. *Power measured at 1.6V nominal*
2. *Power measured at 1.7V nominal*
3. *Power measured at 1.75V nominal*
4. *Power measured at 1.8V nominal*
5. *Sleep state operating conditions measured at 1.3V*
6. *I_{CC} measured at maximum VCC_CORE = 1.7V—Power supply designs must take into account the maximum power supply current.*
7. *I_{CC} measured at maximum VCC_CORE = 1.8V—Power supply designs must take into account the maximum power supply current.*
8. *I_{CC} measured at maximum VCC_CORE = 1.85V—Power supply designs must take into account the maximum power supply current.*
9. *I_{CC} measured at maximum VCC_CORE = 1.9V—Power supply designs must take into account the maximum power supply current.*

Table 10. VCC_CORE Power and Current for Model 1, Model 2, and Model 4 (continued)

Frequency (MHz)	Maximum Thermal Power	Typical Thermal Power	Stop Grant (Maximum)[4]	Maximum I_{CC} (Power Supply Current)	Notes
Model 4					
650	36.1 W	32.4 W	5 W	23.8 A	2, 7
700	38.3 W	34.4 W	5 W	25.2 A	2, 7
750	40.4 W	36.3 W	5 W	26.6 A	2, 7
800	42.6 W	38.3 W	5 W	28.0 A	2, 7
850	44.8 W	40.2 W	5 W	29.4 A	2, 7
900	49.7 W	44.6 W	5 W	31.7 A	3, 8
950	52.0 W	46.7 W	5 W	33.2 A	3, 8
1000	54.3 W	48.7 W	5 W	34.6 A	3, 8

Notes:

1. *Power measured at 1.6V nominal*
2. *Power measured at 1.7V nominal*
3. *Power measured at 1.75V nominal*
4. *Power measured at 1.8V nominal*
5. *Sleep state operating conditions measured at 1.3V*
6. *I_{CC} measured at maximum VCC_CORE = 1.7V—Power supply designs must take into account the maximum power supply current.*
7. *I_{CC} measured at maximum VCC_CORE = 1.8V—Power supply designs must take into account the maximum power supply current.*
8. *I_{CC} measured at maximum VCC_CORE = 1.85V—Power supply designs must take into account the maximum power supply current.*
9. *I_{CC} measured at maximum VCC_CORE = 1.9V—Power supply designs must take into account the maximum power supply current.*

6.10 DC Characteristics

The DC characteristics of the AMD Athlon processor are shown in Table 11. These values are defined at the card edge of the AMD Athlon processor module.

Table 11. DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{REF}	DC Input Reference Voltage		(0.47*VCC_CORE) –50	(0.47*VCC_CORE) +50	mV	1
I_{VREF}	V_{REF} Input Pin Current	$0 < V_{IN} <$ VCC_CORE	–250	+250	µA	2
V_{IH-DC}	DC Input High Voltage		V_{REF} + 325	VCC_CORE + 300	mV	
V_{IL-DC}	DC Input Low Voltage		–300	V_{REF} + 75	mV	
V_{IH-AC}	AC Input High Voltage		V_{REF} + 450	VCC_CORE + 500	mV	
V_{IL-AC}	AC Input Low Voltage		–500	V_{REF} – 50	mV	
V_{OH-DC}	DC Output High Voltage		VCC_CORE	VCC_CORE + 300	mV	3
V_{OL-DC}	DC Output Low Voltage	$I_{OUT}= I_{OL-DC-MAX}$	–300	+300	mV	3
V_{OH-AC}	AC Output High Voltage		VCC_CORE	VCC_CORE + 500	mV	3
V_{OL-AC}	AC Output Low Voltage		–500	400	mV	3
I_{OL-DC}	DC Output Current Low	$V_{OUT}= V_{OL-DC-MAX}$	–	33	mA	
I_{LEAK}	Tristate Leakage	$0 < V_{IN} <$ VCC_CORE	–100	+100	µA	4
I_{IH}	Input High Current	$V_{IN}=V_{IH-DC-MIN}$	0	500	µA	
I_{IL}	Input Low Current	$V_{IN}=V_{IL-DC-MAX}$	0	500	µA	
C_{IN}	Input Pin Capacitance		4	12	pF	5, 6

Notes:

1. *V_{REF}:*
   – V_{REF} is nominally set by a (1%) resistor divider from VCC_CORE.
   – The suggested divider resistor values are 90.9 ohms over 80.6 ohms to produce a divisor of 0.47.
   – The internal V_{REF} ($V_{REF-INT}$) is the external V_{REF} scaled by 0.80 ($V_{REF-INT} = (V_{REF}/0.80)$). (Processor pin SysVrefMode = High)
   *– Example: VCC_CORE = 1.6V, V_{REF} = 752mV (1.6 * 0.47), $V_{REF-INT}$ = 940mV (752mV/0.8).*
   – Peak-to-Peak AC noise on V_{REF} (AC) should not exceed 2% of V_{REF} (DC).
2. *I_{VREF} should be measured at nominal V_{REF}.*
3. *$V_{OL-DC-MAX}$, $V_{OL-AC-MAX}$, $V_{OH-DC-MIN}$ and $V_{OH-AC-MIN}$ are specified at T = 100°C and VCC_CORE = 1.4V.*
4. *Does not apply to V_{REF}.*
5. *The SYSCLK and SYSCLK# signals have twice the capacitance because they connect to two input pads. SYSCLK connects to CLKIN/RSTCLK. SYSCLK# connects to CLKIN#/RSTCLK#.*
6. *The following information pertains only to Model 1 and Model 2. The SDATAINCLK[3:0]# signals have twice the capacitance because they connect to two input pads. SDATAINCLK[3:0]# connects two byte clocks to form a word sized clock.*

6.11 AC Characteristics

Table 12 shows the AC characteristics for the AMD Athlon processor. The parameters are grouped based on the source or destination of the signals involved. All parameters are defined at the card edge of the AMD Athlon processor module.

Table 12. AC Characteristics

Group	Symbol	Parameter	Min	Max	Units	Notes
All Signals	T_{RISE}	Output Rise Slew Rate	1	3	V/ns	1
	T_{FALL}	Output Fall Slew Rate	1	3	V/ns	1
Clock Forward	$T_{SKEW-SAMEEDGE}$	Output skew with respect to the same clock edge	–	385	ps	2
	$T_{SKEW-DIFFEDGE}$	Output skew with respect to a different clock edge	–	770	ps	2
	T_{SU}	Input Data Setup Time	300	–	ps	3
	T_{HD}	Input Data Hold Time	300	–	ps	3
	C_{IN}	Capacitance on input Clocks	4	12	pF	
	C_{OUT}	Capacitance on output Clocks	4	12	pF	
Sync *4	T_{VAL}	RstClk to Output Valid	250	2000	ps	5
	T_{SU}	Setup to RstClk	500	–	ps	6
	T_{HD}	Hold from RstClk	1000	–	ps	6

Notes:

– Test Circuit used—See Figure 8 on page 34.

1. *Rise and fall time ranges are guidelines over which the I/O has been characterized.*
2. *$T_{K7-SKEW-SAMEEDGE}$ is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to the same clock edge.*
   $T_{K7-SKEW-DIFFEDGE}$ is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to different clock edges.
3. *Input SU and HD times are with respect to the appropriate Clock Forward Group input clock.*
4. *The synchronous signals include PROCRDY, CONNECT, CLKFWDRST.*
5. *T_{VAL} is RstClk rising edge to output valid for PROCRDY. Test Load—25pf.*
6. *T_{SU} is setup of CONNECT/CLKFWDRST to rising edge of RSTCLK. T_{HD} is hold of CONNECT/CLKFWDRST from rising edge of RSTCLK.*

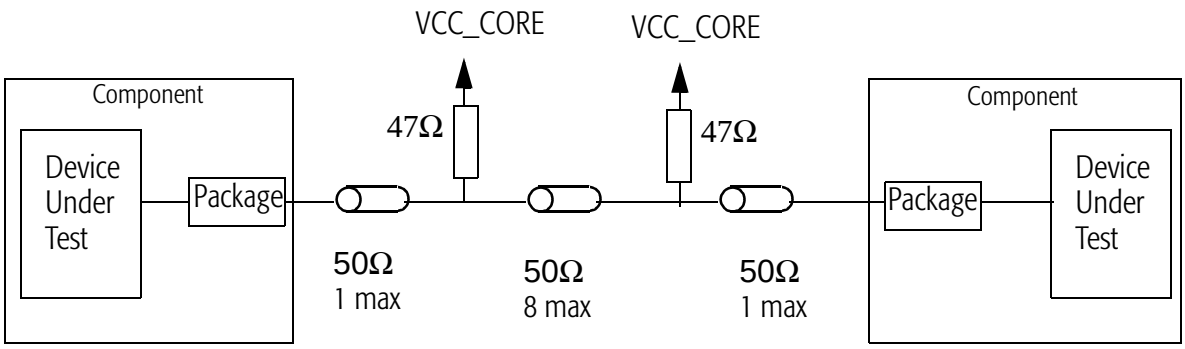


Figure 8. Test Circuit

6.12 Southbridge AC and DC Characteristics

Table 13 shows the AC and DC characteristics of the AMD Athlon processor Southbridge pins.

Table 13. Southbridge AC and DC Characteristics*

Symbol	Parameter Description	Min	Nominal	Max	Units	Notes
V_{IH}	Input High Voltage	VCC_CORE Min		VCC_CORE Max	V	1,2
V_{IL}	Input Low Voltage	–300		400	mV	1,2
Delta V_{RB}	Hysteresis change in V_{IX}	180		250	mV	
V_{OH}	Output High Voltage	VCC_CORE – 400		VCC_CORE + 300	mV	
V_{OL}	Output Low Voltage	–300		400	mV	
I_{LEAK}	Tristate Leakage	–100		100	uA	
I_{IH}	Input High Current	–100		100	uA	
I_{IL}	Input Low Current	–100		100	uA	
I_{OH}	Output High Current			–21	mA	4
I_{OL}	Output Low Current	27			mA	4
T_{SU}	Sync Input Setup Time	2.0			nS	5,6
T_{HD}	Sync Input Hold Time	0.0			pS	5,6
T_{DELAY}	Output Delay with respect to RSTCLK	0.0		6.1	nS	6
T_{BIT}	Input Time to Acquire	20.0			nS	8,9
T_{RPT}	Input Time to Reacquire	40.0			nS	10–14
V_{IN}	DC Input Voltage	–300		VCC_CORE + 300	mV	

Notes:

* *These parameters pertain to the Southbridge signals listed in Table 4 on page 24.*

1. *Characterized across DC supply voltage range.*
2. *Values specified at nominal VCC_CORE. Scale parameters with VCC_CORE.*
3. *Hysteresis values refer to the difference between initial and return switching points.*
4. *I_{OL} and I_{OH} are measured at V_{OL} max and V_{OH} min, respectively.*
5. *Synchronous inputs/outputs are specified with respect to RSTCLK and RSTCK# at the pins.*
6. *These are aggregate numbers. The specific pins vary widely within this window.*
7. *Edge rates indicate the range over which inputs were characterized.*
8. *In asynchronous operation, the signal must persist for this time to guarantee capture.*
9. *This value assumes RSTCLK frequency is 10ns ⟹ TBIT = 2*fRST.*
10. *The approximate value for standard case in normal mode operation.*
11. *This value is dependent on RSTCLK frequency, divisors, LowPower mode, and core frequency.*
12. *Reassertions of the signal within this time are not guaranteed to be seen by the core.*
13. *This value assumes that the skew between RSTCLK and K7CLKOUT is much less than one phase.*
14. *This value assumes RSTCLK and K7CLKOUT are running at the same frequency, though the processor is capable of other configurations.*

Table 13. Southbridge AC and DC Characteristics* (continued)

Symbol	Parameter Description	Min	Nominal	Max	Units	Notes
T_{RISE}	Signal Rise Time	1.0		3.0	V/nS	7
T_{FALL}	Signal Fall Time	1.0		3.0	V/nS	7
C_{PIN}	Pin Capacitance	4		12	pF	

Notes:

* *These parameters pertain to the Southbridge signals listed in Table 4 on page 24.*

1. *Characterized across DC supply voltage range.*
2. *Values specified at nominal VCC_CORE. Scale parameters with VCC_CORE.*
3. *Hysteresis values refer to the difference between initial and return switching points.*
4. *I_{OL} and I_{OH} are measured at V_{OL} max and V_{OH} min, respectively.*
5. *Synchronous inputs/outputs are specified with respect to RSTCLK and RSTCK# at the pins.*
6. *These are aggregate numbers. The specific pins vary widely within this window.*
7. *Edge rates indicate the range over which inputs were characterized.*
8. *In asynchronous operation, the signal must persist for this time to guarantee capture.*
9. *This value assumes RSTCLK frequency is 10ns ==> TBIT = 2*fRST.*
10. *The approximate value for standard case in normal mode operation.*
11. *This value is dependent on RSTCLK frequency, divisors, LowPower mode, and core frequency.*
12. *Reassertions of the signal within this time are not guaranteed to be seen by the core.*
13. *This value assumes that the skew between RSTCLK and K7CLKOUT is much less than one phase.*
14. *This value assumes RSTCLK and K7CLKOUT are running at the same frequency, though the processor is capable of other configurations.*

6.13 APIC Pin AC and DC Characteristics

Table 14 shows the AC and DC characteristics of the AMD Athlon processor APIC pins.

Table 14. APIC Pin AC and DC Characteristics

Symbol	Parameter Description	Min	Nominal	Max	Units	Notes
V_{IH}	Input High Voltage	1.7		2.625	V	1,3
V_{IL}	Input Low Voltage	–300		700	mV	1,2
V_{OH}	Output High Voltage			2.625	V	3
V_{OL}	Output Low Voltage	–300		400	mV	
I_{LEAK}	Tristate Leakage	–100		100	uA	
I_{IH}	Input High Current	–100		100	uA	
I_{IL}	Input Low Current	–100		100	uA	
I_{OL}	Output Low Current	27			mA	4
T_{RISE}	Signal Rise Time	1.0		3.0	V/nS	5
T_{FALL}	Signal Fall Time	1.0		3.0	V/nS	5
C_{PIN}	Pin Capacitance	4		12	pF	

Notes:

1. *Characterized across DC supply voltage range*
2. *Values specified at nominal VDD (1.5V). Scale parameters with VDD*
3. *2.625V = 2.5V + 5% maximum*
4. *I_{OL} is measured at V_{OL} max*
5. *Edge rates indicate the range over which inputs were characterized*

6.14 Signal and Power-Up Requirements

For information about the signal and power-up requirements for the AMD Athlon processor module, see the *AMD Athlon™ Processor Module Signal and Power-Up Requirements Application Note*, order#23811.

7 Mechanical Data

7.1 Introduction

The AMD Athlon™ processor module is comprised of a processor, L2 cache, passive components, a thermal plate, and a cover plate. The AMD Athlon processor connects to the motherboard through insertion into a connector known as Slot A.

7.2 Module Dimensions

Table 15 shows the dimensions of the AMD Athlon processor module.

Table 15. AMD Athlon™ Processor Module Dimensions

Description	Min	Max	Figure
Module Length	5.505 inches	5.515 inches	10 on page 41
Module Height	2.451 inches	2.483 inches	10
Module Depth	0.637 inch	0.657 inch	10
Thermal Plate Length	5.331 inches	5.351 inches	11 on page 42
Thermal Plate Height	1.917 inches	1.927 inches	11

Figures 10 through 14 starting on page 41 show the critical dimensions of the AMD Athlon processor module. All dimensions in the drawings are in inches and are not to scale. Table 16 lists the notes that pertain to the dimension drawings.

Table 16. Notes for Dimension Drawings

Note	Description
6	Area for part number and traceability information
7	Rivscrew attach hole. Maximum insertion depth: 0.269″
8	Heatsink clip attach hole. Maximum insertion depth: 0.233″
9	Thermal grease centered on SRAM pedestal

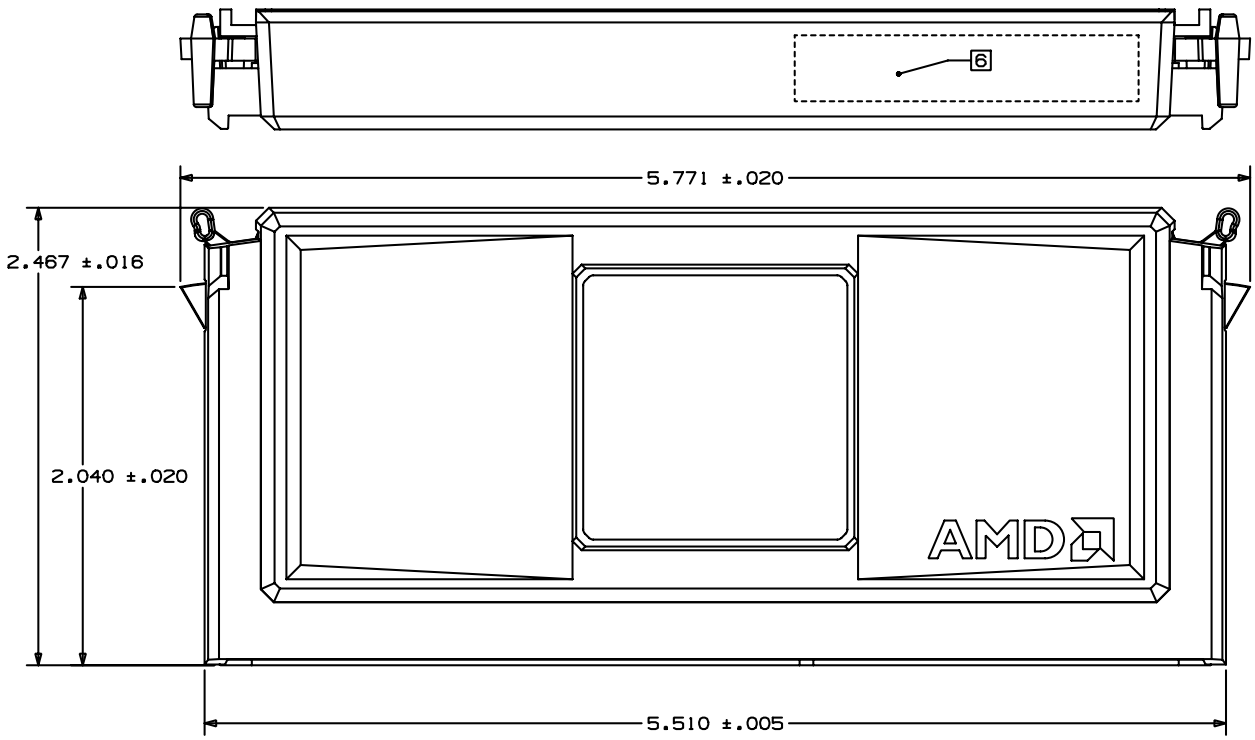


Figure 9. AMD Athlon™ Processor Module Dimensions—Front View

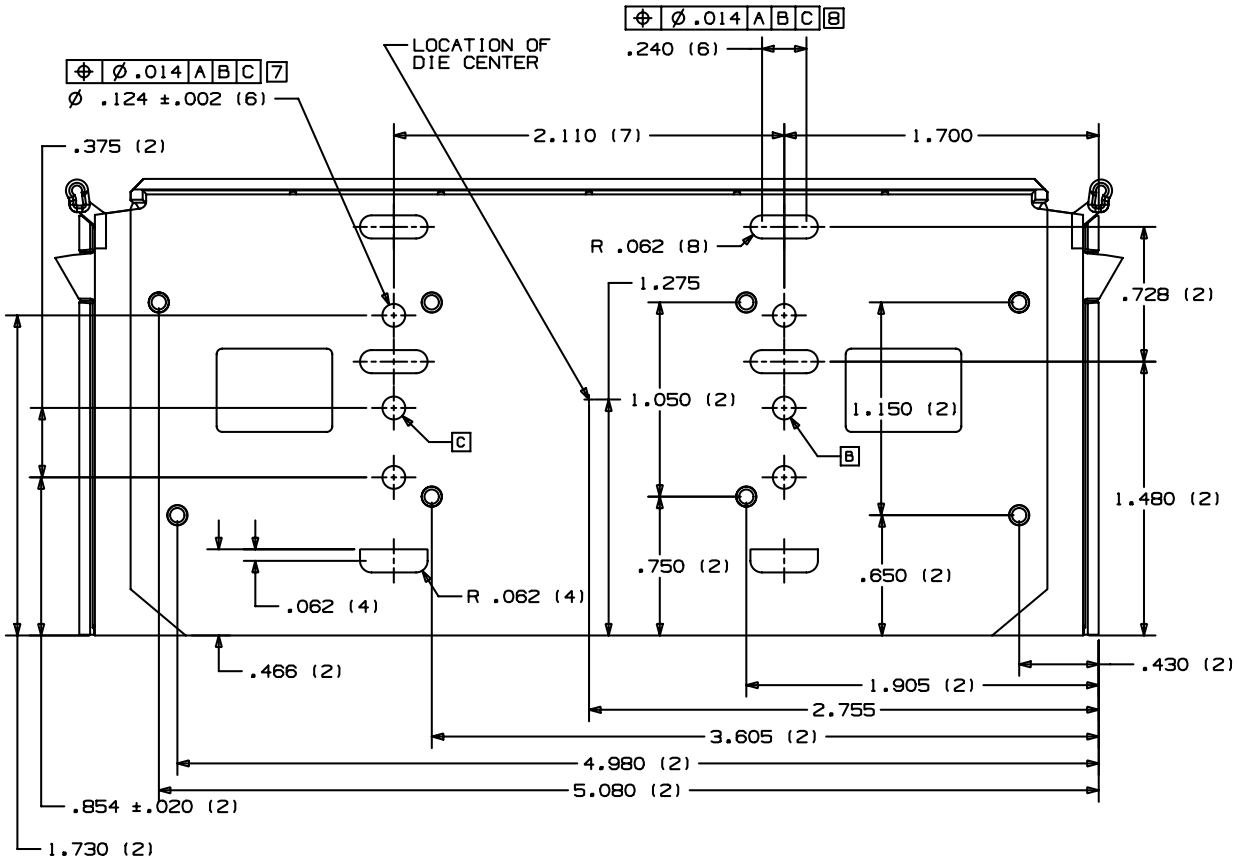


Figure 10. AMD Athlon™ Processor Module Dimensions—Plate Side View

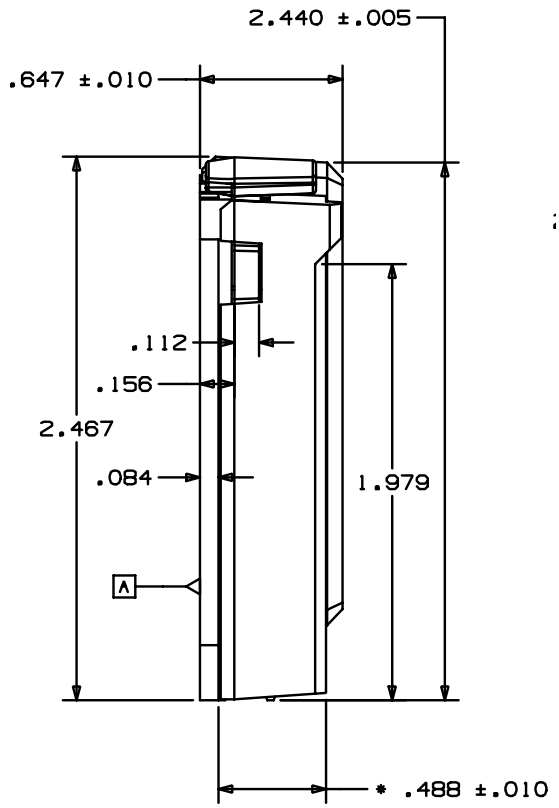


Figure 11. AMD Athlon™ Processor Module Dimensions—Side View

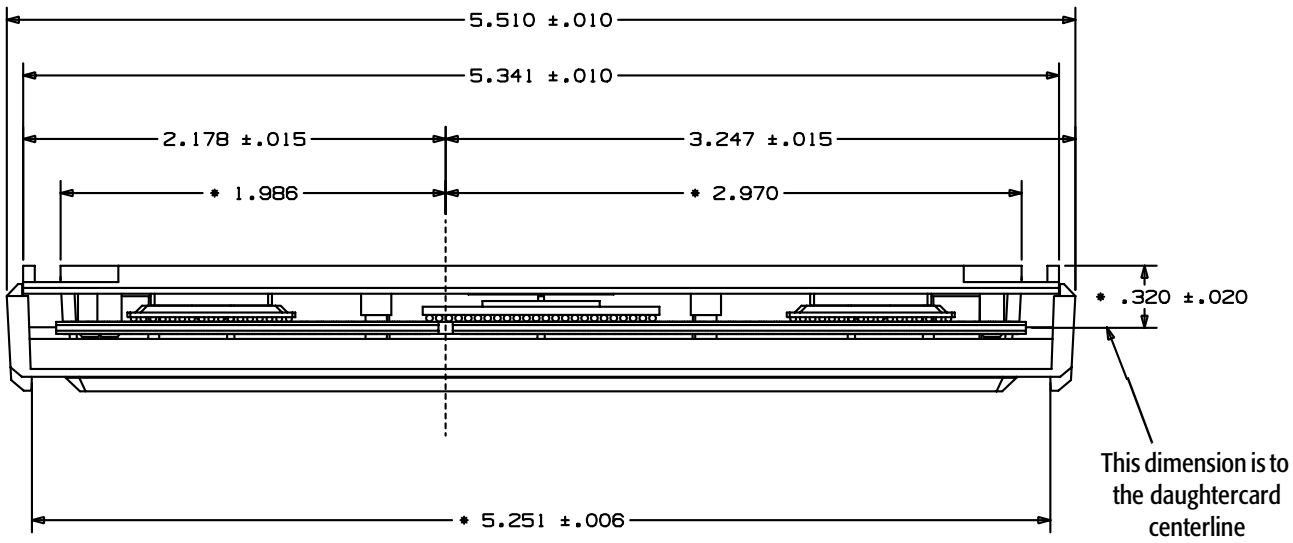


Figure 12. AMD Athlon™ Processor Module Dimensions—Edge View

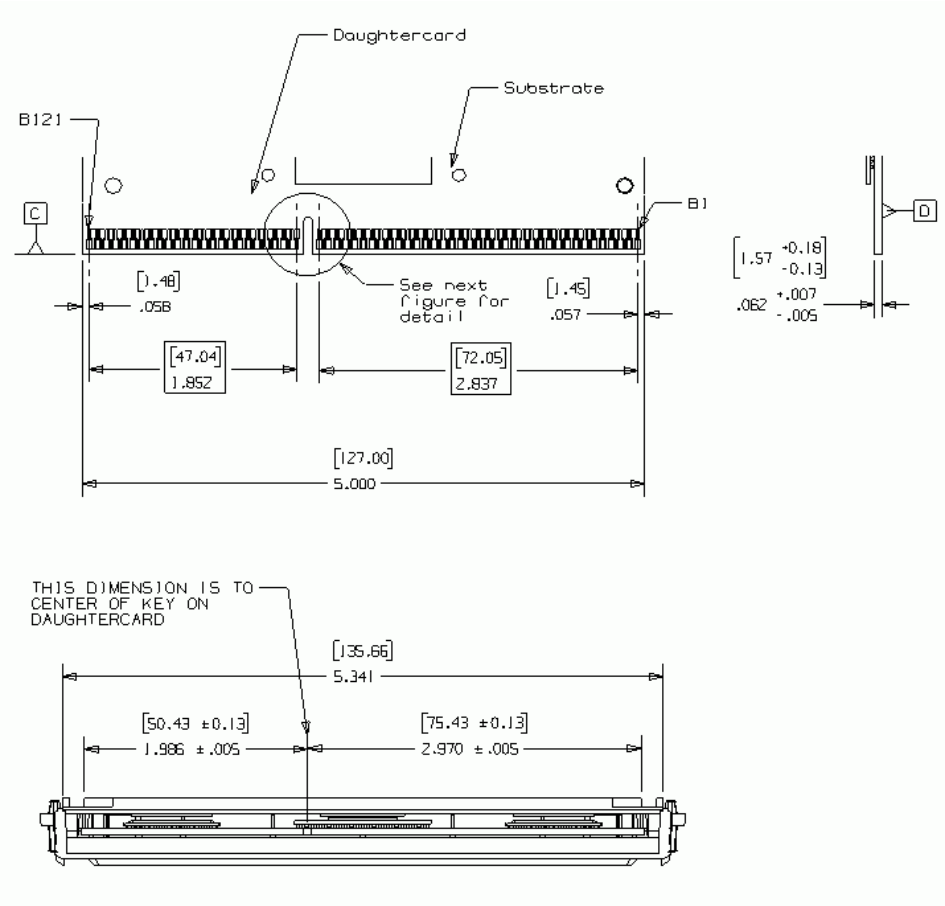


Figure 13. Card Edge Dimensions—Thermal Plate Side View

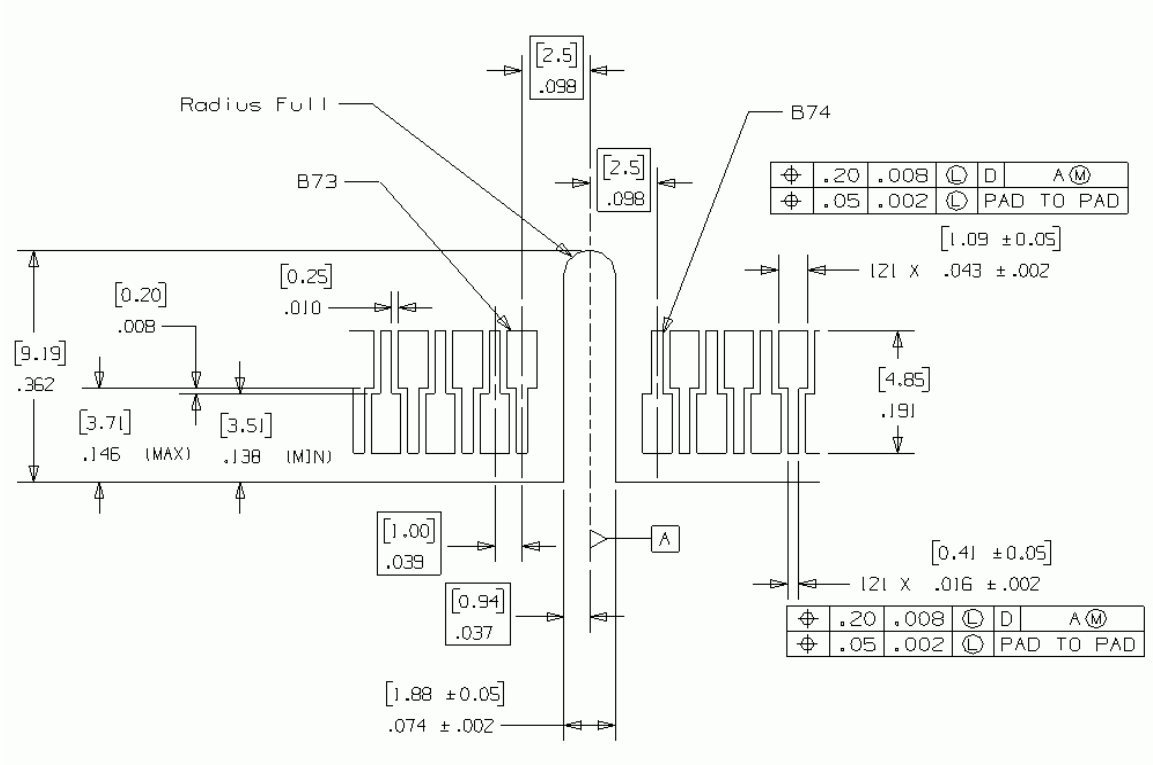


Figure 14. Card Edge Dimensions (Detail)

7.3 AMD Athlon™ Processor Card-Edge Signal Listing

Tables 17 through 19 shows the Slot A signals and pins ordered by pin number, pin name, and their physical position on the slot, respectively. The *High* and *Low* designation in the *Pin Name* column in Table 19 refers to the staggered high/low arrangement of the pins on the slot.

Three additional APIC-related signals have been designated (PICD[1:0]# and PICCLK), which are detailed in Tables 17 through 19. On Model 1, these pins are reserved.

Table 17. AMD Athlon™ Processor Signals Ordered by Pin Number

Pin No.	Pin Name	Pin No.	Pin Name
A1	VCC2SEL	B1	SADDOUT[14]#
A2	VCC_SRAM[7]	B2	GND[10]
A3	PICCLK (Not present on Model 1)	B3	SADDOUT[13]#
A4	VCC_SRAM[6]	B4	SADDOUT[7]#
A5	PICD[0] (Not present on Model 1)	B5	GND[51]
A6	VCC_SRAM[5]	B6	SADDOUTCLK#
A7	PICD[1] (Not present on Model 1)	B7	GND[7]
A8	VCC_SRAM[4]	B8	SADDOUT[12]#
A9	SMI#	B9	GND[21]
A10	VCC_SRAM[3]	B10	SADDOUT[9]#
A11	FERR	B11	SADDOUT[8]#
A12	INIT#	B12	GND[20]
A13	NMI	B13	SADDOUT[5]#
A14	VCC_SRAM[2]	B14	SADDOUT[6]#
A15	INTR	B15	GND[30]
A16	VCC_SRAM[1]	B16	SADDOUT[2]#
A17	RESET#	B17	GND[44]
A18	STPCLK#	B18	SADDOUT[3]#
A19	IGNNE#	B19	GND[19]
A20	VCC_SRAM[8]	B20	SDATAOUTCLK[3]#
A21	A20M#	B21	GND[40]
A22	VCC_CORE[41]	B22	SCHECK[6]#
A23	SADDOUT[10]#	B23	SDATA[53]#
A24	VCC_CORE[1]	B24	GND[8]
A25	SADDOUT[11]#	B25	SDATA[49]#
A26	VCC_CORE[19]	B26	SDATA[63]#
A27	SADDOUT[4]#	B27	GND[32]
A28	VCC_CORE[44]	B28	SDATAINCLK[3]#
A29	SDATA[55]#	B29	GND[3]
A30	VCC_CORE[10]	B30	SDATA[62]#
A31	SDATA[54]#	B31	GND[1]
A32	VCC_CORE[11]	B32	SDATA[60]#

Table 17. AMD Athlon™ Processor Signals Ordered by Pin Number (continued)

Pin No.	Pin Name	Pin No.	Pin Name
A33	SDATA[52]#	B33	GND[13]
A34	VCC_CORE[35]	B34	SCHECK[7]#
A35	SDATA[61]#	B35	SDATA[59]#
A36	VCC_CORE[25]	B36	GND[2]
A37	SDATA[50]#	B37	SDATA[58]#
A38	VCC_CORE[4]	B38	SDATA[57]#
A39	SDATA[51]#	B39	GND[16]
A40	VCC_CORE[26]	B40	SDATA[39]#
A41	SDATA[48]#	B41	GND[39]
A42	VCC_CORE[34]	B42	SDATA[56]#
A43	SDATA[36]#	B43	GND[38]
A44	VCC_CORE[16]	B44	SDATA[47]#
A45	SDATA[46]#	B45	SDATA[38]#
A46	VCC_CORE[38]	B46	GND[41]
A47	SDATA[37]#	B47	SDATA[45]#
A48	VCC_CORE[20]	B48	SDATA[44]#
A49	SDATA[35]#	B49	GND[37]
A50	VCC_CORE[30]	B50	SDATAINCLK[2]#
A51	SCHECK[4]#	B51	GND[34]
A52	VCC_CORE[3]	B52	SCHECK[5]#
A53	SDATA[34]#	B53	GND[33]
A54	VCC_CORE[31]	B54	SDATA[43]#
A55	SDATA[33]#	B55	SDATA[42]#
A56	VCC_CORE[29]	B56	GND[22]
A57	SDATA[32]#	B57	SDATA[41]#
A58	VCC_CORE[7]	B58	SDATA[40]#
A59	SDATAOUTCLK[2]#	B59	GND[50]
A60	VCC_CORE[18]	B60	SDATAOUTCLK[1]#
A61	SDATA[30]#	B61	GND[31]
A62	VCC_CORE[15]	B62	SDATA[22]#
A63	SDATA[31]#	B63	GND[35]
A64	VCC_CORE[14]	B64	SDATA[23]#
A65	SCHECK[3]#	B65	GND[36]
A66	VCC_CORE[33]	B66	SDATA[21]#
A67	SDATAINCLK[1]#	B67	GND[49]
A68	VCC_CORE[32]	B68	SDATA[20]#
A69	SDATA[29]#	B69	GND[14]
A70	SDATA[28]#	B70	SDATA[19]#
A71	VCC_CORE[9]	B71	SCHECK[2]#
A72	SDATA[26]#	B72	GND[9]
A73	SDATA[27]#	B73	SDATA[18]#
A74	VCC_CORE[42]	B74	SDATA[7]#
A75	SDATA[25]#	B75	GND[23]
A76	VCC_CORE[13]	B76	SDATA[17]#
A77	SDATA[24]#	B77	GND[15]

Table 17. AMD Athlon™ Processor Signals Ordered by Pin Number (continued)

Pin No.	Pin Name	Pin No.	Pin Name
A78	VCC_CORE[27]	B78	SDATA[16]#
A79	SDATA[15]#	B79	GND[27]
A80	VCC_CORE[24]	B80	SDATA[6]#
A81	SDATA[1]#	B81	SDATA[5]#
A82	VCC_CORE[2]	B82	GND[28]
A83	SDATA[12]#	B83	SCHECK[0]#
A84	VCC_CORE[23]	B84	SDATA[4]#
A85	SCHECK[1]#	B85	GND[29]
A86	VCC_CORE[5]	B86	SDATA[2]#
A87	SDATA[8]#	B87	GND[25]
A88	VCC_CORE[39]	B88	SDATAINCLK[0]#
A89	SDATA[10]#	B89	GND[26]
A90	VCC_CORE[22]	B90	SDATA[3]#
A91	SDATAOUTCLK[0]#	B91	GND[6]
A92	VCC_CORE[21]	B92	SDATA[0]#
A93	SADDIN[7]#	B93	GND[5]
A94	VCC_CORE[40]	B94	SDATA[13]#
A95	SADDIN[6]#	B95	SDATA[14]#
A96	VCC_CORE[37]	B96	GND[4]
A97	SADDIN[8]#	B97	SDATA[11]#
A98	VCC_CORE[6]	B98	SDATA[9]#
A99	SDATAOUTVAL#	B99	GND[17]
A100	VCC_CORE[28]	B100	SADDIN[5]#
A101	SDATAINVAL#	B101	GND[18]
A102	VCC_CORE[36]	B102	SADDIN[11]#
A103	CONNECT	B103	GND[45]
A104	VCC_CORE[12]	B104	SADDIN[2]#
A105	CLKFWDRST	B105	GND[48]
A106	PROCRDY	B106	SADDIN[3]#
A107	VCC_CORE[43]	B107	SADDIN[4]#
A108	SYSCLK#	B108	GND[46]
A109	SYSCLK	B109	SADDIN[10]#
A110	VCC_CORE[17]	B110	SADDIN[9]#
A111	PWROK	B111	GND[43]
A112	VID[0]	B112	SADDIN[13]#
A113	VID[1]	B113	GND[42]
A114	VID[2]	B114	SADDINCLK#
A115	VID[3]	B115	GND[11]
A116	FID[3]	B116	SADDIN[14]#
A117	FID[2]	B117	GND[12]
A118	FID[1]	B118	SFILLVAL#
A119	FID[0]	B119	GND[47]
A120	COREFB+	B120	SADDIN[12]#
A121	COREFB–	B121	GND[24]

Table 18. AMD Athlon™ Processor Signals Ordered by Pin Name

Pin Name	Pin No.	Pin Name	Pin No.
A20M#	A21	GND[25]	B87
CLKFWDRST	A105	GND[26]	B89
CONNECT	A103	GND[27]	B79
COREFB+	A120	GND[28]	B82
COREFB–	A121	GND[29]	B85
FERR	A11	GND[30]	B15
FID[0]	A119	GND[31]	B61
FID[1]	A118	GND[32]	B27
FID[2]	A117	GND[33]	B53
FID[3]	A116	GND[34]	B51
GND[1]	B31	GND[35]	B63
GND[2]	B36	GND[36]	B65
GND[3]	B29	GND[37]	B49
GND[4]	B96	GND[38]	B43
GND[5]	B93	GND[39]	B41
GND[6]	B91	GND[40]	B21
GND[7]	B7	GND[41]	B46
GND[8]	B24	GND[42]	B113
GND[9]	B72	GND[43]	B111
GND[10]	B2	GND[44]	B17
GND[11]	B115	GND[45]	B103
GND[12]	B117	GND[46]	B108
GND[13]	B33	GND[47]	B119
GND[14]	B69	GND[48]	B105
GND[15]	B77	GND[49]	B67
GND[16]	B39	GND[50]	B59
GND[17]	B99	GND[51]	B5
GND[18]	B101	IGNNE#	A19
GND[19]	B19	INIT#	A12
GND[20]	B12	INTR	A15
GND[21]	B9	NMI	A13
GND[22]	B56	PICCLK (Not present on Model 1)	A3
GND[23]	B75	PICD[0] (Not present on Model 1)	A5
GND[24]	B121	PICD[1] (Not present on Model 1)	A7
PROCRDY	A106	SCHECK[3]#	A65
PWROK	A111	SCHECK[4]#	A51
RESET#	A17	SCHECK[5]#	B52
SADDIN[2]#	B104	SCHECK[6]#	B22
SADDIN[3]#	B106	SCHECK[7]#	B34
SADDIN[4]#	B107	SDATA[0]#	B92
SADDIN[5]#	B100	SDATA[1]#	A81
SADDIN[6]#	A95	SDATA[2]#	B86
SADDIN[7]#	A93	SDATA[3]#	B90
SADDIN[8]#	A97	SDATA[4]#	B84

Table 18. AMD Athlon™ Processor Signals Ordered by Pin Name (continued)

Pin Name	Pin No.	Pin Name	Pin No.
SADDIN[9]#	B110	SDATA[5]#	B81
SADDIN[10]#	B109	SDATA[6]#	B80
SADDIN[11]#	B102	SDATA[7]#	B74
SADDIN[12]#	B120	SDATA[8]#	A87
SADDIN[13]#	B112	SDATA[9]#	B98
SADDIN[14]#	B116	SDATA[10]#	A89
SADDINCLK#	B114	SDATA[11]#	B97
SADDOUT[2]#	B16	SDATA[12]#	A83
SADDOUT[3]#	B18	SDATA[13]#	B94
SADDOUT[4]#	A27	SDATA[14]#	B95
SADDOUT[5]#	B13	SDATA[15]#	A79
SADDOUT[6]#	B14	SDATA[16]#	B78
SADDOUT[7]#	B4	SDATA[17]#	B76
SADDOUT[8]#	B11	SDATA[18]#	B73
SADDOUT[9]#	B10	SDATA[19]#	B70
SADDOUT[10]#	A23	SDATA[20]#	B68
SADDOUT[11]#	A25	SDATA[21]#	B66
SADDOUT[12]#	B8	SDATA[22]#	B62
SADDOUT[13]#	B3	SDATA[23]#	B64
SADDOUT[14]#	B1	SDATA[24]#	A77
SADDOUTCLK#	B6	SDATA[25]#	A75
SCHECK[0]#	B83	SDATA[26]#	A72
SCHECK[1]#	A85	SDATA[27]#	A73
SCHECK[2]#	B71	SDATA[28]#	A70
SDATA[29]#	A69	SDATA[63]#	B26
SDATA[30]#	A61	SDATAINCLK[0]#	B88
SDATA[31]#	A63	SDATAINCLK[1]#	A67
SDATA[32]#	A57	SDATAINCLK[2]#	B50
SDATA[33]#	A55	SDATAINCLK[3]#	B28
SDATA[34]#	A53	SDATAINVAL#	A101
SDATA[35]#	A49	SDATAOUTCLK[0]#	A91
SDATA[36]#	A43	SDATAOUTCLK[1]#	B60
SDATA[37]#	A47	SDATAOUTCLK[2]#	A59
SDATA[38]#	B45	SDATAOUTCLK[3]#	B20
SDATA[39]#	B40	SDATAOUTVAL#	A99
SDATA[40]#	B58	SFILLVAL#	B118
SDATA[41]#	B57	SMI#	A9
SDATA[42]#	B55	STPCLK#	A18
SDATA[43]#	B54	SYSCLK	A109
SDATA[44]#	B48	SYSCLK#	A108
SDATA[45]#	B47	VCC2SEL	A1
SDATA[46]#	A45	VCC_CORE[1]	A24
SDATA[47]#	B44	VCC_CORE[2]	A82
SDATA[48]#	A41	VCC_CORE[3]	A52
SDATA[49]#	B25	VCC_CORE[4]	A38

Table 18. AMD Athlon™ Processor Signals Ordered by Pin Name (continued)

Pin Name	Pin No.	Pin Name	Pin No.
SDATA[50]#	A37	VCC_CORE[5]	A86
SDATA[51]#	A39	VCC_CORE[6]	A98
SDATA[52]#	A33	VCC_CORE[7]	A58
SDATA[53]#	B23	VCC_CORE[9]	A71
SDATA[54]#	A31	VCC_CORE[10]	A30
SDATA[55]#	A29	VCC_CORE[11]	A32
SDATA[56]#	B42	VCC_CORE[12]	A104
SDATA[57]#	B38	VCC_CORE[13]	A76
SDATA[58]#	B37	VCC_CORE[14]	A64
SDATA[59]#	B35	VCC_CORE[15]	A62
SDATA[60]#	B32	VCC_CORE[16]	A44
SDATA[61]#	A35	VCC_CORE[17]	A110
SDATA[62]#	B30	VCC_CORE[18]	A60
VCC_CORE[19]	A26	VCC_CORE[38]	A46
VCC_CORE[20]	A48	VCC_CORE[39]	A88
VCC_CORE[21]	A92	VCC_CORE[40]	A94
VCC_CORE[22]	A90	VCC_CORE[41]	A22
VCC_CORE[23]	A84	VCC_CORE[42]	A74
VCC_CORE[24]	A80	VCC_CORE[43]	A107
VCC_CORE[25]	A36	VCC_CORE[44]	A28
VCC_CORE[26]	A40	VCC_SRAM[1]	A16
VCC_CORE[27]	A78	VCC_SRAM[2]	A14
VCC_CORE[28]	A100	VCC_SRAM[3]	A10
VCC_CORE[29]	A56	VCC_SRAM[4]	A8
VCC_CORE[30]	A50	VCC_SRAM[5]	A6
VCC_CORE[31]	A54	VCC_SRAM[6]	A4
VCC_CORE[32]	A68	VCC_SRAM[7]	A2
VCC_CORE[33]	A66	VCC_SRAM[8]	A20
VCC_CORE[34]	A42	VID[0]	A112
VCC_CORE[35]	A34	VID[1]	A113
VCC_CORE[36]	A102	VID[2]	A114
VCC_CORE[37]	A96	VID[3]	A115

Table 19. AMD Athlon™ Processor Signals Ordered by Physical Location

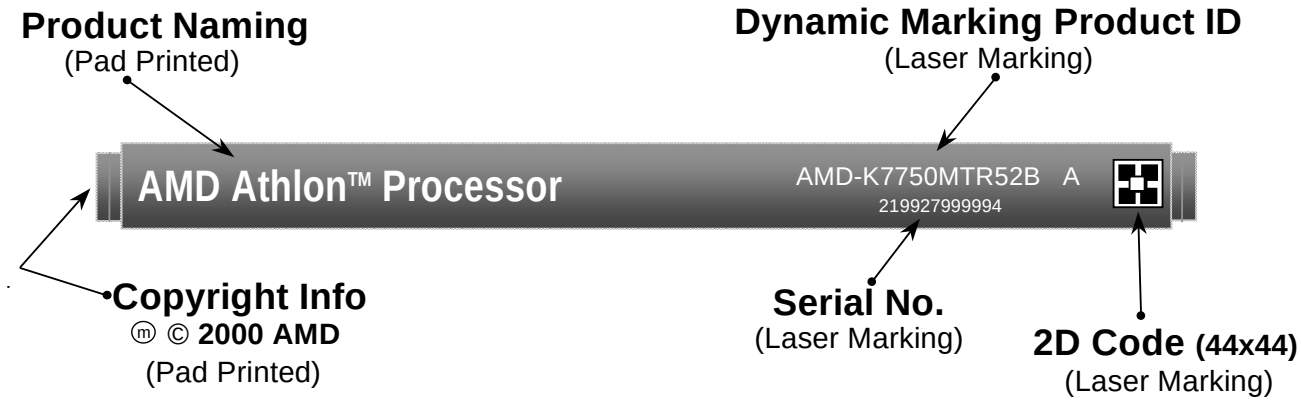
Pin No.	Pin Name—High	Pin Name—Low	Pin No.	Pin No.	Pin Name—High	Pin Name—Low	Pin No.
A121	COREFB–	COREFB+	A120	B121	GND[24]	SADDIN[12]#	B120
A119	FID[0]	FID[1]	A118	B119	GND[47]	SFILLVAL#	B118
A117	FID[2]	FID[3]	A116	B117	GND[12]	SADDIN[14]#	B116
A115	VID[3]	VID[2]	A114	B115	GND[11]	SADDINCLK#	B114
A113	VID[1]	VID[0]	A112	B113	GND[42]	SADDIN[13]#	B112
A111	PWROK	VCC_CORE[17]	A110	B111	GND[43]	SADDIN[9]#	B110
A109	SYSCLK	SYSCLK#	A108	B109	SADDIN[10]#	GND[46]	B108
A107	VCC_CORE[43]	PROCRDY	A106	B107	SADDIN[4]#	SADDIN[3]#	B106
A105	CLKFWDRST	VCC_CORE[12]	A104	B105	GND[48]	SADDIN[2]#	B104
A103	CONNECT	VCC_CORE[36]	A102	B103	GND[45]	SADDIN[11]#	B102
A101	SDATAINVAL#	VCC_CORE[28]	A100	B101	GND[18]	SADDIN[5]#	B100
A99	SDATAOUTVAL#	VCC_CORE[6]	A98	B99	GND[17]	SDATA[9]#	B98
A97	SADDIN[8]#	VCC_CORE[37]	A96	B97	SDATA[11]#	GND[4]	B96
A95	SADDIN[6]#	VCC_CORE[40]	A94	B95	SDATA[14]#	SDATA[13]#	B94
A93	SADDIN[7]#	VCC_CORE[21]	A92	B93	GND[5]	SDATA[0]#	B92
A91	SDATAOUTCLK[0]#	VCC_CORE[22]	A90	B91	GND[6]	SDATA[3]#	B90
A89	SDATA[10]#	VCC_CORE[39]	A88	B89	GND[26]	SDATAINCLK[0]#	B88
A87	SDATA[8]#	VCC_CORE[5]	A86	B87	GND[25]	SDATA[2]#	B86
A85	SCHECK[1]#	VCC_CORE[23]	A84	B85	GND[29]	SDATA[4]#	B84
A83	SDATA[12]#	VCC_CORE[2]	A82	B83	SCHECK[0]#	GND[28]	B82
A81	SDATA[1]#	VCC_CORE[24]	A80	B81	SDATA[5]#	SDATA[6]#	B80
A79	SDATA[15]#	VCC_CORE[27]	A78	B79	GND[27]	SDATA[16]#	B78
A77	SDATA[24]#	VCC_CORE[13]	A76	B77	GND[15]	SDATA[17]#	B76
A75	SDATA[25]#	VCC_CORE[42]	A74	B75	GND[23]	SDATA[7]#	B74
A73	SDATA[27]#	SDATA[26]#	A72	B73	SDATA[18]#	GND[9]	B72
A71	VCC_CORE[9]	SDATA[28]#	A70	B71	SCHECK[2]#	SDATA[19]#	B70
A69	SDATA[29]#	VCC_CORE[32]	A68	B69	GND[14]	SDATA[20]#	B68
A67	SDATAINCLK[1]#	VCC_CORE[33]	A66	B67	GND[49]	SDATA[21]#	B66
A65	SCHECK[3]#	VCC_CORE[14]	A64	B65	GND[36]	SDATA[23]#	B64
A63	SDATA[31]#	VCC_CORE[15]	A62	B63	GND[35]	SDATA[22]#	B62
A61	SDATA[30]#	VCC_CORE[18]	A60	B61	GND[31]	SDATAOUTCLK[1]#	B60
A59	SDATAOUTCLK[2]#	VCC_CORE[7]	A58	B59	GND[50]	SDATA[40]#	B58
A57	SDATA[32]#	VCC_CORE[29]	A56	B57	SDATA[41]#	GND[22]	B56
A55	SDATA[33]#	VCC_CORE[31]	A54	B55	SDATA[42]#	SDATA[43]#	B54
A53	SDATA[34]#	VCC_CORE[3]	A52	B53	GND[33]	SCHECK[5]#	B52
A51	SCHECK[4]#	VCC_CORE[30]	A50	B51	GND[34]	SDATAINCLK[2]#	B50
A49	SDATA[35]#	VCC_CORE[20]	A48	B49	GND[37]	SDATA[44]#	B48
A47	SDATA[37]#	VCC_CORE[38]	A46	B47	SDATA[45]#	GND[41]	B46
A45	SDATA[46]#	VCC_CORE[16]	A44	B45	SDATA[38]#	SDATA[47]#	B44
A43	SDATA[36]#	VCC_CORE[34]	A42	B43	GND[38]	SDATA[56]#	B42
A41	SDATA[48]#	VCC_CORE[26]	A40	B41	GND[39]	SDATA[39]#	B40
A39	SDATA[51]#	VCC_CORE[4]	A38	B39	GND[16]	SDATA[57]#	B38
A37	SDATA[50]#	VCC_CORE[25]	A36	B37	SDATA[58]#	GND[2]	B36
A35	SDATA[61]#	VCC_CORE[35]	A34	B35	SDATA[59]#	SCHECK[7]#	B34
A33	SDATA[52]#	VCC_CORE[11]	A32	B33	GND[13]	SDATA[60]#	B32
A31	SDATA[54]#	VCC_CORE[10]	A30	B31	GND[1]	SDATA[62]#	B30
A29	SDATA[55]#	VCC_CORE[44]	A28	B29	GND[3]	SDATAINCLK[3]#	B28
A27	SADDOUT[4]#	VCC_CORE[19]	A26	B27	GND[32]	SDATA[63]#	B26
A25	SADDOUT[11]#	VCC_CORE[1]	A24	B25	SDATA[49]#	GND[8]	B24
A23	SADDOUT[10]#	VCC_CORE[41]	A22	B23	SDATA[53]#	SCHECK[6]#	B22
A21	A20M#	VCC_SRAM[8]	A20	B21	GND[40]	SDATAOUTCLK[3]#	B20
A19	IGNNE#	STPCLK#	A18	B19	GND[19]	SADDOUT[3]#	B18
A17	RESET#	VCC_SRAM[1]	A16	B17	GND[44]	SADDOUT[2]#	B16
A15	INTR	VCC_SRAM[2]	A14	B15	GND[30]	SADDOUT[6]#	B14
A13	NMI	INIT#	A12	B13	SADDOUT[5]#	GND[20]	B12
A11	FERR#	VCC_SRAM[3]	A10	B11	SADDOUT[8]#	SADDOUT[9]#	B10
A9	SMI#	VCC_SRAM[4]	A8	B9	GND[21]	SADDOUT[12]#	B8
A7	PICD[1] (Not present on Model 1)	VCC_SRAM[5]	A6	B7	GND[7]	SADDOUTCLK#	B6
A5	PICD[0] (Not present on Model 1)	VCC_SRAM[6]	A4	B5	GND[51]	SADDOUT[7]#	B4
A3	PICCLK (Not present on Model 1)	VCC_SRAM[7]	A2	B3	SADDOUT[13]#	GND[10]	B2
A1	VCC2SEL			B1	SADDOUT[14]#		

8 Ordering Information

Standard AMD Athlon™ Processor Products

AMD standard products are available in several operating ranges. The ordering part numbers (OPN) for Model 1 are shown in Table 21 on page 55. The OPNs for Model 2 are shown in Table 20 on page 55. These OPNs are formed by a combination of the elements shown in Figure 15.

The OPNs for Model 4 are shown in Table 22 on page 56. These OPNs are formed by a combination of the elements shown in Figure 16 on page 54.



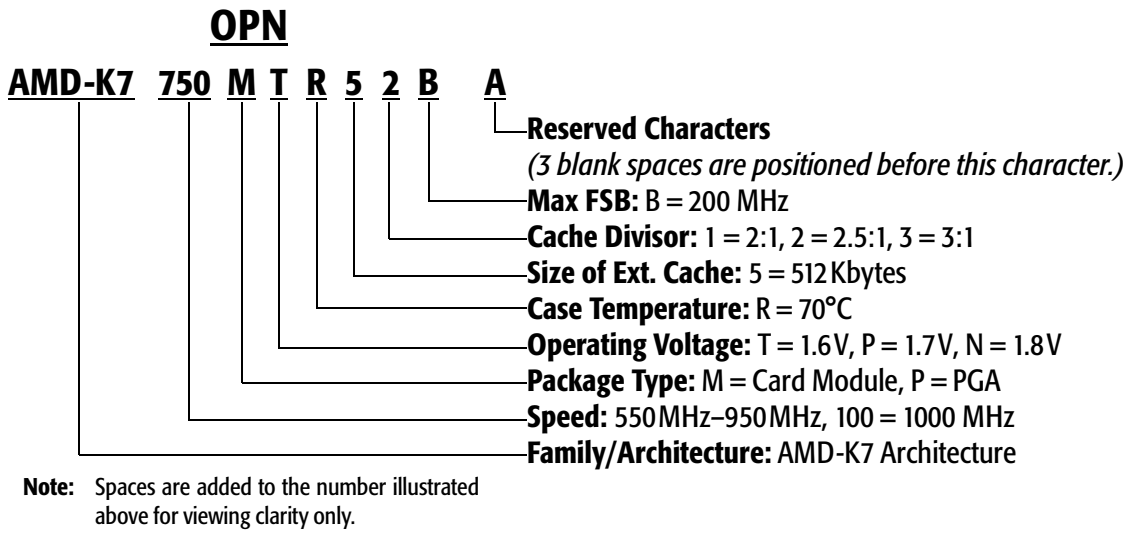


Figure 15. OPN Example for the AMD Athlon™ Processor Model 2

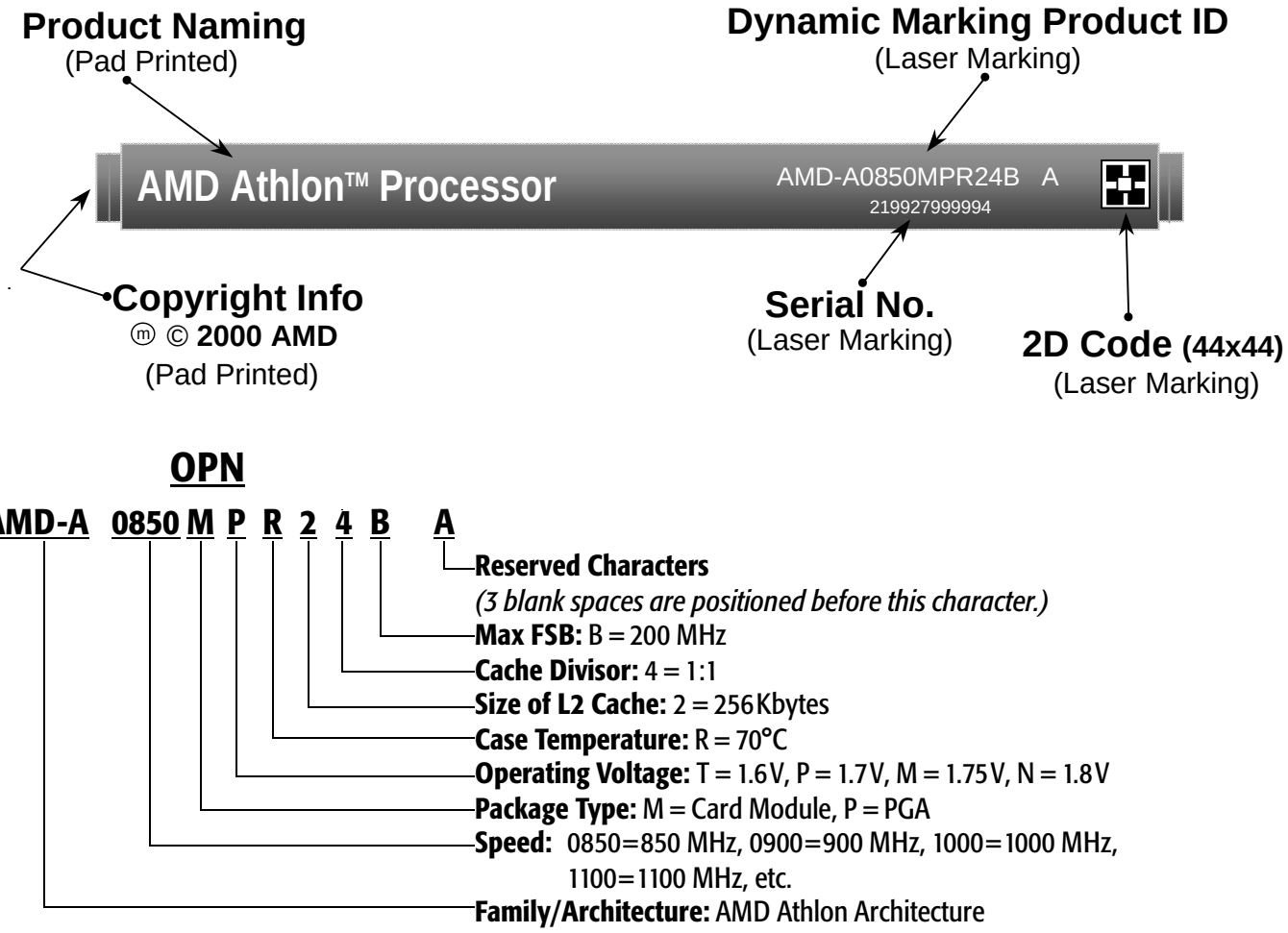


Figure 16. OPN Example for the AMD Athlon™ Processor Model 4

Table 20. Valid Ordering Part Number Combinations for Model 1

OPN	Package Type	Operating Voltage	Plate Temperature
AMD-K7500MTR51B C	Card Module	1.6 V	0°C–70°C
AMD-K7550MTR51B C	Card Module	1.6 V	0°C–70°C
AMD-K7600MTR51B C	Card Module	1.6 V	0°C–70°C
AMD-K7650MTR51B C	Card Module	1.6 V	0°C–70°C
AMD-K7700MTR51B C	Card Module	1.6 V	0°C–70°C

Notes:

This table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly-released combinations.

Table 21. Valid Ordering Part Number Combinations for Model 2

OPN	Package Type	Operating Voltage	Plate Temperature
AMD-K7550MTR51B A	Card Module	1.6 V	0°C–70°C
AMD-K7600MTR51B A	Card Module	1.6 V	0°C–70°C
AMD-K7650MTR51B A	Card Module	1.6 V	0°C–70°C
AMD-K7700MTR51B A	Card Module	1.6 V	0°C–70°C
AMD-K7750MTR52B A	Card Module	1.6 V	0°C–70°C
AMD-K7800MPR52B A	Card Module	1.7 V	0°C–70°C
AMD-K7850MPR52B A	Card Module	1.7 V	0°C–70°C
AMD-K7900MNR53B A	Card Module	1.8 V	0°C–70°C
AMD-K7950MNR53B A	Card Module	1.8 V	0°C–70°C
AMD-K7100MNR53B A	Card Module	1.8 V	0°C–70°C

Notes:

This table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly-released combinations.

Table 22. Valid Ordering Part Number Combinations for Model 4

OPN	Package Type	Operating Voltage	Plate Temperature
AMD-A0650MPR24B A	Card Module	1.7 V	0°C–70°C
AMD-A0700MPR24B A	Card Module	1.7 V	0°C–70°C
AMD-A0750MPR24B A	Card Module	1.7 V	0°C–70°C
AMD-A0800MPR24B A	Card Module	1.7 V	0°C–70°C
AMD-A0850MPR24B A	Card Module	1.7 V	0°C–70°C
AMD-A0900MMR24B A	Card Module	1.75 V	0°C–70°C
AMD-A0950MMR24B A	Card Module	1.75 V	0°C–70°C
AMD-A1000MMR24B A	Card Module	1.75 V	0°C–70°C

Notes:

This table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly-released combinations.

Appendix A

Conventions, Abbreviations, and References

This section contains information about the conventions and abbreviations used in this document and a list of related publications.

Signals and Bits

- Active-Low Signals—Signal names containing a pound sign, such as SFILL#, indicate active-Low signals. They are asserted in their Low-voltage state and negated in their High-voltage state. When used in this context, High and Low are written with an initial upper case letter.
- Signal Ranges—In a range of signals, the highest and lowest signal numbers are contained in brackets and separated by a colon (for example, D[63:0]).
- Reserved Bits and Signals—Signals or bus bits marked *reserved* must be driven inactive or left unconnected, as indicated in the signal descriptions. These bits and signals are reserved by AMD for future implementations. When software reads registers with reserved bits, the reserved bits must be masked. When software writes such registers, it must first read the register and change only the non-reserved bits before writing back to the register.
- Three-State—In timing diagrams, signal ranges that are high impedance are shown as a straight horizontal line half-way between the high and low levels.

- Invalid and Don't-Care—In timing diagrams, signal ranges that are invalid or don't-care are filled with a screen pattern.

Data Terminology

The following list defines data terminology:

- Quantities
  - A *word* is two bytes (16 bits)
  - A *doubleword* is four bytes (32 bits)
  - A *quadword* is eight bytes (64 bits)
  - An AMD Athlon™ processor cache line is eight quadwords (64 bytes)
- Addressing—Memory is addressed as a series of bytes on eight-byte (64-bit) boundaries in which each byte can be separately enabled.
- Abbreviations—The following notation is used for bits and bytes:
  - Kilo (K, as in 4-Kbyte page)
  - Mega (M, as in 4 Mbits/sec)
  - Giga (G, as in 4 Gbytes of memory space)

  See Table 24 for more abbreviations.
- Little-Endian Convention—The byte with the address xx...xx00 is in the least-significant byte position (little end). In byte diagrams, bit positions are numbered from right to left—the little end is on the right and the big end is on the left. Data structure diagrams in memory show low addresses at the bottom and high addresses at the top. When data items are aligned, bit notation on a 64-bit data bus maps directly to bit notation in 64-bit-wide memory. Because byte addresses increase from right to left, strings appear in reverse order when illustrated.
- Bit Ranges—In text, bit ranges are shown with a dash (for example, bits 9–1). When accompanied by a signal or bus name, the highest and lowest bit numbers are contained in brackets and separated by a colon (for example, AD[31:0]).
- Bit Values—Bits can either be set to 1 or cleared to 0.

- Hexadecimal and Binary Numbers—Unless the context makes interpretation clear, hexadecimal numbers are followed by an h and binary numbers are followed by a b.

Abbreviations and Acronyms

Table 24 contains the definitions of abbreviations used in this document.

Table 23. Abbreviations

Abbreviation	Meaning
A	Ampere
F	Farad
G	Giga-
Gbit	Gigabit
Gbyte	Gigabyte
H	Henry
h	Hexadecimal
K	Kilo-
Kbyte	Kilobyte
M	Mega-
Mbit	Megabit
Mbyte	Megabyte
MHz	Megahertz
m	Milli-
ms	Millisecond
mW	Milliwatt
µ	Micro-
µA	Microampere
µF	Microfarad
µH	Microhenry
µs	Microsecond
µV	Microvolt
n	nano-
nA	nanoampere
nF	nanofarad
nH	nanohenry
ns	nanosecond

Table 23. Abbreviations (continued)

Abbreviation	Meaning
ohm	Ohm
p	pico-
pA	picoampere
pF	picofarad
pH	picohenry
ps	picosecond
s	Second
V	Volt
W	Watt

Table 24 contains the definitions of acronyms used in this document.

Table 24. Acronyms

Abbreviation	Meaning
ACPI	Advanced Configuration and Power Interface
AGP	Accelerated Graphics Port
APCI	AGP Peripheral Component Interconnect
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
BIOS	Basic Input/Output System
BIST	Built-In Self-Test
BIU	Bus Interface Unit
DDR	Double-Data Rate
DIMM	Dual Inline Memory Module
DMA	Direct Memory Access
DRAM	Direct Random Access Memory
ECC	Error Correcting Code
EIDE	Enhanced Integrated Device Electronics
EISA	Extended Industry Standard Architecture
EPROM	Enhanced Programmable Read Only Memory
EV6	Digital™ Alpha™ Bus
FIFO	First In, First Out
GART	Graphics Address Remapping Table

Table 24. Acronyms (continued)

Abbreviation	Meaning
HSTL	High-Speed Transistor Logic
IDE	Integrated Device Electronics
ISA	Industry Standard Architecture
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LAN	Large Area Network
LRU	Least-Recently Used
LVTTL	Low Voltage Transistor Transistor Logic
MSB	Most Significant Bit
MTRR	Memory Type and Range Registers
MUX	Multiplexer
NMI	Non-Maskable Interrupt
OD	Open Drain
PBGA	Plastic Ball Grid Array
PA	Physical Address
PCI	Peripheral Component Interconnect
PDE	Page Directory Entry
PDT	Page Directory Table
PLL	Phase Locked Loop
PMSM	Power Management State Machine
POS	Power-On Suspend
POST	Power-On Self-Test
RAM	Random Access Memory
ROM	Read Only Memory
RXA	Read Acknowledge Queue
SDI	System DRAM Interface
SDRAM	Synchronous Direct Random Access Memory
SIP	Serial Initialization Packet
SMbus	System Management Bus
SPD	Serial Presence Detect
SRAM	Synchronous Random Access Memory
SROM	Serial Read Only Memory
TLB	Translation Lookaside Buffer
TOM	Top of Memory

Table 24. Acronyms (continued)

Abbreviation	Meaning
TTL	Transistor Transistor Logic
VAS	Virtual Address Space
VPA	Virtual Page Address
VGA	Video Graphics Adapter
USB	Universal Serial Bus
ZDB	Zero Delay Buffer

Related Publications

The following books discuss various aspects of computer architecture that may enhance your understanding of AMD products:

AMD Publications

AMD Athlon™ Processor Technical Brief, order# 22054

AMD Athlon™ Processor Voltage Regulation Application Note, order# 22651

AMD Athlon™ Processor Thermal Application Note, order# 22439

AMD-751™ System Controller Data Sheet, order# 21910

AMD-756™ Peripheral Bus Controller Data Sheet, order# 22548

AMD Processor Recognition Application Note, order# 20734

AMD Athlon™ Processor Module Signal and Power-Up Requirements Application Note, order#23811

AMD Thermal, Mechanical, and Chassis Cooling Design Guide, order# 23794

Websites

Visit the AMD website for documentation of AMD products.

www.amd.com

Other websites of interest include the following:

- JEDEC home page—www.jedec.org
- IEEE home page—www.computer.org
- AGP Forum—www.agpforum.org