# TR-20 COMPUTER OPERATOR'S REFERENCE HANDBOOK

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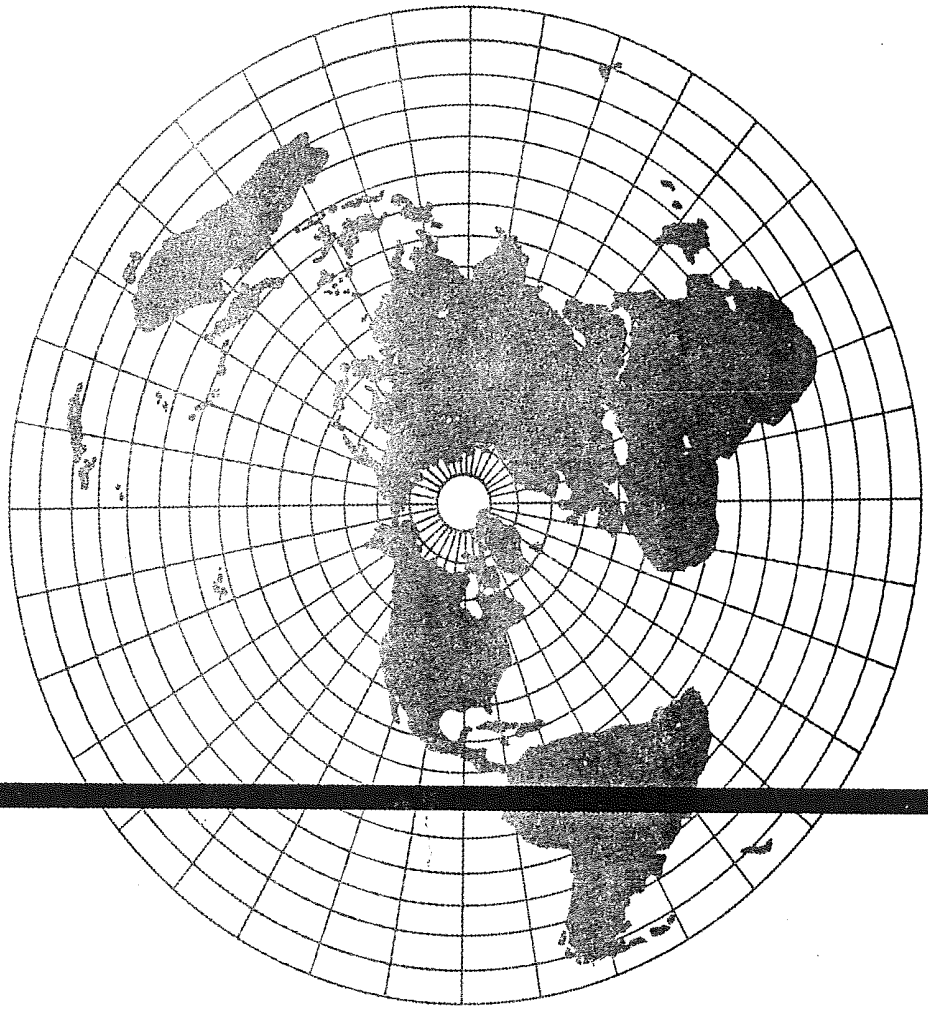

EAI

ELECTRONIC ASSOCIATES INC. ■ LONG BRANCH, NEW JERSEY

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ELECTRONIC ASSOCIATES, INC. *Long Branch, New Jersey*

# TR-20 COMPUTER OPERATOR'S REFERENCE HANDBOOK

Publ. No. D800 2003 0A

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September 1964

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# CHAPTER I

## INTRODUCTION

Many problems encountered in scientific or engineering work involve mathematical equations or sets of equations whose solution in most cases is difficult or practically impossible to obtain by the classical approach to equation solution. The TR-20 Analog Computer provides the technical worker with a general purpose computer which permits the rapid solution of linear or non-linear equations.

Although the analog machine is correctly termed a computer, it does not perform its computations by serial calculations as does the desk calculator or digital computer. Instead it performs the required mathematical operations in a parallel manner on continuous variables. In the TR-20, as in most modern analog computers, the continuous variables are direct current voltages. The electronic analog computer makes it possible to build an electrical model of a physical system, where the voltages on the computer represent the dependent variables of the physical system. Except for a constant of proportionality, or scale factor, each voltage will behave with time in a manner similar to the physical system variable. Thus, if the vertical position of the center of gravity of an automobile oscillates with time during a disturbance, then the voltage representing the height of the center of gravity above the surface will also oscillate; if the temperature of the coolant at the exhaust port of a condenser rises exponentially to a steady value, then so will the voltage representing it on the computer.

It can be said that the actual system and the electrical model are analogous in that the variables which demonstrate their characteristics are described by relations which are mathematically equivalent. The actual system has thus been simulated because of the similarity of operation of the electrical model and the physical system. This capability of the analog computer is of great value in performing scientific research or engineering design calculations because it permits an insight into the relationship between the mathematical equations and the response of the physical system. Once the electrical model is completed, well-controlled experiments can be performed quickly, inexpensively, and with great flexibility to predict the behavior of the primary physical system.

Although the analog computer utilizes electronic components in its operation, it is not essential that the user have an extensive knowledge of electrical circuits. The TR-20 is basically a set of mathematical building blocks, each able to perform specific mathematical operations on direct voltages and capable of being easily interconnected. By appropriately interconnecting these building blocks, an electrical model is produced in which the voltages at the outputs of the blocks obey the relations given in the mathematical description of a physical problem.

Since our interest is frequently in the dynamic behavior of physical systems, the mathematical equations are usually differential equations having time as the independent variable. In order to solve such equations, the standard components of the computer must perform the following operations: inversion, algebraic summation, integration with respect to time, multiplication and division, and function generation.

The sequence of steps for constructing a dynamic model on an analog computer requires first a mathematical description of the physical system, usually in equation form. From this description the operator derives the information necessary to set up a computer program for interconnecting the computing components and determines the required initial conditions and forcing functions. The computing components are interconnected with wires called patch cords. The input and output terminations of the computing components are brought out to a patch bay which is usually fitted with a removable Pre-Patch Panel so that patching may be accomplished away from the computer. The problem is placed on the computer by inserting the patch panel and adjusting the problem parameters to the value of the first case to be investigated. Selected voltages are applied to various components in the form of inputs or initial conditions. These voltages are derived from a precise reference voltage.

Once the computing elements have been patched, adjusted, and energized, the computer is switched into the operate mode. The voltages on the computer change with time in accordance with the equations that govern the physical system variables. The behavior of the computer model is viewed through an output device such as an X-Y plotter, oscilloscope, strip-chart recorder, or digital voltmeter.

This TR-20 Reference Handbook has been prepared to serve as a working guide to the analog programmer or computer operator. The information contained presupposes a knowledge of the analog computer, its basic principles of operation, and programming procedures. (Instructional information in these areas can be obtained from "Basics of Analog Computer Programming" by the EAI Education and Training Group.) Readers interested in more detailed circuit information are referred to the TR-20 Maintenance Manual.

# CHAPTER II

## THE TR-20 COMPUTER AND COMPUTING COMPONENTS

### 1. GENERAL DESCRIPTION

The PACE® TR-20 (Figure 1) is a general purpose analog computer composed of solid-state computing components. The TR-20 is compact in size and is able to operate with stability and precision in a normal office or classroom environment. Reliable, with simplicity in functional design, the TR-20 is easy to use and can be a powerful aid to the individual engineer in the rapid solution of scientific and engineering problems.

Table I lists the currently available computing components and accessories for the TR-20. The TR-20 utilizes a building block concept, in which individual computing components may be easily interconnected to solve the required equations by forming electronic models analogous to the system under study. Each building block, either individually or in combination with others, is capable of performing one or more mathematical operations. The computing components in the TR-20 occupy the area above the slanting control panel area. This area is divided into three rows; the top row contains the coefficient attenuators; the middle row houses the integrator networks, comparators, and other non-linear computing components; the bottom row provides space for twenty (10 dual units) operational amplifiers. The computing components are constructed on plug-in chassis, and the front of each computing component consists of a color-coded plastic patching block that contains the input and output terminations for the unit. The computing components are inter-connected by placing patch cords or bottle plugs between the appropriate input and output terminations. Most TR-20's are equipped with a removable pre-patch panel that allows problem patching away from the computer. The pre-patch panel consists of a rigid aluminum frame with individual rows that contain patching blocks identical with the patching blocks that form the front panels of the components. Contact between the pre-patch panel and the computing components is accomplished by means of gold-plated contact springs.

Below the patching area is the monitoring and control panel area which contains controls and components that permit (a) switching the computer on and off, (b) mode control of the computer, and (c) measuring stationary problem voltages. A hinged cover plate directly below the control panel covers the amplifier balancing potentiometers and the variable diode function generators.

### 2. OPERATING CONSIDERATIONS

The TR-20 is completely tested and calibrated at the time of manufacture and is shipped with all components in place. After performing the preliminary check-out procedure outlined in the TR-20 Maintenance Manual, the computer is ready for operation.

It should be noted that the low voltage levels used in the TR-20 eliminate any shock hazard to the operator when patching components with the computer turned on. Current-limiting circuits protect the reference supplies from damage during short-term overloading if they are inadvertantly patched to ground or to each other. A patching connection that is dangerous to a component usually triggers the overload alarm system.

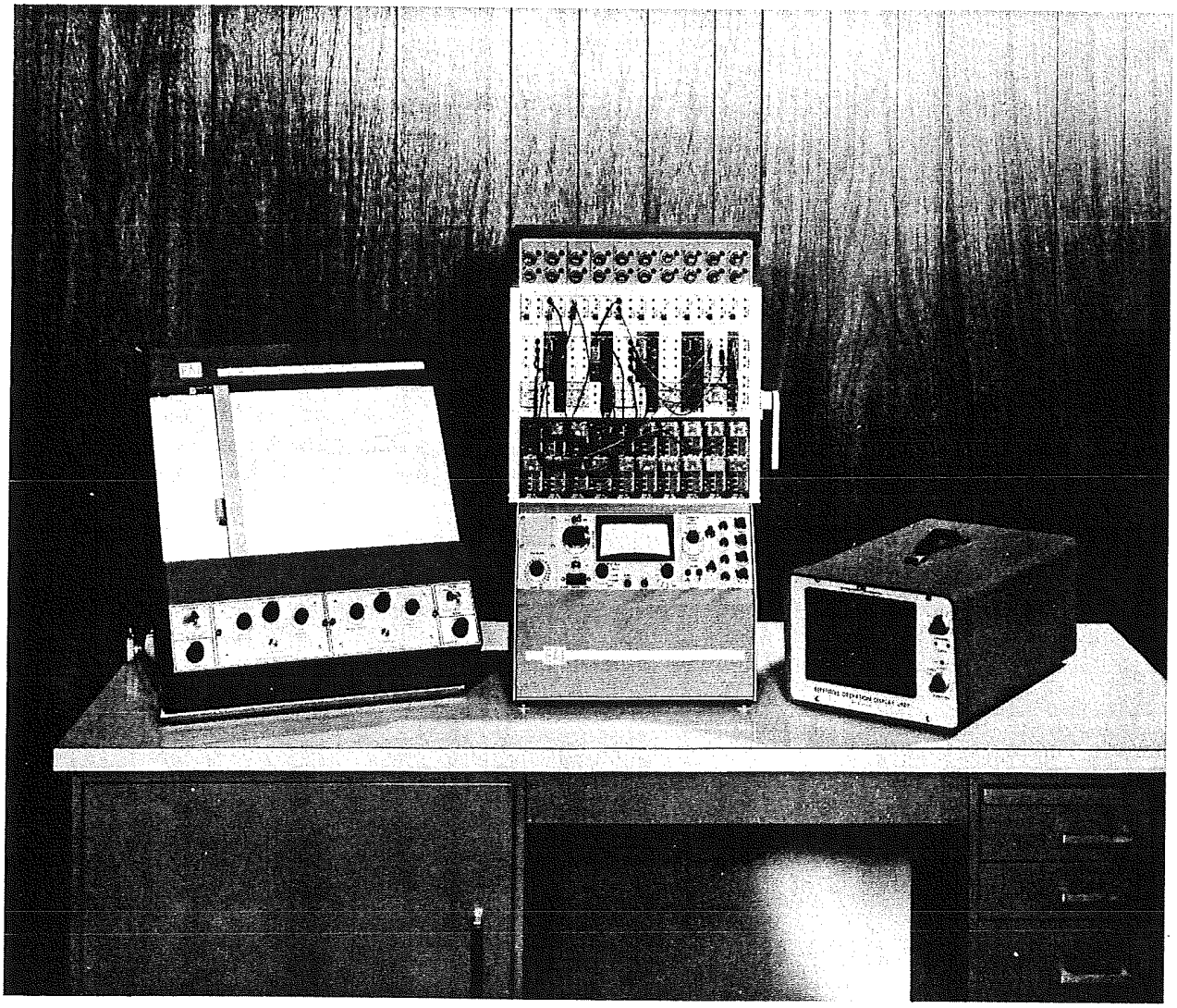


*Figure 1. The TR-20 Desktop Analog Computer with Display Units*

TABLE I. TR-20 COMPONENTS

| GROUP | COMPONENT | MODEL NUMBER |
|---|---|---|
| | COMPUTING COMPONENTS | |
| 1 | Dual DC Amplifier | 6.712 |
| 2a | Dual Integrator Network (Non Rep-Op) | 12.1116 |
| 2b | Dual Repetitive Operation Integrator Network | 12.1115 |
| 3a | Quarter-Square Multiplier | 7.045 |
| 3b | Bi-Polar Quarter-Square Multiplier | 7.117* |
| 4a | $X^2$ Diode Function Generator | 16.101 |
| 4b | Log X Diode Function Generator | 16.126 |
| 4c | 1/2 Log X Diode Function Generator | 16.133 |
| 4d | Sine/Cosine Function Generator | 16.313/1016.004* |
| 5a | Variable Diode Function Generator Group Consists of: | 2.713 |
| | -Variable Diode Function Generator | 16.154-1 |
| | +Variable Diode Function Generator | 16.156-1 |
| | VDFG Readout Module | 16.310 |
| 5b | Variable Diode Function Generator Group Consists of: | 2.645-0 |
| | +Variable Diode Function Generator | 16.304-1 |
| | -Variable Diode Function Generator | 16.306-1 |
| | VDFG Readout Module | 16.308 |
| 5c | Variable Diode Function Generator Group Consists of: | 2.748 |
| | $\pm$Variable Diode Function Generator | 16.165-1 |
| | VDFG Readout Module | 16.310 |
| 6a | Attenuator Group | 42.183 |
| 6b | Attenuator Group | 42.187 |
| 6c | Attenuator Group | 42.188 |
| 6d | Attenuator Group | 2.128 |

| GROUP | COMPONENT | MODEL NUMBER |
|---|---|---|
| | COMPUTING COMPONENTS (Cont) | |
| | Consists of: | |
| | Attenuator Panel | 42.185 |
| | Readout Module | 12.265 |
| 7a | Reference Network | 12.266 |
| 7b | Tiepoint Network | 12.267 |
| 7c | Dual Function Switch Group | 2.127 |
| | Consists of: | |
| | Function Switch Assembly | 20.366 |
| | Readout Module | 12.264 |
| 8a | Relay Comparator | 6.143 |
| 8b | Electronic Comparator | 40.538 |
| | POWER AND REFERENCE SUPPLIES | |
| 9 | Regulated Power Supply | 10.179 |
| 10 | Reference Regulator | 43.037 |
| 11 | Dual DC Amplifier | 6.282 |
| | OPTIONAL COMPONENTS AND ACCESSORY EQUIPMENT | |
| 12 | Repetitive Operation Expansion Group<br>Consists of: | 2.715 |
| | High Speed Repetitive Operation Control Panel | 20.532 |
| | Repetitive Operation Timing Unit | 36.082 |
| | Dual Repetitive Operation Integrator Networks | 12.1115 |

| GROUP | COMPONENT | MODEL NUMBER |
|---|---|---|
| | OPTIONAL COMPONENTS AND ACCESSORY EQUIPMENT | |
| 13 | Display Unit** | 12.987 |
| 14 | Reactor Kinetics Group | 2.475* |
| 15 | Transport Delay Simulator | 2.448* |
| 16 | Audio Overload Alarm | 13.017 |
| 17 | Slave Cable | 510.038 |
| 18 | Patching Kit | 100.007 |
| 19 | Service Shelf | 51.039 |
| 20 | AC Power Cable | 51.040 |
| 21 | Pre-Patch Panel | 5.235 |
| 22 | Rep-Op Slave Panel | 20.567 |
| | AUXILIARY EQUIPMENT | |
| 1 | VARIPLOTTER® | 1110* |
| 2 | Repetitive Operation Display Unit | 34.035* |

The operator should be familiar with the following paragraphs before attempting to use the computer.

*These Components described in separate manuals.

**This Component not required if the Electronic Comparator, Model 40.538 is provided.

a. Insertion of the Pre-Patch Panel

Before inserting the pre-patch panel, the operator should verify that the patch blocks on the pre-patch panel are aligned in the same order as the computing components. Hold the pre-patch panel at a slight angle and place it in the patch bay groove; see Figure 2. Move the pre-patch panel to the right until it contacts the right-hand side of the patch bay. Gently, push the pre-patch panel forward until it is flush with the computer. Turn the locking lever down; the pre-patch panel will slide to the left.

To remove the pre-patch panel, apply a light pressure to the panel to keep it from falling forward when dis-engaged, and lift the locking lever.

b. Feedback for the Amplifiers

All operational amplifiers should be provided with feedback whenever the computer is turned on. Bottle plugs, connected as shown in Figure 3a, provide feedback and prepare the amplifiers for use as standard inverters or summers.

c. Application of Power

Connect the computer line cord to a receptacle following the precautions given in the TR-20 Maintenance Manual, and place the OFF-ON switch to the ON position. Place the RESET-HOLD-OPER switch to the RESET position. Initially, the amplifier overload alarm system will be triggered due to transients; after a few seconds, the overload indication should cease.

d. Amplifier Balance

Under normal circumstances, the amplifiers will remain balanced for periods of weeks. However, at intervals it is desirable to check this condition. If an amplifier is found to be unbalanced, an adjustment should be made. If the check indicates that the amplifier balance is within tolerance, no adjustment is necessary.

The amplifier must have some sort of feedback in order to be balanced. Normally, this requirement is satisfied by the circuit in which the amplifier is used. The amplifier may be balanced while normal inputs are applied. Each amplifier has a balance potentiometer located behind a hinged cover plate below the Control Panel (Figure 4). The balance controls are labeled with the number of the amplifier they serve. To set a balance control, proceed as follows:

(1) Place the computer in the reset mode. Place the Voltmeter Function switch in the BAL position. Rotate the AMPL SEL switch to the number of the amplifier to be balanced.

(2) Vary the appropriate Amplifier Balance control until the Voltmeter reads within two or three divisions of zero. (The amplifier overload alarm system may be triggered during the balancing process.)

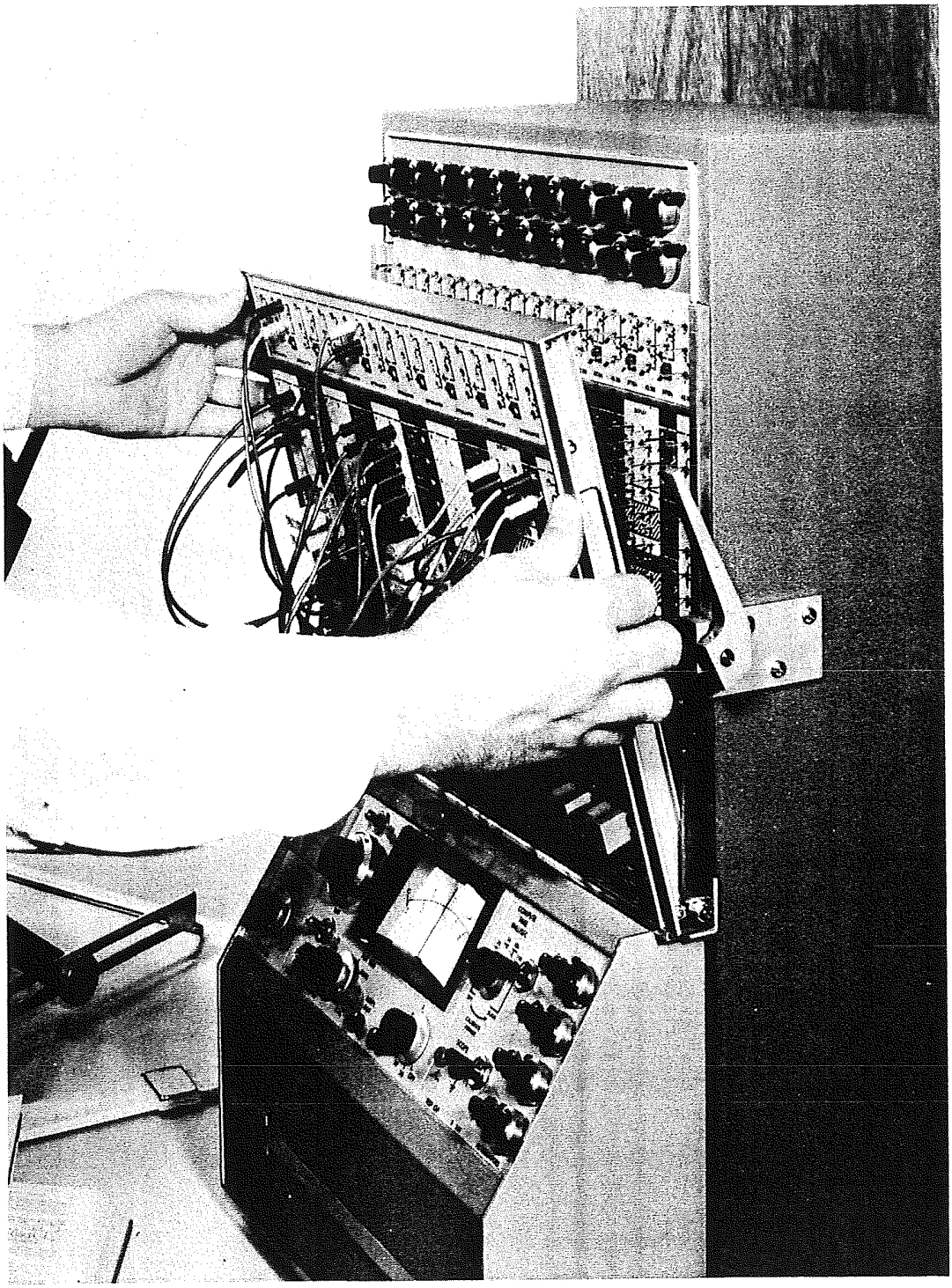
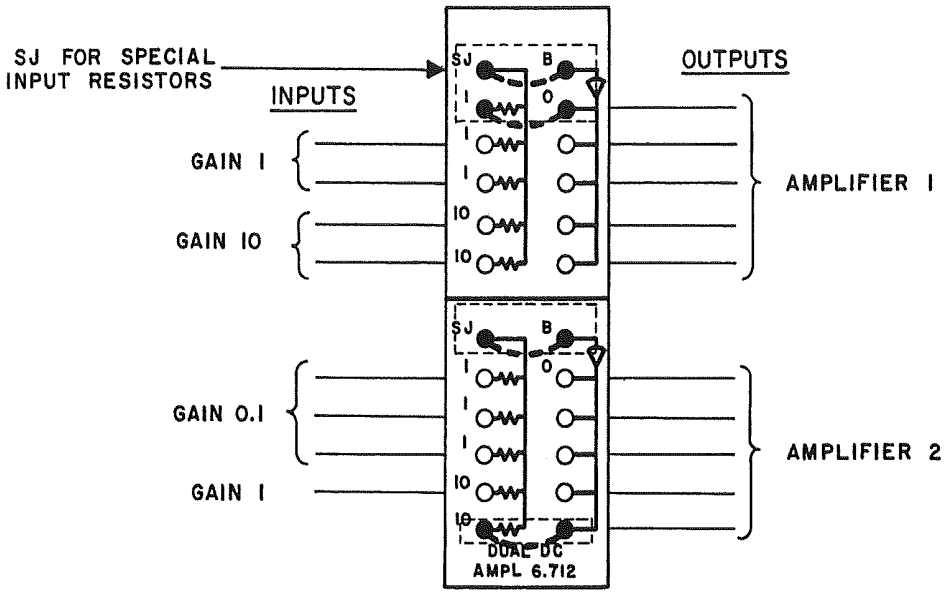
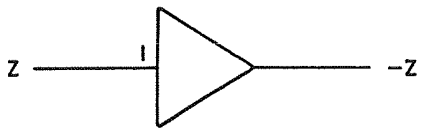


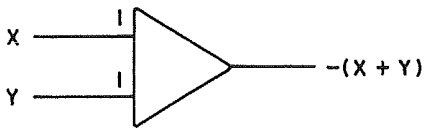
*Figure 2. Inserting the Pre-Patch Panel*



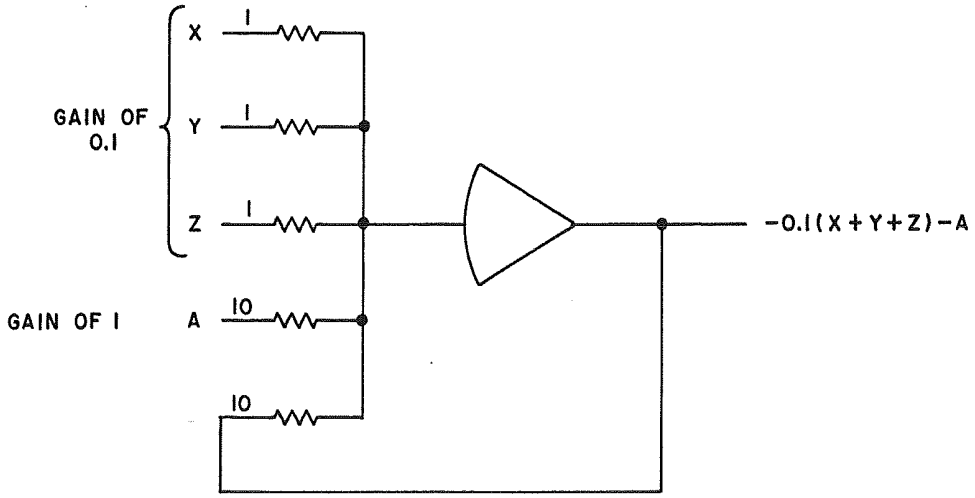

a. PATCHING WITH BOTTLE PLUGS




b. AN INVERTER




c. A SUMMER




d. A HIGH-GAIN AMPLIFIER PATCHED FOR GAINS OF 0.1 AND 1

*Figure 3. The 6.712 Dual DC Amplifier, Showing Use of Bottle Plugs*

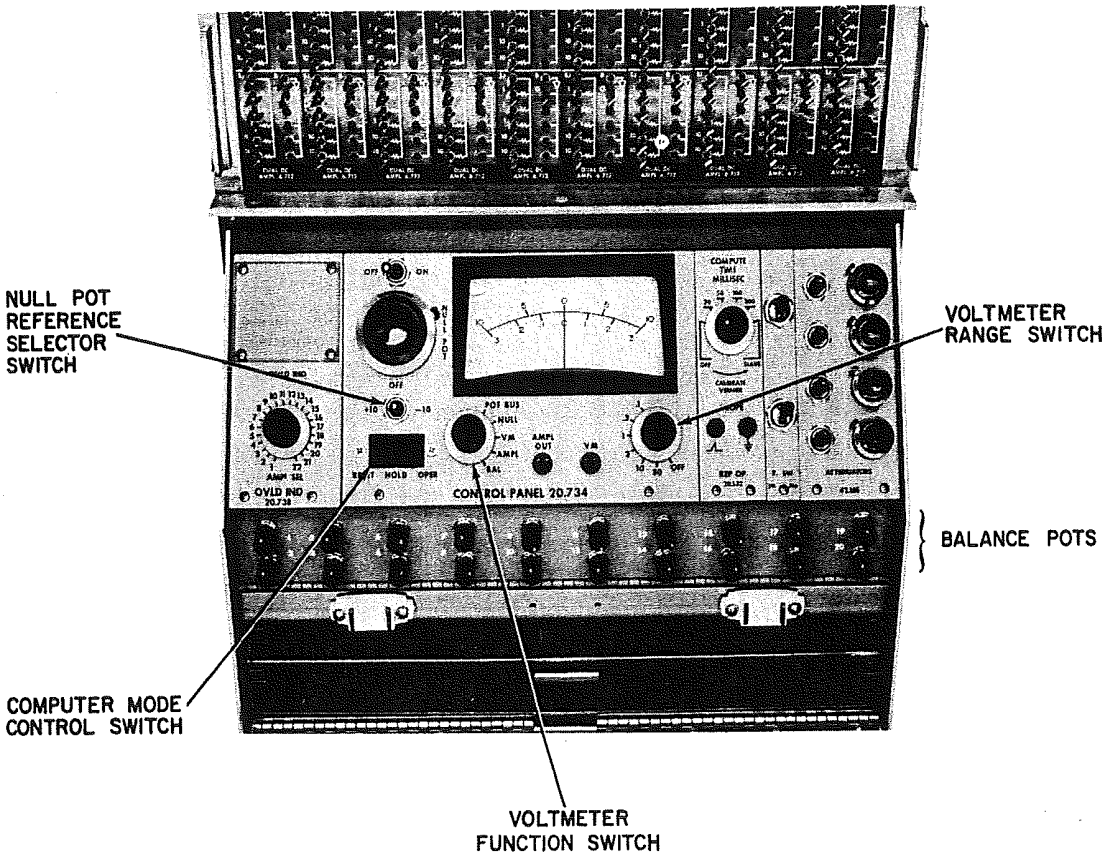



*Figure 4. The TR-20 Control Panel*

When the computer is first turned on, a check of amplifier balance will show deflections that are slightly high, but they will return to normal levels after a warm-up period. For unusual problems that might be especially sensitive to amplifier unbalance or integrator drift, the amplifier can be balanced at more frequent intervals in order to keep the meter deflection below one division.

e. Overloads

The computer is equipped with an overload alarm system that indicates the presence of an overloaded amplifier. The visual overload alarm is located on the left side of the control panel. The lamps are illuminated whenever their associated amplifier is overloaded. Lamps 1 to 20 serve the 20 operational amplifiers; lamps 21 and 22 serve the amplifiers associated with the plus and minus reference amplifiers respectively. The computer may be equipped with an audio overload alarm that is located in the rear of the cabinet; it sounds an audible alarm when an amplifier is overloaded.

The overload alarm system indicates that something is wrong with the problem patching, the problem operation, or the computing components. Usually, no harm is done to the equipment by short-term overloads, unless they are caused by excessively high voltages other than those normally obtainable from the computer itself. However, several other reasons exist for clearing overloads soon after they are noticed.

(1) If an overload is indicated for amplifier 21 or 22, the value of the plus or minus reference voltage may be other than $\pm$10.00 volts, adversely affecting problem solution. An overload in either of these amplifiers generally indicates a patching error, and should not be allowed to continue over an extended period of time.

(2) Overload of unassigned amplifiers does not damage the amplifiers or affect the problem solution. However, the fact that one or more overload lamps are lit, however, may cause the operator to overlook an overload occurring in an assigned amplifier, thus causing an erroneous problem solution and defeating the purpose of the alarm system.

## 3. READOUT FACILITIES AND MANUAL MODE CONTROLS

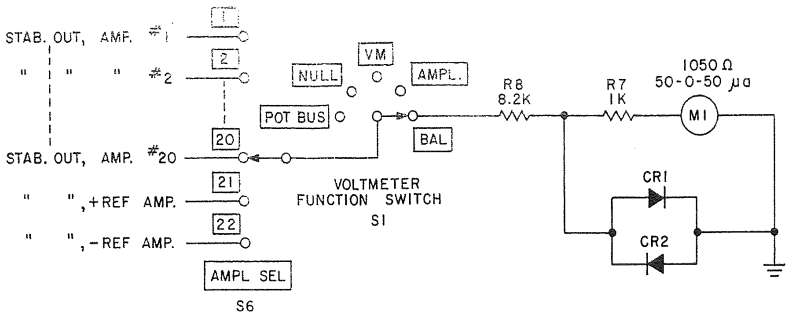
The operating controls for the readout and mode control circuits are grouped on the sloping control panel area below the computing component cradles as shown in Figure 4. The functions of the controls are:

| Control | Function |
|---|---|
| Power ON-OFF Switch, S4 | Controls application of primary ac power to the power supply of the computer. The voltmeter is illuminated when power is applied. |
| Mode Control Switch, S5 | Controls the operational mode of the computer. Positions are RESET, HOLD, and OPERATE. |
| Voltmeter Function Switch, S1 | Controls voltmeter operation. Positions are POT BUS, NULL, VM, AMPL, and BAL. |
| Voltmeter Range Switch, S2 | Selects sensitivity for voltmeter. Full scale ranges of 0.1, 0.3, 1, 3, 10, and 30 volts are provided. |
| NULL POT and Reference Selector Switch, +10/OFF/-10 (S3) | Used in conjunction with the voltmeter to measure voltages by the null comparison method. |
| VM Jack | Provides for external inputs to the voltmeter when the Voltmeter Function Switch is in the NULL or VM position |
| Amplifier Selector Switch, S6 (AMPL SEL) | Selects an amplifier for output monitoring or balancing. |
| AMPL OUT Jack | Connected to the wiper of the AMPL SEL switch; facilitates connecting any amplifier output to external monitoring or measuring equipment. |
| Overload Indicators, OVLD IND | Indicate an overload in the associated amplifier when illuminated. |

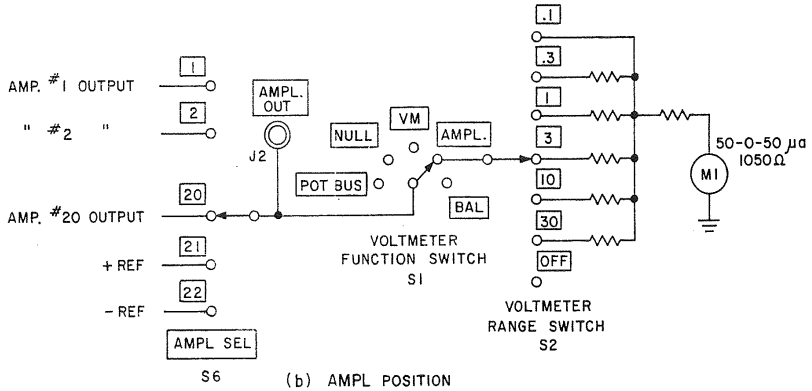
a. Readout Facilities

The readout facilities consist of a sensitive voltmeter, selector switches for connecting the voltmeter to various points in the computer, and a precision ten-turn potentiometer that is used to measure voltages by the null-comparison method. The function of the related controls is described below.

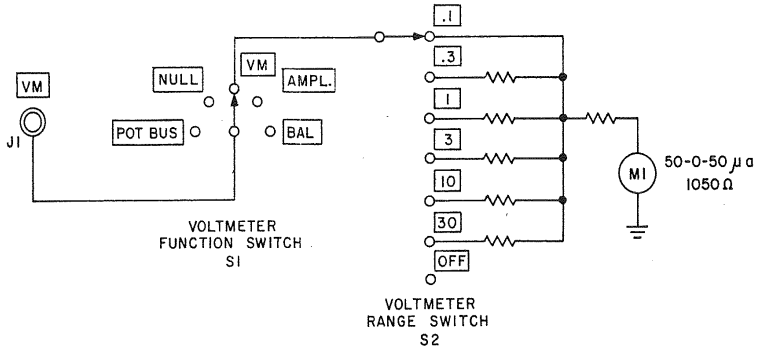
The BAL position of the Voltmeter Function Switch (S1) is used when balancing the dc amplifiers. The AMPL SEL switch (S6) is used to select the stabilizer output of the amplifier to be balanced, (Figure 5a). The balance potentiometer of the amplifier is rotated until the meter reads zero. Positions 1 to 20 of the AMPL SEL switch are connected to the stabilizers of the 20 operational amplifiers; positions 21 and 22 are connected to the stabilizers of the plus and minus reference amplifiers respectively. The diodes in parallel with the meter protect the meter movement.




(a) BAL POSITION

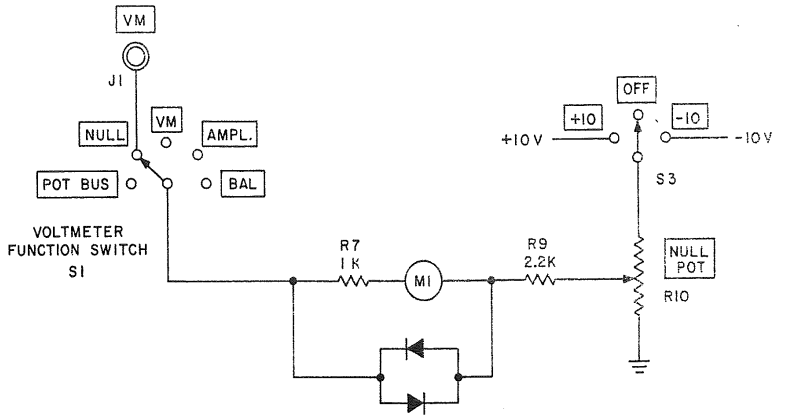



(b) AMPL POSITION

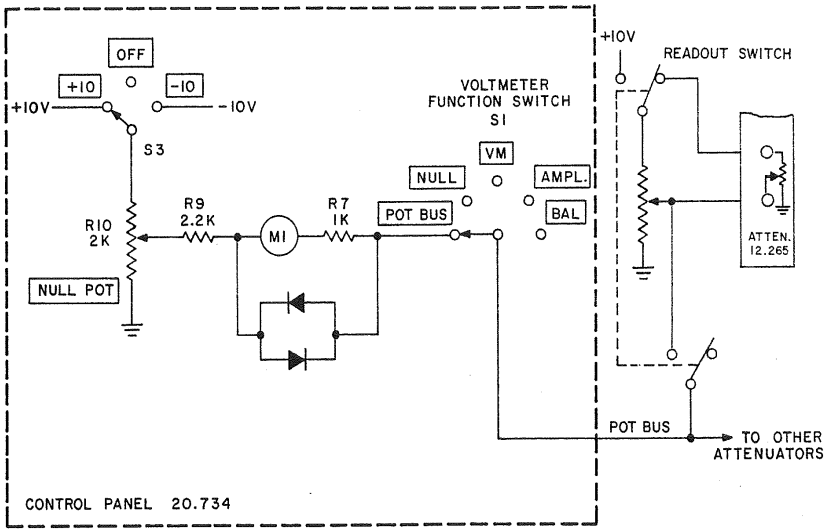



(c) VM POSITION

*Figure 5. Readout Circuits Simplified Schematics*




(d) NULL POSITION




(e) POT BUS POSITION

The AMPL position of the Voltmeter Function switch establishes the circuit shown in Figure 5b where the output of the selected amplifier provides the input to the voltmeter. The Voltmeter Range switch is used to select a convenient full-scale range for the voltmeter. Note that the wiper of the AMPL SEL switch is connected to the AMPL OUT jack so that amplifier outputs can be monitored with external equipment.

The VM position of the Voltmeter Function switch connects the VM jack to the Voltmeter Range switch (Figure 5c). Voltages patched into the VM jack are read on the voltmeter.

The NULL position of S1 provides a means of accurately measuring unknown voltages with respect to the computer reference voltage. The circuit arrangement is shown in Figure 5d. The voltage to be measured is patched to the VM jack and connected to one side of the meter. The wiper of the NULL POT is connected to the other side of the meter. The Reference Selector switch S3 is switched to the position that supplies reference voltage with the same polarity as the voltage to be measured. The NULL POT is varied until the meter reads zero. The position of the turns-counting dial on the NULL POT indicates the magnitude of the unknown voltage; the position of S3 indicates the polarity of the unknown voltage. This null comparison method of voltage measurement provides a measurement accurate to within $\pm$0.1% of full scale. An important feature of the method is that no current is drawn from the source being measured once a balance is attained. Thus the resistance of the source has no effect in the measurement. A large source resistance, however, will decrease the sensitivity of the meter to unbalanced conditions.

The POT BUS position of S1 is used when setting attenuators (Figure 5e). The readout circuit is connected to measure the voltage on the pot bus by the null comparison method. When the pushbutton switch associated with an attenuator is depressed, +10 volts is connected to the top of the attenuator, and the wiper is connected to the pot bus. The Reference Selector switch, S3 must be in the +10 position. The NULL POT is set to the desired attenuator coefficient. The attenuator is adjusted until the meter reads zero. The attenuator is then set to the same coefficient as the NULL POT.

b. Manual Mode Control

The Mode Control switch (S5) on the Control Panel provides a means of starting and stopping computer solutions and of establishing initial conditions. The switch controls the operation of a circuit which actuates the reset and operate relays of the integrators. The switch positions are RESET, HOLD, and OPER (operate). All computing components except the integrators are operational in all three modes. The integrators are controlled as follows:

RESET — In the reset mode, the output voltages of the integrators are set to the values required by initial conditions of the problem. All other inputs to the integrator are disconnected.

HOLD — In the hold mode, the inputs to the integrators are removed; integration ceases and all variables are held at the present values.

OPER — In the operate mode, the integrators accept inputs and integration with respect to time takes place.

4. ATTENUATORS

One of the simplest and most useful operations performed on an analog computer is accomplished by using a potentiometer to multiply a voltage by a positive constant that is less than one. This corresponds to attenuation of the voltage, therefore potentiometers are often called attenuators. Both terms are used interchangeably here. Four types of attenuator groups are available for use in the TR-20, All groups use ten-turn, 5000 ohm potentiometers. The groups are listed below.

| GROUP | NO. OF POTS | TYPE OF POT | DIAL | REMARKS |
|---|---|---|---|---|
| 42.183 | 2 | Carbon | Uncalibrated | Does not have Readout Switches |
| 42.187 | 2 | Carbon | Uncalibrated | Has Readout Switches |
| 42.188 | 2 | Wirewound | Calibrated | Has Readout Switches |
| 2.128 (42.183 & 12.265) | 4 | Wirewound | Calibrated | Has Readout Switches<br>Pots located in Control Panel area |

The Type 42.183, Type 42.187, and Type 42.188 Groups have similar patching terminations. The top potentiometer is terminated on the left side of the patching module and the lower end of this potentiometer is grounded. The lower potentiometer is terminated on the right side of the patching module and both ends of the potentiometer are available for patching. The Type 2.128 Group consists of a patching module (Type 12.265) that mounts in the non-linear row of computing components, and Quad Coefficient Assembly, Type 42.185 that mounts in the control panelarea. The lower end of each potentiometer is grounded. The potentiometers are terminated in order, top to bottom, on the patching module.

When an input voltage $E_{in}$ is applied to an attenuator as shown in Figure 6, the output voltage $E_o$ is K times $E_{in}$, where $K = R_1/R_T$. If the attenuator is unloaded, the mechanical ratio of $R_1 : R_T$ is the same as the electrical ratio $E_o : E_{in}$ and the attenuator could be set to the exact ratio by means of the vernier dial attached to the wiper shaft. Normally, however, the attenuator is loaded and the two ratios are not equal. The most common use of the attenuator is to feed an amplifier; thus the wiper is loaded by the amplifier input resistor. In order to account for loading, it is more convenient to set the attenuator under loaded conditions by monitoring the wiper voltage and adjusting the wiper until the desired output is obtained.

Figure 7a shows the circuit used in the TR-20 to permit setting grounded attenuators under load. A pushbutton switch is located next to each attenuator; depressing the switch connects the wiper to the pot bus, removes the voltage applied at the patch panel, and applies +10 volts to the top of the attenuator. The wiper voltage, on the pot bus, can be measured by the null-comparison method by using the NULL POT on the control panel.

The ungrounded attenuators are connected in the circuit configuration shown in Figure 7b. Depressing the pushbutton switch applies +10 volts to the top of the potentiometer and connects the loaded wiper to the pot bus for measuring purposes. Note that the lower end of the attenuator is not grounded and voltages may be patched to both ends of the attenuator. The patching block has a ground termination near the low end of the ungrounded potentiometer to make it convenient to ground the low end if so desired.

The Type 42.183 Attenuator Group does not include the pushbutton switches. The wiper of each attenuator is brought out to a termination next to the attenuator to facilitate readout under loaded conditions. Figure 7 contains schematics and symbols for two potentiometer types. The address or number of the potentiometer (i.e., 1 or 2) is placed within the circle; the coefficient setting (K) is written near the symbol. The high and/or low end of ungrounded potentiometers is also indicated.

## 5. THE OPERATIONAL AMPLIFIER

### a. General Considerations

When a high-gain dc amplifier is used in conjunction with input and feedback networks to perform mathematical operations, the resulting system is generally referred to as an operational amplifier. The operational amplifier is the basic and most versatile unit in the analog computer. It can be used for inversion, summation, multiplication by a constant, integration, and used in conjunction with special networks for squaring, extracting square root, generating logarithmic functions, etc.

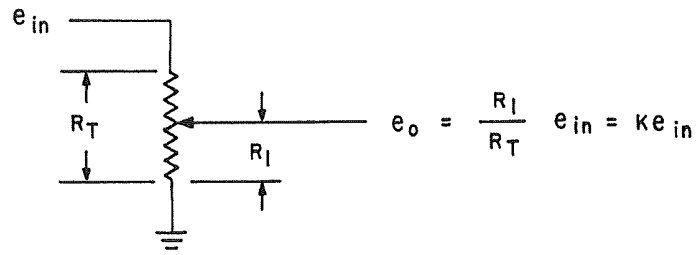
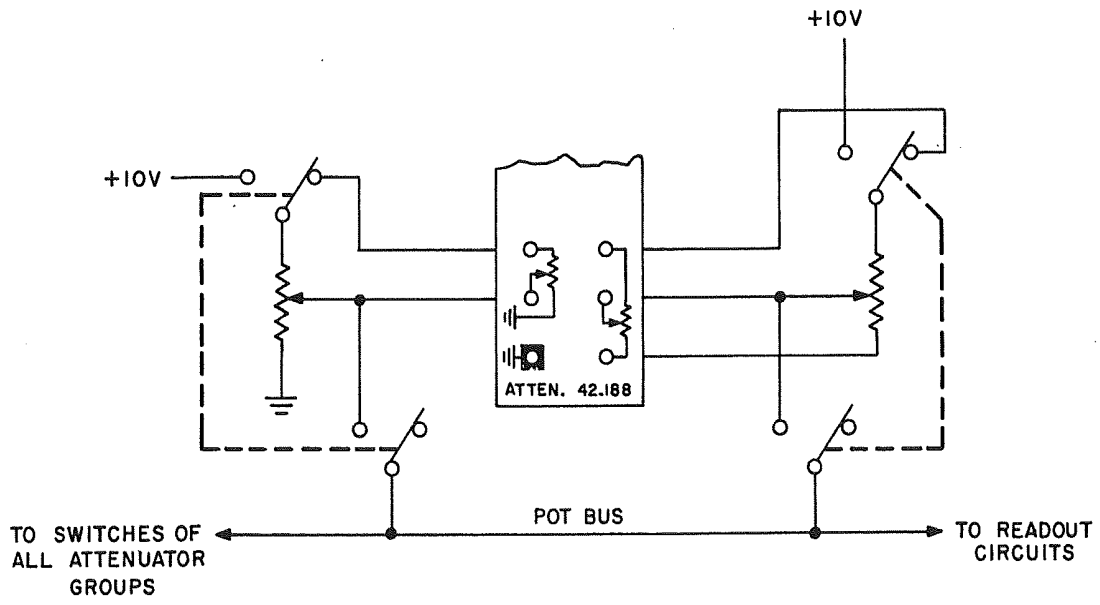
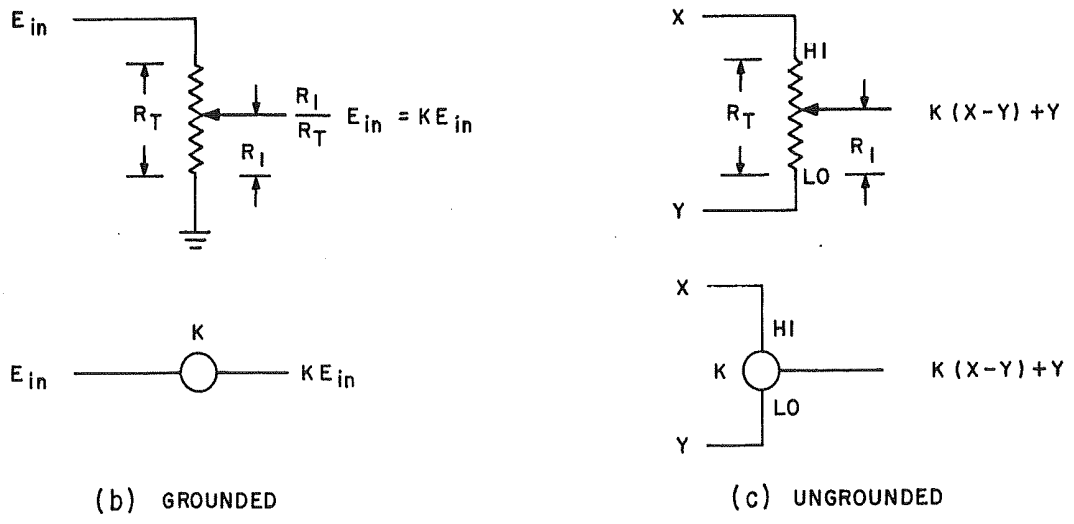



*Figure 6. An Attenuator*




(a) ATTENUATORS, SIMPLIFIED SCHEMATIC




(b) GROUNDED (c) UNGROUNDED

*Figure 7. Schematics and Symbols for Attenuators*

Recall that the amplifier is designed to have three essential characteristics (see Figure 8):

(1) The amplifier output ($e_o$) is related to the summing junction voltage ($e_b$) by the gain of the amplifier: $e_o = -Ae_b$

(2) The input stage of the amplifier draws negligible current: $i_b \approx 0$

(3) The open loop gain of the amplifier is extremely high: $A \gg 1$ (on the order of $3 \times 10^7$ at dc).

Therefore, the amplifier output voltage is related to the input voltage by the equation:

$$e_o = \left(\frac{Zf}{Z_{in}}\right) e_{in} \qquad \text{(EQ. 2-1)}$$

Equation 2-1 illustrates one of the most important characteristics of the operational amplifier: the input-output relationship of the operational amplifier is solely dependent on the ratio of the feedback to the input impedance.

Using Equation 2-1 as the basis of discussion, the following sub-paragraphs describe the various uses of the operational amplifier.

b. Inversion

When the same value resistor is used for both the feedback and the input impedance, the amplifier output voltage has the same amplitude as the input voltage but is opposite in polarity. In the TR-20 the value of $R_f$ and $R_{in}$ used for the inverter is normally 100,000 ohms (100K), therefore:

$$e_o = -\frac{R_f}{R_{in}} e_{in} = -\frac{100K}{100K} e_{in} = -e_{in}$$

Thus a +10 volt input results in a -10 volt output, and the amplifier is said to have a gain of minus one. The accuracy of the output to input ratio depends solely on the accuracy of the ratio $R_f/R_{in}$.

c. Multiplication by a Constant

A change in the ratio of the resistors results in multiplication by a constant. For example, with $R_f$ equal to 100K and $R_{in}$ equal to 10K, the amplifier output is:

$$e_o = -\frac{100K}{10K} e_{in} = -10e_{in}$$

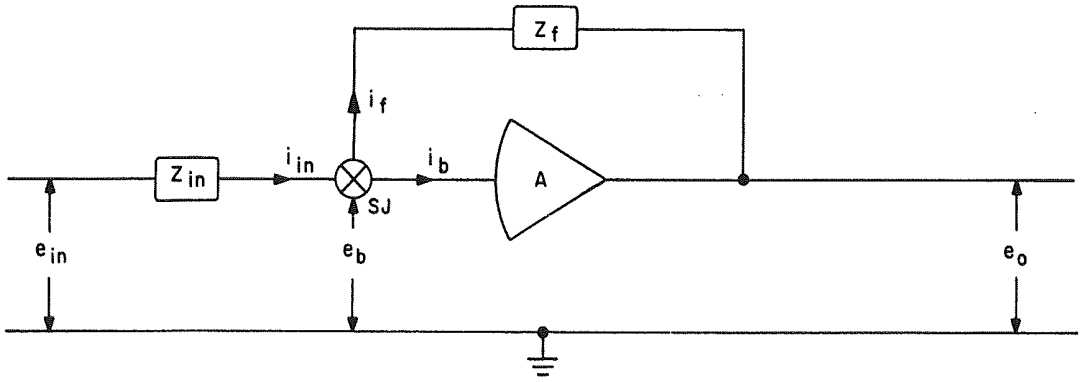



*Figure 8. Operational Amplifier, Simplified Block Diagram*

An input of plus one volt results in an output of minus ten volts. This operational amplifier has a gain of ten. The multiplying constant can be made smaller than one by using a 10K feedback resistor with a 100K input resistor.

$$e_o = -\frac{10K}{100K} e_{in} = -0.1e_{in}$$

An input of minus ten volts produces an output of plus one volt.

d. Summation

When multiple input resistors are used with a feedback resistor $R_f$, the basic relationship is extended to:

$$e_o = -\left(\frac{R_f}{R_1} e_1 + \frac{R_f}{R_2} e_2 + \cdots + \frac{R_f}{R_n} e_n\right)$$

The circuit can be used to algebraically sum an indefinite number of inputs; furthermore, each input may be multiplied by an arbitrary constant.

e. Integration with Respect to Time

When the feedback element $Z_f$ is a capacitor rather than a resistor, the operational amplifier becomes an integrator. If $Z_f$ is a capacitor having an operational impedance 1/pC and $Z_{in}$ is a resistor, the basic operational amplifier relationship, Equation 2-1, becomes:

$$e_o = -\frac{E_{in}}{pRC} = -\frac{1}{RC}\int_o^t e_{in}\, dt$$

An indefinite number of inputs may be applied to produce the time-integral of the sum of the input voltages.

f. Other Mathematical Operations

As previously indicated, the operational amplifier has uses other than those described above. Complicated transfer functions can be simulated by using series and parallel RC networks for the feedback and input impedance. The circuit performance is still governed by the basic relationship of Equation 2-1. For the general case where three-terminal networks are used, the short-circuit transfer impedance of $Z_f$ and $Z_{in}$ must be used. The input and feedback elements need not be linear; therefore, almost any non-linear characteristics can be approximated. The amplifier can also be used in conjunction with diodes and resistors to simulate the non-linear operations of limiting, dead-zone generation, $X^2$, Log X, etc.

g. Patching the Amplifier as a Summer/Inverter

Five precision input/feedback resistors are terminated at the front of each amplifier section of the patch block. Three of these resistors have a value of 100K each, and are designated 1 on the patch block. The two remaining resistors, with a value of 10K each, are connected to terminals designated 10. The other end of each resistor is connected to a common bus, and terminated at a point designated SJ (summing junction) on the patch block. The input of the amplifier is terminated at a point designated B (base), and the output of the amplifier is connectd to five 0 terminals in the red area of the patch block.

To patch an amplifier as a summer or inverter, insert a double (four-prong) bottle plug as shown in the upper amplifier of Figure 3a. A voltage applied to one of the 1 input terminals is multiplied by -1, and the amplifier is referred to as an inverter (Figure 3b). If two inputs (for example x and y) are connected to the 1 inputs as shown in Figure 3c, the output of the amplifier is equal to $-(x + y)$, and the amplifier is acting as a summer.

The lower amplifier of Figure 3a is patched with two prong bottle plugs to provide one gain-of-one input and three gain-of-one-tenth inputs, as shown in Figure 3d.

h. Patching the Amplifier as an Integrator

The amplifier becomes an integrator by providing the proper patching connections to an integrator network. Two types of integrator networks are available for the TR-20. Each network contains the passive elements and control circuits necessary to form two integrators. The Model 12.1116 is supplied with computers that are not equipped for repetitive operation. The Model 12.1115 is supplied as a part of the repetitive operation expansion group (see Section 11 of this chapter). Both networks are similar, and are described here.

(1) Integrator Network 12.1116. Figure 9 is a diagram which illustrates the patching required to convert an amplifier into an integrator. The patching is straight-forward, with the SJ, 0, and B terminals of the amplifier connected to the SJ, 0, and B terminals respectively of an integrator network. Two additional patching connections are required on the 12.1116 Integrator Network, indicated by the heavy lines in the lower cross-hatched area of the integrator patch block (Figure 9). These connections may be easily made by inserting two-prong bottle plugs in this area.

The diagram at the right side of Figure 9 shows the essential components of one half of a dual integrator network. The relays (K1 and K2) are common to both sections of the network, although only one set of contacts is shown for each. Both relays are shown de-energized, as they exist in the hold mode. In this mode, the inputs at the SJ terminal are connected to ground by the contacts of K1. The initial condition voltage is also connected to ground (through a 10K resistor) by the contacts of K2. The capacitor remains connected as the feedback element of the amplifier, between the B and 0 terminals. This allows the capacitor to retain any voltage which may have been applied during the operate or reset modes, and the output of the integrator remains constant.

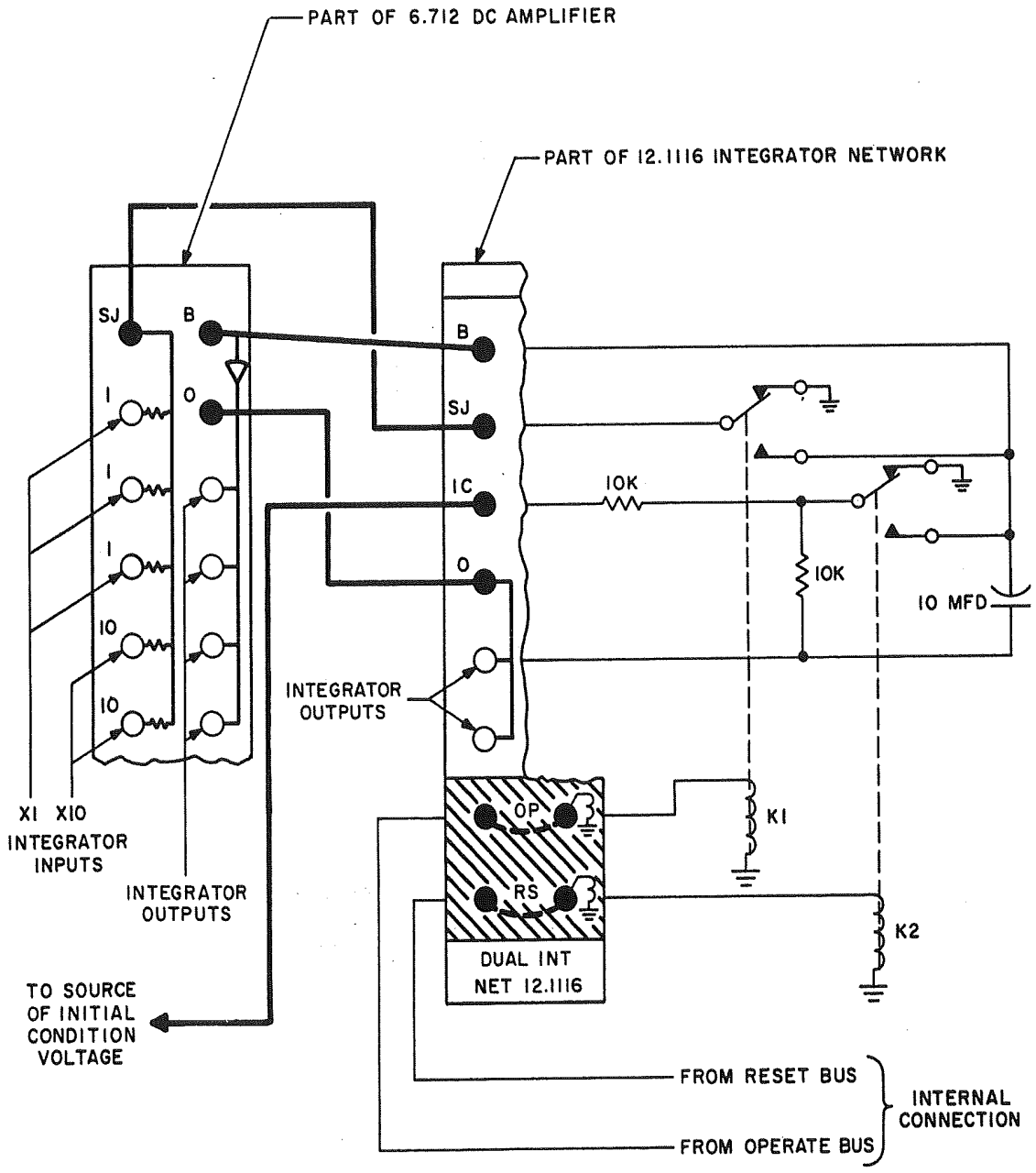



*Figure 9. Patching an Amplifier as an Integrator, Showing Simplified Schematic of an Integrator Network*

When the computer is placed in the reset mode, relay voltage is present on the reset bus. If the indicated patching connection in the RS area is made, K2 is energized, and its contact moves to the alternate position shown. This allows a voltage at the IC terminal to be coupled through a 10K input resistor to the base of the amplifier. The feedback capacitor is now shunted by a 10K resistor. This allows the amplifier to perform as a unity-gain inverter (for the initial condition voltage) with a time lag of approximately 0.5 seconds. For this reason, the computer should always be left in the reset mode for at least one-half second before switching to the hold or operate modes, to assure that the correct initial condition potentials are established.

When the computer is switched to the operate mode, K2 de-energizes and K1 energizes. This applies the input potentials at the SJ terminal of the network to the base of the amplifier. Since K2 is de-energized, the capacitor provides the only feedback path for the amplifier, and integration with respect to time takes place.

The patching connections in the cross-hatched area have been indicated for standard operation. For special situations, these connections may be different. For example, if the RS connection is deleted, the integrator cannot be placed in the reset mode; remaining in hold when the other integrators in the computer are being reset. This allows the value reached during a solution to be used as an initial condition for the next solution. Patching and a brief description of these special situations is provided in the appendix.

(2) Integrator Network 12.1115. This network differs from the network previously described principally by providing two values of feedback capacitor. These values (10 mfd and 0.02 mfd) allow a 500 to 1 change in time scale. Figure 10 illustrates the patching connection and the circuit arrangement of the network. Note that the patching connections to the amplifier are identical to those for a 12.1116 Network. An additional patching connection is required on the integrator network in the cross-hatched area designated SPEC, if the integrator is to be used in the standard rep-op mode.

The Operate and Reset relays (K1 and K2 of Figure 9) have been replaced by a single balanced-armature relay (K3 of Figure 10). This allows the integrator to be switched between operate and reset modes very rapidly, a necessary requirement for repetitive operation. Relay K1 selects the correct value of feedback capacitance for normal or repetitive operation. If the connection in the SPEC area is delected, the integrator has a feedback capacitance of 10 mfd for either mode. This patching is described in the appendix.

Relay K2 grounds the SJ input during the reset and hold modes. The relay is energized during the operate and rep-op modes, through CR1 or CR2 respectively. When K2 is energized, the SJ input is connected to the operate contact of the Repetitive Operation relay (K3). Therefore, when a problem is being set up on a computer equipped with the 12.1115 Networks, the Mode Control switch must be placed in the RESET position and the COMPUTE TIME MILLISEC switch must be placed in the OFF position.

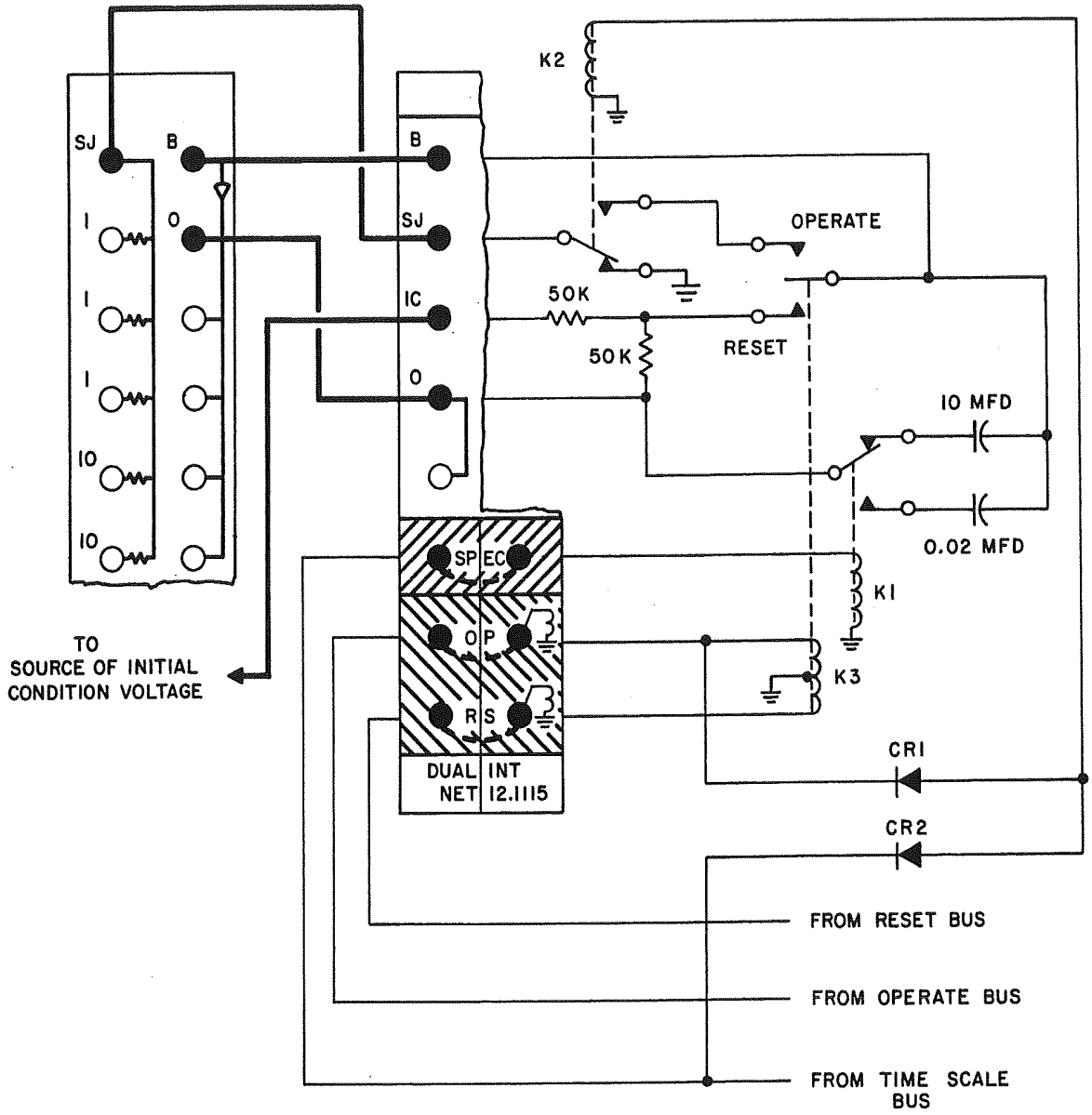



*Figure 10. Patching an Amplifier to a Rep-Op Integrator, Showing Simplified Schematic of Integrator Network*

## 6. QUARTER-SQUARE MULTIPLIER

### a. General Description

The quarter-square multiplier is used in conjunction with a dc amplifier to produce a four quadrant product proportional to XY from inputs of +X, -X, +Y, and -Y. In addition to multiplication, the TR-20 multiplier is capable of performing the mathematical operations of division, squaring, and square root extraction.

The operation of the quarter-square multiplier is based on the identity:

$$XY = \frac{1}{4}\left[ (X + Y)^2 - (X - Y)^2 \right]$$

which reduces multiplication to the operations of summation and squaring. The squaring operations are performed by diode function generators (DFG's) that contain biased diode networks. The diode function generators or squaring cards generate a segmented straight-line approximation to a square law curve. The complete multiplier assembly contains four squaring cards that are connected so as to permit multiplication of input signals of either plus or minus polarities. (Only two of the squaring cards conduct at any one time.) The outputs of the squaring cards are summed in an external amplifier.

Operators who are interested in the circuit details of the quarter-square multiplier are referred to the TR-20 Maintenance Manual.

### b. Multiplication

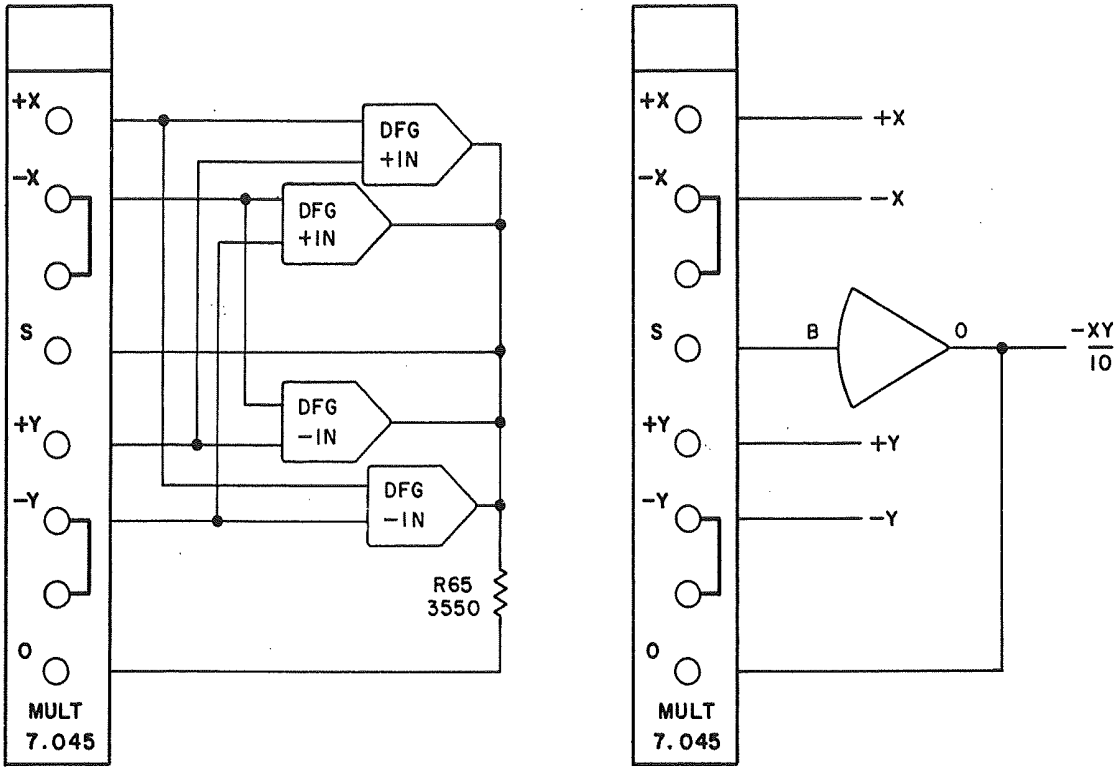
The general configuration of the quarter-square multiplier is shown in Figure 11a. The DFG's contain biased diode networks that produce a current proportional to the square of the sum of the input voltages to the DFG when the sum of the input voltages has the proper polarity. A positive DFG conducts only when the sum of its inputs is positive.

The unit is patched as a multiplier in Figure 11b. The squaring cards (DFG's) form the input network of the amplifier; a 3550 ohm resistor (R65) is the feedback element. The input voltages are patched to the +X, -X, +Y, and -Y terminations. The output voltage from the amplifier is $-\frac{XY}{10}$. The output is changed to $+\frac{XY}{10}$ by reversing the +X and -X inputs or the +Y and -Y inputs. All four input voltages must be patched in. The squaring cards have a variable input impedance, therefore the input voltages should not be obtained from potentiometers. The output amplifier can be used to sum additional inputs; the gain for an additional 10K ohm input resistor is 0.355 since the amplifier has a 3550 ohm feedback resistor.

A programming symbol for the multiplier is shown in Figure 11c.

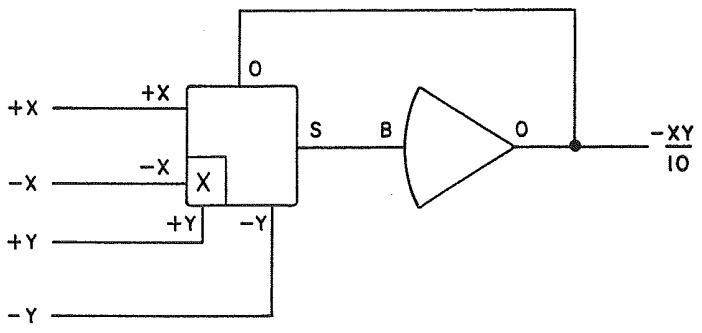
### c. Division

Division of a variable voltage A by a variable voltage B is accomplished by placing




a. SIMPLIFIED DIAGRAM OF UNIT

b. MULTIPLIER PATCHING




c. SYMBOL

*Figure 11. Quarter-Square Multiplier Patching*

the multiplier in the feedback loop of a high-gain amplifier as shown in Figure 12. Assume that the output voltage of amplifier 1 is C; then at the summing junction of amplifier 1, the null relationship

$$\frac{CB}{10} + A = 0$$

is satisfied by automatic changes in the value of C. Therefore:

$$C = -\frac{10A}{B}$$

Note that although the voltage A can have both positive and negative values, the voltage B must always be positive. If B is always negative, then the use of -B in its place (by interchanging the inputs to +Y and -Y) will produce

$$C = +\frac{10A}{B}$$

at the output of amplifier 1.

The following restrictions must be placed on the division circuit:

(a) The absolute value of the divisor B must be greater than or equal to the absolute value of the dividend A to avoid overloads in the output amplifiers.

(b) The divisor B must not change sign. It must not go to zero, for this implies an indeterminate or infinite quotient. The circuit requires that the high-gain amplifier (amplifier 1) be surrounded by negative feedback, and this can only be arranged for one or the other polarity of the voltage B.

Circuits using the quarter-square multiplier are summarized in the appendix.

## 7. $X^2$ DIODE FUNCTION GENERATOR

### a. General Description

The $X^2$ Diode Function Generator is used in conjunction with a dc amplifier to produce an output voltage that is proportional to the square or square root of the input voltage.

The $X^2$ DFG contains two independent sections that generate quadratic curves. One accepts positive input voltages; one accepts negative input voltages. Biased diode networks similar to those in the quarter-square multiplier are used to approximate

the $X^2$ function by a series of straight-line segments. An output voltage proportional to the square root of an input voltage is obtained by placing the $X^2$ DFG in the feedback loop of an amplifier.

b. Generating the Square of an Input Voltage (Single Polarity)

A simplified diagram of the $X^2$ DFG is shown in Figure 13a. The DFG terminated on the upper portion of the patching block accepts only negative inputs; the lower DFG accepts only positive inputs. If the input voltage has the wrong polarity, the DFG output is zero. Resistor $R_f$ (R52) is not associated with either DFG; it can be used wherever required.

A typical use of the unit is illustrated in Figure 13b. The unit is patched to yield two independent squaring circuits. In each case, the DFG is used as the input element of an amplifier that has a 3550 ohm feedback resistor. The voltage X must be negative; the voltage Y must be positive. Since the DFG's have a variable input impedance, the voltages applied to the -IN and +IN terminations should not be obtained from potentiometers. The output amplifiers can be used to sum additional inputs.

A programming symbol for the $X^2$ DFG is shown in Figure 13c.

c. Generating the Square of an Input Voltage (Bi-Polar)

The $X^2$ DFG's are connected as shown in Figure 14 to generate $+\frac{X^2}{10}$ from an input voltage X where $-10 \leq X \leq +10$. When X is negative, the upper DFG conducts and produces an output of $+X^2/10$ from amplifier 1; the lower DFG does not conduct. When X is a positive voltage, the lower DFG conducts and generates $-X^2/10$ at the output of amplifier 2. This output is applied through resistor $R_f$ to the base of amplifier 1. This signal is inverted and appears at the output of amplifier 1 as $+X^2/10$. Thus for an input of either polarity, the output of amplifier 1 is $+X^2/10$.

Circuits using the $X^2$ DFG are summarized in the appendix.

8. LOG X DFG AND 1/2 LOG X DFG

a. General Description

The Log X DFG's are used in conjunction with a dc amplifier to produce an output voltage that is proportional to the logarithm of the input signal voltage. Common base or natural logarithms and antilogarithms can be generated. The output of the DFG's is in the form of straight-line segments that closely approximate a logarithmic curve for a single polarity input voltage. The desired function is produced by summing the outputs of simple limiter circuits that use solid-state diodes as voltage sensitive switches.

The Dual Log X DFG, Model 16.126, consists of two independent logarithmic function generators. One generator accepts a positive input voltage, X, and produces a negative output voltage $Y = -5 \log_{10} 10X$. The other generator accepts a negative input voltage, -X, and produces a positive output voltage $Y = +5 \log_{10} |10X|$.

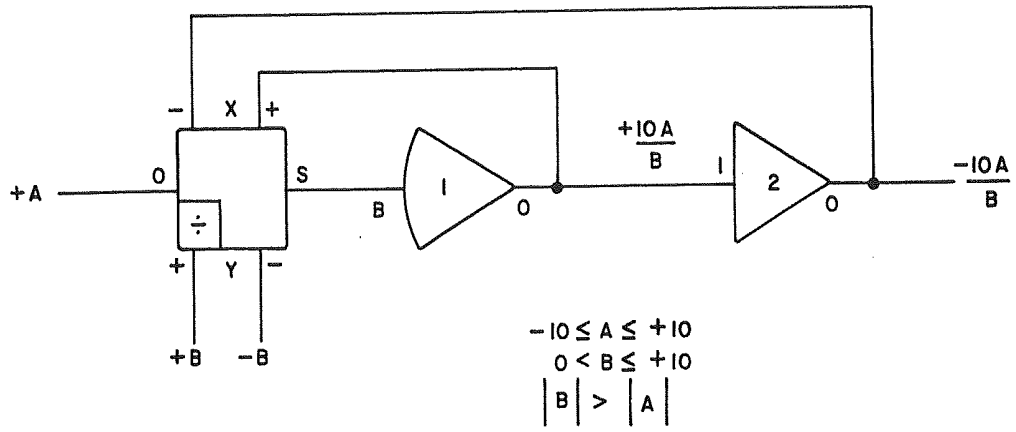



*Figure 12. Division Circuit for a Quarter-Square Multiplier*

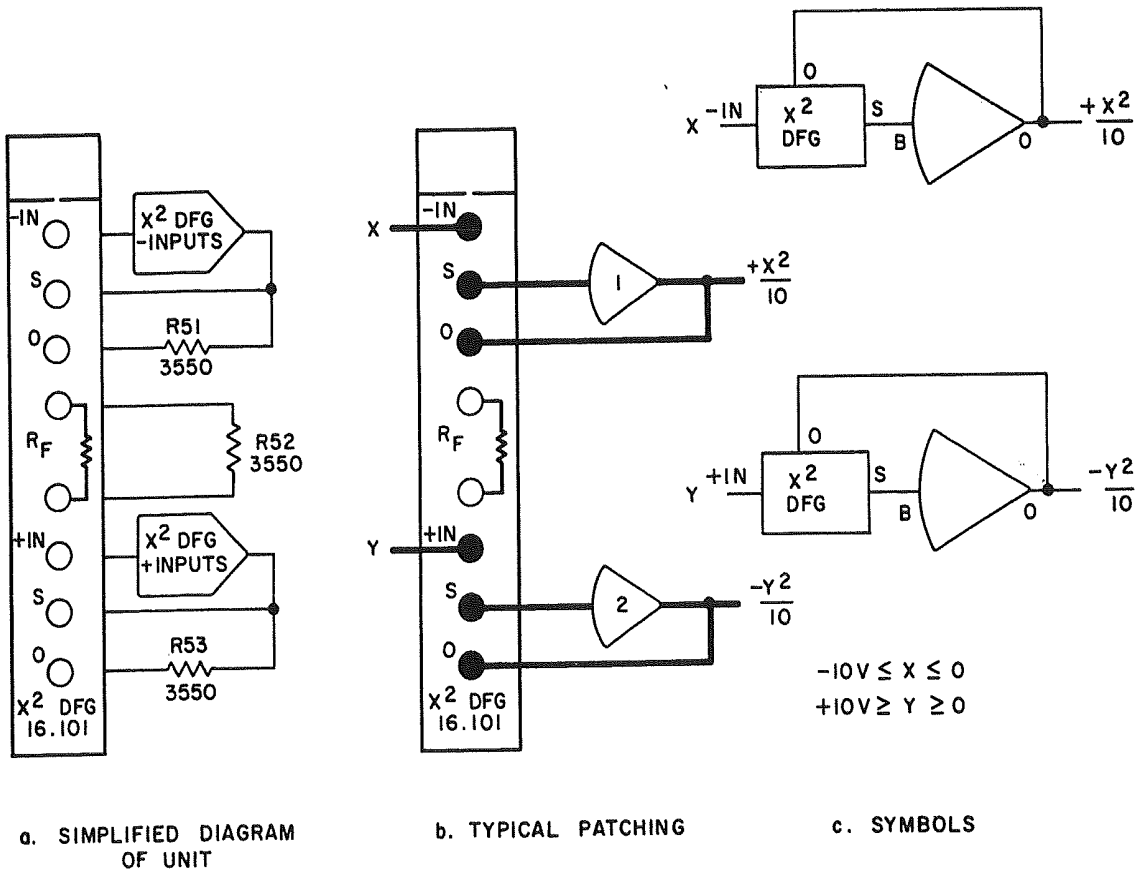



*Figure 13. $X^2$ DFG Patching*

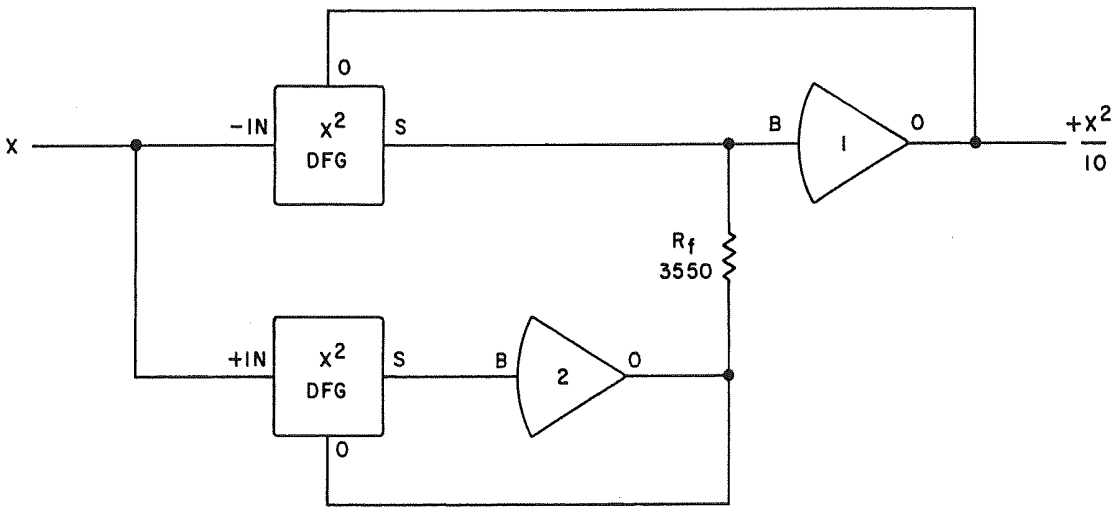



*Figure 14. Generating* $+\frac{X^2}{10}$ *for* $-10 \leq X \leq +10$

b. Patching

A simplified diagram and a typical patching scheme for the Dual Log X DFG and the Dual 1/2 Log X DFG are shown in Figure 15. The Dual Log X DFG is shown in the figure but the information is applicable to both units except for the labeling of the output variable. The DFG terminated on the upper portion of the patching module accepts a negative voltage, -X, and produces a positive voltage of 5 $\log_{10}$ |10X| from the associated amplifier. The lower DFG accepts a positive voltage, Y, and produces a negative voltage of -5 $\log_{10}$ 10Y from its associated amplifier. Each amplifier has a 5000 ohm feedback resistor. The input voltage magnitude should not be less than 0.1 volts in order to maintain accuracy and/or avoid overloads. Care should be taken not to apply an input voltage of the wrong polarity; doing so will not damage the DFG but it does constitute a severe overload on the amplifiers in the circuit.

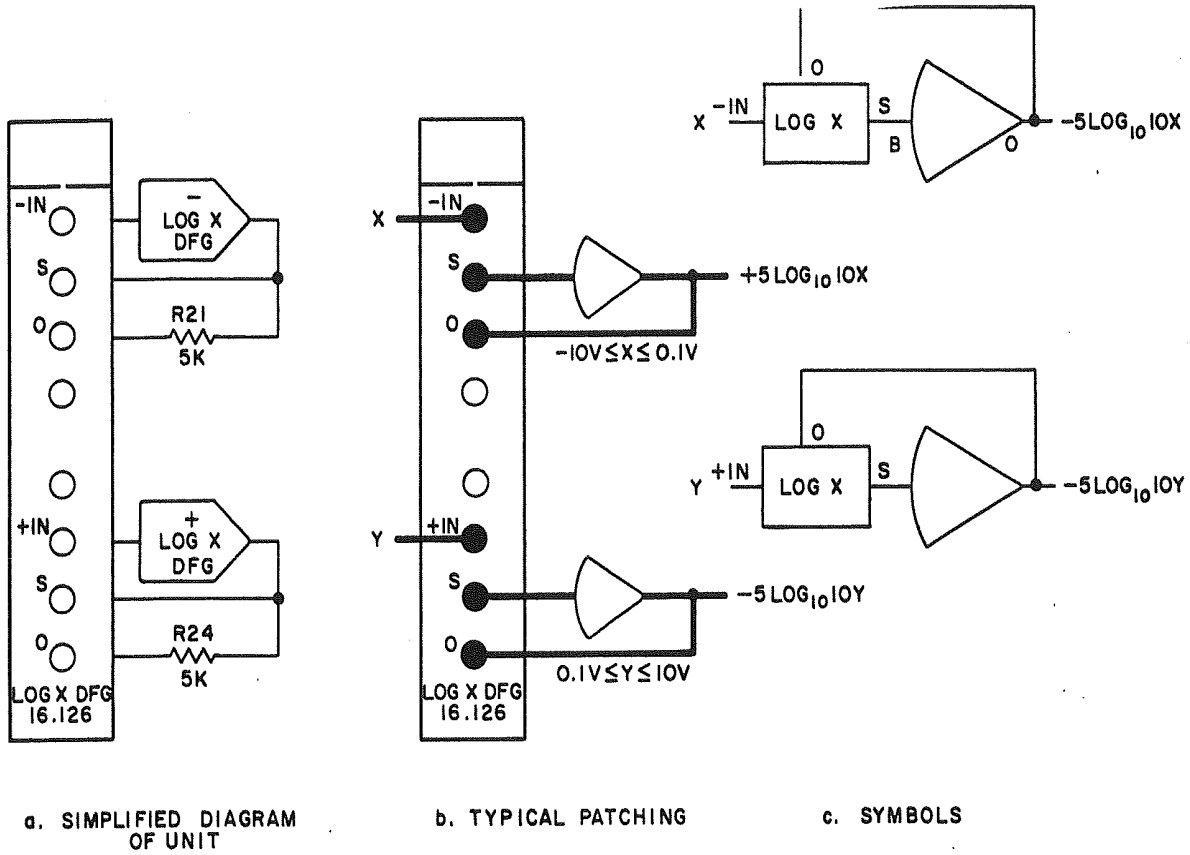



*Figure 15. Patching the Log X DFG's*

## 9. VARIABLE DIODE FUNCTION GENERATOR GROUPS 2.645 AND 2.713

### a. General Description

The variable diode function generators (VDFG's) are used in conjunction with dc amplifiers to produce a segmented straight-line approximation to an arbitrary function. They accept an input voltage X and produce an output voltage Y = f(X), where f is a predetermined, single-valued function that can be non-monotonic. The desired function is produced by summing the outputs from biased diode networks. As the input voltage changes, the diodes effectively switch the input resistors of a summing amplifier, thus varying the amplifier gain. The output voltage of the amplifier changes in accordance with the input voltage by a sequence of straight-line segments.

Two basic VDFG groups are available. The 2.645 Groups provide plus and minus units with variable slopes and breakpoints; the 2.713 Groups have variable slopes and fixed breakpoints. The groups are listed below.

| GROUP NUMBER | +VDFG UNIT | READOUT MODULE | -VDFG UNIT |
|---|---|---|---|
| 2.713-0 | 16.156-1 | 16.310 | 16.154-1 |
| 2.713-1 | 16.156-1 | 16.310 | --- |
| 2.713-2 | --- | 16.310 | 16.154-1 |
| 2.645-0 | 16.304-1 | 16.308 | 16.306-1 |
| 2.645-1 | 16.304-1 | 16.308 | --- |
| 2.645-2 | --- | 16.308 | 16.306-1 |

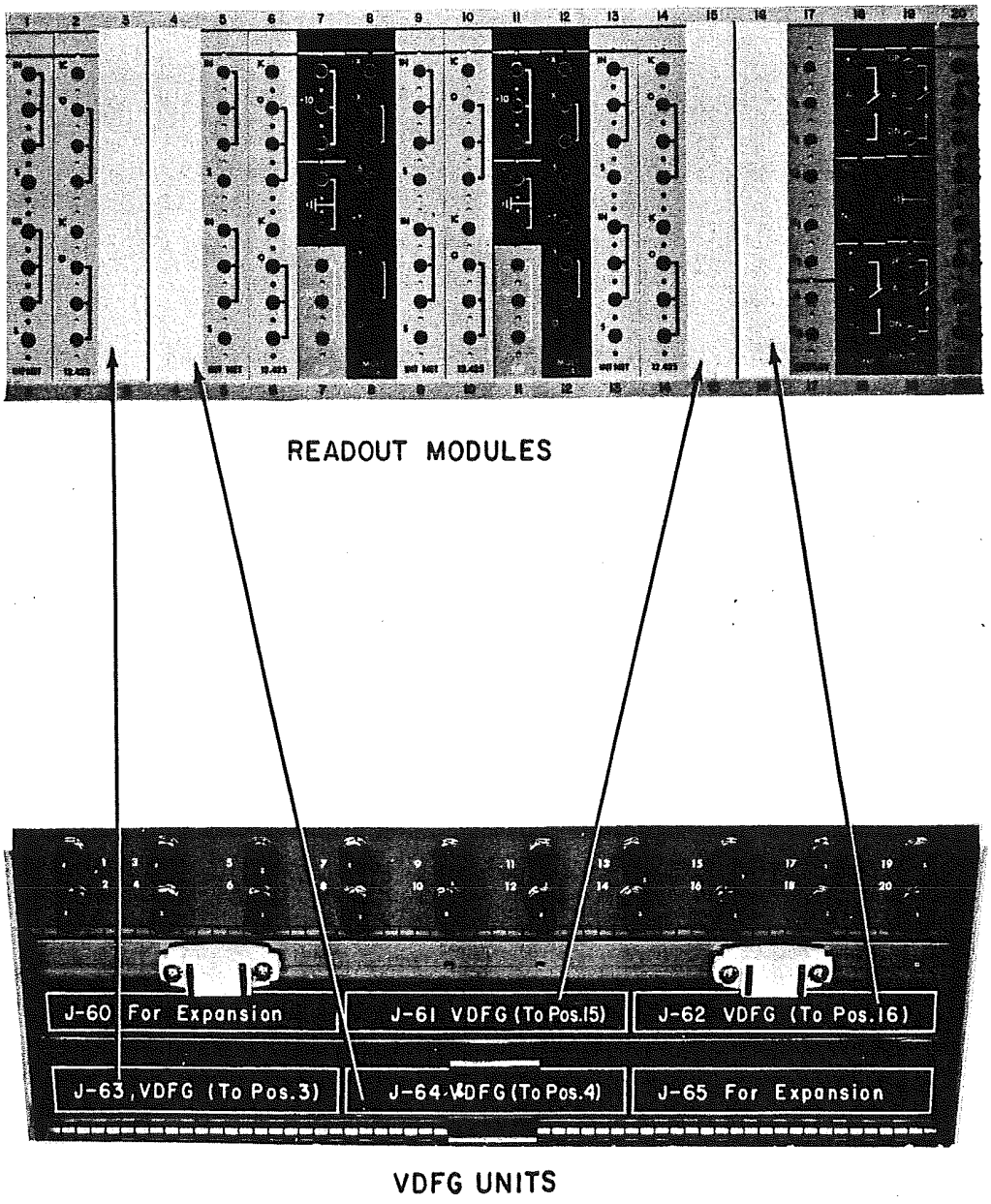



*Figure 16. VDFG Mounting Locations*

NOTE: The 16.165-1 ±VDFG Unit may be located in J-61, J-62, J-63, or J-64.

The 16.154 Minus VDFG Unit is identical to the 16.156 Plus VDFG, except that diode and reference polarities are reversed. Similarly, the 16.306 and 16.304 Units are identical except for diode and reference polarities. Therefore, the 16.156 Plus (fixed breakpoint) VDFG and the 16.304 Plus (variable breakpoint) VDFG are the only units described in this section.

b. Setup Procedure (Fixed Breakpoint VDFG's)

A simplified diagram and a typical patching scheme for the 16.156 Plus VDFG is shown in Figure 16. This information is applicable to the other VDFG's, however, the input voltage polarity restrictions for each unit must be observed.

The function shown in Figure 17a is used to illustrate the procedure for setting up a fixed breakpoint VDFG. Proceed as follows:

(1) Prepare a table (Figure 17b) of the appropriately scaled voltages desired at the output of the VDFG when the input voltage is equal to 0, +1, +2, +3, +4, +5, +6, +7, +8, +9, and +10 volts.

(2) Open the door below the control panel and slide the appropriate VDFG tray forward, exposing the adjustment potentiometers. Patch the circuit shown in Figure 17c.

(3) Turn the VDFG potentiometers fully counter-clockwise. Temporarily disconnect the output of amplifier 1 from the VDFG, and ground the +IN terminal. Adjust the PARALLAX pot to obtain the appropriate output voltage, in this case +2.6 volts.

(4) Re-connect amplifier 1 to the +IN terminal, and adjust the setup pot to provide an input of +1 volt. Adjust the +1 volt pot until the correct output voltage is reached (+3.3 volts in this case).

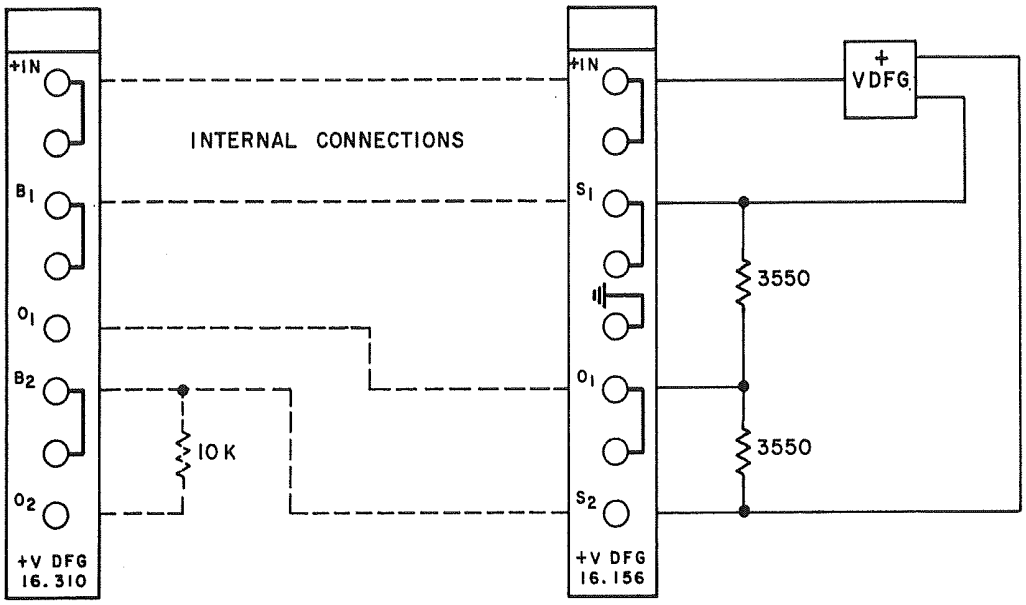
(5) Apply an input of +2 volts. Adjust the +2 volt pot until the correct output voltage is attained. For the sample function shown, this value is +4.0 volts.

(6) Continue to change the input voltages sequentially, and obtain the correct output voltage for each input increment by adjusting the appropriate slope potentiometers. The slope adjustments must be made in order, going from 0 to +10 volts (0 to -10 volts for a Minus VDFG).

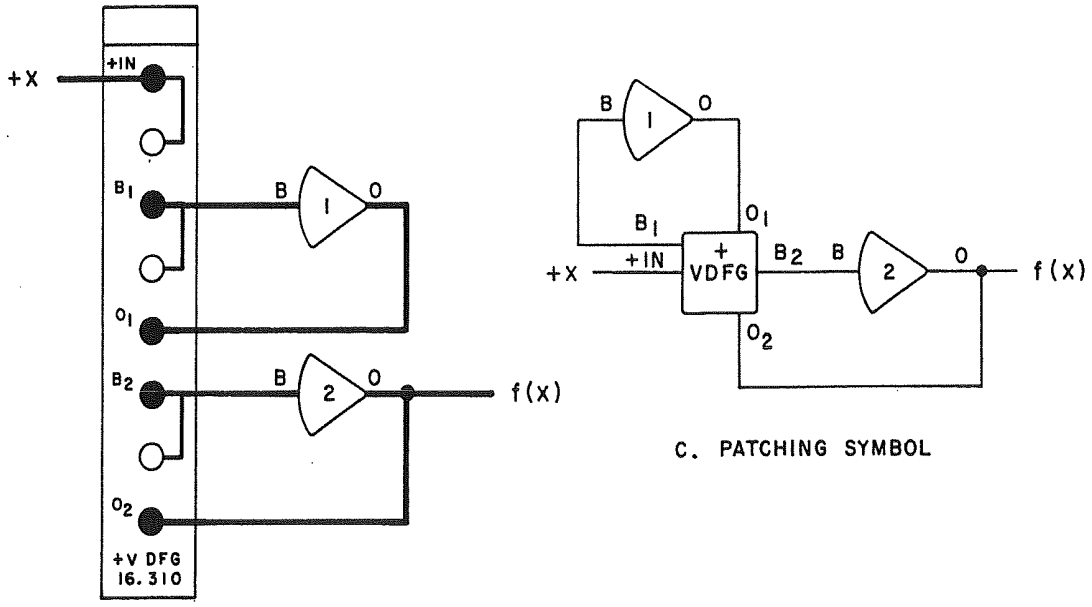
(7) Check the complete setup (preferably with a plotter) to ensure that the function is well adjusted. Slide the VDFG tray into its operating position and close the cover.

c. Setup Procedure (Variable Breakpoint VDFG's)

The variable breakpoint VDFG's provide for ten variable breakpoints in the interval from 0 to +10 volts (Model 16.304), or 0 to -10 volts (Model 16.306). This feature adds considerably improved flexibility and accuracy over the fixed breakpoint VDFG's, but requires a more complicated setup procedure. This sub-paragraph details a practical procedure for setting up the plus variable breakpoint VDFG without any external equipment except the X-Y plotter. The setup procedure for the minus variable breakpoint VDFG is identical, except for the polarity of the input voltage.



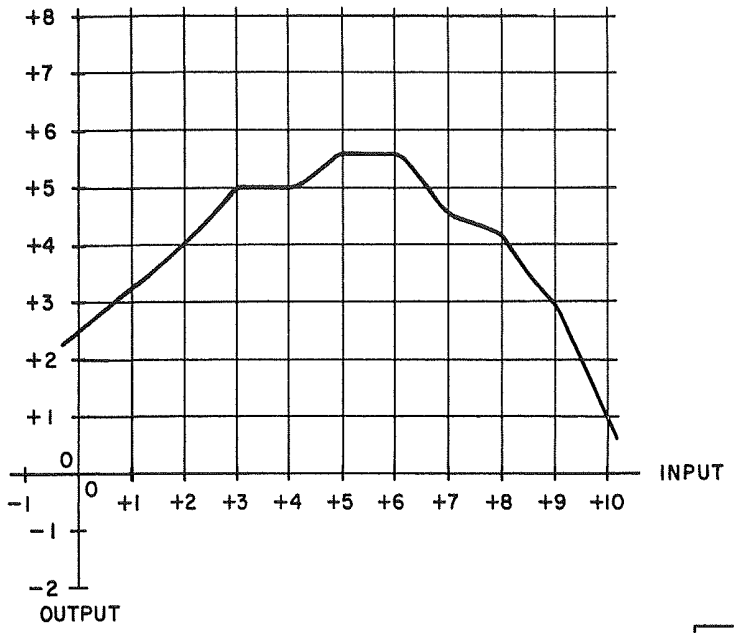

a. SIMPLIFIED SCHEMATIC




b. PATCHING

c. PATCHING SYMBOL

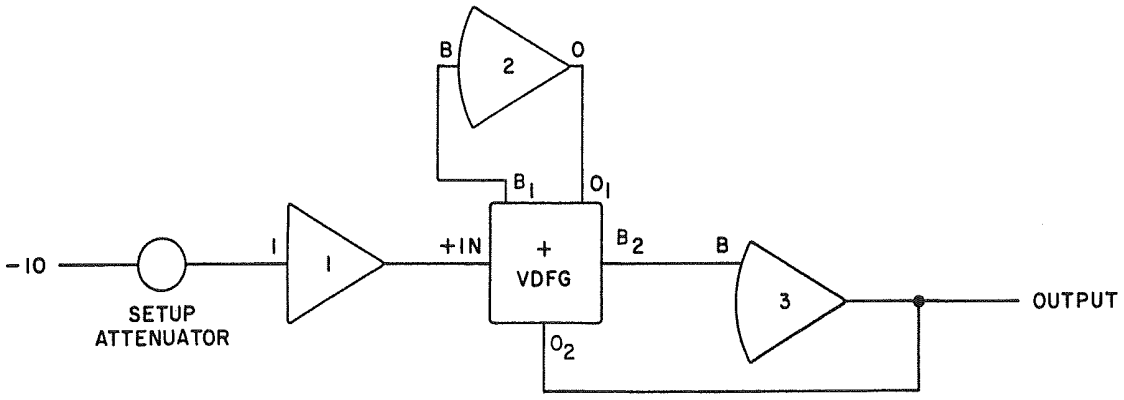
*Figure 16a. ±VDFG Patching*




a. SAMPLE FUNCTION

b. TABLE OF FUNCTION VALUES

| INPUT | ADJUST | OUTPUT |
|---|---|---|
| 0 | PARALLAX | +2.6 |
| +1 | +1V | +3.3 |
| +2 | +2V | +4.0 |
| +3 | +3V | +5.0 |
| +4 | +4V | +5.0 |
| +5 | +5V | +5.7 |
| +6 | +6V | +5.7 |
| +7 | +7V | +4.6 |
| +8 | +8V | +4.2 |
| +9 | +9V | +3.0 |
| +10 | +10V | +1.0 |




c. SETUP PATCHING

*Figure 17. Sample Function and Setup Information*

(1) Basic Setup Considerations. The diodes used in the construction of the VDFG are not ideal switches. The transition from the non-conducting to the conducting state is not abrupt, but gradual. As a result, instead of a sharp "corner" in the DFG output graph, a rounded corner will result. Since the straight-line segment curve is usually only an approximation to a desired smooth curve this "rounding" effect improves the accuracy of the DFG. However, it complicates the setup procedure for two reasons:

(a) It takes a variation of about one-fifth of a volt in the input voltage to switch the diode off or on. Hence the setting of the breakpoint is complicated by the fact that the breakpoint is not clearly defined.

(b) If the breakpoints are close together, adjusting the value at either one of them will affect the value at the other. This interaction necessitates setting the function values by successive approximation - first set the value at breakpoint 1, then set the value at breakpoint 2, then return to breakpoint 1, and touch it up, then return to 2, etc. This process can be somewhat lengthy.

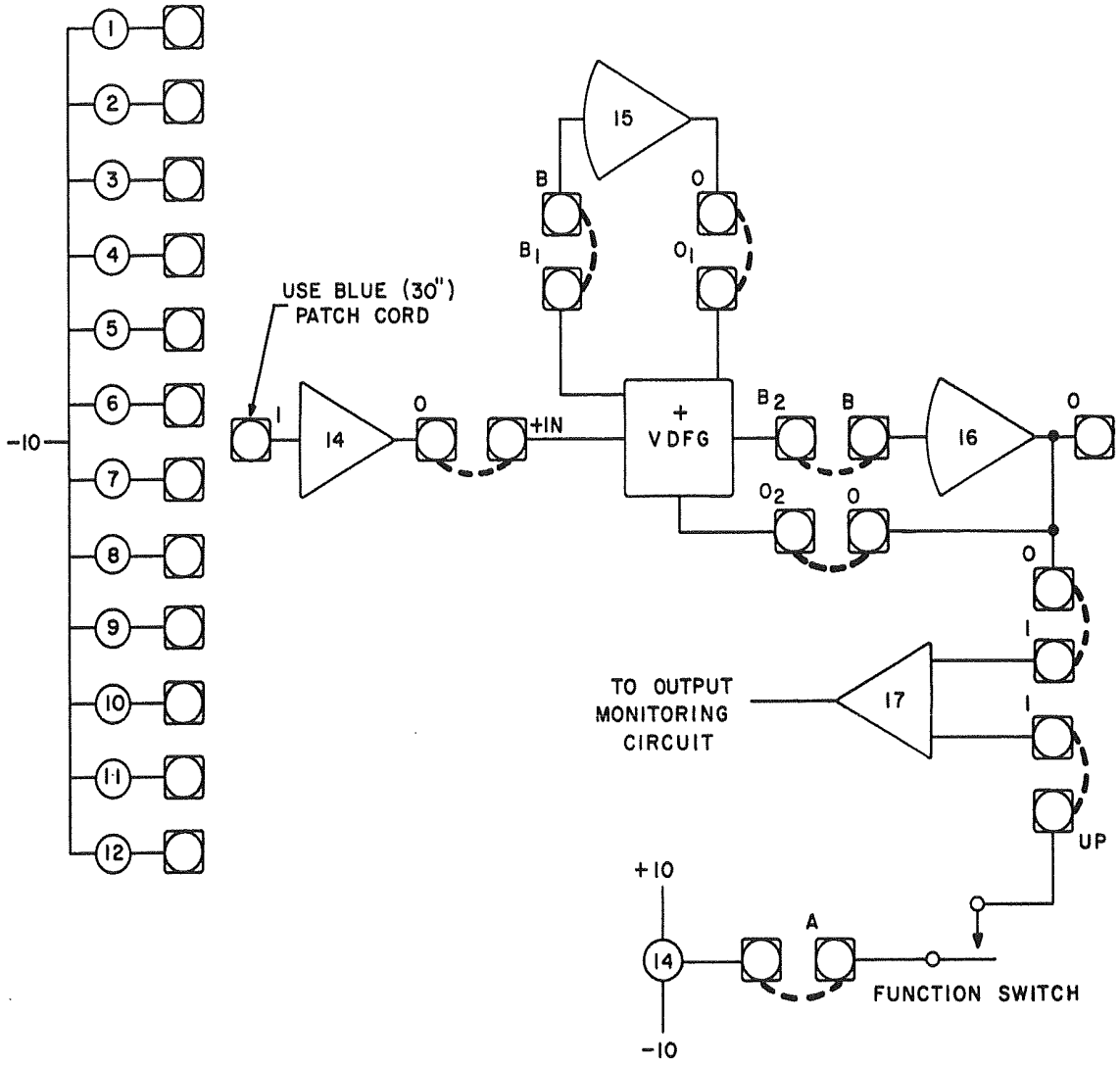
To avoid these difficulties, the following rules are adopted:

(c) The breakpoint is defined as the input voltage that produces 1.0 microamp of current through the diode. This is approximately on the "knee" of the diode characteristic curve. With a feedback resistor of 100K, this current contributes 0.10 volts to the DFG output. This is relatively easy to measure.

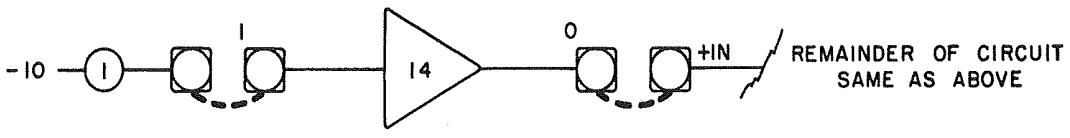
(d) To minimize interaction between the function values at different breakpoints, adjacent breakpoints should never be placed closer together than one-fifth of a volt. This is not a serious restriction. Since a change of about 0.2 volt in the input is required to make a diode change state, two breakpoints closer together than 0.2 volt will produce in effect only one breakpoint, and the interaction described above will make setup difficult. If the spacing is about 0.2 to 0.25 volt, the interaction will be less severe, and the portion of the graph between the breakpoints will be a smooth curve rather than a straight-line.

(e) As in all diode function generators and multipliers, the input impedance changes with a change in input voltage. Therefore, the input should always be supplied by an amplifier rather than a potentiometer.

(2) Breakpoint Setup Patching. If sufficient coefficient-setting attenuators are available, patch the configuration shown in Figure 18a. If the required number of attenuators is not available, the circuit of Figure 18b may be used. The method described in Figure 18a is much faster, and therefore preferred. The attenuators are required for setup only, and are released for other functions when the setup is complete. The first part of the setup procedure consists of




a. BREAKPOINT SETUP PATCHING (PREFERRED)




b. BREAKPOINT SETUP PATCHING (ALTERNATE METHOD)

*Figure 18. Breakpoint Setup Patching*

setting the breakpoints. The steps outlined in this procedure should be followed carefully to assure maximum accuracy of the diode generated function.

(a) Prepare a table of values for the function to be generated (Figure 19a). The function (for a Plus VDFG) can be arbitrarily specified at twelve points $X_0$, $X_1$, $X_2$, ... $X_{11}$. Of these, the ten internal points are called breakpoints (corners) and the other two are endpoints. We should pick $X_0 = 0$, and normally $X_{11} = +10$ volts. No two of these points should be closer together than 0.2 volt. These values should be selected from a graph of the function to occur at locations on the curve near important points of inflection and other areas requiring the most accurate delineation. If the patching arrangement of Figure 18a is used, set the attenuators (1 through 12) accurately to the twelve values of X specified in the table. Be sure to ground the low end of even numbered pots 2 through 12. Place the computer in the reset mode, and slide the tray containing the 16.304 Plus VDFG forward.

(b) Set all breakpoint pots fully clockwise (this means all breakpoints are close to +10 volts). Place the function switch in the center position. Ground the input to amplifier 14.

(c) Rotate slope pot 1 fully clockwise. Rotate slope pot 2 fully counter-clockwise, and continue alternating the slope pots in this manner. This step helps prevent amplifier overload and aids in identifying the breakpoints during the setup procedure.

(d) Set the output (amplifier 16) approximately to zero by adjusting the PARALLAX potentiometer.

(e) Set the input (amplifier 14) to +1 volt. Set the output (amplifier 16) approximately to zero with the CENTRALSLOPE potentiometer.

Steps (d) and (e) above are performed simply to help prevent amplifier overload during the remaining steps.

(f) If the patching arrangement of Figure 18 is used, connect the input of amplifier 14 to the wiper of pot 1 with the long patchcord. If the method of Figure 18b is used, adjust pot 1 to the correct coefficient using the NULL POT.

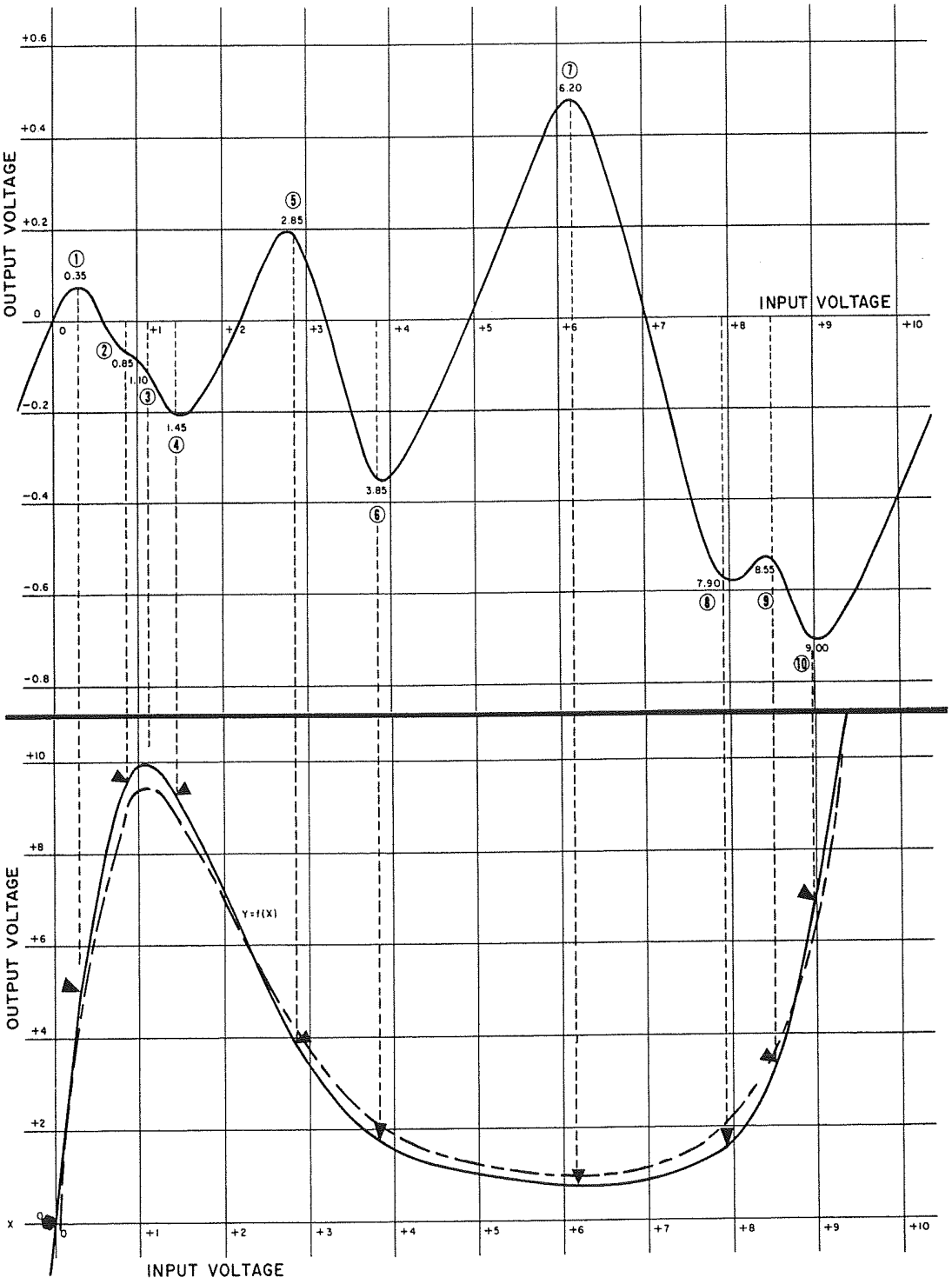
(g) Set the voltmeter function switch to the AMPL position, the range switch to the 3 position, and the AMPL SEL switch to position 17. The reading should be close to zero, although the precise value is not critical.

(h) Place the function switch in the UP position, and adjust pot 14 until the voltmeter reading decreases to zero. To avoid over-

| LOCATION | X | f(X) |
|---|---|---|
| $X_0$ — LEFT ENDPOINT | 0.00 | 0.00 |
| $X_1$ — FIRST BREAKPOINT | 0.35 | 5.81 |
| $X_2$ — SECOND BREAKPOINT | 0.85 | 9.34 |
| $X_3$ — THIRD BREAKPOINT | 1.10 | 9.93 |
| $X_4$ — FOURTH BREAKPOINT | 1.45 | 9.36 |
| $X_5$ — FIFTH BREAKPOINT | 2.85 | 3.67 |
| $X_6$ — SIXTH BREAKPOINT | 3.85 | 1.69 |
| $X_7$ — SEVENTH BREAKPOINT | 6.20 | 0.89 |
| $X_8$ — EIGHTH BREAKPOINT | 7.90 | 1.56 |
| $X_9$ — NINTH BREAKPOINT | 8.55 | 3.20 |
| $X_{10}$ — TENTH BREAKPOINT | 9.00 | 6.75 |
| $X_{11}$ — RIGHT ENDPOINT | 9.50 | 12.00 |

a. TABLE OF FUNCTION VALUES

b. BREAKPOINT LOCATION CURVE




● – ENDPOINT

▲ – BREAKPOINTS

c. PLOT OF DESIRED FUNCTION

– – – – – CURVE BEFORE TRIMMING

——— CURVE AFTER TRIMMING

*Figure 19. +Variable Breakpoint Diode Function Generator Sample Curves*

loading the meter (in the .3 volt range), it is advisable to set pot 14 to approximately .500 before closing the function switch. The first breakpoint is now located close to +10 volts and we want to relocate it at $X_1$ (the desired first breakpoint).

Rotate breakpoint pot 1 counter-clockwise while observing the meter. At first, nothing will happen, but when the breakpoint is in the vicinity of $X_1$ the output will start to change. Rotate the pot until the output changes by 0.1 volt. The first breakpoint is now correctly set at $X_1$. Do not change any slope pot settings at this time.

(i) Repeat Step (f), setting the value of potentiometer 1 to the value required for the second breakpoint (Figure 18b), or move the long patch cord to pot 2. Place the function switch in the center position and repeat Step (g) above.

Repeat Step (h), adjusting the breakpoint 2 potentiometer for a 0.10 volt change on the meter. For instance, potentiometer 14 is adjusted until the meter reads a null (zero volt) in Step (h). The breakpoint potentiometer is then rotated until the voltmeter reads +0.10 or -0.10 volts, whichever is appropriate. Set the remaining breakpoints in this manner.

(j) The breakpoints are now set correctly, but the slopes are still set at the extremes (approximately $\pm 1$ volt per volt). It is a good idea to plot the output of the DFG versus the input at this time. The resulting curve will zig zag up and down (see Figure 19b), and will not look much like the desired curve, but it enables one to check at a glance that the breakpoints are properly located.

To make this plot, adjust the DFG input voltage to $X_{11}$ (the endpoint of the interval of interest - usually +10 volts) and adjust the CENTRALSLOPE pot so that the output is approximately zero. This does not affect the breakpoint location, but merely shifts the entire curve so as to provide a more easily read plot.

Patch the configuration shown in Figure 20, and place the computer in the operate mode. An initial condition voltage of -1 volt is provided so that the plotter pen describes the entire curve under consideration. With an input of -1 volt to the integrator, the plotter will cover the range of -1 to +10 volts in 11 seconds.

(3) Setting the Function Values. Set all slope pots approximately to zero. This adjustment is not critical, and could be omitted, but it helps prevent amplifier overload during setup. Since fully clockwise rotation of the slope pot produces a slope of +1 volt per volt and fully counter-clockwise rotation produces

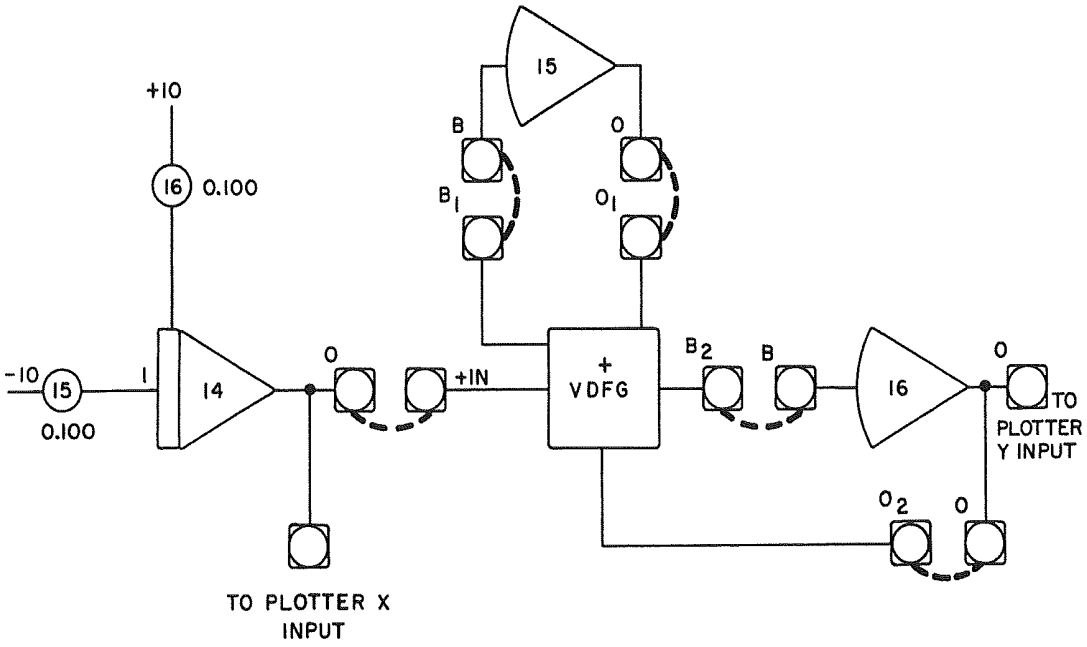



*Figure 20. Breakpoint Location Plot Patching*

-1 volt per volt, zero slope is found with the pot at the center of its rotation. Since the pots rotate through approximately 300 degrees, zero slope may be approximately obtained by watching the screwdriver blade and rotating the pot a little less than $180^{o}$ from its extreme position.

(a) Patch the circuit shown in Figure 21a and ground the input to amplifier 14, or adjust potentiometer 1 to produce zero volts (Figure 21b). Adjust the PARALLAX potentiometer to produce f(0) accurately. This is best accomplished by connecting the output of amplifier 17 to the VM jack, and using the voltmeter in the NULL function (see Chapter II, Paragraph 3a.).

(b) Set the VDFG input to $X_1$ (the first breakpoint). Adjust the CENTRAL SLOPE potentiometer to read $f(X_1)$ accurately on the meter.

(c) Set the VDFG input to $X_2$ (the second breakpoint). Adjust slope pot 1 until the meter indicates a null with the NULL POT set to $f(X_2)$.

NOTE

Except for the first two points, the function value at a given breakpoint is set by adjusting the slope pot for the preceding breakpoint.

(d) Continue in this way until all breakpoints have been set. The last value set is the right endpoint, $X_{11}$, which is usually +10 volts.

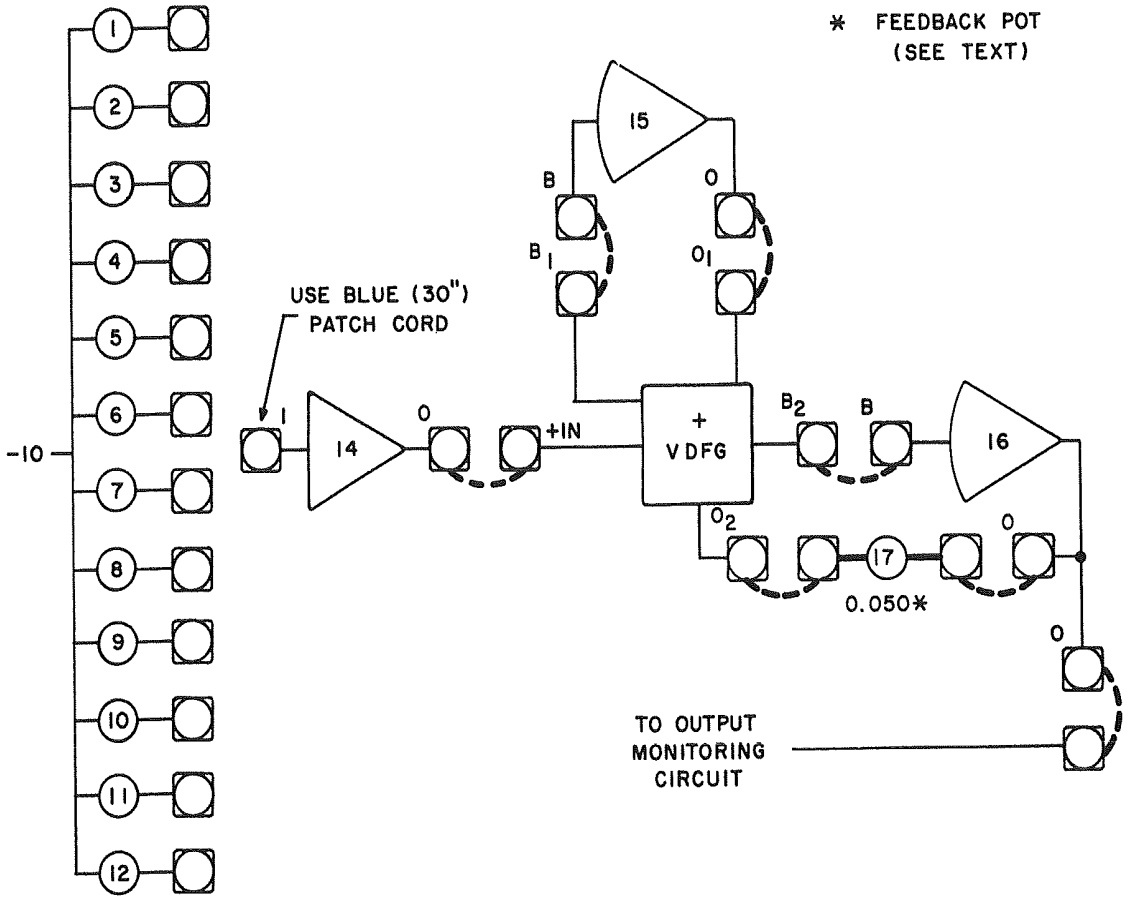
(e) Patch the circuit shown in Figure 20, and plot the entire curve as done previously in Sub-paragraph (2)(j).

(4) Trimming Adjustments. Frequently a slight shift may be noted in the function values that were first set up. This is due to the interaction mentioned above - setting the value at one point has a slight effect on the previously set values. This effect will be largest where the breakpoints are closest together, or where the curve is steepest.

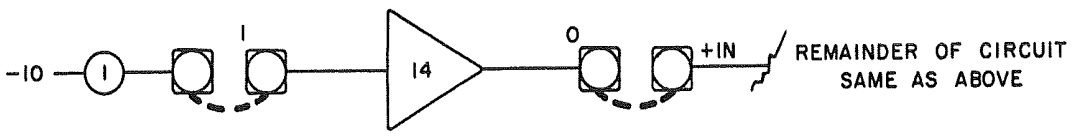
It is, for this reason, necessary to perform a trimming adjustment of the function values. The best way to do this is to start at $X_0$ and proceed out to $X_{11}$, as above. Plot out the entire curve again. In extreme cases, a second trimming adjustment may be necessary, but this is seldom the case. The best way to determine whether additional trimming is necessary is to plot the entire curve and compare it with the desired one.

(5) Additional Considerations

(a) Amplifier Overloads. If the above procedure is followed carefully, no overloads should occur during the set up of the breakpoints. However, the set up of the function values may cause overloads. (If the desired function value is close to 10 volts, it may be considerably more than 10 volts before adjustment.)




a. FUNCTION SETUP PATCHING (PREFERRED)




b. FUNCTION SETUP PATCHING (ALTERNATE METHOD)

*Figure 21. Function Setup Patching*

Of course, if the function is properly scaled and is within the slope limitations of the DFG, it should be possible to adjust the appropriate slope pot to set f(X) to the desired value and remove the overload. However, if the amplifier is saturated, it is hard to adjust the correct value, as the voltmeter will not respond immediately to the slope pot. In this case, the following steps are recommended:

-1- Temporarily patch an extra 10K feedback resistor around the amplifier producing f(X).

-2- Put the computer in the reset mode. The output should not overload.

-3- Adjust the output to zero, or as close to zero as possible.

-4- Remove the extra feedback resistor. The output should increase, but not overload.

-5- Set the output to the desired value.

(b) Pot Loading. The DFG input should always come from an amplifier, not from a pot. The load on any pot should always be a fixed resistor from the pot output terminal to ground. If a pot is fed into a DFG, the load on the pot will depend on the number of diodes conducting, and a loading error will result.

(c) Insufficient Slope. The maximum slope of 1 volt per volt per segment is not enough for all functions to be generated. If more slope is needed, the DFG feedback resistor can be increased, or a pot may be placed in the feedback path. With this arrangement, the maximum obtainable slope per segment is 1 volt per volt divided by the pot-setting (e.g., a pot-setting of 1/2 gives a slope of 2 volts per volt per segment). This increase in slope will increase the noise level proportionately, but this effect will not be objectionable with reasonable gains. Even the sample curve shown in Figure 19c, which requires a pot-setting of 0.050 (slope of 20 volts per volt) should present no noise problems. When setting breakpoints, the standard 100K feedback should be used (no pot). Otherwise the 0.10 volt criterion for setting the breakpoint will not apply.

To find out whether amplification is necessary, the slopes between adjacent breakpoints may be tabulated. The slope between the i-th and the (i + 1)st breakpoints is:

$$\frac{f(X_i + 1) - f(X_i)}{X_i + 1 - X_i}$$

This is easily calculated. It is important to realize that, except for the center slope (the slope at X = 0) the actual slope of the curve is not as important as the increment in slope. For instance, if a function had a center slope of 0.85 volt per volt, and successive slopes of 1.50, 2.10 and 3 volts per volt, no amplification would be necessary, since the center slope and the slope increments are all less than one volt per volt. (The slope at any point, is the sum of the slopes due to all diodes that are conducting at the point, plus the center slope. Hence, except for the center slope, any slope may exceed 1 volt per volt as long as the change in slope between successive segments does not.)

d. Paralleling Fixed Breakpoint VDFG's

In some cases, it may be desirable to generate a function over an input range of $-10 \leq X \leq +10$. A Plus VDFG and a Minus VDFG can be paralleled and the desired function approximated by 19 straight-line segments. Certain points must be noted when VDFG's are paralleled. The PARALLAX potentiometer of each generator can adjust the output at f(0). Therefore, the two PARALLAX controls are interdependent. Note also that there is no breakpoint at X = 0. The first breakpoint occurs at X = +1 in the Plus VDFG and at X = -1 in the Minus VDFG. The initial slope adjustment, labeled 1 volt, in each unit determines the slope of the output when no diodes are conducting, that is, in the range $-1 \leq X \leq +1$ for the paralleled units. Therefore, the values of f(-1), f(0), and f(+1) must be colinear. The segment about $-1 \leq X \leq +1$ is two volts long instead of the usual one volt. The paralleled function generators can be set up easily by means of the following procedure.

(1) Determine the values of f(-1) and f(+1) that give a good straight-line fit over the range $-1 \leq X \leq +1$.

(2) Calculate $f(0) = \frac{1}{2}\left[f(-1) + f(+1)\right]$.

(3) Adjust either or both PARALLAX controls until f(0) measures the calculated value.

(4) Apply an input of -1 volt and adjust the -1 volt control on the Minus VDFG until f(-1) is set correctly.

(5) Apply an input of +1 volt and check f(+1). No adjustment should be necessary; however, if a small deviation from the desired value is found, adjust the +1 volt control on the Plus VDFG to remove half the error. The error should now be divided equally between f(-1) and f(+1).

(6) Adjust f(+2), f(+3), ..., f(+10).

(7) Adjust f(-2), f(-3), ..., f(-10).

(8) Recheck the entire function.

## 10. SIGNAL COMPARATORS AND FUNCTION SWITCHES

### a. Relay Comparator

(1) General Description. The Relay Comparator consists of a high-gain amplifier and a double-pole, double-throw relay. The amplifier compares a variable input voltage to an arbitrary reference input voltage and operates the relay when the weighted algebraic sum of the input voltages is negative. The relay is de-energized when the weighted algebraic sum of the input voltages is positive.

The circuit configuration of the relay comparator is shown in Figure 22a. The signal input is applied to $IN_1$; the reference input is applied to $IN_2$. When the inputs produce a negative voltage at the summing junction of the amplifier, the amplifier energizes the relay and the relay arms are connected to the minus contacts. The relay is de-energized when the summing junction is positive or when no inputs are applied; the relay arms are connected to the plus contacts. Since the input resistors, R1 and R2, have different values, the voltages applied to $IN_1$ and $IN_2$ have different weights in their effect on the summing junction voltage. Therefore, the setup procedure described below must be followed if precise switching levels are desired.

(2) Adjustment of Voltage Switching Level. To obtain a precise voltage switching level, say +5 volts, proceed as follows:

(a) Refer to Figure 22b. Connect a coefficient potentiometer to the input of an amplifier and adjust the wiper until the output of the amplifier is at the desired switching level (+5 volts in this example). Connect the output of the amplifier to the $IN_1$ termination of the comparator.

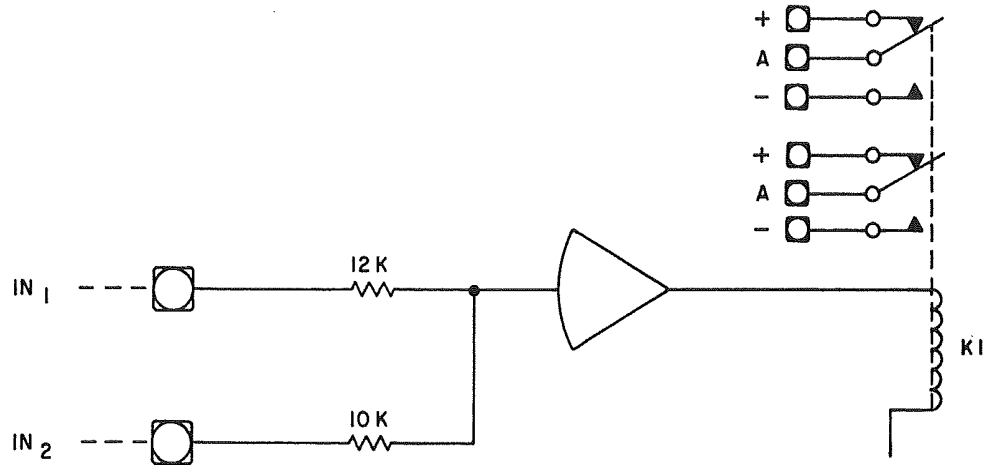
(b) Connect the appropriate computer reference voltage (-10 vdc in this case) to a second potentiometer. Connect the wiper to the $IN_2$ termination.

(c) Adjust the wiper of the second potentiometer until switching occurs. The switching action can be observed by patching reference voltage into a relay arm and monitoring the voltage on a contact with the voltmeter.

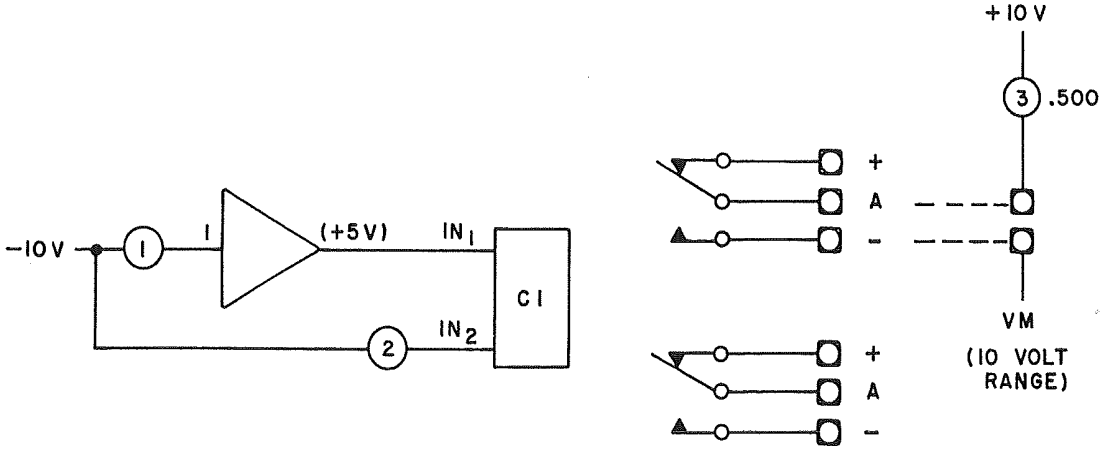
(d) Remove the amplifier input to $IN_1$ and apply an arbitrary signal input.

### b. Electronic Comparator

The Model 40.538 Electronic Comparator (Figure 23) is a versatile high-speed switching device. The unit operates in conjunction with external operational amplifiers, and consists of a comparator unit which produces binary output levels, and two electronic switch units. These units may be combined or used independently, depending on the circuit requirements and the patching arrangements.




(a) SIMPLIFIED DIAGRAM




(b) CIRCUIT FOR SETTING VOLTAGE SWITCHING LEVEL

*Figure 22. Relay Comparator, Simplified Diagrams and Setup Patching*

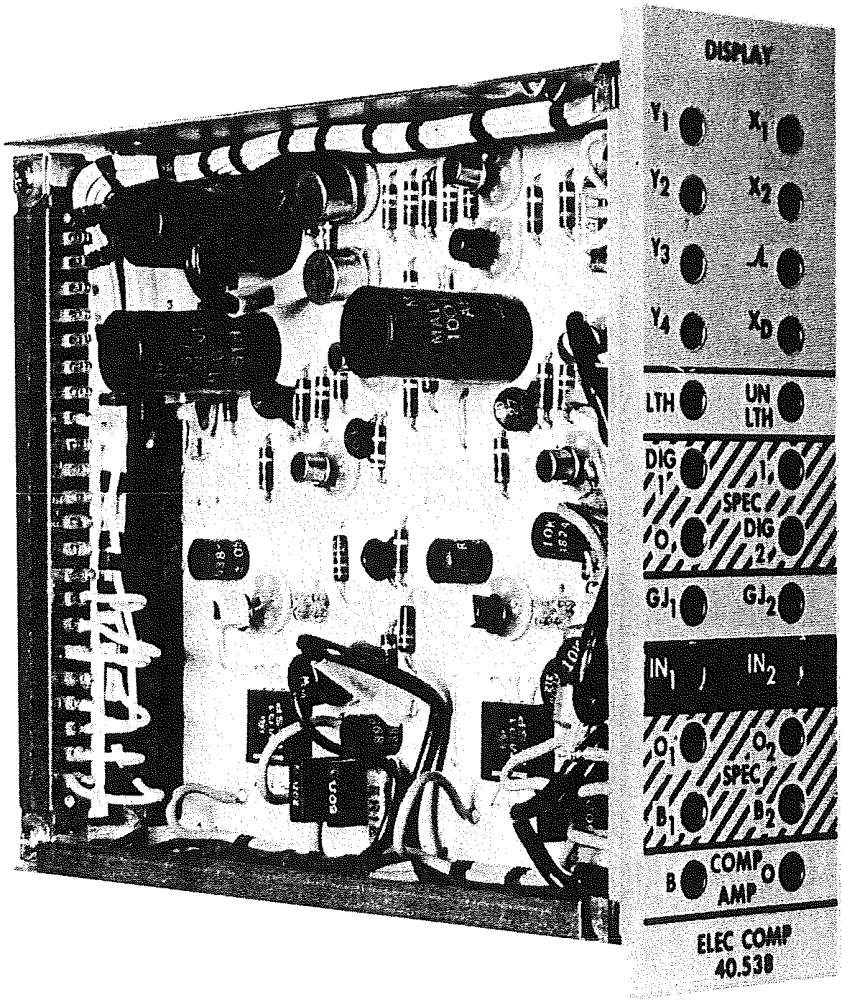



*Figure 23. 40.538 Electronic Comparator Unit*

(1) The Comparator. A functional block diagram of the comparator unit is provided in Figure 24. The analog voltages to be compared are applied to the input of the amplifier, which is provided with a special feedback network within the comparator. This feedback network consists of two back-to-back diodes, and allows the high-gain of the amplifier under open loop conditions to provide highly accurate switching. The output of the comparator unit is provided at two terminals designated DIG 1 and 0. Only two voltage levels are available at these terminals, zero volts or +5 volts. In addition, the voltages at the 1 and 0 terminals are always complementary (opposite from each other). For example, if the voltage at the summing junction of the comparator amplifier is positive, the circuit will produce plus 5 volts at the 1 terminal and zero volts at the 0 terminal. These levels are referred to as binary ONE and binary ZERO respectively. If the voltage at the summing junction of the amplifier goes negative, the state of the circuit reverses and a binary ZERO appears at the 1 terminal while +5 volts (binary ONE) appears at the 0 terminal.

In addition to the analog inputs, binary logic levels may be connected to the latch (LTH) or unlatch (UNLTH) terminals to control the operation of the comparator. If a binary ONE (+5 volts) is applied to the latch terminal, the output of the comparator amplifier is effectively disconnected from the comparator unit, and the binary output levels from the comparator remain in their previous states. If a binary ZERO (ground or 0 volt) is applied to the unlatch terminal, the analog input voltages regain control of the comparator. The binary ZERO applied to the unlatch terminal overrides the binary ONE at the latch terminal, so that if both are applied together, the comparator responds to analog input voltages.

The binary output levels from the comparator unit may be connected to either or both of the electronic switch units, trunked to another computer, or used for other special purposes.

(2) The Electronic Switch. Two electronic switches are included in the comparator unit. Figure 25 provides a block diagram of a switch unit. Each switch consists of a four-diode gate; precision input and feedback resistors; and a transistorized control circuit. When a binary ONE (+5 volts) is applied to the digital input terminal, the gate is opened and an analog current is passed through the gate to the associated amplifier. The analog input is normally connected to the appropriate IN terminal, then coupled through an input resistor and the gate to the amplifier. For special applications, the analog input may be connected to the GJ (gate junction) terminal, which by-passes the input resistor and applies the current directly through the gate to the amplifier summing junction. Circuits and patching for the electronic comparator are summarized in the appendix.

c. Dual Function Switch Group 2.127

The Dual Function Switch Group consists of a patching module, Type 12.264, and a Dual Function Switch Assembly, Type 20.366. The function switches are mounted on the Control Panel and are terminated on the patching module which is located in the middle row of the patch panel. Each function switch is a single-pole, double-throw switch with a center-off position. The upper switch is terminated on the upper

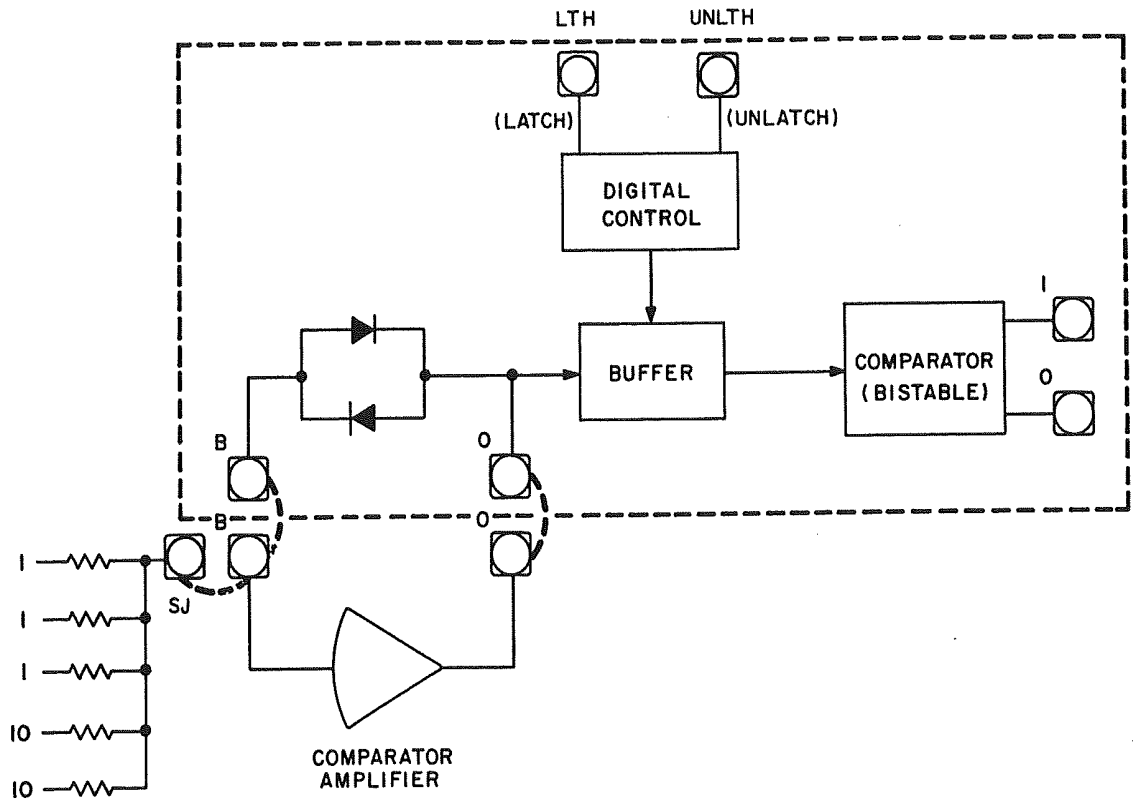



*Figure 24. Comparator Unit, Functional Block Diagram*

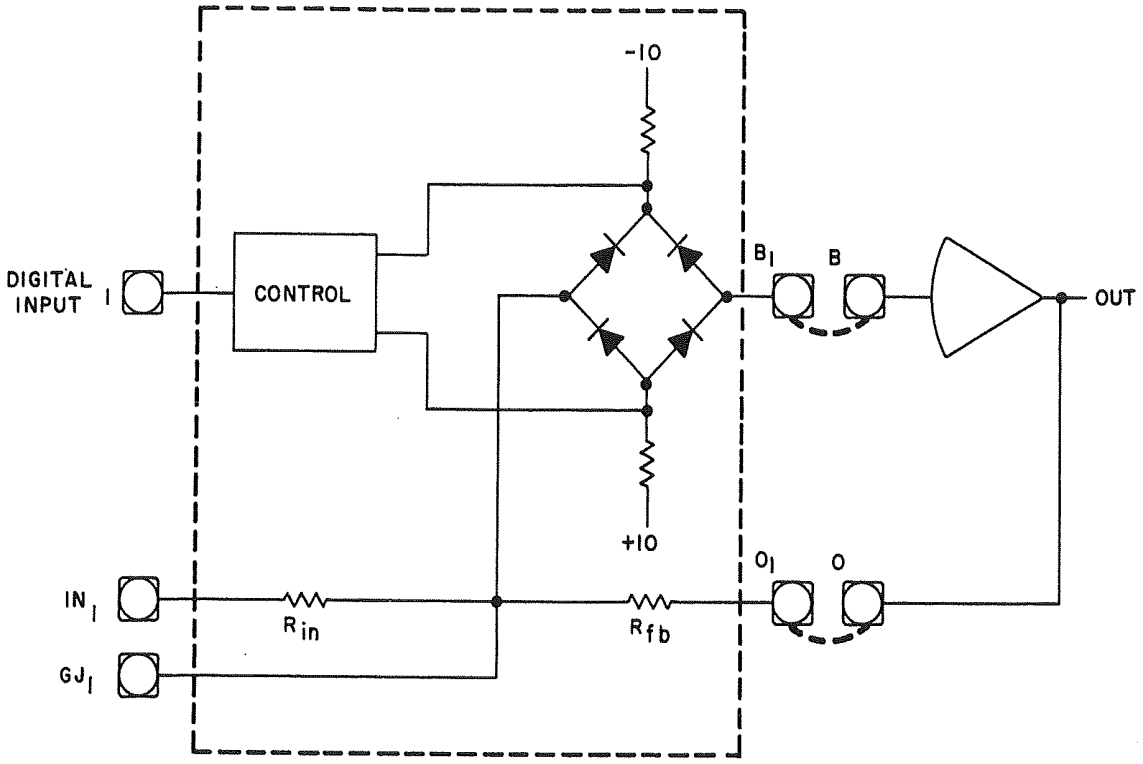



*Figure 25. Electronic Switch Unit, Functional Block Diagram*

portion of the patching module; the lower switch is terminated on the lower portion of the patching module. The switch contacts are rated at 120 volts, 10 amperes (resistive load).

## 11. REPETITIVE OPERATION

### a. General Description

The addition of the Repetitive Operation (Rep Op) Group to the TR-20 provides a means of switching the integrators between the reset and operate modes at rates greater than 30 cycles per second. The usual 10 mfd integrator feedback capacitors are replaced with 0.02 mfd capacitors to change the problem time scale by a factor of 500. Thus, the Rep Op Group gives the operator faster acquisition of problem solutions. The problem variables are displayed on the Model 34.035 Rep Op Display Unit, or an external oscilloscope. The computer can still be used as a real time simulator when the Rep Op Group is installed.

The Repetitive Operation Group consists of three units:

(1) A Model 20.532 Control Panel, which mounts in the sloping control panel area of the TR-20. It contains two controls, the COMPUTE TIME MILLISEC switch and the CALIBRATE VERNIER potentiometer, that determine the length of time the integrators are in operate. The COMPUTE TIME MILLISEC switch has an OFF position, four compute time positions of 20, 50, 100, and 200 milliseconds, and a SLAVE position. The CALIBRATE VERNIER permits continuous coverage between the fixed compute times and can increase the selected compute time by a factor of 2.5.

(2) A timing Unit that is located in the rear of the computer. It provides the integrator networks with a reset pulse that has a constant 10 millisecond duration and an operate pulse whose duration is determined by the position of the COMPUTE TIME MILLISEC switch and the CALIBRATE VERNIER.

(3) The Model 12.1115 Integrator Networks replace the standard Model 12.1116 Networks in computers equipped with repetitive operation. These networks are described in Paragraph 5 of this handbook.

(4) The 34.035 Repetitive Operation Display Unit is available as an accessory. It provides a large rectangular display and provision for up to four Y (vertical) inputs, which may be applied singly or through a four-position sequential electronic switch. A cable is provided with the unit which allows convenient installation, and signals to be observed are simply connected to the appropriate terminals on the readout patching module. An additional feature included with this unit is the ability to use the time base output from the Rep Op Timing Unit as a sweep (X) input, or by rotating a switch, the $Y_4$ input at the readout patching module provides a time base against which the other Y inputs ($Y_1$, $Y_2$, or $Y_3$) may be plotted.

Operating and maintenance instructions for the Model 34.035 are provided in a separate manual supplied with this instrument.

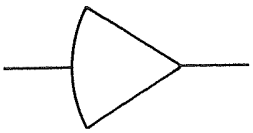
The electrical details of the Repetitive Operation Group are covered in the TR-20 Maintenance Manual.

b. Using Repetitive Operation

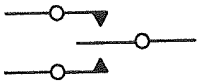
The computer is placed in the repetitive operation mode by selecting an appropriate compute time with the COMPUTE TIME MILLISEC and CALIBRATE VERNIER controls. The Mode Control switch must be placed in the HOLD position. The Rep Op Control Panel has two terminations labeled SCOPE; one is a ground termination and the other provides a sweep voltage for an external oscilloscope. The use of this sweep voltage eliminates difficulties in synchronizing the oscilloscope. When the CALIBRATE VERNIER is fully counter-clockwise, the compute time is indicated by the position of the COMPUTE TIME MILLISEC switch. As the CALIBRATE VERNIER is rotated, the compute time increases beyond the duration indicated by the COMPUTE TIME MILLISEC switch. During the setup of a problem when attenuators are being adjusted, the COMPUTE TIME MILLISEC switch must be placed in the OFF position so that the relays in the Integrator Networks can ground the summing junctions. If this is not done, loading errors will cause the attenuators to be set incorrectly.

# APPENDIX I

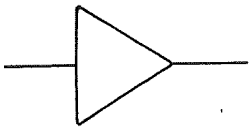
## COMPUTER SYMBOLS



HIGH GAIN AMPLIFIER

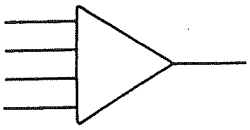


FUNCTION SWITCH



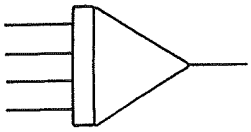
INVERTING AMPLIFIER

SOLID-STATE DIODE

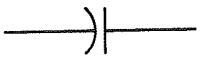


SUMMING AMPLIFIER

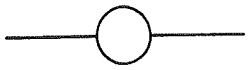
FIXED RESISTOR



INTEGRATING AMPLIFIER

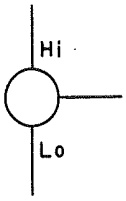


CAPACITOR



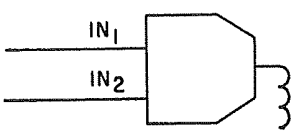
ATTENUATOR, LOWER END GROUNDED

Y INPUT OF XY PLOTTER

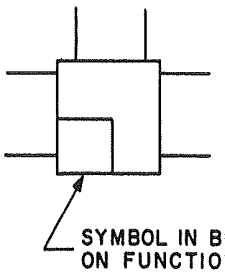



ATTENUATOR, UNGROUNDED

X INPUT OF XY PLOTTER




RELAY COMPARATOR



SYMBOL IN BLOCK DEPENDENT ON FUNCTION (SEE NOTE)

QUARTER-SQUARE MULTIPLIER

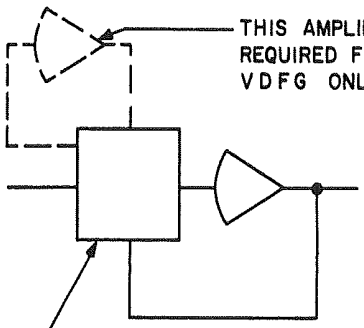
NOTE :

X = MULTIPLICATION

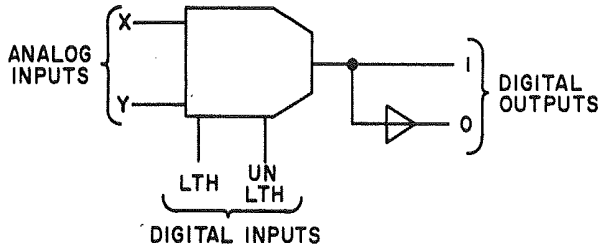
÷ = DIVISION

$X^2$ = SQUARING

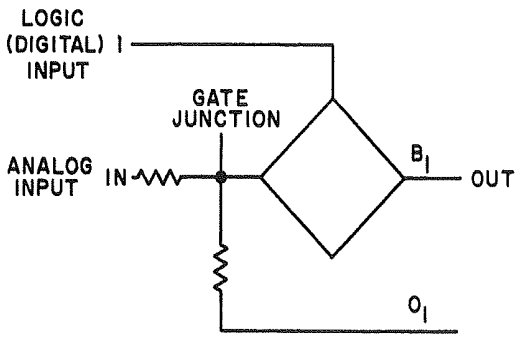
$\sqrt{X}$ = SQUARE ROOT




DIODE FUNCTION GENERATOR




ELECTRONIC COMPARATOR (AMPLIFIER INCLUDED)




ELECTRONIC SWITCH

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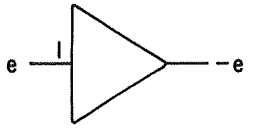
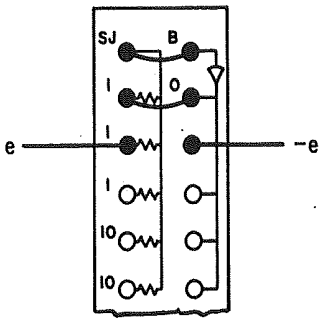
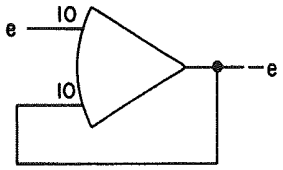
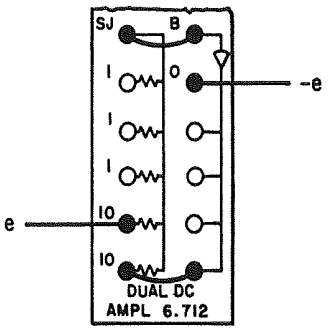
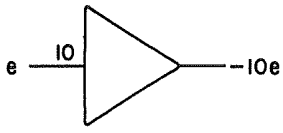
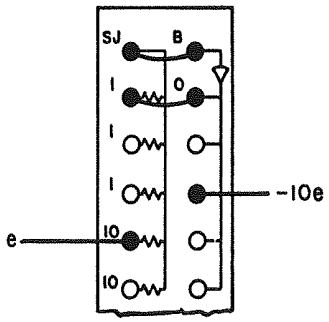
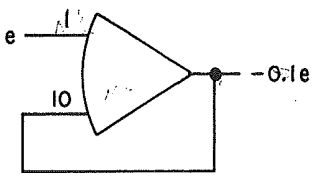
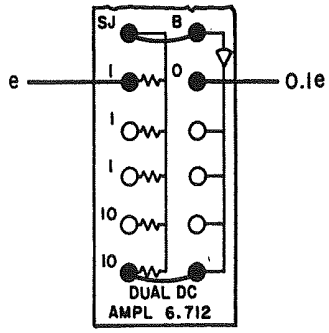
| INVERTERS |  |  | STANDARD CIRCUIT<br>100K INPUT IMPEDANCE |
| |  |  | 10K INPUT IMPEDANCE |
| MULTIPLIERS |  |  | GAIN OF 10 |
| |  |  | GAIN OF 0.1 |

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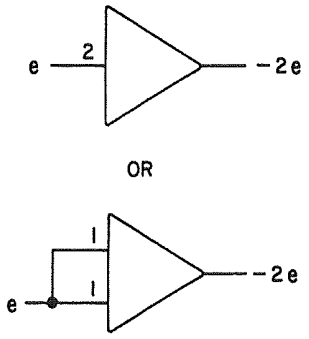
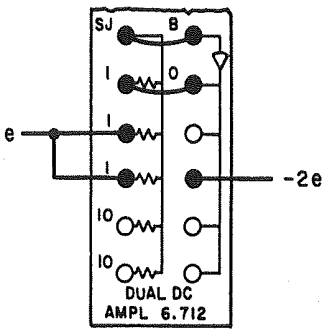
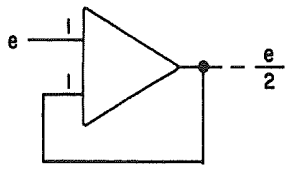
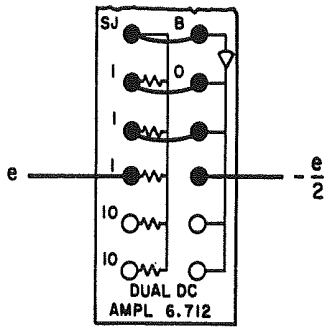
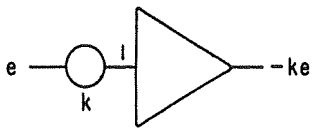
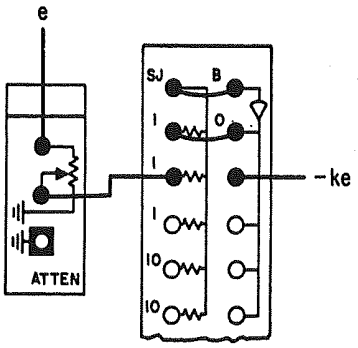
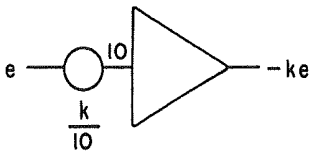
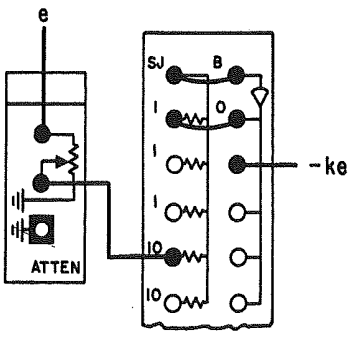
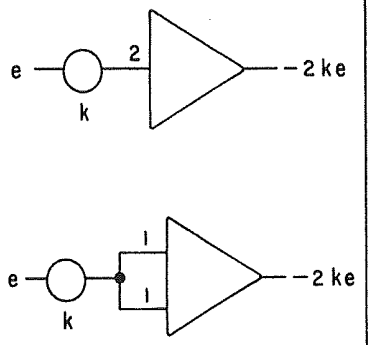
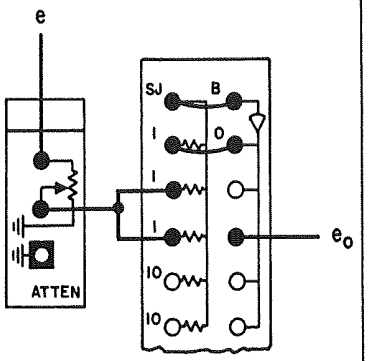
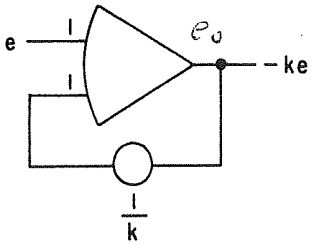
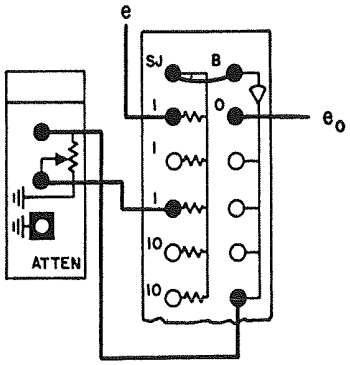
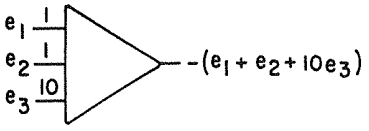
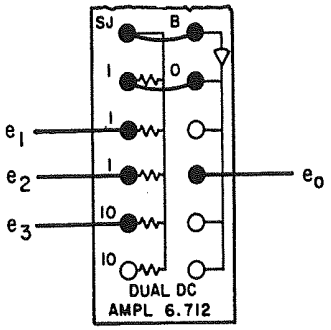
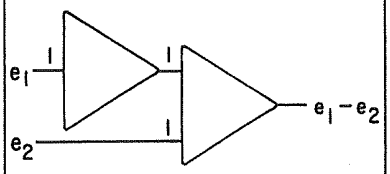
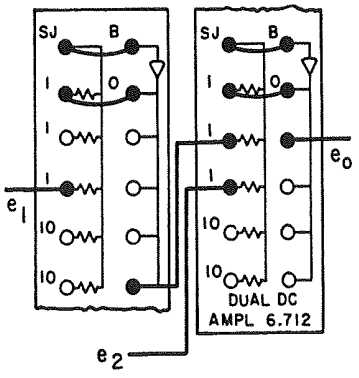
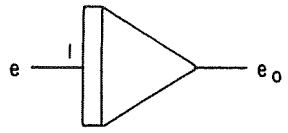
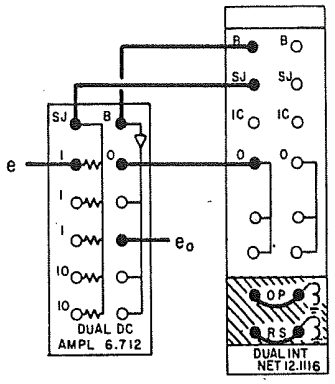
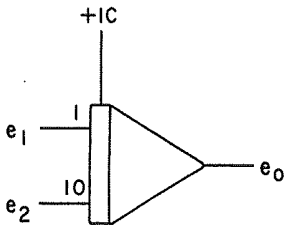
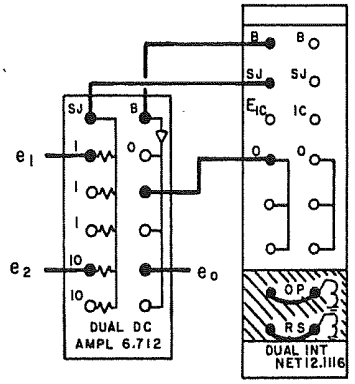
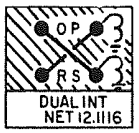
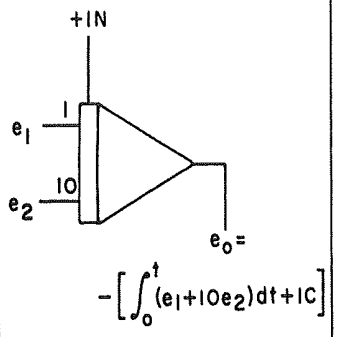
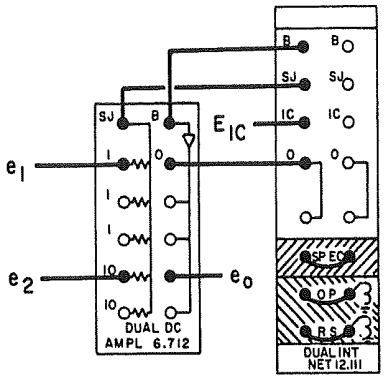
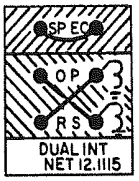
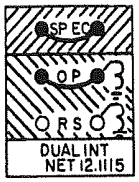
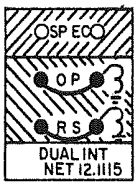
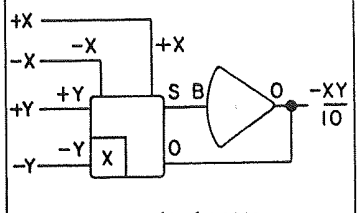
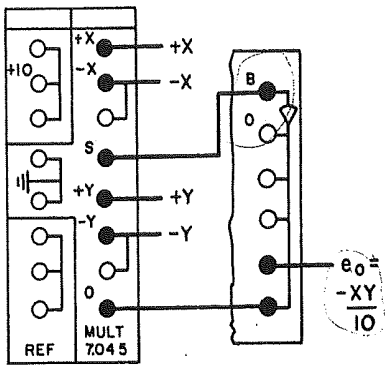
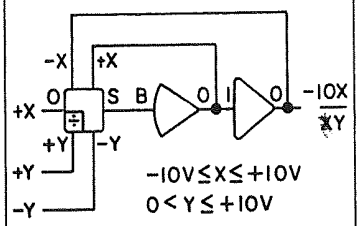
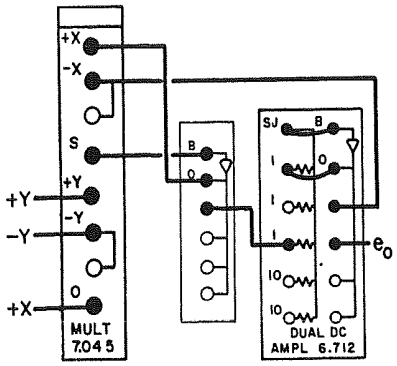
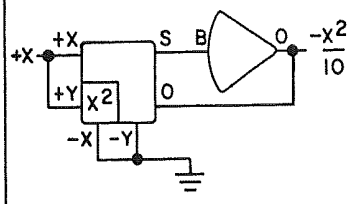
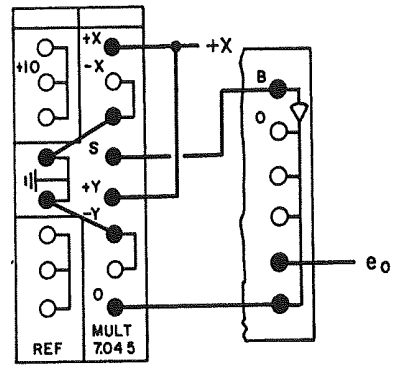
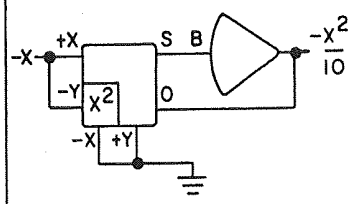
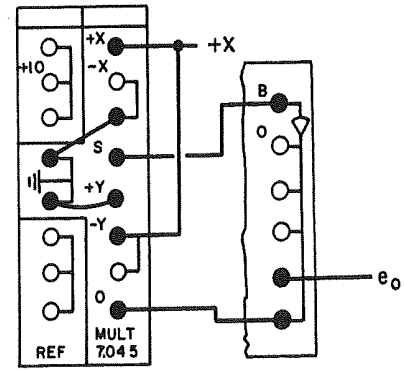
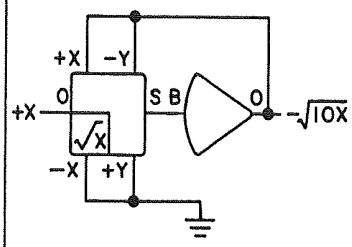
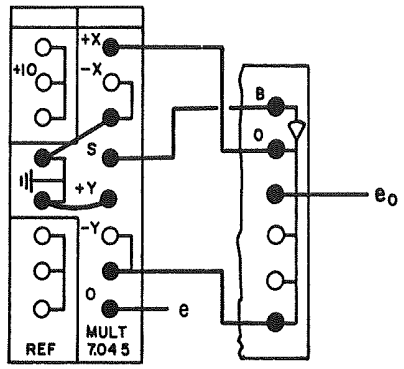
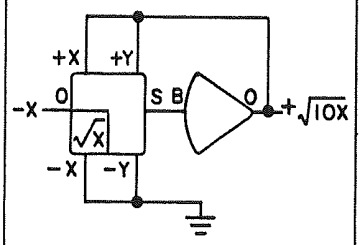
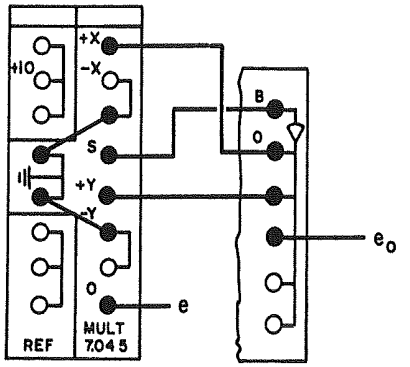
| MULTIPLIERS (CONTINUED) |  |  | GAIN OF 2 |
| |  |  | GAIN OF 1/2 |
| |  |  | ke FOR 0< k < 1 |
| |  |  | ke FOR 1< k < 10 |

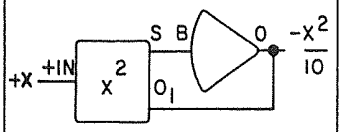
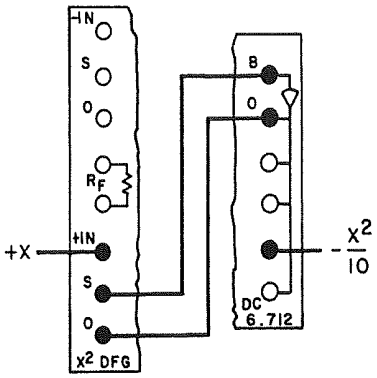
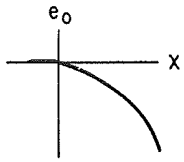
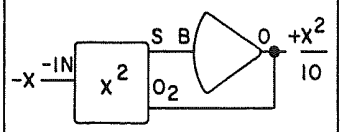
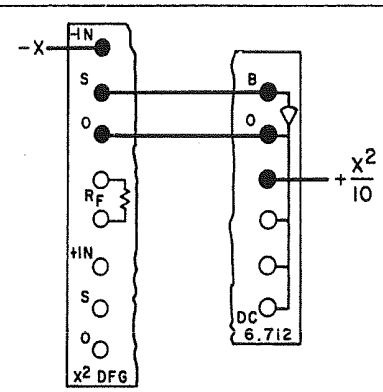
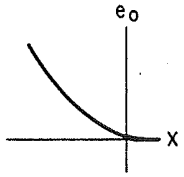
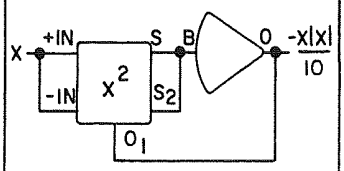
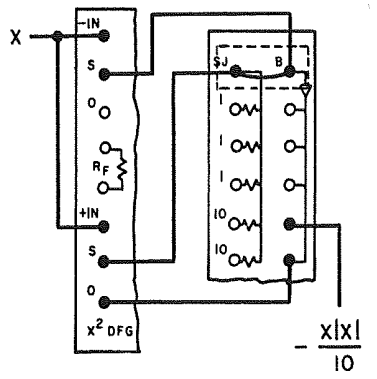
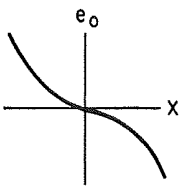
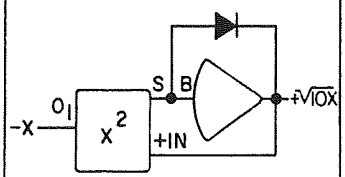
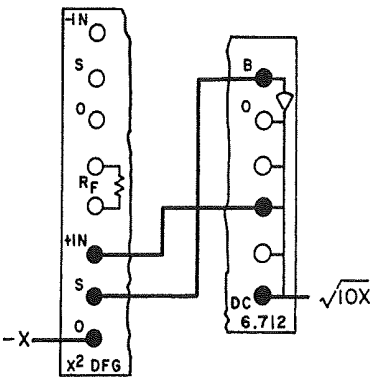
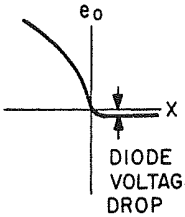
| CIRCUIT DESCRIPTION | COMPUTER SYMBOL | PATCHING | COMMENTS |
|---|---|---|---|
| MULTIPLIERS (CONTINUED) |  |  | 2ke FOR 0< k<1 |
| |  |  | ke FOR 1< k |
| ADDITION |  |  | TYPICAL SUMMATION CIRCUIT |
| SUBTRACTION |  |  | TYPICAL SUBTRACTION CIRCUIT |

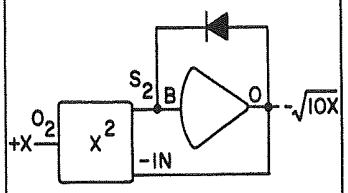
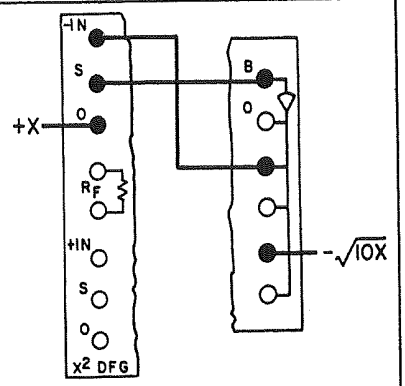
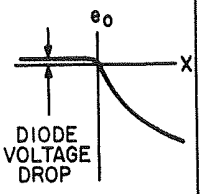
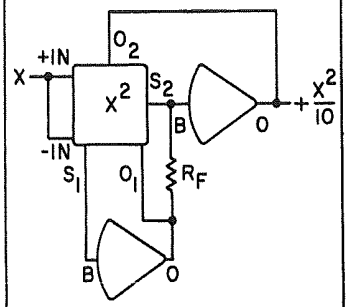
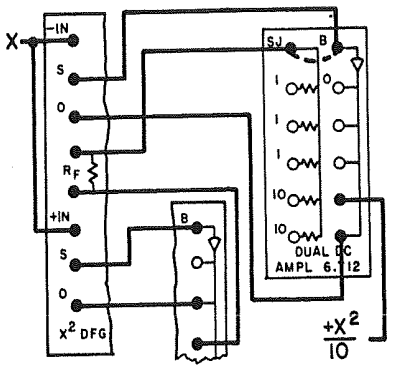
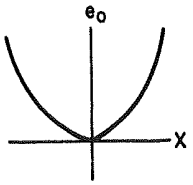
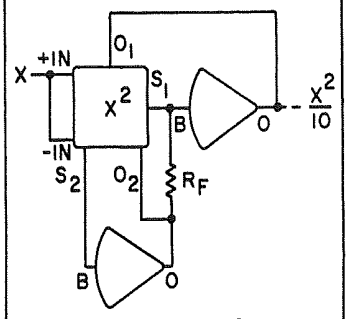
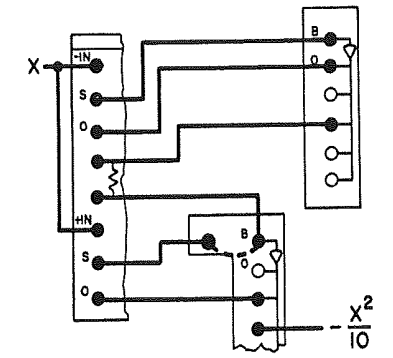
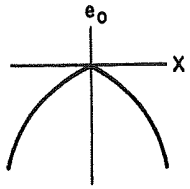
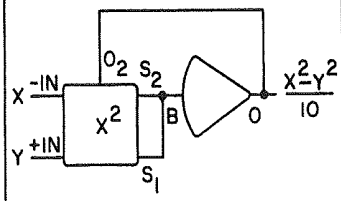
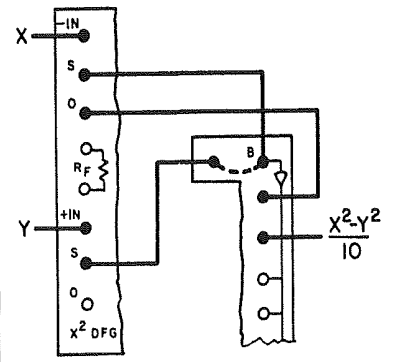
| CIRCUIT DESCRIPTION | COMPUTER SYMBOL | PATCHING | COMMENTS |
|---|---|---|---|
| DUAL INTEGRATOR NETWORK 12.1116 |  $e_o = -\int_o^t (e)\,dt$ |  | BASIC INTEGRATOR CIRCUIT |
| |  $e_o = -\left[\int_o^t (e_1 + 10e_2)\,dt + IC\right]$ |  | TYPICAL SUMMING INTEGRATOR CIRCUIT |
| | AS REQUIRED |  REMAINDER OF PATCHING AS REQUIRED. | INTEGRATOR IS IN RESET WHEN COMPUTER IS IN OPERATE; INTEGRATOR IS IN OPERATE WHEN COMPUTER IS IN RESET (SPECIAL) |
| | AS REQUIRED | REMAINDER OF PATCHING AS REQUIRED. | INTEGRATOR IS IN OPERATE WHEN COMPUTER IS IN OPERATE; INTEGRATOR IS IN HOLD WHEN COMPUTER IS IN HOLD OR RESET (SPECIAL) |

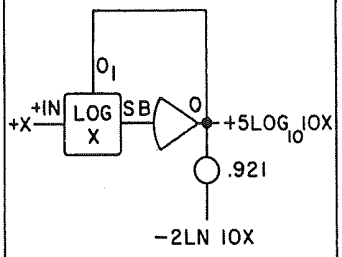
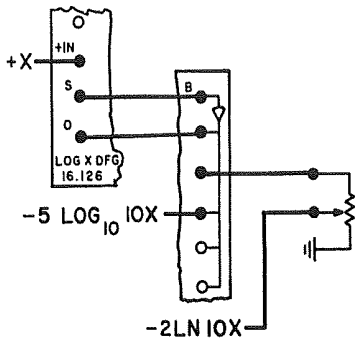
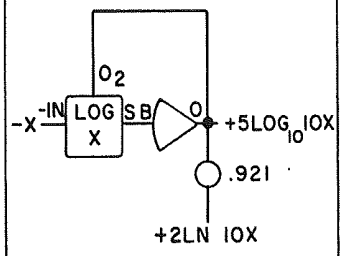
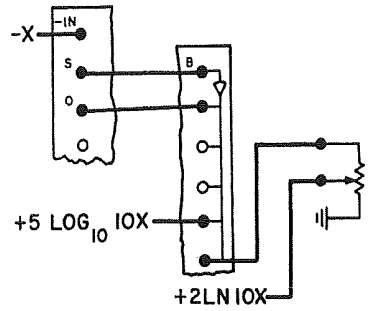
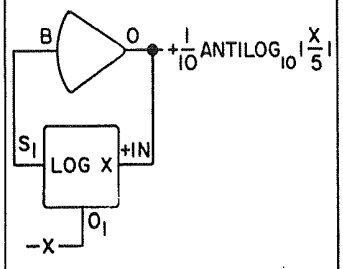
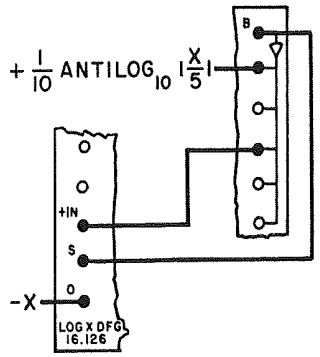
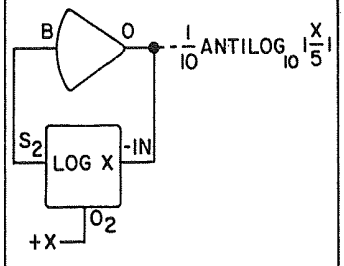
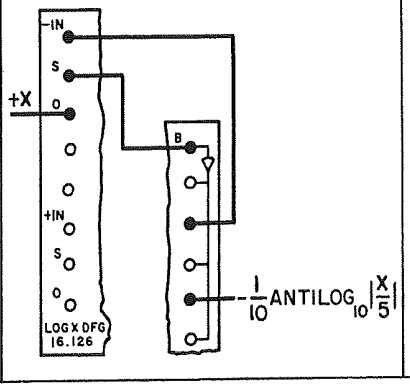
| CIRCUIT DESCRIPTION | COMPUTER SYMBOL | PATCHING | COMMENTS |
|---|---|---|---|
| REPETITIVE OPERATION INTEGRATOR NETWORK 12.1115 |  |  | TYPICAL SUMMING INTEGRATOR CIRCUIT (STANDARD) |
| | AS REQUIRED |  <br>REMAINDER OF PATCHING AS REQUIRED | INTEGRATOR IN RESET WHEN COMPUTER IN OPERATE; INTEGRATOR IN OPERATE WHEN COMPUTER IN RESET<br>(SPECIAL) |
| | AS REQUIRED |  <br>REMAINDER OF PATCHING AS REQUIRED | INTEGRATOR IN OPERATE WHEN COMPUTER IN OPERATE; INTEGRATOR IN HOLD WHEN COMPUTER IS IN HOLD OR RESET<br>(SPECIAL) |
| | AS REQUIRED |  <br>REMAINDER OF PATCHING AS REQUIRED | INTEGRATOR REMAINS IN REAL TIME WHEN COMPUTER IS IN REP-OP<br>(SPECIAL) |

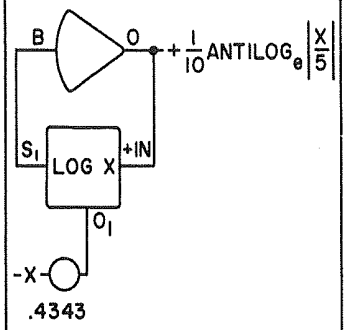
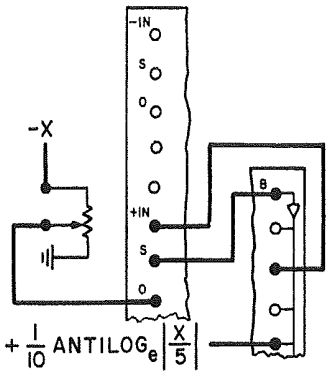
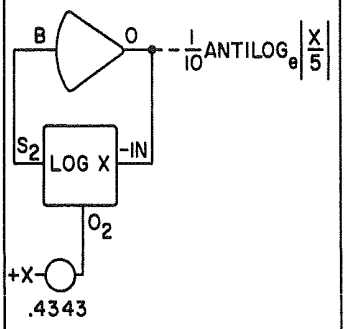
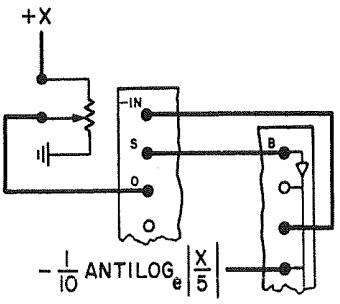
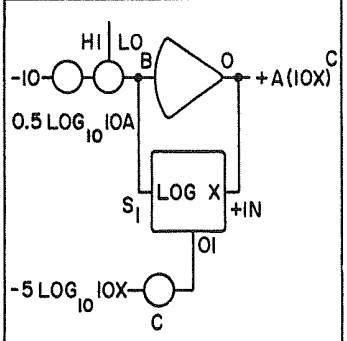
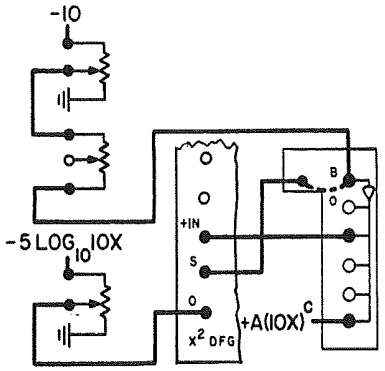
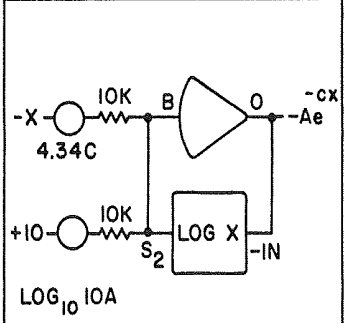
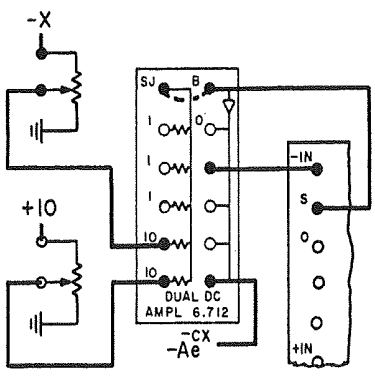
| CIRCUIT DESCRIPTION | COMPUTER SYMBOL | PATCHING | COMMENTS |
|---|---|---|---|
| QUARTER-SQUARE MULTIPLIER |  <br>$-10V \leq X \leq +10V$<br>$-10V \leq Y \leq +10V$ |  | $\frac{X \cdot Y}{10}$ |
| |  <br>$-10V \leq X \leq +10V$<br>$0 < Y \leq +10V$ |  | $\frac{10X}{Y}$<br>$0 < Y \leq +10$ |
| |  <br>$0 \leq X \leq +10V$ |  | $X^2$ POSITIVE INPUT |
| |  |  | $X^2$ NEGATIVE INPUT |

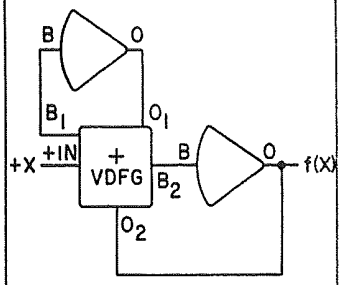
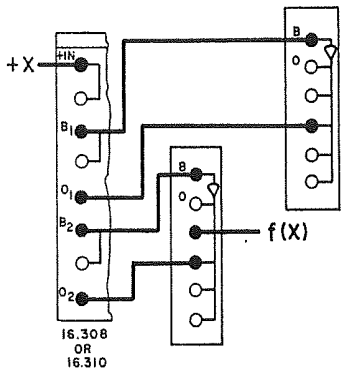
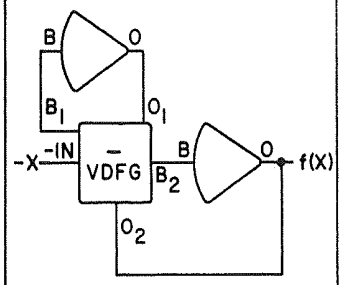
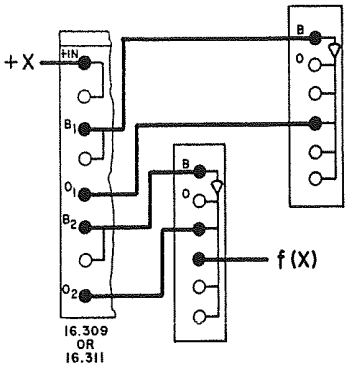
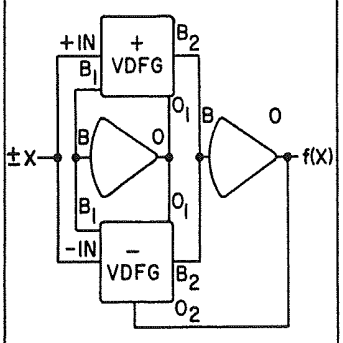
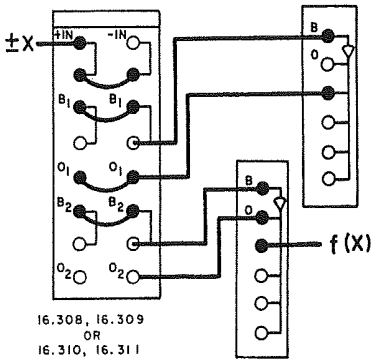
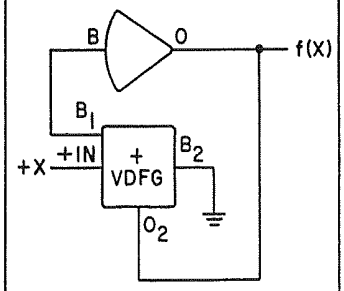
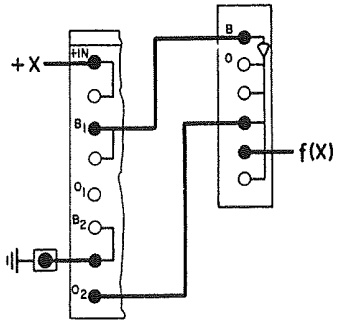
| CIRCUIT DESCRIPTION | COMPUTER SYMBOL | PATCHING | COMMENTS |
|---|---|---|---|
| QUARTER-SQUARE MULTIPLIER |  |  | $\sqrt{X}$<br>POSITIVE INPUT |
| |  |  | $\sqrt{X}$<br>NEGATIVE INPUT |
| | | | |

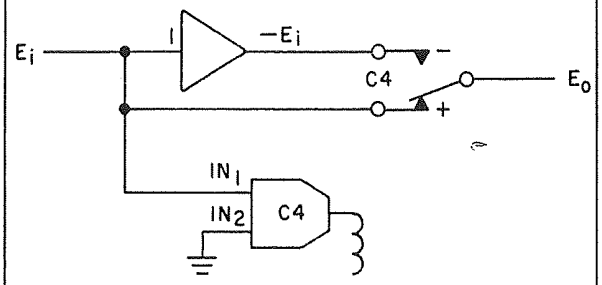
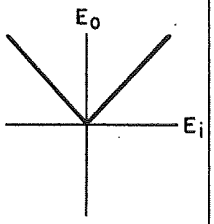
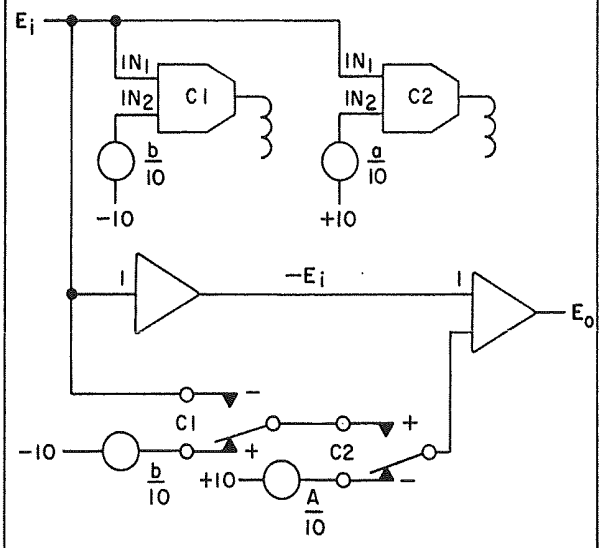
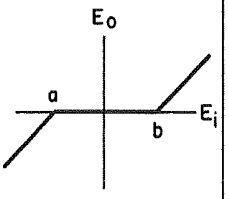
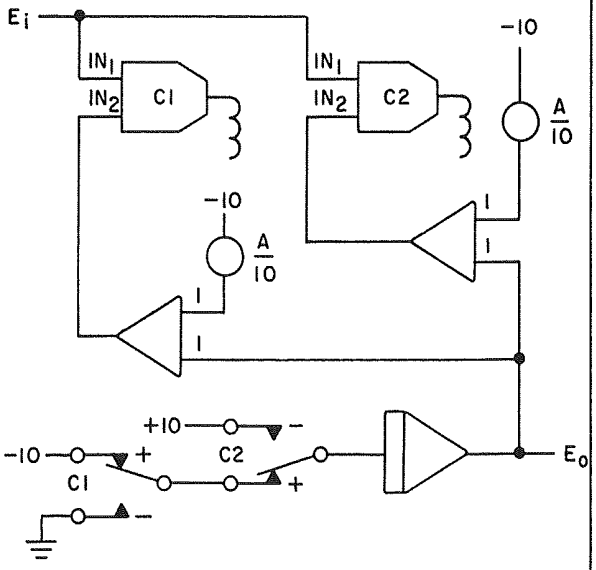
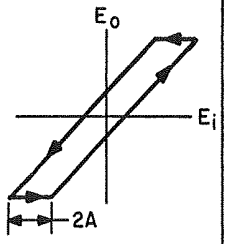
| CIRCUIT DESCRIPTION | COMPUTER SYMBOL | PATCHING | COMMENTS |
|---|---|---|---|
| 16.101 $X^2$ DFG CIRCUITS |   $0 \leq X \leq +10$ |   | $X^2$ POSITIVE INPUT   |
| |   $-10 \leq X \leq 0$ |   | $X^2$ NEGATIVE INPUT   |
| |   $-10 \leq X \leq +10$ |   | $X^2$ BI-POLAR INPUT/OUTPUT   |
| |   $-10 \leq X \leq 0$ |   | $\sqrt{X}$ NEGATIVE INPUT   |

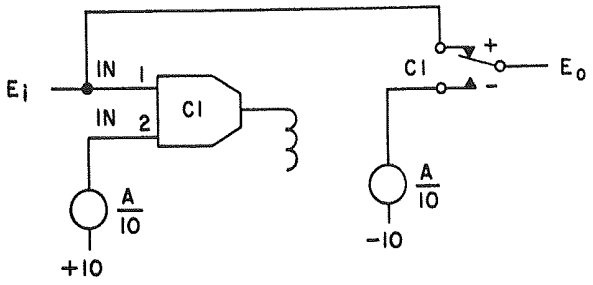
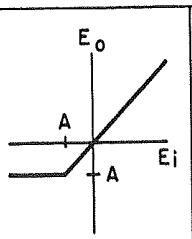
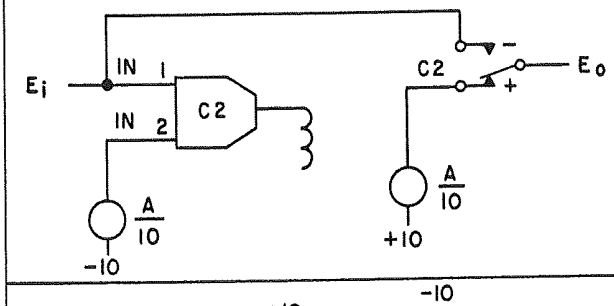
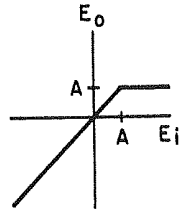
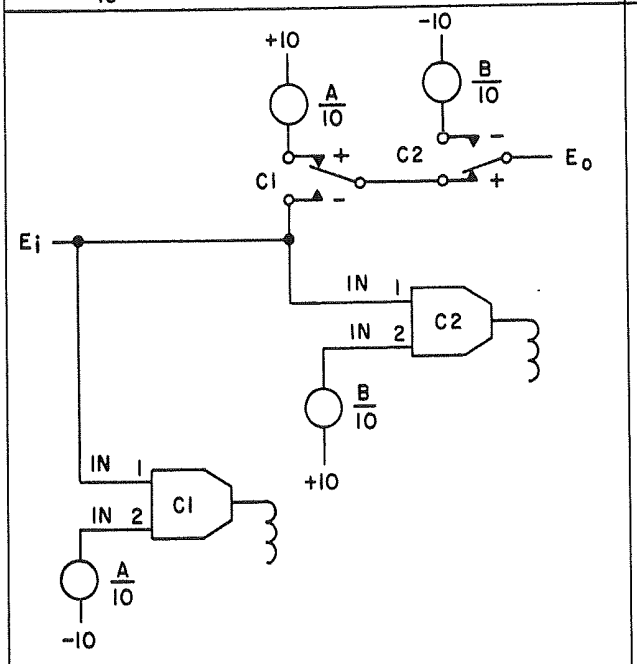
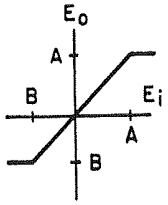
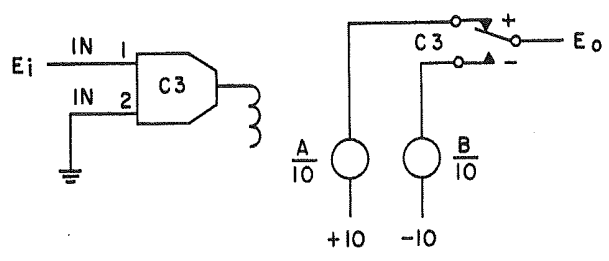
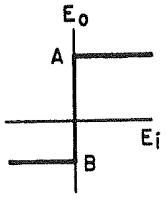
| CIRCUIT DESCRIPTION | COMPUTER SYMBOL | PATCHING | COMMENTS |
|---|---|---|---|
| 16.101 $X^2$ DFG CIRCUITS (CONTINUED) |  $0 \le X \le +10$ |  | $\sqrt{X}$ POSITIVE INPUT  |
| |  $-10 \le X \le +10$ |  | $X^2$ BI-POLAR INPUT POSITIVE OUTPUT  |
| |  $-10 \le X \le +10$ |  | $X^2$ BI-POLAR INPUT NEGATIVE OUTPUT  |
| |  |  | $X^2 - Y^2$ X INPUT NEGATIVE Y INPUT POSITIVE |

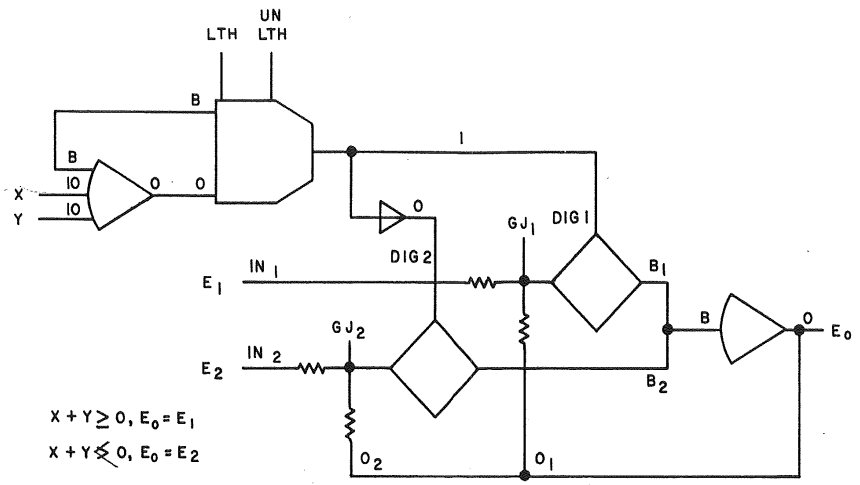
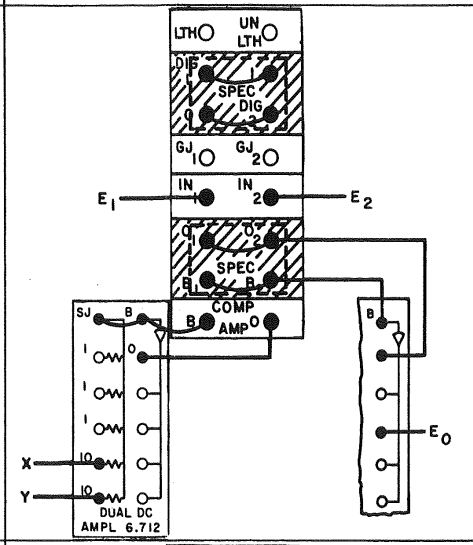
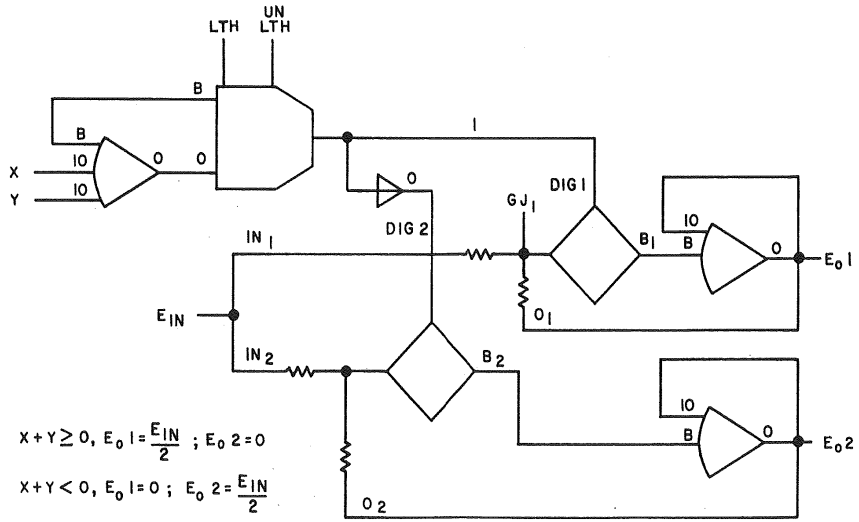
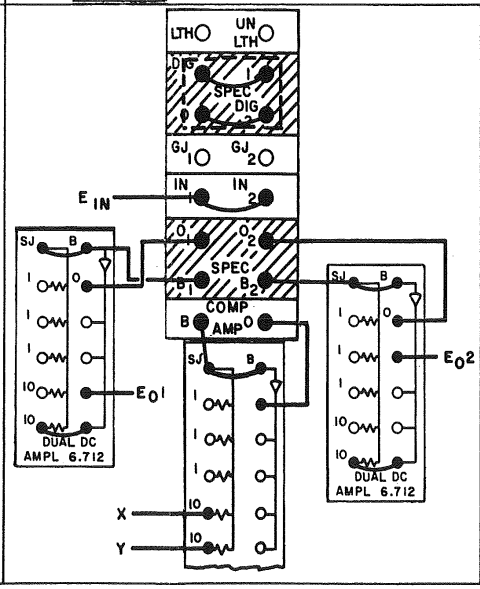
| CIRCUIT DESCRIPTION | COMPUTER SYMBOL | PATCHING | COMMENTS |
|---|---|---|---|
| 16.126 LOG X DFG CIRCUITS |  |  | LOG X POSITIVE INPUT (BASE 10 AND NATURAL) |
| |  |  | LOG X NEGATIVE INPUT (BASE 10 AND NATURAL) |
| |  |  | ANTILOG X NEGATIVE INPUT (BASE 10) |
| |  |  | ANTILOG X POSITIVE INPUT (BASE 10) |

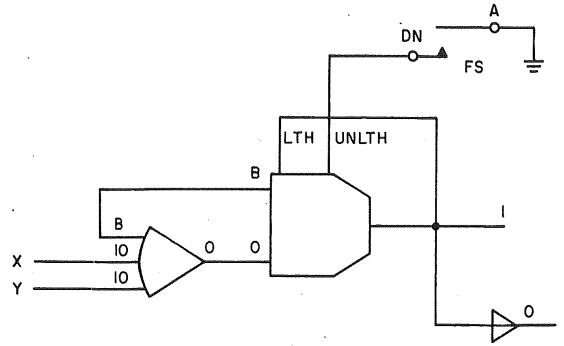
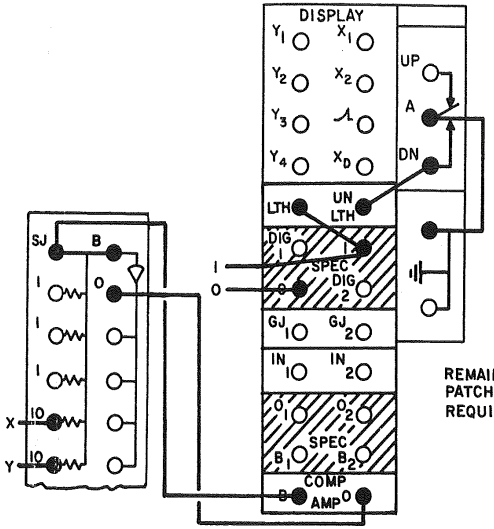
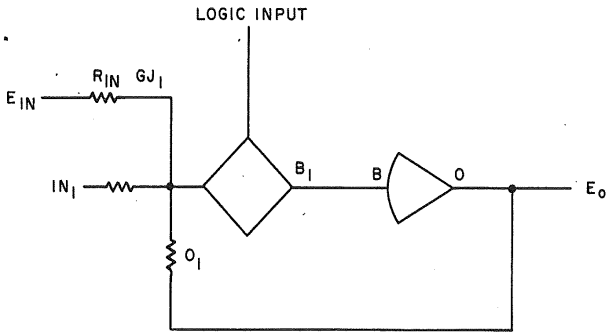
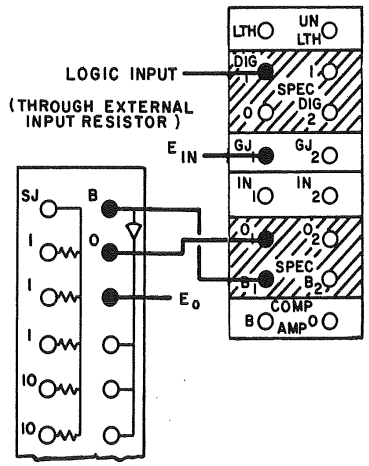
| CIRCUIT DESCRIPTION | COMPUTER SYMBOL | PATCHING | COMMENTS |
|---|---|---|---|
| 16.126 LOG X DFG CIRCUITS (CONTINUED) |  |  | ANTILOG X NEGATIVE INPUT (NATURAL BASE) |
| |  |  | ANTILOG X POSITIVE INPUT (NATURAL BASE) |
| |  |  | $X^C$ NEGATIVE INPUT |
| |  |  | EXPONENTIAL FUNCTION |

| CIRCUIT DESCRIPTION | COMPUTER SYMBOL | PATCHING | COMMENTS |
|---|---|---|---|
| VDFG CIRCUITS ( FIXED AND VARIABLE BREAKPOINT UNITS ) |  $0 \leq X \leq +10$ |  | POSITIVE X |
| |  $-10 \leq X \leq 0$ |  | NEGATIVE X |
| |  $-10 \leq X \leq +10$ |  | BI-POLAR X |
| |  |  | POSITIVE X, f (X) MONOTONIC AND INCREASING ($X^3$, Tan X, ETC.) |

| CIRCUIT DESCRIPTION | COMPUTER SYMBOL | COMMENTS | |
|---|---|---|---|
| RELAY COMPARATOR 6.143 |  |  | ABSOLUTE VALUE |
| |  |  | DEAD ZONE |
| |  |  | BACKLASH |

| CIRCUIT DESCRIPTION | COMPUTER SYMBOL | COMMENTS | |
|---|---|---|---|
| RELAY COMPARATOR 6.143 (CONTINUED) |  |  | |
| |  |  | |
| |  |  | LIMITS |
| |  |  | BANG-BANG |

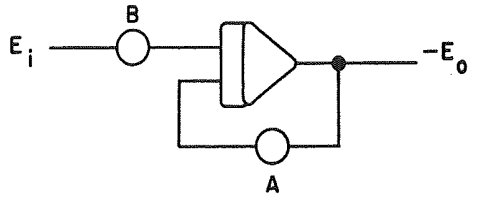
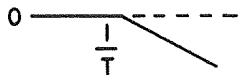
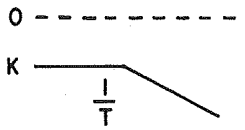
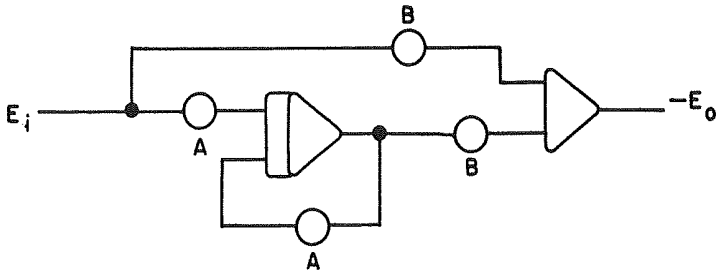
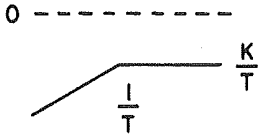
| CIRCUIT DESCRIPTION | COMPUTER SYMBOL | PATCHING | COMMENTS |
|---|---|---|---|
| ELECTRONIC COMPARATOR 40.538 |  |  | ELECTRONIC SELECTOR SWITCH |
| |  |  | ELECTRONIC DISTRIBUTOR SWITCH |

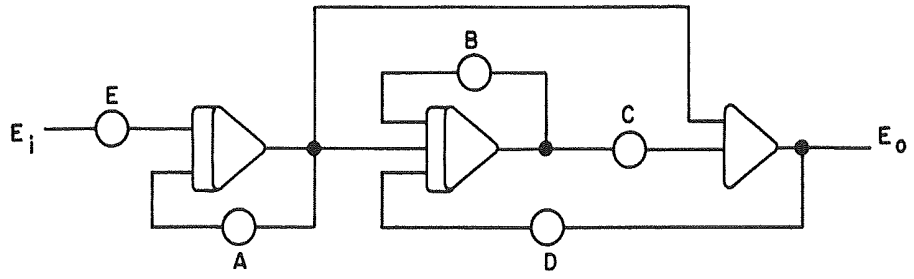
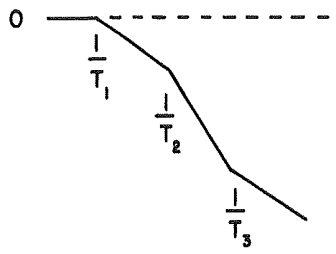
| CIRCUIT DESCRIPTION | COMPUTER SYMBOL | PATCHING | COMMENTS |
|---|---|---|---|
| ELECTRONIC COMPARATOR 40.538 (CONTINUED) |  |  <br>REMAINDER OF PATCHING AS REQUIRED. | SELF-LATCHING CIRCUIT. WHEN X+Y>0, DIG 1 TERMINAL GOES TO +5 VOLTS. OUTPUT REMAINS IN THIS STATE UNTIL MANUALLY RESET WITH FUNCTION SWITCH. |
| |  <br>WHEN THE LOGIC INPUT IS AT BINARY ONE,<br>$E_o = -E_{IN} \frac{Rfb}{R_{IN}}$ WHERE Rfb = IOK |  <br>REMAINDER OF PATCHING AS REQUIRED. | COMPARATOR CIRCUIT FOR A GAIN OTHER THAN UNITY THROUGH AN ELECTRONIC SWITCH. |

APPENDIX III

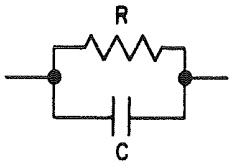
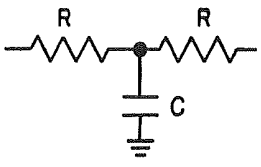
AMPLIFIER CIRCUITS FOR SIMULATING TRANSFER FUNCTIONS

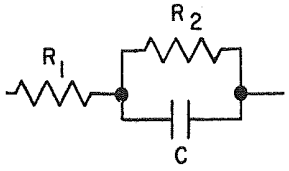
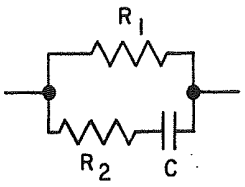
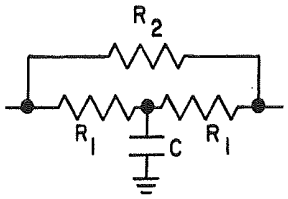
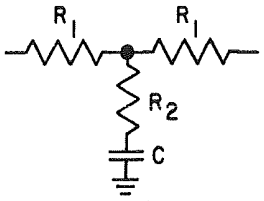
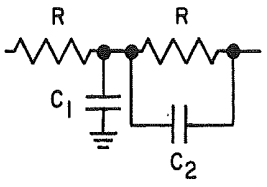
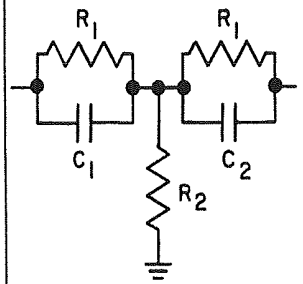
(a) The following Table contains examples of amplifier circuits for simulating transfer functions. A more complete listing may be found in Jackson, A.S.: "Analog Computation", McGraw-Hill Book Company, Inc., New York, 1960.

| NO. | BODE PLOT | TRANSFER FUNCTION | TIME CONSTANTS | GAINS |
|---|---|---|---|---|
| |   | | | |
| 1 |   | $\frac{1}{1+Tp}$ | $T = \frac{1}{A}$ | $A = B = \frac{1}{T}$ |
| 2 |   | $\frac{K}{1+Tp}$ | $T = \frac{1}{A}$ $K = \frac{B}{A}$ | $A = \frac{1}{T}$ $B = AK$ |
| |   | | | |
| 3 | | $\frac{Tp}{1+Tp}$ | $T = \frac{1}{A}$ | $A = \frac{1}{T}$ $B = 1$ |
| 4 |   | $\frac{Kp}{1+Tp}$ | $T = \frac{1}{A}$ $K = BT$ | $A = \frac{1}{T}$ $B = AK$ |

| NO. | BODE PLOT | TRANSFER FUNCTION | TIME CONSTANTS | GAINS |
|---|---|---|---|---|
| |   | | | |
| 5 |   | $\frac{1+T_3p}{(1+T_1p)(1+T_2p)}$ | $T_1 = \frac{1}{A}$ $T_2 = \frac{1}{B-CD}$ $T_3 = \frac{1}{B-C}$ | $A = \frac{1}{T_1}$ $B = C + \frac{1}{T_3}$ $D = \frac{1}{C}\left(\frac{1}{T_3} - \frac{1}{T_2}\right)+1$ $E = \frac{T_3}{T_1T_2}$ |

(b) The following table contains the short-circuit admittance and component values for some useful networks for simulating transfer functions. A more extensive listing may be found in Jackson, A.S.: "Analog Computation", and Fifer, S.: "Analog Computation". (See Bibliography.)

| NO. | $Y_{ss}$ SHORT-CKT. ADMITTANCE | NETWORK | |
|---|---|---|---|
| 1. | $\frac{1}{A}$ | | $A = R$ |
| 2. | $\frac{1 + pT}{A}$ |   | $A = R$ $T = RC$ |
| 3. | $\frac{1}{A\,(1 + pT)}$ |   | $A = 2R$ $T = \frac{RC}{2}$ |

| NO. | Yss<br>SHORT-CKT. ADMITTANCE | NETWORK | |
|---|---|---|---|
| 4. | $\frac{1}{A}\left(\frac{1+pT}{1+p\theta T}\right)$<br>$\theta < 1$ |  | $A = R_1 + R_2$<br>$T = R_2 C$<br>$\theta = \frac{R_1}{R_1 + R_2}$ |
| 5. | $\frac{1}{A}\left(\frac{1+pT}{1+p\theta T}\right)$<br>$\theta < 1$ |  | $A = R_1$<br>$T = (R_1 + R_2)\ C$<br>$\theta = \frac{R_2}{R_1 + R_2}$ |
| 6. | $\frac{1}{A}\frac{1+p\theta T}{1+pT}$<br>$\theta < 1$ |  | $A = \frac{2R_1 R_2}{R_1 + R_2}$<br>$T = \frac{R_1 C}{2}$ $\theta = \frac{2R_1}{2R_1 + R_2}$ |
| 7. | $\frac{1}{A}\frac{1+p\theta T}{1+pT}$<br>$\theta < 1$ |  | $A = 2R_1$<br>$T = (R_2 + \frac{R_1}{2})\ C$<br>$\theta = \frac{2R_2}{2R_2 + R_1}$ |
| 8. | $\frac{1}{A}\frac{1+p\theta T}{1+pT}$<br>$\theta < 1$ |  | $A = 2R$<br>$T = \frac{R}{2}(C_1 + C_2)$<br>$\theta = \frac{2C_2}{C_1 + C_2}$ |
| 9. | $\frac{1}{A}\left(\frac{(1+pT_1)(1+pT_3)}{(1+pT_2)}\right)$<br>$T_2 \leqslant T_1 \leqslant T_3$ |  | $A = 2R_1 + \frac{R_1^2}{R_2}$<br>$T_1 = R_1 C_1$<br>$T_2 = \left[\frac{R_1 R_2}{R_1 + 2R_2}\right](C_1 + C_2)$ |

APPENDIX IV

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