80L286

Low-Power High-Performance Microprocessor with Memory Management and Protection

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

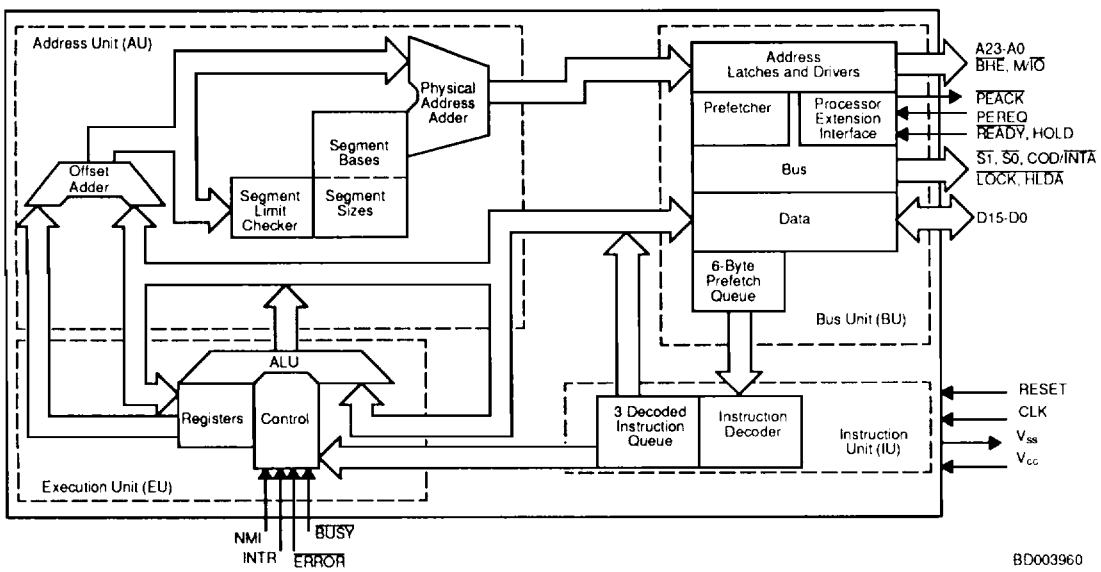
- **High-performance processor (up to 13.3 times iAPX 86 when using the 16-MHz 80L286)**
- **Identical to the 80286 except consumes less power**
- **Available in cost-effective Plastic Leaded Chip Carrier (PLCC) package**
- **Socketed PLCC footprint is compatible with socketed LCC and PGA footprints**
- **Surface-mountable PLCC for high density board utilization**
- **8-, 10-, and 12.5- and16-MHz operation**
- **Large address space**
  - 16-Mb physical
  - 1-Gb virtual memory per task
- **Integrated memory management, four-level memory protection and support for virtual memory and operating systems**

GENERAL DESCRIPTION

The 80L286 is an advanced, high performance microprocessor, identical to the 80286, except consumes less power. Its reduced power enables the 80L286 to be packaged in low-cost, Plastic Leaded Chip Carrier (PLCC) without a heat sink or heat spreader. Cooler operation also enhances reliability. The PLCC package can be surface-mounted or socketed. The footprint of the socketed PLCC package is identical to the socketed LCC or PGA packages so no board layout change is needed. The 80L286 is available in 8-, 10-, 12-, and 16-MHz speeds and is fully compatible with the 82C288 Bus Controller and the 82284 Clock Driver functions.

The 80L286 is upward compatible with iAPX 86 and 88 software. Using iAPX real address mode, the 80L286 is object code compatible with existing iAPX 86, 88 software. In protected virtual address mode, the 80L286 is source code compatible with iAPX 86, 88 software and may require upgrading to use virtual addresses supported by the 80L286's integrated memory management and protection mechanism. Both modes operate at full 80L286 performance and execute a superset of the iAPX 86 and 88 instructions.

BLOCK DIAGRAM

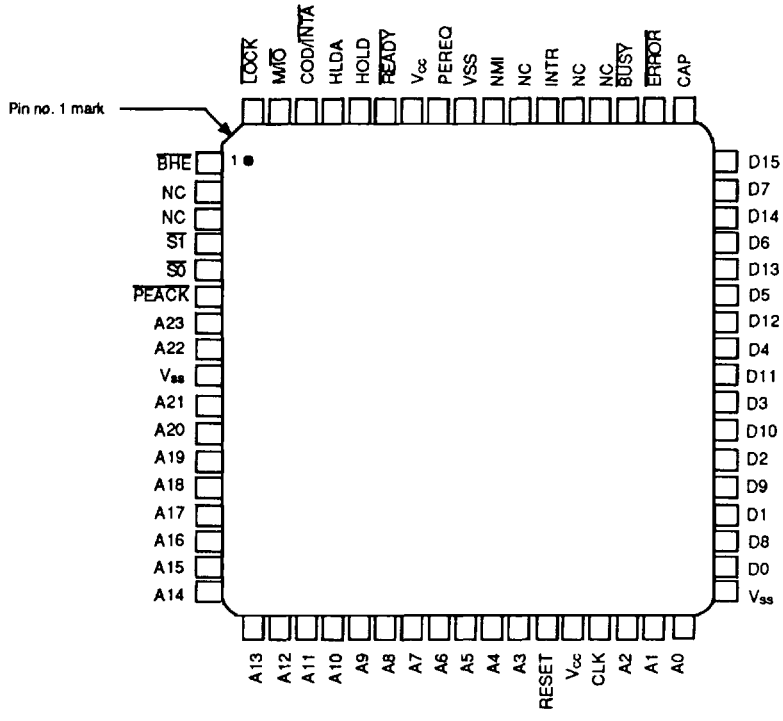


GENERAL DESCRIPTION (continued)

The 80L286 provides special operations to support the efficient implementation and execution of operating systems. For example, one instruction can end execution of one task, save its state, switch to a new task, load its state, and start execution of the new task. The 80L286 also supports virtual memory systems by providing a segment-not-present exception and restartable instructions.

CONNECTION DIAGRAM
Top View

Plastic Leaded Chip Carrier
(PL 068)



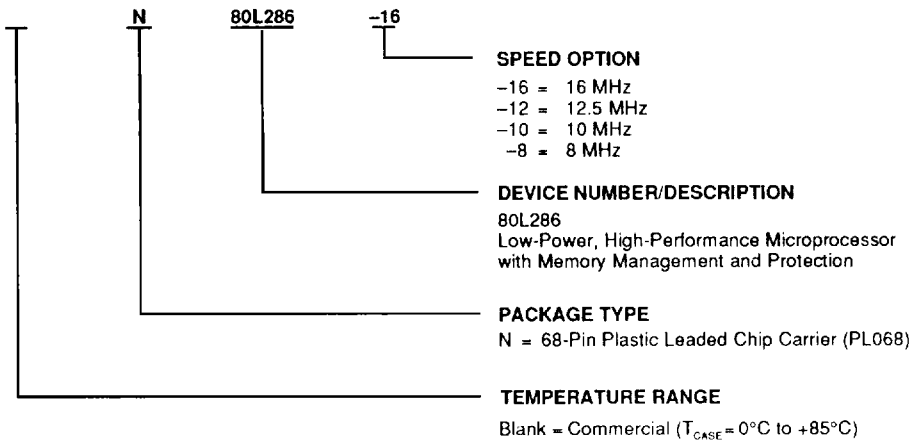
CD010641

As viewed from top of package (PC side of component board)

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
N	80L286-16 80L286-12 80L286-10 80L286-8

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

CLK

System Clock (Input; Active High)

System Clock provides the fundamental timing for 80L286 systems. It is a 16 MHz signal divided by two inside the 80L286 to generate the 8 MHz processor clock. The internal divide-by-two circuitry can be synchronized to an external clock generator by a Low-to-High transition on the RESET input.

D0–D15

Data Bus (Input/Output; Active High)

Data Bus inputs data during memory, I/O, and interrupt acknowledge read cycles; outputs data during memory and I/O write cycles. The data bus is active High and floats to three-state OFF during bus hold acknowledge.

A23–A0

Address Bus (Output; Active High)

Address Bus outputs physical memory and I/O port addresses. A0 is Low when data is to be transferred on pins D7–D0. A23–A16 are Low during I/O transfers. The address bus is active High and floats to three-state OFF during bus hold acknowledge.

$\overline{BHE}$

Bus High Enable (Output; Active Low)

Bus High Enable indicates transfer of data on the upper byte of the data bus D15-D8. Eight-bit oriented devices assigned to the upper byte of the data bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is active Low and floats to three-state OFF during bus hold acknowledge.

$\overline{BHE}$ and A_0 Encodings

$\overline{BHE}$ Value	A0 Value	Function
0	0	Word transfer
0	1	Byte transfer on upper half of data bus (D15–D8)
1	0	Byte transfer on lower half of data bus (D7–D0)
1	1	Reserved

$\overline{S1}$, $\overline{S0}$

Bus Cycle Status (Output; Active Low)

Bus Cycle Status indicates initiation of a bus cycle and, along with M/$\overline{IO}$ and COD/$\overline{INTA}$, defines the type of bus cycle. The bus is in a Ts state whenever one or both are Low. $\overline{S1}$ and $\overline{S0}$ are active Low and float to three-state OFF during bus hold acknowledge.

80L286 Bus Cycle Status Definition

COD/$\overline{INTA}$	M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	Bus cycle initiated
0 (Low)	0	0	0	Interrupt acknowledge
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	None; not a status cycle
0	1	0	0	IF A1 = 1 then halt; else shutdown
0	1	0	1	Memory data read
0	1	1	0	Memory data write
0	1	1	1	None; not a status cycle
1 (High)	0	0	0	Reserved
1	0	0	1	I/O Read
1	0	1	0	I/O Write
1	0	1	1	None; not a status cycle
1	1	0	0	Reserved
1	1	0	1	Memory instruction read
1	1	1	0	Reserved
1	1	1	1	None; not a status cycle

M/$\overline{IO}$

Memory/IO Select (Output)

Memory/IO Select distinguishes memory access from I/O access. If High during Ts, a memory cycle or a halt/shutdown cycle is in progress. If Low, an I/O cycle or an interrupt acknowledge cycle is in progress M/$\overline{IO}$ floats to three-state OFF during bus hold acknowledge.

COD/$\overline{INTA}$

Code/Interrupt Acknowledge (Output)

Code/Interrupt Acknowledge distinguishes instruction fetch cycles from memory data read cycles. Also distinguishes interrupt acknowledge cycles from I/O cycles. COD/$\overline{INTA}$ floats to three-state OFF during bus hold acknowledge.

$\overline{LOCK}$

Bus Lock (Output; Active Low)

Bus Lock indicates that other system bus masters are not to gain control of the system bus following the current bus cycle. The $\overline{LOCK}$ signal may be activated explicitly by the "LOCK" instruction prefix or automatically by 80286 hardware during memory XCHG instructions, interrupt acknowledge, or descriptor table access. $\overline{LOCK}$ is active Low and floats to three-state OFF during hold acknowledge.

PIN DESCRIPTION (continued)

$\overline{\text{READY}}$

Bus Ready (Input; Active Low)

Bus Ready terminates a bus cycle. Bus cycles are extended without limit until terminated by $\overline{\text{READY}}$ Low. $\overline{\text{READY}}$ is an active Low synchronous input requiring setup and hold times relative to the system clock be met for correct operation. $\overline{\text{READY}}$ is ignored during bus hold acknowledge.

HOLD, HLDA

Bus Hold Request and Hold Acknowledge (Input/Output; Active High)

Bus Hold Request and Hold Acknowledge control ownership of the 80L286 local bus. The HOLD input allows another local bus master to request control of the local bus. When control is granted, the 80L286 will float its bus drivers to three-state OFF and then active HLDA, thus entering the bus hold acknowledge condition. The local bus will remain granted to the requesting master until HOLD becomes inactive which results in the 80L286 deactivating HLDA and regaining control of the local buys. This terminates the bus hold acknowledge condition. HOLD may be asynchronous to the system clock. These signals are active HIGH.

INTR

Interrupt Request (Input; Active High)

Interrupt Request requests the 80L286 to suspend its current program execution and service a pending external request. Interrupt requests are masked whenever the interrupt enable bit in the flag word is cleared. When the 80L286 responds to an interrupt request, it performs two interrupt acknowledge bus cycles to read an 8-bit interrupt vector that identifies the source of the interrupt. To assure program interruption, INTR must remain active until the first interrupt acknowledge cycle is completed. INTR is sampled at the beginning of each processor cycle and must be active High at least two processor cycles before the current instruction ends in order to interrupt before the next instruction. INTR is level sensitive, active High, and may be asynchronous to the system clock.

NMI

Non-maskable Interrupt Request (Input; Active High)

Non-maskable Interrupt Request interrupts the 80L286 with an internally supplied vector value of 2. No interrupt acknowledge cycles are performed. The interrupt enable bit in the 80L286 flag word does not affect this input. The NMI input is active High, may be asynchronous to the system clock, and is edge triggered after internal synchronization. For proper recognition, the input must have been previously Low for at least four system clock cycles and remain High for at least four system clock cycles.

PEREQ, $\overline{\text{PEACK}}$

Processor Extension Operand Request and Acknowledge (Input/Output)

Processor Extension Operand Request and Acknowledge extends the memory management and protection capabilities of the 80L286 to processor extensions. The PEREQ input requests the 80L286 to perform a data operand transfer for a processor extension. The $\overline{\text{PEACK}}$ output signals the processor extension when the requested operand is being transferred. PEREQ is active High and may be asynchronous to the system clock. $\overline{\text{PEACK}}$ is active Low.

$\overline{\text{BUSY}}$, $\overline{\text{ERROR}}$

Processor Extension Busy and Error (Input; Active Low)

Processor Extension Busy and Error indicate the operating condition of a processor extension to the 80L286. An active $\overline{\text{BUSY}}$ input stops 80L286 program execution on WAIT and some ESC instructions until $\overline{\text{BUSY}}$ becomes inactive (High). The 80L286 may be interrupted while waiting for $\overline{\text{BUSY}}$ to become inactive. An active $\overline{\text{ERROR}}$ input causes the 80L286 to perform a processor extension interrupt when executing WAIT or some ESC instructions. These inputs are active Low and may be asynchronous to the system clock.

RESET

System Reset (Input; Active High)

System Reset clears the internal logic of the 80L286 and is active High. The 80L286 may be reinitialized at any time with a Low-to-High transition on RESET which remains active for more than 16 system clock cycles. During RESET active, the output pins of the 80C286 enter the state shown below:

80L286 Pin State during Reset

Pin Value	Pin Names
1 (High)	$\overline{S0}$, $\overline{S1}$, $\overline{\text{PEACK}}$, A23–A0, $\overline{\text{BHE}}$, $\overline{\text{LOCK}}$
0 (Low)	M/$\overline{IO}$, COD/$\overline{\text{INTA}}$, HLDA
Three-state OFF	D15–D0

Operation of the 80L286 begins after a High-to-Low transition on RESET. The High-to-Low transition of RESET must be synchronous to the system clock. Approximately 50 system clock cycles are required by the 80L286 for internal initializations before the first bus cycle to fetch code from the power-on execution address is performed.

PIN DESCRIPTION (continued)

A Low-to-High transition of RESET synchronous to the system clock, will begin a new processor cycle at the next High-to-Low transition of the system clock. The Low-to-High transition of RESET may be asynchronous to the system clock; however, in this case it cannot be predetermined which phase of the processor clock will occur during the next system period. Synchronous Low-to-High transitions of RESET are only required for systems where the processor clock must be phase synchronous to another clock.

V_{SS}
System Ground (Input)

System Ground: 0 V.

V_{CC}
System Power (Input)

System Power: +5-V power supply.

CAP
Substrate Filter Capacitor (Input; Active High)

Substrate Filter Capacitor: a 0.047 µF ±20% 12 V capacitor must be connected between this pin and ground. This capacitor filters the output of the internal substrate bias generator. A maximum DC leakage current of 1 µA is allowed through the capacitor.

For correct operation of the 80L286, the substrate bias generator must charge this capacitor to its operating voltage. The capacitor charge-up time is 5 ms (max.) after V_{CC} and CLK reach their specified AC and DC parameters. RESET may be applied to prevent spurious activity by the CPU during this time. After this time, the 80L286 processor clock can be phase synchronized to another clock by pulsing RESET Low synchronous to the system clock.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... −1.0 V to 7.0 V
Power Dissipation ..... 2.89 Watts

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Operating Voltage Range ..... +4.75 V to +5.25 V
Case Operating Temperature Range .. 0°C to +85°C

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range

(T_{CASE} = 0°C to 85°C, V_{CC} = 5 V ±5%)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input Low Voltage		−0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{ILC}	CLK Input Low Voltage		−0.5	.6	V
V_{IHC}	CLK Input High Voltage		3.8	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA	2.4		V
I_{LI}	Input Leakage Current	0 V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0.45 V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	T_C = 0°C		550	mA
		T_C = 85°C		475	mA
C_{CLK}	CLK Input Capacitance	F_C = 1 MHz		20	pF
C_{IN}	Other Input Capacitance	F_C = 1 MHz		10	pF
C_O	Input/Output Capacitance	F_C = 1 MHz		20	pF
I_{LO}	Output Leakage Current	0 V ≤ V_{OUT} < 0.45 V		±1	mA
I_{IL}	Input Sustaining Current on $\overline{\text{BUSY}}$ and $\overline{\text{ERROR}}$ pins	V_{IN} = 0 V	30	500	µA
I_{LCR}	Input CLK Leakage Current	0.45 ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LCR}	Input CLK Leakage Current	0 V ≤ V_{IN} ≤ 0.45 V		±1	mA

Note: Low temperature is worst case.

SWITCHING CHARACTERISTICS

V_{CC} = +5 V ±5%, T_{CASE} = 0°C to +85°C

AC timings are referenced to 0.8 V and 2.0 V points of the signals as illustrated in data sheet waveforms, unless otherwise noted.

Parameter Symbol	Parameter Description	Test Conditions	8 MHz		10 MHz		Unit
			Min.	Max.	Min.	Max.	
1	System Clock (CLK) Period		62	125	50	125	ns
2	System Clock (CLK) Low Time	@ 1.0 V	15	100	12	109	ns
3	System Clock (CLK) High Time	@ 3.6 V	25	110	16	113	ns
17	System Clock (CLK) RISE Time	1.0 V to 3.6 V		10		8	ns
18	System Clock (CLK) FALL Time	3.6 V to 1.0 V		10		8	ns
4	Asynchronous Inputs SETUP Time	(Note 1)	20		20		ns
5	Asynchronous Inputs HOLD Time	(Note 1)	20		20		ns
6	RESET SETUP Time		28		23		ns
7	RESET HOLD Time		5		5		ns
8	Read Data SETUP Time		10		8		ns
9	Read Data HOLD Time		8		8		ns
10	$\overline{\text{READY}}$ SETUP Time		38		26		ns
11	$\overline{\text{READY}}$ HOLD Time		25		25		ns
12	Status/$\overline{\text{PEACK}}$ Valid Delay	(Notes 2, 3)	1	40	–	–	ns
12A	Status/$\overline{\text{PEACK}}$ Active Delay	(Notes 2, 3)	–	–	1	22	ns
12B	Status/$\overline{\text{PEACK}}$ Inactive Delay	(Notes 2, 3)	–	–	1	30	ns
13	Address Valid Delay	(Notes 2, 3)	1	60	1	35	ns
14	Write Data Valid Delay	(Notes 2, 3)	0	50	0	30	ns
15	Address/Status/Data Float Delay	(Notes 2, 4)	0	50	0	47	ns
16	HLDA Valid Delay	(Notes 2, 3)	0	50	0	47	ns
19	Address Valid to Status SETUP Time	(Notes 3, 5, 6)	38		27		ns

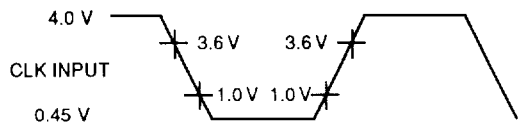
SWITCHING CHARACTERISTICS (continued)

Parameter Symbol	Parameter Description	Test Conditions	12.5 MHz		16 MHz		Unit
			Min.	Max.	Min.	Max.	
1	System Clock (CLK) Period		40	125	31	125	ns
2	System Clock (CLK) Low Time	@ 1.0 V	11	112	10	113	ns
3	System Clock (CLK) High Time	@ 3.6 V	13	114	12	115	ns
17	System Clock (CLK) RISE Time	1.0 V to 3.6 V		8		5	ns
18	System Clock (CLK) FALL Time	3.6 V to 1.0 V		8		4	ns
4	Asynchronous Inputs SETUP Time	(Note 1)	15		11		ns
5	Asynchronous Inputs HOLD Time	(Note 1)	15		11		ns
6	RESET SETUP Time		18		14		ns
7	RESET HOLD Time		5		3		ns
8	Read Data SETUP Time		5		5		ns
9	Read Data HOLD Time		6		5		ns
10	$\overline{\text{READY}}$ SETUP Time		22		15		ns
11	$\overline{\text{READY}}$ HOLD Time		20		15		ns
12	Status/$\overline{\text{PEACK}}$ Valid Delay	(Notes 2, 3)	–	–	–	–	ns
12A	Status/$\overline{\text{PEACK}}$ Active Delay	(Notes 2,3)	3	18	1	18	ns
12B	Status/PEACK Inactive Delay	(Notes 2,3)	3	20	1	20	ns
13	Address Valid Delay	(Notes 2, 3)	1	32	1	29	ns
14	Write Data Valid Delay	(Notes 2, 3)	0	30	0	22	ns
15	Address/Status/Data Float Delay	(Notes 2, 4)	0	32	0	29	ns
16	HLDA Valid Delay	(Notes 2, 3)	0	25	0	25	ns
19	Address Valid to Status SETUP Time	(Notes 3, 5, 6)	22		22		ns

Notes:
1. Asynchronous inputs are INTR, NMI, HOLD, PEREQ, $\overline{\text{ERROR}}$, and $\overline{\text{BUSY}}$. This specification is given only for testing purposes, to assure recognition at a specific CLK edge.
2. Delay from 1.0 V on the CLK to 0.8 V or 2.0 V or float on the output as appropriate for valid or floating condition.
3. Output load: $C_L = 100$ pF.
4. Float condition occurs when output current is less than I_{LO} in magnitude.
5. Delay measured from address either reaching 0.8 V or 2.0 V (valid) to status going active reaching 2.0 V or status going inactive reaching 0.8 V.
6. For load capacitance of 10 pF on STATUS/PEACK lines, subtract typically 7 ns for 8 MHz spec, and maximum 7 ns for 10 MHz spec.

Note 7:
AC Test Loading on Outputs

TC004190

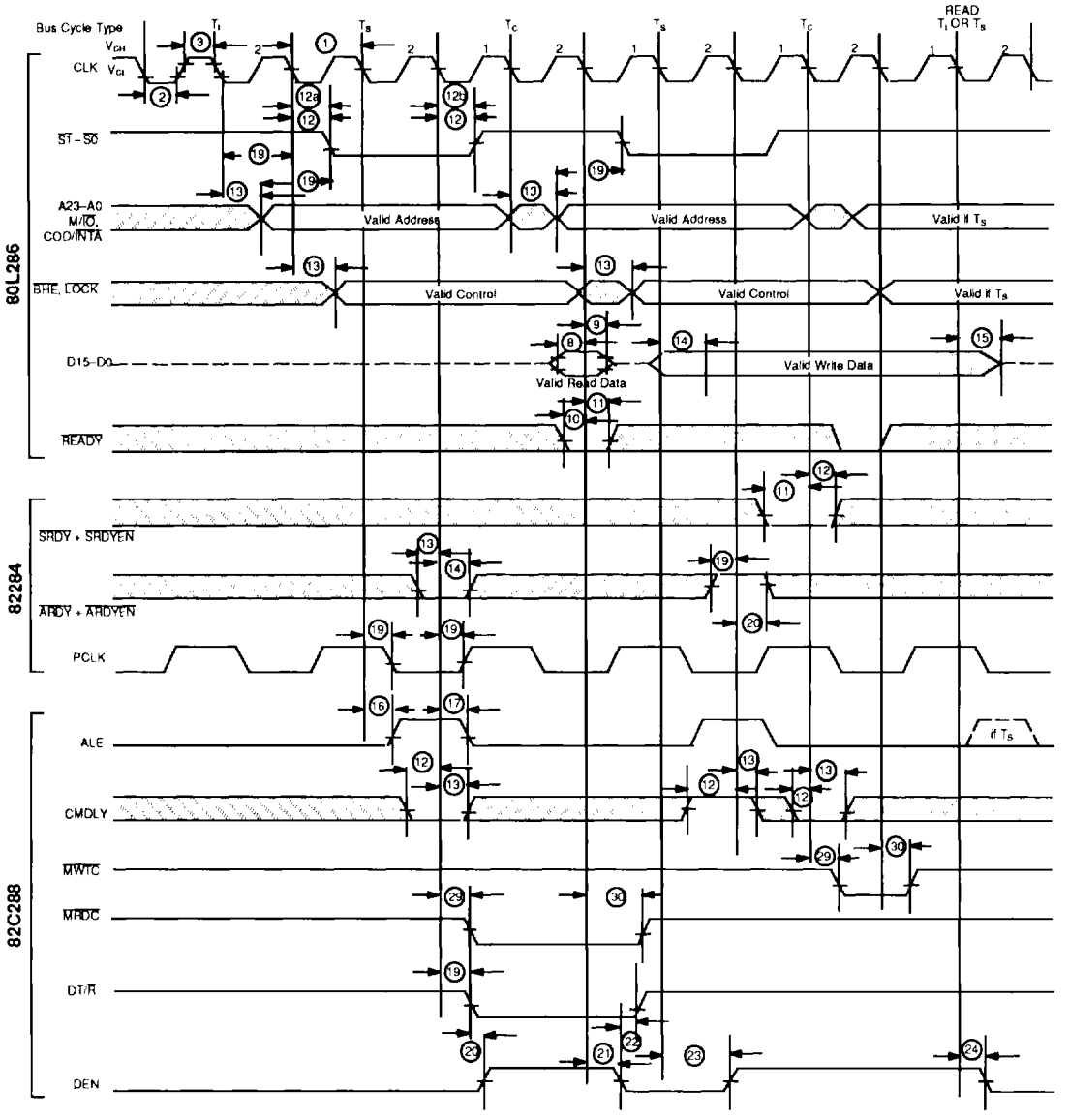


Note 8:
AC Drive and Measurement Points—CLK Input

WF024240

SWITCHING WAVEFORMS

Major Cycle Timing

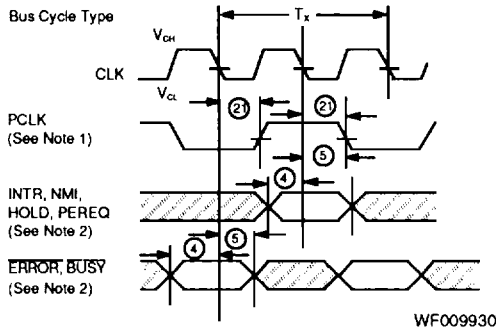


WF007983

Note: $\overline{\text{MWTC}}$ is valid at this point only if $\overline{\text{CMDLY}}$ is Low.

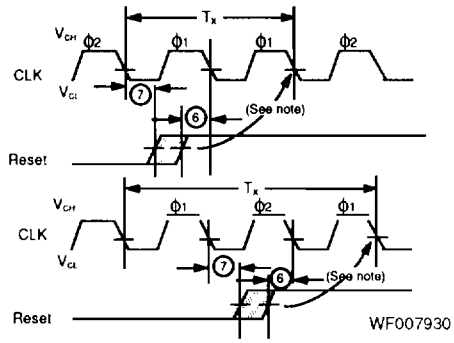
SWITCHING WAVEFORMS (continued)

80L286 Asynchronous Input Signal Timing



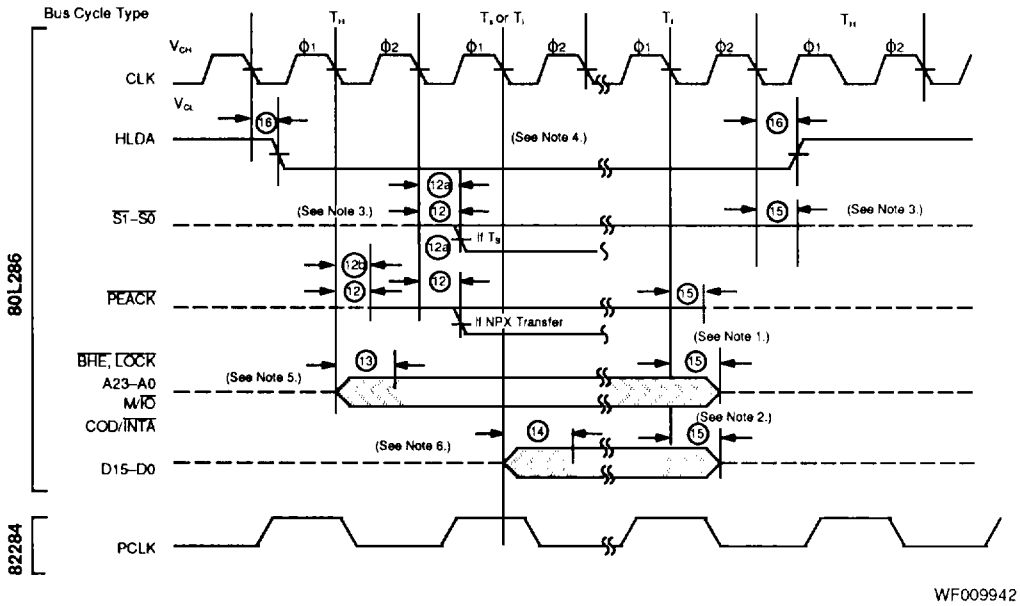
Notes: 1. PCLK indicates which processor cycle phase will occur on the next CLK. PCLK may not indicate the correct phase until the first bus cycle is performed.
2. These inputs are asynchronous. The setup and hold times shown assure recognition for testing purposes.

80L286 Reset Input Timing and Subsequent Processor Cycle Phase



Note: When RESET meets the set-up time shown, the next CLK will start or repeat $\phi 1$ of a processor cycle.

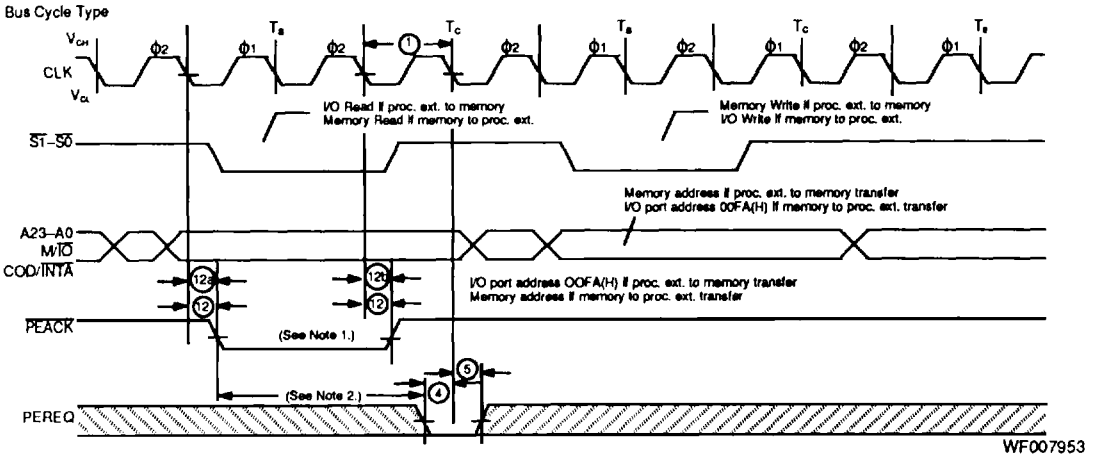
Exiting and Entering Hold



Notes: 1. These signals may not be driven by the 80L286 during the time shown. The worst case in terms of latest float time is shown.
2. The data bus will be driven as shown if the last cycle before T_i in the diagram was a write T_c.
3. The 80L286 floats its status pins during T_H. External 20 kΩ resistors keep these signals High.
4. For HOLD request set-up to HLDA, refer to Figure 34.
5. $\overline{BHE}$ and $\overline{LOCK}$ are driven at this time but will not become valid until T_s.
6. The data bus will remain in three-state OFF if a read cycle is performed.

SWITCHING WAVEFORMS (continued)

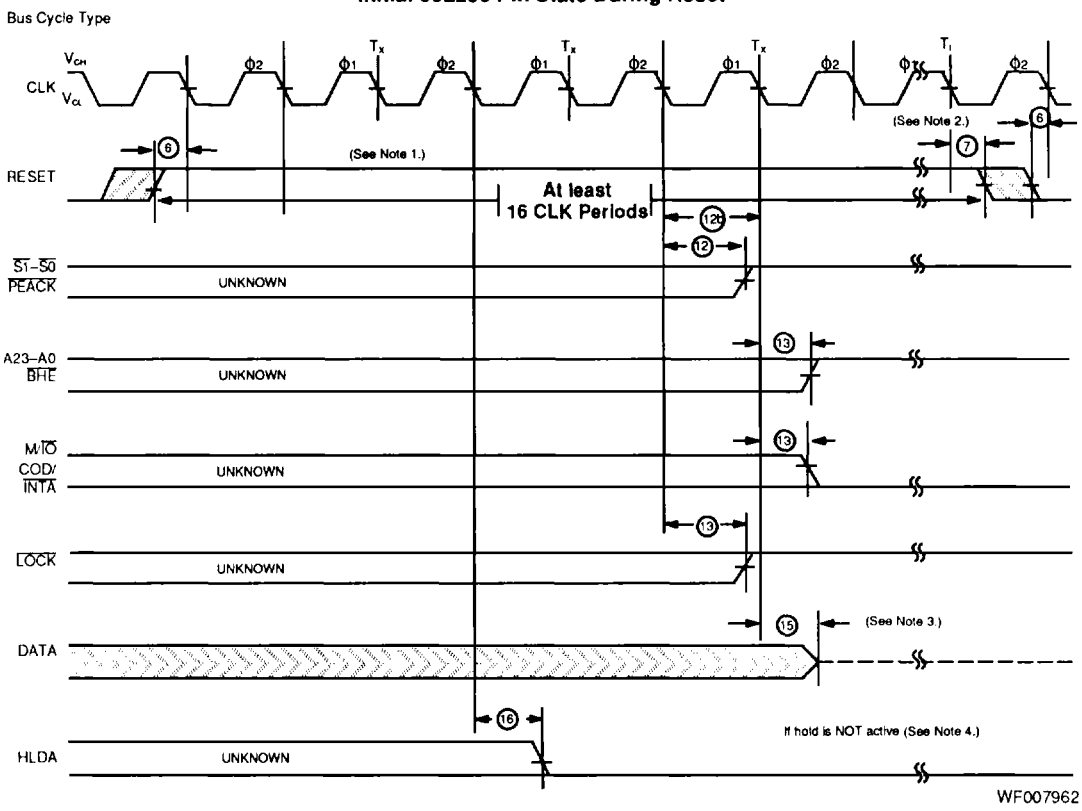
80L286 PEREQ/$\overline{\text{PEACK}}$ Timing Required PEREQ Timing for One Transfer Only



Notes: 1. $\overline{\text{PEACK}}$ always goes active during the first bus operation of a processor extension data operand transfer sequence. The first bus operation will be either a memory read at operand address or I/O read at port address 00FA(H).

2. To prevent a second processor extension data operand transfer, the worst case maximum time (shown above) is: 3 x 1–12a max–4 min. The actual, configuration dependent, maximum time is: 3 x 1–12a max–4 min + A x 2 x 1. A is the number of extra T_c states added to either the first or second bus operation of the processor extension data operand transfer sequence.

Initial 80L286 Pin State During Reset



Notes: 1. Set-up time for RESET ↑ may be violated with the consideration that ϕ1 of the processor clock may begin one system CLK period later.

2. Set-up and hold times for RESET ↓ must be met for proper operation, but RESET ↓ may occur during ϕ1 or ϕ2.

3. The data bus is only guaranteed to be in three-state OFF at the time shown.

4. HOLD is acknowledged during RESET, causing HLDA to go active and the appropriate pins to float. If HOLD remains active while RESET goes inactive, the 80L286 remains in HOLD state and will not perform any bus accesses until HOLD is deactivated.