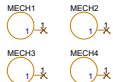
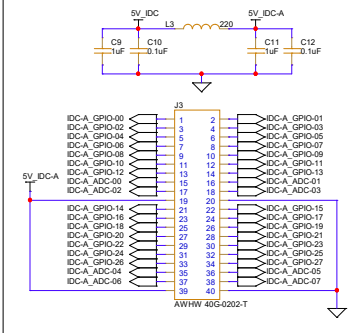


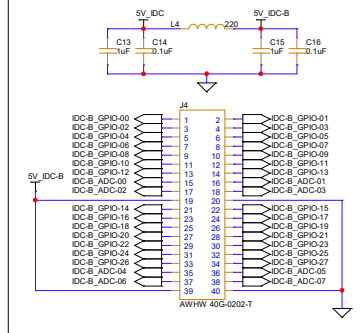
Mounting Holes



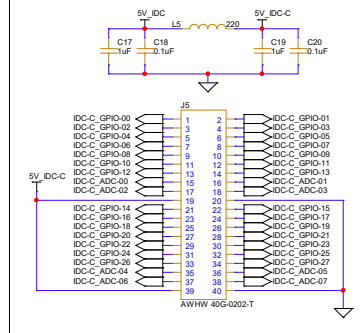
IDC Interface (IDC-A)



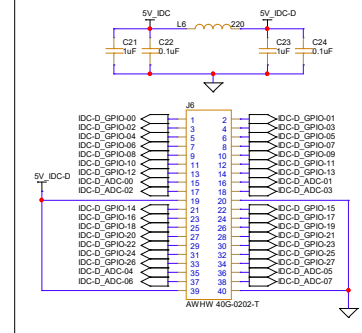
IDC Interface (IDC-B)



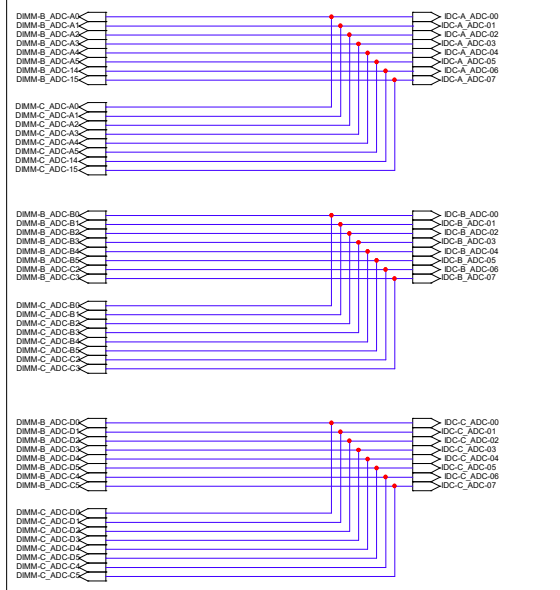
IDC Interface (IDC-C)



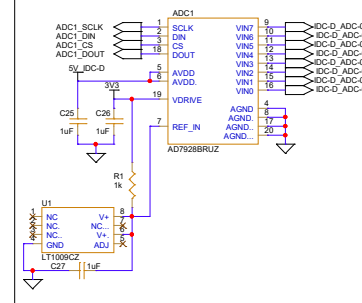
IDC Interface (IDC-D)



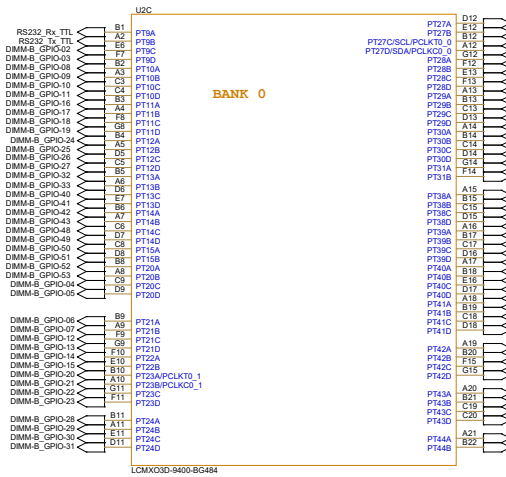
ADC Mapping (IDC-A and IDC-B and IDC-C)



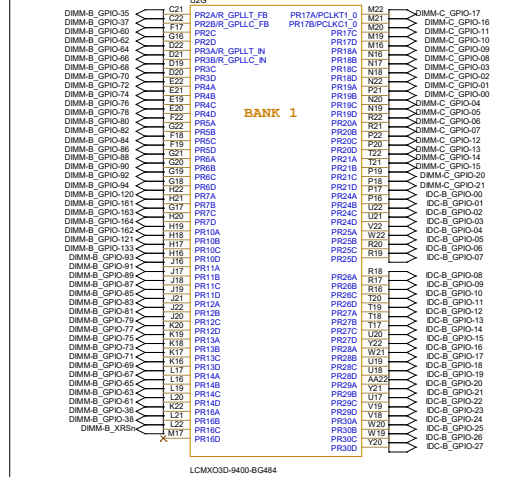
SPI ADC1 - 5V Input, 3.3V I/O



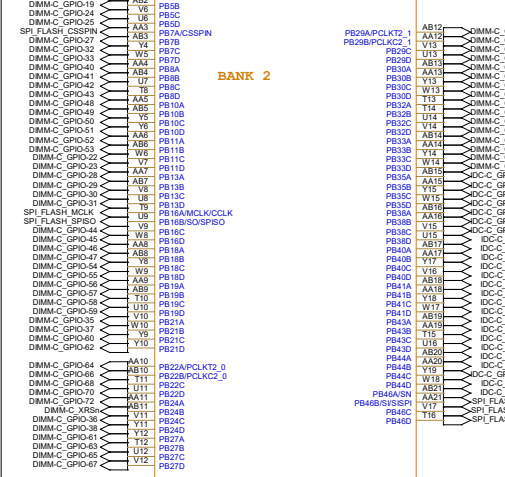
CPLD/FPGA Bank_0



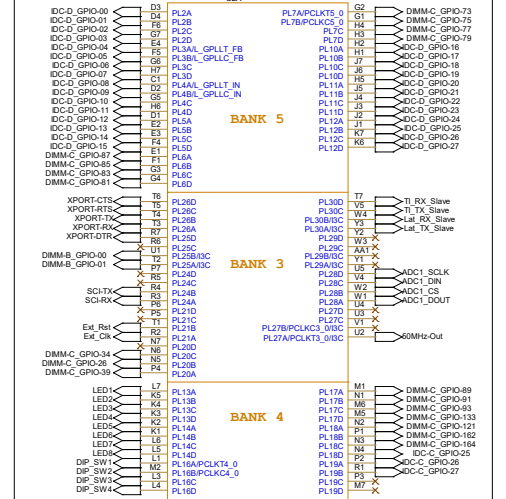
CPLD/FPGA Bank_1



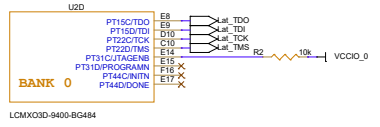
CPLD/FPGA Bank_2



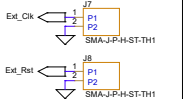
CPLD/FPGA Bank_3-4-5



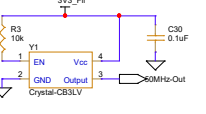
CPLD/FPGA Bank_0 (Comms)



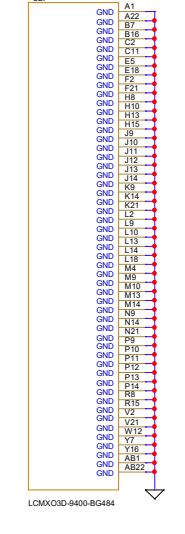
External Sync



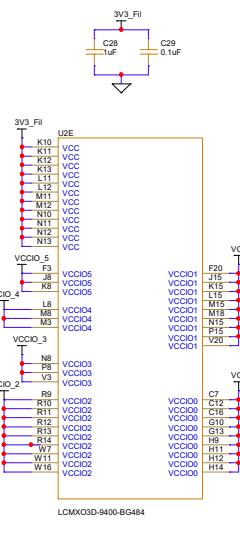
50MHz Oscillator



CPLD/FPGA Grounds



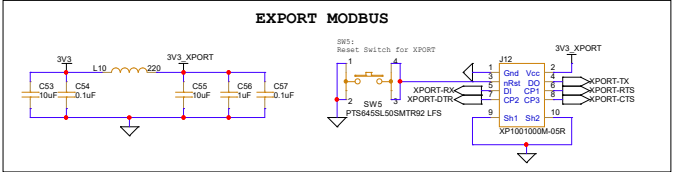
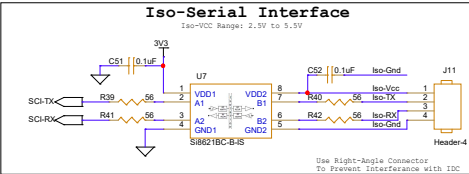
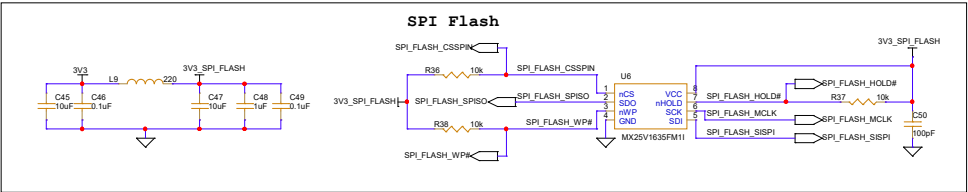
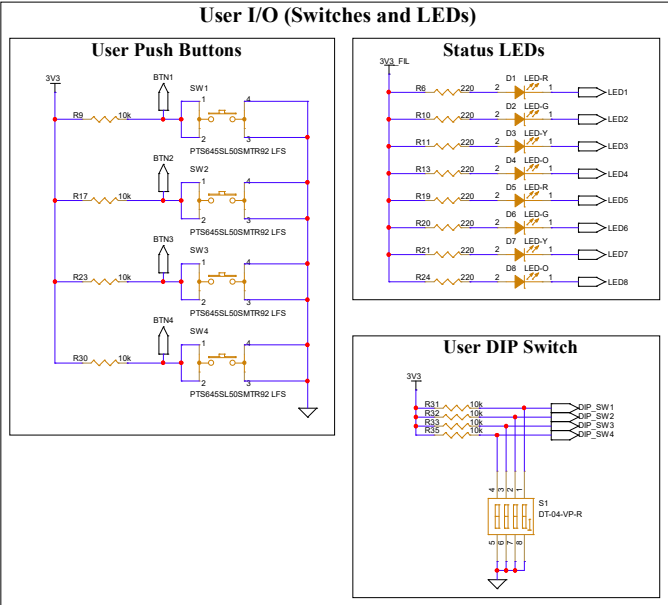
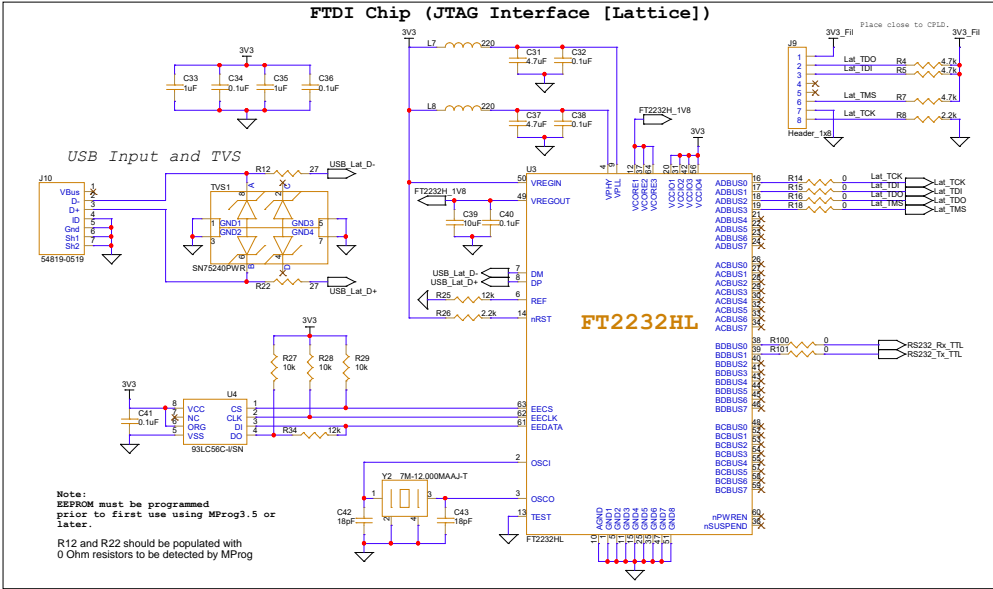
CPLD/FPGA Power Rails



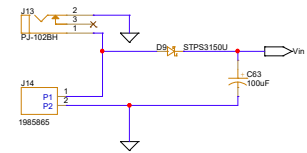
UNIVERSITY OF ARKANSAS
COLLEGE OF ENGINEERING
NCREPT
NATIONAL CENTER FOR RELIABLE
ELECTRIC POWER TRANSMISSION

Organization: University of Arkansas (NCREPT)
File: Unified Controller Board (UCB)
Size: 2
Date: Monday, November 11, 2024
Sheet: 3 of 5

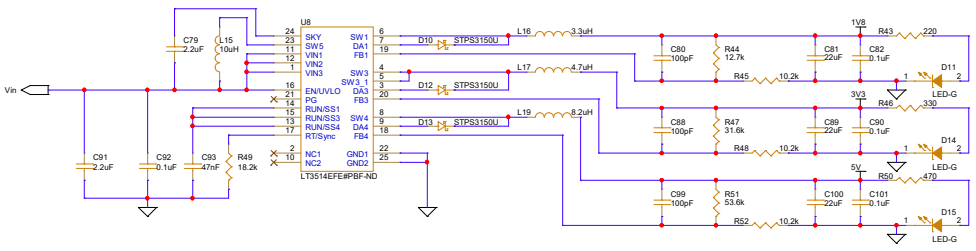
Address: 700 W. Research Center Blvd
Fayetteville, AR 72701
Engineers: Anne Cusick, Justin Jackson, & Chris Farnet



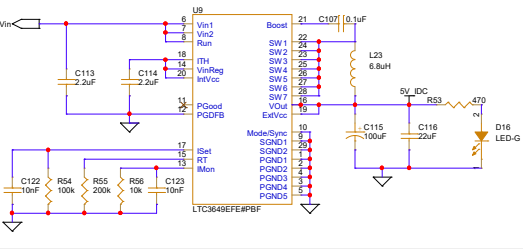
DC Power Entry (9V-36V)



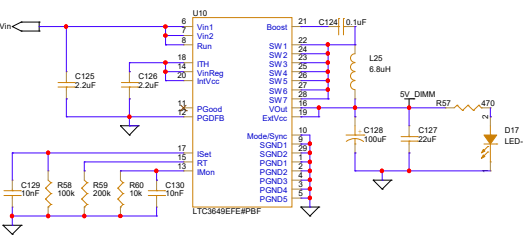
9-36Vdc to 5V/3.3V/1.8V Converter (Digital)



9-36Vdc to 5V_IDC (External)



9-36Vdc to 5V_DIMM (External)



Voltage Filtering

