وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

Analog IC Design

Lecture 22
Variability and Mismatch

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Outline

- Introduction to PVT variations
- Corners and mismatch
- Mismatch in amplifiers: Offset voltage

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Variability (PVT Variations)

- Manufacturing variations: Process variations
- Environmental variations: Voltage and temperature variations

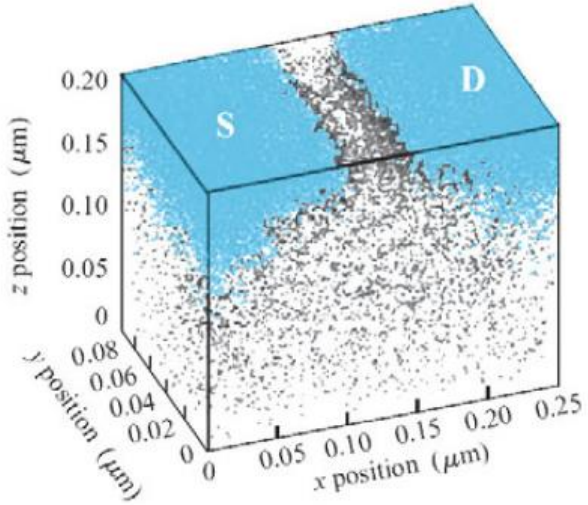
- PVT: Process, voltage, and temperature

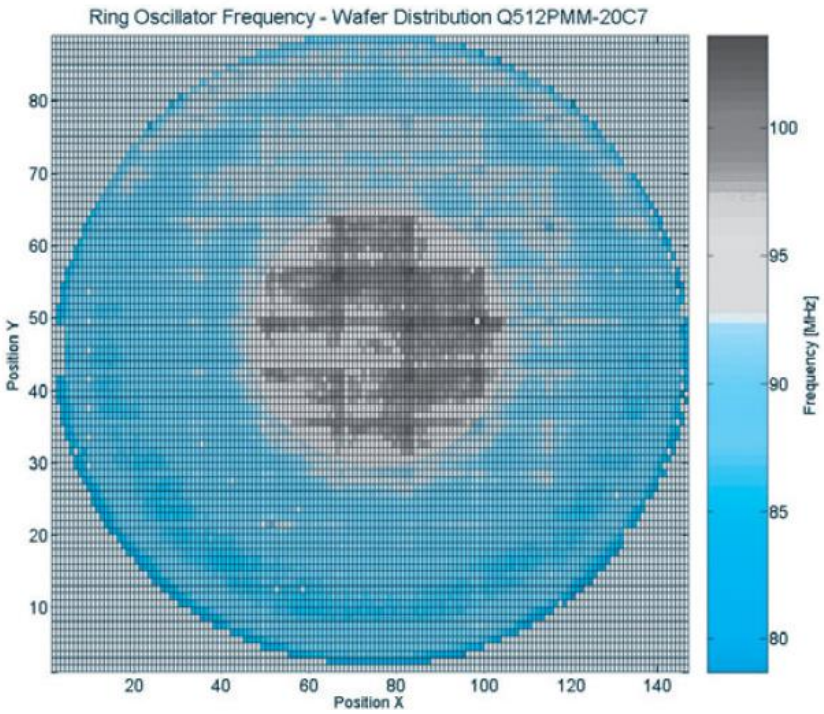
- Variability is a random process
  - Model using a statistical distribution

- The statistical distribution can be
  1. Uniform distribution
  2. Normal (Gaussian) distribution

Process Variations

- Examples of process variations
  - Threshold voltage
    - Random dopant fluctuations (RDF)
  - Channel length
    - Lithography limitations
    - Varying etch rates
    - Line edge roughness
- Binning: Faster parts are rated for higher frequency and sold for more money
  - Ex: Intel CPU binning

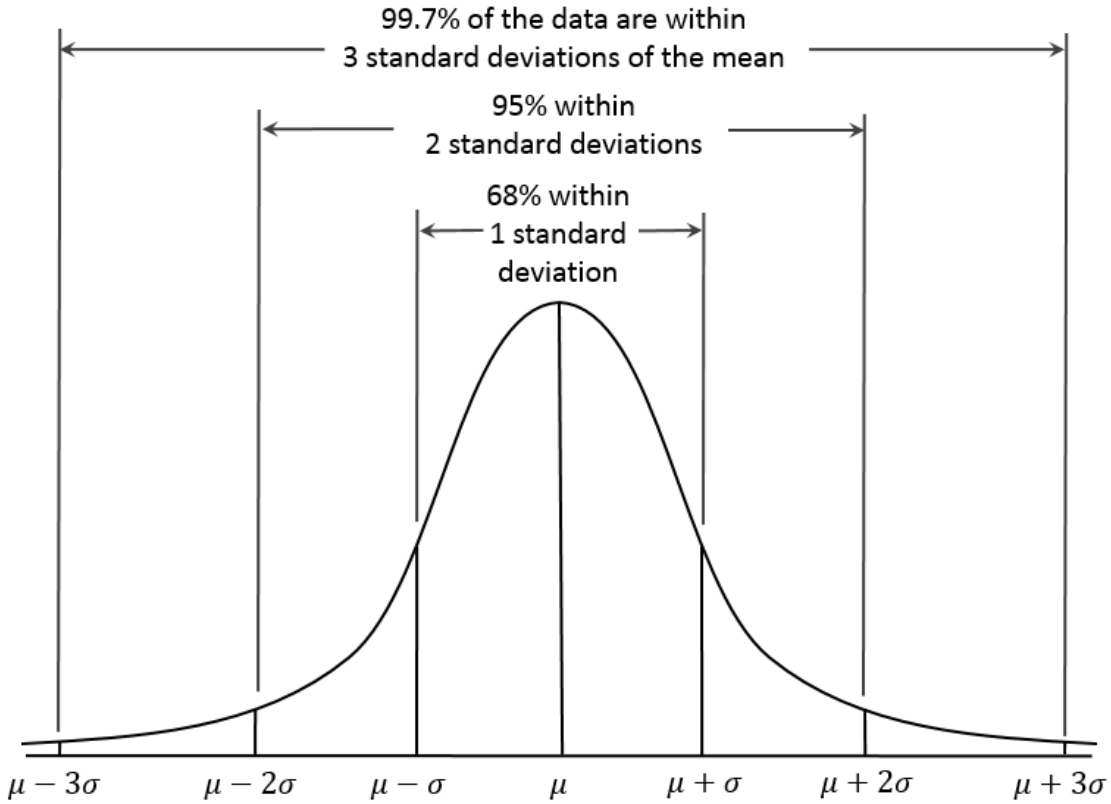




[Weste and Harris, 2010]

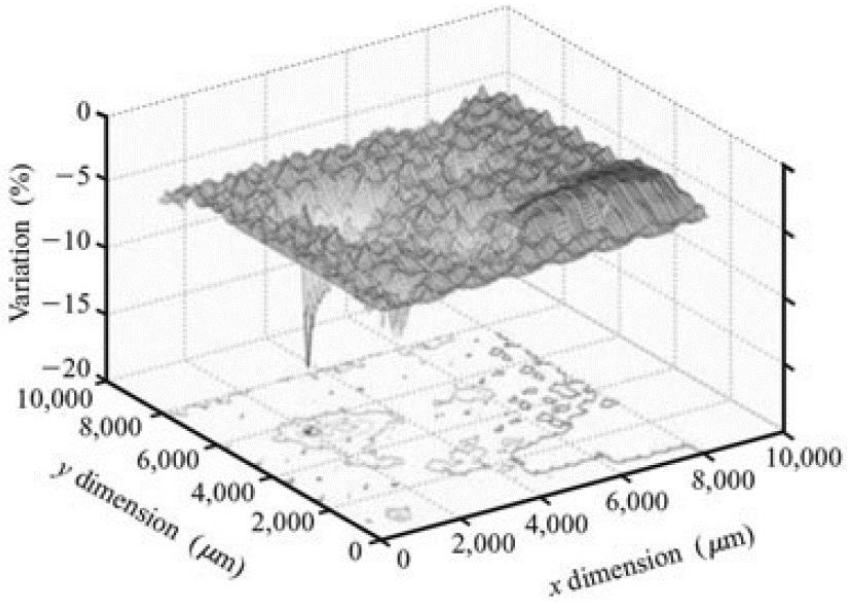
Normal (Gaussian) Distribution

- 68–95–99.7 rule: More accurately, 68.27%, 95.45% and 99.73%
- 3-sigma range is usually acceptable (0.27% of parts rejected)
- Components replicated millions of times (e.g., memory cells) are designed to tolerate 5- to 7-sigma variations



Voltage Variations

- Supply voltage may vary around its nominal value
  - Regulator tolerances
  - iR drops
  - L*di/dt noise
- Voltage varies in both space (across chip) and time
- Typically tolerate 10% variation
- CAD tools can draw voltage droop map



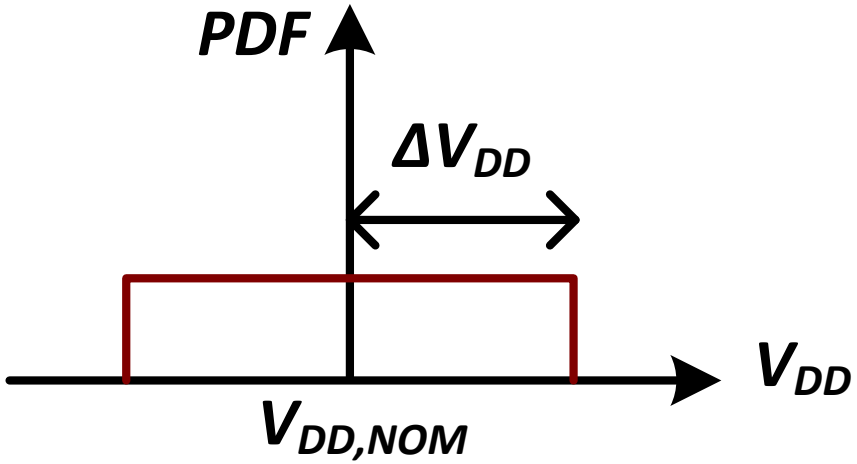
[Weste and Harris, 2010]

Uniform distribution

- Usually assume uniform distribution for voltage variations

$$V_{DD} = V_{DD,NOM} \pm \Delta V_{DD}$$

- Tolerate all variations within $\pm \Delta V_{DD}$
- Ex: $V_{DD} = 1V \pm 10\% \rightarrow \Delta V_{DD} = 100mV$



Temperature Variations

- Ambient temp ranges:
  - Commercial (0 to 70°C)
  - Industrial (-40 to 85°C)
  - Military (-55 to 125°C)
- Junction temp may significantly exceed the ambient
  - Commercial parts commonly verified at 125°C junction temp
- Temperature varies in both space (across chip, a.k.a. temperature gradients) and time (temperature fluctuations)
  - Circuits in a 1 mm diameter see nearly the same temperature
  - Temperature varies in time on a scale of milliseconds
- Drain current in WI (SI) increases (decreases) with temperature

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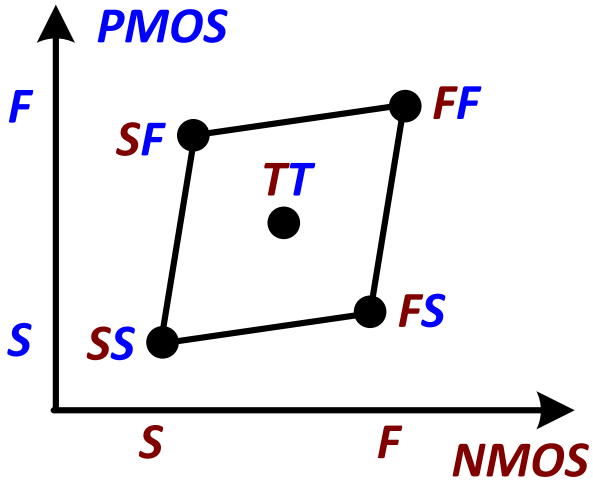
Design Corners

- MOS: Slow (S), typical/nominal (T), and fast (F)
- Voltage: S ($0.9V_{DD}$), T (V_{DD}), and F ($1.1V_{DD}$)
- Temp: S (125°C), T (70°C), and F (0°C)
- Few corners for old technologies
  - Simulate all
- Thousands of corners for DSM nodes
  - Identify what corners are important for a given circuit
  - Depend on experience or use specialized CAD tools

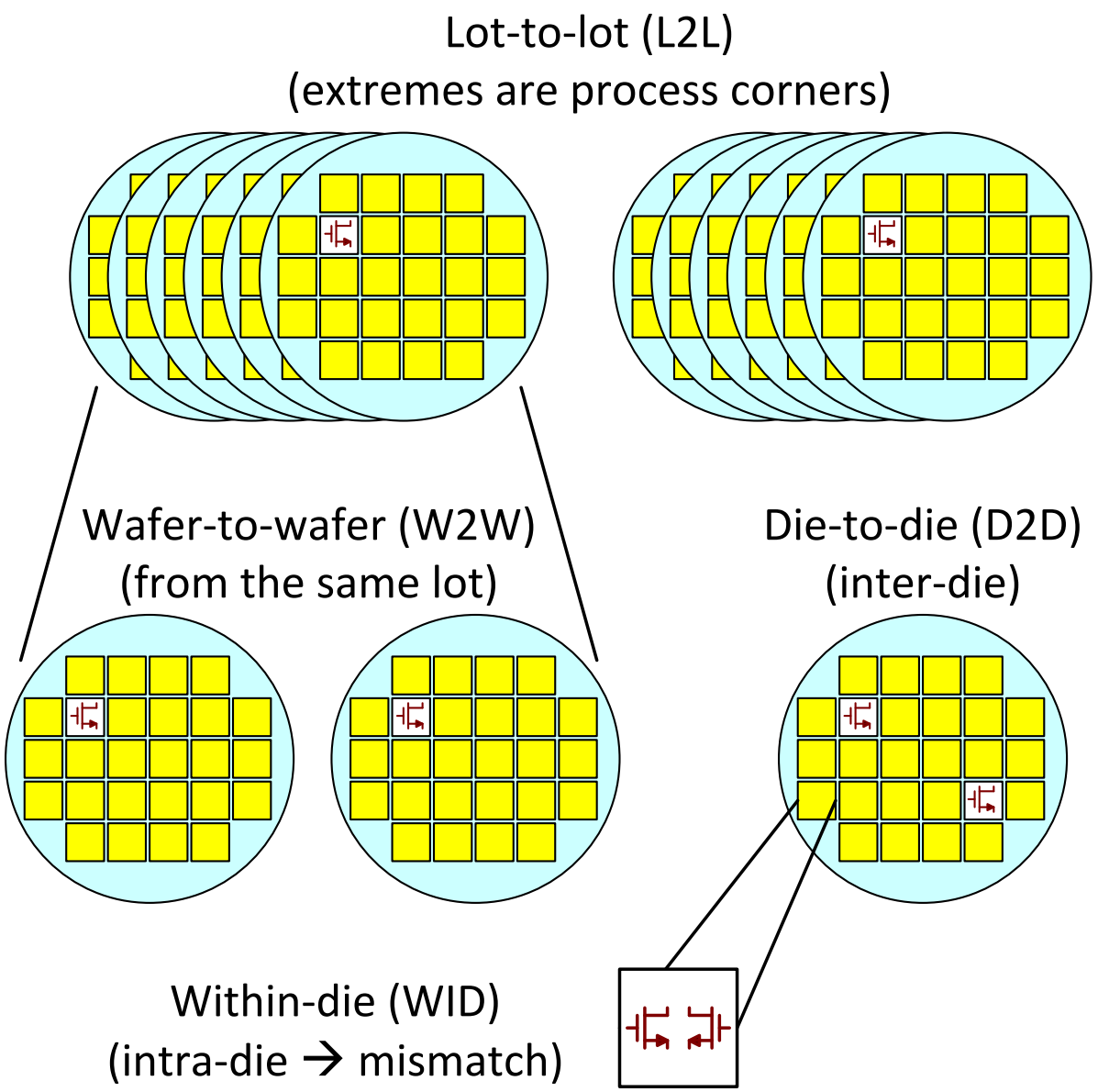


Monte Carlo Simulation

- The worst-case corners can be too pessimistic for practical design
  - Lead to using unnecessary excessive design margins
  - Results in performance degradation
- Monte Carlo generates the statistical distribution of the variations
  - Repeated simulations with parameters randomly varied each time
  - The design margins can be adjusted depending on the required yield
- Yield (Y) is the fraction of manufactured chips that are operational or that work according to specifications
  - Can tolerate one-sigma: Y = 68%
  - Can tolerate two-sigma: Y = 95%

Process Variations Classification

- Process corners (L2L extremes) are very pessimistic
- Within-die (WID) variation is what matters most for analog design
- A.k.a. **mismatch**
  - Modeled using Pelgrom's model
  - Simulated using Monte Carlo simulation



Pelgrom's Mismatch Model

- The standard deviation of random within die (WID) variations is inversely proportional to the square root of the transistor area (WL)
- This makes sense intuitively because variations tend to average out over a larger area

$$\sigma_{V_{TH}} = \frac{A_{V_{TH}}}{\sqrt{WL}}$$

$$\sigma_{\Delta\beta/\beta} = \frac{A_{\beta}}{\sqrt{WL}}$$

- $A_{V_{TH}}$ and A_{β} are constants (Pelgrom's coefficients) determined by the foundry by experimental measurements
- $A_{V_{TH}} \sim 2 - 5\ mV \cdot \mu m$ and $A_{\beta} \sim 1 - 2\% \cdot \mu m$

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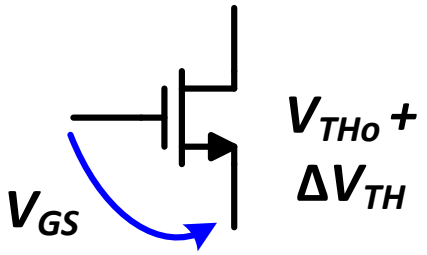
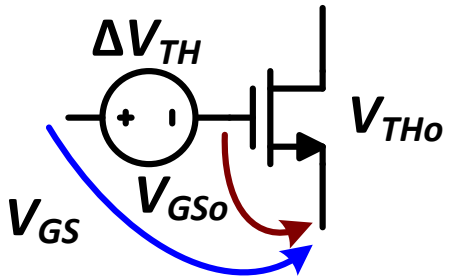
Mismatch Circuit Model

- The most important mismatch effects in MOS devices is V_{TH} mismatch
  - V_{TH} is a function of doping levels in the channel
  - These levels vary randomly from one device to another
- V_{TH} variation can be modeled by a dc source at the gate
  - ΔV_{TH} is a random variable with $\sigma_{V_{TH}} = \frac{A_{V_{TH}}}{\sqrt{WL}}$

$V_{ov} = V_{GS} - V_{THo} - \Delta V_{TH}$

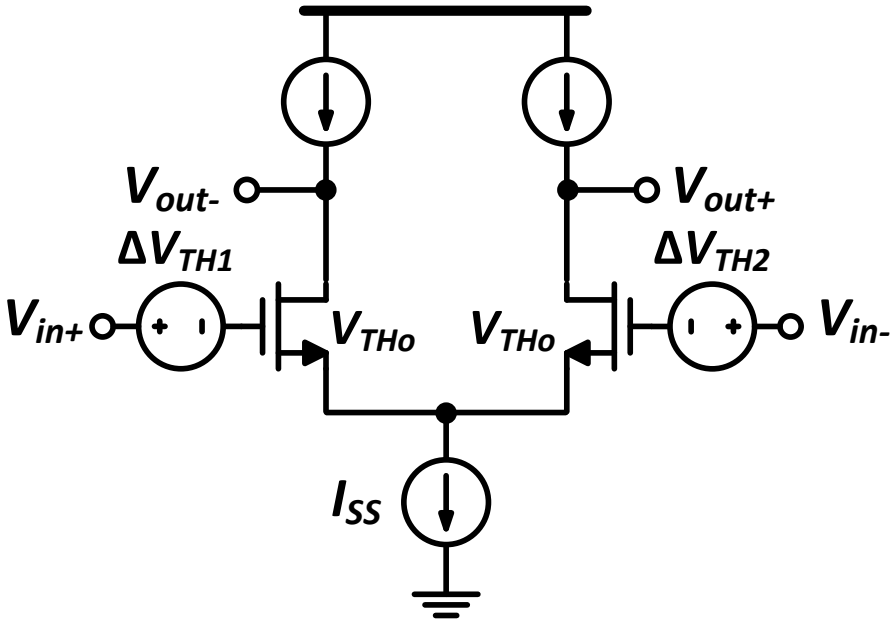


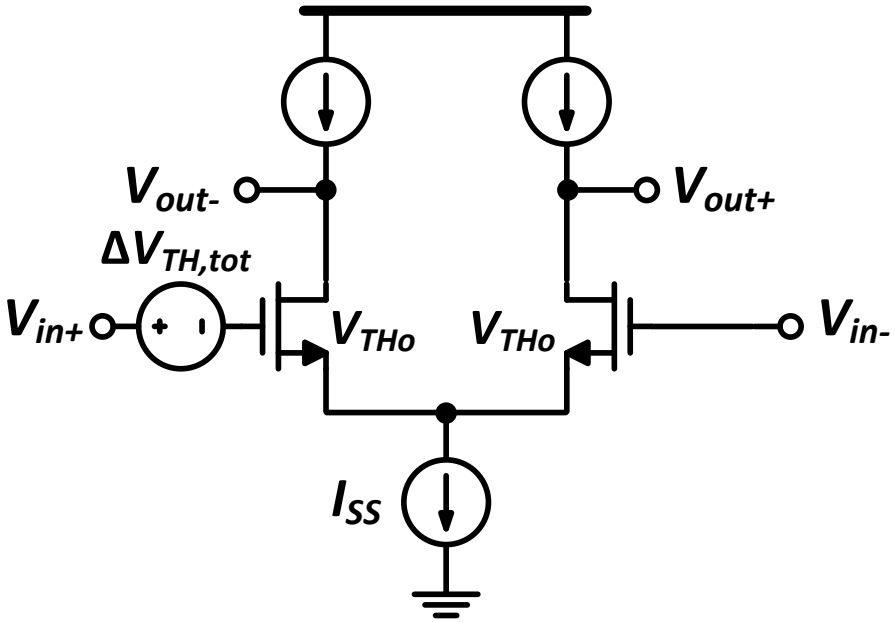
$V_{ov} = V_{GSo} - V_{THo}$
$= V_{GS} - V_{THo} - \Delta V_{TH}$



Mismatch in Diff Pair

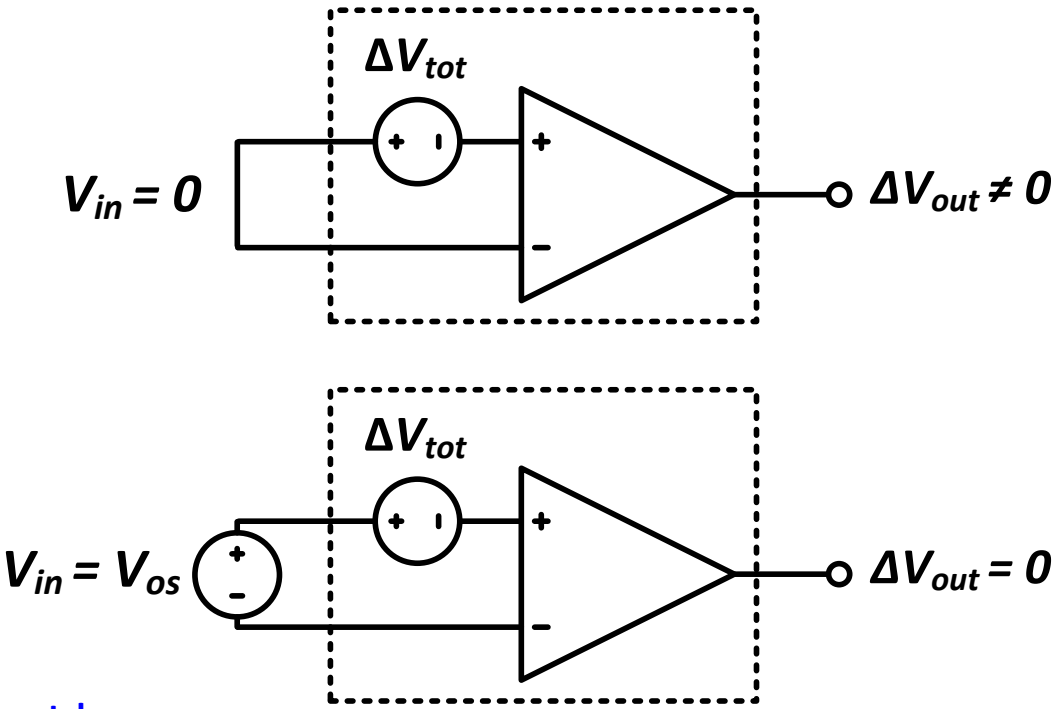
- ΔV_{TH} is a random variable with $\sigma_{V_{TH}} = \frac{A_{V_{TH}}}{\sqrt{WL}}$
- $\sigma(V_{TH,tot}) = \sqrt{\sigma^2_{V_{TH1}} + \sigma^2_{V_{TH2}}} = \sqrt{2}\,\sigma_{V_{TH}}$





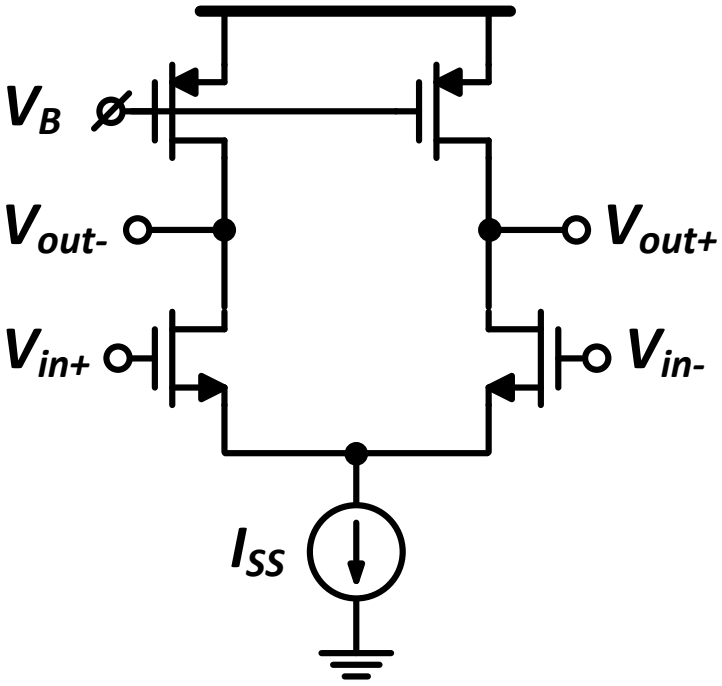
Offset Voltage

- With $V_{id} = 0$ and perfect symmetry: $\Delta V_{out} = 0$
  - But in the presence of mismatches: $\Delta V_{out} \neq 0$
- The input-referred offset voltage (V_{os}): the input level that forces the output voltage to go back to zero
- V_{os} is random variable: $\sigma(V_{os}) = \sigma(\Delta V_{tot})$



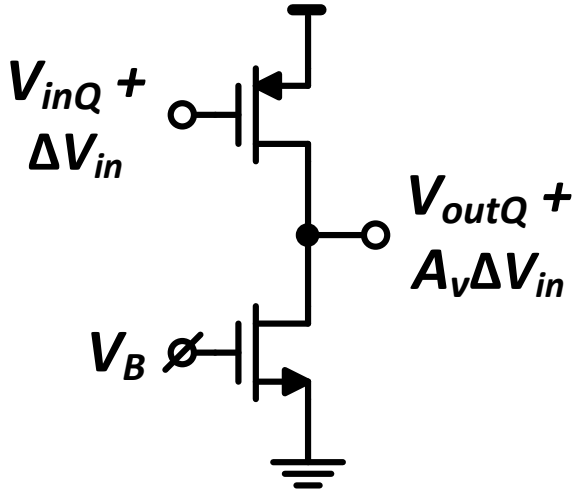
Quiz: Offset Voltage

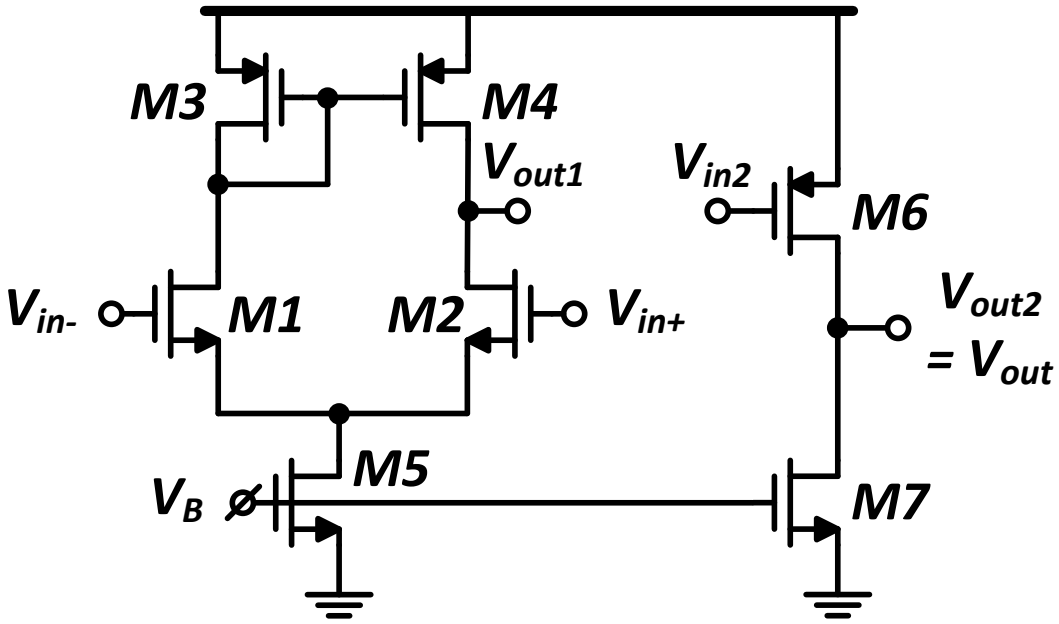
- Assume PMOS V_{TH} mismatch is σ_P and NMOS mismatch is σ_N
- What is the rms input referred offset voltage?
- Hint: The mismatch is usually a small perturbation
  - We can analyze it using small signal models (same as noise)



Systematic Offset

- Systematic offset is due to design or layout issues rather than random variations
  - It can be nulled by proper design and layout
- One common example is Miller OTA
  - Must size M6 such that $V_{GS6} = V_{GS3,4} \rightarrow V_{out1Q} = V_{in2Q}$





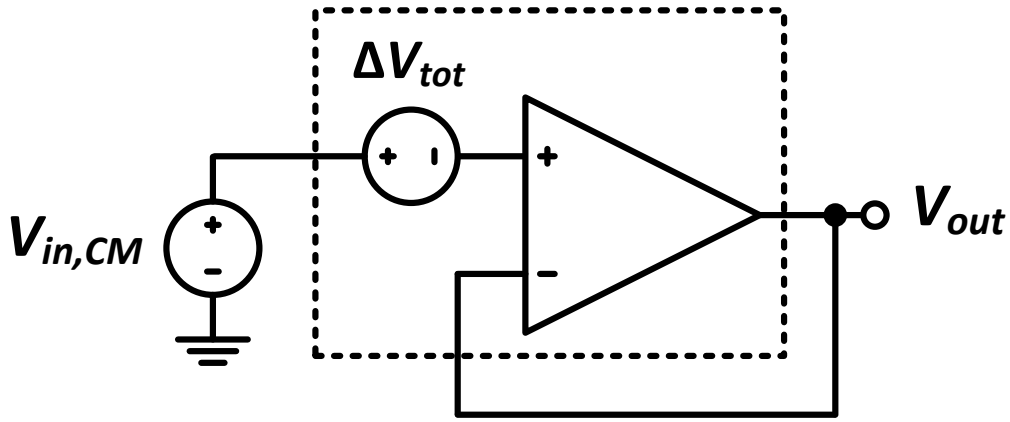
OTA Offset Simulation

- Connect the OTA in unity-gain negative feedback loop

$$V_{out} \approx V_{in,CM} - \Delta V_{tot}$$

$$V_{os} \approx V_{in,CM} - V_{out}$$

- Set $V_{in,CM}$ to $V_{out,CM}$ to avoid finite loop-gain errors
- A non-inverting amplifier topology can be also used



References

- B. Razavi, “Design of Analog CMOS Integrated Circuits,” McGraw-Hill, 2nd ed., 2017
- Neil Weste and David Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, Pearson, 4th ed., 2010

Thank you!