وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

Analog IC Design

Lecture 23
Reference Circuits

Dr. Hesham A. Omran

Integrated Circuits Laboratory (ICL)
Electronics and Communications Eng. Dept.
Faculty of Engineering
Ain Shams University

Outline

- Reference circuits
- Bandgap reference (BGR) circuit
  - BGR basic operation
  - BGR practical CMOS implementation
- Constant-gm circuit

Outline

- Reference circuits
- Bandgap reference (BGR) circuit
  - BGR basic operation
  - BGR practical CMOS implementation
- Constant-gm circuit

Reference Circuits

- Stable DC voltage and DC current generation
  - Little dependence on process (P) and supply (V)
  - Well-defined dependence on temperature (T)
    - Not necessarily independent!
- Temperature dependence
  - Positive temperature coefficient (+ve TC): Proportional to absolute temperature (PTAT)
  - Negative temperature coefficient (-ve TC): Complementary to absolute temperature (CTAT)
  - **Temperature independent (Zero-TC): ZTAT = PTAT + CTAT**
- Most process parameters vary with temperature
  - If we achieve a temperature independent reference it will also be process independent

Why Reference Circuits?

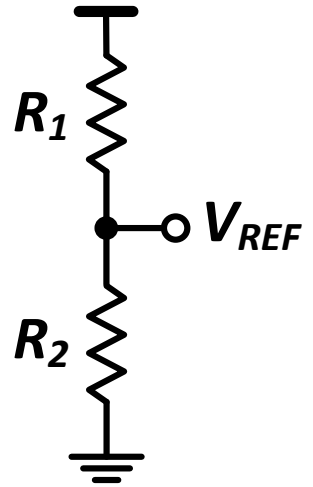
- Applications:
  - Voltage regulators
  - ADCs and DACs
  - Biasing of amplifiers
  - Common-mode (CM) level of fully-differential circuits
  - …

- Types of references we usually need (all should be PV insensitive):
  - PTAT: Proportional to absolute temperature (+ve TC)
  - Temperature independent (Zero-TC) → PVT insensitive
  - Constant-transconductance (constant-Gm)

Poor Man's Reference Voltage

$$V_{REF} = V_{DD} \frac{R_2}{R_1 + R_2}$$

- Good layout makes V_{REF} independent of process and temperature.
- V_{REF} absolute value depends on V_{DD}.
- V_{REF} is sensitive to V_{DD} variations (poor PSR).

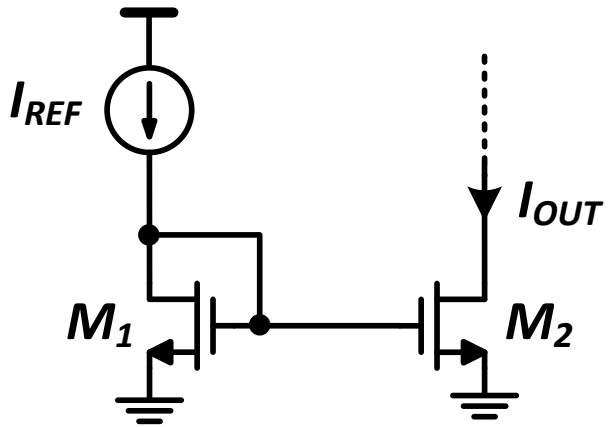


$$PSR = \frac{\Delta V_{REF}}{\Delta V_{DD}} = \frac{R_2}{R_1 + R_2}$$

Poor Man's Reference Current

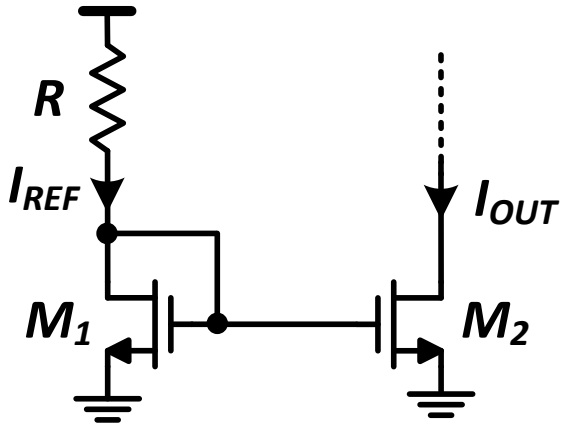
$$I_{REF} = \frac{\mu C_{ox}}{2}\frac{W_1}{L_1}(V_{GS} - V_{TH})^2 = \frac{\beta_1}{2}(V_{GS} - V_{TH})^2$$

$$I_{REF} = \frac{V_{DD} - V_{GS}}{R} = \frac{V_{DD} - \sqrt{\frac{2I_{REF}}{\beta_1}} - V_{TH}}{R}$$



- I_{REF} depends on process, supply voltage, and temperature (PVT).
- I_{REF} is sensitive to V_{DD} variations (poor PSR).

$$\Delta I_{REF} = \frac{\Delta V_{DD}}{R + 1/g_{m1}} \quad \rightarrow \quad \frac{\Delta I_{REF}}{\Delta V_{DD}} \approx \frac{1}{R}$$

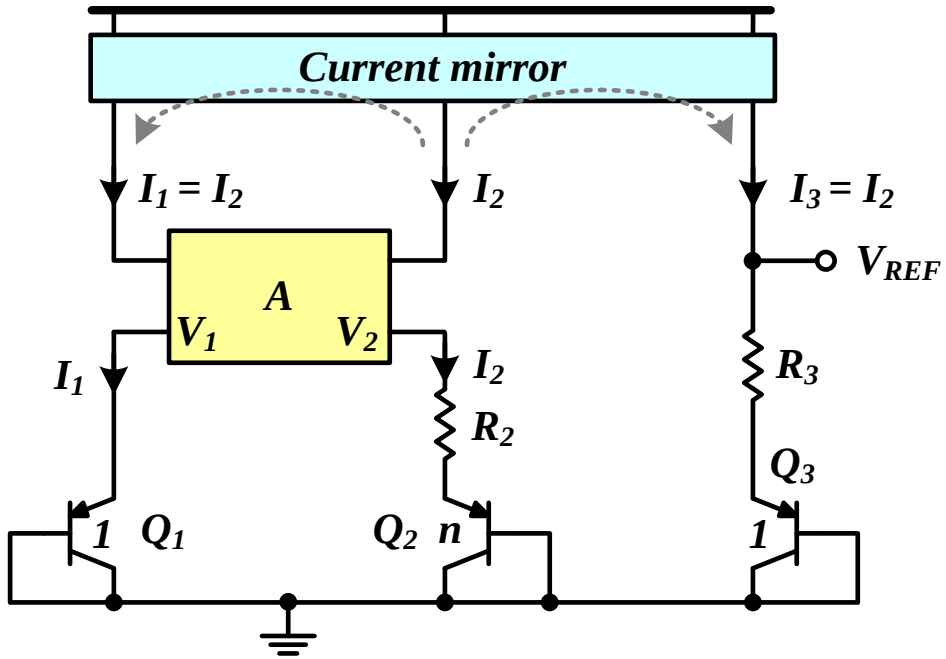


Outline

- Reference circuits
- Bandgap reference (BGR) circuit
  - BGR basic operation
  - BGR practical CMOS implementation
- Constant-gm circuit

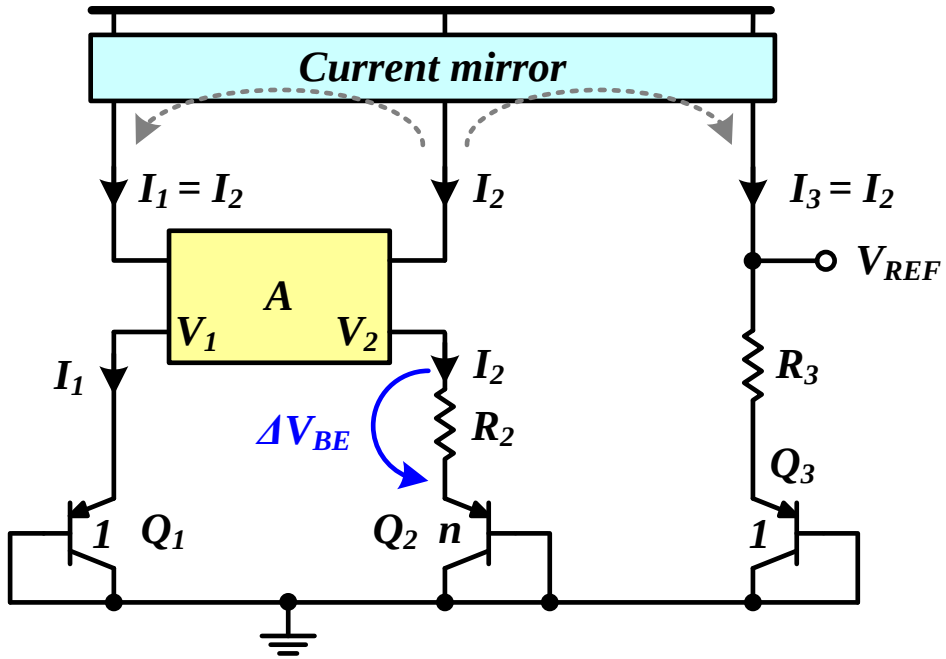
Basic Bandgap Reference (BGR) Circuit

- Q1, Q2, and Q3 are diode connected PNP BJTs.
- The A-block is a circuit that makes $V_1 = V_2$.
- The current mirror copies I_2 to I_1 and I_3.
- V_{REF} is ZTAT → How?



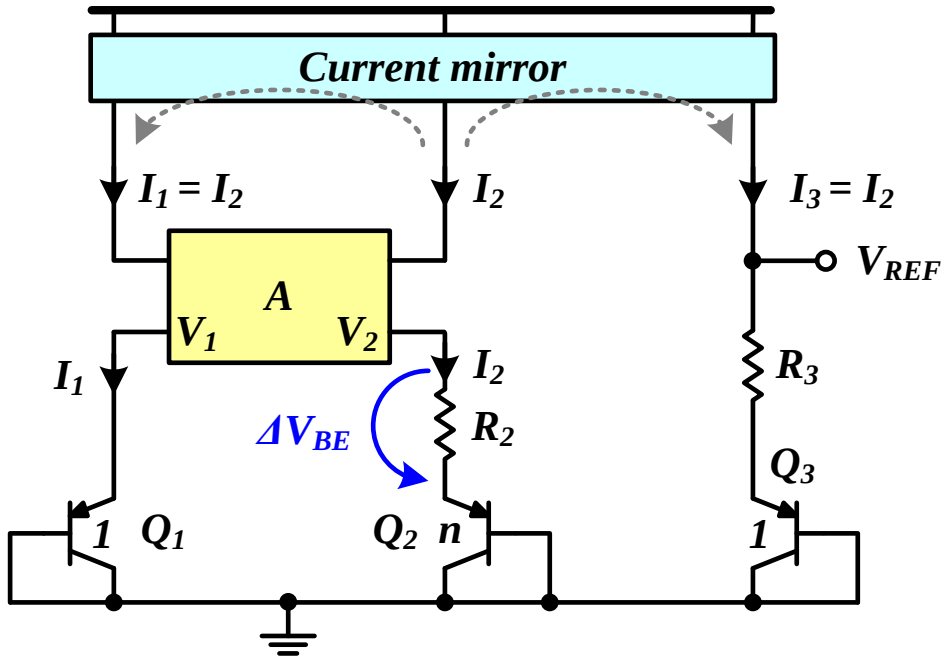
How much is I_2?

- Using simple diode model you may expect $I_2 = 0$.
- But Q2 is n BJTs (diodes) connected in parallel.
  - $I_{C1} \approx I_1$ and $I_{C2} \approx I_2/n$
- $I_C = I_S e^{\frac{|V_{BE}|}{V_T}} \rightarrow |V_{BE}| = V_T \ln \frac{I_C}{I_S}$



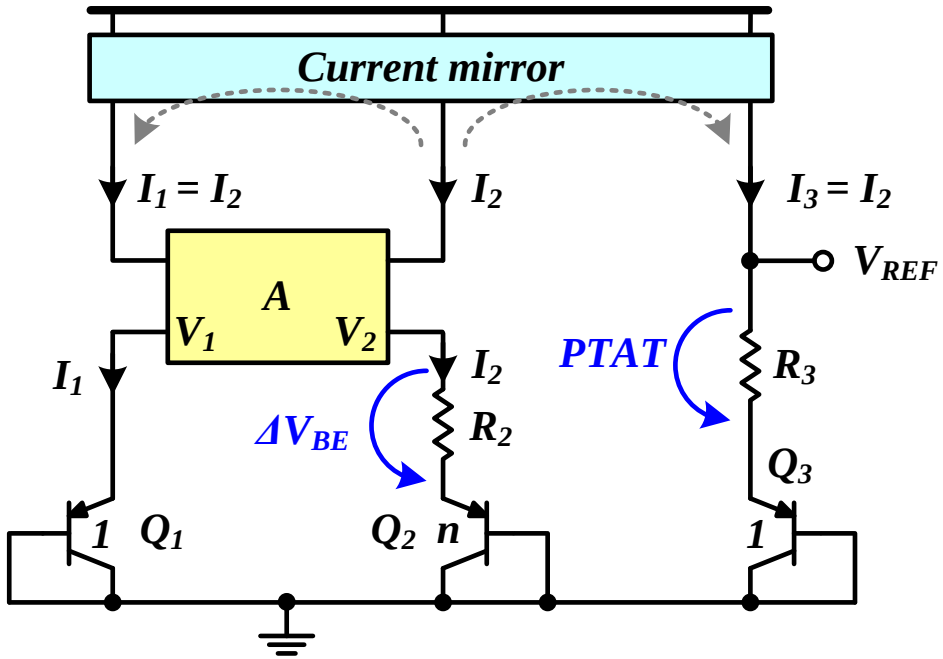
I_2 is PTAT

- $I_C = I_S e^{\frac{|V_{BE}|}{V_T}} \rightarrow |V_{BE}| = V_T \ln \frac{I_C}{I_S}$
- $I_{C1} \approx I_1$ and $I_{C2} \approx I_2/n$
- $|V_{BE1}| \approx V_T \ln \frac{I_1}{I_S}$ and $|V_{BE2}| \approx V_T \ln \frac{I_2/n}{I_S} = V_T \ln \frac{I_2}{I_S} - V_T \ln n$
- $\Delta V_{BE} = |V_{BE1}| - |V_{BE2}| = V_T \ln n = \frac{kT}{q} \ln n \quad \propto T \rightarrow$ PTAT!



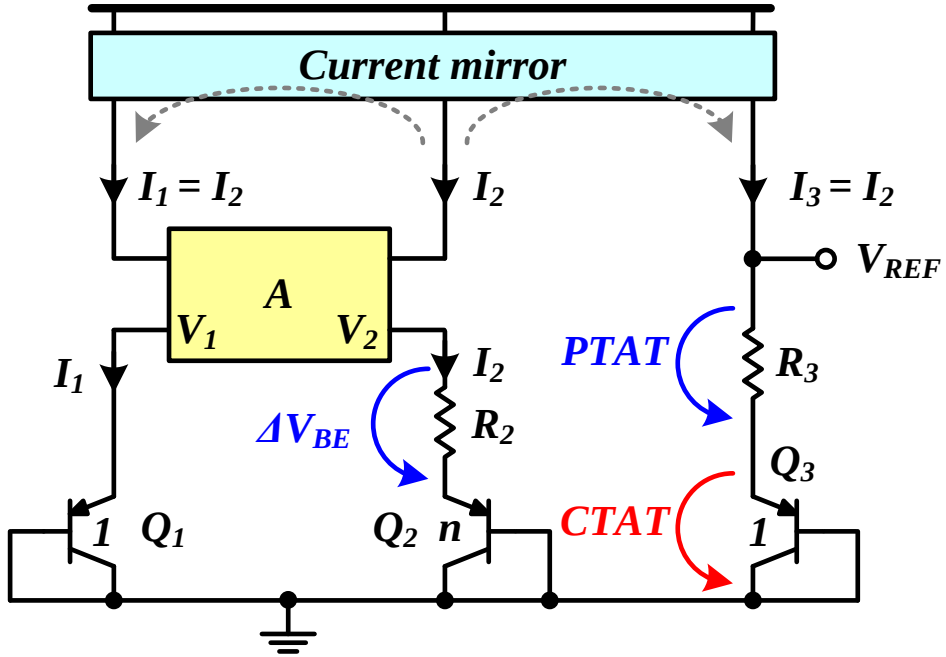
The PTAT Component

- $\Delta V_{BE} = |V_{BE1}| - |V_{BE2}| = V_T \ln n = \frac{kT}{q} \ln n \quad \propto T \rightarrow$ PTAT
- $I_2 = \frac{\Delta V_{BE}}{R_2} = \frac{kT}{q} \ln n \cdot \frac{1}{R_2} \quad \propto T \rightarrow$ PTAT
- $V_{R_3} = I_3 R_3 = \Delta V_{BE} \cdot \frac{R_3}{R_2} = V_T \ln n \cdot \frac{R_3}{R_2} = a_1 T \quad \propto T \rightarrow$ PTAT
- $a_1 = \frac{k}{q} \ln n \cdot \frac{R_3}{R_2} \approx 0.086 \ln n \cdot \frac{R_3}{R_2}\ mV/K$



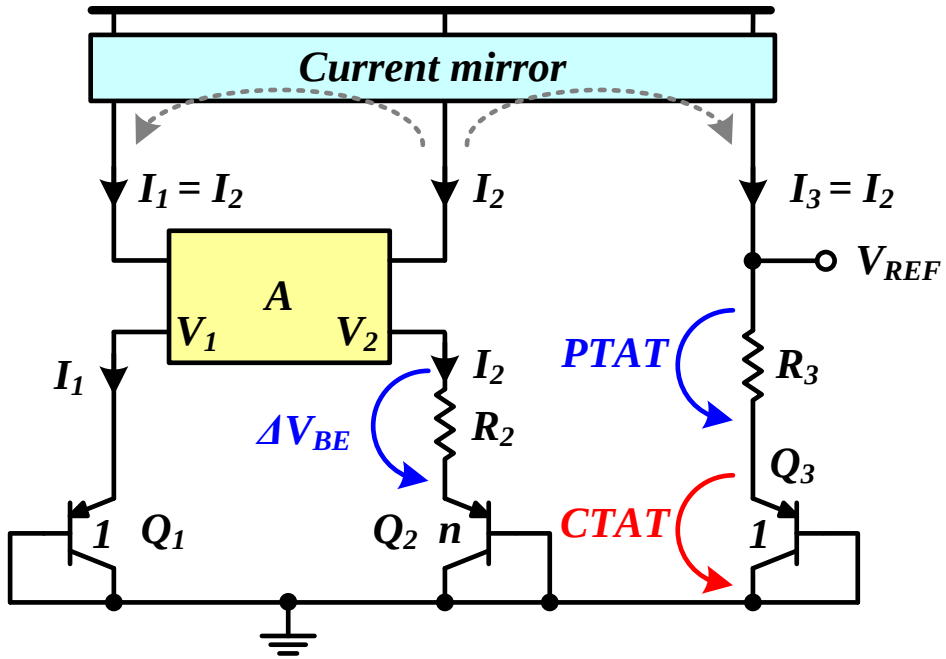
V_{BE} is CTAT

- It can be shown that $|V_{BE}| = V_T \ln \frac{I_C}{I_S} \approx V_{G0} - b_1 T$ → CTAT
  - I_S is a strong function of temperature.
  - $|V_{BE}|$ is CTAT even if I_C itself is PTAT!
- All "simple" analytical models are inaccurate (and complicated).
  - Get b_1 from simulations: Usually $b_1 \approx 1.5 - 2\ mV/K$.



V_{REF} is ZTAT

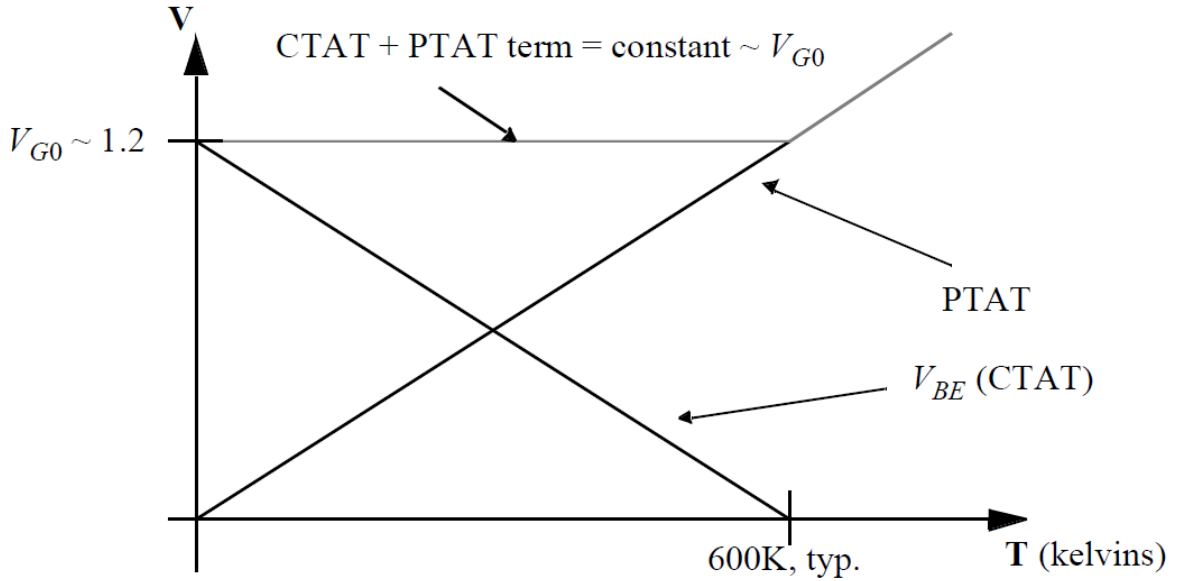
- $V_{R_3} = I_3 R_3 = \Delta V_{BE} \cdot \frac{R_3}{R_2} = V_T \ln n \cdot \frac{R_3}{R_2} = a_1 T$ → PTAT
- $|V_{BE}| = V_T \ln \frac{I_C}{I_S} \approx V_{G0} - b_1 T$ → CTAT
- $V_{REF} = \Delta V_{BE} \cdot \frac{R_3}{R_2} + |V_{BE3}| = a_1 T + V_{G0} - b_1 T \approx V_{G0}$
- $V_{REF} = PTAT + CTAT = ZTAT \approx V_{G0}$



Why the Name "Bandgap"?

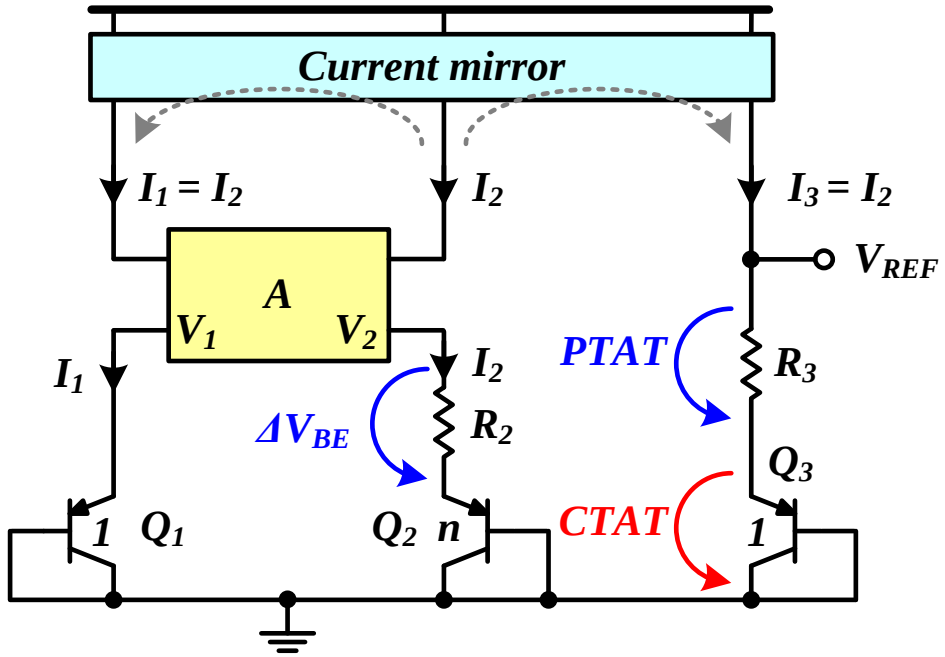
- $V_{R_3} = I_3 R_3 = \Delta V_{BE} \cdot \frac{R_3}{R_2} = V_T \ln n \cdot \frac{R_3}{R_2} = a_1 T$ → PTAT
- $|V_{BE}| = V_T \ln \frac{I_C}{I_S} \approx V_{G0} - b_1 T$ → CTAT
- $V_{REF} = \Delta V_{BE} \cdot \frac{R_3}{R_2} + |V_{BE3}| = a_1 T + V_{G0} - b_1 T \approx V_{G0}$
- $V_{REF} = PTAT + CTAT = ZTAT \approx V_{G0}$

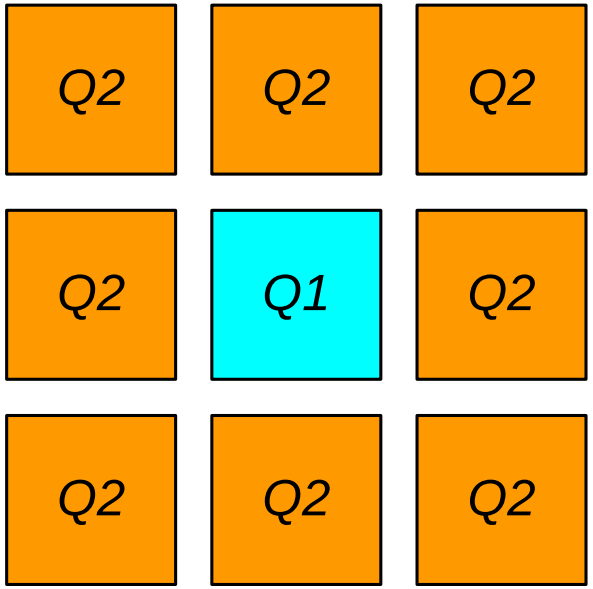
$V_{G0} = E_{g0}/q$ ≈ 1.2 V is the bandgap voltage (energy) of Si extrapolated at absolute zero Kelvin



BGR Design Example: n

- Due to layout considerations, two values of n are usually used.
  - $n = 8$
  - $n = 24$





BGR Design Example: R_2

- Given current consumption select R_2.

$$I_2 = \frac{\Delta V_{BE}}{R_2} = \frac{\frac{kT}{q}\ln n}{R_2}$$

- Ex: $I_{total} = 30\mu A$ and $n = 8$

$$I_2 = 10\mu A$$

$$R_2 \approx 5.4k\Omega$$

BGR Design Example: R_3

- Choose R_3 to achieve ZTAT V_{REF} (set $a_1 = b_1$).

$$V_{REF} = \Delta V_{BE} \cdot \frac{R_3}{R_2} + |V_{BE3}| = a_1 T + V_{G0} - b_1 T \approx V_{G0}$$

- $a_1 \approx \frac{k}{q} \ln n \cdot \frac{R_3}{R_2} \approx 0.086 \ln n \cdot \frac{R_3}{R_2}\ mV/K$
- Get b_1 from simulations (all analytical models are inaccurate).
  - Usually $b_1 \approx 1.5 - 2\ mV/K$
- Ex: $n = 8$ and $b_1 = 1.8 mV/K$

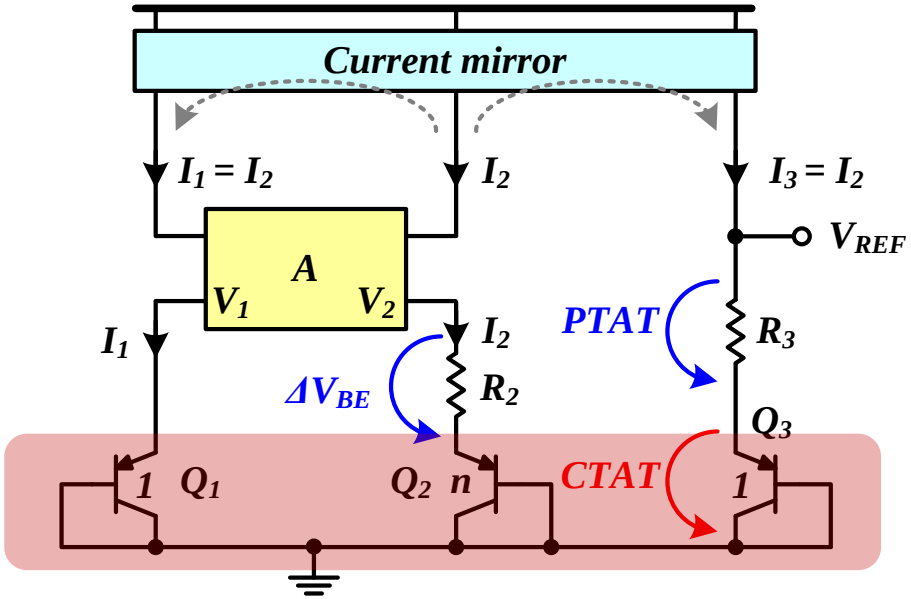
$$\frac{R_3}{R_2} \approx 10$$

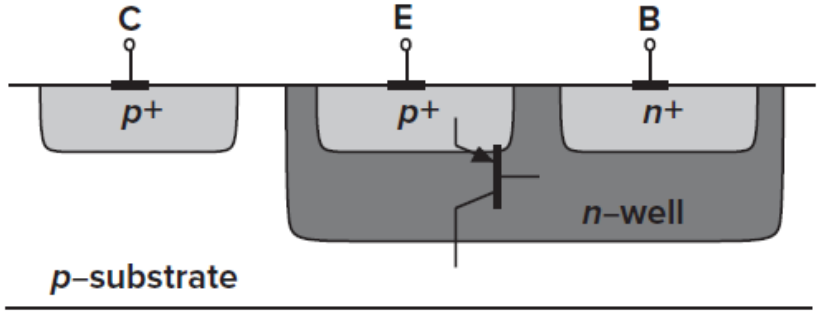
$$R_3 \approx 54 k\Omega$$

- Fine tune R_3 in SPICE.

Parasitic / Substrate / Native PNP

- The diode connected PNP can be implemented in any standard CMOS process.
  - But it usually has very low $\beta = I_C/I_B$ (< 10).
  - The n-well has relatively high parasitic ohmic resistance.
- Can be replaced by MOSFET in WI.
  - Necessary for low supply voltage operation.





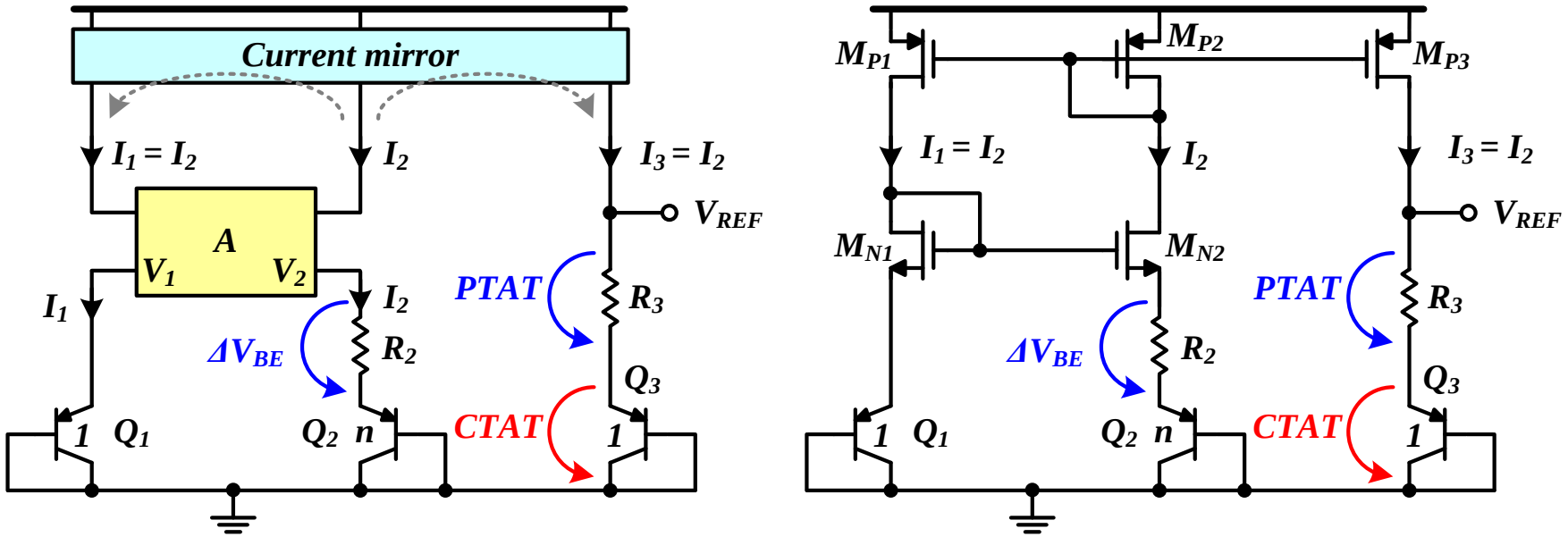
[Razavi, 2017]

Outline

- Reference circuits
- Bandgap reference (BGR) circuit
  - BGR basic operation
  - BGR practical CMOS implementation
- Constant-gm circuit

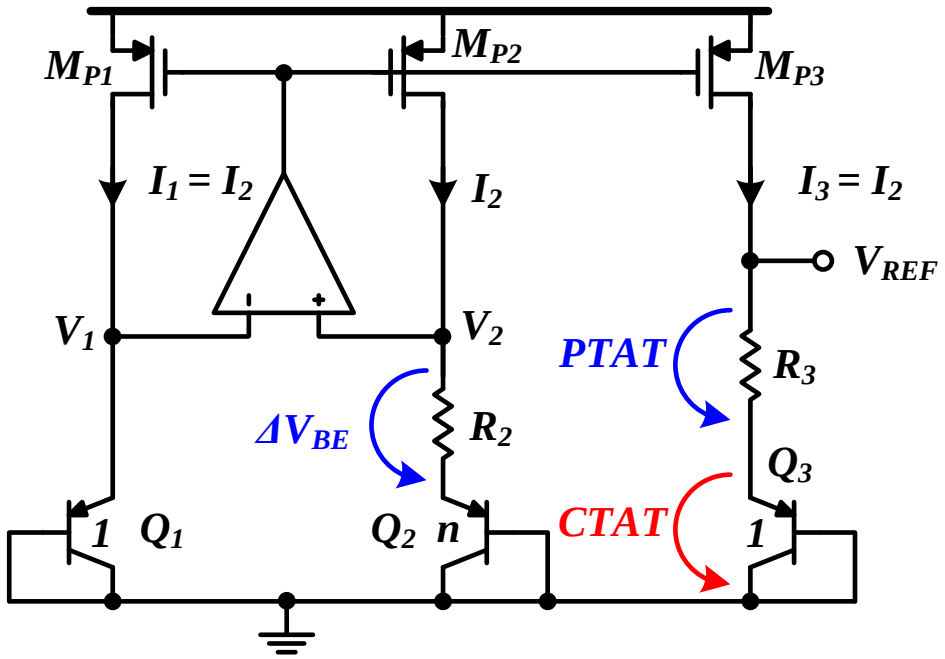
CMOS BGR Example (1)

- Current mirror: M_{P1-3}
- A-block: $M_{N1,2}$ → Same current → Same V_{GS}
- Choice of L and W
  - Large L ($> 1\mu m$) is usually used: Reduce CLM and flicker noise.
  - For low supply voltage, bias the transistors in MI or WI
    - Given L, g_m/I_D, and I_D → get W from charts / look-up tables



CMOS BGR Example (2)

- The op-amp keeps V_1 and V_2 at the same voltage.
- The op-amp can be implemented as a simple 5T OTA.
  - Folded cascode may be used if wide input range is required.
- Bias the op-amp using a constant-gm circuit.
  - Or use the BGR itself to bias it (self-biased)!

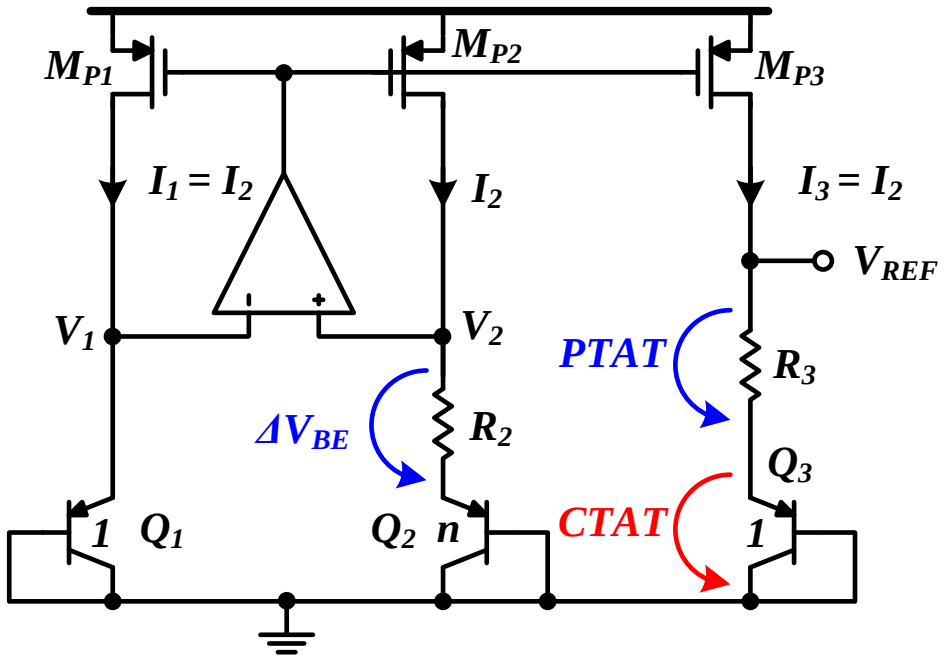


Positive or Negative FB?

- Cut the loop at OTA output: We must guarantee $\beta_N > \beta_P$.
- Note that $M_{P1,2}$ add 180^o phase shift.

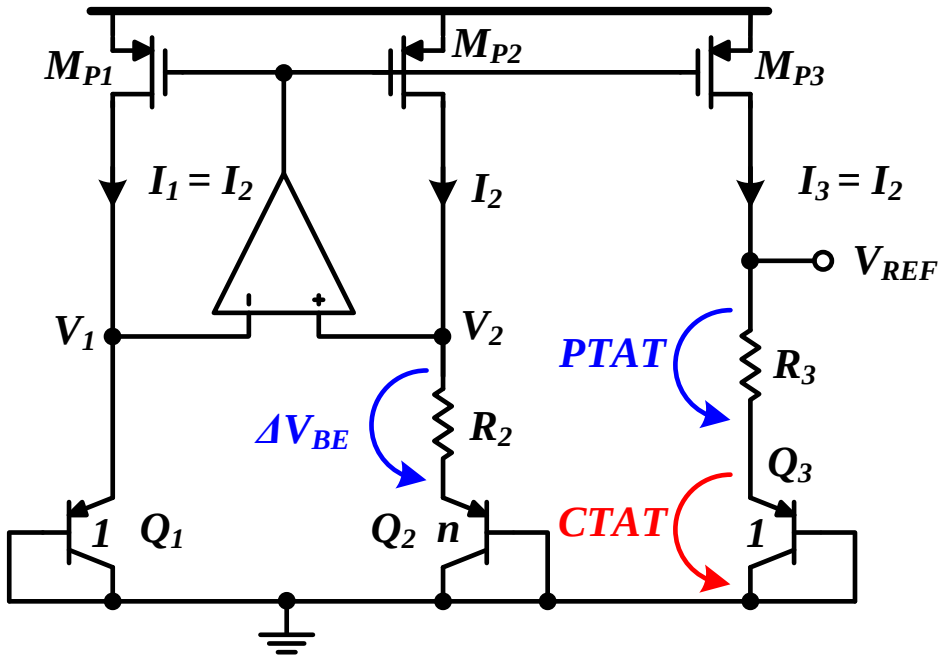
$$\beta_N \approx g_{mP2}\left(R_2 + 1/g_{mQ}\right) \qquad \beta_P \approx g_{mP1}\left(1/g_{mQ}\right)$$

- Ex: To set $\beta_N > 2\beta_P$ → $R_2 > \frac{1}{g_m} = \frac{V_T}{I_C}$ → $V_{R_2} = V_T \ln n > V_T$



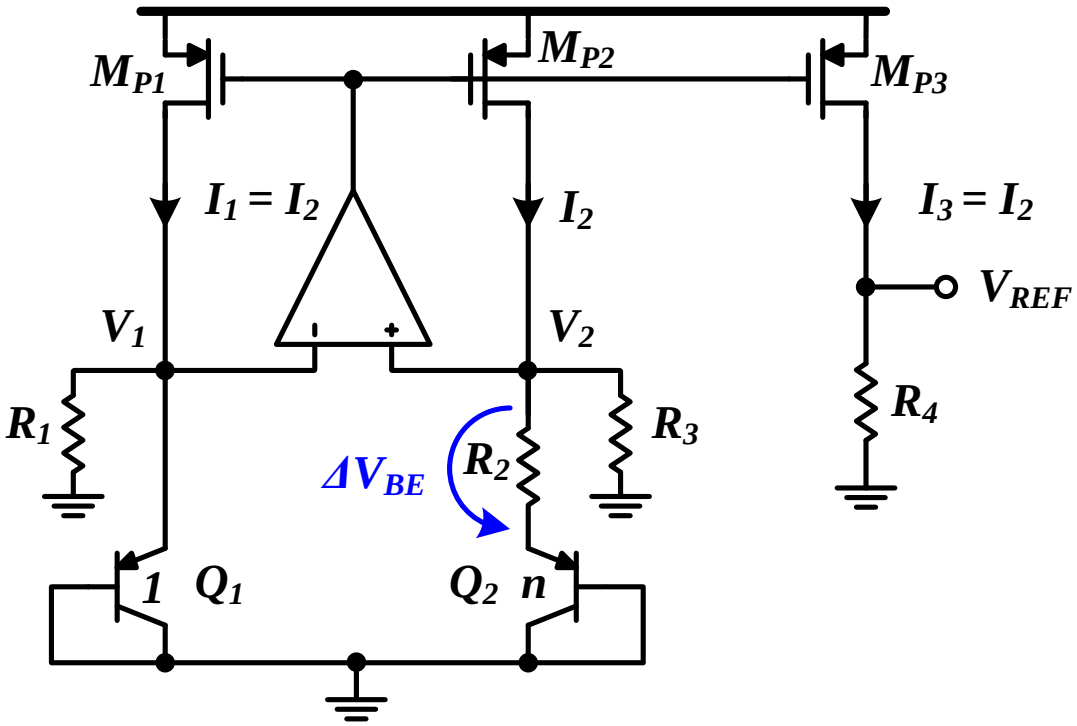
Low Voltage BGR: How?

- Adding PTAT and CTAT in voltage domain gives $V_{REF} \approx 1.2V$.
- For modern technologies, this value is higher than V_{DD} itself!
- The solution is to add PTAT and CTAT in the current domain.



Low Voltage BGR

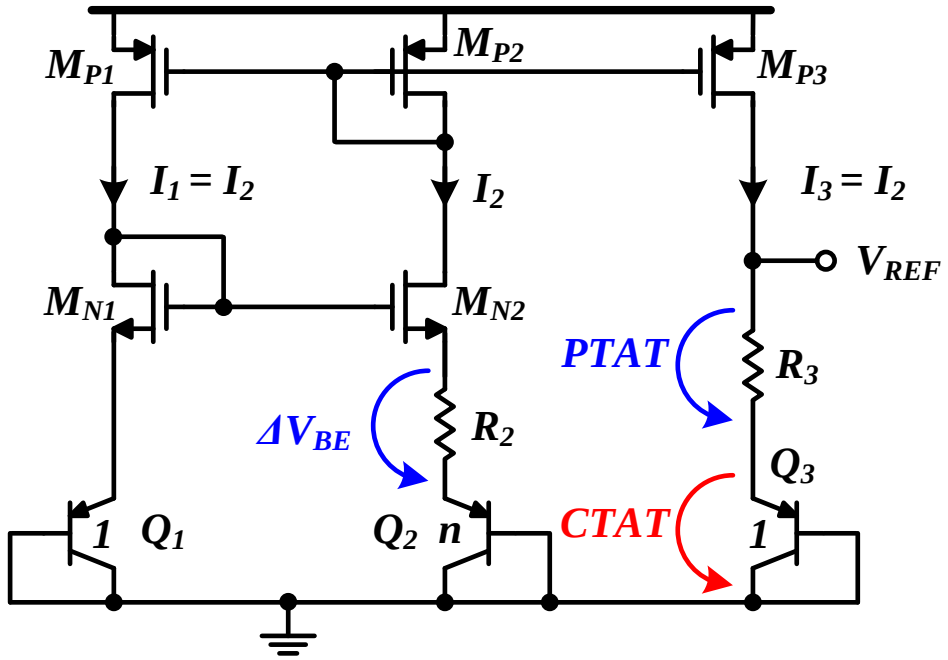
- Q2 carries PTAT current
- R_3 converts CTAT voltage (V_{BE1}) to CTAT current.
- R_1 maintains $I_{E1} = I_{E2}$
- I_2 is PTAT + CTAT = ZTAT
- $V_{BG} = R_4\left(\frac{\Delta V_{BE}}{R_2} + \frac{V_{BE1}}{R_3}\right) < 1.2V$



H. **Banba** et al., "A CMOS Bandgap Reference Circuit with Sub-1-V Operation," IEEE J. of Solid-State Circuits, vol. 34, pp. 670–674, May 1999.

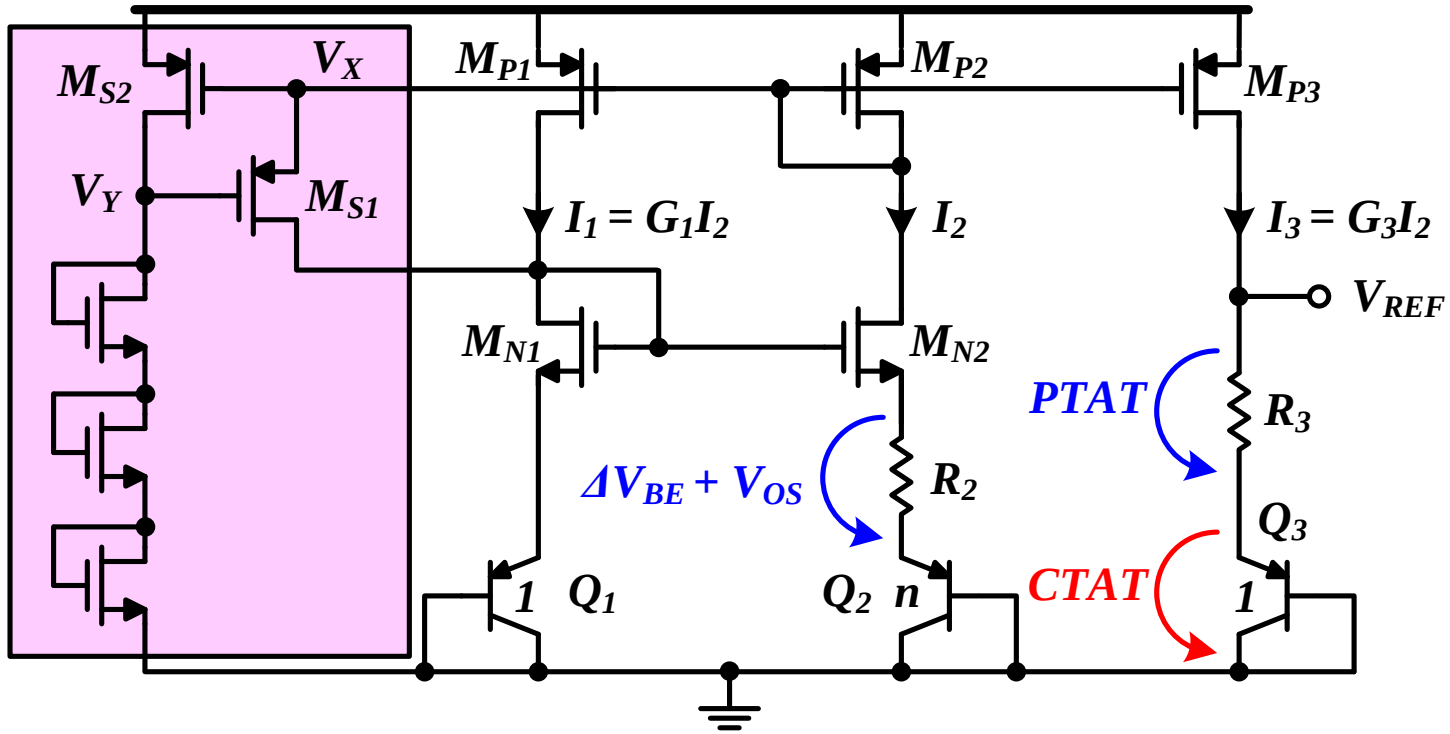
The Start-up Problem

- All currents = 0 is another valid solution for the circuit!
- Start-up circuit must drive the circuit out of the zero bias point.
  - Then it should automatically turn-off or consume little current
- Start-up verified by ramping-up VDD from zero in DC sweep and transient simulations.



Startup Circuit Example

- Startup problem means $V_X = V_{DD}$ and $V_Y = 0$.
  - M_{S1} will turn on charging the gates of $M_{N1,2}$.
  - $Q_{1,2}$ will turn on and the BGR starts.
  - V_Y will increase turning off M_{S1} and driving M_{S2} in linear region.



BGR Curvature

- PTAT and CTAT are **not perfectly linear.**
  - They both have convex upward curvature → Curvatures add!
- If expressed mathematically:

$$V_{PTAT} \approx a_1 T - a_2 T^2$$

$$V_{CTAT} \approx V_{G0} - b_1 T - b_2 T^2$$

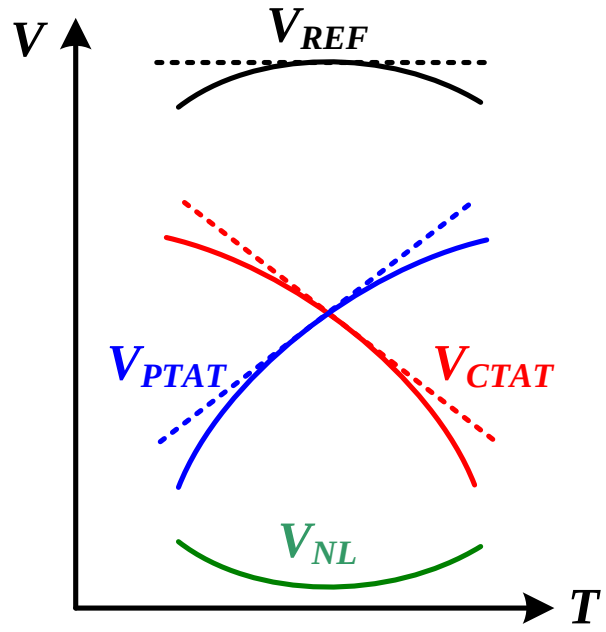
$$V_{REF} \approx V_{G0} + (a_1 - b_1) T - (a_2 + b_2) T^2$$

- We can set $a_1 = b_1$
- But a_2 and b_2 add (convex upward)

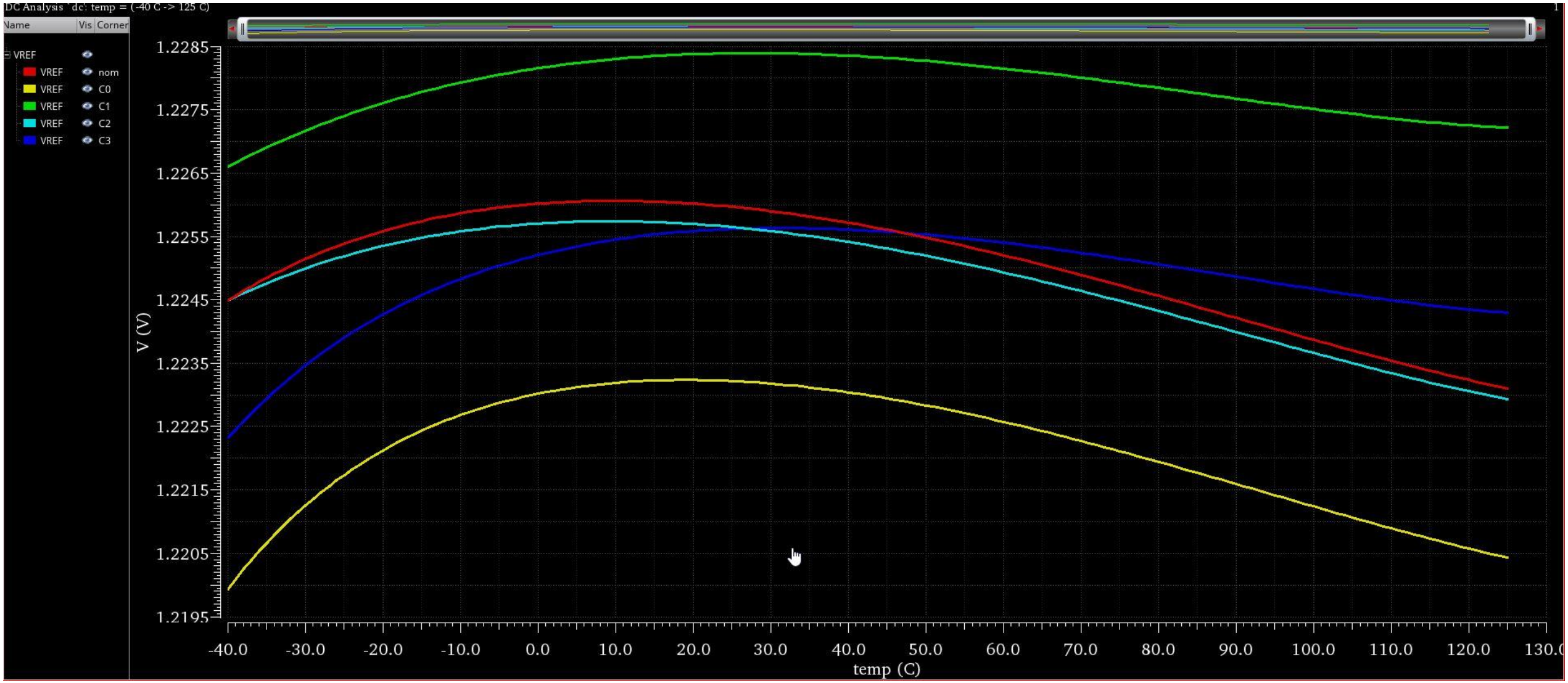
$$V_{REF} \approx V_{G0} - (a_2 + b_2) T^2$$

- Curvature can be corrected by adding a **convex downward** signal (e.g., PTAT^2).

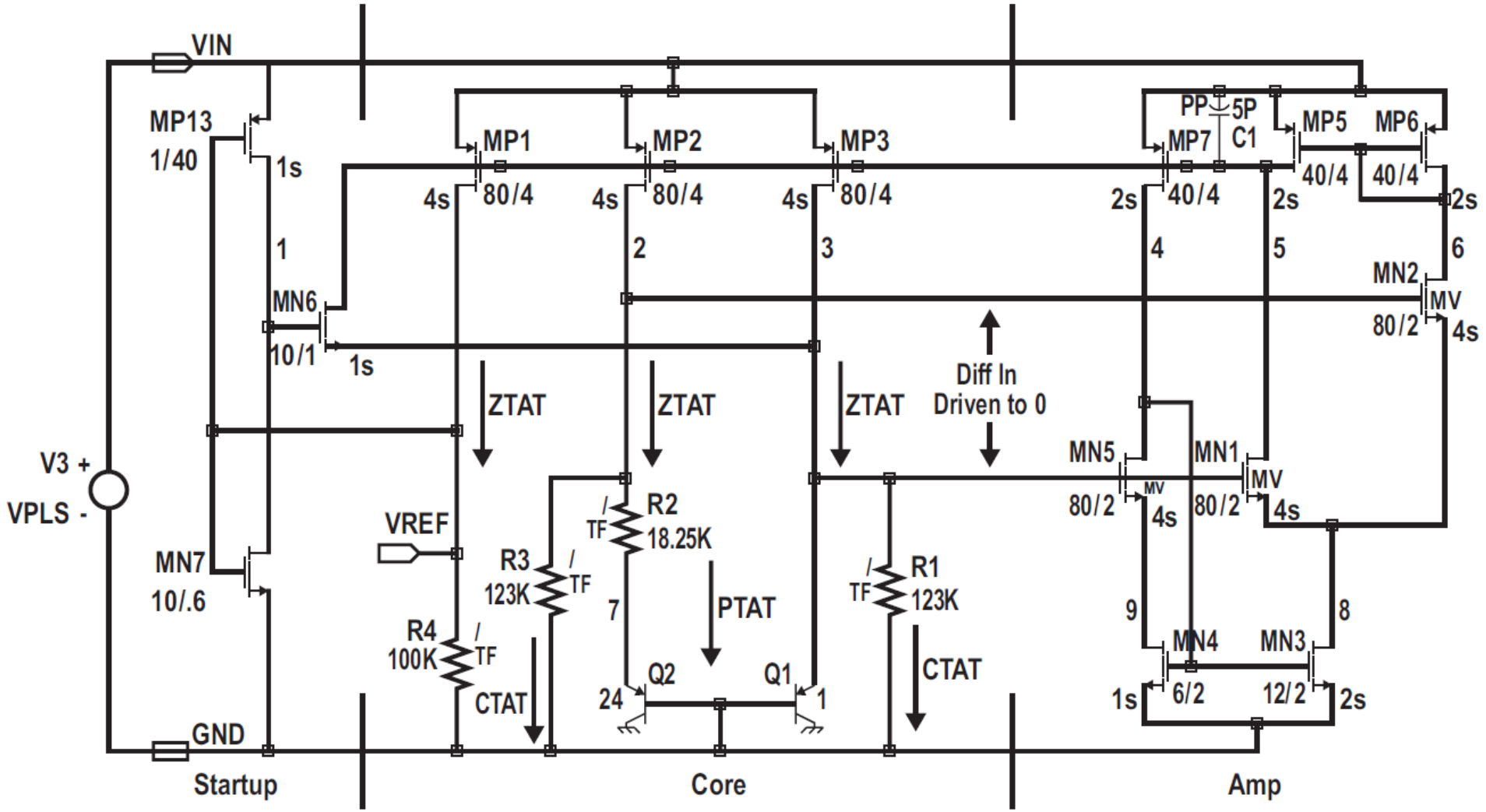
$$V_{NL} \approx c_2 T^2 \rightarrow c_2 = a_2 + b_2$$



Example of BGR Simulation Results



Complete BGR Example



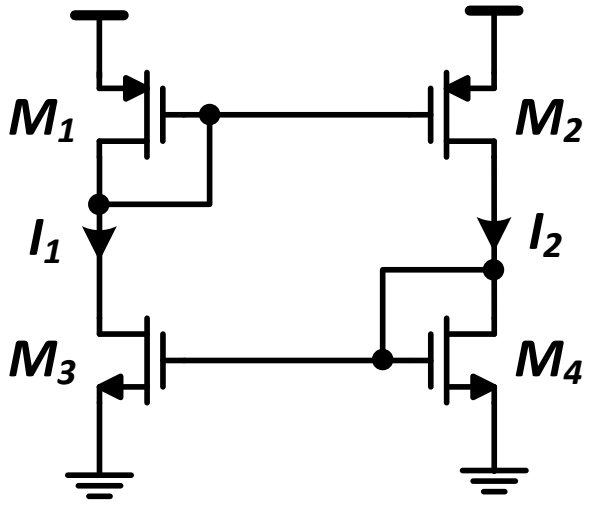
[Brokaw, IDT, 2011]

Outline

- Reference circuits
- Bandgap reference (BGR) circuit
  - BGR basic operation
  - BGR practical CMOS implementation
- Constant-gm circuit

Supply Independent Reference Current

- To avoid V_{DD} dependence, the circuit must bias itself!
- The circuit is governed by only one equation: $I_1 = I_2$
- The currents are supply-independent (if CLM is neglected)
  - But they are undefined!
  - To uniquely define the currents, we must add another constraint to the circuit



Self-Biased Circuit

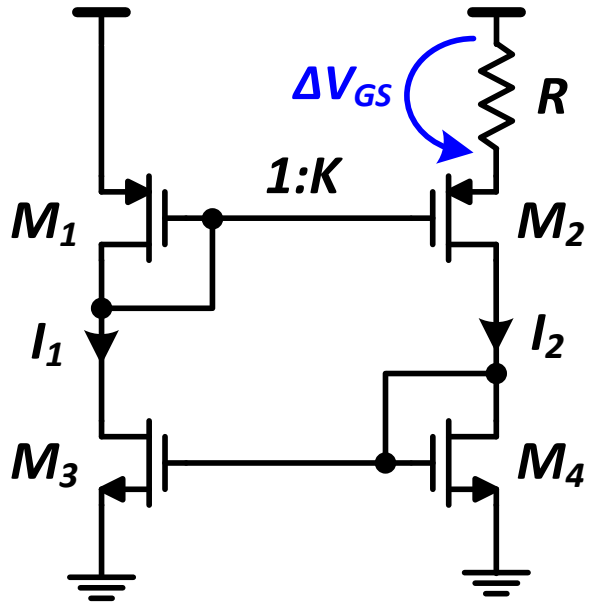
- Assume sq. law is valid:

$$I_D = \frac{\beta}{2}(V_{GS} - V_{TH})^2$$

$$\frac{\beta_2}{\beta_1} = \frac{W_2}{W_1} = K$$

$$\Delta V_{GS} = \sqrt{\frac{2I_{1,2}}{\beta_1}} - \sqrt{\frac{2I_{1,2}}{K\beta_1}} = I_{1,2}R$$

- Solve quadratic equation for $\sqrt{I_{1,2}}$
  - 1st soln: $\sqrt{I_{1,2}} = 0$
    - Startup circuit is required!
  - 2nd soln: $\sqrt{I_{1,2}} = \frac{1}{R}\sqrt{\frac{2}{\beta_1}}\left(1 - \frac{1}{\sqrt{K}}\right)$
    - Is this useful?



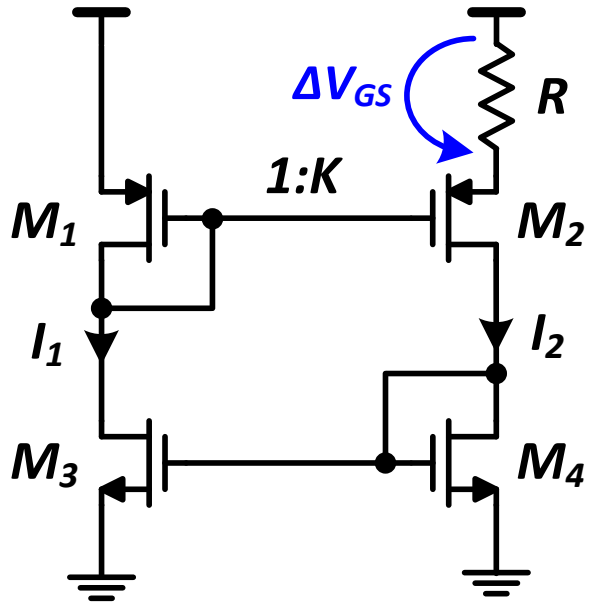
Self-Biased Circuit

$$I_{1,2} = \frac{1}{R^2} \cdot \frac{2}{\beta_1}\left(1 - \frac{1}{\sqrt{K}}\right)^2$$

- $I_{1,2}$ independent of supply, but depends on process and temp

$$g_{m1} = \sqrt{\beta_1 \cdot 2I_1} = \frac{2}{R}\left(1 - \frac{1}{\sqrt{K}}\right)$$

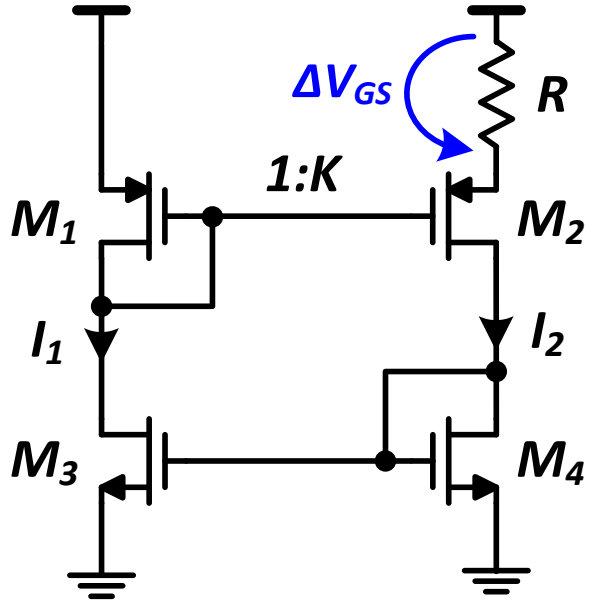
- Independent of process, supply, and temperature
  - Assuming ideal R



Constant-g_m Circuit

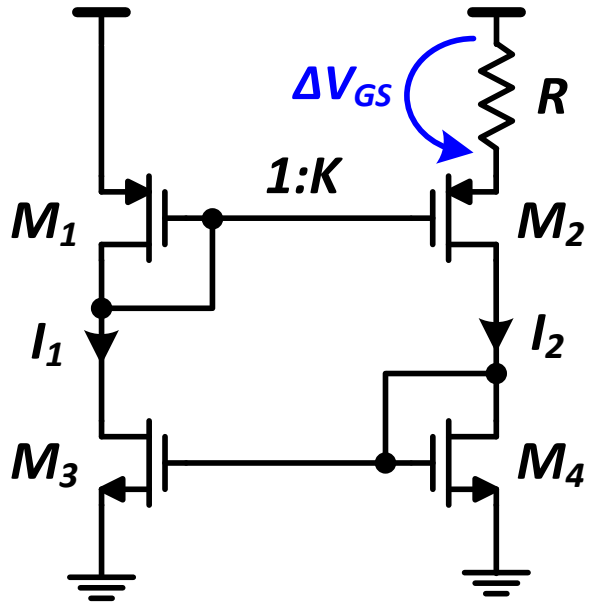
$$g_{m1} = \sqrt{\beta_1 \cdot 2I_1} = \frac{2}{R}\left(1 - \frac{1}{\sqrt{K}}\right)$$

- Independent of process, supply, and temperature
  - Assuming ideal R
- g_m is what actually matters!
  - Determines gain, noise, and speed.
  - We want constant-g_m!
- Ex: $K = 4$ ➔ $g_{m1} = \frac{1}{R}$
  - Let $|A_v| = g_{m1}R_D = \frac{R_D}{R} = constant$!
- It can be shown that g_m is still constant even if biased at MI or WI!



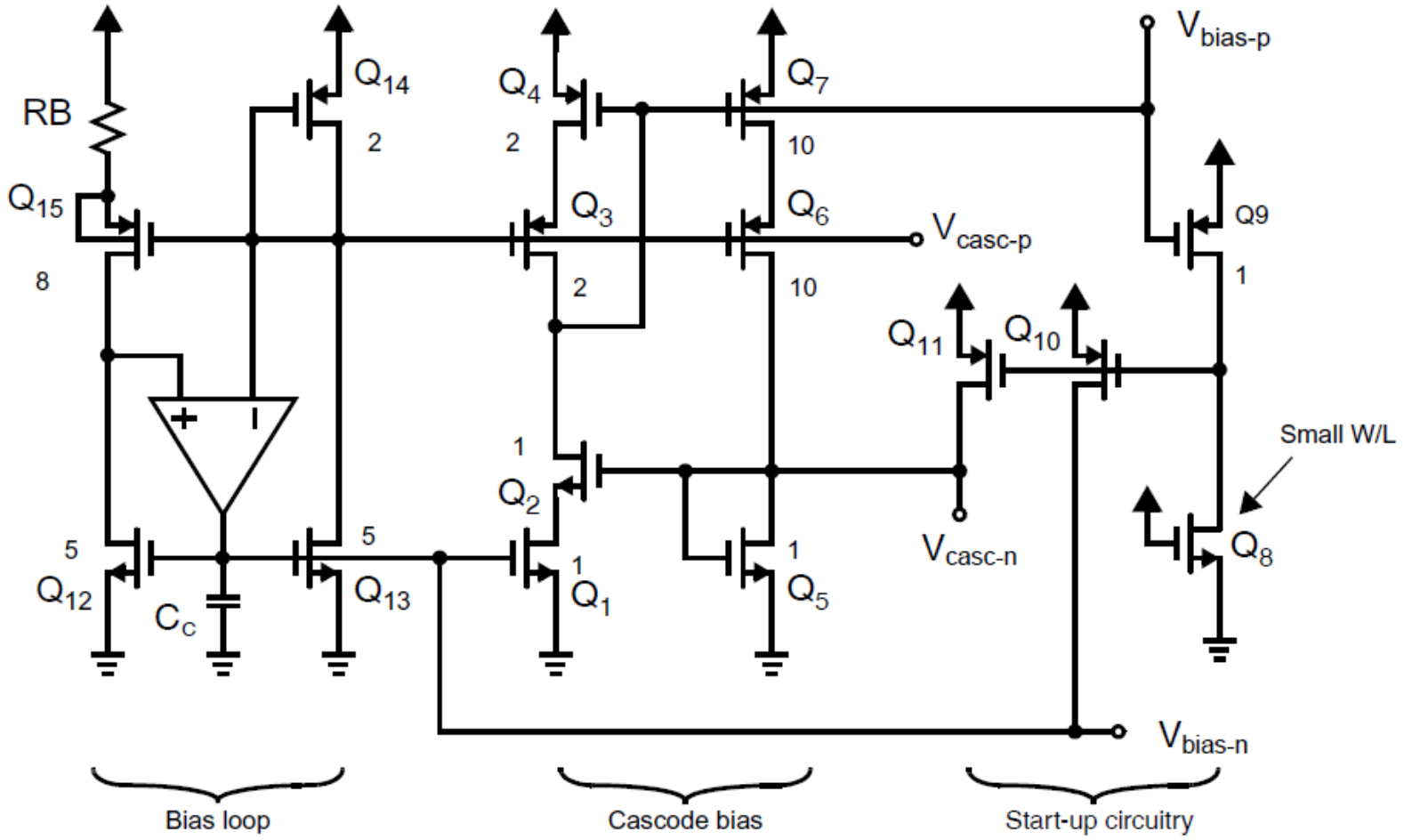
Quiz

- Note that the FB loop formed by M1-M4 is a +ve FB loop.
  - Does it oscillate?
  - Find the loop gain and find the stability condition (LG < 1)
  - Is the stability affected if R is off-chip?



OTA Bias Circuit Example

- $Q_{12,13} \rightarrow V_{bias-n} \rightarrow Q_1 \rightarrow Q_4 \rightarrow V_{bias-p}$
- $Q_4 \rightarrow Q_7 \rightarrow Q_5 \rightarrow V_{casc-n}$ $(I_{Q5} = 5 \times I_{Q1})$
- $Q_{14} \rightarrow V_{casc-p}$ $(I_{Q14} = 5 \times I_{Q4})$
- Startup: Q_8 (large res) → $Q_{10,11}$ (ON) → $Q_{5,13}$ → Q_9 → $Q_{10,11}$ (OFF)



MOSFET Temperature Effects

- V_{TH} of long channel MOS:

  $\partial V_{THN}/\partial T \approx -1\ mV/K$ and $\partial V_{THP}/\partial T \approx -1.4\ mV/K$

- V_{TH} of short channel MOS:

  $\partial V_{THN}/\partial T \approx -0.6\ mV/K$ and $\partial V_{THP}/\partial T \approx -0.6\ mV/K$

- Mobility: $\mu \approx \mu(T_o)\left(\frac{T_o}{T}\right)^{1.5}$

- V_{TH} dominate at low V_{GS} (WI): $I_D \uparrow$ with temperature

- μ dominate at high V_{GS} (SI): $I_D \downarrow$ with temperature

Thank you!

References

- B. Razavi, “Design Of Analog CMOS Integrated Circuit,” 2nd ed., McGraw-Hill, 2017.
- T. C. Carusone, D. Johns, and K. W. Martin. “Analog Integrated Circuit Design,” 2nd ed., Wiley, 2012.
- R. J. Baker, “CMOS circuit design,” 3rd ed., Wiley, 2010.