وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

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Analog IC Design (Xschem, Ngspice, ADT)
Lab 03
Cascode Amplifier

Intended Learning Objectives

In this lab you will:

- Learn how to use the Sizing Assistant (SA) to size the transistors.
- Design and simulate a cascode amplifier.
- Design a bias circuit for the cascode amplifier.
- Investigate the gain, the bandwidth, and the GBW of a cascode amplifier.

Part 1: Device Sizing Using SA

1) From the square law, we have

$$g_m = \frac{2I_D}{V_{ov}} \rightarrow V_{ov} = \frac{2}{g_m/I_D}$$

For a real MOSFET, if we compute V_{ov} and $\frac{2}{g_m/I_D}$ they will not be equal. In the previous lab we defined V-star (V^*), which is calculated from actual simulation data using the formula

$$V^* = \frac{2}{g_m/I_D} \leftrightarrow g_m = \frac{2I_D}{V^*}$$

The lower the V^* the higher the g_m, but the larger the area and the lower the speed. An often used sweet-spot that provides good compromise between different trade-offs is $V^* = 200mV$.

2) Although the V^* is a nice parameter that is inspired by the square-law, it does not have an intuitive or a physical meaning (it is not an actual voltage in the circuit). We actually defined V^* in order to be able to define a relation between the g_m and I_D. Thus, the real parameter that we should care about is the g_m over I_D ratio (g_m/I_D).

If the square-law is valid

$$g_m = \frac{2I_D}{V_{ov}} \rightarrow \frac{g_m}{I_D} = \frac{2}{V_{ov}}$$

Using V^*

$$\frac{g_m}{I_D} = \frac{2}{V^*}$$

A small g_m/I_D means large V_{ov} (biasing in strong inversion) and a large g_m/I_D means small V_{ov} (biasing in weak inversion).

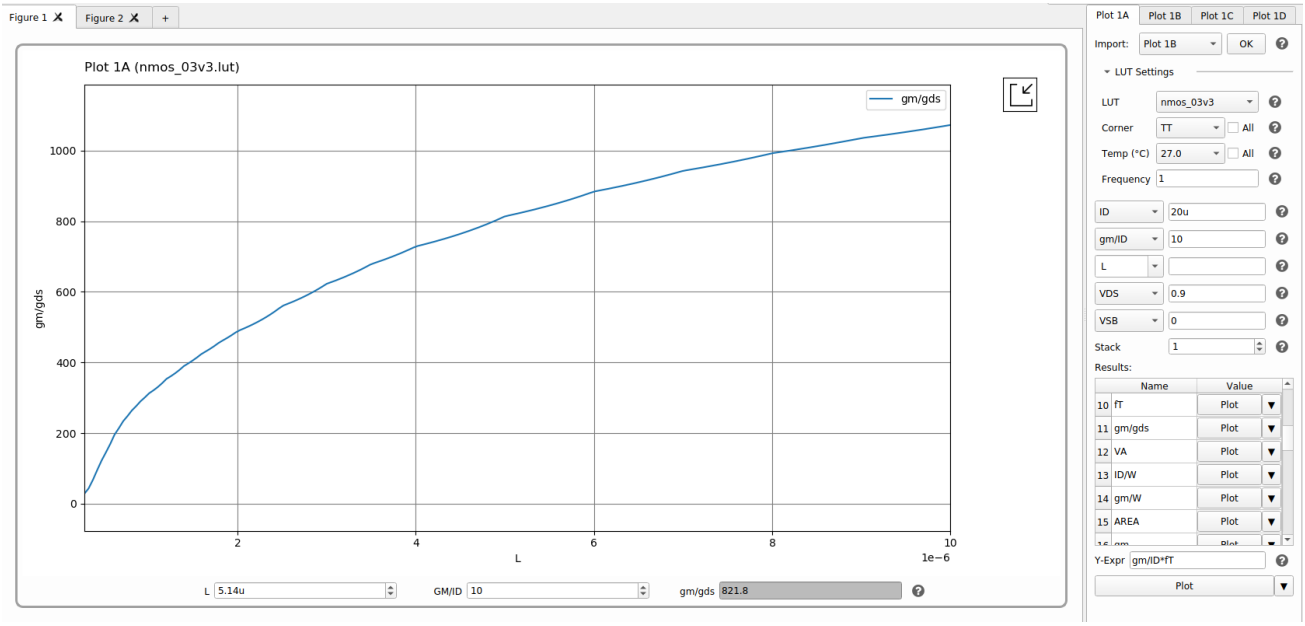
3) There are many good things about using the g_m/I_D as a design knob:

- The g_m/I_D gives a direct relation between the most important MOSFET parameter (gm) and the most valuable resource (ID). For example, a $g_m/I_D = 10\ S/A$ means you get $10\ \mu S$ of g_m for every $1\ \mu A$ of bias current.
- The g_m/I_D is a normalized knob: it has a limited search range (typically from 5 to 25 S/A) independent of the technology or the device type.
- The g_m/I_D is intuitive because it tells you directly about the inversion level (bias point) and consequently all related trade-offs. For example, $g_m/I_D = 5\ S/A$ means strong inversion (SI), $g_m/I_D = 15\ S/A$ means moderate inversion (MI), and $g_m/I_D = 25\ S/A$ means weak inversion (WI).
- The g_m/I_D is an orthogonal knob: If we define the g_m/I_D then we define the inversion level (bias point). If you change I_D or L while keeping g_m/I_D fixed, then the inversion level (bias point) is kept fixed. The W is treated as an output variable instead of being treated as an input variable.
- The higher the g_m/I_D (the lower the V^*) the higher the efficiency and the headroom (the available swing), but the larger the area and the lower the speed. An often used sweet-spot that provides good compromise between different trade-offs is $g_m/I_D = 10\ S/A$ ($V^* = 200mV$). Larger g_m/I_D is usually used for low-voltage and low-power designs.

4) We want to design a common source (CS) amplifier that has ideal current source load with the following parameters.

Parameter	Value
$A_v = g_m r_o$	50
g_m/I_D	$10\ S/A$
Supply (V_{DD})	$1.8\ V$
Quiescent (DC) output voltage	$V_{DD}/2 = 0.9\ V$
Bias Current	$20\ \mu A$

5) Since the square-law is not accurate, we cannot use it to calculate the sizing. Instead, we will use the Sizing Assistant (SA) which is a powerful analog calculator that uses LUTs that are pre-generated from the simulations. Sweep L and plot gm/gds. Pick L.



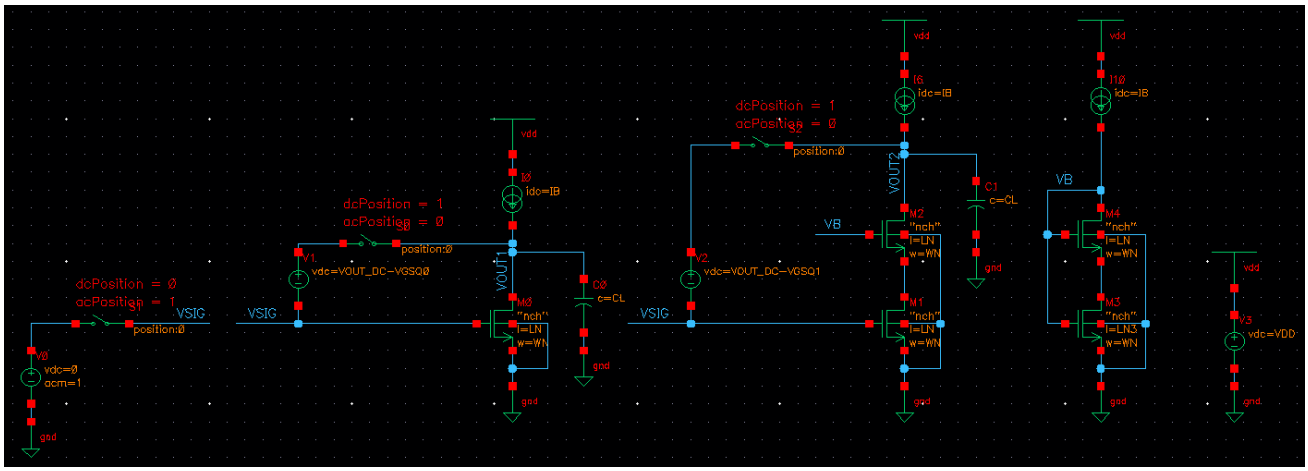
6) Fill the picked L back into SA to get W.

7) Notice that gm/gds depends on VDS. For the picked L, plot gm/gds vs VDS=0:0.9.
8) For the cascode amplifier, we will use the same sizing, but the VDS will be split across two transistors. What is the expected gm/gds?

Part 2: Cascode for Gain

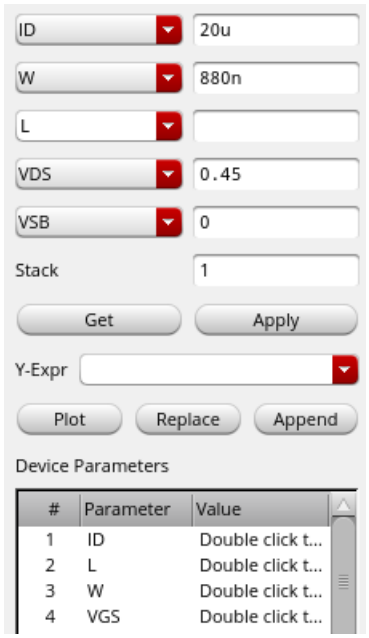
1. OP Analysis

1) Create a new schematic. Construct the circuit shown below. Use $I_B = 20\mu A$. Use L and W as selected in Part 1 for M0, M1, M2, and M4. Use the same W for M3 but it will have different L as will be shown later. Use $C_L = 1pF$.

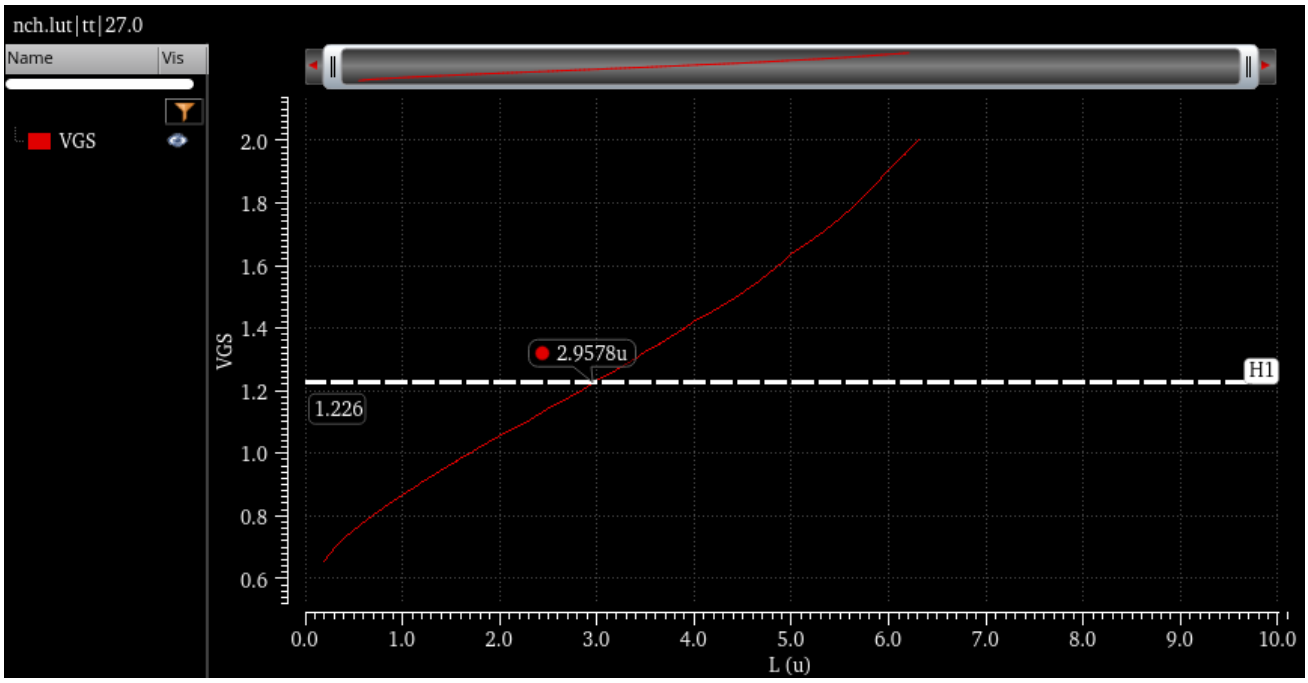


2) We need to set the quiescent (DC) output voltage of the amplifiers to bias the transistors in saturation. However, the output node is a high impedance node; thus, it is difficult to control its DC voltage.
3) As a simulation workaround, we use res_ac with different resistance values in DC/AC analysis so that it acts as s.c. or o.c. depending on the simulation type. At DC, the transistor is diode connected and V_{GS} is set by the current source. At AC, the diode connection is removed, and the input signal source is applied.
4) For the cascode amplifier, we will design V_B to set $V_{DS1} \approx V_{DS2} \approx 0.45\ V$ as will be shown shortly.
5) A dc shift (V1 and V2) is used to set the quiescent (DC) output voltage "roughly" to the required value. Setting the output voltage to exactly $0.9\ V$ is neither practical nor required. V_{GS0} and V_{GS1} can be retrieved from SA. Note that $V_{DS0} \approx 0.9\ V$ but $V_{DS1} \approx 0.45\ V$ so V_{GS0} and V_{GS1} will be slightly different. This can be ignored as V_{GS} is already always affected by V_{TH} variations, so a precise value is neither practical nor required.
6) To calculate V_B we need to find V_{GS2} because $V_B = V_{GS2} + V_{DS1}$. Note that M2 experiences body effect, so its V_{GS} will be higher than M0 and M1.

7) M3 and M4 form ***the magic battery*** that will be used to generate the cascode bias voltage. Note that M4 is always in saturation and M3 is always in triode (why?). We need to find the L of M3, so we set a sweep for M3 as shown below.
   ➔ Note: We can also keep L fixed and sweep W to get higher VGS. Note that to get higher VGS we need to make L longer, or W smaller. Sometimes we have to do both.



8) Plot V_{GS} and find L that gives the required $V_{GS} = V_B = V_{GS2} + V_{DS1}$.



9) Simulate the DC OP point of the above CS and cascode amplifiers. Report a snapshot showing the following parameters for M0 to M4 in addition to DC node voltages clearly annotated.

ID
VGS
VDS
VTH
VDSAT
GM
GDS
GMB
CDB
CGD
CGS
CSB

NOTE: "vdsat" is the minimum drain-source voltage required to bias the transistor in saturation. It is equal to V_{ov} for a square-law device. It is also referred to as "vdss" (drain-source saturation voltage) in some models. It is considered an ambiguous parameter because the transition from triode to saturation is gradual, not abrupt.

10) Check that all transistors operate in saturation. Does any transistor operate in triode? Why?
11) Do all transistors have the same vth? Why?
12) What is the relation ($\ll, <, \approx, >, \gg$) between gm and gds?
    NOTE: use $\gg$ or $\ll$ if the difference is 10 times or more (one order of magnitude).
13) What is the relation ($\ll, <, \approx, >, \gg$) between gm and gmb?
14) What is the relation ($\ll, <, \approx, >, \gg$) between cgs and cgd?
15) What is the relation ($\ll, <, \approx, >, \gg$) between csb and cdb?

2. AC Analysis

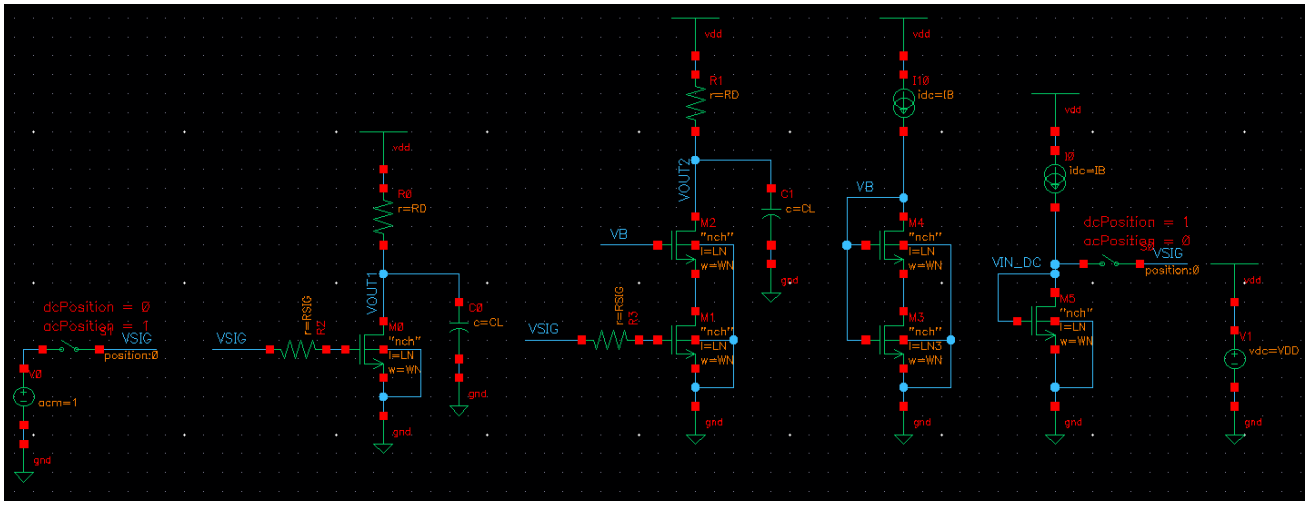
1) Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade) to simulate gain and bandwidth.
2) Use measure expressions to calculate parameters (DC gain, BW, GBW, and UGF) and export them to a text file.

3) Report the Bode plot (magnitude) of CS and cascode **appended on the same plot**.
4) Using small signal parameters from OP simulation or SA, perform hand analysis to calculate DC gain, BW, and GBW of both circuits.
5) Report a table comparing the DC gain, BW, UGF, and GBW of both circuits from simulation and hand analysis.
6) Comment on the results.

Part 3: Cascode for BW[1]

3. OP Analysis

1) Create a new schematic. Copy the old schematic instances to the new one. Make the following modifications:
    - Remove the feedback connection used to set the DC output voltage. The DC output voltage is going to be set by the voltage drop on the resistance.
    - Replace the current source with a resistor load R_D.
    - Create a diode connected transistor (M5) that is used to generate the DC bias input voltage of the two amplifiers (replica biasing). This voltage is connected to the amplifier in DC only. In AC analysis, the AC input source is connected.
    - Set $C_L = 1fF$ and the signal source resistance $R_{sig} = 10M\Omega$. This will make the dominant pole the input pole instead of the output pole.



2) Calculate R_D analytically such that the voltage drop on it is $\approx V_{DD}/2$ (the current remains roughly the same as in Part 2 because we are using the VGS generated by M5). Note that the DC voltage of the output node is set by the resistance (R_D); thus, we don't need a feedback loop as in the previous case.
3) Simulate the DC OP point of the new CS and cascode amplifiers. Report a snapshot showing the following parameters for M0 to M5 in addition to DC node voltages clearly annotated.

ID
VGS
VDS

[1] A relatively small L is necessary for Part 3 to make sure that Cgd is not negligible compared to Cgs. The L used in Part 2 is already reasonable.

VTH
VDSAT
GM
GDS
GMB
CDB
CGD
CGS
CSB

4) Check that all transistors operate in saturation. Does any transistor operate in triode? Why?

AC Analysis

1) Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade) to simulate gain and bandwidth.
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5) Report a table comparing the DC gain, BW, UGF, and GBW of both circuits from simulation and hand analysis. Comment on the results.

Lab Summary

In Part 1 you learned:

- How to find transistor sizing using the Sizing Assistant (SA).
- How to design a common-source and a cascode amplifier.

In Part 2 you learned:

- How to build a testbench for a cascode amplifier with current-source load.
- How to use cascode to boost the amplifier's gain.
- How to simulate the gain, the bandwidth and the GBW of a cascode amplifier with current-source load.

In Part 3 you learned:

- How to build a testbench for a cascode amplifier with resistive load.
- How to use cascode to boost the amplifier's bandwidth.
- How to simulate the gain, the bandwidth and the GBW of a cascode amplifier with resistive load.

Acknowledgements

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