Analog IC Design

Lecture 10
Current Mirrors

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Outline

1. Recapping previous key results
2. Why current source?
3. How to copy (mirror) currents?
4. Cascode current mirror
5. Wide-swing current mirror
6. Super cascode current mirror

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MOSFET in Saturation

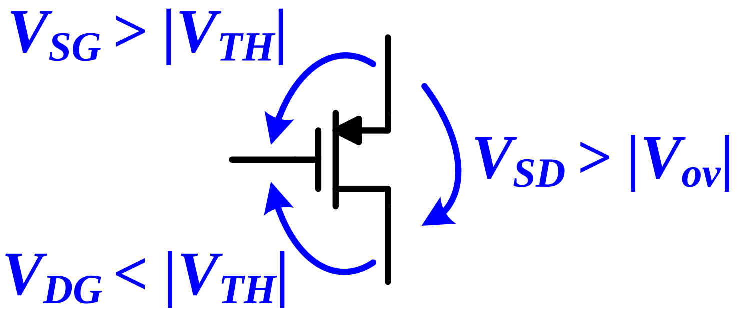
- The channel is pinched off if the difference between the gate and drain voltages is not sufficient to create an inversion layer

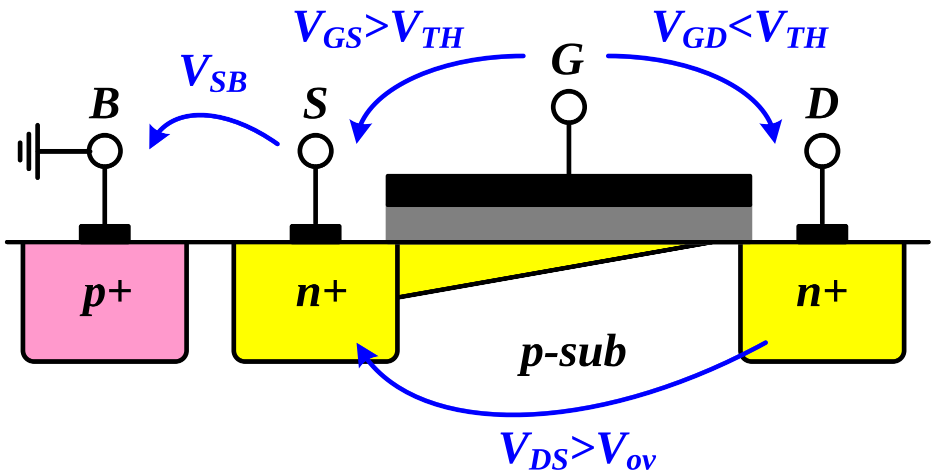
$$V_{GD} \leq V_{TH} \quad OR \quad V_{DS} \geq V_{ov}$$

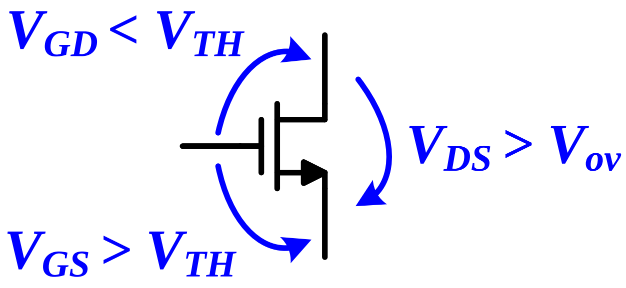
- Square-law (long channel MOS)

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \cdot V_{ov}^2 (1 + \lambda V_{DS})$$

$$V_{SB} \uparrow \;\Rightarrow\; V_{TH} \uparrow$$







Regions of Operation Summary

OFF (Subthreshold)

$V_{GS} < V_{TH}$

ON

$V_{GS} > V_{TH}$

Triode

$V_{DS} < V_{ov}$

Or

$V_{GD} > V_{TH}$

$$I_D = \mu C_{ox} \frac{W}{L} \left(V_{ov} V_{DS} - \frac{V_{DS}^2}{2} \right)$$

Pinch-Off (Saturation)

$V_{DS} \geq V_{ov}$

Or

$V_{GD} \leq V_{TH}$

$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} V_{ov}^2 (1 + \lambda V_{DS})$$

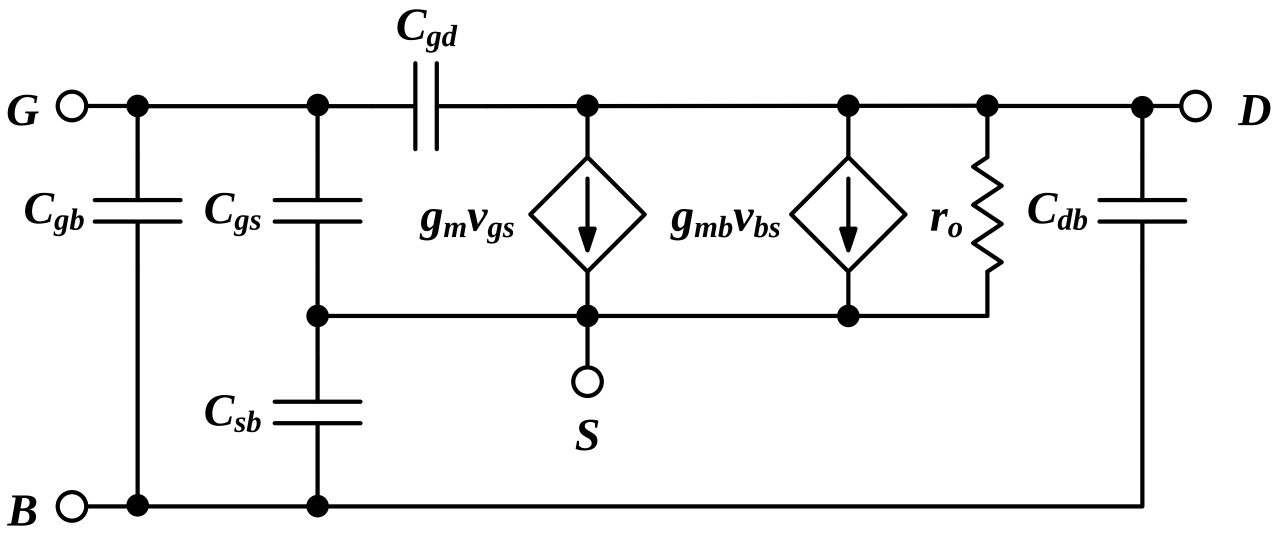
High Frequency Small Signal Model

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu C_{ox} \frac{W}{L} V_{ov} = \sqrt{\mu C_{ox} \frac{W}{L} \cdot 2 I_D} = \frac{2 I_D}{V_{ov}}$$

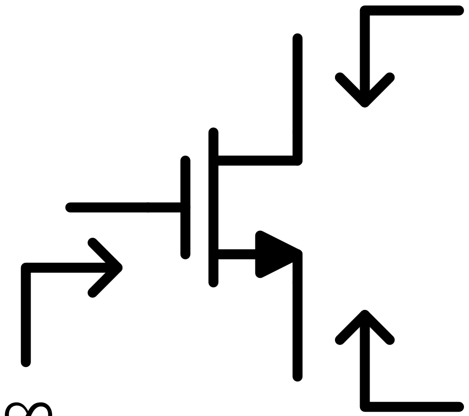
$$g_{mb} = \eta g_m \qquad \eta \approx 0.1 - 0.25$$

$$r_o = \frac{1}{\partial I_D / \partial V_{DS}} = \frac{V_A}{I_D} = \frac{1}{\lambda I_D} \qquad V_A \propto L \leftrightarrow \lambda \propto \frac{1}{L} \qquad V_{DS} \uparrow V_A \uparrow$$

$$C_{gb} \approx 0 \qquad C_{gs} \gg C_{gd} \qquad C_{sb} > C_{db}$$



Rin/out Shortcuts Summary



$$r_o[1 + (g_m + g_{mb})R_S]$$

H.I.N.

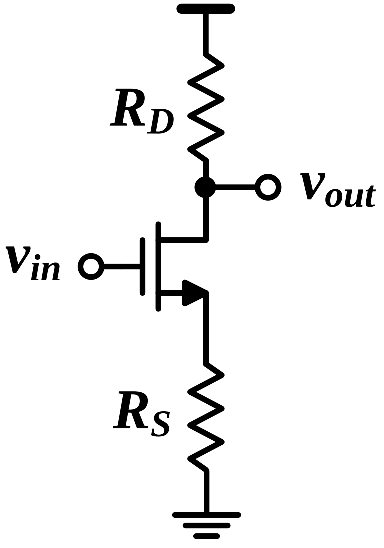
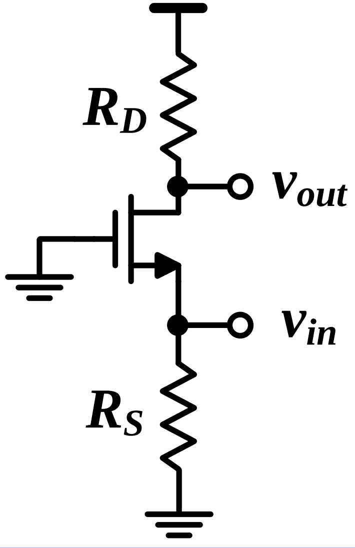
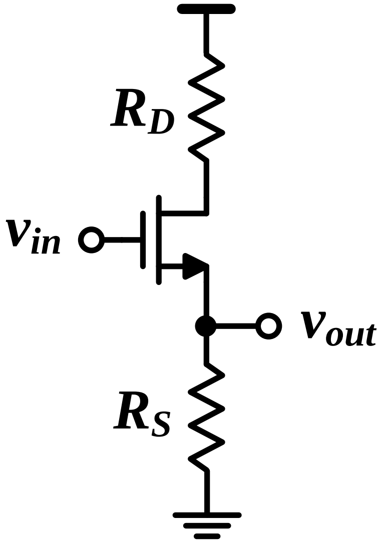
∞

At low frequencies **ONLY**

$$\frac{1}{g_m + g_{mb}}\left(1 + \frac{R_D}{r_o}\right)$$

L.I.N.

Summary of Basic Topologies

	CS	CG	CD (SF)
			
	Voltage & current amplifier	Voltage amplifier Current buffer	Voltage buffer Current amplifier
Rin	∞	$R_S \| \| \frac{1}{g_m + g_{mb}}\left(1 + \frac{R_D}{r_o}\right)$	∞
Rout	$R_D \| \| r_o[1 + (g_m + g_{mb})R_S]$	$R_D \| \| r_o$	$R_S \| \| \frac{1}{g_m + g_{mb}}\left(1 + \frac{R_D}{r_o}\right)$
Gm	$\boldsymbol{\frac{-g_m}{1 + (g_m + g_{mb})R_S}}$	$\boldsymbol{g_m + g_{mb}}$	$\boldsymbol{\frac{g_m}{1 + R_D/r_o}}$

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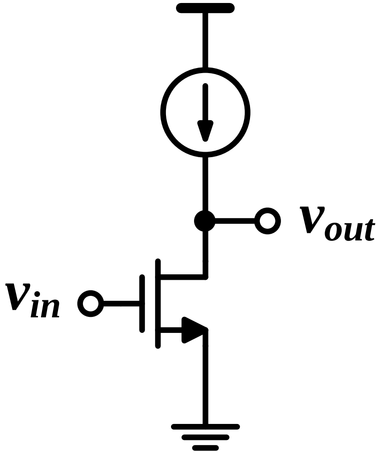
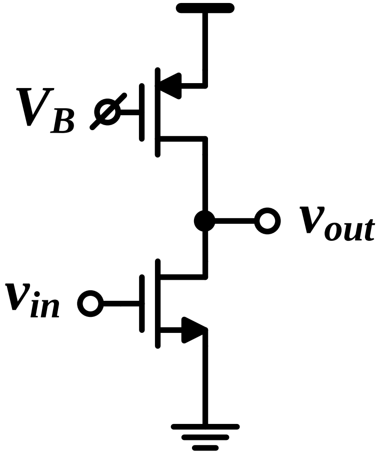
Why Current Source?

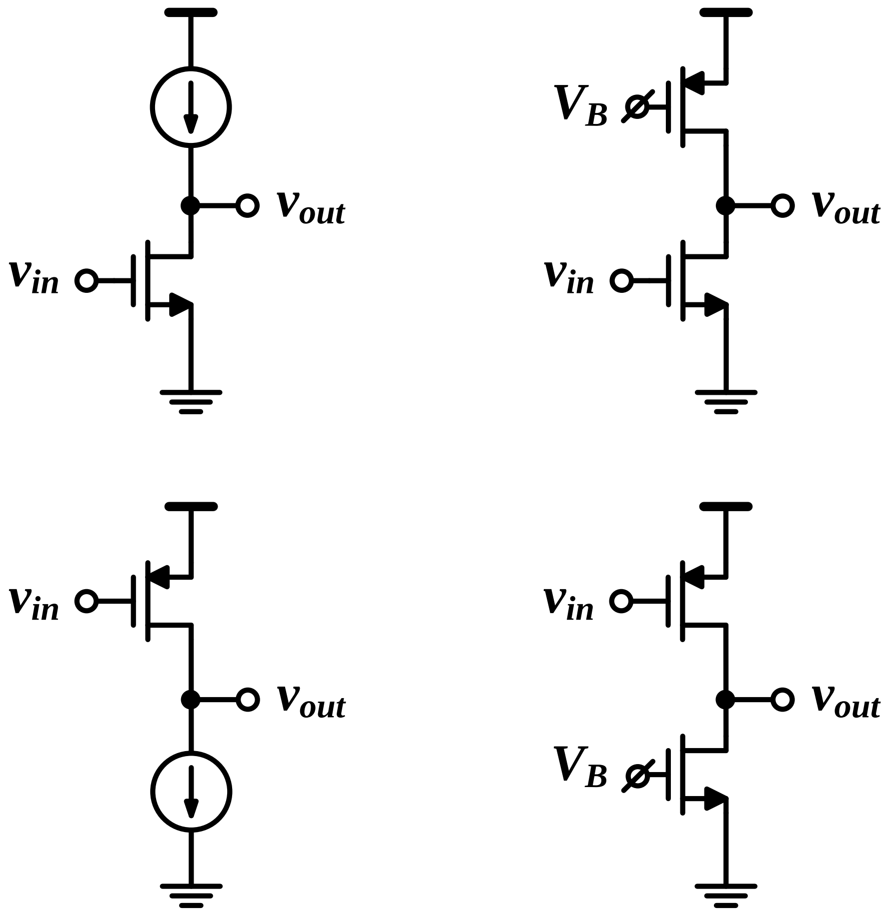
- A current source is an ideal load
  - Sets DC bias point accurately
  - Infinite R_{out} (ac o.c.)
  - No DC voltage drop
  - Small chip area
- Simply, a large resistor without the large resistor drawbacks
- The current source is practically implemented using a MOSFET
  - Finite $R_{out} = r_o$ and subtracts V_{ov} from voltage headroom





Sink and Source Currents

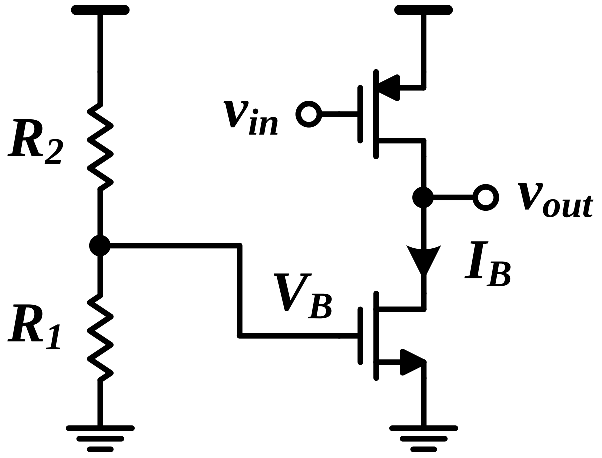
- Use PMOS to source current (from VDD)
- Use NMOS to sink current (to GND)



BAD Current Source

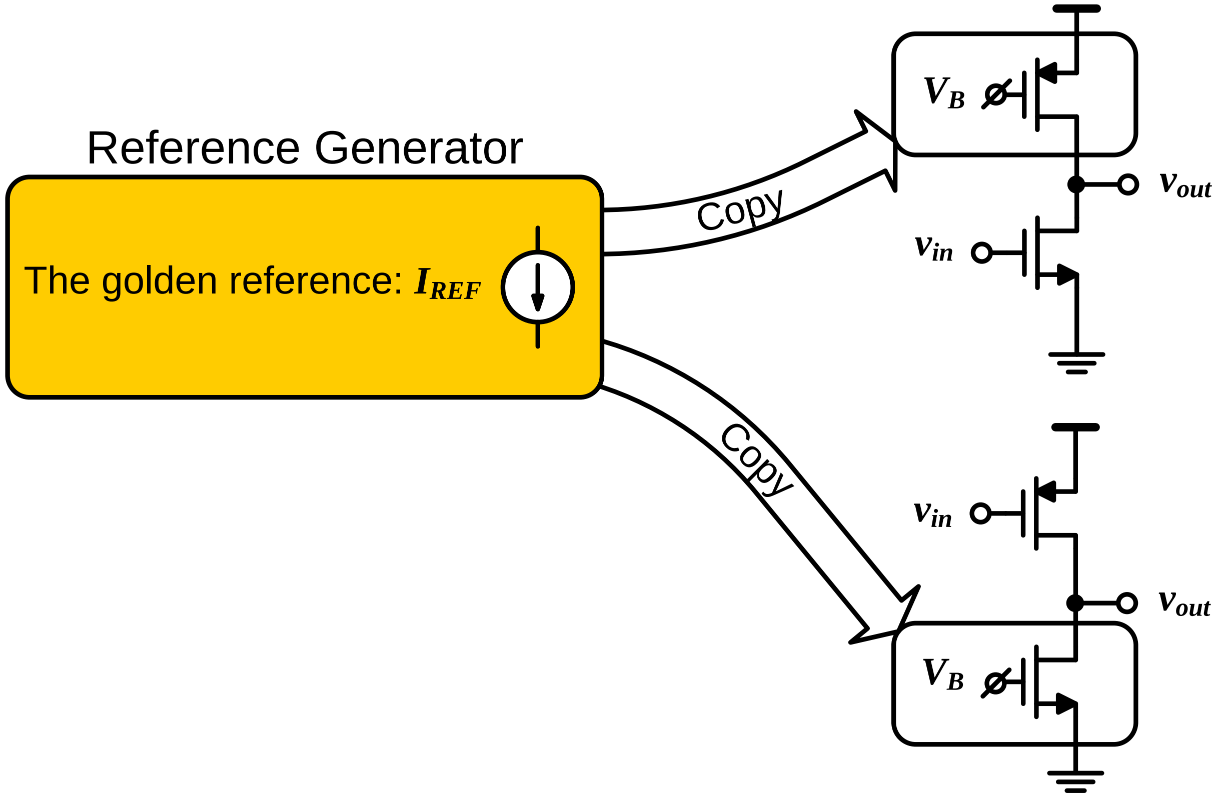
$$I_B \approx \frac{\mu C_{ox}}{2}\frac{W}{L}(V_B - V_{TH})^2 = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(\frac{R_1}{R_1 + R_2}V_{DD} - V_{TH}\right)^2$$

- Sensitive to PVT (process, voltage, and temperature) variations
  - P: V_{TH} may vary $\pm 50\ mV$
  - V: V_{DD} may vary $\pm 10\%$
  - T: μ varies a lot with temperature
- Even if V_B is stable, I_B will not be stable



How to Generate Robust Currents?

- The golden reference (I_{REF}) is designed to be PVT insensitive
  - I_{REF} is generated using a relatively complicated reference circuit
  - We cannot make a reference circuit for every biasing branch!
  - Solution: Make copies of I_{REF}.



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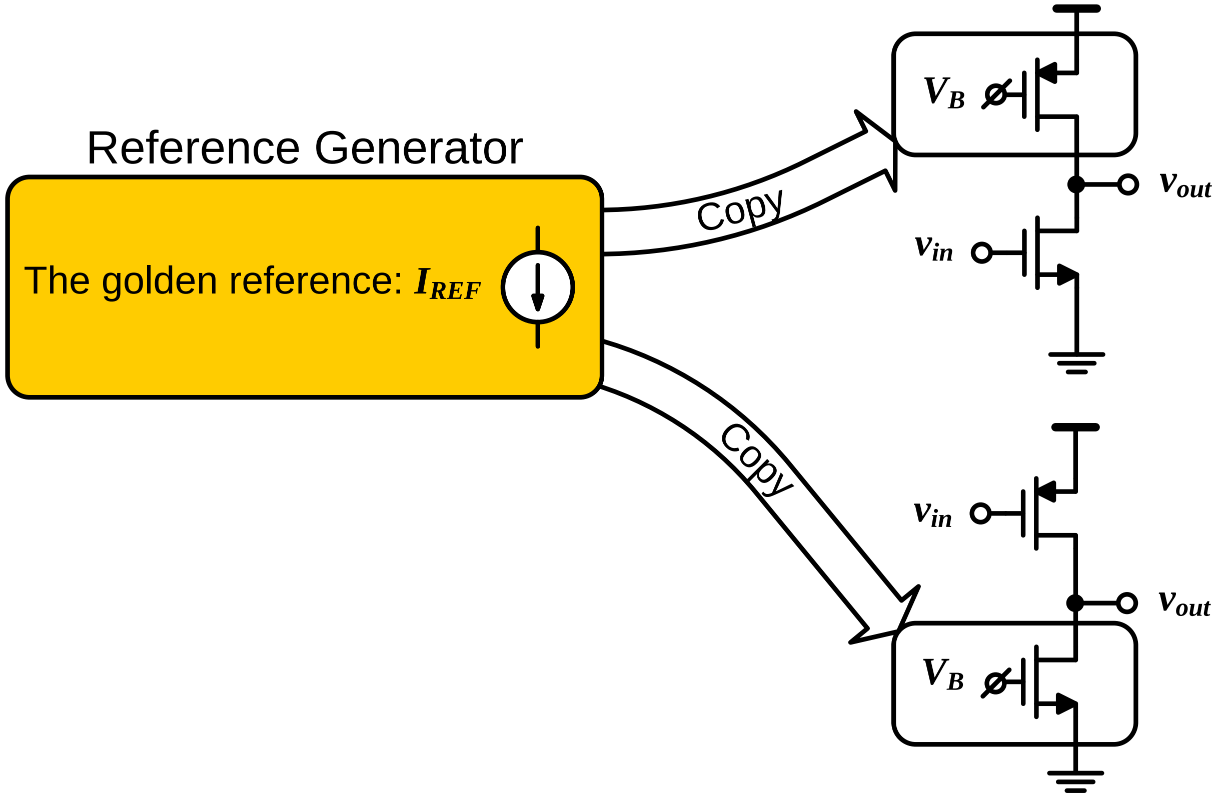
How to Copy (Mirror) Currents?

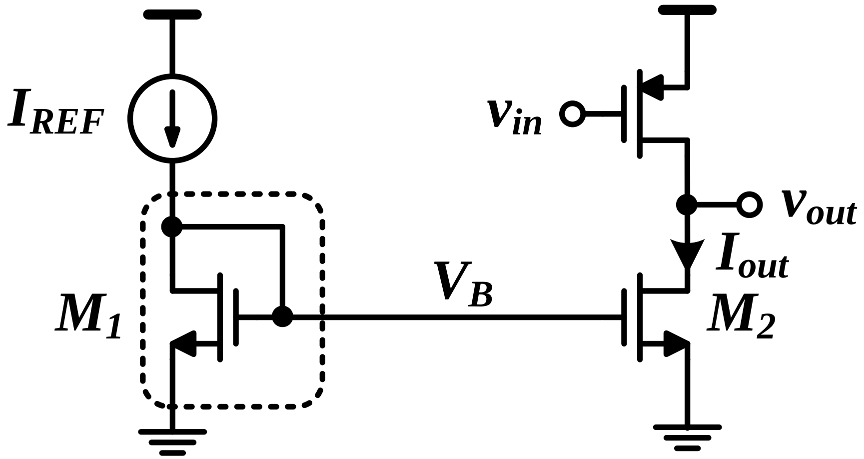
- We normally use the transistor to convert V to I
- We now need to convert I to V: convert I_{REF} to V_B
  - How to convert I to V?



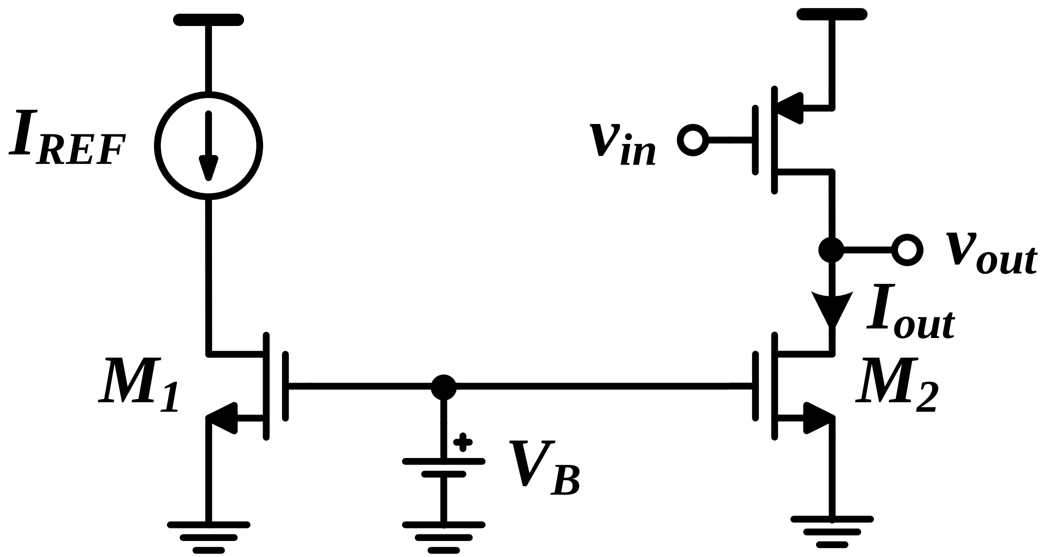
How to Copy (Mirror) Currents?

- We can convert I to V using a **diode connected transistor** (M1).
- M2 converts V back to I.
- M1 and M2 have the same V_{GS} and both work in saturation.
  - They will have the same current (if they are MATCHED).
- If sizing is different, we can scale I_{REF} up or down.
- I_{out} is **insensitive** to PVT variations.
  - But V_B may change due to PVT variations.

$$\frac{I_{out}}{I_{REF}} = \frac{\frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_2 (V_B - V_{TH})^2}{\frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_B - V_{TH})^2} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}$$

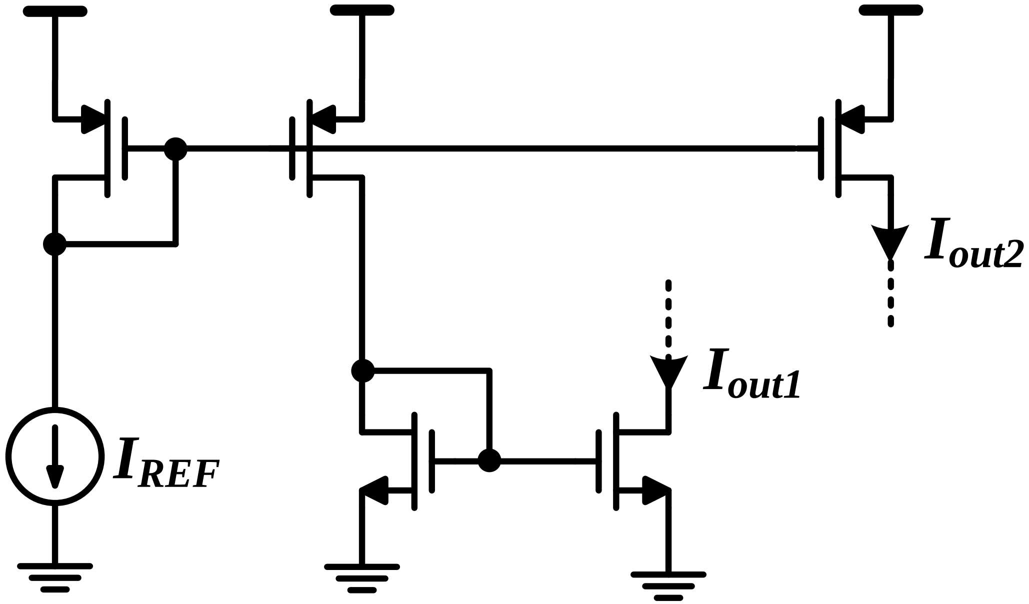


Is This a Current Mirror?



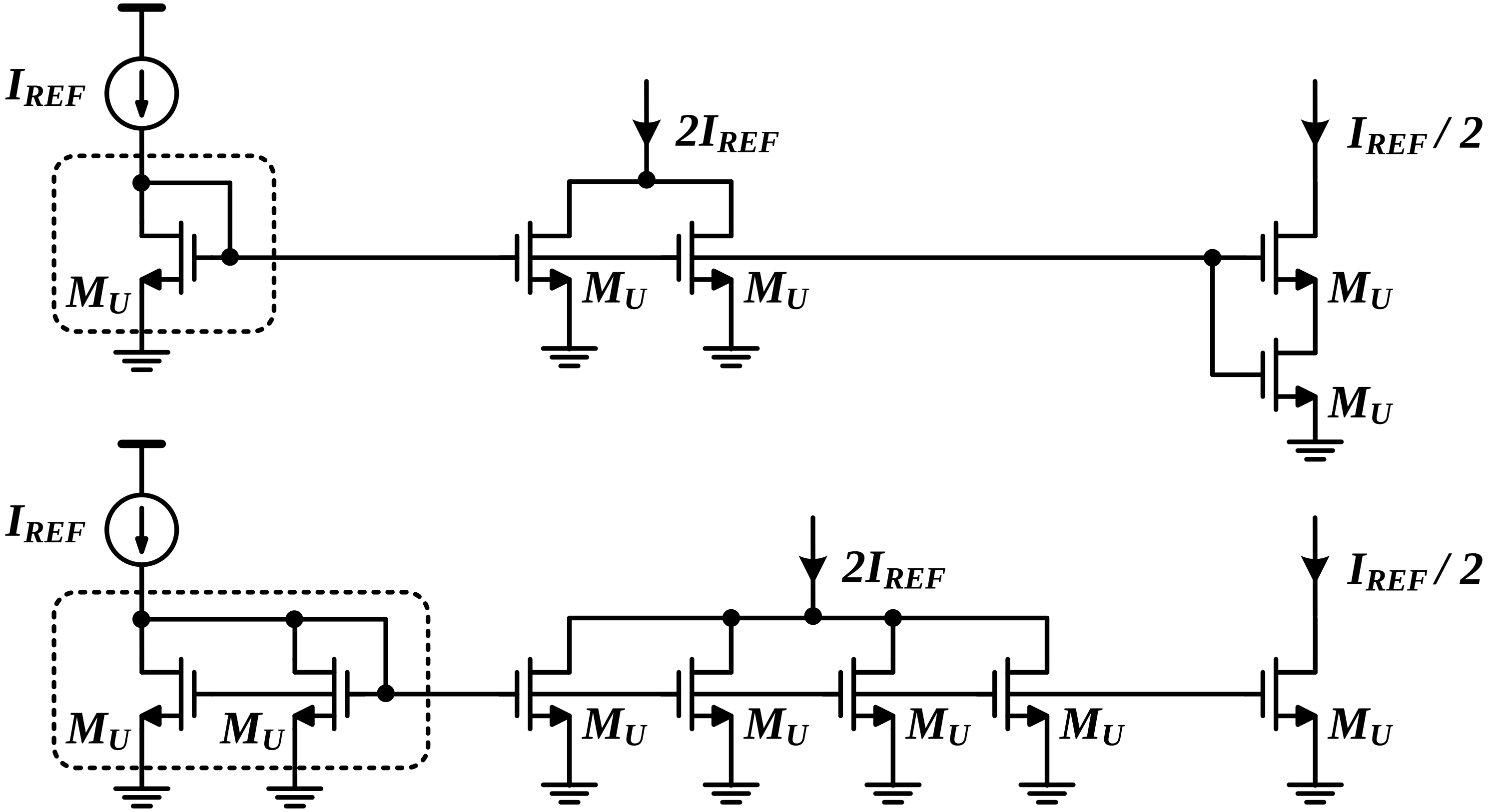
Sink and Source Currents

- Use PMOS mirror to source current (from VDD)
- Use NMOS mirror to sink current (to GND)



Scale Current Up and Down

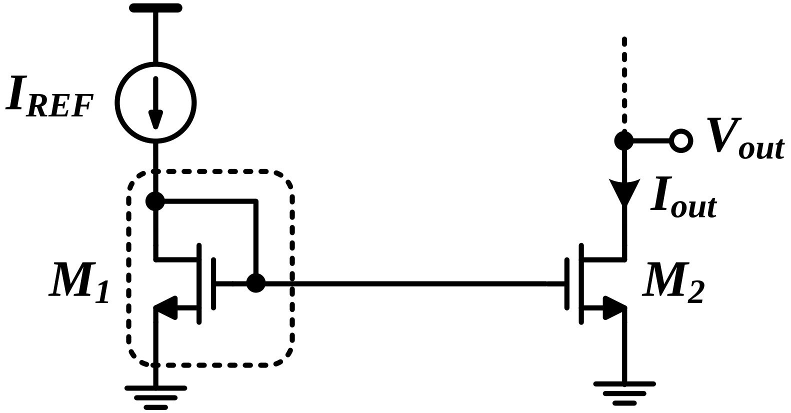
- Currents can be scaled up or down by connecting unit transistors in parallel (accurate) or series (not as accurate: why?)
- ALWAYS use matched unit transistors (same L, W, orientation, etc.)



V_{DS} Dependence

- Dependence of I_D on V_{DS} introduces two types of errors
  1. M2 has finite $R_{out} = \frac{\Delta V_{out}}{\Delta I_{out}}$ → If V_{out} varies, I_{out} will vary
  2. Even if V_{out} does not vary: $V_{DS1} \neq V_{DS2}$
- We usually scale W (unit transistors) and keep L equal: $\lambda_1 \approx \lambda_2$

$$\frac{I_{out}}{I_{REF}} = \frac{\frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_2 (V_B - V_{TH})^2(1+\lambda_2 V_{DS2})}{\frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_B - V_{TH})^2(1+\lambda_1 V_{DS1})} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}\frac{(1+\lambda_2 V_{DS2})}{(1+\lambda_1 V_{DS1})}$$



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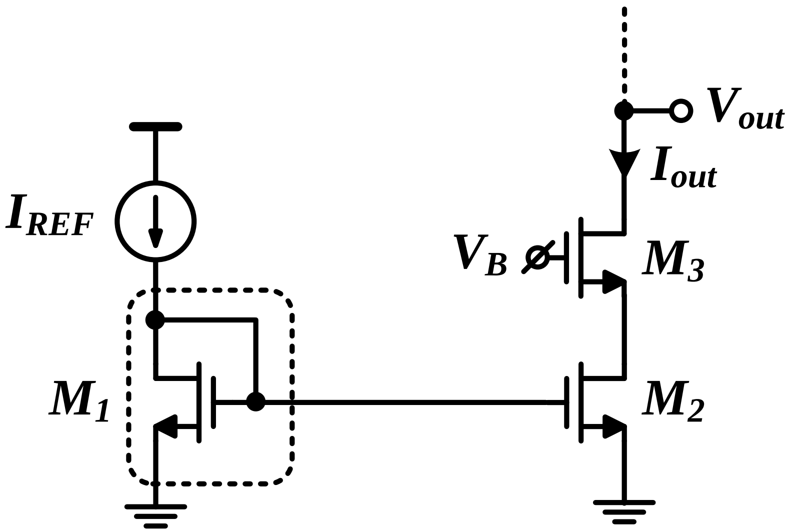
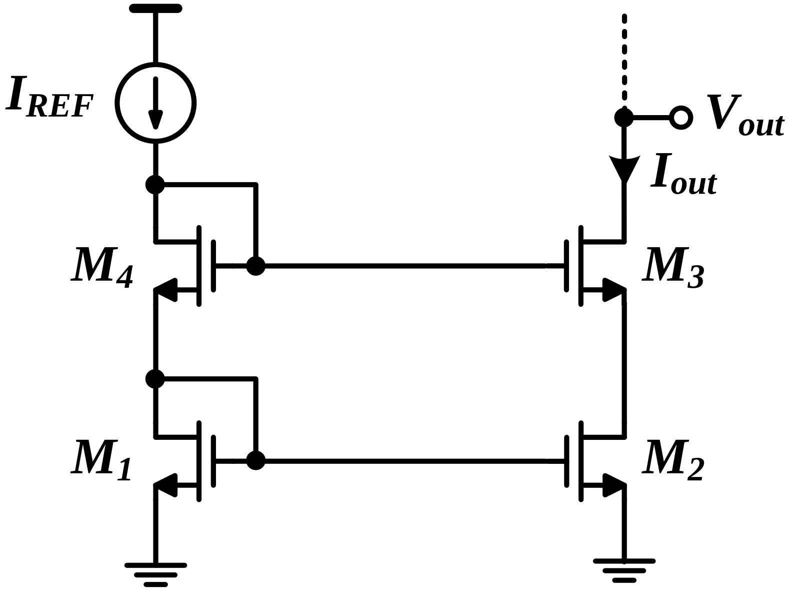
Cascode Current Mirror (1)

- R_{out} can be boosted by using cascode
  - Reduced $\Delta I_{out} = \frac{\Delta V_{out}}{R_{out}}$ for a given ΔV_{out}
- But still $V_{DS1} \neq V_{DS2}$ → still have static error in the mirroring ratio
  - Set $V_B = V_{GS3} + V_{GS1}$ → $V_{DS2} = V_{DS1} = V_{GS1}$
- How to generate V_B?



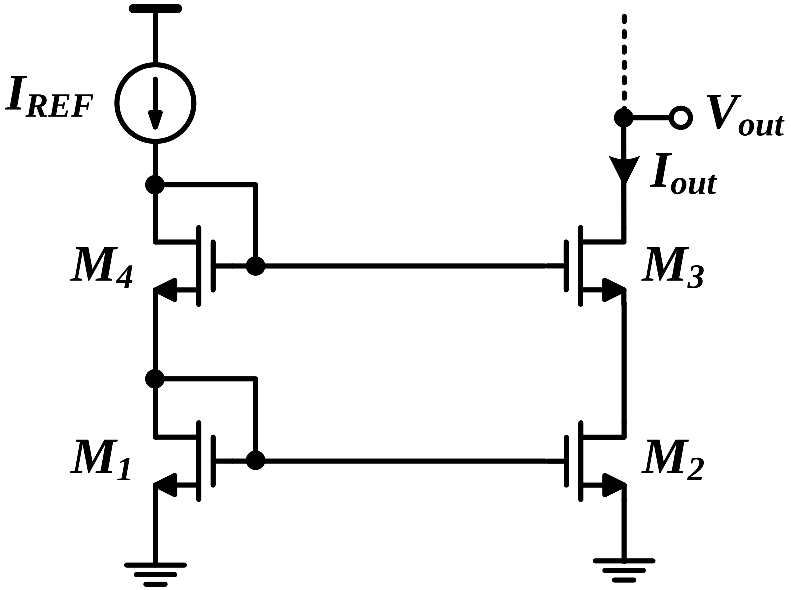
Cascode Current Mirror (2)

- M3 and M4 have the same V_{GS}.
  - Thus M1 and M2 will have the same V_{DS}.
- Note that the mirroring action is performed by M1 and M2 only.
  - The role of M3 and M4 is to guarantee $V_{DS1} = V_{DS2}$.
- If both V_{GS} and V_{DS} are equal, current will be perfectly mirrored.
  - Actually even if the transistors are not in saturation!



Quiz

- Compliance range: V_{out} range where the CS behaves as a CS
- Assume $V_{TH1,2} = 0.4V$, $V_{TH3,4} = 0.45V$ (body effect), $V_{ov} = 0.1V$.
- Calculate the CS compliance range.



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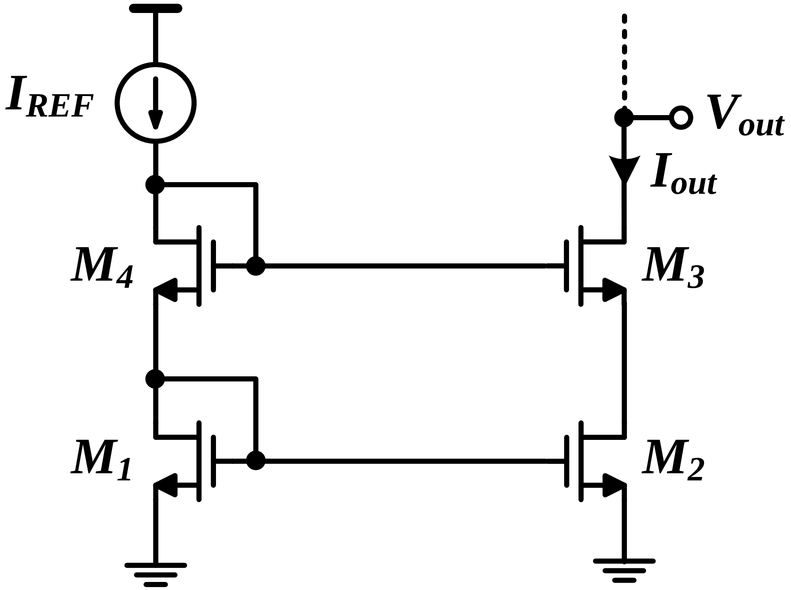
Cascode CM Wastes Headroom

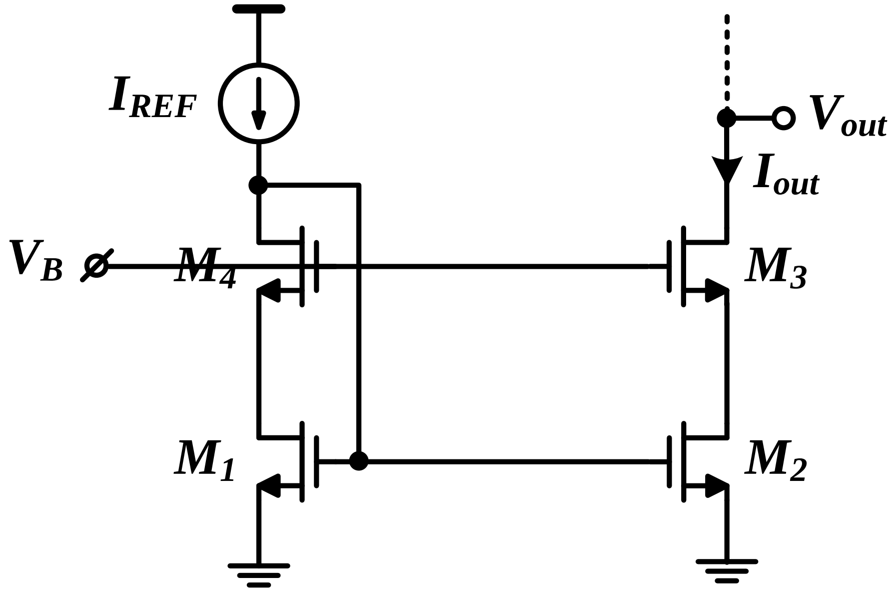
- We forced $V_{DS2} = V_{DS1} = V_{GS1} = V_{TH} + V_{ov1}$
- But to remain in saturation we only need $V_{DS2} > V_{ov1}$
- V_{DS2} has an extra unneeded V_{TH} → waste of headroom
- Solution: Do not set $V_{DS2} = V_{DS1}$
  - Instead, force $V_{DS1} = V_{DS2,min} = V_{ov1}$ → wide-swing CM



Wide-swing Cascode CM

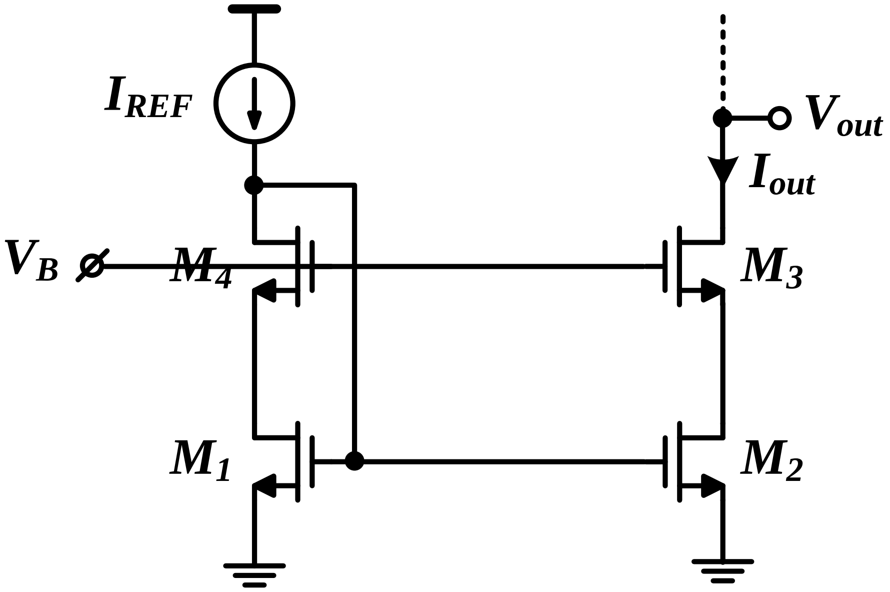
$$V_{TH3,4} + V_{ov3,4} + V_{ov1,2} < \boldsymbol{V_B} < V_{TH3,4} + V_{TH1,2} + V_{ov1,2}$$

- As long as V_B is in the valid range, M1-4 will be in sat.
- The most widely used CM architecture
- A.k.a. low-voltage current mirror, low-compliance current mirror



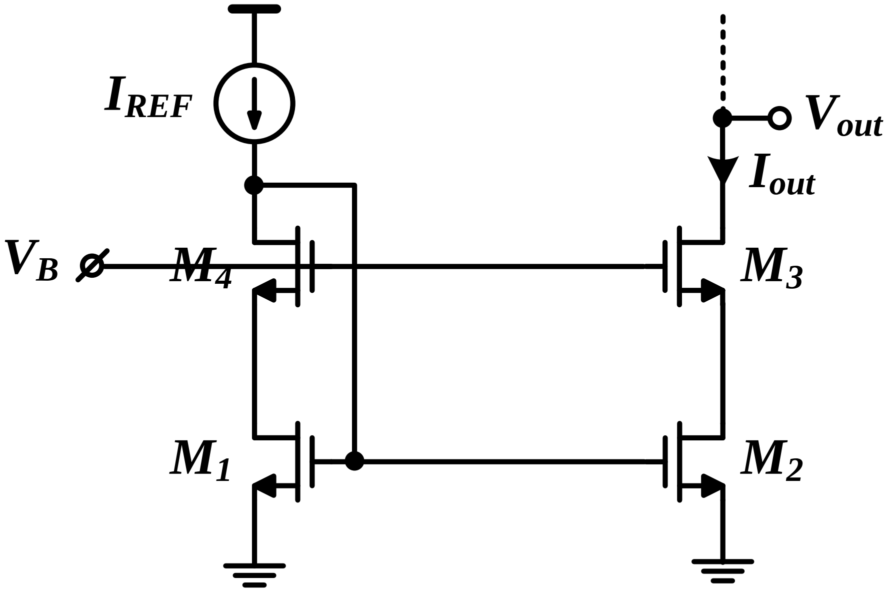
Quiz

- Compliance range: V_{out} range where the CS behaves as a CS.
- Assume $V_{TH1,2} = 0.4V$, $V_{TH3,4} = 0.45V$ (body effect), $V_{ov} = 0.1V$.
- Assume V_B is set $50mV$ above its minimum value.
- Calculate the CS compliance range.



Quiz

- Compliance range: V_{out} range where the CS behaves as a CS.
- Assume $V_{TH1,2} = 0.4V$, $V_{TH3,4} = 0.45V$ (body effect), $V_{ov} = 0.1V$.
- Assume V_B is set $50mV$ above its minimum value.
- Calculate the CS compliance range.
- Practically, we don't bias M1-2 at the edge of saturation (why?).
- What is the magic battery that will generate V_B?

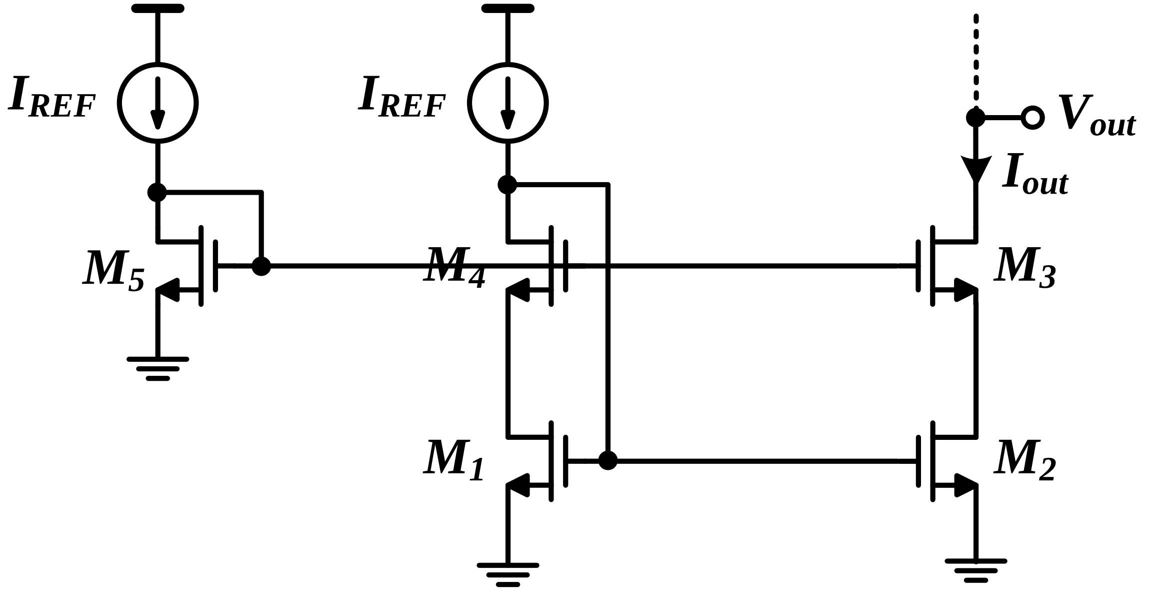


The Magic Battery

- To generate voltages we use I-to-V: diode connected transistor
- Assume M1-M4 have the same W/L: $V_B > V_{TH3,4} + 2V_{ov1-4}$

$$V_{ov5} > 2V_{ov1-4} \rightarrow L_5 > 4L_{1-4}$$

- Always select $V_B > V_{B,min}$ (e.g., $L_5 \sim 6L_{1-4}$)
  - Need to drive M1 and M2 a bit deeper into saturation
  - Account for body effect of M3 and M4



M5 is usually implemented as unit transistors in series

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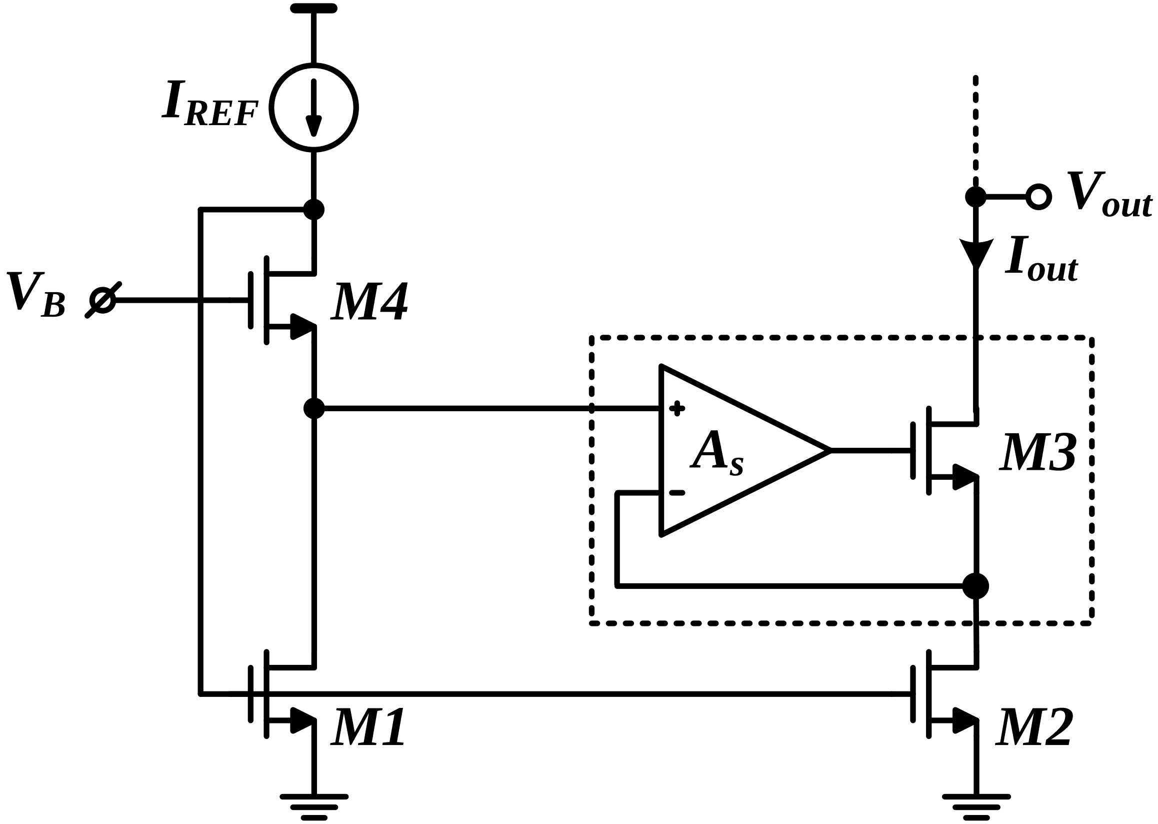
Regulated (Super) Cascode CM

- Feedback keeps $V_{DS1} \approx V_{DS2}$ and boosts R_{out}

$$R_{out} \approx r_{o,super}\left(1 + g_{m,super}R_S\right) = r_{o3}(A_s g_{m3} r_{o2}) \sim A_s(g_m r_o^2)$$

- Since both V_{GS} and V_{DS} are equal, the mirror works even if M1 and M2 are not in saturation!



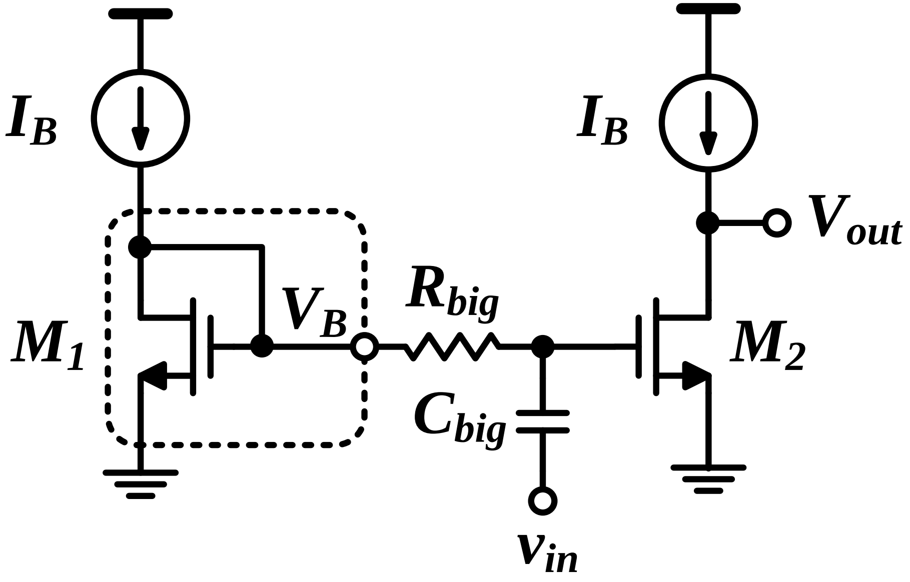
Thank you!

References

- B. Razavi, “Design Of Analog CMOS Integrated Circuit,” McGraw-Hill, 2nd ed., 2017
- T. C. Carusone, D. Johns, and K. W. Martin. “Analog Integrated Circuit Design,” Wiley, 2nd ed., 2012
- R. J. Baker, “CMOS circuit design,” 3rd ed., Wiley, 2010

Replica Biasing

- ❑ To bias the CS amplifier (M2) a replica (M1) is used
- ❑ R_{big} and C_{big} will take a lot of area
  - Only practical for RF circuits (why?)
- ❑ For analog ICs a better trick is used
  - More when we study differential amplifier



Advanced Current Mirrors

- Can operate with 50mV compliance!
  - Amplifier gain compensate for low Rout in triode