Lab 2

MOSFET Sizing and CS Amplifier

(Xschem, NGSpice & ADT)

Part 1: Sizing Chart

Required Spec:

DC Gain	-10
Supply	2.5v
Current Consumption	10uA

Analytic Calculations:

$$|A_v| \approx gmR_D = \frac{2I_D}{V_{ov}} = \frac{2V_{RD}}{V_{ov}}$$

$$In\ Simulation\ V_{ov} \neq \frac{2I_D}{gm}\ all\ the\ time, \qquad Instead\ use\ V^* = \frac{2I_D}{gm}$$

$$|A_v| = \frac{2V_{RD}}{V^*}$$

To get Large Output Swing: Assume $\text{CM output} = V_{RD} = 1V$

$$R = \frac{V_{RD}}{I_D} = \frac{1}{10\mu} = 100K\Omega \qquad (first\ design\ parameter\ calculated)$$

$$V_Q^* = \frac{2V_{RD}}{|A_v|} = 2 * \frac{1}{10} = 0.2\ V$$

This concludes the initial Gain Calculation, We will use the obtained results on a ADT to get the remaining design parameters required to meet the Spec.

On ADT we assumed a relatively Length of 2um such that we are not affected by short channel effects, and get a high output resistance from the mosfet

V* and Vov Overlaid vs VGS:

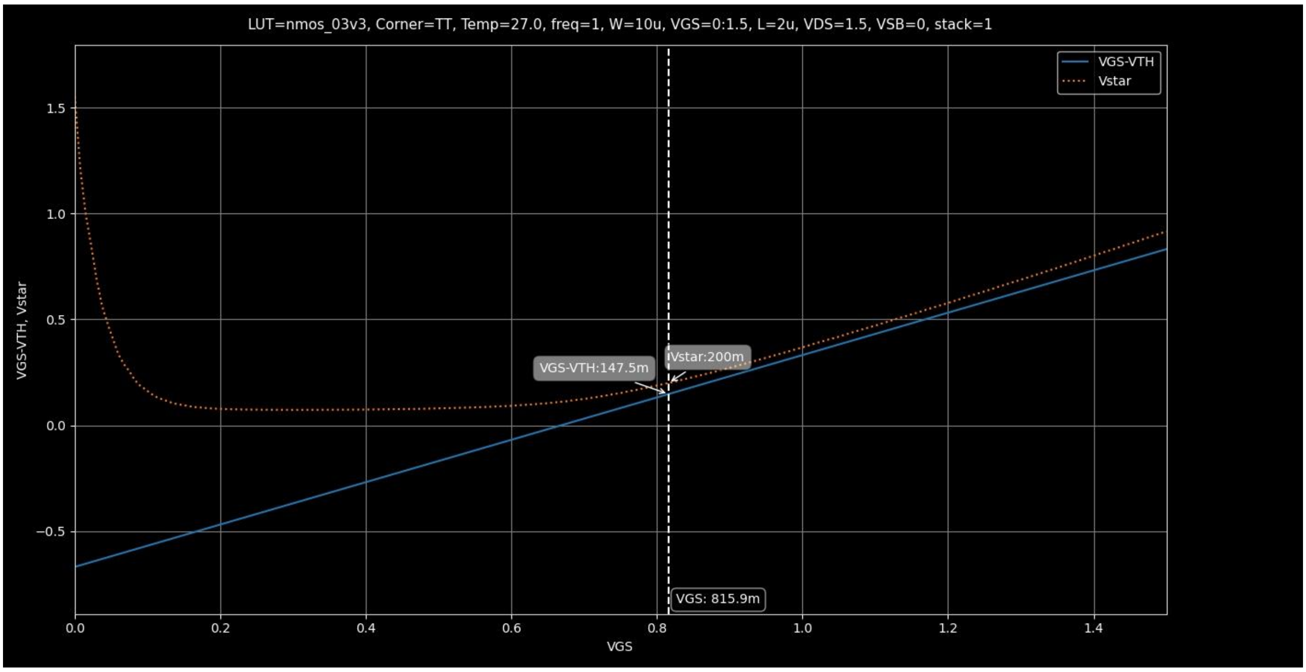

Figure 1 V and Vov vs VGS (ADT)*

Comment: Vov and V* are relatively close in value to each other at the beginning of the Strong Inversion region meaning the square law is relatively valid in that region. But for Deep Strong inversion (Large Vov) or weak inversion, the behavior is quite far despite using a Long Channel Length.

Locating V^*_Q and V_{GSQ}, V_{ovq}:

$$@V_Q^* = 200mV, \quad V_{ovQ} = 147.5mV, \qquad V_{GSQ} = 815.9mV$$

Plotting ID, gm, gds vs V_{GS}:

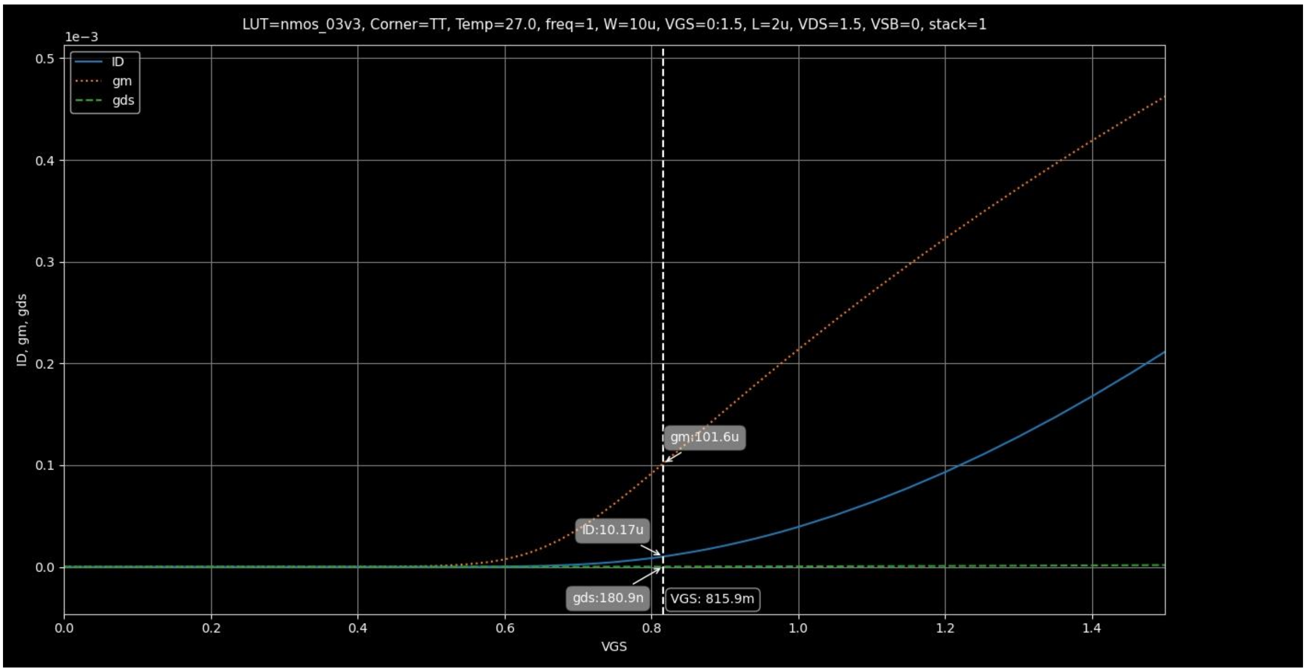

Figure 2 ID, gm, gds vs VGS and their corresponding values at VgsQ

IDx	10.17uA
gmx	101.6uS
gdsx	180.9nS

Getting the Value of W, ID_Q, g_{mQ}, g_{dsQ}:

We can get the required values for the design using cross multiplication since W and I are directly proportional to each other

W	ID
$\mathbf{10\mu m}$	I_{DX} $@VQ*$ (from the chart)
?	I_{DQ} = $10\mu A$ (from the specs)

But the easier approach would be to calculate them directly on ADT.

Figure 3 Calculated Parameters from ADT

Verifying Gain:

$$A_v = -gm(R_D//ro) = -99.17\mu * \frac{100K * 5.66M}{100K + 5.66M} = -9.74 \approx -10$$

The parameters are correct!

Final Parameter List:

W	9.76 um
L	2 um
gm	99.17 uS
gds	176.7 nS
ro	5.66 MΩ
R_D	100 KΩ
Vgs	815.9 mV

Part 2: CS Amplifier

What

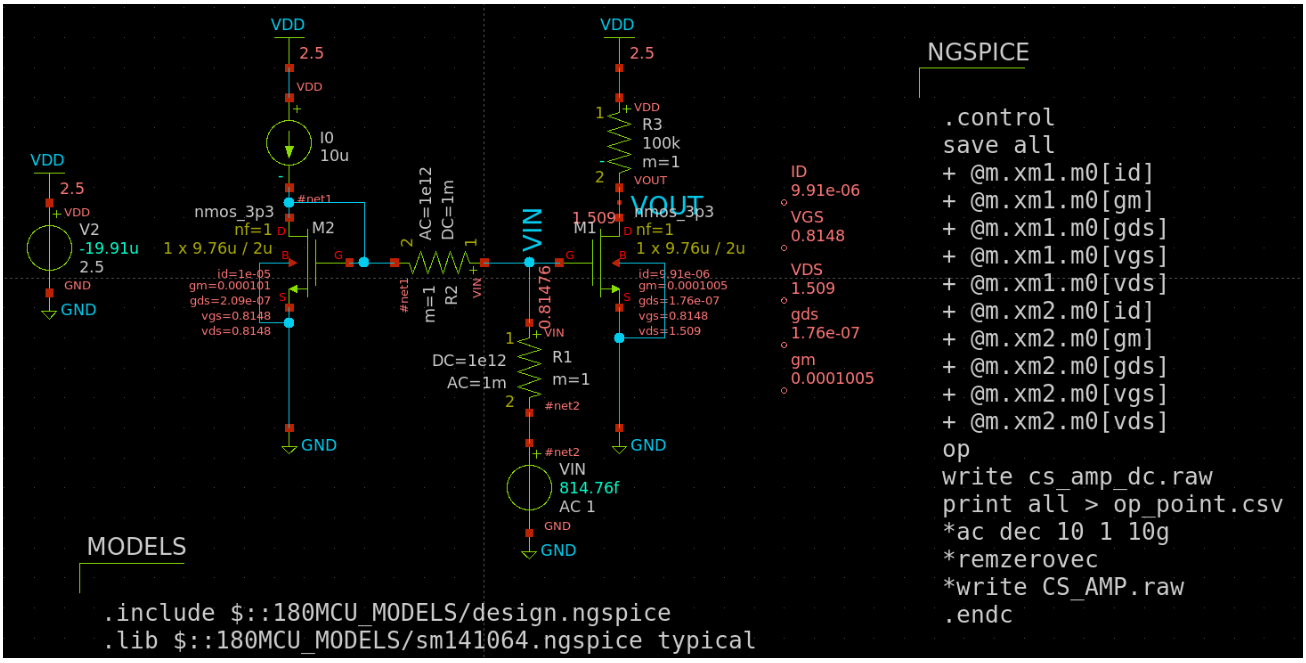

Figure 4 Testbench showcasing OP Points using all Required Methods

Comparing Analytic and Simulation Results for OP Point:

Parameter	Simulation	Analytic
Vgs	814.8 mV	815.9 mV
Id	9.91 uA	10 uA
gm	100.5 uS	99.17 uS
gds	176 nS	176.7 nS
ro	5.68 MΩ	5.66 MΩ

The results are almost identical due to using a chart-based approach.

Compare ro and R_D. Is the assumption of ignoring ro justified in this case? Do you expect the error to remain the same if we use min L?

$$R_D = 100\ K\Omega \quad , \quad ro \approx 5.68\ M\Omega \quad , \qquad ro \gg R_D$$

Therefore, It is safe to neglect ro in this case.

In case of using min L, Since ro and L are directly proportional, ro will massively decrease by decreasing L to a point where it is no longer valid to neglect it as it will have a value comparable with Rd.

- **Calculate the intrinsic gain of the transistor.**

$$Intrinsic\ Gain\ |A_v| = gm * ro = 100.5u * 5.68M = \mathbf{570.84}$$

- **Calculate the amplifier gain analytically. What is the relation (≪, <, ≈, >, ≫) between the amplifier gain and the intrinsic gain?**

$$Amplifier\ Gain\ |A_v| = gm(R_D//ro) = 100.5u * (100K//5.68M) = \mathbf{9.876} \ll \mathbf{547.2}$$

Amplifier Gain is much less than (≪) Intrinsic Gain.

2. AC Analysis:

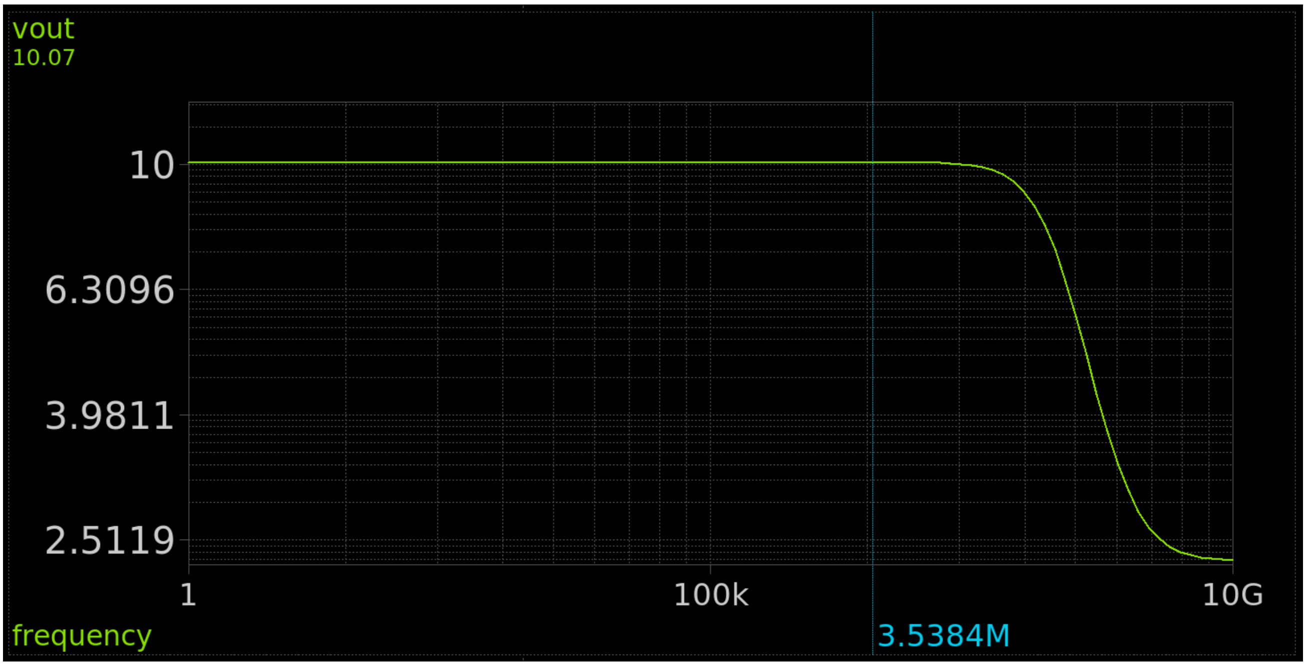

Figure 5 DC Gain from AC Analysis

Gain = 10.07 , Agrees with Analytical Results and approximately equal to the required spec.

3. Gain Non-Linearity:

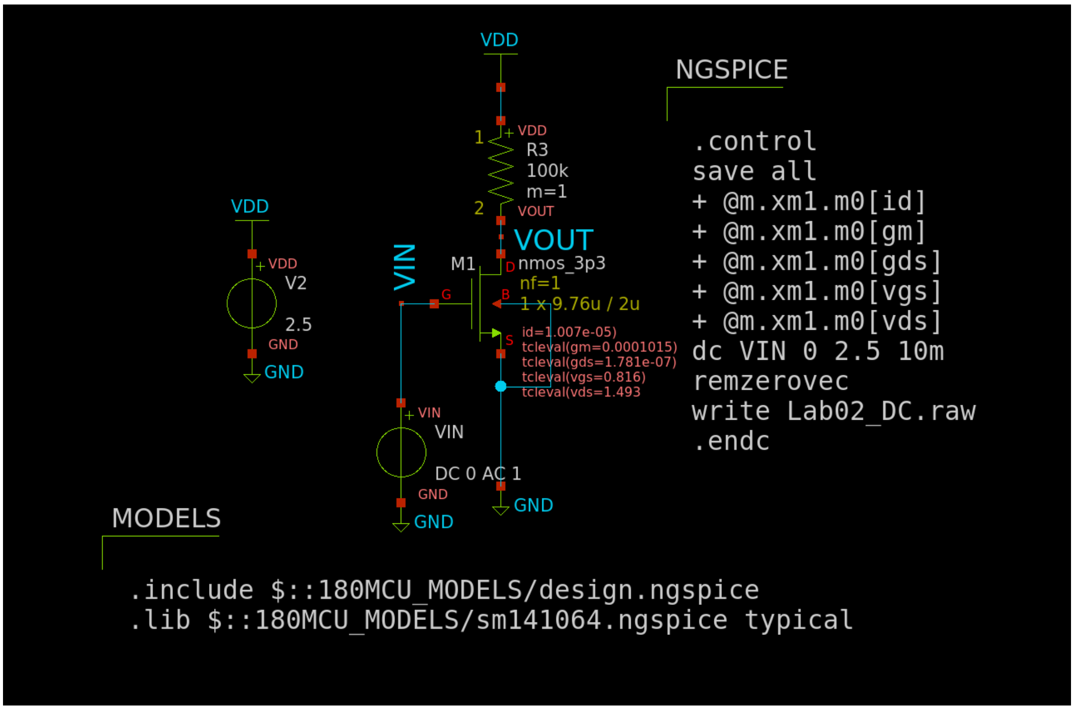

Figure 6 DC Testbench

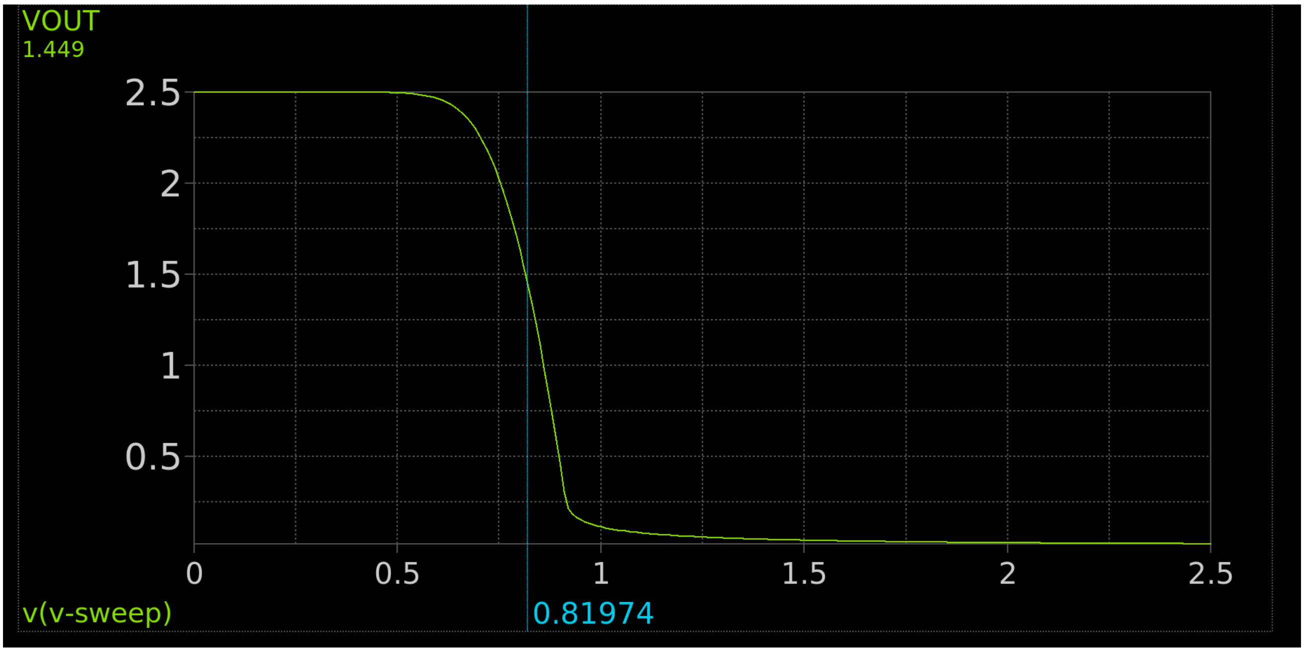

Figure 7 VIN vs VOUT Graph

Comment:

The relation between VIN and VOUT differs according to the region of operation of the transistor:

VOUT is given by VOUT = VDD – ID*RD

@ Vin < Vth: Cutoff region, ID = 0 thus VOUT = VDD

@ Vin > Vth & Vout > Vov: Saturation region, The relation is quadratic according to the Square Law.

Notice: Due to the big slope in that area, if a small signal is applied around the Operational point it could be approximated that the relation is linear in that case. Hence that's the preferred region to operate the amplifier but still the relation is not linear enough to consider the amplifier linear.

@ Vin > Vth & Vout < Vov: Triode Region, The relation is almost linear according to the triode current equation.

Though with a much smaller slope than the one in the saturation region.

Derivative of VOUT vs VIN:

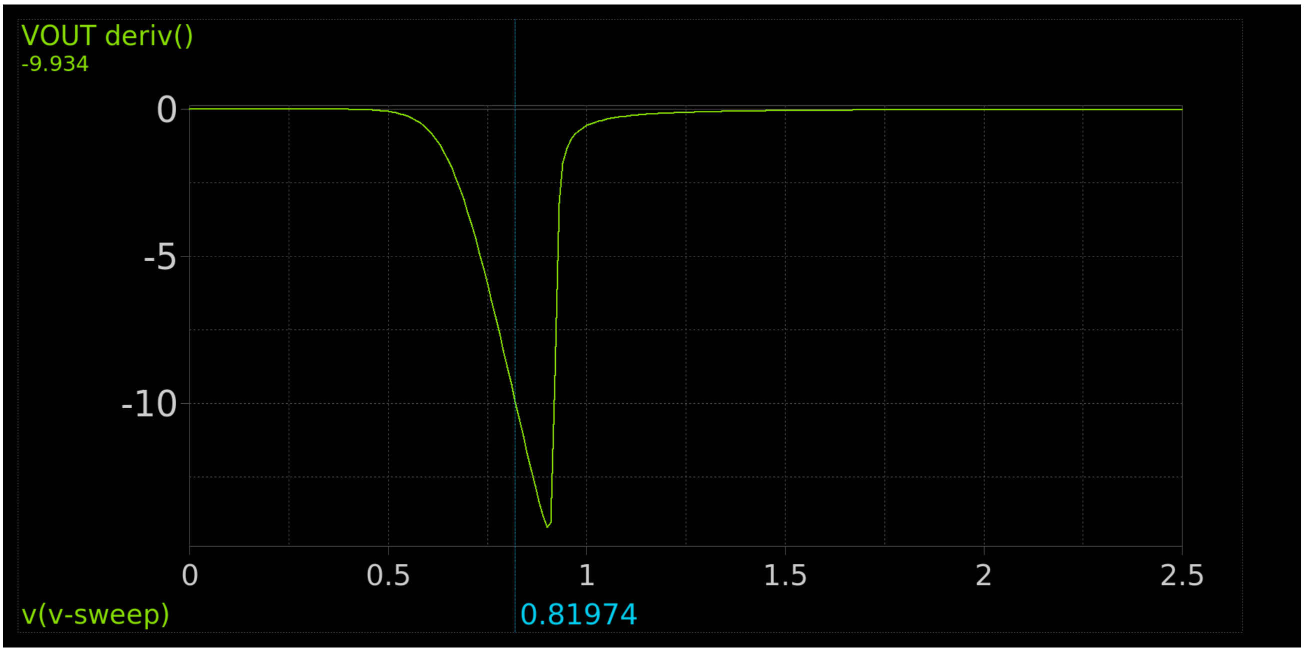

Figure 8 Derivative of VOUT vs VIN graph

Is the Gain Linear?

Since VIN = VGS, gm = 2*ID/Vov = k*Vov depends on VGS and the gain Av = gm*Rd (Depends on gm)

The Gain is the function of the input and as seen from the graph it is not linear. Though if zoomed in for a small signal it can be approximated to be linear in that case.

4. Transient Analysis:

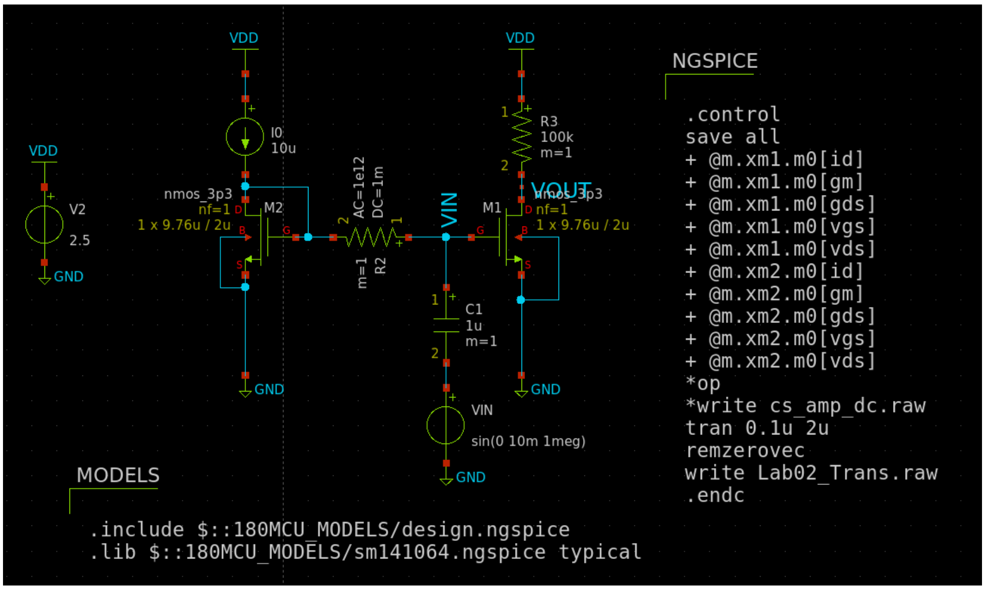

Figure 9 Transient Simulation Testbench

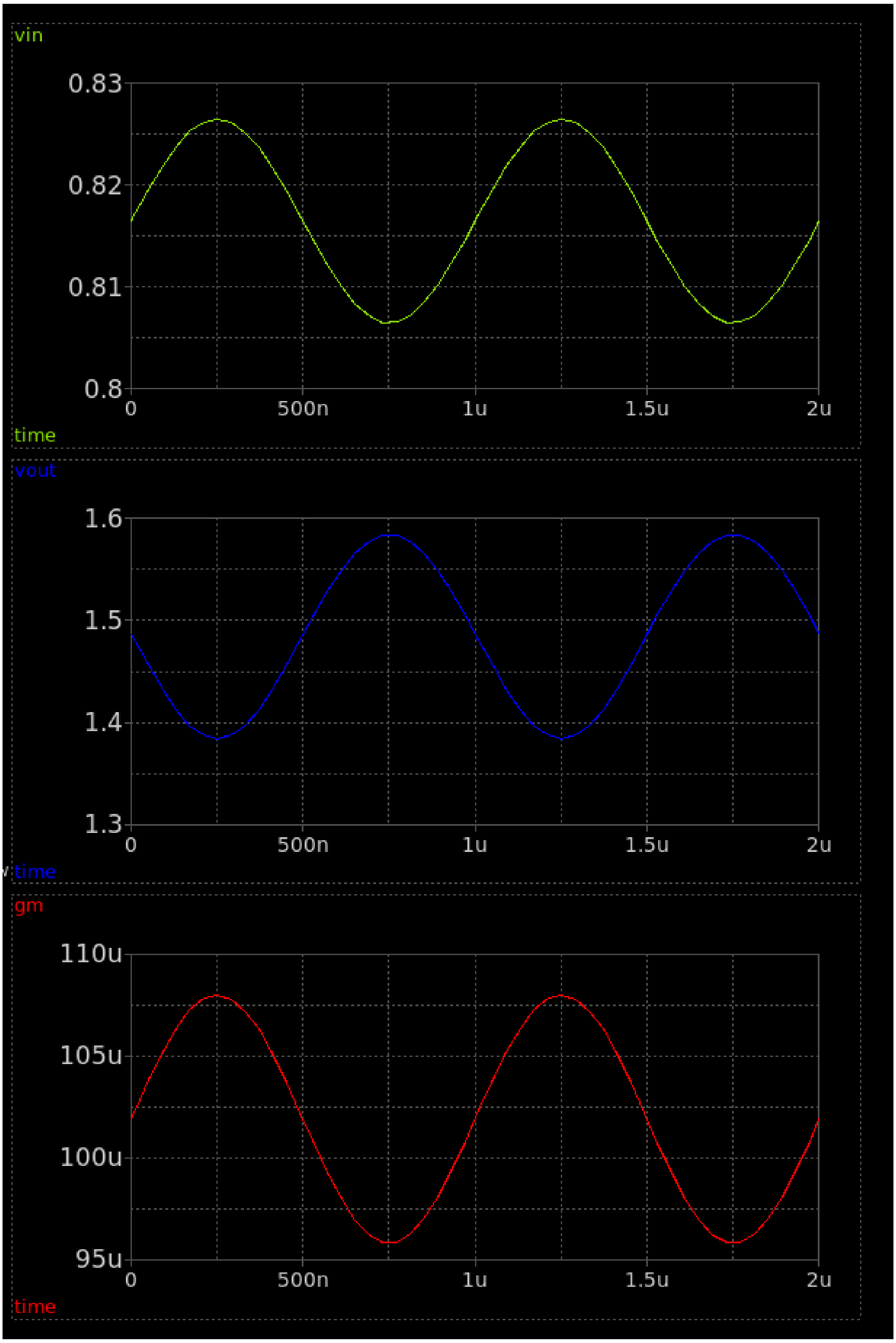

Figure 10 VIN (Green), VOUT (Blue) and gm (Red) vs Time

Does gm vary with the input signal? What does that mean?

gm does vary across time as it is a function of the input. Which means the gain also varies with the input signal

Is this amplifier linear? Comment.

No , The amplifier is not Linear.

While some linear behavior can be noticed on very small signals, those are merely approximations and do not show the entire picture. Vout varies with Vin which affects different parameters and makes the gain non-linear as well.

5. Gain Linearity (Negative Feedback):

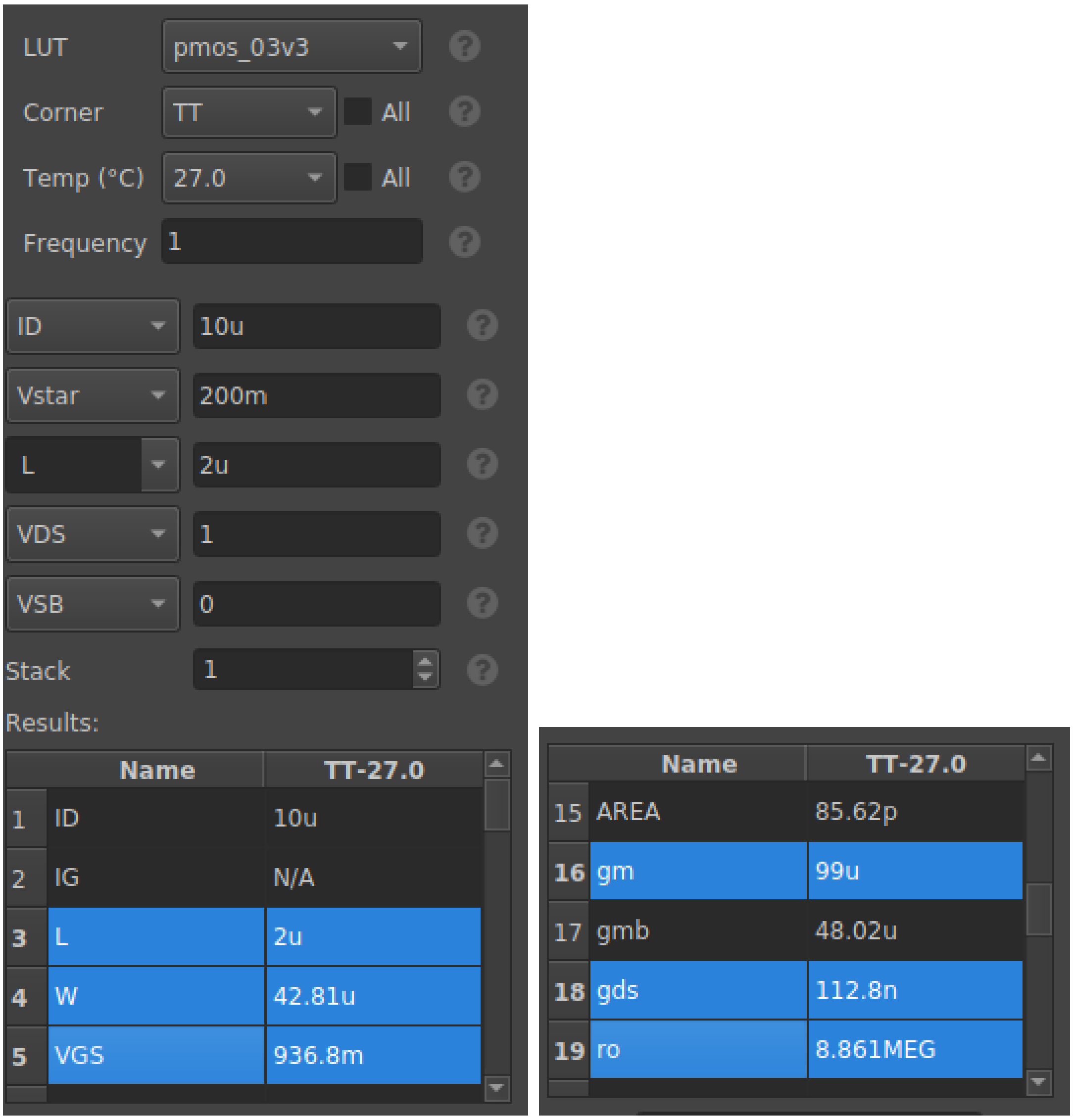

Figure 11 PMOS Sizing using ADT

$$L = 2\mu m \, , W = 42.81\mu m$$

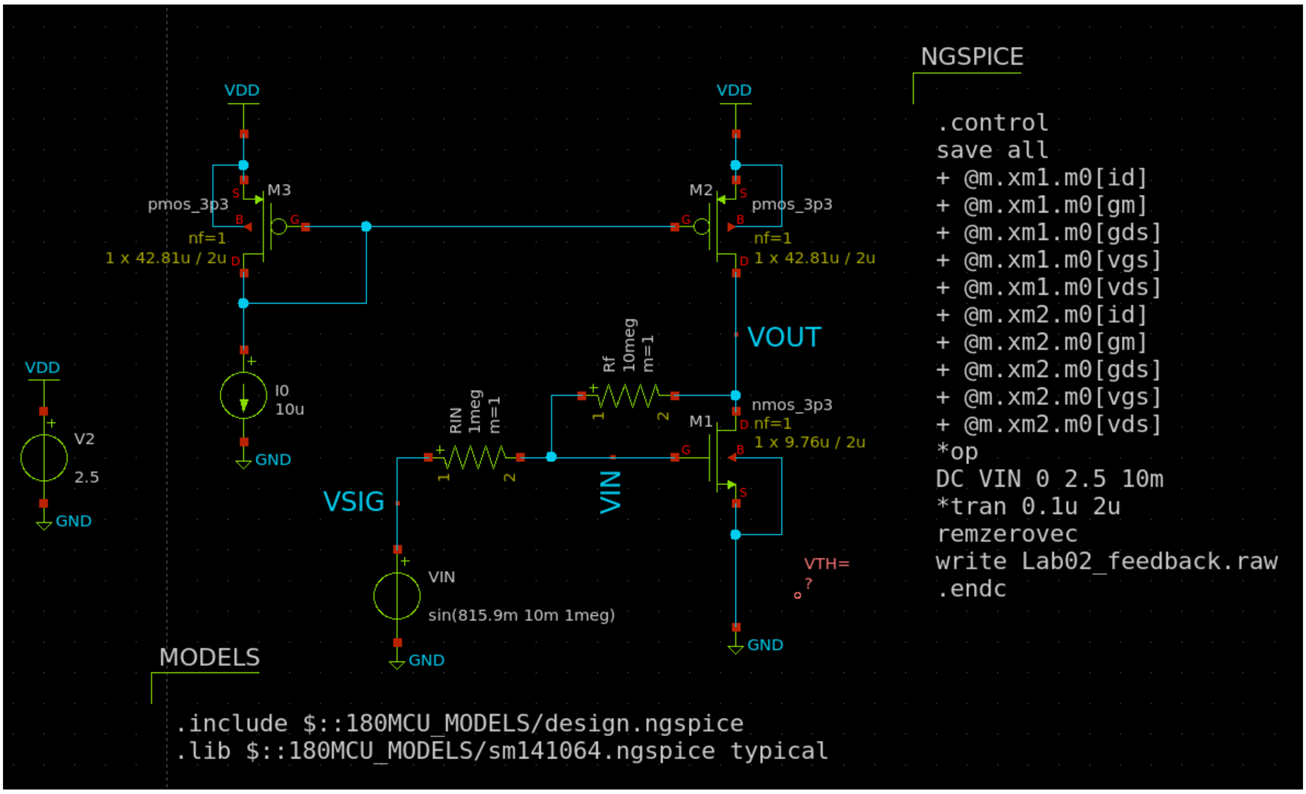

Figure 12 Negative Feedback Testbench

Chossing Rsig=1MΩ as the gain is equal to Rf/Rsig thus choosing the appropriate Rsig to make the gain equal to -10 as required from the spec.

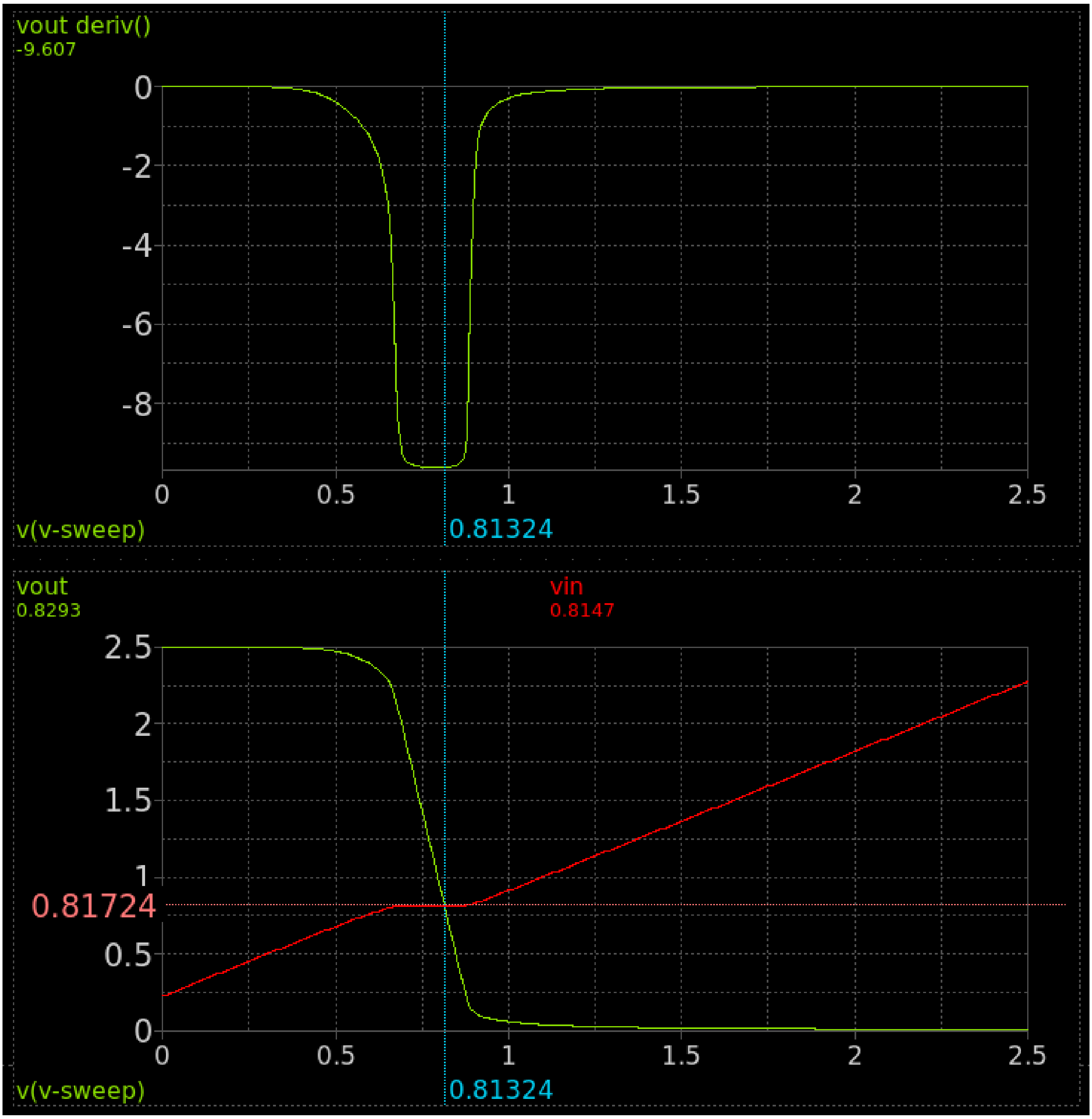

Figure 13 Gain, VIN and VOUT vs VSIG

Report VIN and VOUT vs VSIG (overlaid). At what voltage do the two curves cross? Why?

The two curves cross paths at approximately VGS of the Q-Point of the transistor, where VIN equals VOUT the transistor is considered to be diode connected. This is where the current produced by the NMOS and PMOS is equal each other.

Is VOUT vs VSIG linear in the operating range of the amplifier? Why?

It is Linear, Due to the effect of negative feedback as it desensitizes the gain from the transistor parameters and makes it dependent only on the Rf resistor and the Rsig only

The negative feedback senses a change in voltage at the output node and return it to the input node by subtracting it thus returning the Gain to its original value and this cycle continue in the operating range sustaining a linear relation.

Report the derivative of VOUT vs VSIG. The derivative is itself the small signal gain. Is the gain linear (independent of the input) in the operating range of the amplifier? Why?

As the transitor reaches its operating range. We can see a flat gain curve at approximately -10 which is the required gain from the circuit. The flat curve indicates the gain is linear and is inpdendent of the input. Due to the negative feedback as mentioned previously

VIN is almost constant in the operating range of the amplifier. What is its value? Why?

The Value of VIN is 817.224mV which is approximately equal to the bias VGS Calculated in the previous part, being constant show that the gain is also constant in that are. Due to the negative feedback as explained before.

Analytically calculate the DC input range over which the gain is linear. Compare your analysis with the simulation result.

$$Input\ Range\ \approx \frac{V_{DD} - 2V^*}{|A_v|} = \frac{2.5 - 2 * 0.2}{10} = 0.21V$$

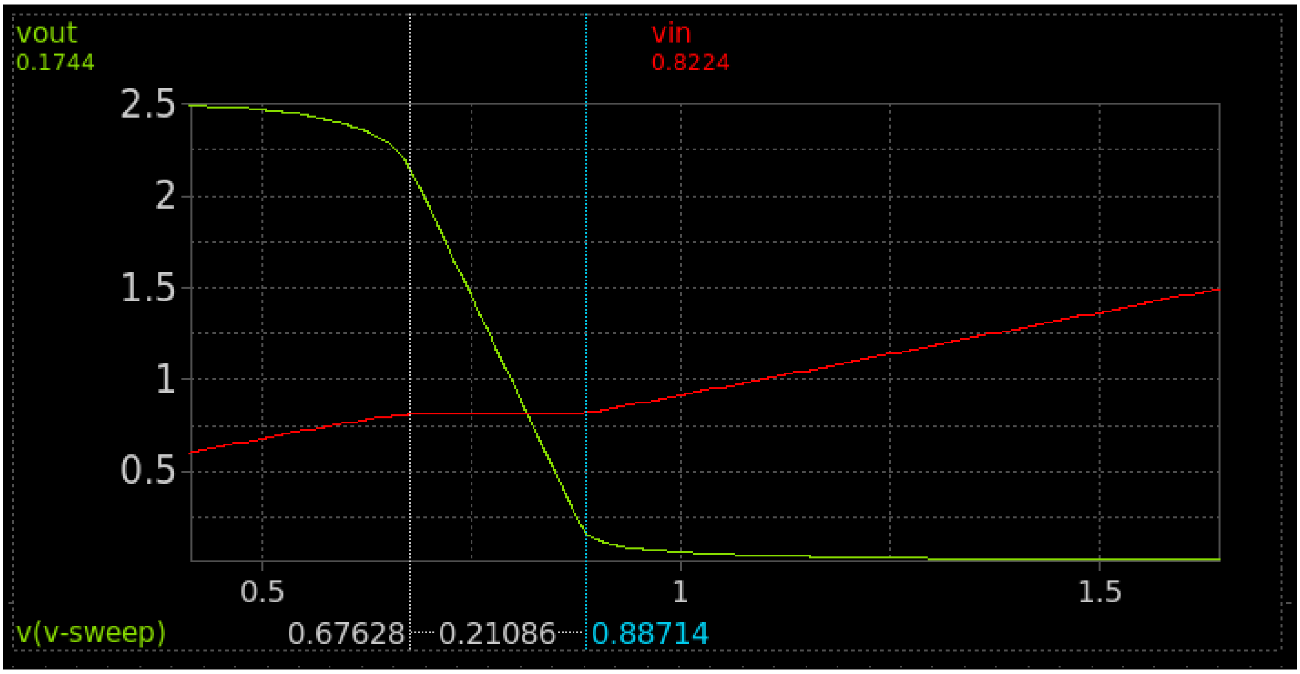

Figure 14 Input Range from Simulation

Simulation results = 0.21086V, Hand Analysis = 0.21V. Approximately equal!

GM vs Time (Transient Analysis)

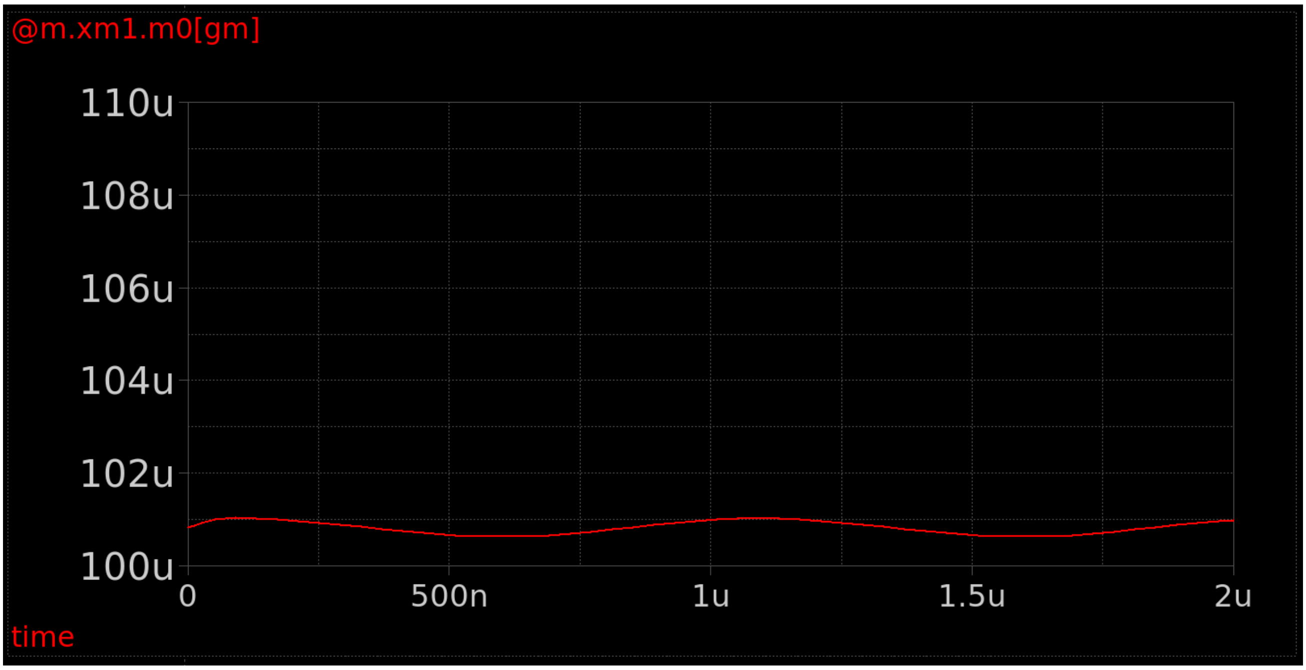

Figure 15 gm vs Time

Compared to figure 10, we can see gm varies at a much smaller range around the 101uS point compared to the bigger variation seen in figure 10, This small variation can be considered approximately Constant in this case.