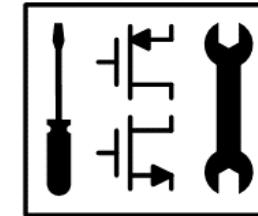


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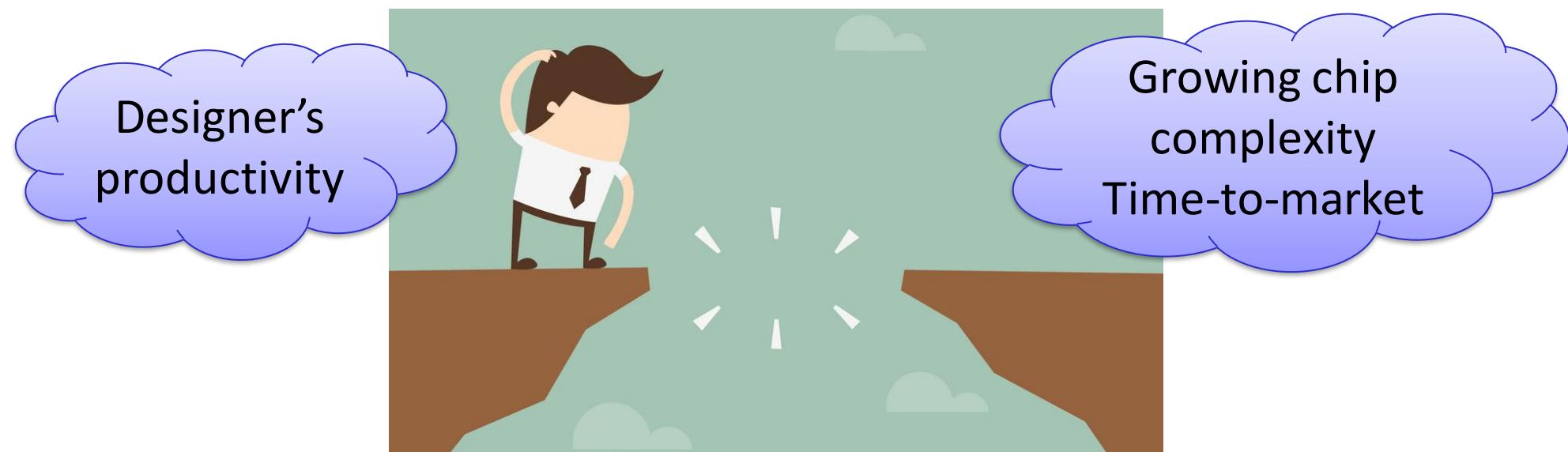
From Designers... To Designers

The gm/ID Design Methodology Demystified

Dr. Hesham A. Omran

The Problem

- Since the release of Berkeley SPICE simulator in the 1970s...
 - No major change in the analog design flow!
- Nanometer transistor models are very complex
 - Time-consuming multi-variable sweeps on simulation tools...
- There is no systematic analog design process!



Outline

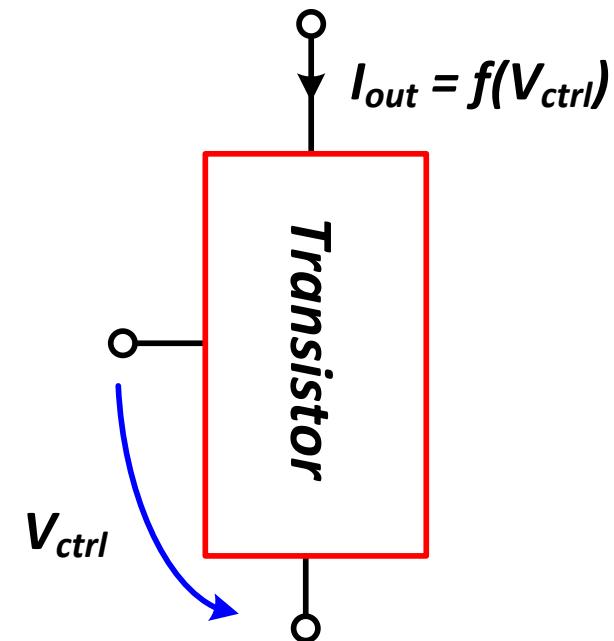
- Why gm/ID?
- The BJT Story
- The MOSFET Story
- The MOSFET Design Problem
- The Look-up Tables (LUTs)
- Design Examples

Outline

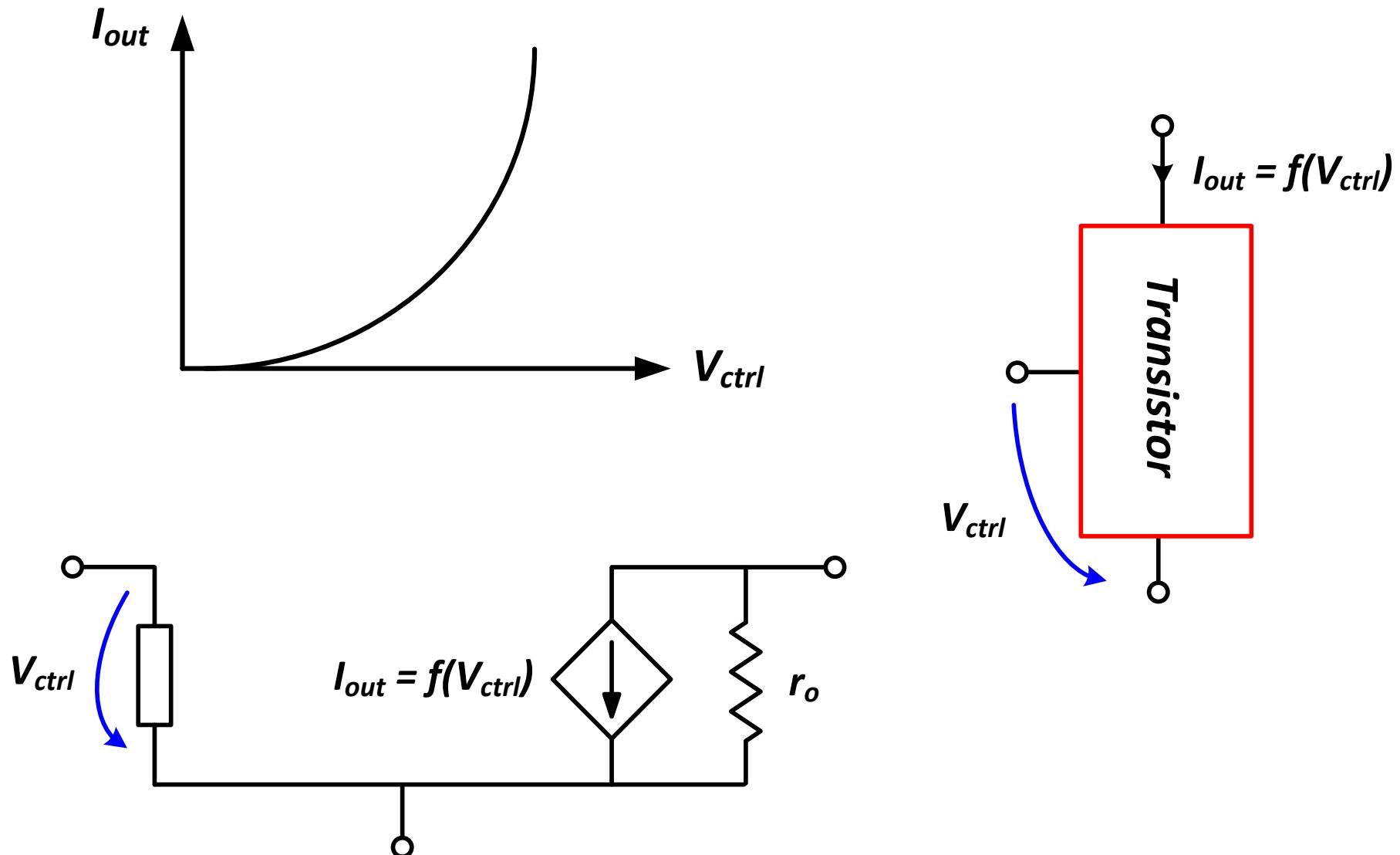
- Why gm/ID?
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- Design Examples

Why is the Transistor Different?

- We are used to two-terminal devices
 - Resistors, capacitors, inductors, diodes
- The transistor is a three-terminal device
 - The voltage between two terminals controls the current flowing into the third terminal
 - V_{ctrl} controls I_{out}
 - Voltage controlled current source (VCCS)
- This feature enabled a multitude of applications that changed our life!
 - Analog signal amplification and processing
 - Digital logic and memory circuits



The Transistor Large Signal Model: Non-linear VCCS

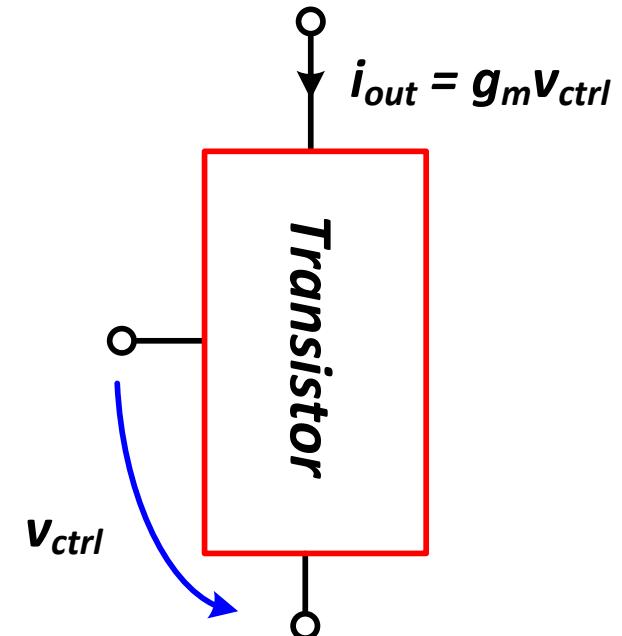
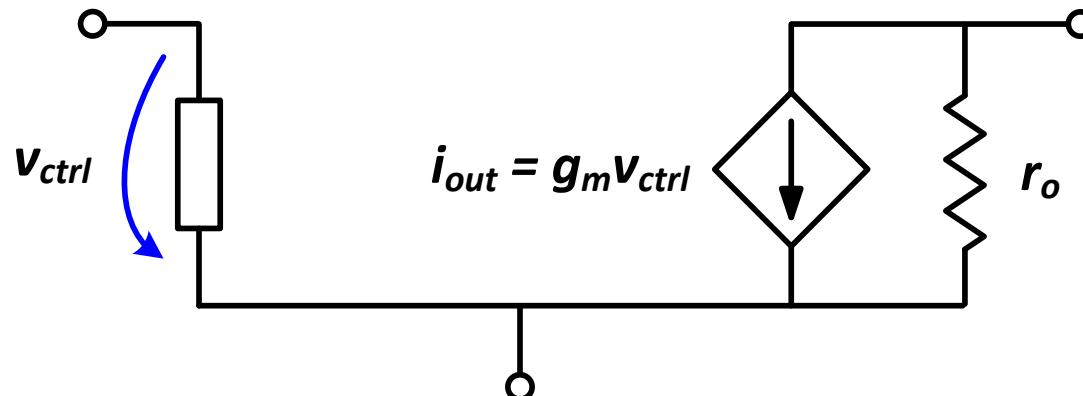
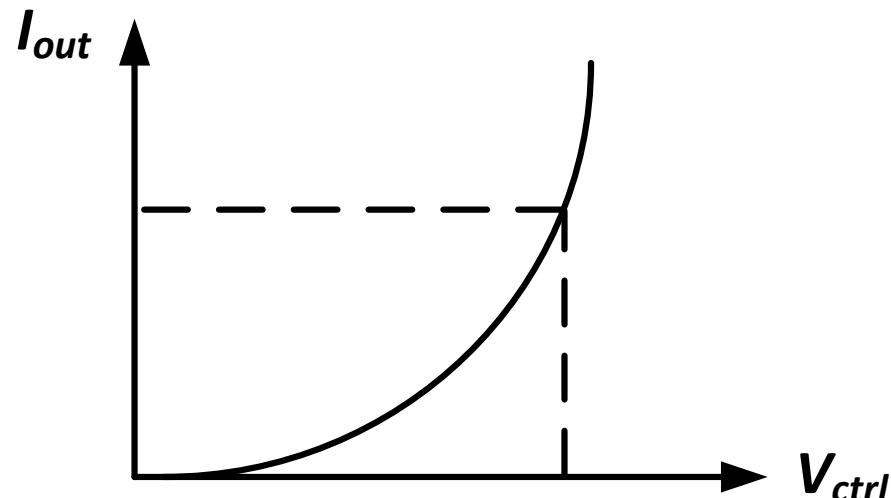


The Small Signal Approximation: Linear VCCS

The Transconductance

$$g_m = \frac{\Delta I_{out}}{\Delta V_{ctrl}}$$

$$= \frac{i_{out}}{v_{ctrl}}$$



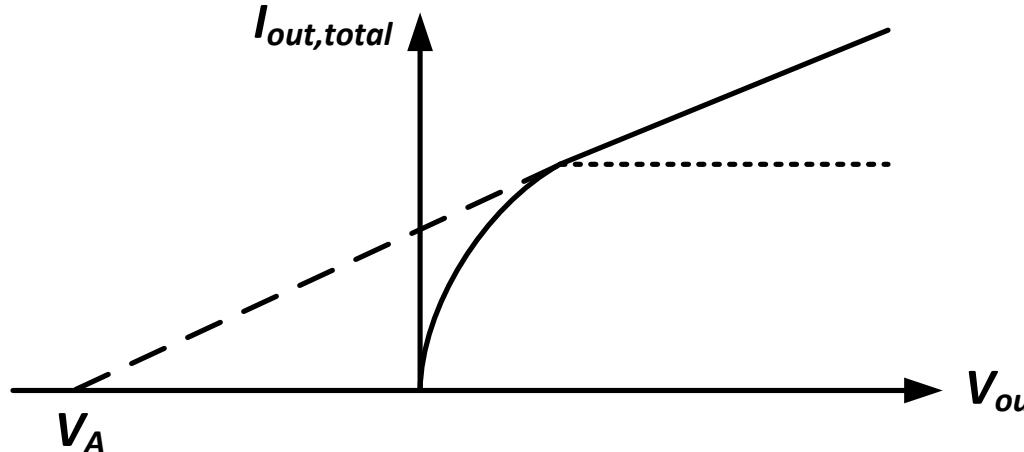
The Output Resistance: Early Voltage (V_A)

The Output Resistance

$$r_o = \frac{1}{g_{out}} = \left(\frac{\Delta I_{out}}{\Delta V_{out}} \right)^{-1}$$

$$\approx \frac{V_A}{I_Q}$$

$I_{out,total}$

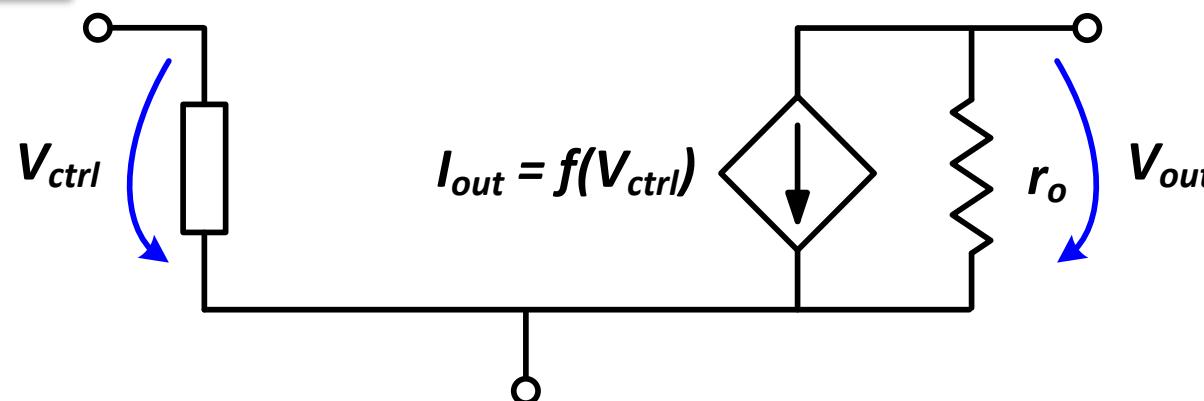


$$I_{out} = f(V_{ctrl})$$

Transistor

V_{ctrl}

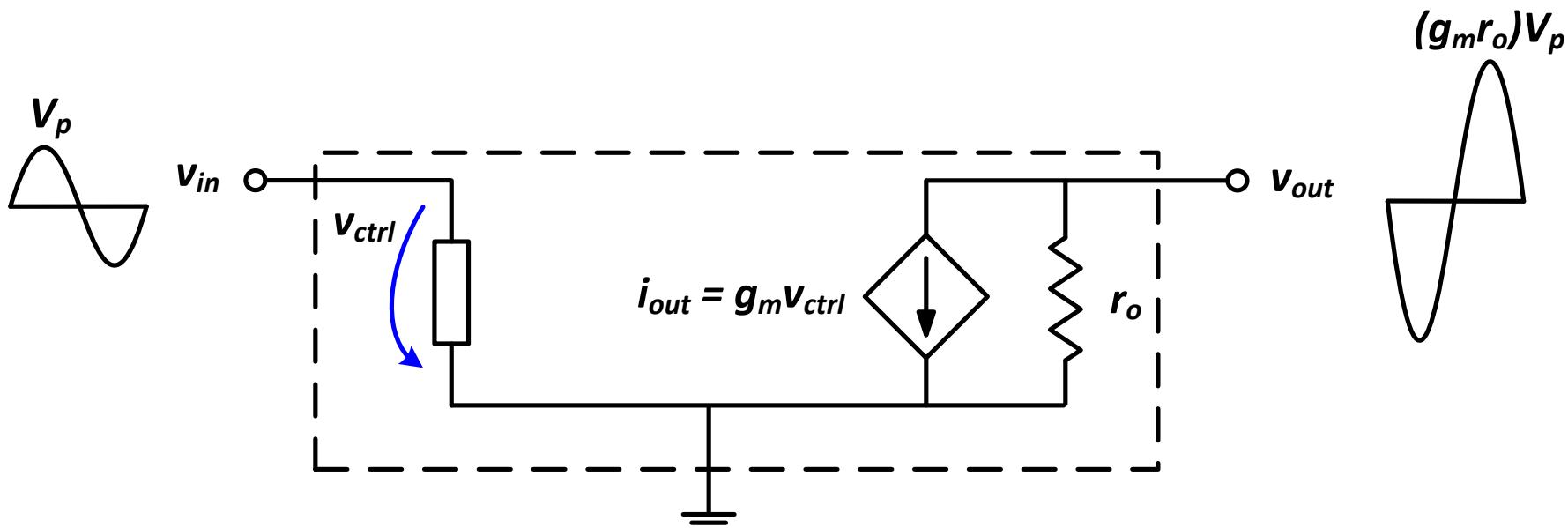
V_{out}



The Transistor Intrinsic Gain

$$v_{out} = -g_m v_{ctrl} \times r_o = -g_m v_{in} \times r_o$$

$$|A_v| = \frac{v_{out}}{v_{in}} = g_m r_o = \frac{g_m}{I_Q} \cdot V_A$$



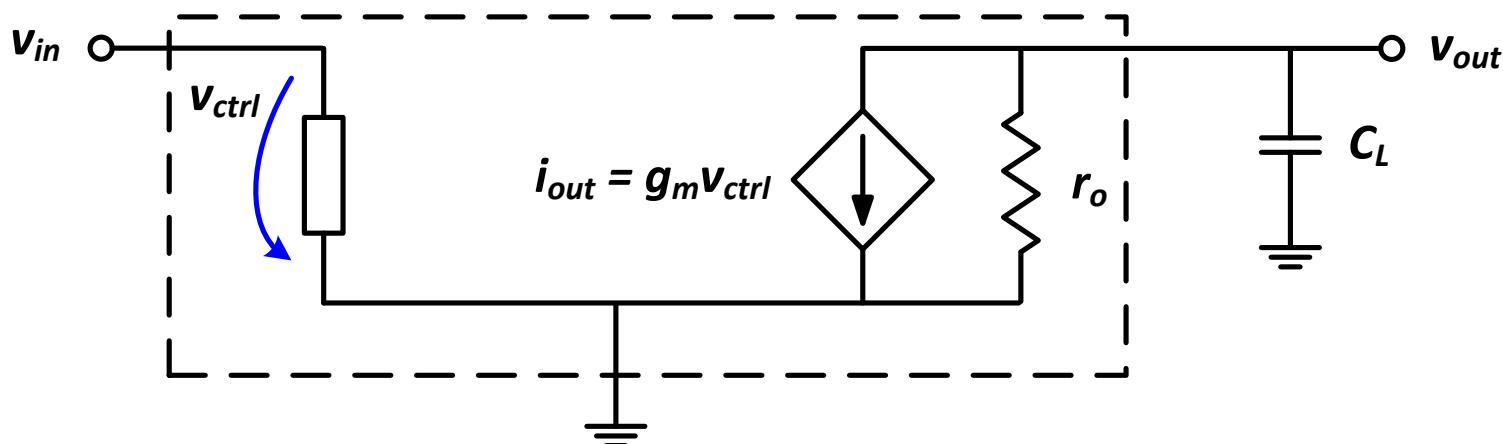
g_m Controls the Speed

$$A_v = \frac{v_{out}}{v_{in}} = g_m r_o$$

$$\tau = r_o C_L$$

$$BW = \frac{\omega_p}{2\pi} = \frac{1}{2\pi\tau} = \frac{1}{2\pi r_o C_L}$$

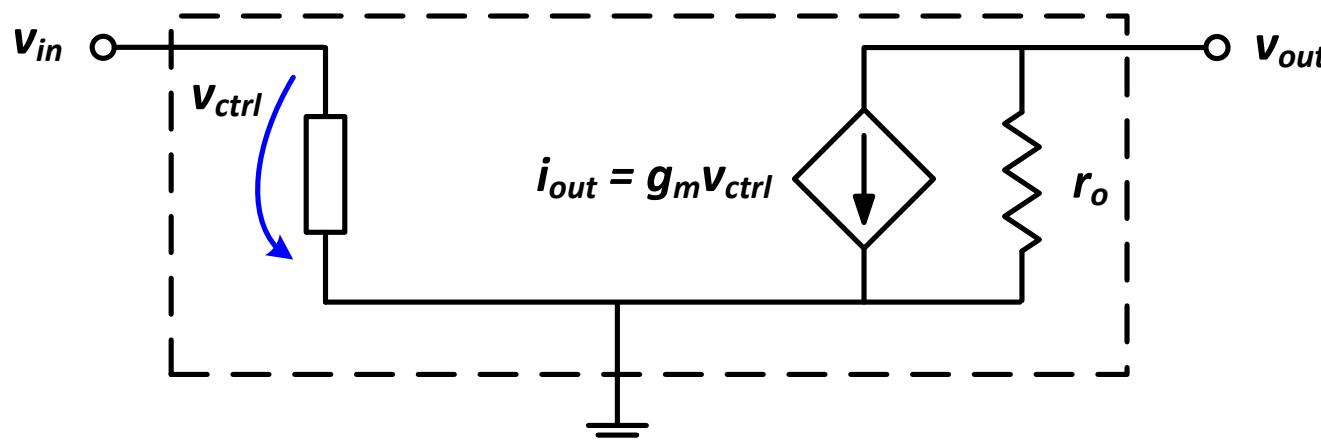
$$GBW = |A_v| \cdot BW = f_u = \frac{g_m}{2\pi C_L}$$



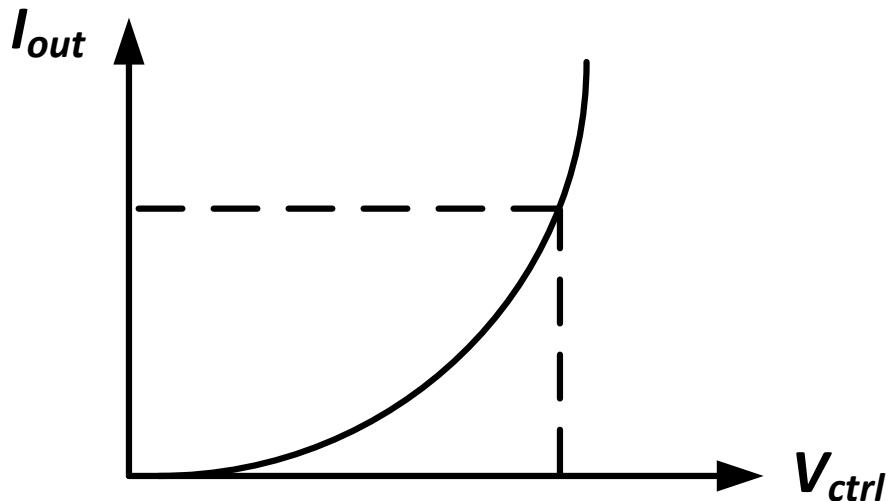
g_m Controls the Noise

- We can show that for both MOSFET thermal noise and BJT shot noise

$$v_{n,in}^2(f) \propto \frac{1}{g_m}$$



We Must Pay I_Q to Buy g_m



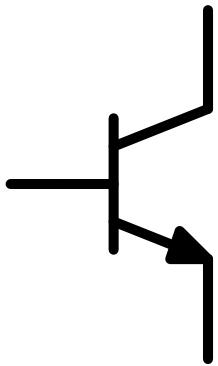
The Transistor Efficiency

$$TE = \frac{\text{What you want}}{\text{What you pay}} = \frac{g_m}{I_Q}$$

Outline

- Why gm/ID?
- **The BJT Story**
- The MOSFET Story
- The MOSFET Design Problem
- The Look-up Tables (LUTs)
- Design Examples

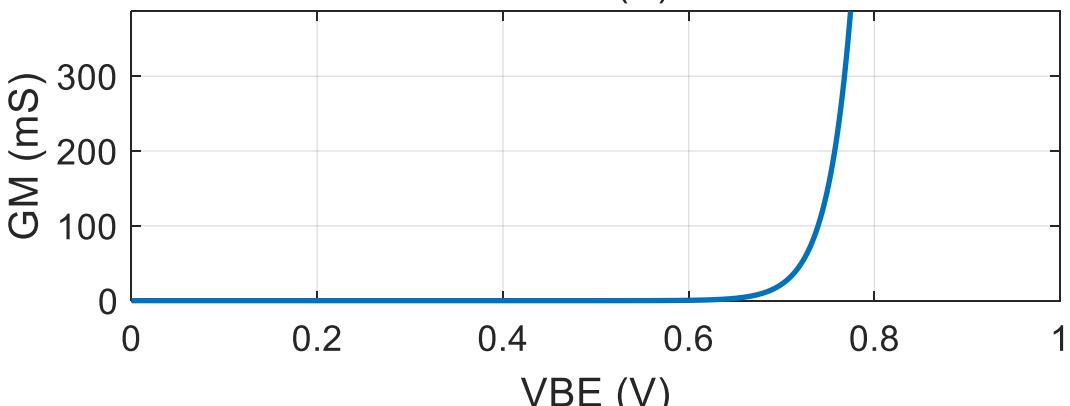
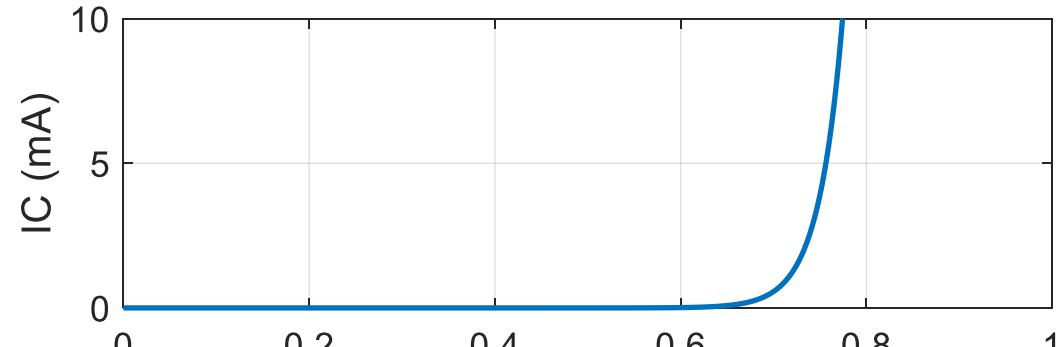
The BJT



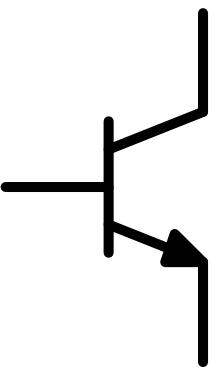
$$I_C = I_S e^{\frac{V_{BE}}{V_T}}$$

$$g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{V_T}$$

$$\frac{g_m}{I_C} = \frac{1}{V_T} \approx \frac{1}{26 \text{ mV}} = 38.5 \text{ S/A}$$



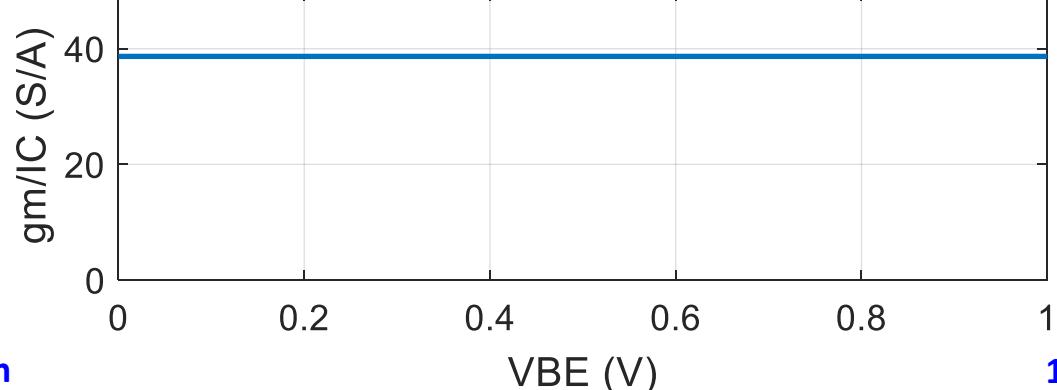
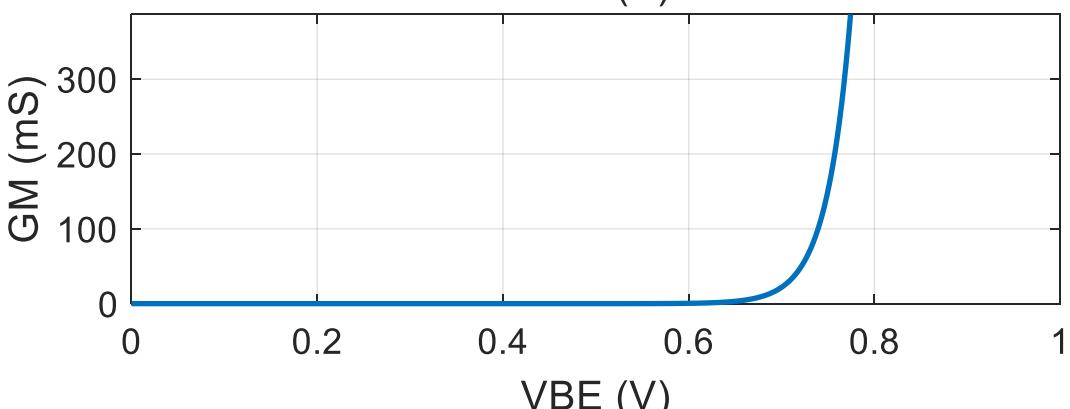
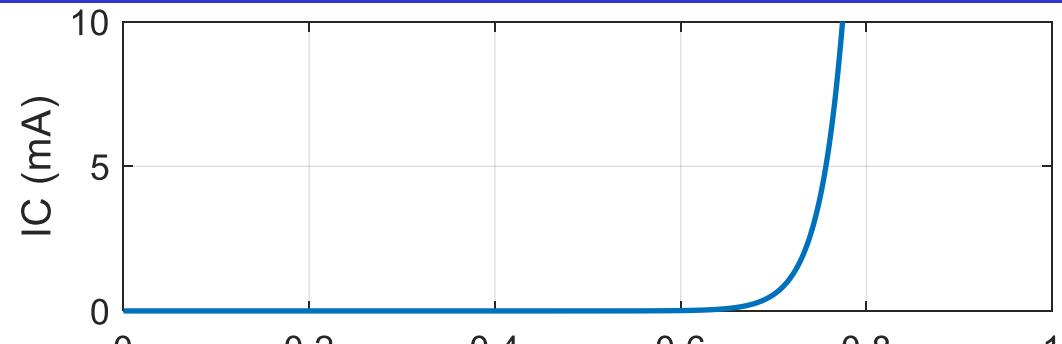
TE Visualized: Method #1



$$I_C = I_S e^{\frac{V_{BE}}{V_T}}$$

$$g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{V_T}$$

$$\frac{g_m}{I_C} = \frac{1}{V_T} \approx \frac{1}{26 \text{ mV}} = 38.5 \text{ S/A}$$



TE Visualized: Method #2

$$\log_e(y) = \ln(10) \log_{10}(y) \approx 2.3 \log_{10}(y)$$

$$\frac{\partial \log_e(I_C)}{\partial V_{BE}} = \frac{\partial I_C / \partial V_{BE}}{I_C} = \frac{g_m}{I_C}$$

$$\frac{\partial \log_e(y)}{\partial x} = \frac{\partial y / \partial x}{y}$$

$$\frac{\partial \log_{10}(I_C)}{\partial V_{BE}} \approx \frac{1}{2.3} \frac{g_m}{I_C} \propto \frac{g_m}{I_C}$$

$$\frac{\partial \log_{10}(y)}{\partial x} \approx \frac{1}{2.3} \frac{\partial y / \partial x}{y}$$

TE \propto Slope of I_C on log scale

$$\frac{g_m}{I_C} \propto \frac{\partial \log_b(I_C)}{\partial V_{BE}}$$

TE Visualized: Method #2

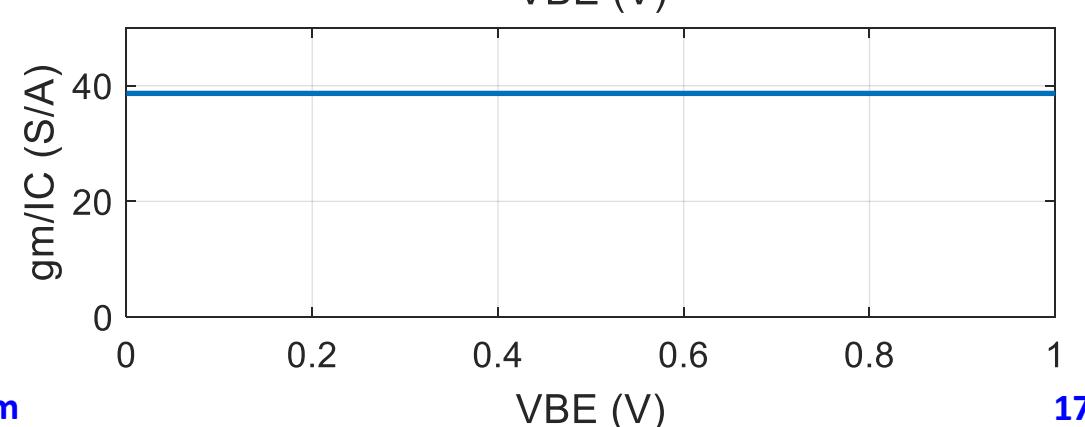
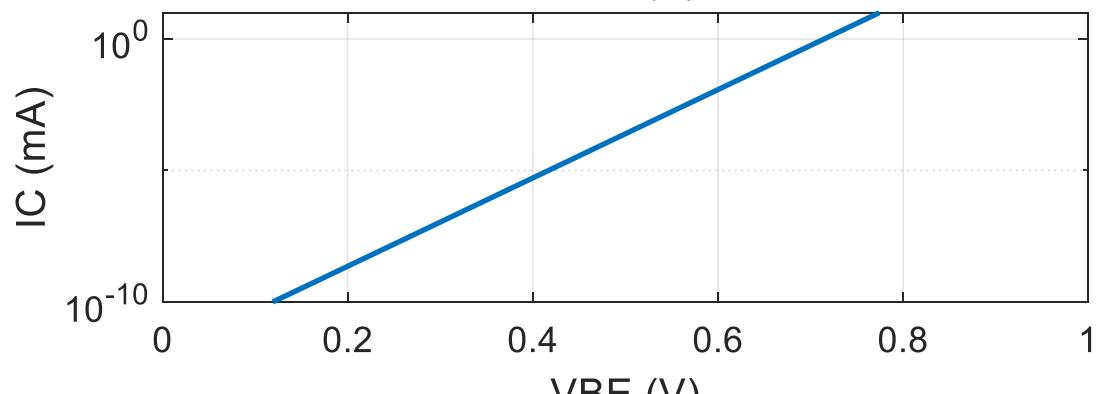
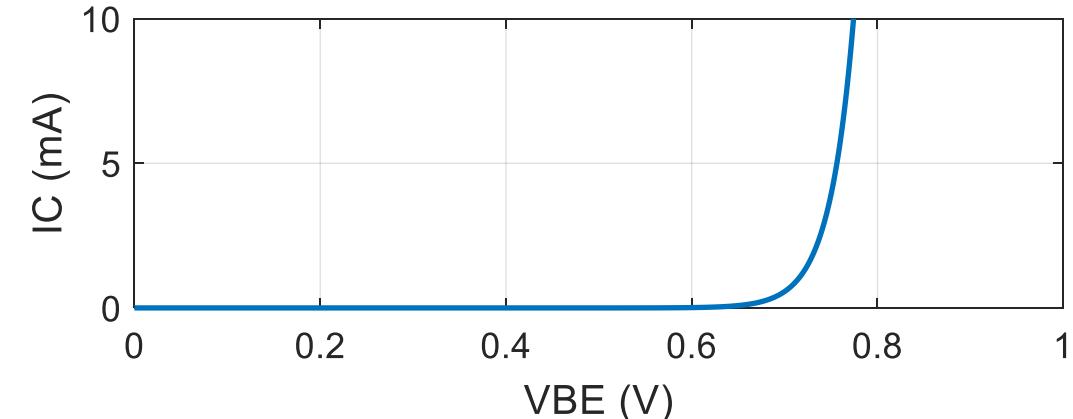
TE \propto Slope of I_C on log scale

$$\frac{g_m}{I_C} \propto \frac{\partial \log_b(I_C)}{\partial V_{BE}}$$

- Slope = constant!

$$\frac{g_m}{I_C} = \frac{1}{V_T} \approx \frac{1}{26 \text{ mV}} = 38.5 \text{ S/A}$$

- There is no gm/IC design methodology 😊!



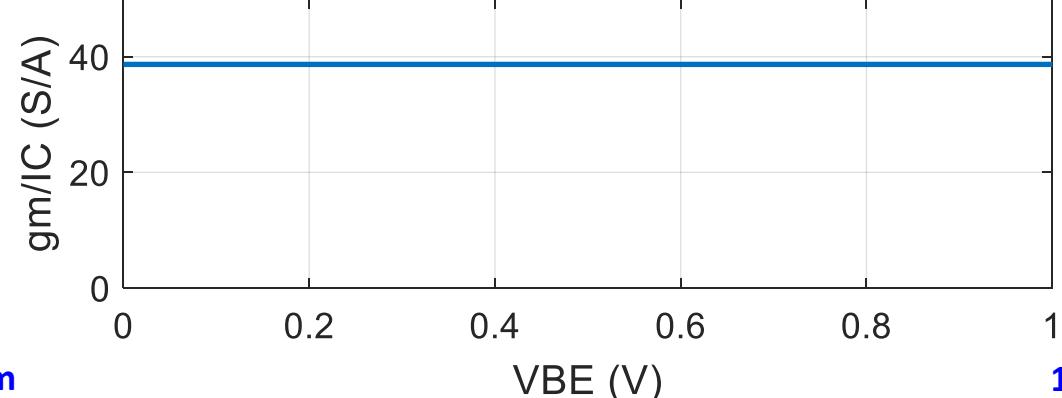
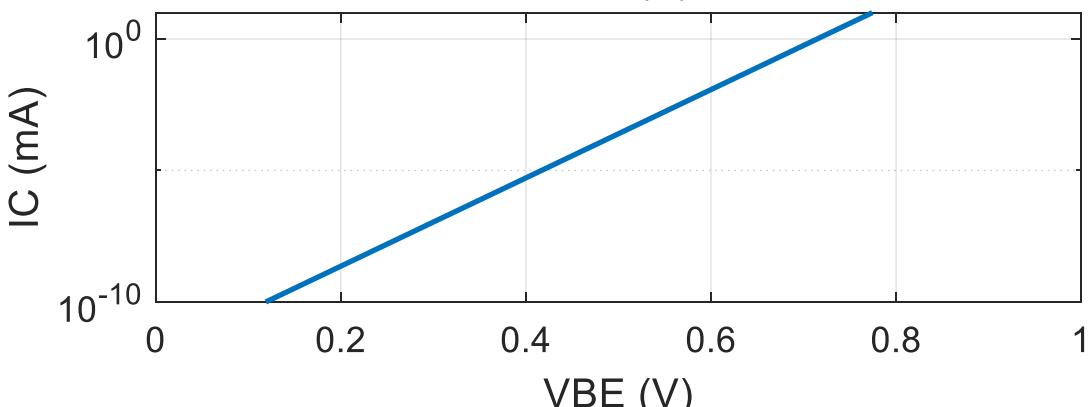
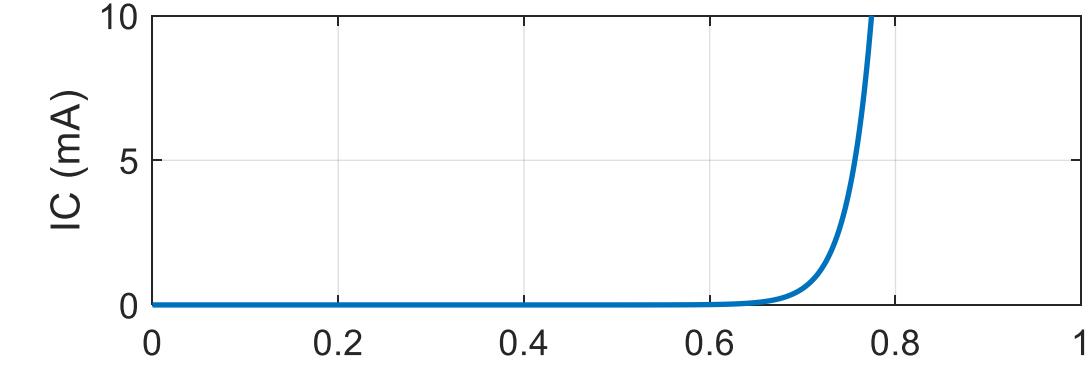
The Digital Perspective

$$\frac{g_m}{I_C} = \frac{1}{V_T} \approx \frac{1}{26 \text{ mV}} = 38.5 \text{ S/A}$$

- How much change in VBE for 10x change in IC

$$S = \left(\frac{\partial \log_{10} I_C}{\partial V_{BE}} \right)^{-1} = \left(\frac{1}{2.3} \frac{g_m}{I_C} \right)^{-1}$$

$$\approx 2.3V_T \approx 60 \text{ mV/decade}$$

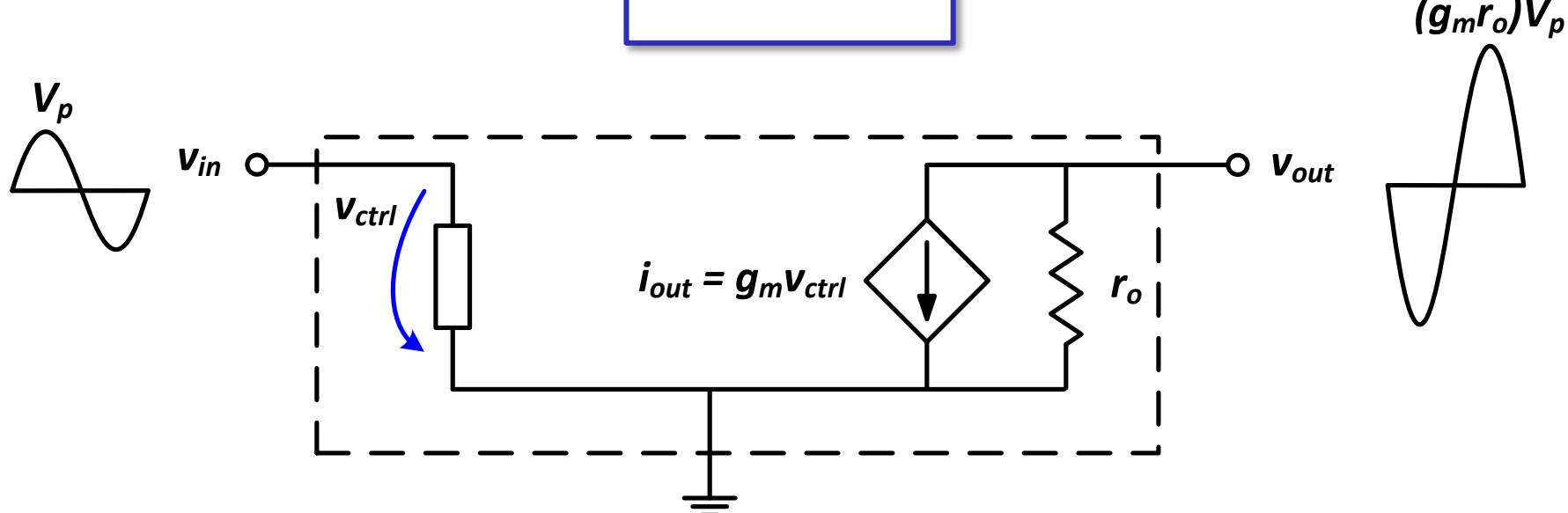


BJT Intrinsic Gain

$$v_{out} = -g_m v_{ctrl} \times r_o = -g_m v_{in} \times r_o$$

$$|A_v| = \frac{v_{out}}{v_{in}} = g_m r_o = g_m \cdot \frac{V_A}{I_C} = \frac{g_m}{I_C} \cdot V_A$$

$$|A_v| = \frac{V_A}{V_T}$$



Outline

- Why gm/ID?
- The BJT Story
- **The MOSFET Story**
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The Old-School MOSFET

- N-type channel region (inversion layer) formed at

$$V_{GS} > V_{TH}$$

$$V_{GS} = V_{TH} + V_{ov}$$

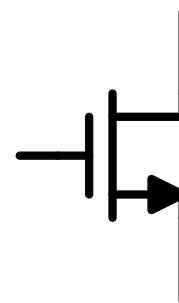
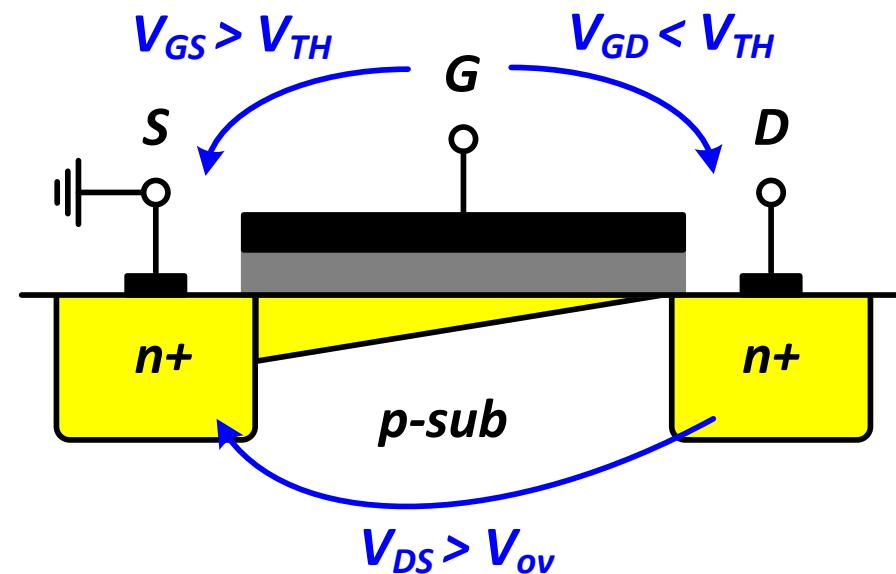
- Threshold voltage: $V_{TH} \sim 0.3V - 1V$

- The channel is pinched off if

$$V_{GD} \leq V_{TH} \Leftrightarrow V_{DS} \geq V_{ov}$$

- The simple long channel model (Square-law)

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 = \frac{\mu_n C_{ox}}{2} \frac{W}{L} V_{ov}^2$$



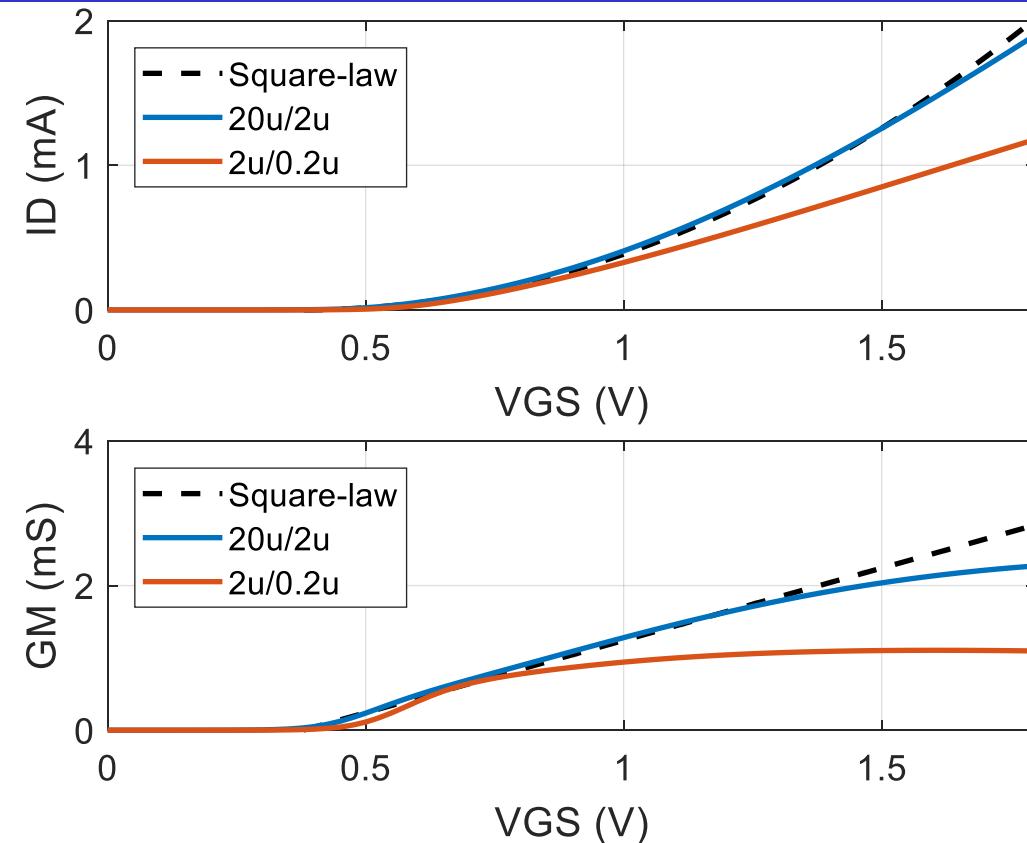
MOSFET IV Characteristics

□ The square law

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 = \frac{\mu_n C_{ox}}{2} \frac{W}{L} V_{ov}^2$$

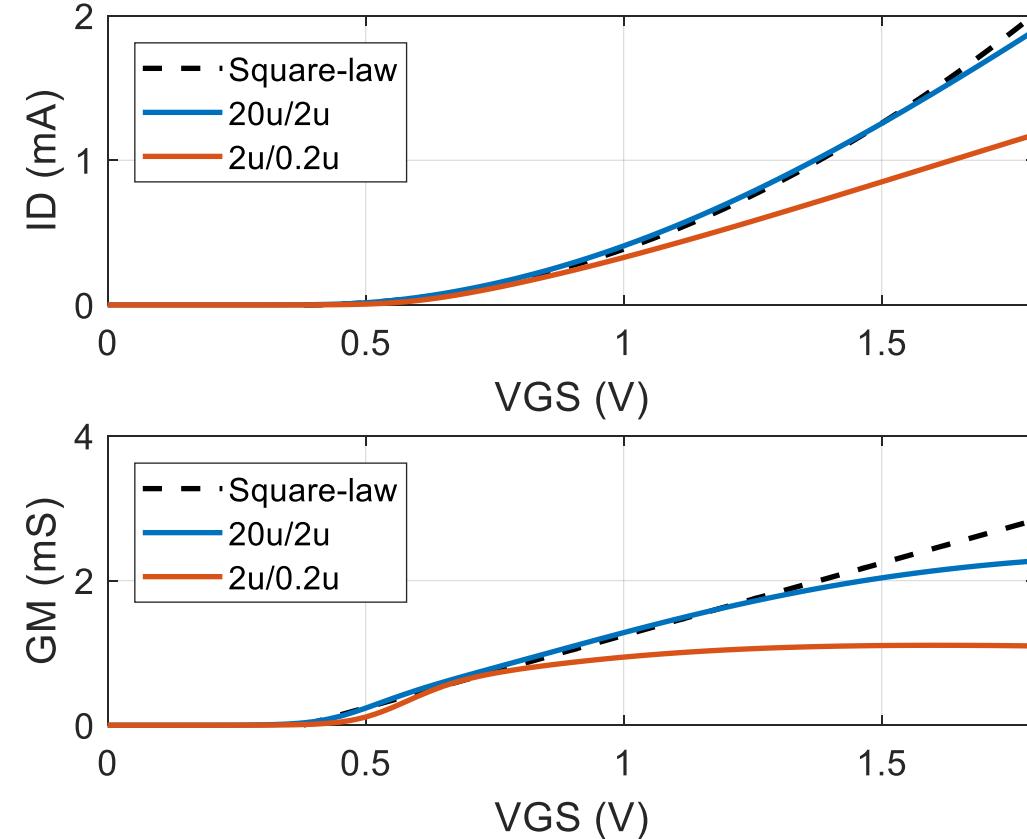
$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})$$

$$= \mu_n C_{ox} \frac{W}{L} V_{ov}$$



Short Channel MOSFET

- Short channel effects
 - Velocity saturation
 - ID has linear dependence on VGS
 - ID has no (or weak) dependence on L
 - Mobility degradation
- Linear rather than quadratic characteristics
 - g_m saturates at large V_{ov}
- The square law fails to describe strong-inversion (SI) **accurately**



MOSFET gm/ID

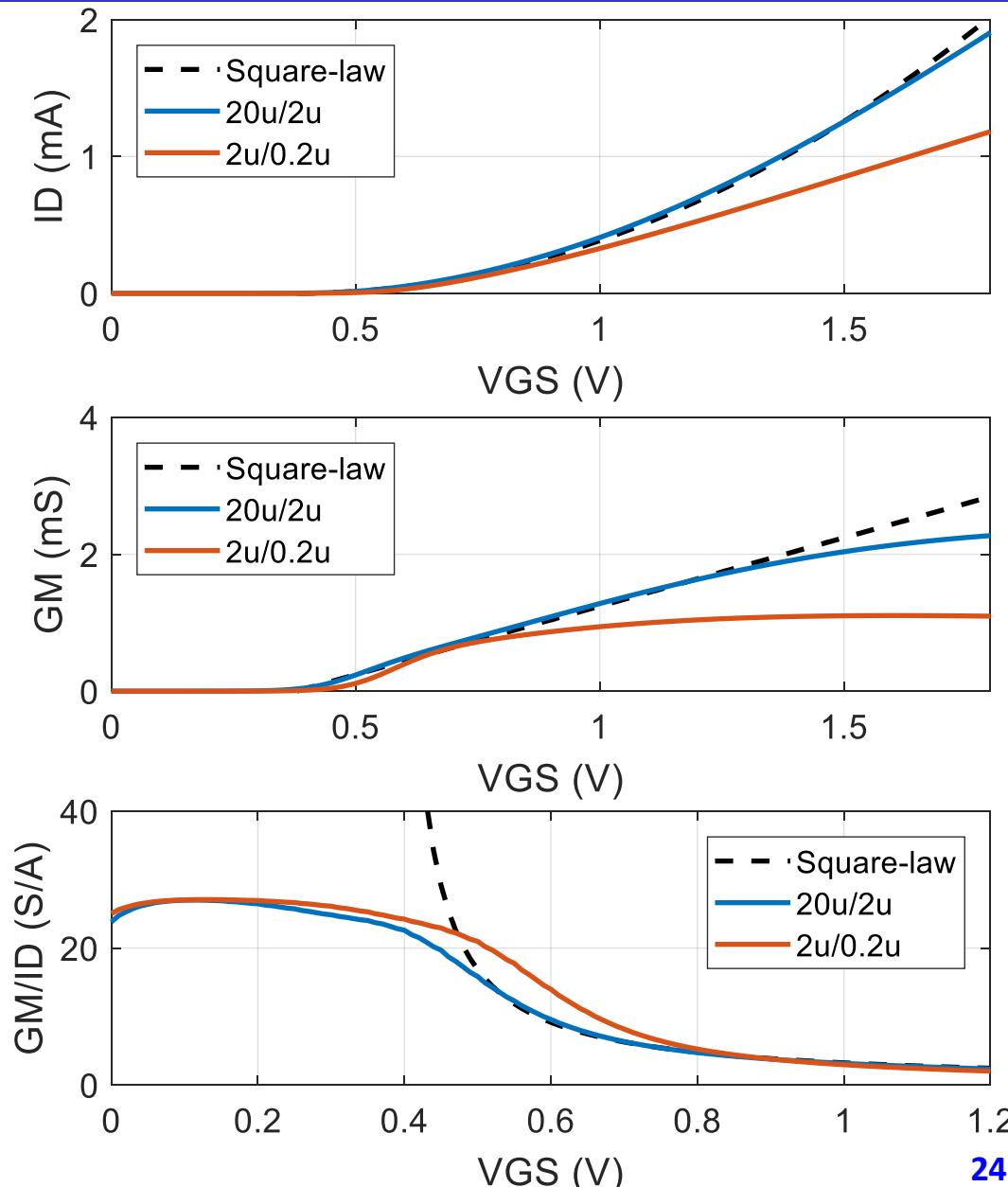
□ The square law

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 = \frac{\mu_n C_{ox}}{2} \frac{W}{L} V_{ov}^2$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})$$

$$= \mu_n C_{ox} \frac{W}{L} V_{ov}$$

$$\frac{g_m}{I_D} = \frac{2}{V_{GS} - V_{TH}} = \frac{2}{V_{ov}}$$

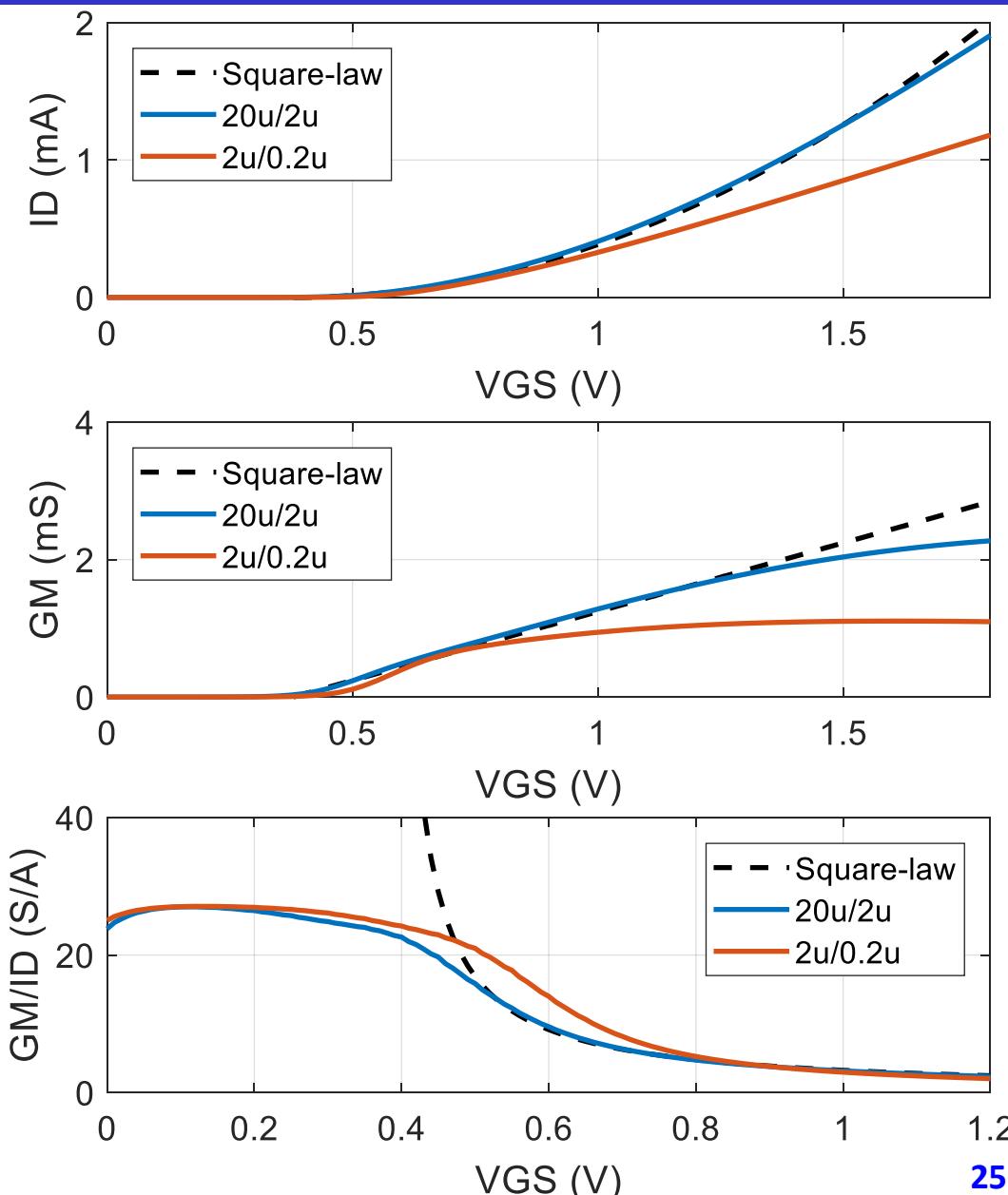


MOSFET gm/ID

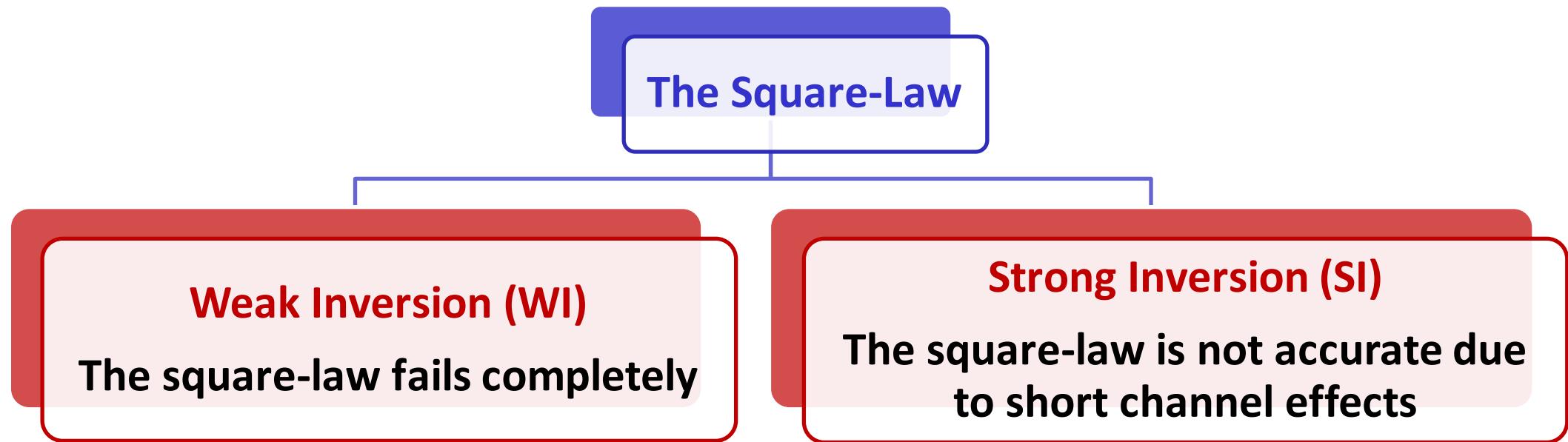
- The square law

$$\frac{g_m}{I_D} = \frac{2}{V_{GS} - V_{TH}} = \frac{2}{V_{ov}}$$

- The square law fails to describe weak-inversion (WI) **completely**
- **MOSFET gm/ID depends on bias point!**
 - Large in weak-inversion (WI)
 - Small in strong-inversion (SI)
- **Tuning MOSFET gm/ID (the TE) is the core of the gm/ID design methodology**



Square-Law End-of-Life?



- ❑ However, ...
 - For analog we use relatively long L and relatively low V_{ov}
 - Short channel effects (e.g., velocity sat.) are less pronounced
 - Simple model provides a great deal of intuition that is necessary in analog design
- ❑ You may use it to “partially” understand trends, **BUT NOT to calculate sizing!**

WI Revisited

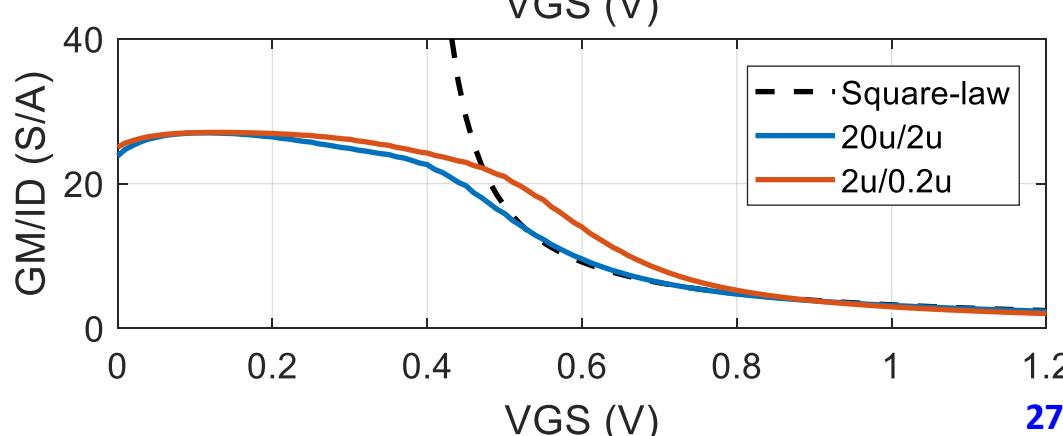
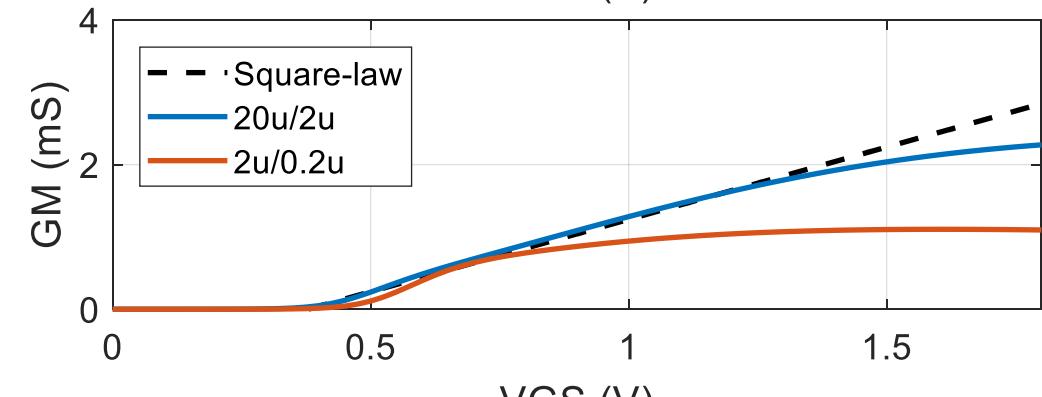
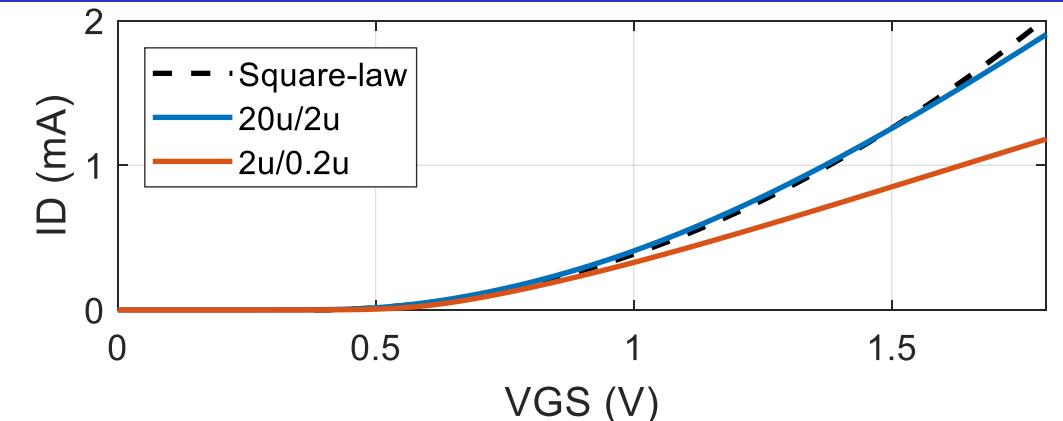
- The square law

$$\frac{g_m}{I_D} = \frac{2}{V_{GS} - V_{TH}} = \frac{2}{V_{ov}}$$

- The square law fails to describe weak-inversion (WI) **completely**

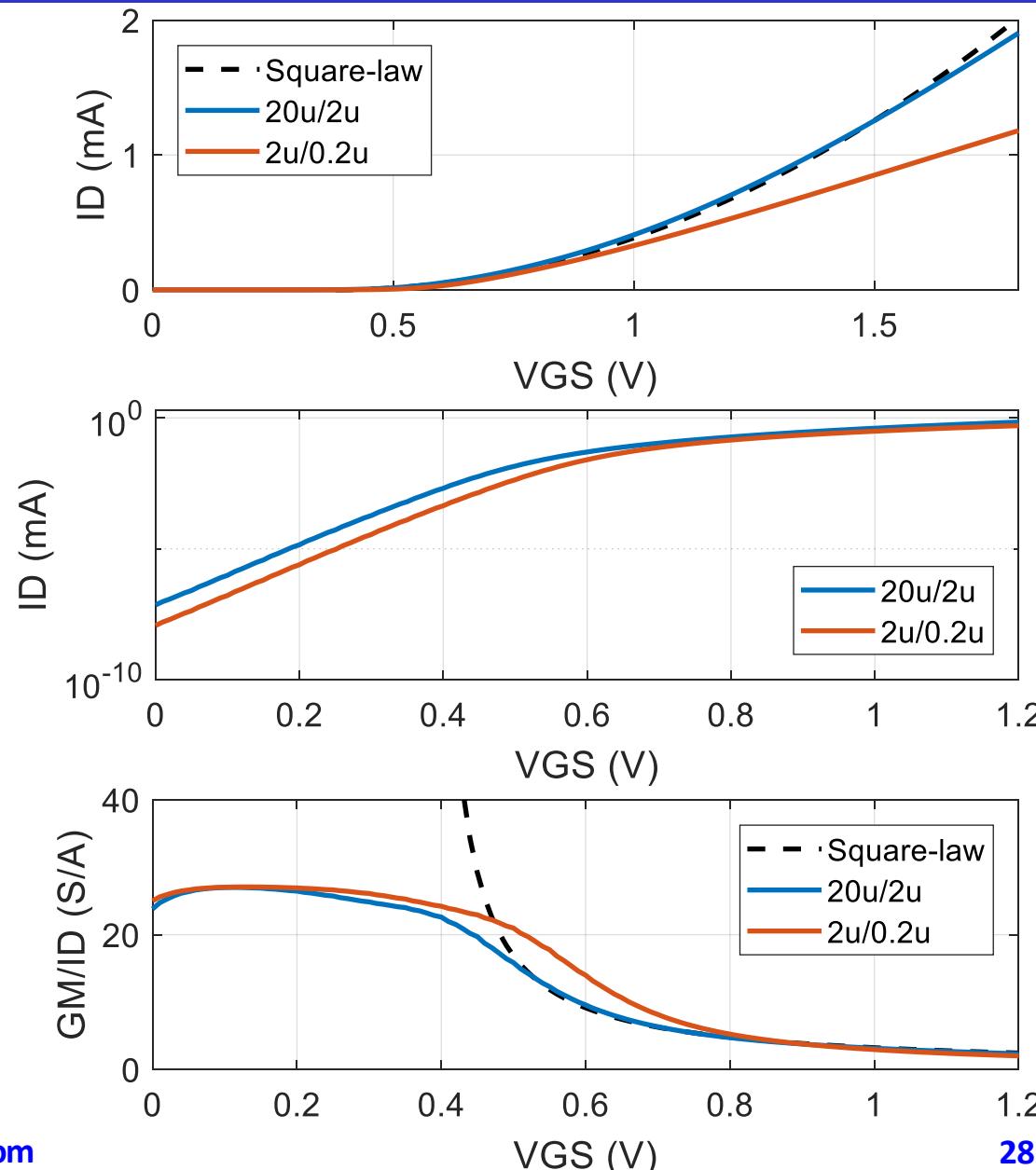
- So, what happens in subthreshold?

- Since gm/ID saturates, we expect ID characteristics is



MOSFET in Subthreshold

- ❑ gm/ID saturates
- ❑ log(ID) vs VGS must be straight line
(constant slope)!
- ❑ ID depends exponentially on VGS
- ❑ Similar to BJT behavior?!



Subthreshold Operation (Weak Inversion)

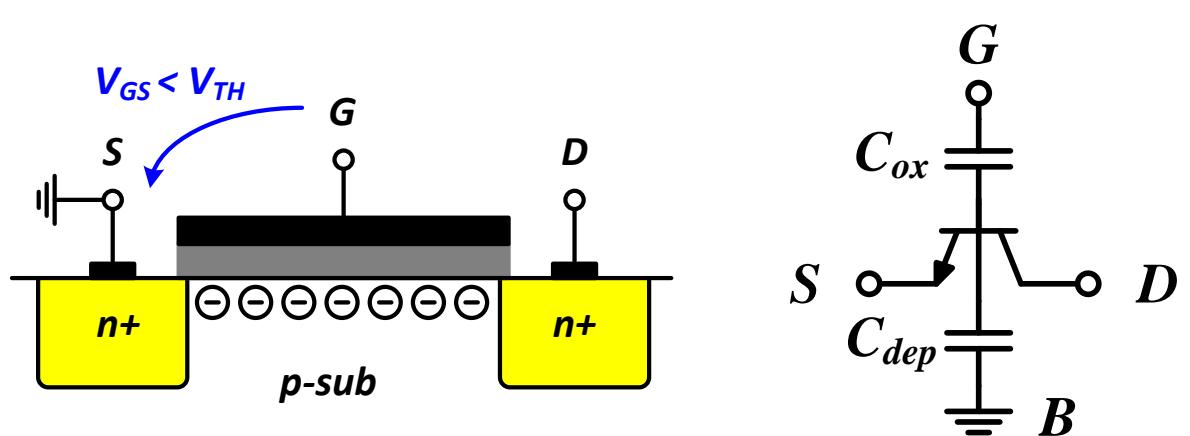
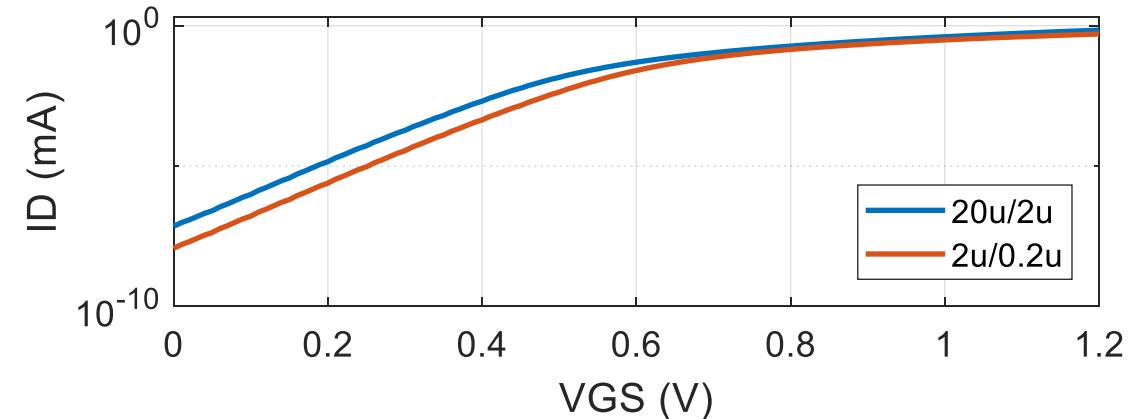
- MOSFET behaves as a BJT (npn for an NMOS) with its base coupled to the gate through capacitive divider

$$V_{BE} = V_{GS} \frac{C_{ox}}{C_{ox} + C_{dep}} = \frac{V_{GS}}{n}$$

$$n = \frac{C_{ox} + C_{dep}}{C_{ox}} > 1$$

$$I_D \approx I_{off} e^{\frac{V_{BE}}{V_T}} = I_{off} e^{\frac{V_{GS}}{nV_T}}$$

- For bulk MOSFET: $n \approx 1.2 \rightarrow 1.5$
- For SOI and FinFET: $n \approx 1.1$



gm/ID in Weak Inversion (WI)

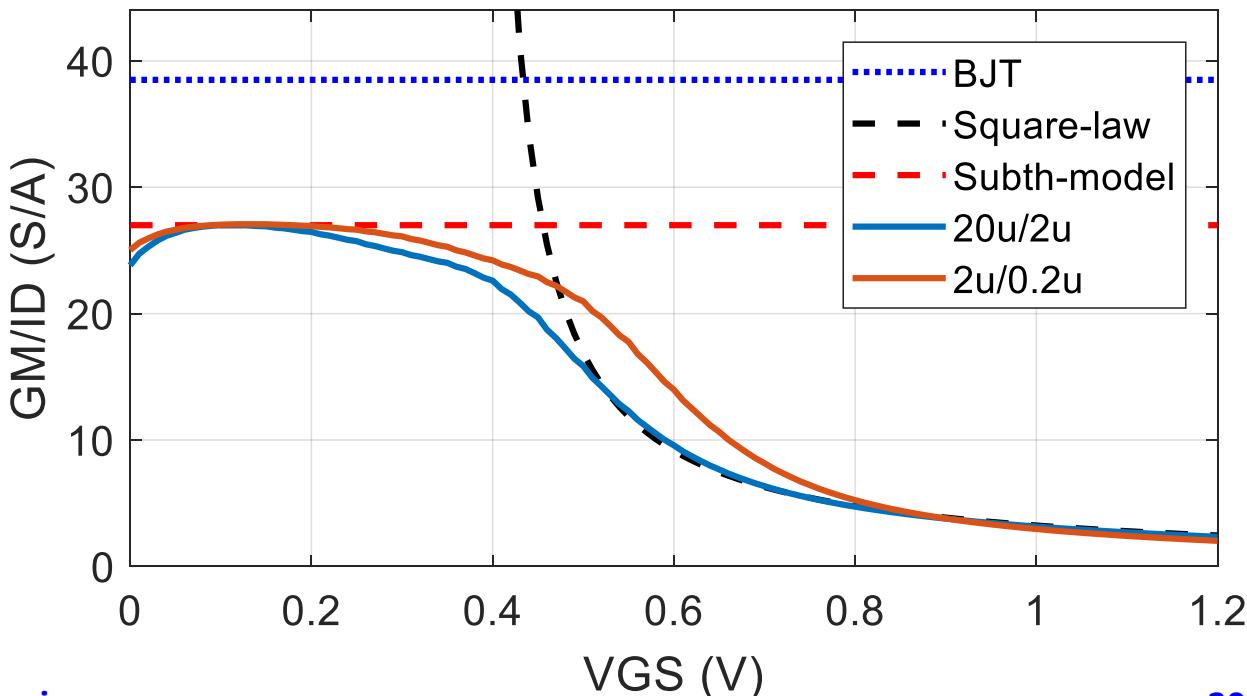
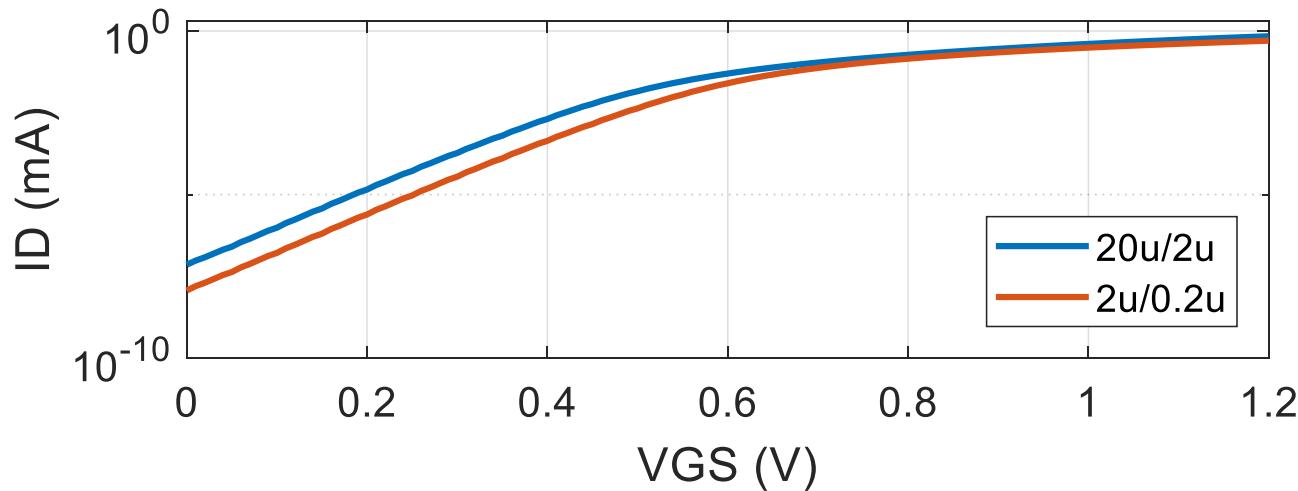
$$I_D \approx I_{off} e^{\frac{V_{GS}}{nV_T}}$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{nV_T}$$

$$\frac{g_m}{I_D} = \frac{1}{nV_T} \approx \frac{38.5}{n}$$

□ $n \approx 1.1 \rightarrow 1.5$

$$\frac{g_m}{I_D} = \frac{1}{nV_T} \approx 25 \rightarrow 35 S/A$$



The Digital Perspective: The Subthreshold Slope (S)

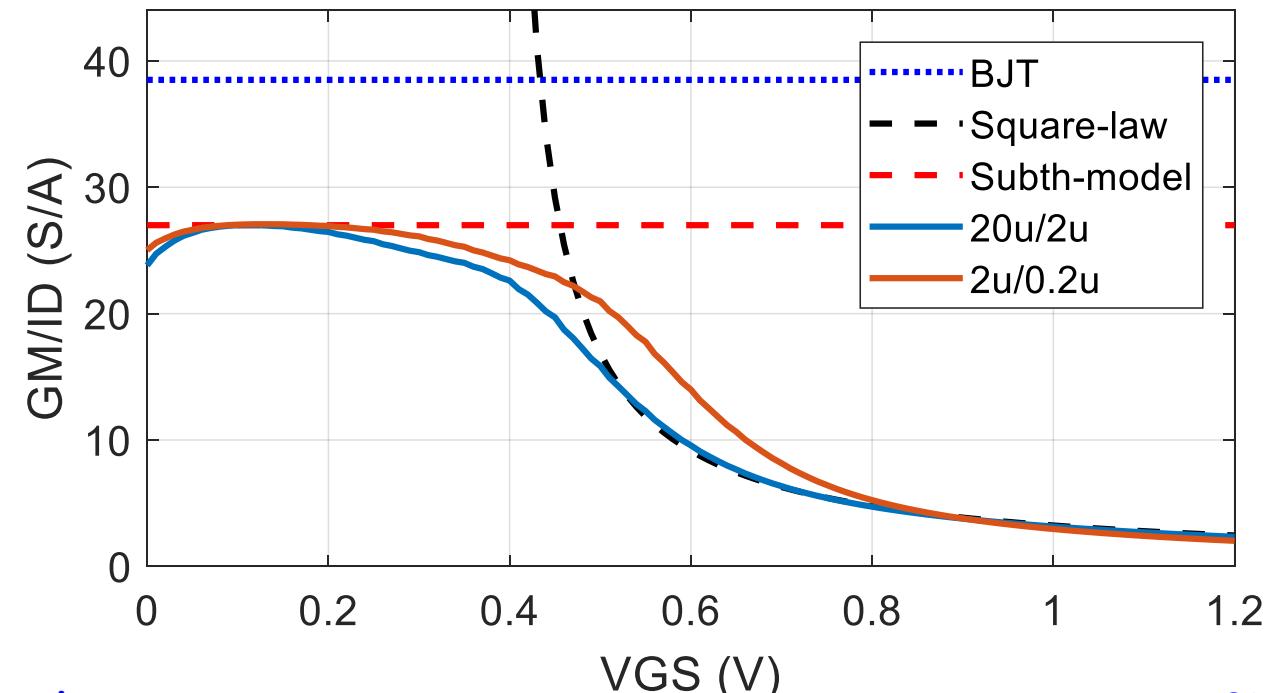
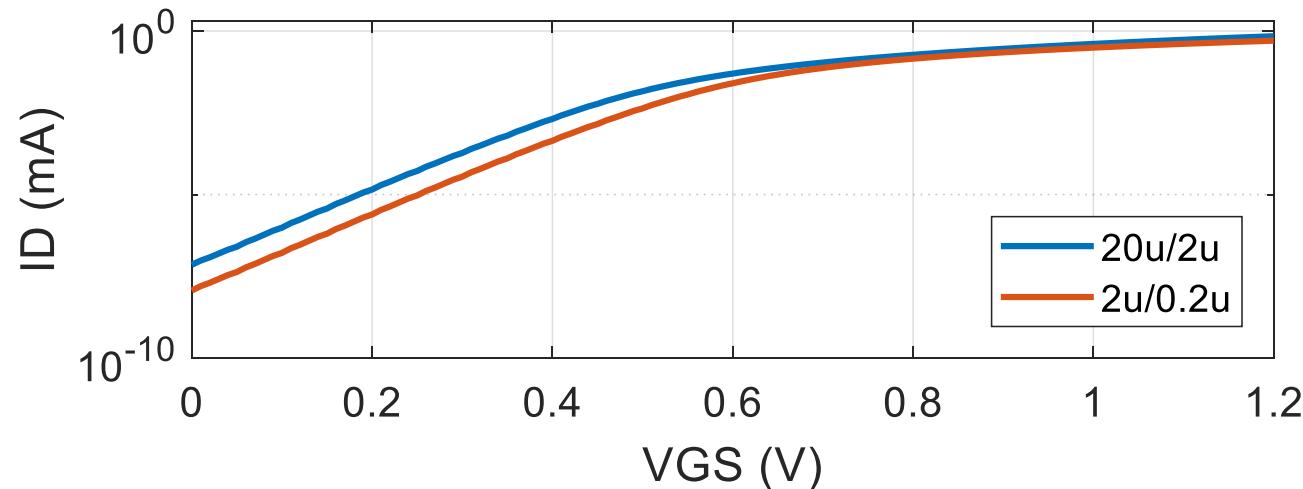
- $n \approx 1.1 \rightarrow 1.5$

$$\frac{g_m}{I_D} = \frac{1}{nV_T} \approx 25 \rightarrow 35 \text{ S/A}$$

- Change in VGS for 10x change in ID

$$S = \left(\frac{\partial \log_{10} I_D}{\partial V_{GS}} \right)^{-1} = \left(\frac{1}{2.3} \frac{g_m}{I_D} \right)^{-1}$$

$$\approx 2.3nV_T \approx 66 \rightarrow 90 \text{ mV/decade}$$



MOSFET Intrinsic Gain

$$|A_v| = g_m r_o = g_m \cdot \frac{V_A}{I_D} = \frac{g_m}{I_D} \cdot V_A$$

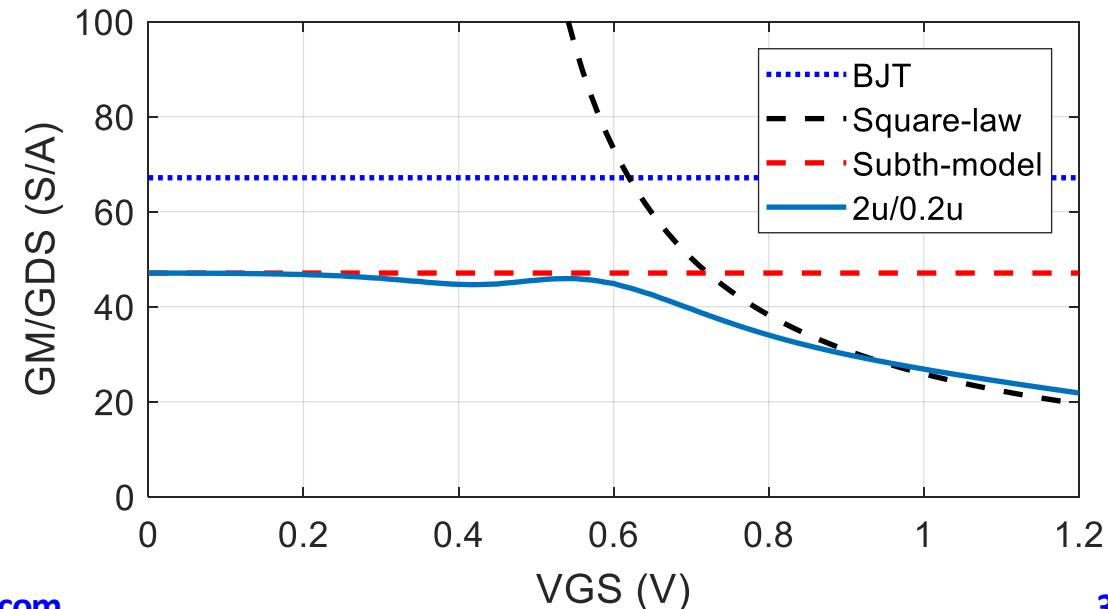
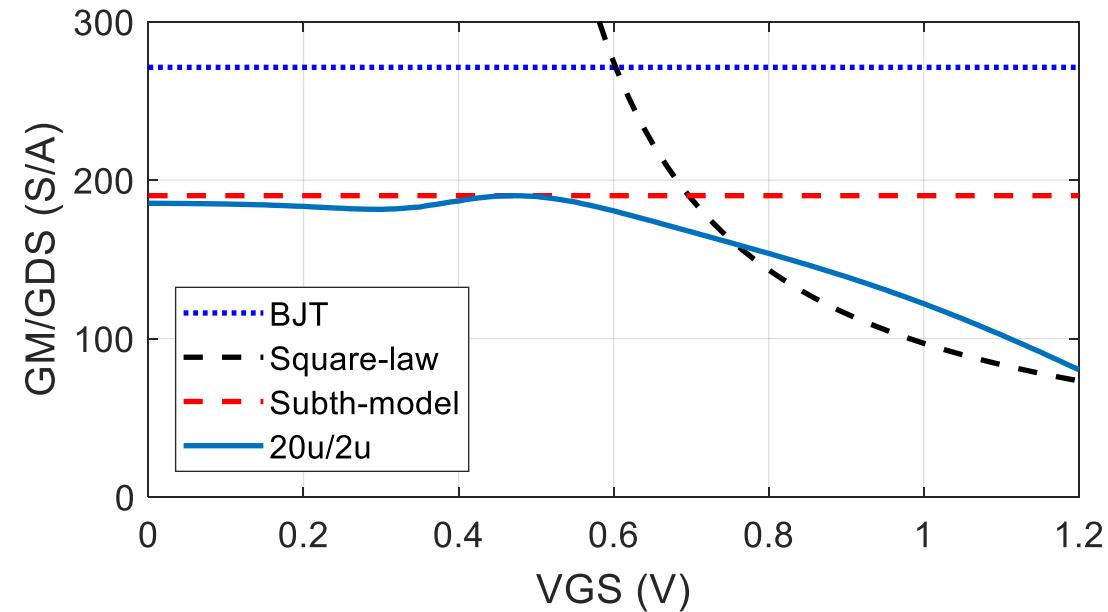
- Longer L gives higher V_A
- Square-law prediction

$$|A_v| = \frac{g_m}{I_D} \cdot V_A = \frac{2V_A}{V_{ov}}$$

- Trend is OK
 - But poor-fit even for long L!

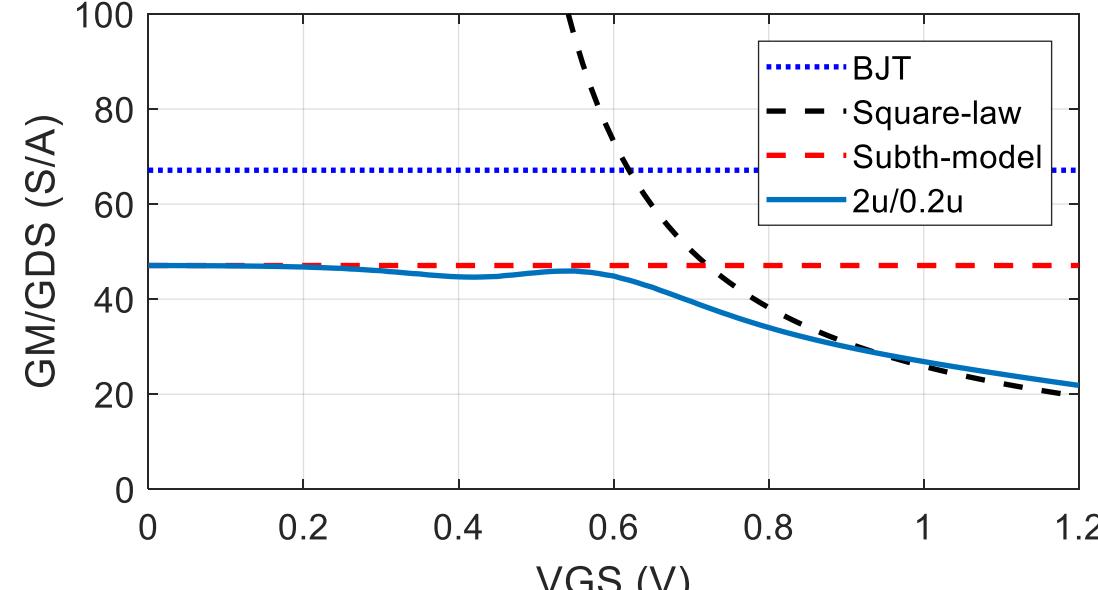
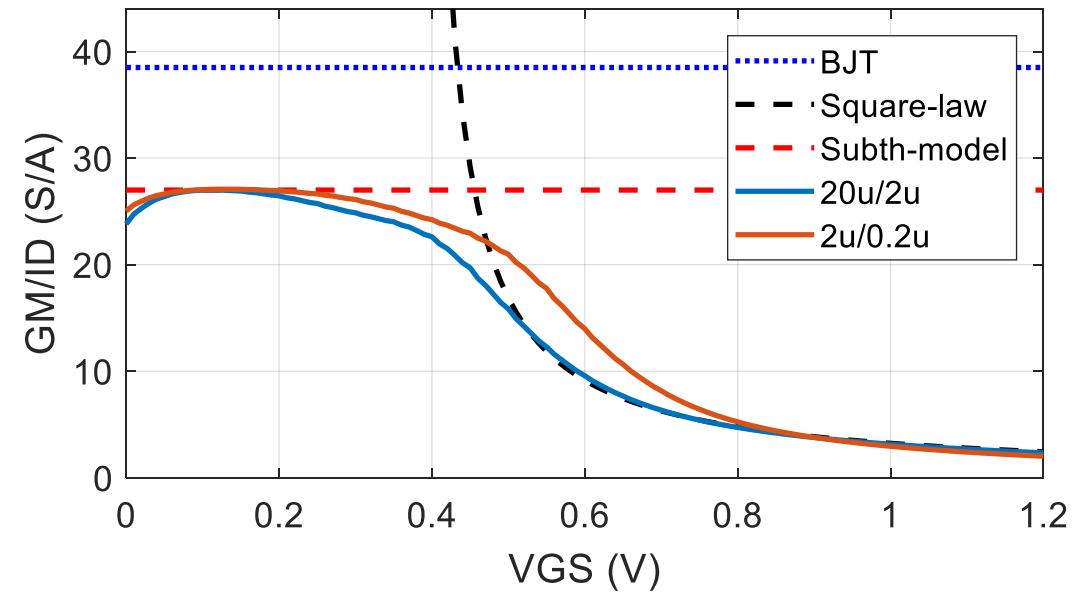
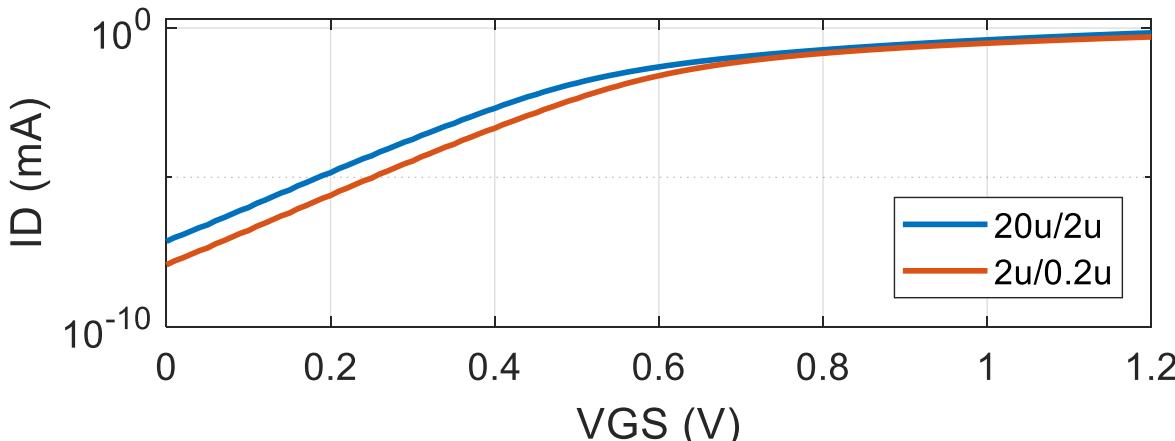
- Subthreshold-model prediction

$$|A_v| = \frac{g_m}{I_D} \cdot V_A = \frac{V_A}{nV_T}$$



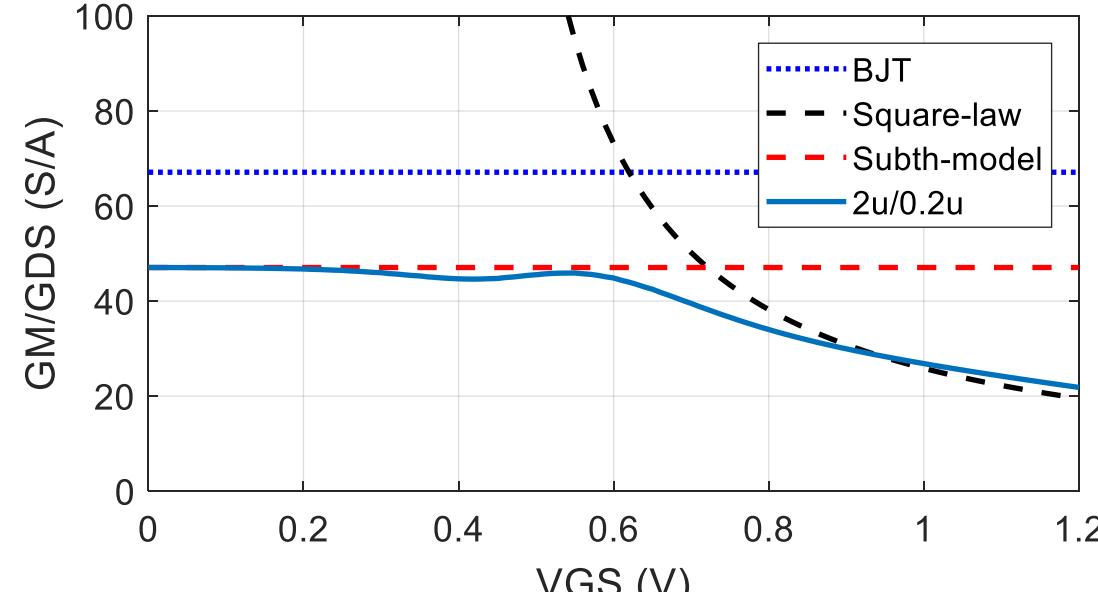
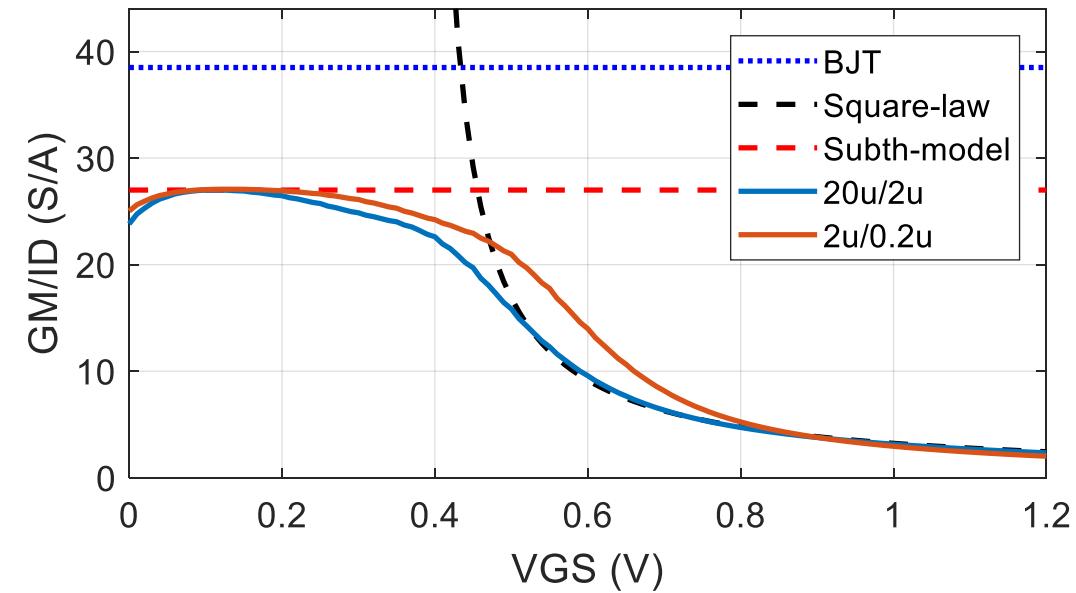
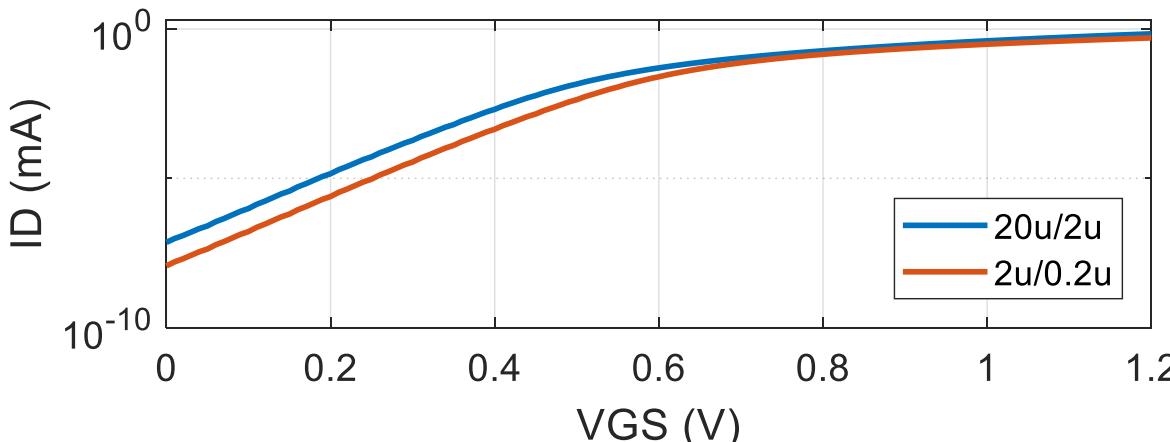
Operation in Weak Inversion (WI)

- You get high gm/ID and high gm/gds
- But current is exponentially decreasing
 - gm is exponentially decreasing
 - Speed is exponentially decreasing
- Why not keep the same ID and gm?
 - You need exponentially increasing W
 - Exponentially increasing area and parasitics



Operation in Moderate Inversion (MI)

- ❑ Operation in MI is becoming increasingly popular
- ❑ We can reap WI benefits
 - High gm/ID and high gm/gds
- ❑ Some degradation in speed is OK
 - Short channel MOSFETs are already very fast
- ❑ But no simple model exists...



Why Do We Need the Models?

- Models are necessary to “roughly” understand trends
- Models are necessary to help designer’s intuition

- Simple models help intuition, but are not accurate
- Accurate models provides NO intuition and are intractable

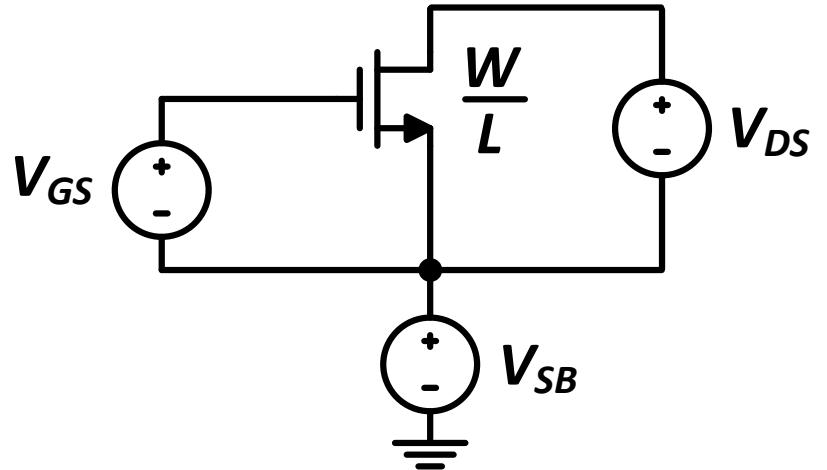
- But do we really need an accurate model?
 - We can calculate sizing using charts or lookup tables (LUTs)

Outline

- Why gm/ID?
- The BJT Story
- The MOSFET Story
- **The MOSFET Design Problem**
- The Look-up Tables (LUTs)
- Design Examples

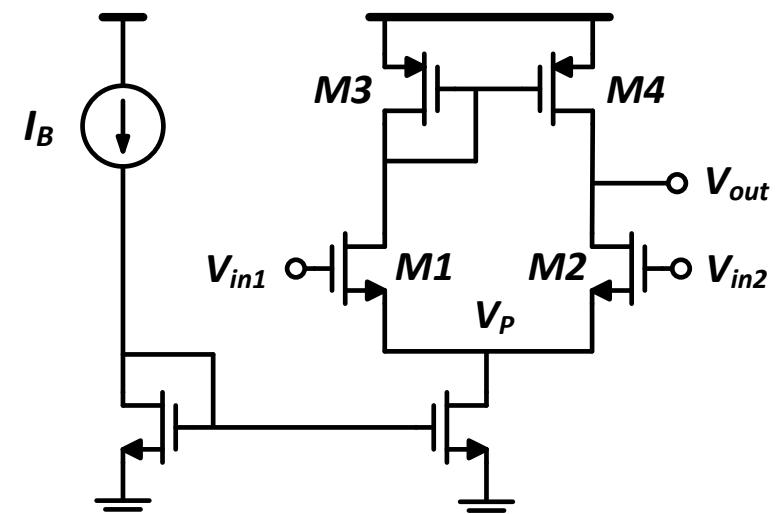
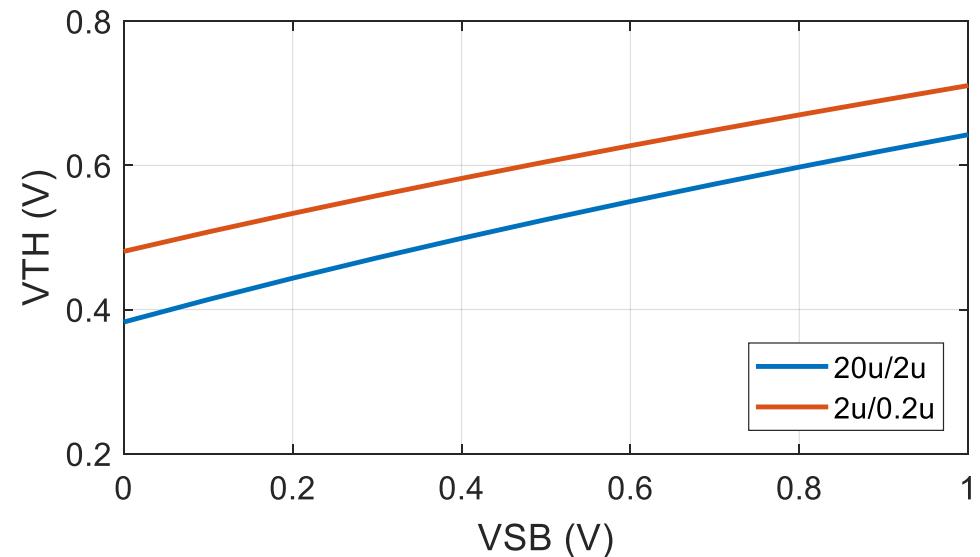
The Design Problem

- MOSFET is a function of five variables
- Three voltages
 - V_{GS}
 - V_{DS}
 - V_{SB}
- Two sizing parameters
 - L
 - W



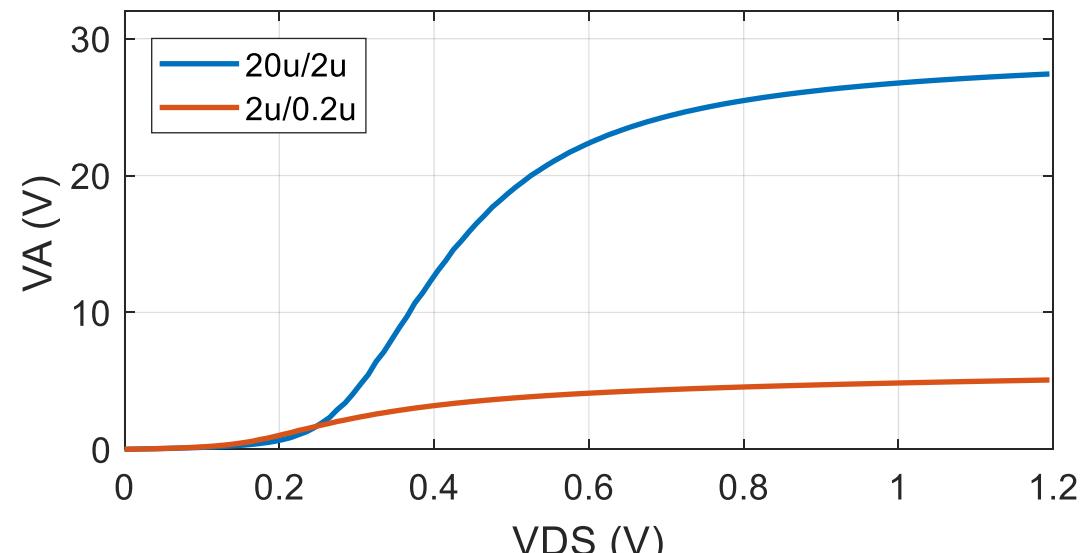
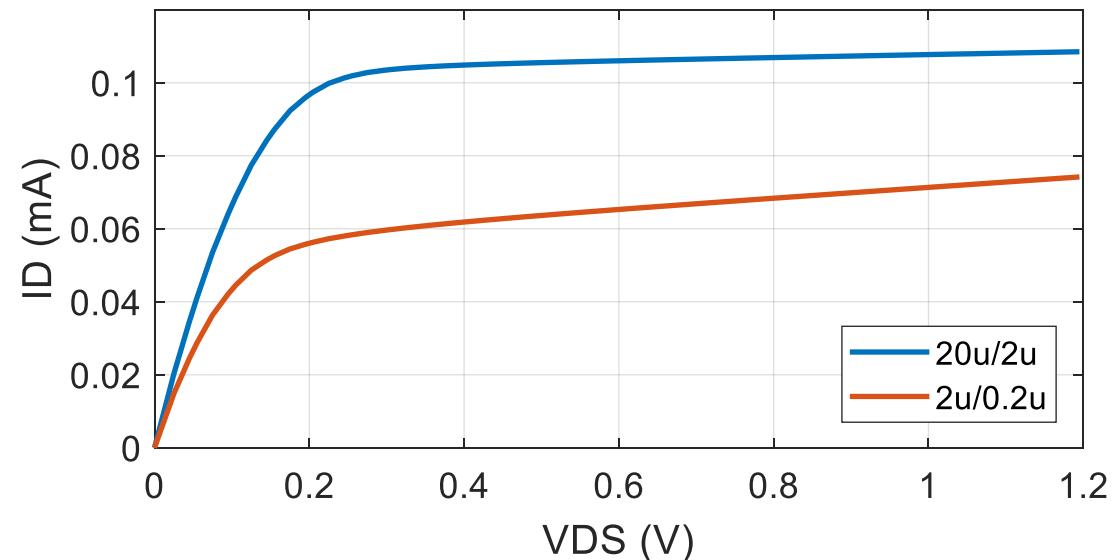
VSB

- VSB causes body effect
 - Increasing VSB increases VTH
- For devices in a dedicated well the body can be tied to the source
 - But extra area, extra well capacitance, coupling between S and D, and maybe extra noise
- Usually, VSB is not a designer degree-of-freedom (DOF)
 - It is imposed by the circuit topology



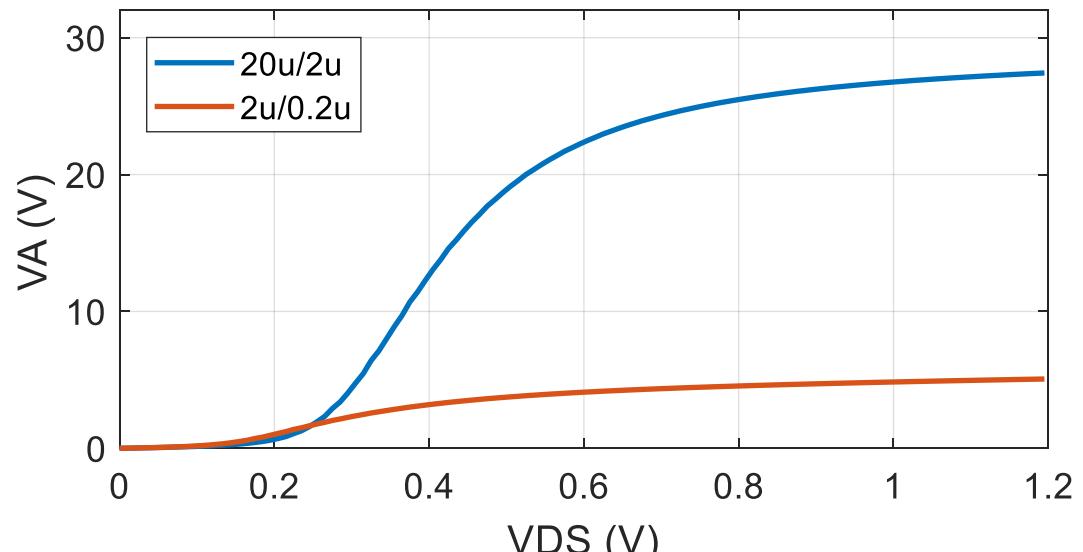
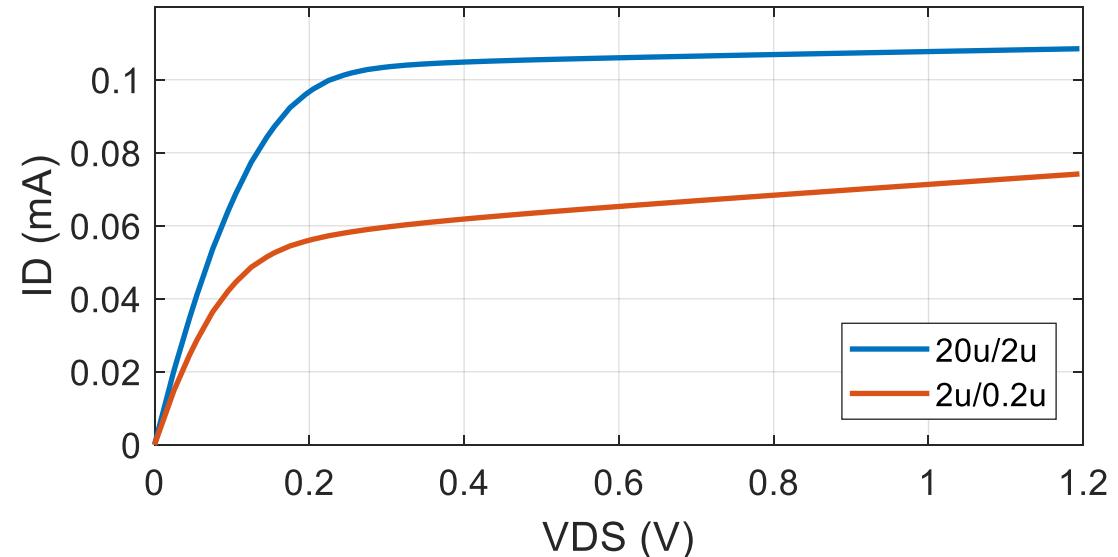
VDS

- Ideally, VDS should not affect ID
 - MOSFET is a VCCS for $V_{DS} > V_{Dsat}$
- But practically, increasing VDS increases ID
 - CLM and DIBL
- VDS effect modeled by $r_o = V_A/I_D = 1/\lambda I_D$
- V_A increases as we increase VDS
 - r_o increases as we go deeper into saturation
- V_A increases as we increase L
 - But need $V_{DS} = V_{Dsat} + \text{margin}$ to notice the difference
- But what is V_{Dsat} ?



V_{Dsat}

- The definition of V_{Dsat} is a bit **vague**
 - ID keeps increasing due to CLM/DIBL
 - At edge of saturation ($V_{DS} = V_{Dsat}$) r_o is quite low
- For a square-law device $V_{Dsat} = V_{ov}$
- In simulation models V_{Dsat} is a bit complex parameter
 - And again, it is vague and not really meaningful



VDsat and V*

- For the square-law

$$\frac{g_m}{I_D} = \frac{2}{V_{ov}} \rightarrow V_{ov} = \frac{2}{g_m/I_D}$$

- We define a new parameter inspired by Vov

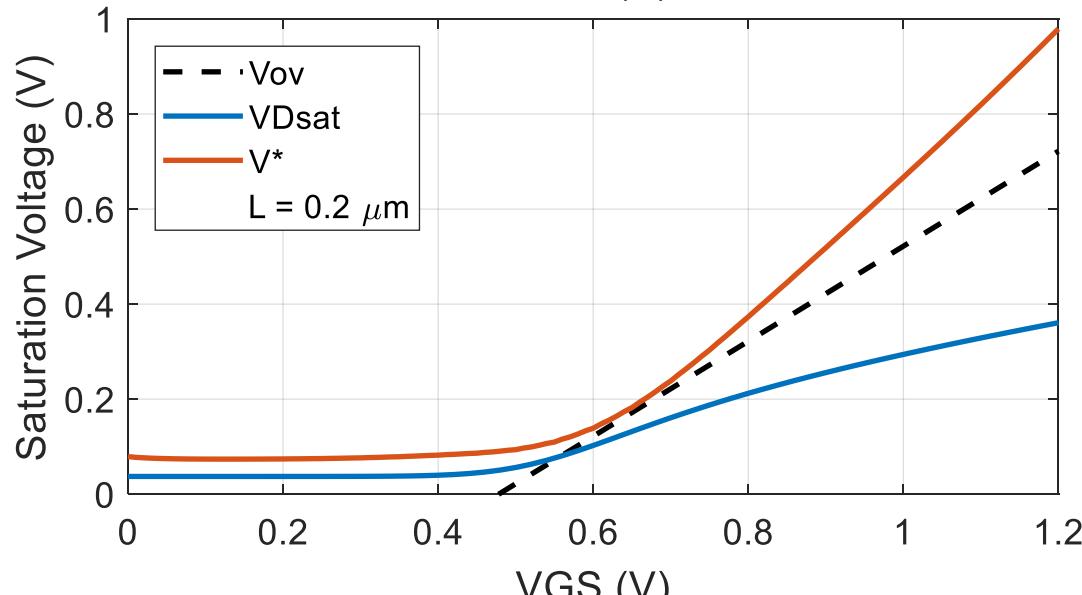
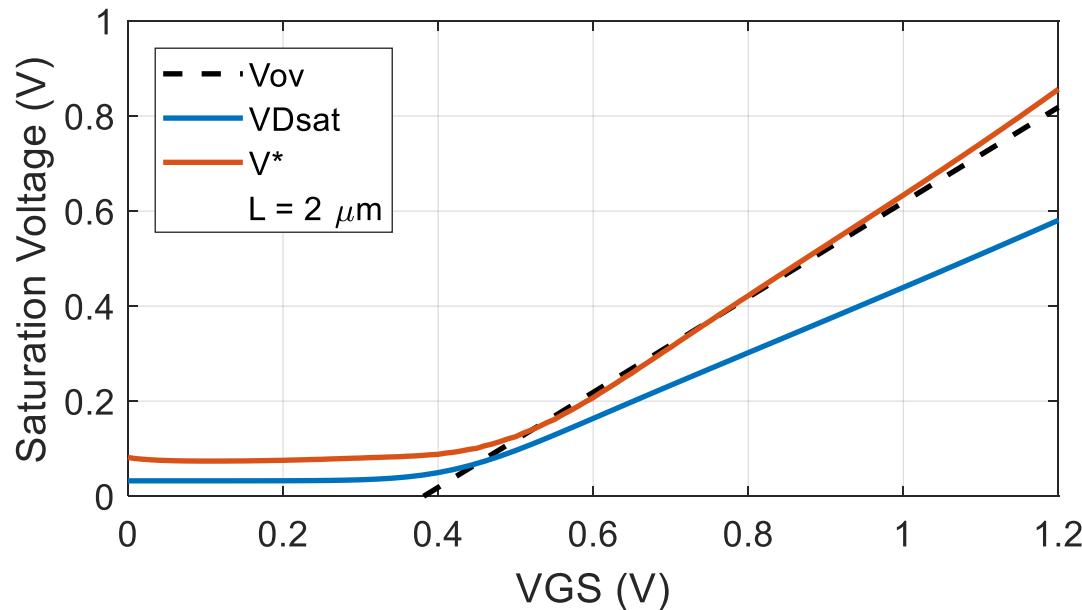
$$V^* = \frac{2}{g_m/I_D}$$

- V* is computed from simulation data

- It is valid in all regions (WI, MI, and SI)

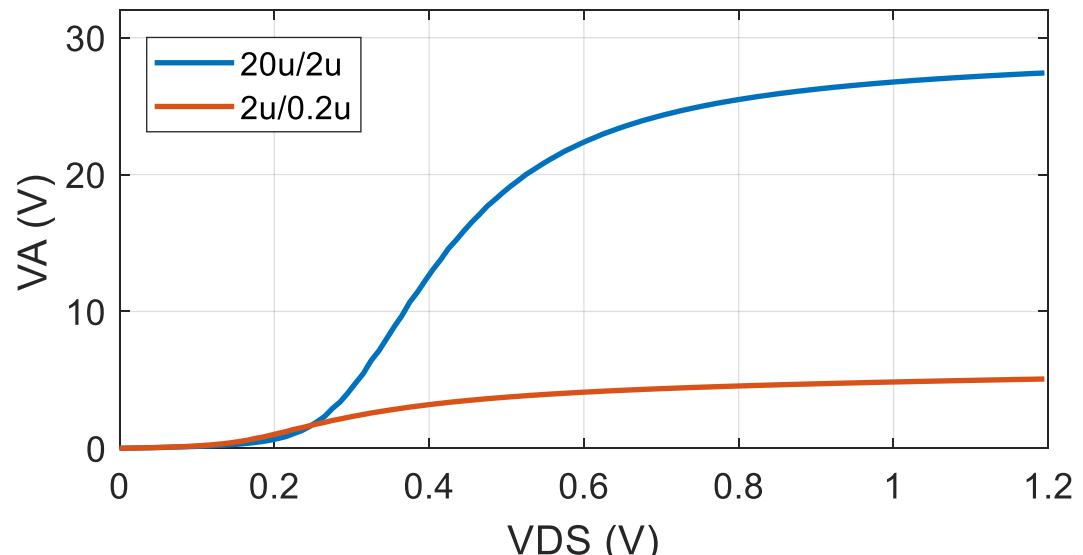
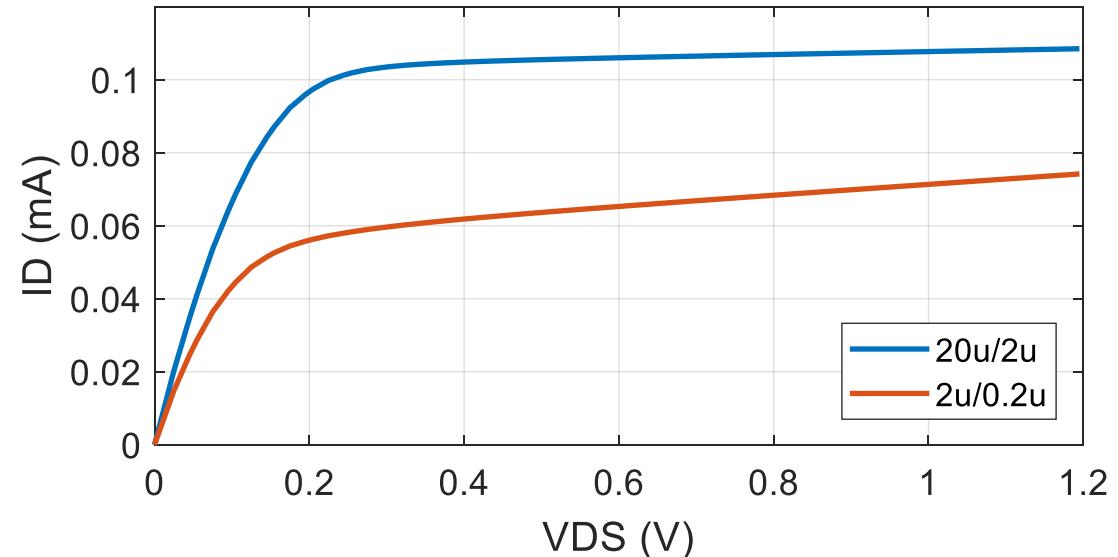
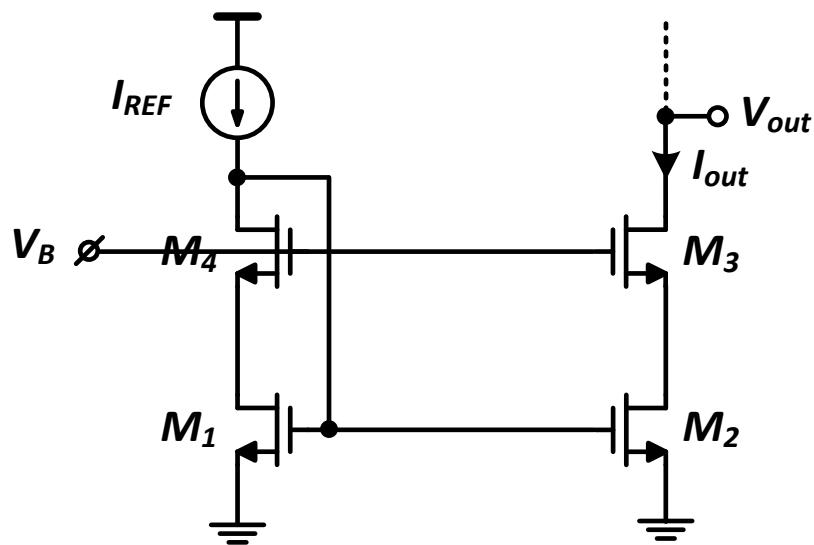
- V* is always larger than VDsat

- It can be used as an estimate for saturation
 - It guarantees biasing a little deeper into saturation



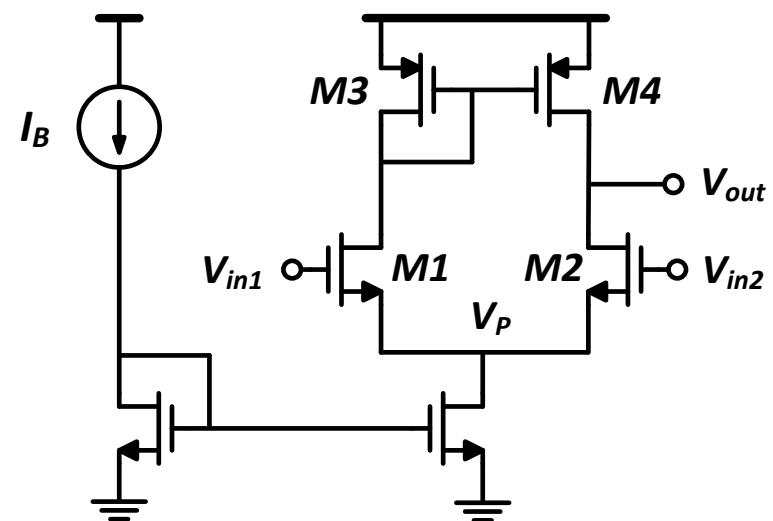
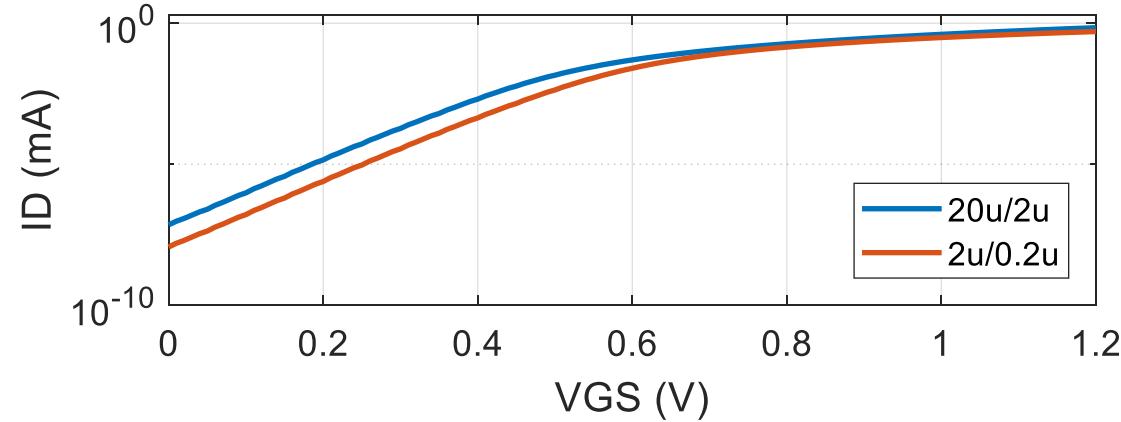
VDS

- VDS is set to $V^* + V_{Dsat_margin}$
- It is desirable to make the margin large
 - But this will come at the expense of headroom, swing, input range, etc.
- Low supply makes the problem more difficult



VGS

- VGS is the primary voltage controlling the device behavior
- VGS is tightly coupled to ID
 - MOSFET is a VCCS
- In analog ICs, we usually set the bias current (ID) rather than setting the bias voltage (VGS)
 - Current mirror biasing
- Replace VGS by ID in the DOFs list



L

- Shorter L allows smaller area and higher speed
- But analog designers usually tend to use relatively long L

Use shorter L if you want

- Smaller area
- Smaller capacitance
- High speed (high $f_T = \frac{g_m}{2\pi C_{gg}}$)

Use longer L if you want

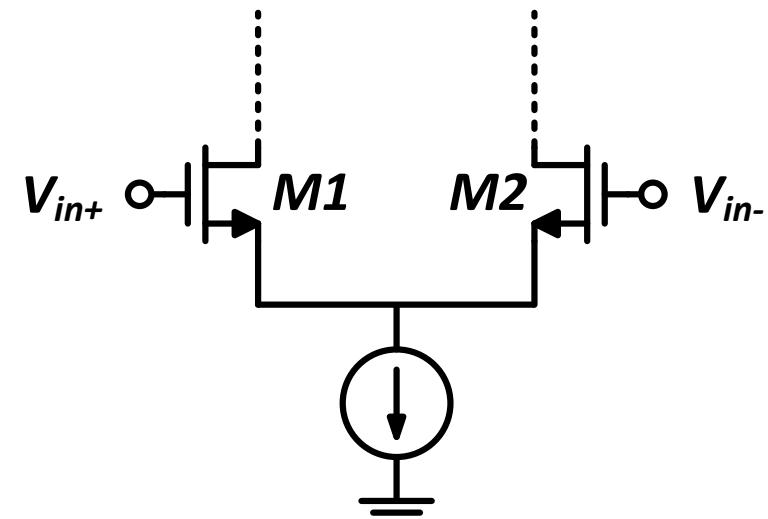
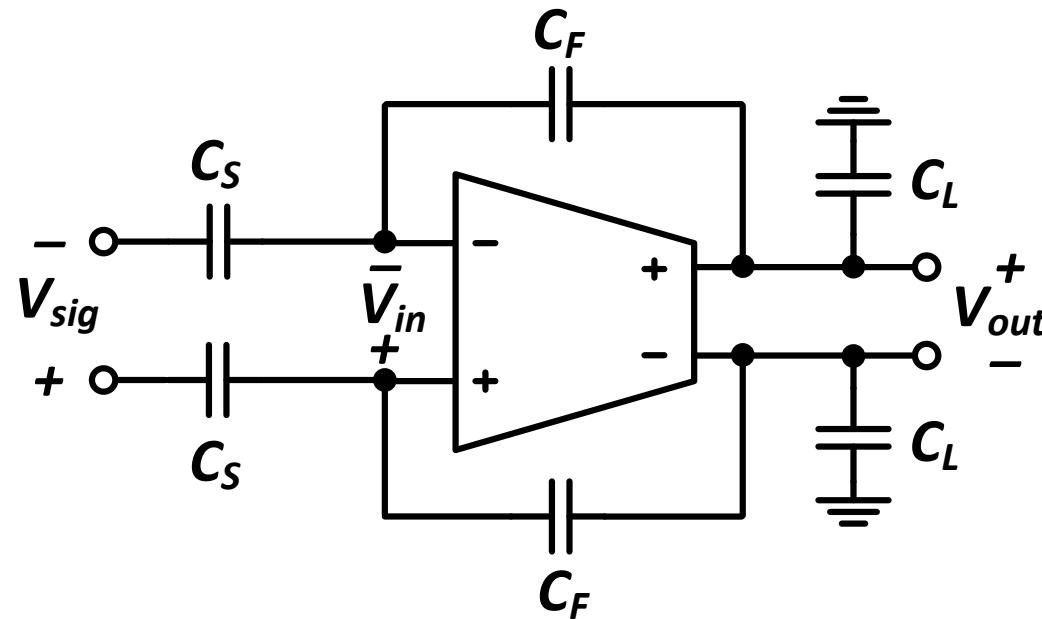
- High gain (high V_A)
 - Must have large VDsat_margin to be effective (beware of exceptions due to feedback)
- Less random mismatch
 - Longer L implies larger area (beware of exceptions due to non-uniform doping profile)
- Low flicker noise
 - Longer L implies larger area

Longer L: Beware of Exceptions

- What really matters is the DC loop gain, not the OTA open-loop gain

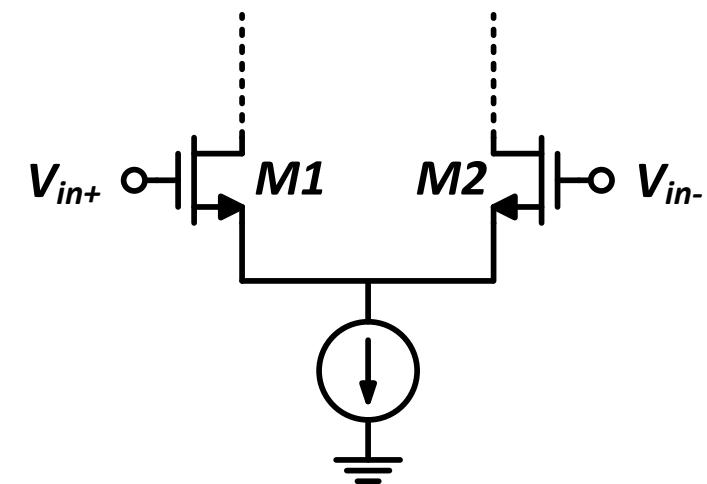
$$LG = \beta A_{OL} = \frac{C_F}{C_F + C_S + C_{in}} A_{OL}$$

- Increasing L of input pair may increase A_{OL} but will give an overall reduction of LG



W

- Choosing W is one of the most difficult tasks
- The choice of W is affected by
 - How much gm/ID do you want (inversion level: WI, MI, SI)?
 - How much L do you use?
 - How much ID do you force?
- The search-range of W can range from sub-1um to 1000um (laid-out as multi-fingers)
 - The meaningful search range depends on gm/ID (inversion level), L, and ID
- Assume you selected a specific W
 - Changing L changes the gm/ID (the TE)
 - Changing ID changes the gm/ID (the TE)

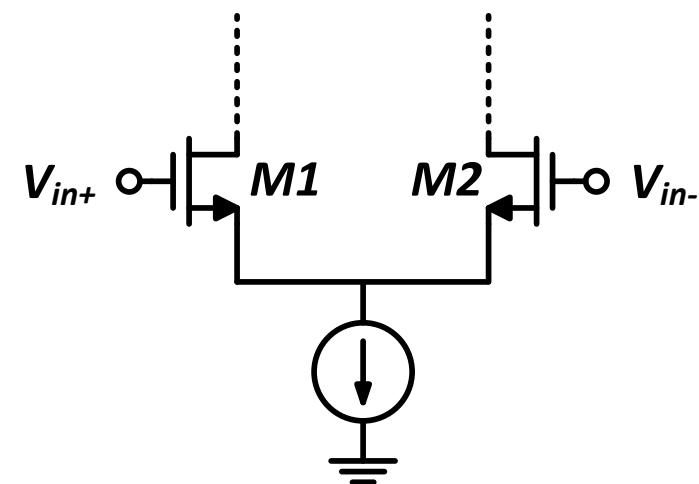


The Old Fix: Vov

- To solve this problem, designers used to replace W by Vov in the DOFs
- Vov used to give an indication for the TE (how much inversion do we have)
- Given ID, L, and Vov: They used to use the square law to calculate W

$$I_D = \frac{\mu_n C_{ox} W}{2L} V_{ov}^2$$

- This fix doesn't work any more
 - The square law and Vov are not accurate in SI
 - They are completely invalid in MI and WI
 - They are not related to circuit specs anymore
 - No direct relation to gain, speed, and noise

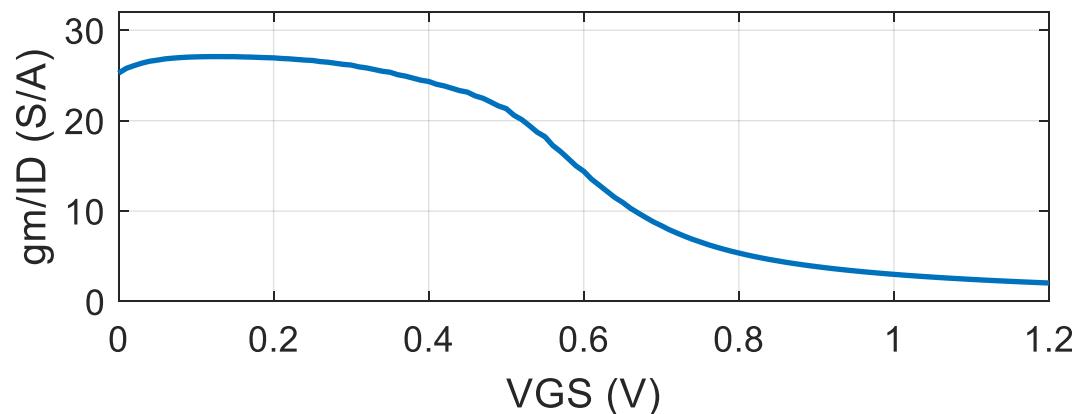


The New Fix: The gm/ID Design Methodology

- What we care most about is the gm/ID, i.e., the Transistor Efficiency (TE)
 - The gm/ID captures the relation between the basic function of the transistor (the transconductance) and the most valuable resource (the power consumption)
- Replace W by gm/ID in the DOFs
- “Orthogonal” control of TE!
- Think gm/ID!

Think gm/ID!

- The gm/ID is an “**orthogonal**” DOF to control the TE (and consequently the inversion level: WI, MI, SI)
 - When ID and/or L change: gm/ID (the TE) is kept unchanged
 - We simply lookup the new W that guarantees this
- The gm/ID is directly related to circuit specs
 - It defines gain, speed, and noise
- The search-range of gm/ID is limited
 - Typically: 5 to 25
 - The range of gm/ID values doesn't differ much
 - From one device to another
 - And from one technology to another



Think gm/ID!

Use small gm/ID if you want

- Strong-inversion (SI) biasing
- Small gm (for a given ID)
 - Devices whose gm do NOT contribute to gain (Ex: active loads)
- Small area
- Small capacitance
- High speed
- Large V_A (large r_o)
 - The gate has better control on channel (V_{DS} effect is less)

Use large gm/ID if you want

- Moderate inversion (MI) or weak-inversion (WI) biasing
- Large gm (for a given ID)
 - Devices whose gm do contribute to gain (Ex: input stage and cascode devices)
- High efficiency
 - Low power consumption (low ID) for a given speed or noise spec (gm spec)
- Less random mismatch
 - Large gm/ID implies larger W (larger area) (beware of exceptions due to non-uniform doping profile)
- Low flicker noise
 - Large gm/ID implies larger W (larger area)
- Large input range and/or output swing
 - Large gm/ID implies small V^*

Think gm/ID!

Use small gm/ID if you want

- Strong-inversion (SI) biasing
- Small gm (for a given ID)
 - Devices whose gm do NOT contribute to gain (Ex: active loads)
- Small area
- Small capacitance
- High speed
- Large V_A (large r_o)
 - The gate has better control on channel (V_{DS} effect is less)

Use large gm/ID if you want

- Moderate inversion (MI) or weak-inversion (WI) biasing
- Large gm (for a given ID)
 - Devices whose gm do contribute to gain (Ex: input stage and cascode devices)

➤ High efficiency

The best compromise is usually in MI

$$\frac{g_m}{I_D} \approx 10 \rightarrow 20$$

- Low flicker noise
 - Large gm/ID implies larger W (larger area)
- Large input range and/or output swing
 - Large gm/ID implies small V^*

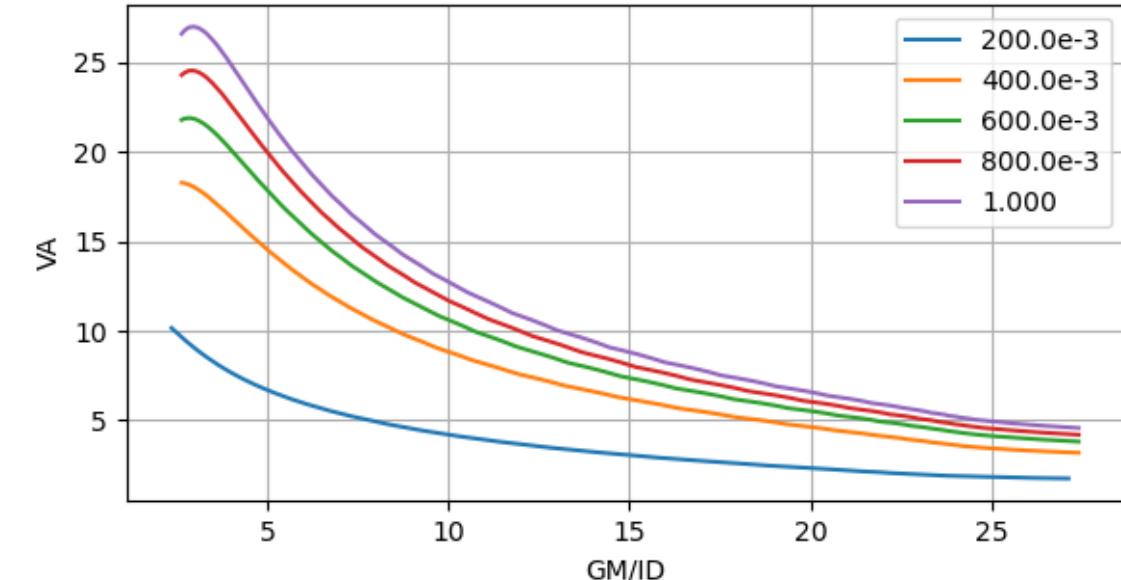
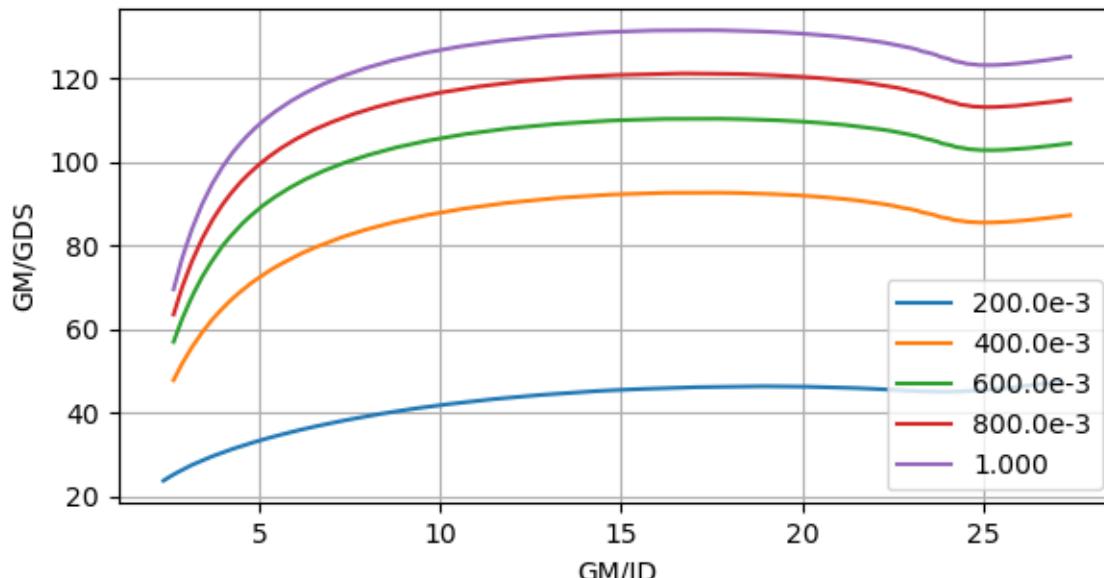
or a given speed or noise

per area) (beware of
drain-to-gate coupling profile)

gm/ID and Gain

$$g_m r_o = \frac{g_m}{I_D} \cdot V_A$$

- For high intrinsic gain go for high gm/ID
- But beware that V_A (and consequently r_o) decreases as you go in WI
 - The gate has less control in WI
 - The effect of VDS on ID increases

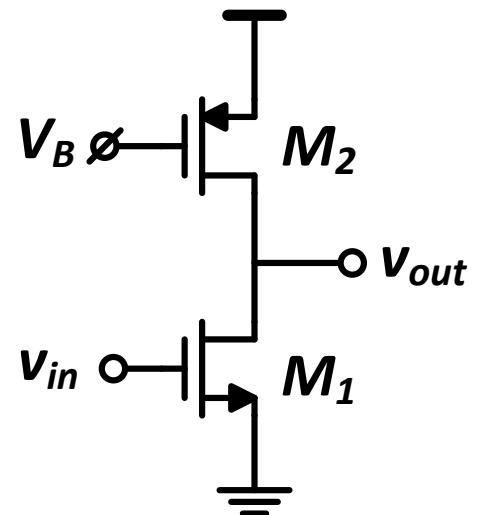


gm/ID and Gain

$$|A_v| = g_{m1}(r_{o1} || r_{o2}) = \frac{g_{m1}}{g_{ds1} + g_{ds2}} = \frac{(g_m/I_D)_1}{\frac{1}{V_{A1}} + \frac{1}{V_{A2}}}$$

- From gain perspective
 - A large gm/ID may be good for M1
 - But a small gm/ID is better for M2 (higher V_{A2})

- Generally, from gain perspective
 - Use large gm/ID for transistors whose g_m contribute to the gain
 - Ex: input stage and cascode devices
 - Use small gm/ID for transistors whose g_m do not contribute to gain
 - Ex: active loads

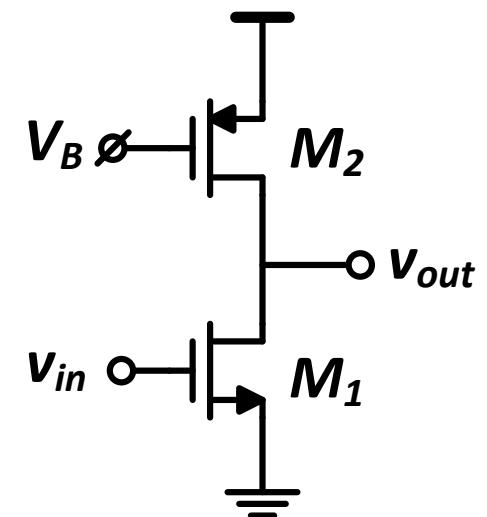


gm/ID and Thermal Noise

$$v_{n,in}^2(f) \approx \frac{4kT\gamma}{g_{m1}} \left(1 + \frac{g_{m2}}{g_{m1}} \right)$$

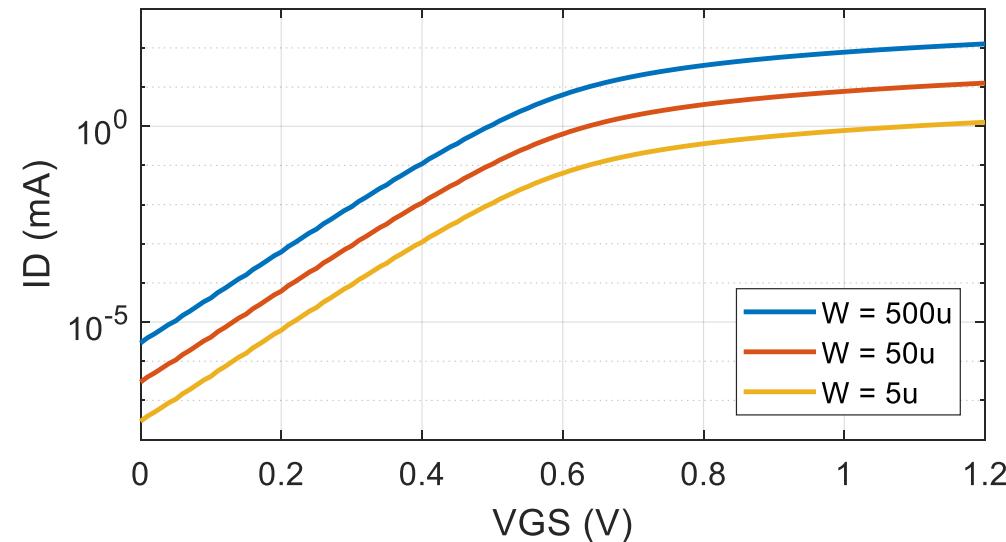
- From noise perspective
 - A large gm/ID is good for M1
 - But a small gm/ID is better for M2 (higher V_{A2})

- Generally, from noise perspective
 - Use large gm/ID for transistors whose g_m contribute to gain
 - Ex: input stage and cascode devices
 - Use small gm/Id for transistors whose g_m do not contribute to gain
 - Ex: active loads



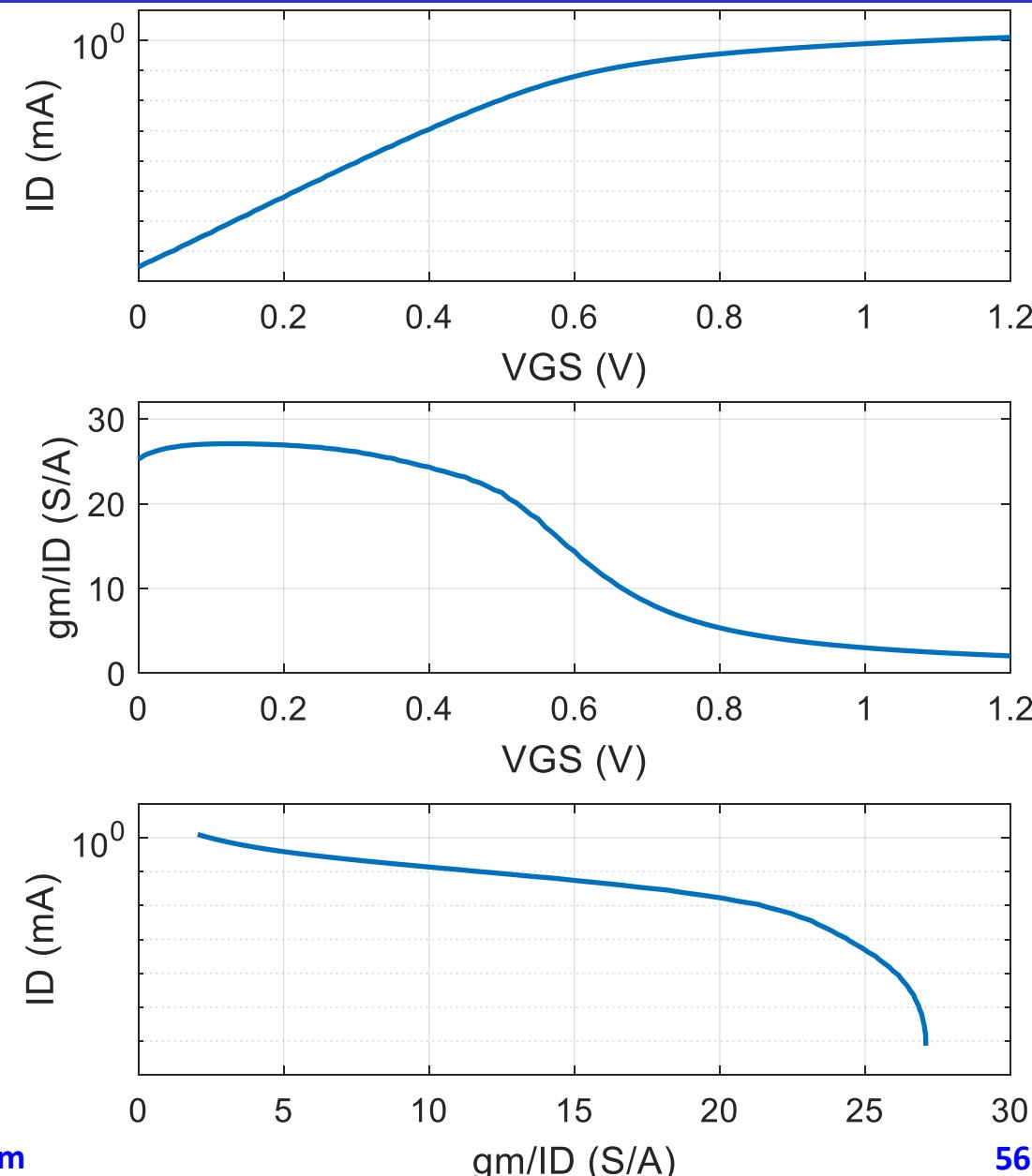
From gm/ID to W

- The problem is that you cannot plugin gm/ID in the simulator
 - Side note: you can directly plugin gm/ID in the Analog Designer's Toolbox (ADT) ☺
- The good news is that ID is always proportional to W: $I_D \propto W$
 - This holds for both long and short channel devices
 - This holds for all operating regions (WI, MI, SI)
 - Simply, the wider the street (the channel) the more cars (electrons) can pass
- The exception is narrow-width devices
 - But they are seldom used in analog as they will have excessive mismatch and excessive flicker noise



From gm/ID to W

- Assume a reference device with Width = W
- For a given L, there is one-to-one correspondence between VGS and ID
- And there is one-to-one correspondence between gm/ID and VGS
 - Points to the left of the max gm/ID are discarded
- Thus, there is one-to-one correspondence between gm/ID and ID
- Similarly, we can plot any other parameter vs gm/ID



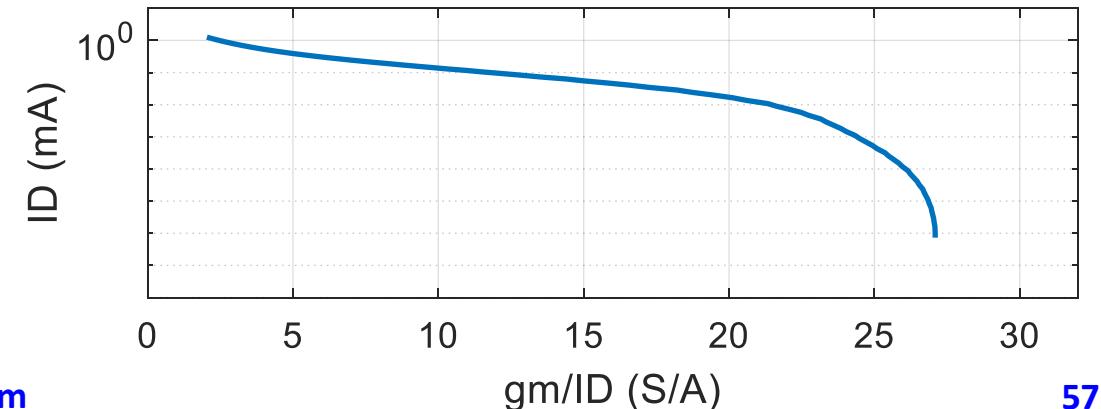
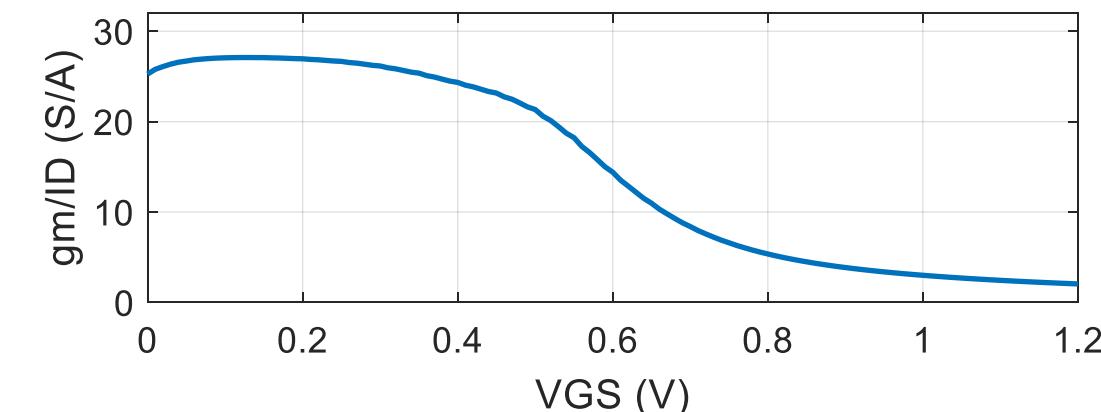
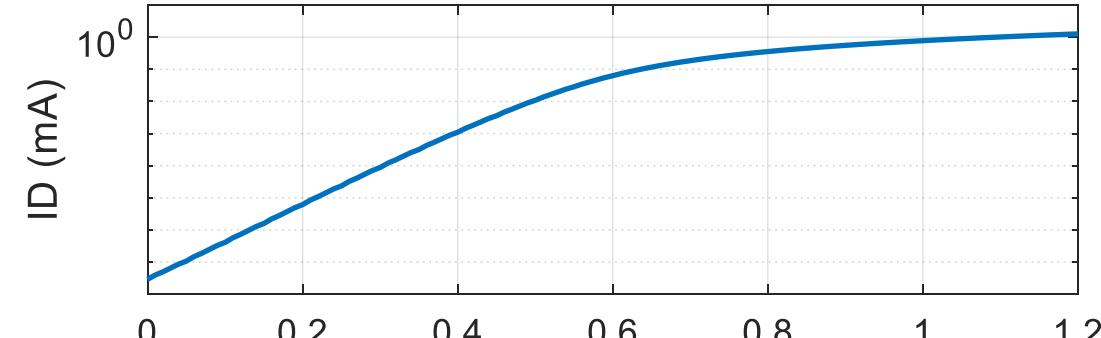
From gm/ID to W

$$I_D \propto W$$

- Apply cross multiplication

Ref Device	ID (from chart or look-up table)	W (reference device width)
Design Problem	I_{Dx} (defined in problem DOFs)	$W_x = ?$

$$W_x = W \times \frac{I_{Dx}}{I_D}$$



Recapping MOSFET DOFs

Original	The Old-School	The gm/ID Methodology
W	Vov (square law)	gm/ID (use charts or LUTs to get W)
L	L (get a rough estimate for $V_A = 1/\lambda$)	L (use charts or LUTs)
VGS	ID (current mirror biasing)	ID (current mirror biasing)
VDS	$V_{DS} = V_{ov} + V_{Dsat_margin}$ (get a rough estimate for V_{Dsat_margin})	$V_{DS} = \text{VDsat} + V_{Dsat_margin}$ (taken into account by using charts or LUTs)
VSB	Forced by topology (use simple model or ignore)	Forced by topology (taken into account by using charts or LUTs)

Outline

- Why gm/ID?
- The BJT Story
- The MOSFET Story
- The MOSFET Design Problem
- **The Look-up Tables (LUTs)**
- Design Examples

Implications of $I_D \propto W$

- Almost all MOSFET parameters are also proportional to W (given other DOFs are constant)
 - gm, gds, gmb
 - cgs, cgd, cgb, csb, cdb
 - Also drain-current thermal noise density (STH) and flicker noise density (SFL)!
- Result #1: Store these parameters for the reference device
 - Calculate the parameters of any other device by cross-multiplication!

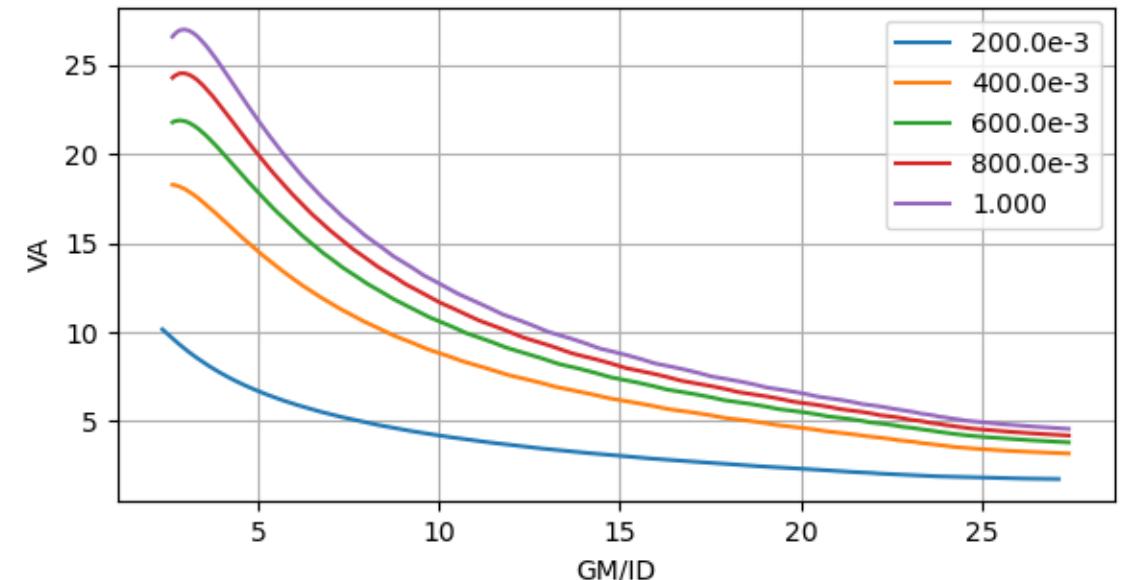
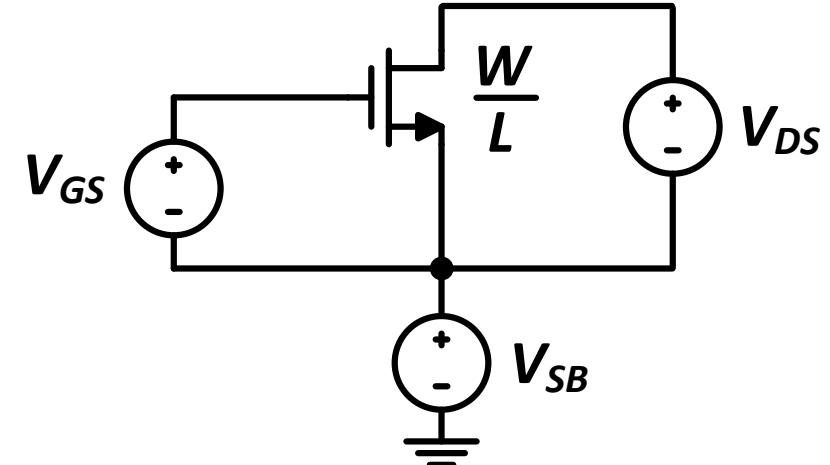
Ref Device	ID	W	gm	...
Design Problem	IDx	Wx	gmx	...

- Result #2: Ratios of these parameters are width independent!

$$\frac{g_m}{I_D}, f_T = \frac{g_m}{2\pi C_{gg}}, \frac{g_m}{W}, g_m r_o = \frac{g_m}{g_{ds}}, V_A = \frac{I_D}{g_{ds}}, \dots$$

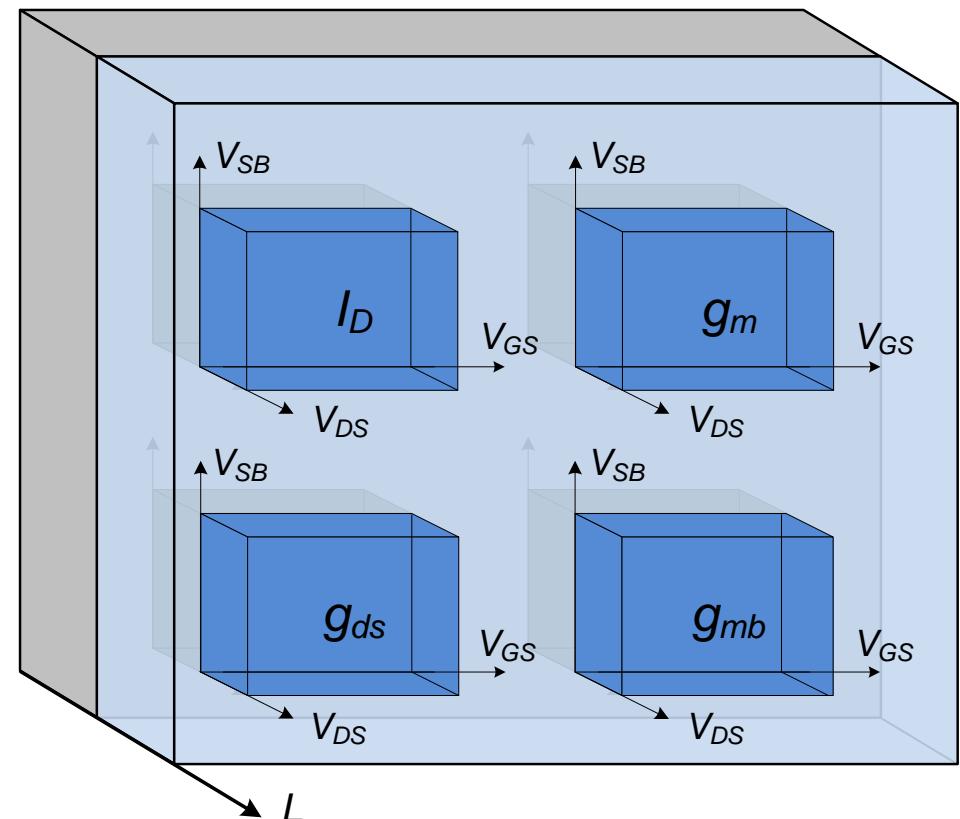
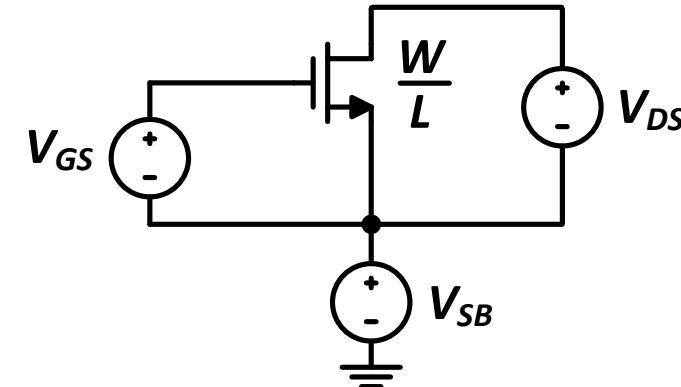
Building The Design Charts

- MOSFET is a function of five variables
- Three voltages
 - **VGS: Sweep (primary variable)**
 - VDS: Set to fixed value
 - VSB: Set to fixed value
- Two sizing parameters
 - **L: Step (secondary variable)**
 - **W: Set to a reference value (e.g., 10um)**
- Run DC and noise sweeps and store large signal and small signal parameters in 2D arrays
- Plot in parametric charts
 - X-axis is VGS or gm/ID (or any ratio)
 - L is a parameter



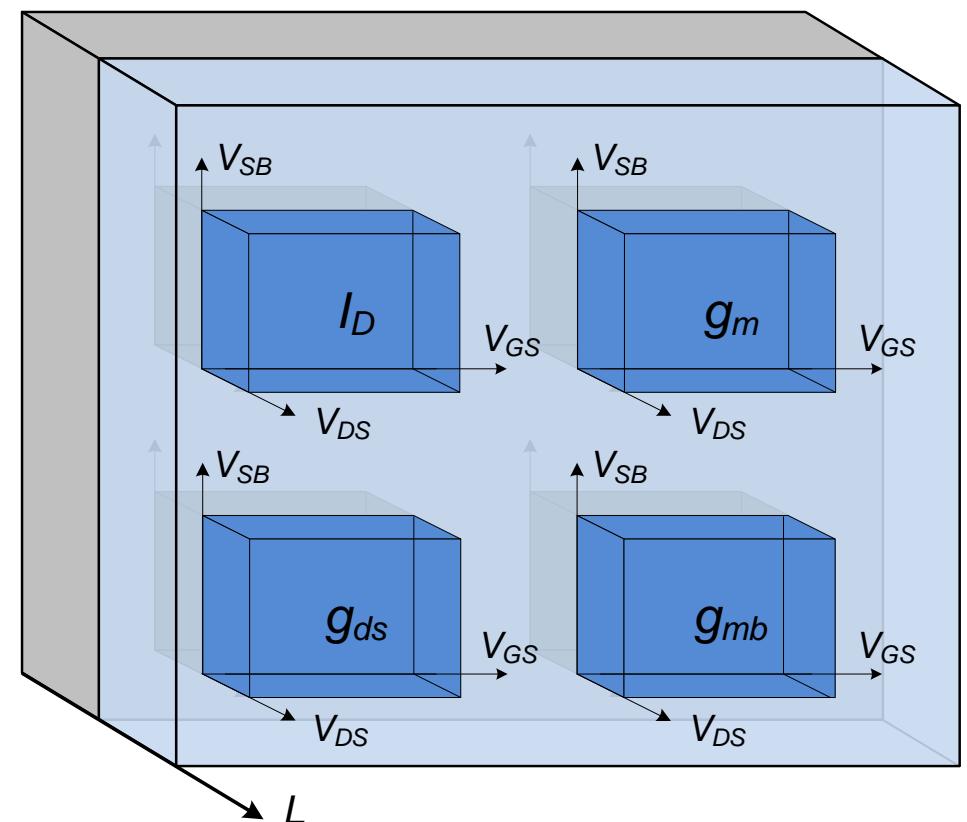
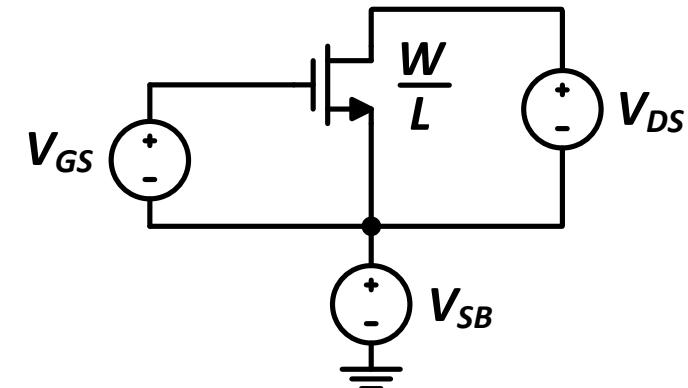
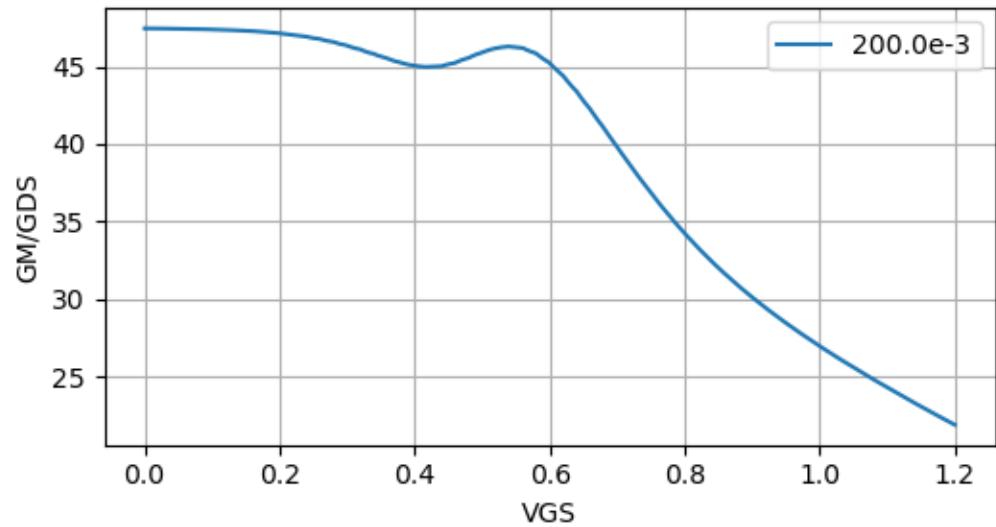
Building The Lookup Table (LUT)

- MOSFET is a function of five variables
- Three voltages: VGS,
 - VGS: Sweep (primary variable)
 - VDS: Step (parametric sweep)
 - VSB: Step (parametric sweep)
- Two sizing parameters
 - L: Sweep (secondary variable)
 - W: Set to a reference value (e.g., 10um)
- Run DC and noise sweeps and store large and small signal parameters in 4D arrays
 - 4D LUT for every parameter



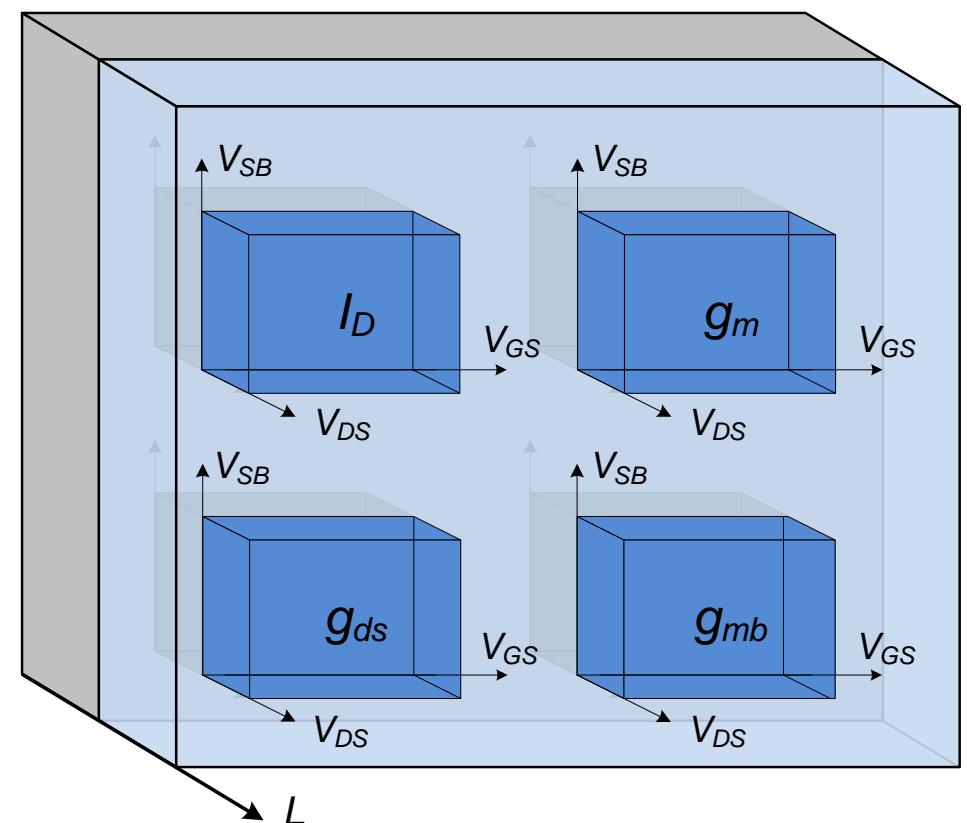
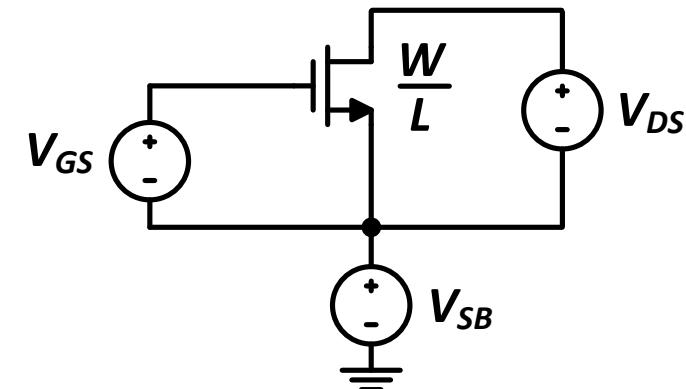
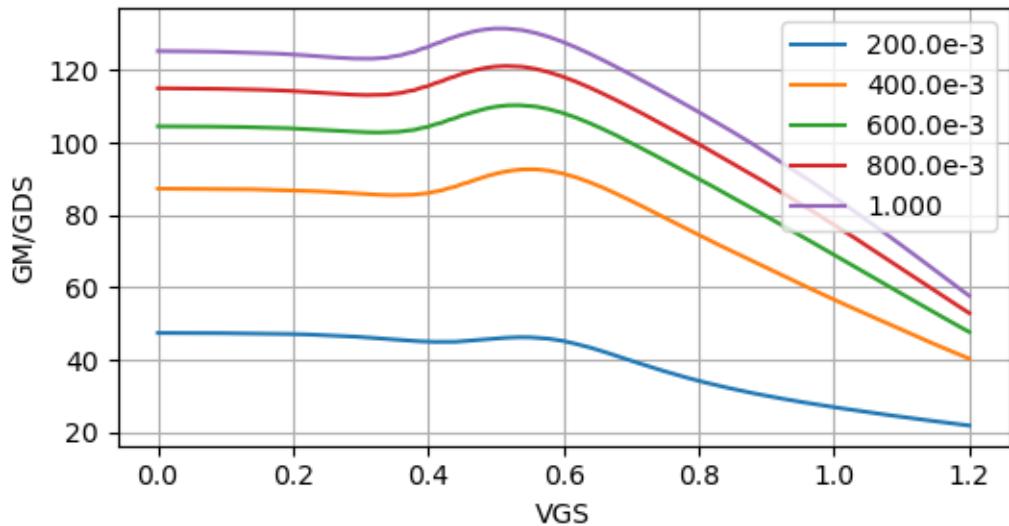
Extracting Design Charts

- 4D LUT for every parameter
- Select specific VDS and VSB to plot 2D parametric charts
- Ex: gm/gds vs VGS @ VSB = 0 V and VDS = 0.9 V



Extracting Design Charts

- 4D LUT for every parameter
- Select specific VDS and VSB to plot 2D parametric charts
- Ex: gm/gds vs VGS @ VSB = 0 V and VDS = 0.9 V
 - Repeat at several values of L





General Settings

Simulator:	Spectre	?
Simulation Command:	spectre	?
Netlist Path:	C:/hesham/demo/ee214b_netlist.scs	?
Save Path:	C:/hesham/demo/	?
Prefix Name:	ee214e	?

Device Characterization Parameters

MOSFET	BJT	
Temperature (°C):	27	?
Ref Total Width (um):	10	?
Ref No. of Fingers:	1	?
Length (um):	0.18:0.02:0.5, 0.6:0.1:1, 1.2:0.2:2	?
VGS:	0:20m:1.2	?
VDS:	25m:25m:1.2	?
VSB:	0:50m:1.2	?
Output Variables:	ID, GM, GMB, GDS, VTH, VDSAT, CGS, CGD, CGB, CDB, CSB, SFL, STH	?

Generate LUTs

Quick Plot

Netlist Editor Simulation Log

```

1 // sample netlist for spectre
2
3 simulator lang=spectre
4 global 0
5 parameters WN LN WP LP
6 include "/mnt/hgfs/vmware_share/ee214b.sp"
7
8
9 M0 (net1 net3 net4 net2) nch w=WN l=LN as=0.64u*WN
ad=0.64u*WN \
ps=2*(0.64u+WN) pd=2*(0.64u+WN)
10
11
12 M1 (net5 net7 net8 net6) pch w=WP l=LP as=0.64u*WP
ad=0.64u*WP \
ps=2*(0.64u+WP) pd=2*(0.64u+WP)
13
14
15 simulatorOptions options reltol=1e-3 vabstol=1e-7
iabstol=1e-12 temp=27 \
tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1
maxnotes=5 maxwarns=5 \
digits=5 cols=80 pivrel=1e-3 sensfile="../psf/
sens.output" \
checklimitdest=psf
16
17
18
19
20 modelParameter info what=models where=rawfile
element info what=inst where=rawfile
21 outputParameter info what=output where=rawfile
22 designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
23 subckts info what=subckts where=rawfile
24 saveOptions options save=allpub
25
26
27

```

Save

Save As

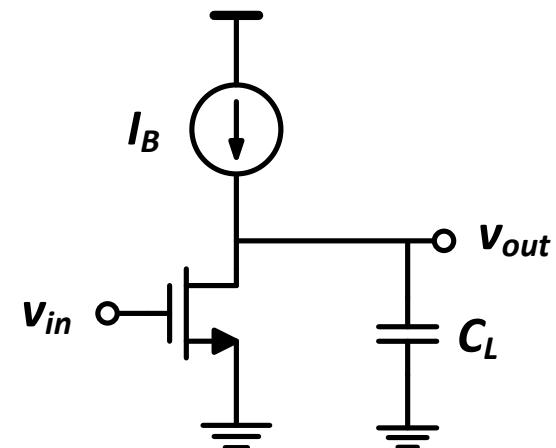
Revert

Outline

- Why gm/ID?
- The BJT Story
- The MOSFET Story
- The MOSFET Design Problem
- The Look-up Tables (LUTs)
- **Design Examples**
 - **Design Example #1**
 - Design Example #2

Design Example #1

- Four DOFs (four unknowns): I_B , gm/ID , L , VDS
- Only two equations (DC gain and GBW)
- We need to assume two DOFs
 - Assume $VDS = VDD/2$
 - Assume a reasonable I_B (if not given as a spec)
- How to get a reasonable estimate for current?
- How to know if a current spec makes sense?



Spec	Constraint
DC Gain	50
GBW	200 MHz
CL	1 pF

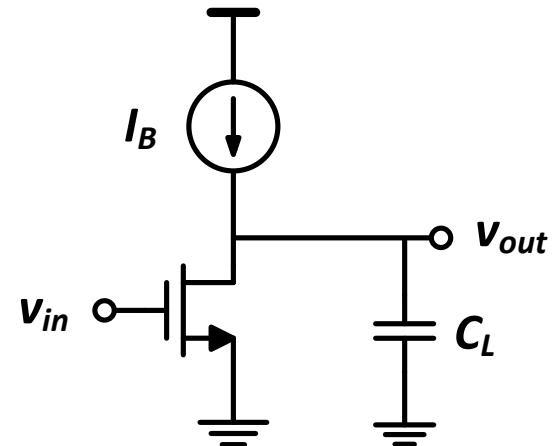
DOF	Value
I_B	?
gm/ID	?
L	?

Think gm/ID!

- How to get a reasonable estimate for current?
- How to know if a current spec makes sense?

- Remember:
 - g_m controls speed
 - We pay current to buy g_m

- Start by getting an estimate for g_m
 - gm/ID has a well-known reasonable range
 - You can now get the reasonable current range



Spec	Constraint
DC Gain	50
GBW	200 MHz
CL	1 pF

DOF	Value
IB	?
gm/ID	?
L	?

gm Spec and Current Range

$$GBW = f_u = G_m R_{out} \times \frac{1}{2\pi R_{out} C_{out}} \approx \frac{g_m}{2\pi C_L}$$

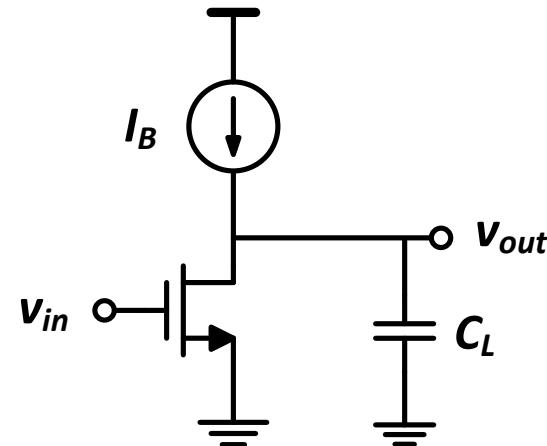
$$g_m = 2\pi C_L \times f_u = 1.257 \text{ mS}$$

□ Let

$$\frac{g_m}{I_D} = 5 \text{ (SI)} \rightarrow 25 \text{ (WI)}$$

□ Then

$$I_D \approx 50 \mu A \text{ (WI)} \rightarrow 250 \mu A \text{ (SI)}$$



Spec	Constraint
DC Gain	50
GBW	200 MHz
CL	1 pF

DOF	Value
IB	?
gm/ID	?
L	?

Pick gm/ID

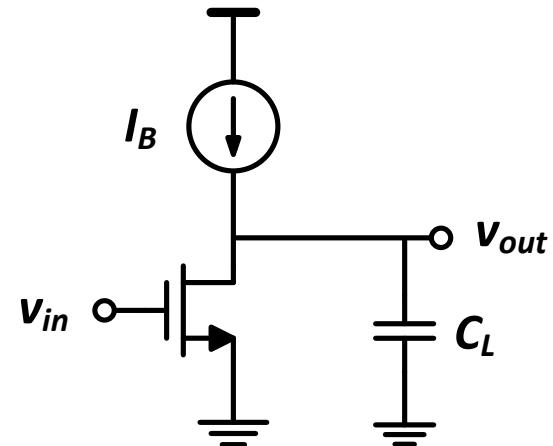
□ Let

$$\frac{g_m}{I_D} = 15 \text{ (MI)}$$

□ Then

$$I_D \approx 83.8 \mu A \rightarrow 80 \mu A$$

$$\frac{g_m}{I_D} = \frac{1.257 m}{0.08 m} = 15.71$$



Spec	Constraint
DC Gain	50
GBW	200 MHz
CL	1 pF

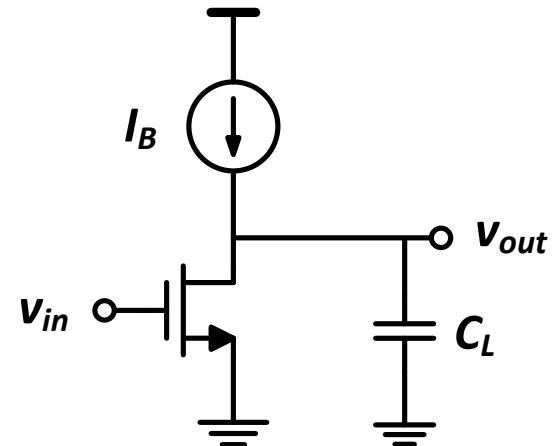
DOF	Value
IB	80 uA
gm/ID	15.71
L	?

Pick L

$$|A_v| = g_m r_o = \frac{g_m}{g_{ds}}$$

$$|A_v| = \frac{g_m}{I_D} \cdot I_D r_o = \frac{g_m}{I_D} \cdot V_A$$

- The higher the L the higher the V_A
- You may expect $|A_v|$ vs gm/ID to be a straight line with slope = V_A
- But V_A depends on gm/ID
 - The design charts take care of all dependencies

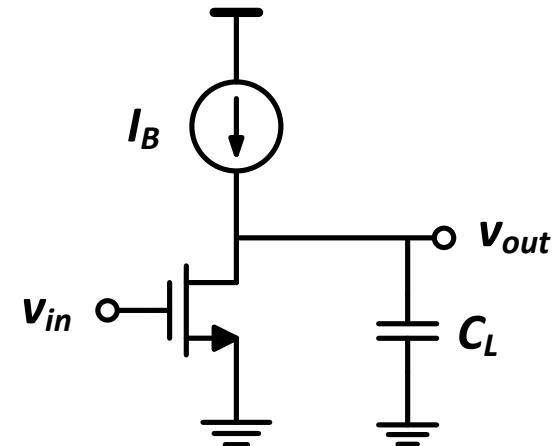
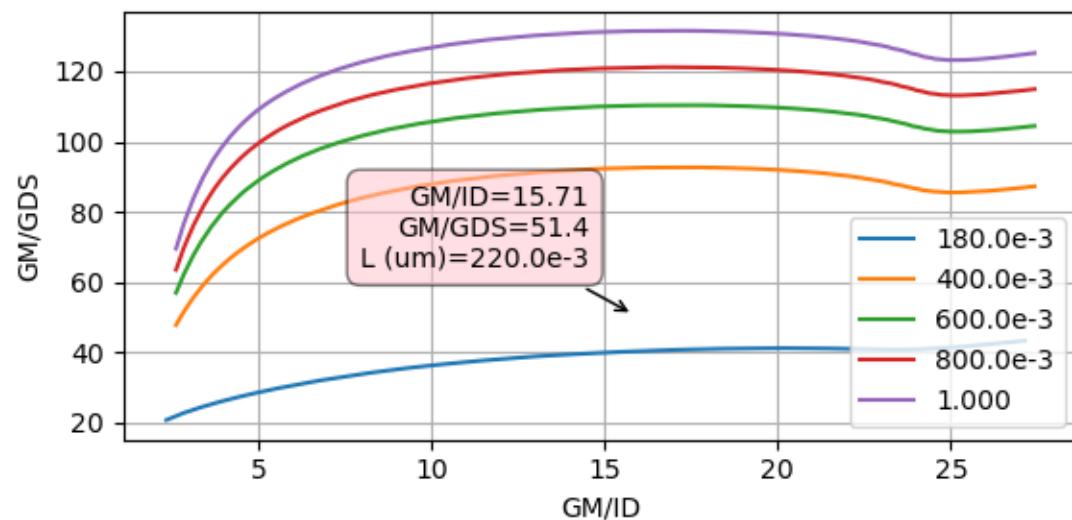


Spec	Constraint
DC Gain	50
GBW	200 MHz
CL	1 pF

DOF	Value
IB	80 uA
gm/ID	15.71
L	?

Pick L

$$|A_v| = g_m r_o = \frac{g_m}{g_{ds}} > 50$$



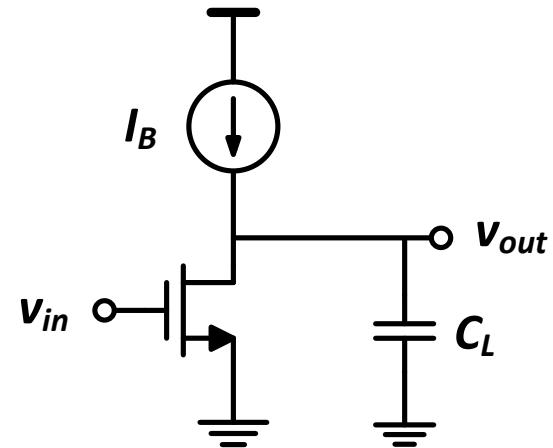
Spec	Constraint
DC Gain	50
GBW	200 MHz
CL	1 pF

DOF	Value
IB	80 uA
gm/ID	15.71
L	0.22 um

Lookup W

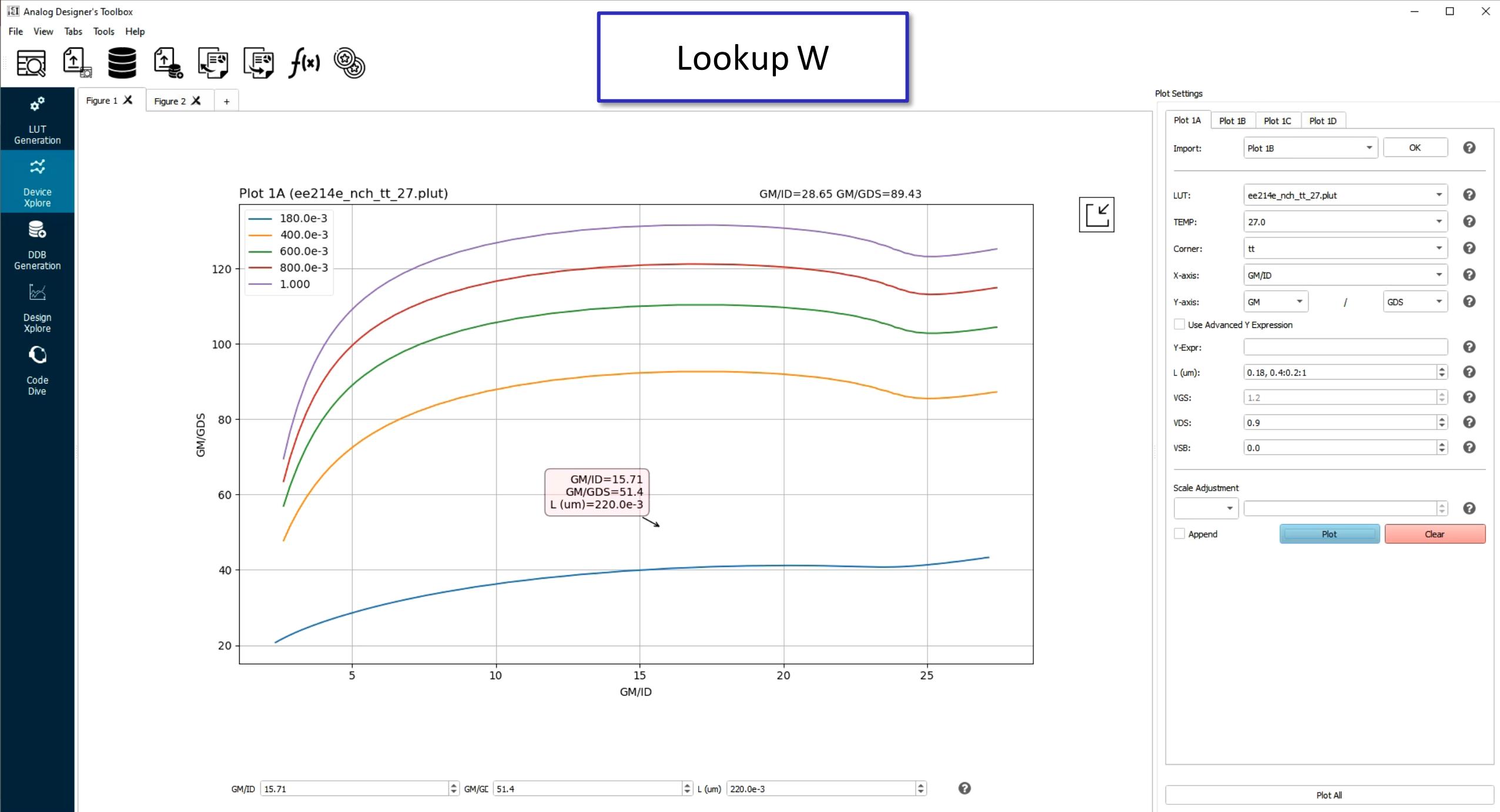
LUT	ID	W
Design Problem	Idx	Wx

$$W_x = W \times \frac{I_{Dx}}{I_D} = W \times \frac{80 \mu A}{I_D}$$



Spec	Constraint
DC Gain	50
GBW	200 MHz
CL	1 pF

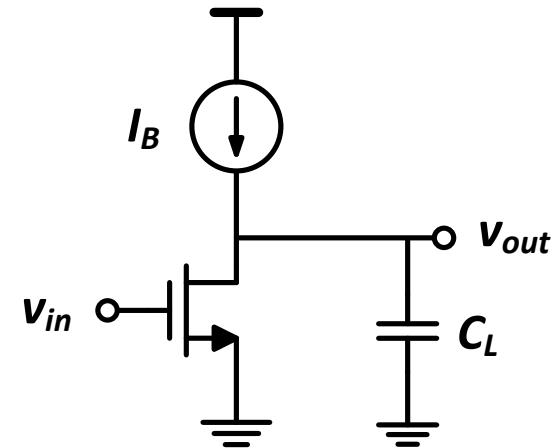
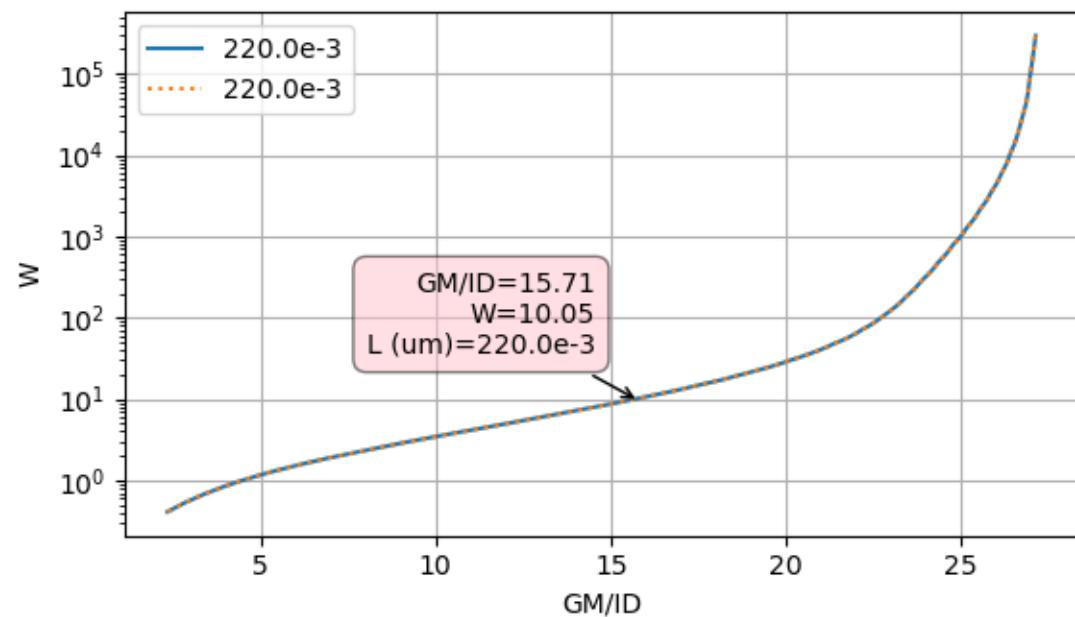
DOF	Value
IB	80 uA
gm/ID	15.71
L	0.22 um



Lookup W

LUT	ID	W
Design Problem	Idx	Wx

$$W_x = W \times \frac{I_{Dx}}{I_D} = W \times \frac{80 \mu A}{I_D} = 10.05 \mu m$$

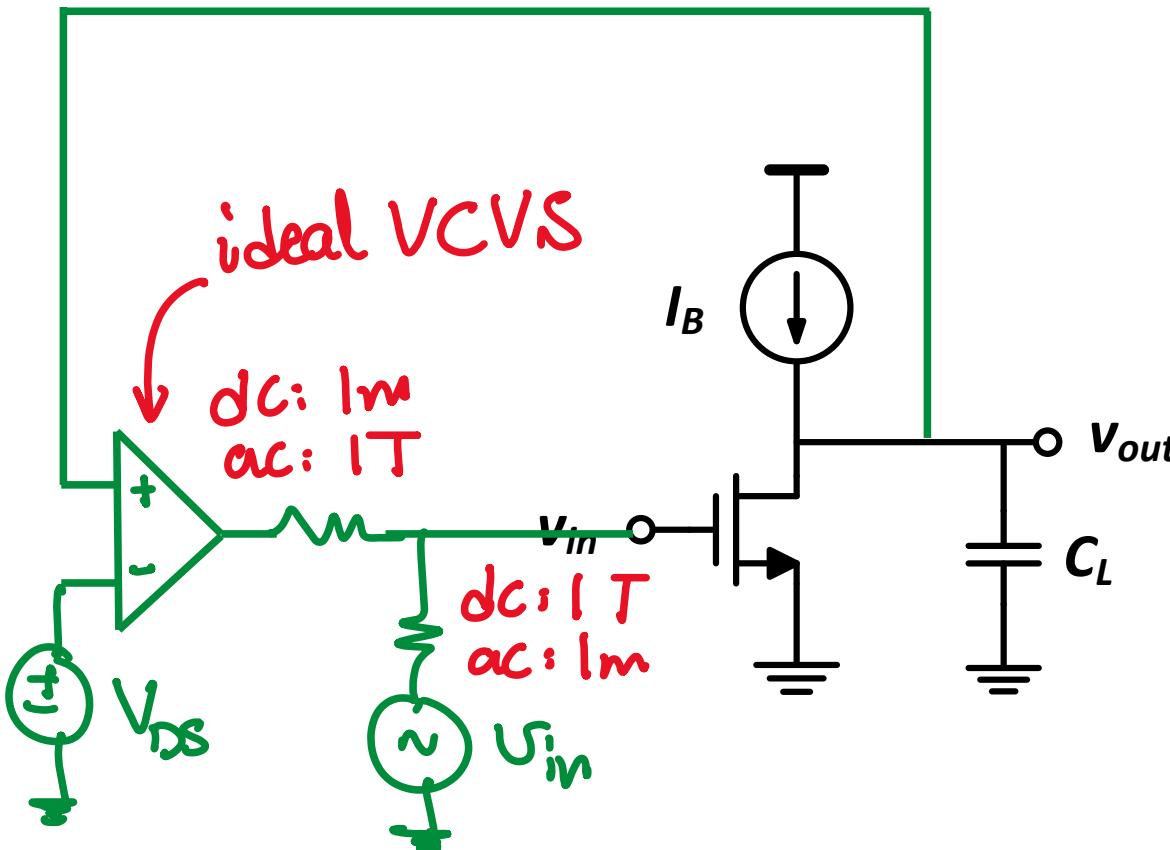


Spec	Constraint
DC Gain	50
GBW	200 MHz
CL	1 pF

DOF	Value
IB	80 uA
gm/ID	15.71
L	0.22 um

Results: Testbench #1

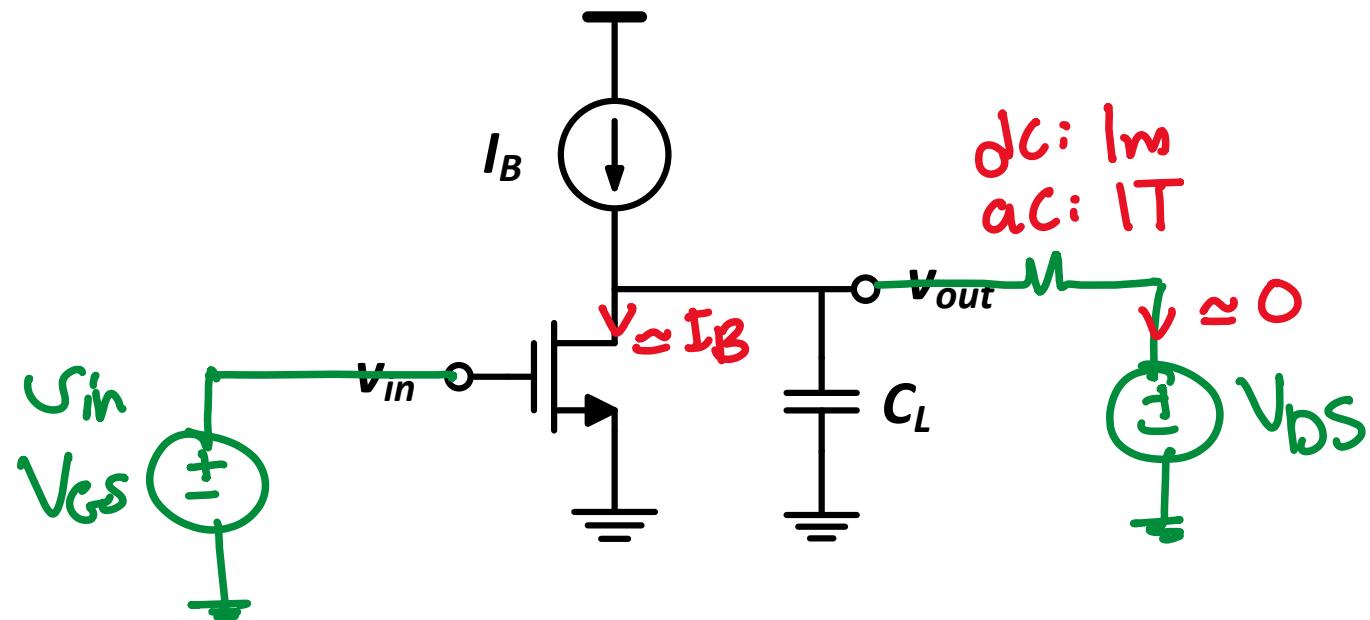
- How to set the high impedance node?

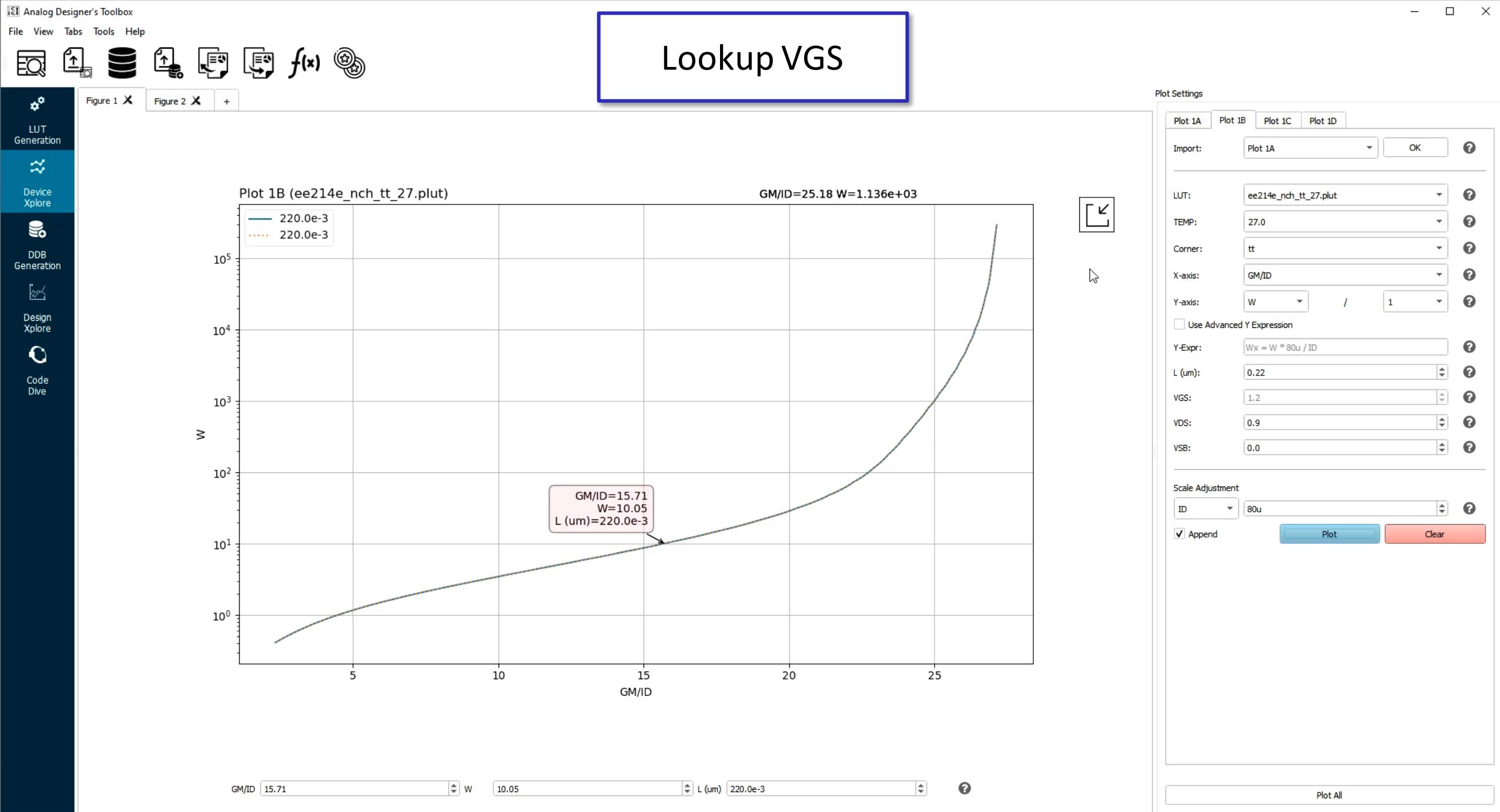


Spec	ADT	Simulation
DC Gain	51.4	51.44
GBW	200 MHz	196.8 MHz

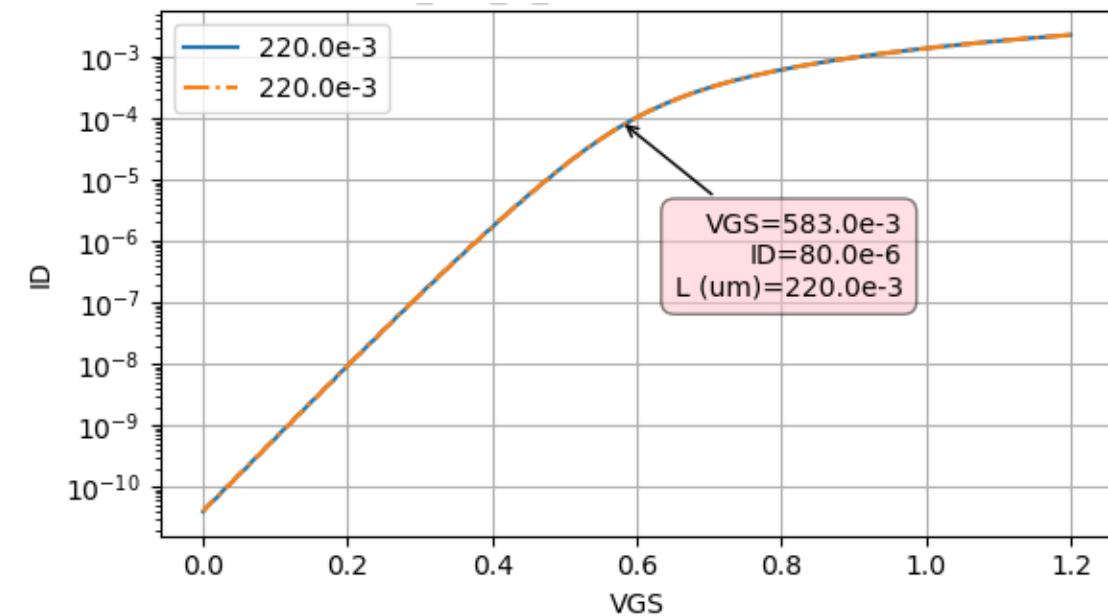
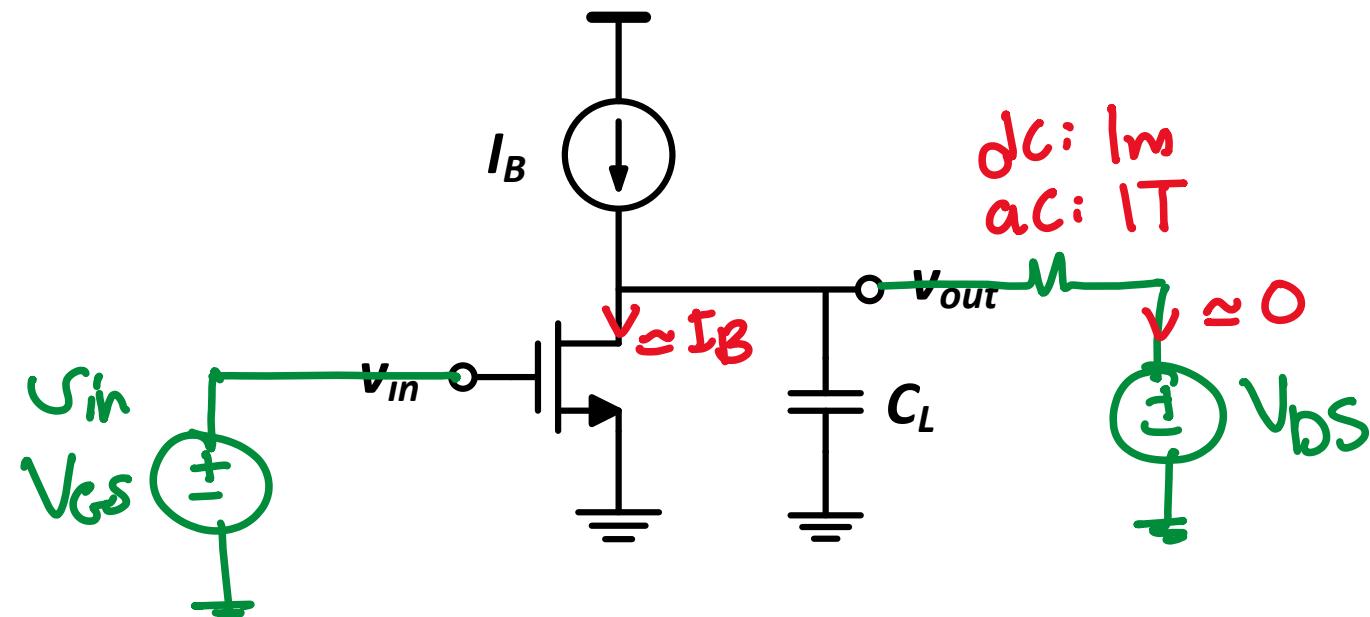
Testbench #2

- How to set the high impedance node?
- But need accurate value of VGS: Look-up VGS





Results: Testbench #2



Spec	ADT	Simulation
DC Gain	51.4	51.44
GBW	200 MHz	196.3 MHz

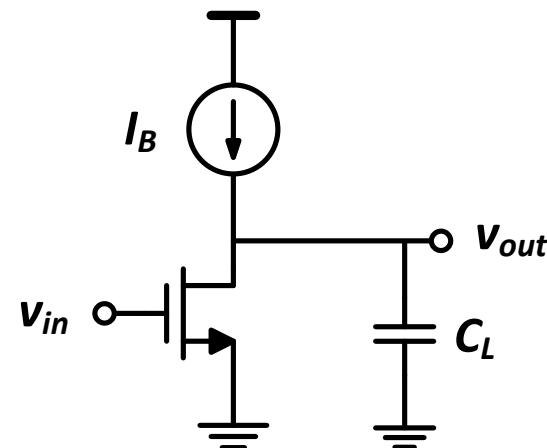
gm Spec Revisited

$$GBW = f_u \approx \frac{g_m}{2\pi(C_L + C_{dd})}$$

$$g_m = 2\pi(1p + C_{dd}) \times 200M = ?$$

- Assuming the same current

- Need higher gm/ID
- But higher gm/ID means larger W and larger C_{dd}
- Need help from ADT!



Spec	Constraint
DC Gain	50
GBW	200 MHz
CL	1 pF

DOF	Value
IB	80 uA
gm/ID	?
L	0.22 um

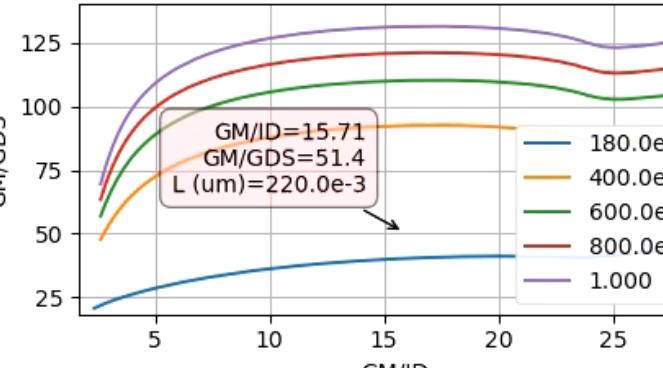
LUT
GenerationDevice
XploreDDB
GenerationDesign
XploreCode
Dive

Revisiting gm/ID

Figure 1 X

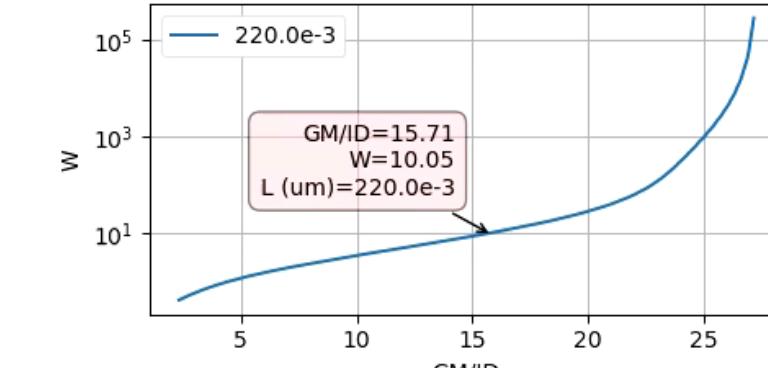
Figure 2 X

Plot 1A (ee214e_nch_tt_27.plut)



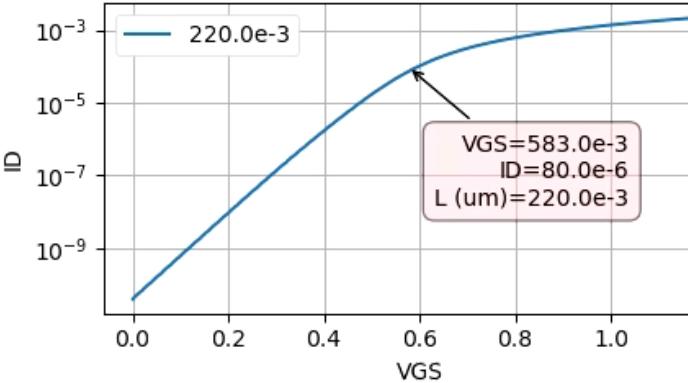
GM/ID 15.71 GM/GD 51.4 L (um) 0.22

Plot 1B (ee214e_nch_tt_27.plut)

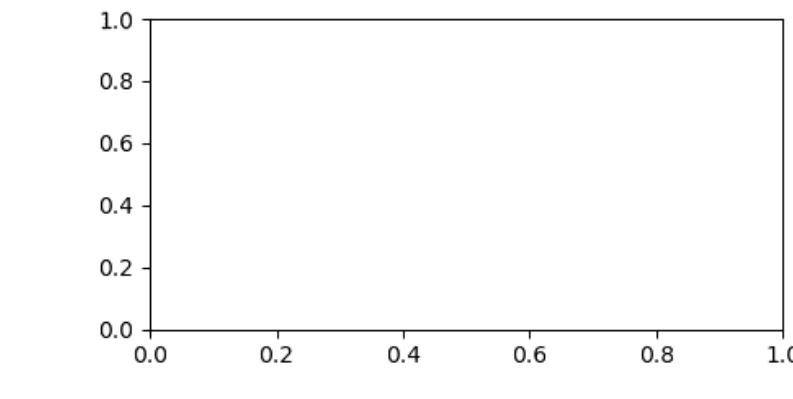


GM/ID 15.71 W 10.05 L (um) 220.0e-3

Plot 1C (ee214e_nch_tt_27.plut)



VGS 583.0e-3 ID 80u L (um) 220.0e-3



Plot Settings

Plot 1A Plot 1B Plot 1C Plot 1D

Import: Plot 1A OK ?

LUT: ee214e_nch_tt_27.plut ?

TEMP: 27.0 ?

Corner: tt ?

X-axis: GM/ID ?

Y-axis: ID / 1 ?

 Use Advanced Y ExpressionY-Expr: $GBW = GM / ((1p + CDD) * 2 * \pi * 1e6)$?

L (um): 0.18, 0.4:0.2:1 ?

VGS: 1.2 ?

VDS: 0.9 ?

VSB: 0.0 ?

Scale Adjustment

ID 80u ?

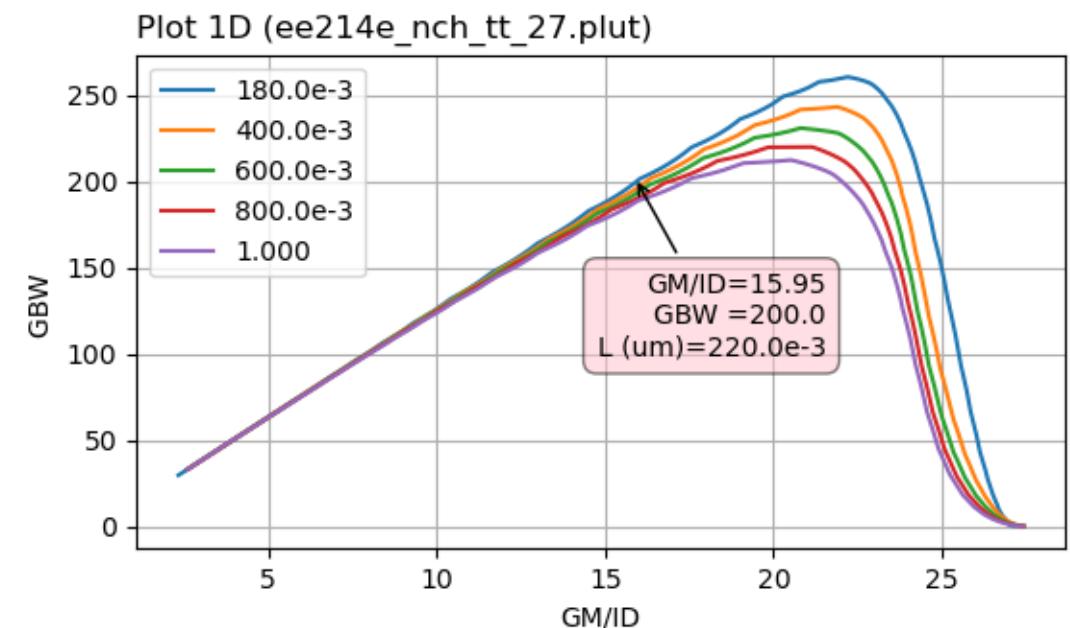
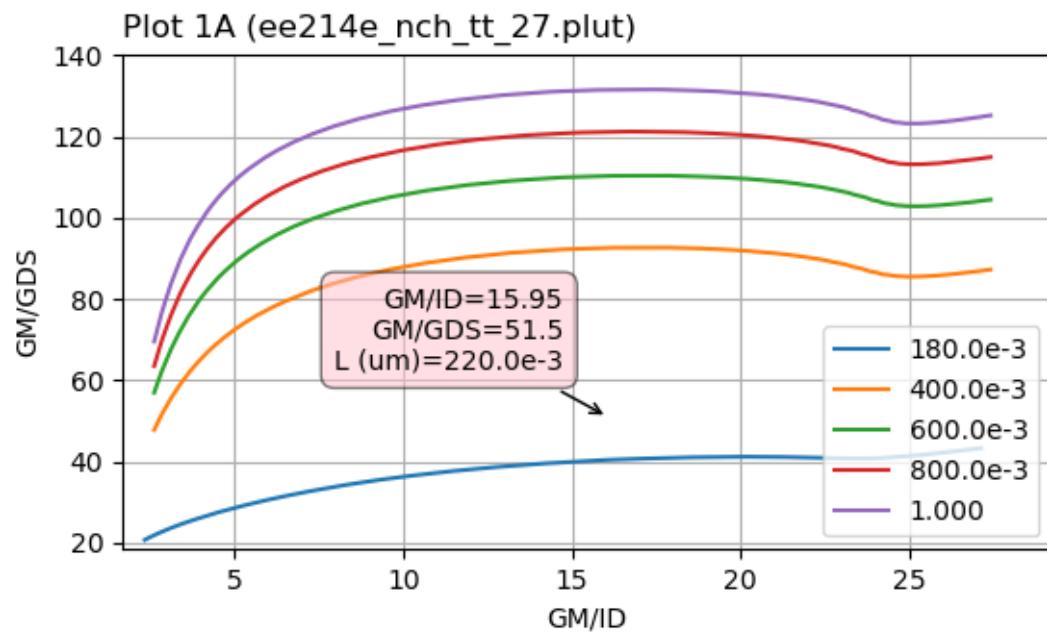
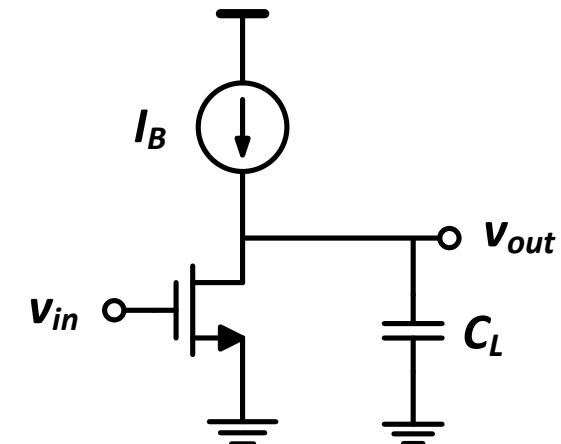
 Append Plot Clear ?

Plot All

Final Design

DOF	Value
IB	80 μ A
gm/ID	15.95
L	0.22 μ m

Spec	ADT	Simulation
DC Gain	51.5	51.53
GBW	200 MHz	199.8 MHz



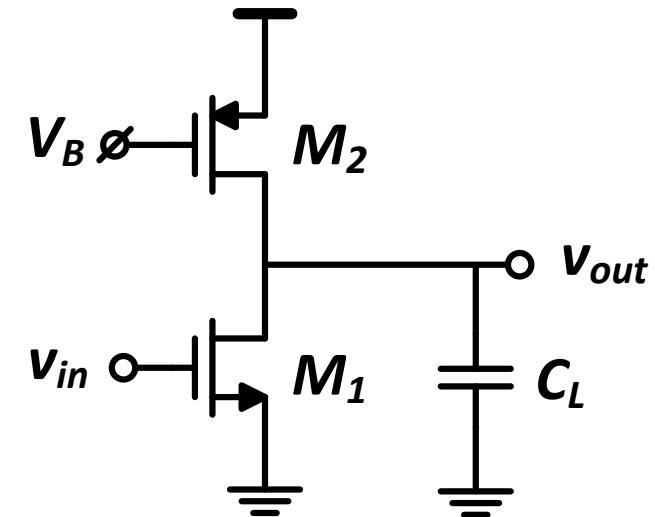
Outline

- Why gm/ID?
- The BJT Story
- The MOSFET Story
- The MOSFET Design Problem
- The Look-up Tables (LUTs)
- **Design Examples**
 - Design Example #1
 - **Design Example #2**

Design Example #2

Spec	Constraint
DC Gain	50
GBW	200 MHz
IB	< 100 uA
ΣW^*L	< 200 um ²
CL	1 pF

DOF	Value
IB	?
M1(gm/ID)	?
M1(L)	?
M2(gm/ID)	?
M2(L)	?



- Use relatively short L and relatively large gm/ID for M1
- Use relatively long L and relatively small gm/ID for M2
- If we start with the previous design as a reference point for M1
 - We will need higher M1(L) to compensate for r_{o2}
 - We will need higher M1(gm/ID) to compensate for added parasitics



Design DB Generation

Design Class: Voltage Amplifier

Search by Desi...



Show/Hide Columns



	Design ID	No. of Stages	FB Type	FB Network 1	FB Network 2	Input Signal 1	Output Signal 1	Input Type 1	Topology 1	Load 1	Tail Bias 1	Input Signal 2	Output Signal 2	Input Type 2
1	A010001	Single-Stage	Open-loop	None	None	Single-Ended	Single-Ended	NMOS	CS	Resistive	Ground	N/A	N/A	N/A
2	A010002	Single-Stage	Open-loop	None	None	Single-Ended	Single-Ended	NMOS	CS	Simple Mirror	Ground	N/A	N/A	N/A
3	A010003	Single-Stage	Open-loop	None	None	Diffrerential	Single-Ended	NMOS	CS	Simple Mirror	Simple Mirror	N/A	N/A	N/A
4	A010004	Single-Stage	Open-loop	None	None	Diffrerential	Diffrerential	PMOS(B)	Folded	Wide-Swing Mirror	Simple Mirror	N/A	N/A	N/A
5	A010005	Two-Stage	Open-loop	None	None	Single-Ended	Diffrerential	NMOS	CS	Simple Mirror	Simple Mirror	Single-Ended	Single-Ended	PMOS
6	A010006	Single-Stage	Open-loop	None	None	Diffrerential	Diffrerential	NMOS	Telescopic	Wide-Swing Mirror	Simple Mirror	N/A	N/A	N/A

Circuit Parameters

min	max

Generate

```
[LUT] ee214e_pch_tt_27.plut is removed.
[LUT] Loading ..
[LUT] ee214e_nch_tt_27.plut is loaded.
[LUT] ee214e_pch_tt_27.plut is loaded.
```

File View Tabs Tools Help

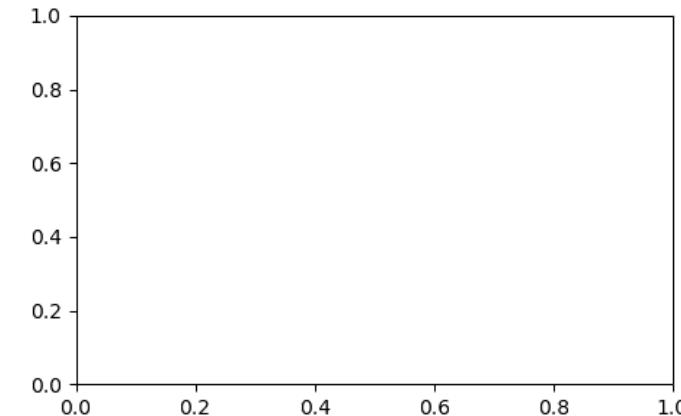
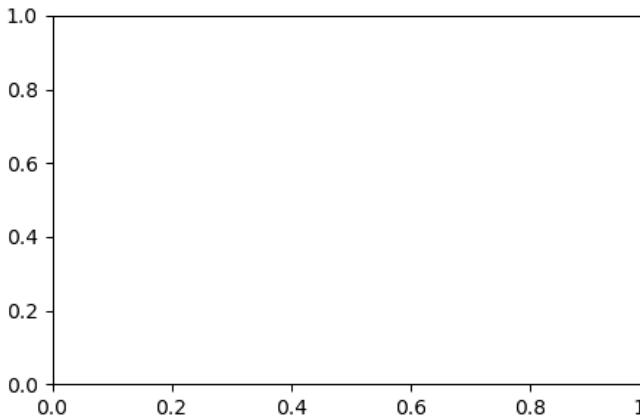
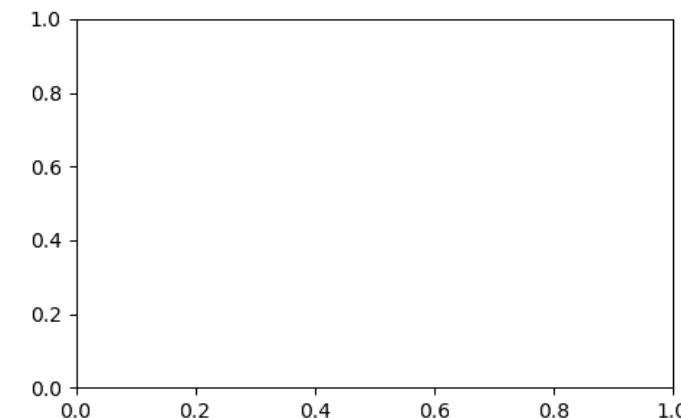
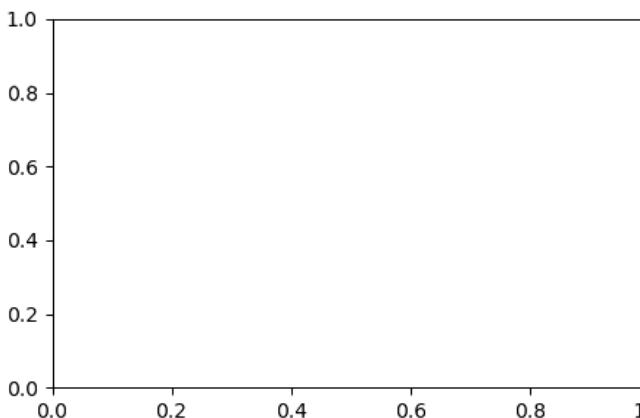
LUT
GenerationDevice
XploreDDB
GenerationDesign
XploreCode
Dive

Design Xplore

Figure 1 X

Figure 2 X

+



Plot Tune Optimize

Plot 1A Plot 1B Plot 1C Plot 1D

Import: Plot 1B OK ?

DDB: ?

X-axis: ?

Y-axis: ?

 Use Advanced X Expression

X-Expr

 Use Advanced Y Expression

Y-Expr

 Show Schematic Append Plot Clear

Plot All

File View Tabs Tools Help



LUT Generation

Device Xplore

DDB Generation

Design Xplore

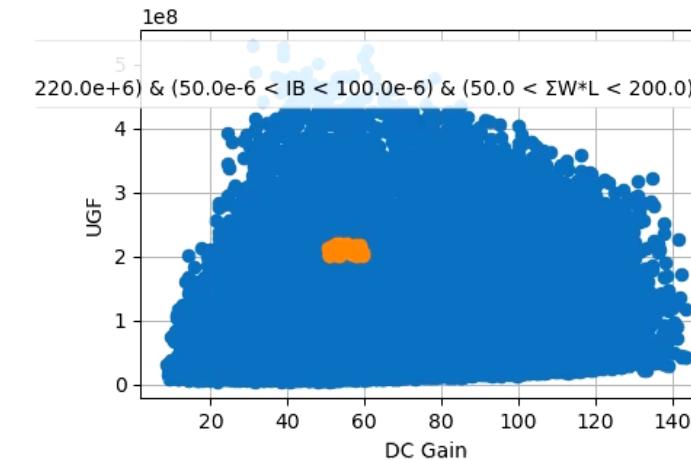
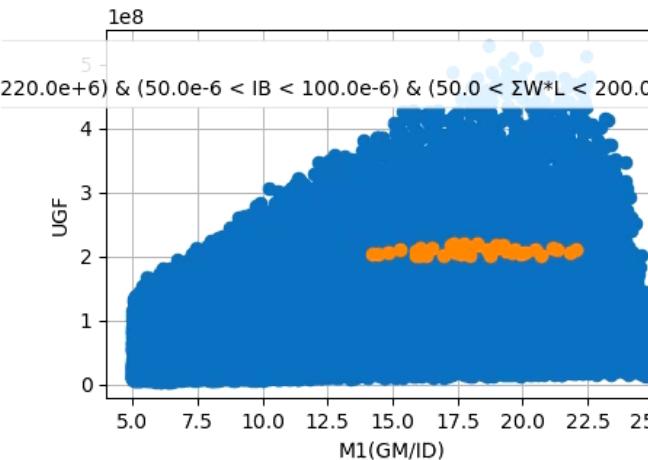
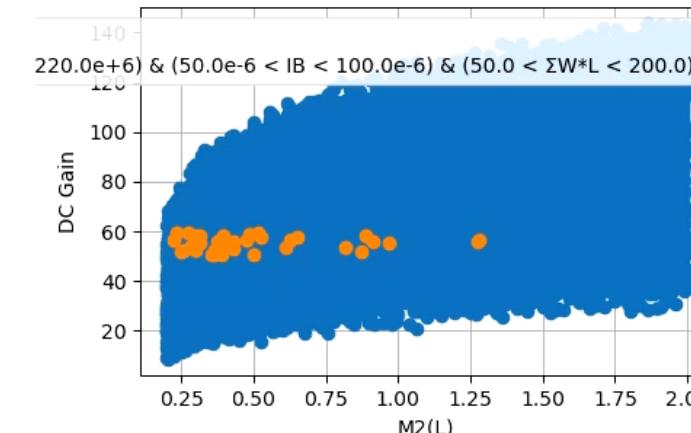
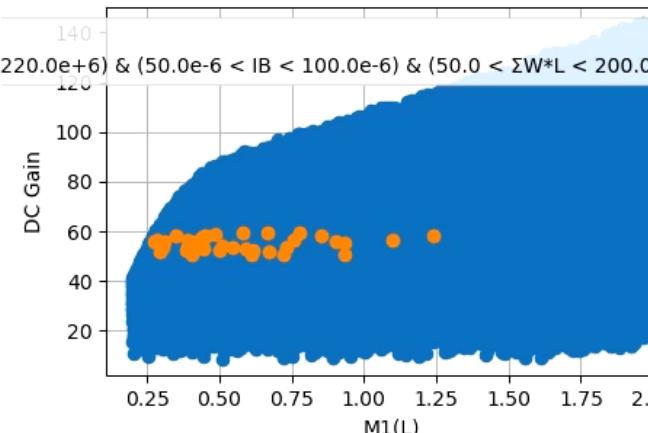
Code Dive

Design Tuning: Pick L

Figure 1 X

Figure 2 X

+



Plot Tune Optimize

Plot 1A Plot 1B Plot 1C Plot 1D

Import: Plot 1A

OK

DDB: A010002_100k.pdb

?

X-axis: M2(L)

?

Y-axis: DC Gain

?

 Use Advanced X Expression Use Advanced Y Expression

Y-Expr

 Show Schematic

VDD

1.8

Temp

Nominal

MOS-Corners

tt

Cout

1e-12

VoutCM

0.9

DC Gain

50

UGF

220e6

 Append

60

 Append

200e6

Clear

Plot

Plot All

Clear

Plot All

Clear

Plot All

Clear

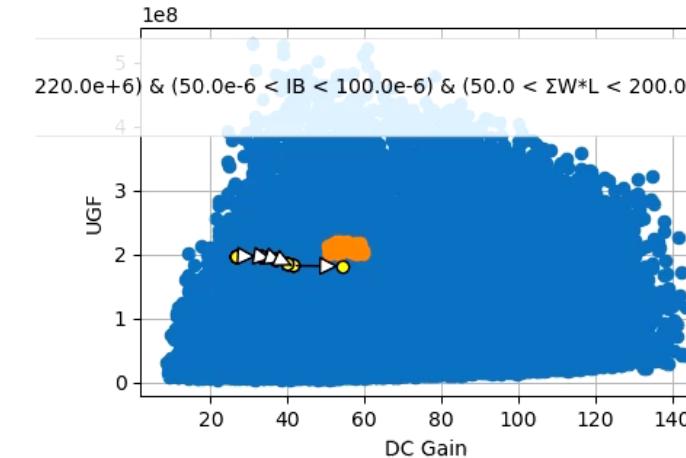
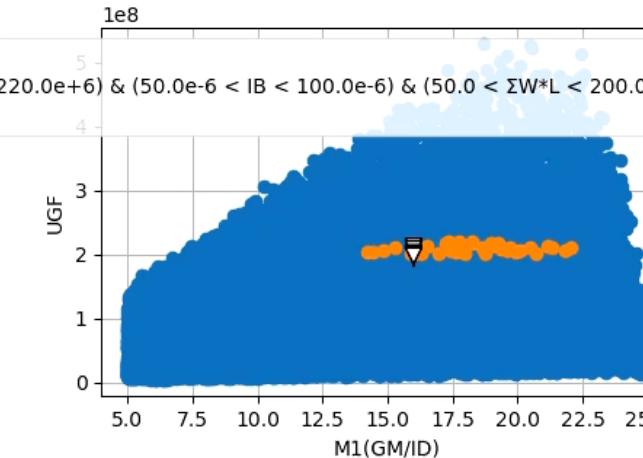
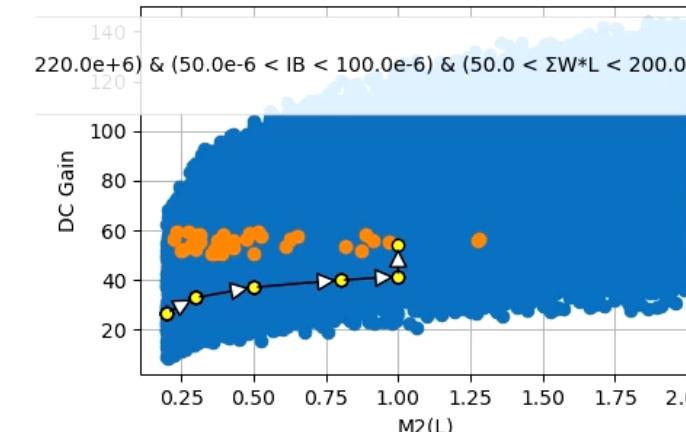
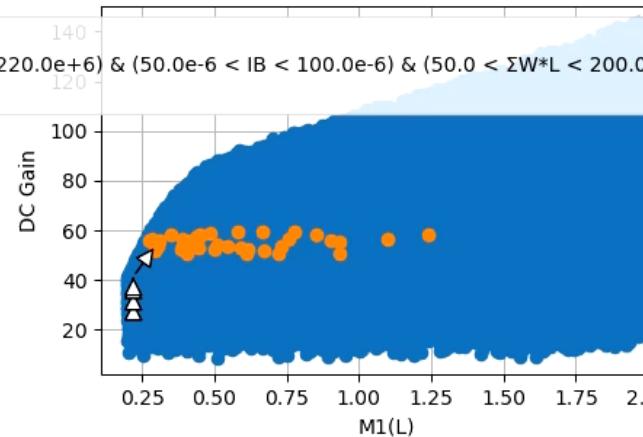
Plot All

Clear

Figure 1 XFigure 2 X

+

Design Tuning: Pick gm/ID


Plot
Tune
Optimize

DDB: A010002_100k.pdb

No of Points: 20

 Live Updates

DOFs

Specs

Spec	Generated Value
Temp	Nominal
M1(L)	300.0e-3
M2(L)	1.000
DC Gain	54.28
DC PSR (dB)	-11.7
input integrate...	13.95e-6
Thermal Output...	53.45e-15
Output Swing	1.475
BW	3.343e+06
UGF	181.4e+6
PM	-89.31
Vout Max	1.600
Vout Min	125.0e-3
$\Sigma W*L$	143.0

Plot

Clear

Verify

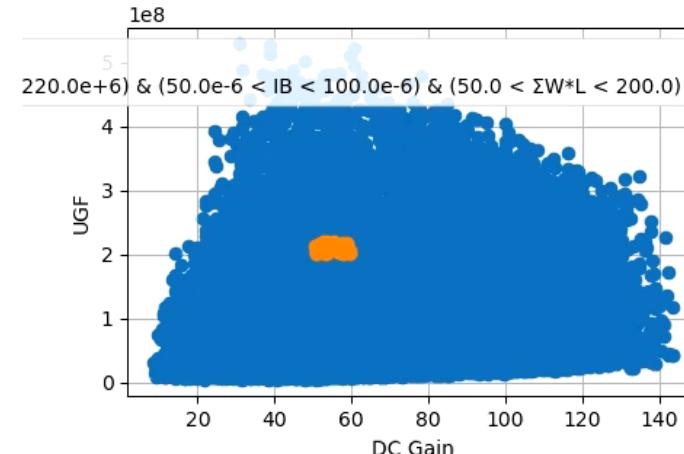
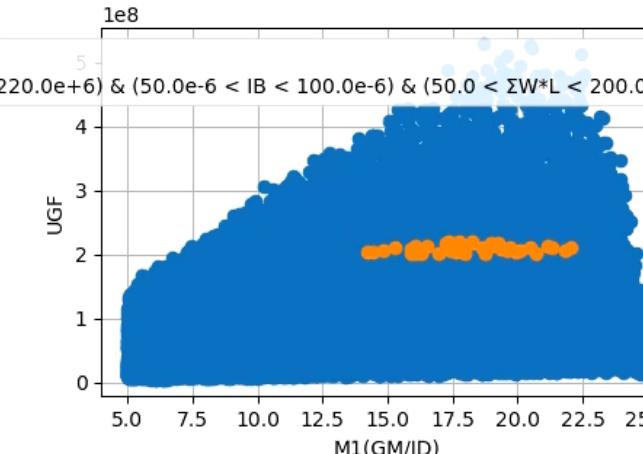
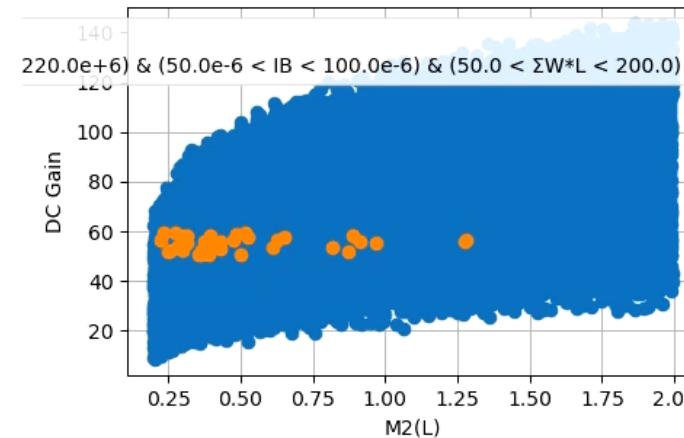
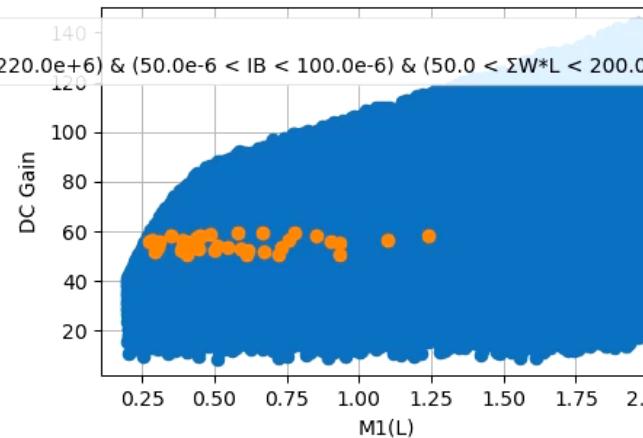


Figure 1

Figure 2



Live Tuning and More!



Plot Tune Optimize

DDB: A010002_100k.pdb

No of Points: 20

 Live Updates

DOFs

NMOS-LUT	ee214e_nch_tt
PMOS-LUT	ee214e_pch_tt
M1(L) (um)	0.3
M1(GM/ID)	18
M2(L) (um)	1
M2(GM/ID)	10
IB	80u
VoutCM	0.9
Cout	1p
Saturation Voltage	Vstar
MOS-Corners	TT
TEMP	Nominal
VDD	1.8

Spec	Generated Value
Temp	Nominal
M1(L)	300.0e-3
M2(L)	1.000
DC Gain	55.95
DC PSR (dB)	-12.49
input integrate...	12.37e-6
Thermal Output...	48.08e-15
Output Swing	1.489
BW	3.616e+06
UGF	202.8e+6
PM	-89.54
Vout Max	1.600
Vout Min	111.1e-3
$\Sigma W*L$	147.9

Plot

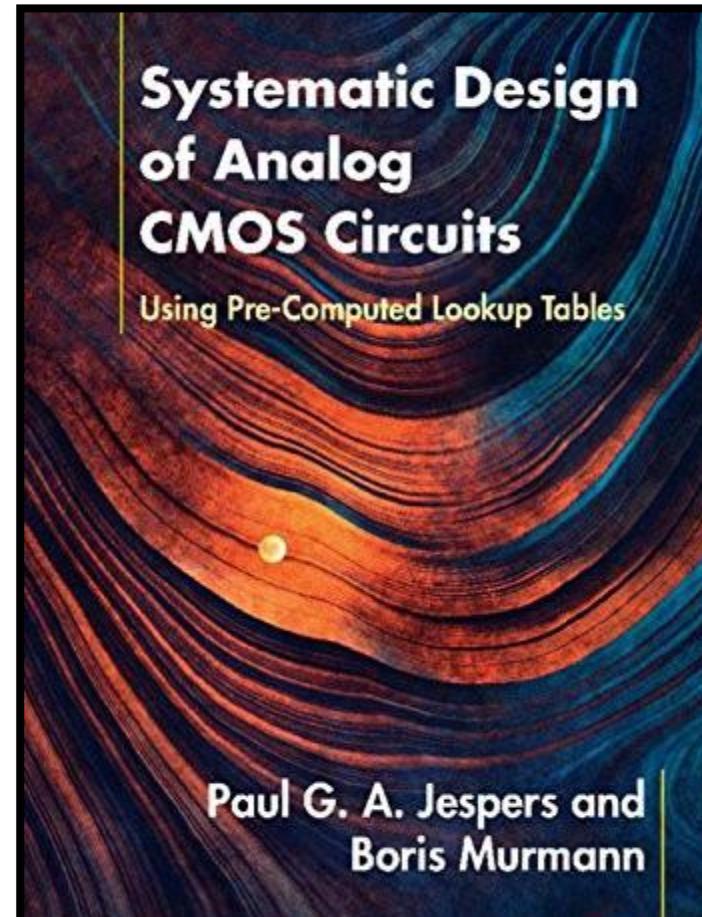
Clear

Verify

Thank you!

References (1/3)

- P. Jespers and B. Murmann, Systematic Design of Analog CMOS Circuits Using Pre-Computed Lookup Tables, Cambridge University Press, 2017.
- B. Murmann, Gm/ID Starter Kit. [Online]. Available: <https://web.stanford.edu/~murmann/gmid>



References (2/3)

- A. A. Youssef, B. Murmann and H. Omran, "Analog IC Design Using Precomputed Lookup Tables: Challenges and Solutions," in IEEE Access, vol. 8, pp. 134640-134652, 2020.



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Digital Object Identifier 10.1109/ACCESS.2020.3010875

Analog IC Design Using Precomputed Lookup Tables: Challenges and Solutions

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AND HESHAM OMRAN^{ID1}**

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²Department of Electrical Engineering, Stanford University, Stanford, CA 94305, USA

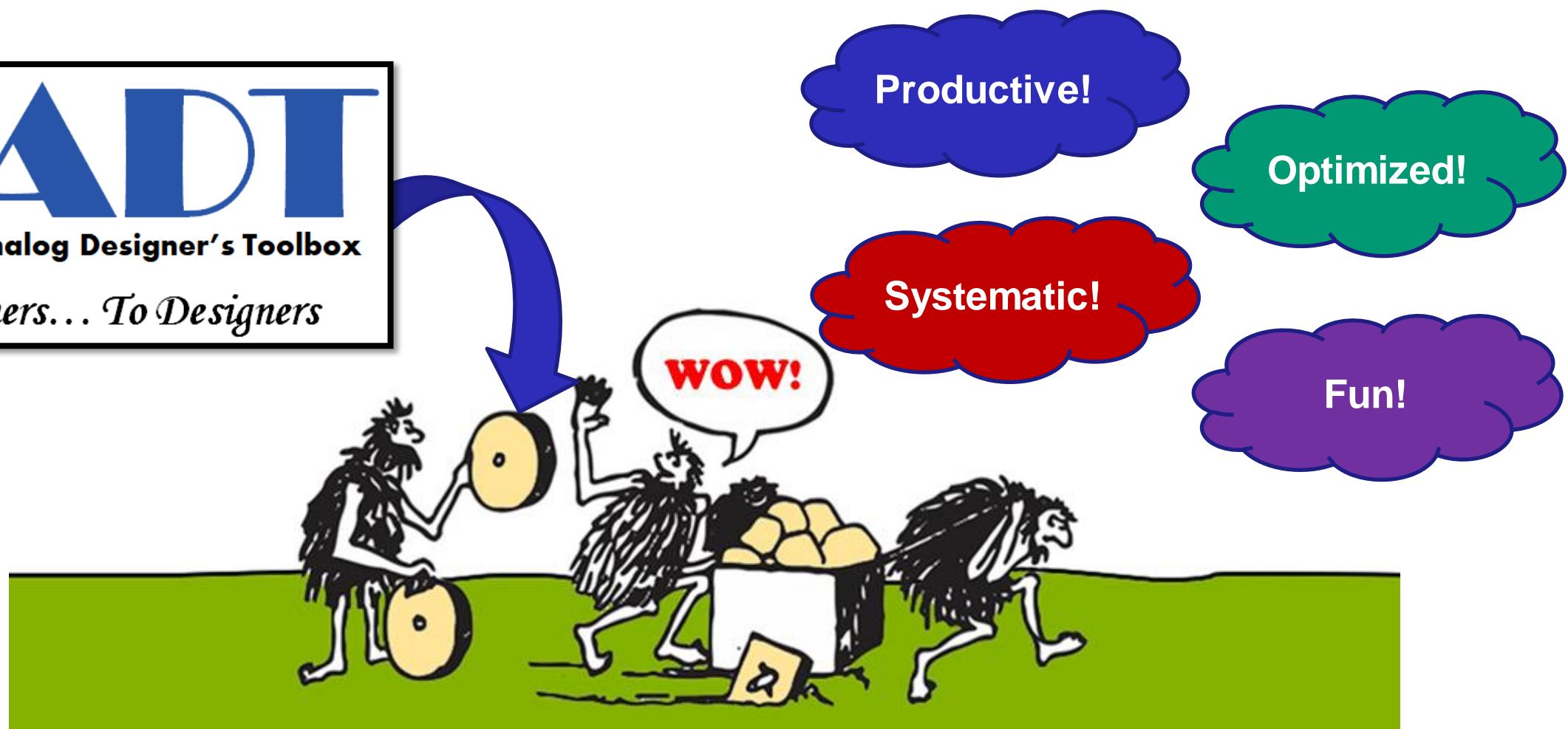
Corresponding author: Hesham Omran (hesham.omran@eng.asu.edu.eg)

References (3/3)

- <https://www.master-micro.com/mastering-microelectronics/courses/analog-ic-design>

The screenshot shows a web browser window displaying the Master Micro website. The URL in the address bar is [master-micro.com/mastering-microelectronics/courses/analog-ic-design](https://www.master-micro.com/mastering-microelectronics/courses/analog-ic-design). The page features a large logo for "MASTER MICRO" with a stylized blue and black "M" and a microchip icon. A prominent red banner across the middle of the page reads "Analog IC Design". To the left, a sidebar menu titled "Master Micro" lists various navigation options: Home, News, Analog Designer's Toolbox, and a expanded section for "Mastering Microelectronics" which includes "Courses" (with "Introduction to Electronics" listed), "Analog IC Design" (with "Course Information", "Course Plan", "Course Resources", and "Analog Systems Design" listed). The main content area contains text about the course and a list of course details, followed by a section titled "What Students Say About This Course".

Q & A



"If you can't describe what you are doing as a process, you don't know what you're doing."

W. Edwards Deming