Analog IC Design

Lecture 13
gm/ID Design Methodology

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Outline

- MOSFET figures-of-merit (FoM)
- SPICE vs square-law
- V^* and V_{Dsat}
- Subthreshold operation (weak inversion)
- Gm/ID design methodology

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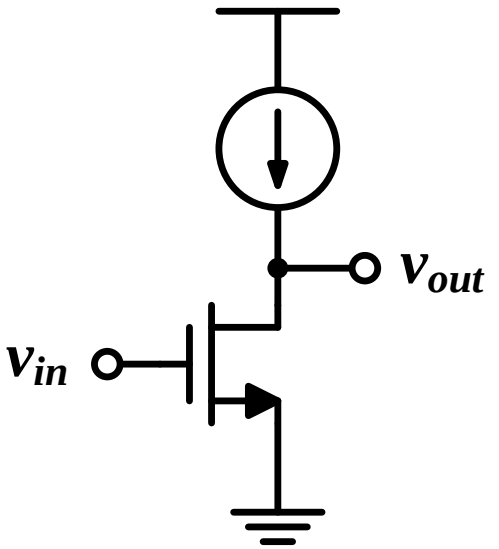
MOSFET Figures-of-Merit (FoM)

- Intrinsic gain: gm*ro
- Intrinsic frequency (transit frequency): gm/Cgg
- Current (transconductance) efficiency: gm/ID

Intrinsic Gain

$$v_{out} = -(g_m v_{in}) r_o$$

$$|A_i| = \left|\frac{v_{out}}{v_{in}}\right| = g_m r_o$$



- $g_m r_o$ is the max gain that can be obtained from a single transistor

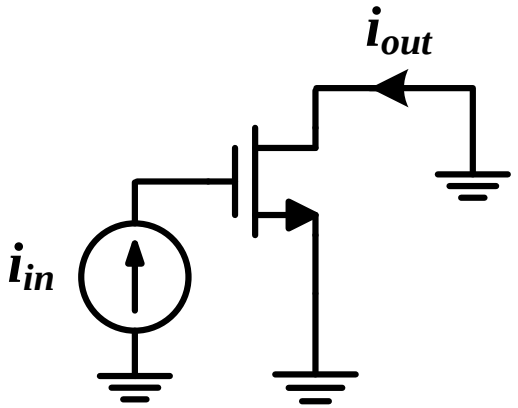
$$g_m r_o = \frac{2I_D}{V_{ov}} \cdot \frac{1}{\lambda I_D} = \frac{2}{\lambda V_{ov}} = \frac{2V_A}{V_{ov}}$$

- For higher gain
  - Lower V_{ov} (or equivalently lower I_D): weak inversion and subthreshold operation
  - Longer L (i.e., smaller λ)
  - Both come at the expense of speed

Intrinsic Frequency

- f_T is the frequency at which the MOSFET s.c. current gain drops to one (i.e., unity-gain frequency)

$$i_{out} = g_m v_{gs} = g_m \frac{i_{in}}{sC_{gg}}$$



@ $i_{out} = i_{in}$

$$f_T = \frac{g_m}{2\pi C_{gg}}$$

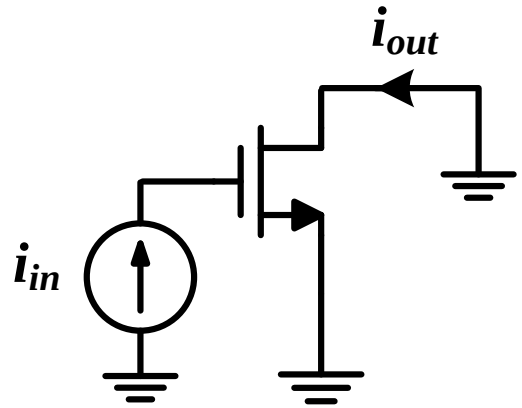
$$\approx \frac{1}{2\pi} \cdot \mu C_{ox} \frac{W}{L} V_{ov} \cdot \frac{1}{\frac{2}{3} WLC_{ox}}$$

$$\approx \frac{3\mu V_{ov}}{4\pi L^2}$$

Intrinsic Frequency (Speed)

- f_T is the frequency at which the MOSFET s.c. current gain drops to one (i.e., unity-gain frequency)

$$f_T \approx \frac{3\mu V_{ov}}{4\pi L^2}$$



- For higher speed
  - Higher V_{ov} (or equivalently higher I_D): strong inversion and higher power consumption
  - Shorter L (technology scaling helps!)
  - Just opposite to higher gain!
  - Analog design is all about trade-offs!
- After velocity sat, g_m and f_T saturate and become independent of V_{ov}

gm/ID

- gm/ID is the transconductance per unit current (a measure of energy efficiency)
  - How much transconductance (or GBW) can we get from each micro-amp of current

$$\frac{g_m}{I_D} = \frac{2}{V_{ov}}$$

- For higher efficiency
  - Lower V_{ov} (or equivalently lower I_D): weak inversion and subthreshold operation
  - Comes at the expense of speed

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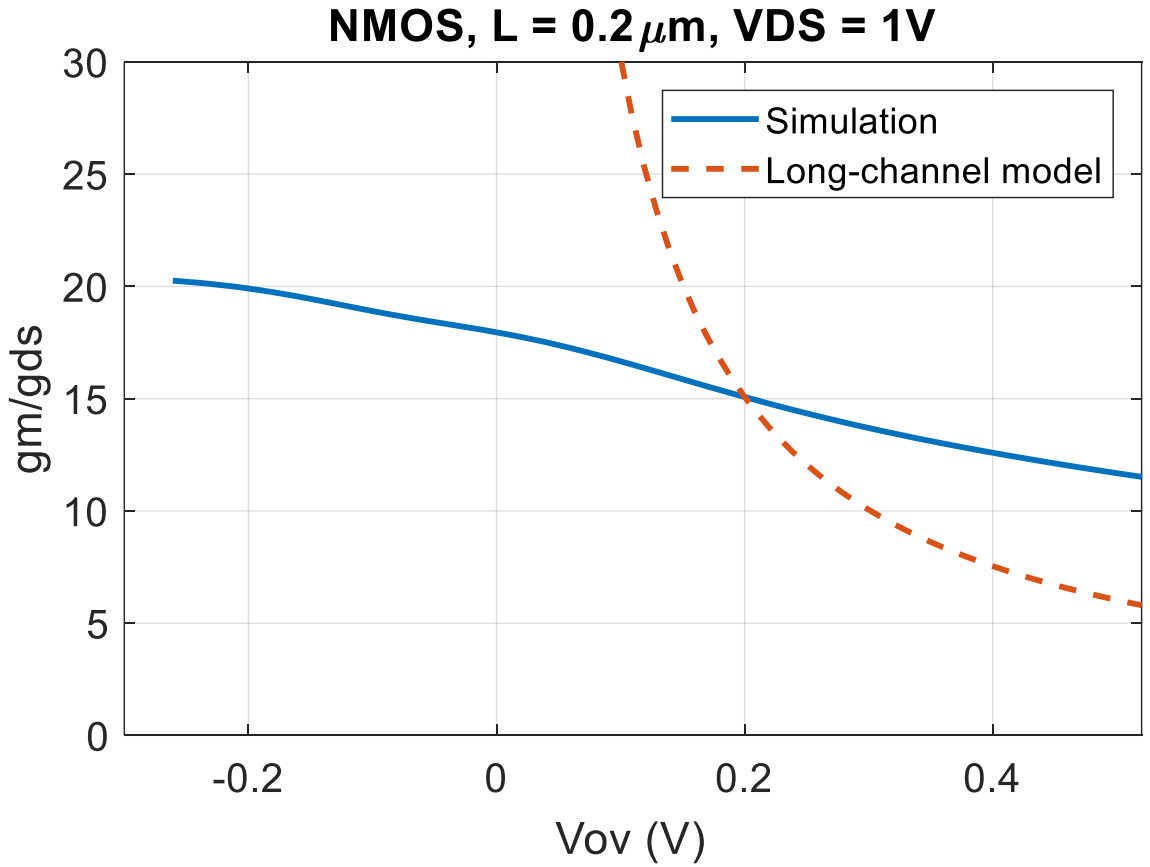
SPICE vs Square-Law: $g_m r_o$

- Square-law expects infinite $g_m r_o$ at $V_{ov} = 0$

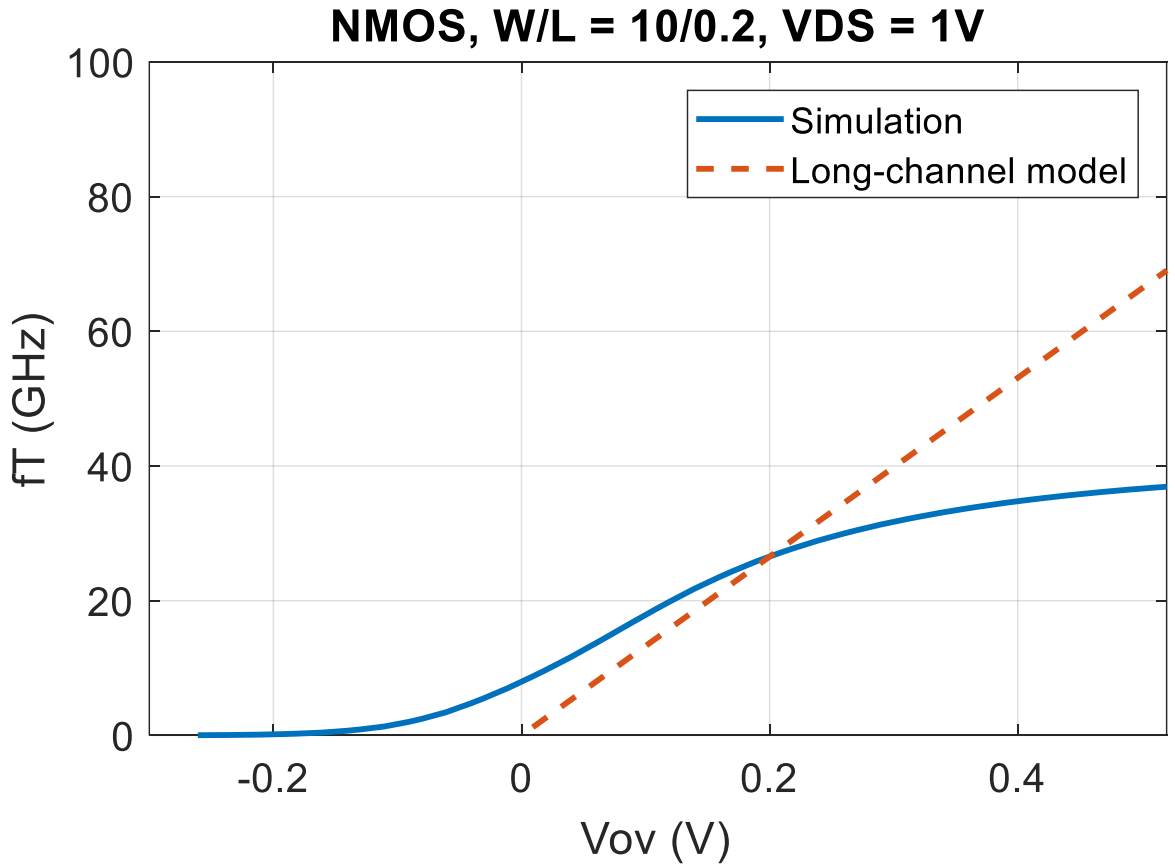
$$g_m r_o = \frac{2}{\lambda V_{ov}} = \frac{2V_A}{V_{ov}}$$



SPICE vs Square-Law: f_T

- Square-law expects f_T increases linearly with V_{ov}

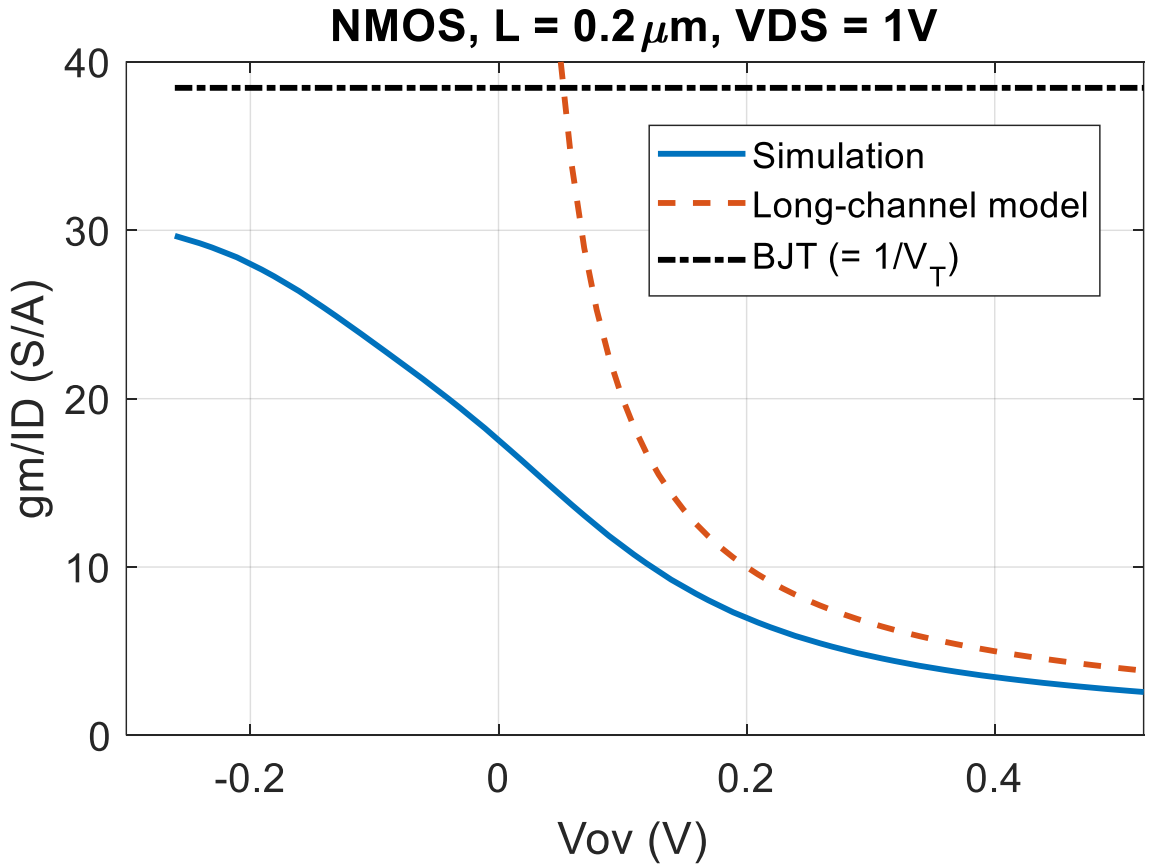
$$f_T = \frac{g_m}{2\pi C_{gg}} \approx \frac{3\mu V_{ov}}{4\pi L^2}$$



SPICE vs Square-Law: g_m/I_D

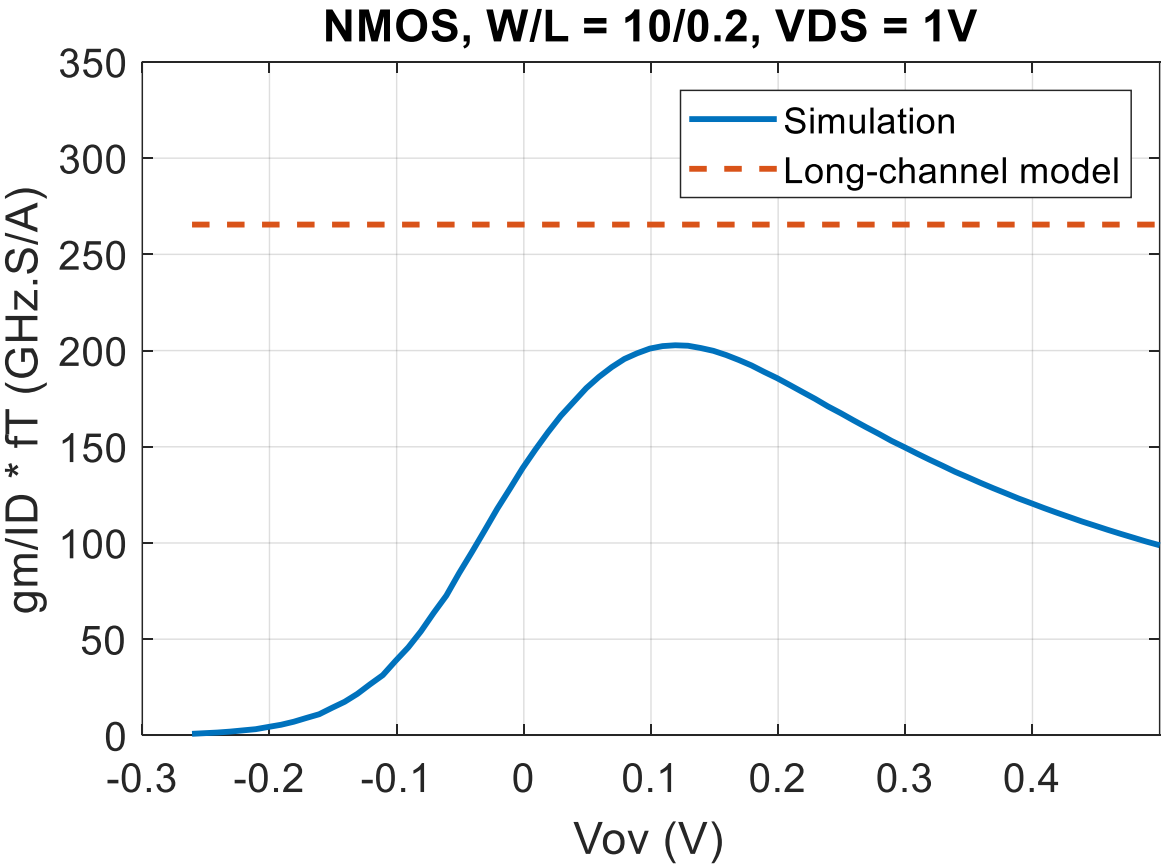
- Square-law expects infinite g_m/I_D at $V_{ov} = 0$

$$\frac{g_m}{I_D} = \frac{2}{V_{ov}}$$



SPICE vs Square-Law: The Sweet-Spot

- Global maximum in MI: Sweet-spot
  - Best compromise between efficiency and speed



SPICE vs Square-Law: Conclusions

- Square-law fails to describe SI accurately
  - Short channel effects (e.g., velocity sat.) are not considered
- Square-law fails to describe MI and WI completely
  - A completely different approach is required

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V-star (V^*)

- We used $g_m = \frac{2I_D}{V_{ov}}$ which is based on the square-law
- For a real MOSFET $V_{ov} \neq \frac{2I_D}{g_m}$
- Let's define a new parameter called V-star (V^*) which is calculated from actual simulation data using the formula

$$V^* = \frac{2I_D}{g_m} \leftrightarrow g_m = \frac{2I_D}{V^*}$$

- For a square-law device, $V^* = V_{ov}$, however, for a real MOSFET they are not equal.

Figures-of-Merit Revisited

- Redefine the figures-of-merit in terms of V^*

$$g_m r_o = \frac{2I_D}{V^*} \cdot \frac{1}{\lambda I_D} = \frac{2}{\lambda V^*} = \frac{2V_A}{V^*}$$

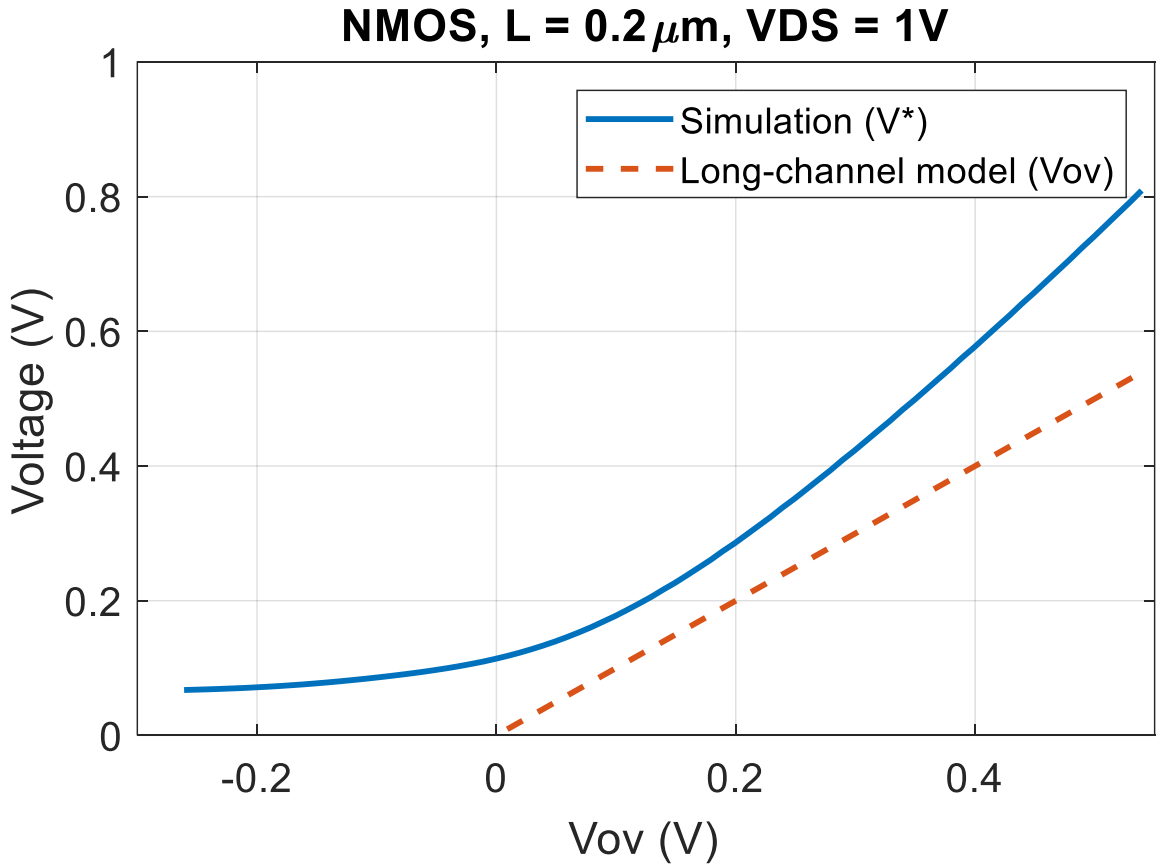
$$f_T = \frac{g_m}{2\pi C_{gg}} = \frac{1}{2\pi} \cdot \frac{2I_D}{V^*} \cdot \frac{1}{C_{gg}}$$

$$\frac{g_m}{I_D} = \frac{2}{V^*}$$

- Does V^* continue to decrease as V_{ov} goes towards weak inversion?

V^* vs V_{ov}

- SI: $V^* > V_{ov} \rightarrow g_m = \frac{2I_D}{V^*}$ is less than square-law expectations
- WI: $V^* \approx constant \rightarrow$ Why?

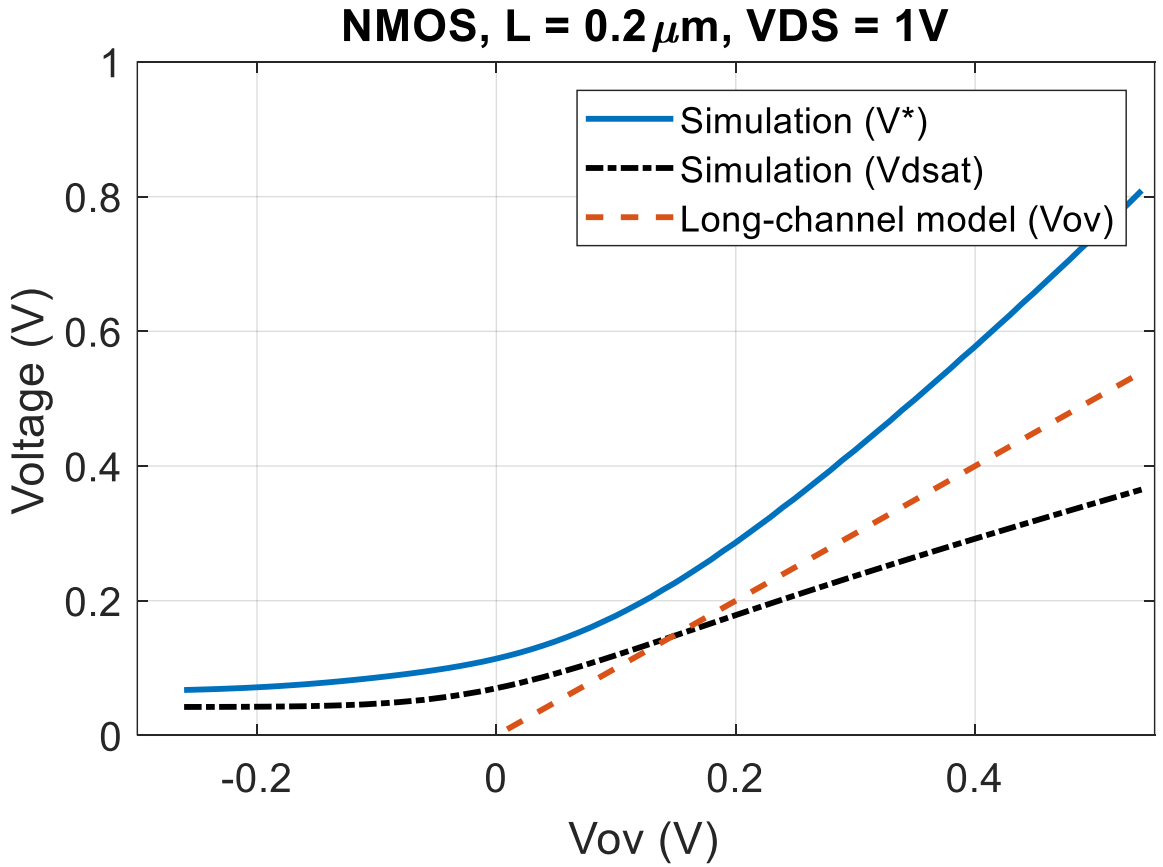


Drain Saturation Voltage (V_{Dsat})

- In general MOSFET is in saturation if $V_{DS} > V_{Dsat}$
- The definition of V_{Dsat} is a bit **vague**
  - I_D keeps increasing if $V_{DS} > V_{Dsat}$ due to CLM/DIBL
  - r_o is quite low at edge of saturation ($V_{DS} = V_{Dsat}$)
    - r_o increases by multiple folds by biasing the MOSFET deeper into saturation
  - For a square-law device: $V_{Dsat} = V_{ov}$
    - In actual model V_{Dsat} is a bit complex parameter
  - V^* is usually larger than V_{Dsat}
    - As an approximation we can use $V_{DS} > V^*$ as sat. condition
    - Guarantees biasing the MOSFET a bit deeper into saturation

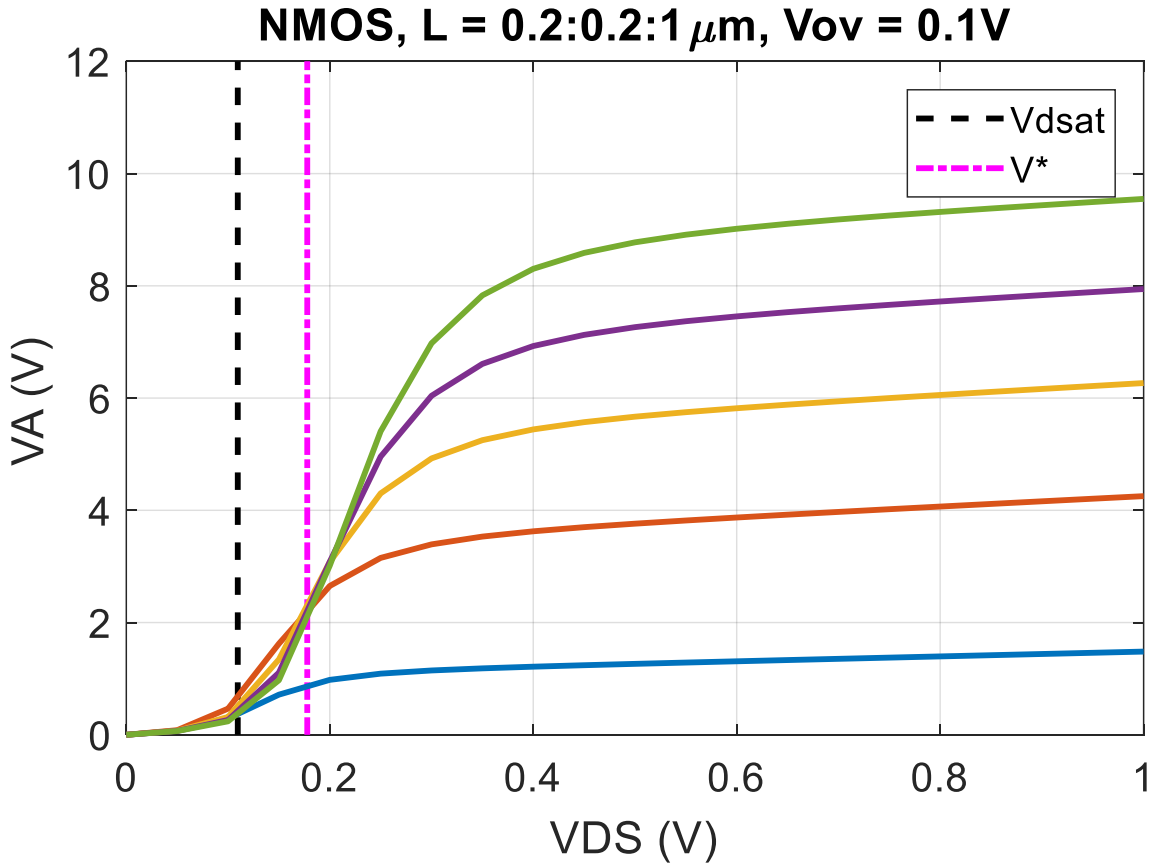
V^* vs V_{Dsat} vs V_{ov}

- $V_{Dsat} < V_{ov}$ in SI but $V_{Dsat} > V_{ov}$ in WI
- V^* always $> V_{Dsat}$



Is V_{Dsat} really meaningful?

- $r_o = \frac{V_A}{I_D}$ is quite low at $V_{DS} = V_{Dsat}$ → Longer L doesn't help!
- r_o increases order of magnitude by going deeper into saturation
  - Longer L helps **only when** V_{DS} is large



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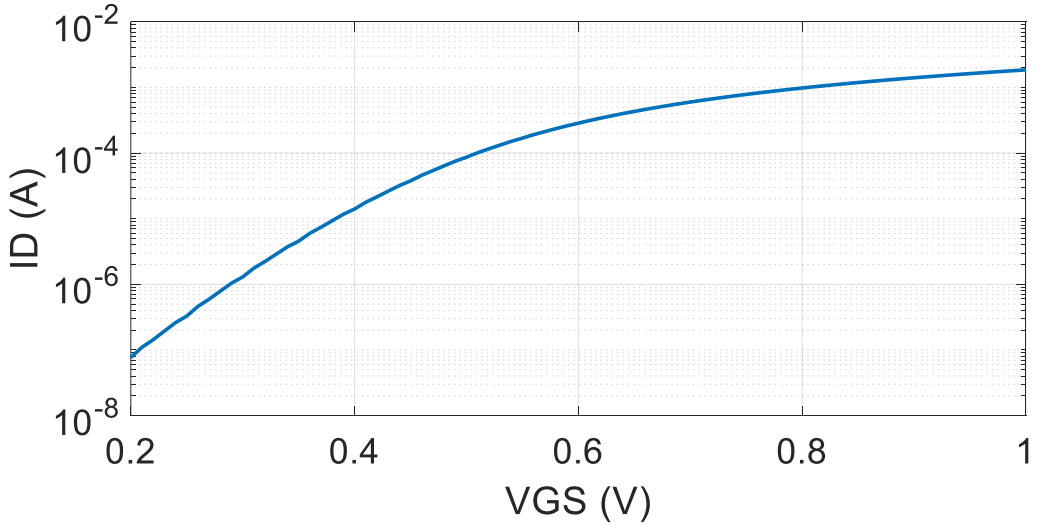
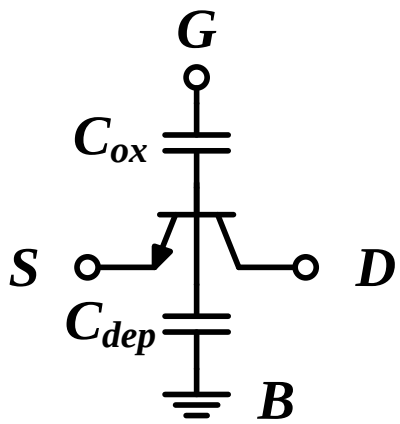
Subthreshold Operation (Weak Inversion)

- MOSFET behaves as a BJT (npn for an NMOS) with its base coupled to the gate through capacitive divider
  - Subthreshold current depends exponentially on V_{GS}
  - For $V_{DS} > V_{Dsat}$ (saturation):

$$I_D \approx I_0 \frac{W}{L} e^{\frac{V_{GS}-V_{TH}}{nV_T}}$$

$$n = \frac{C_{ox} + C_{dep}}{C_{ox}} \approx 1.2 \rightarrow 1.5$$





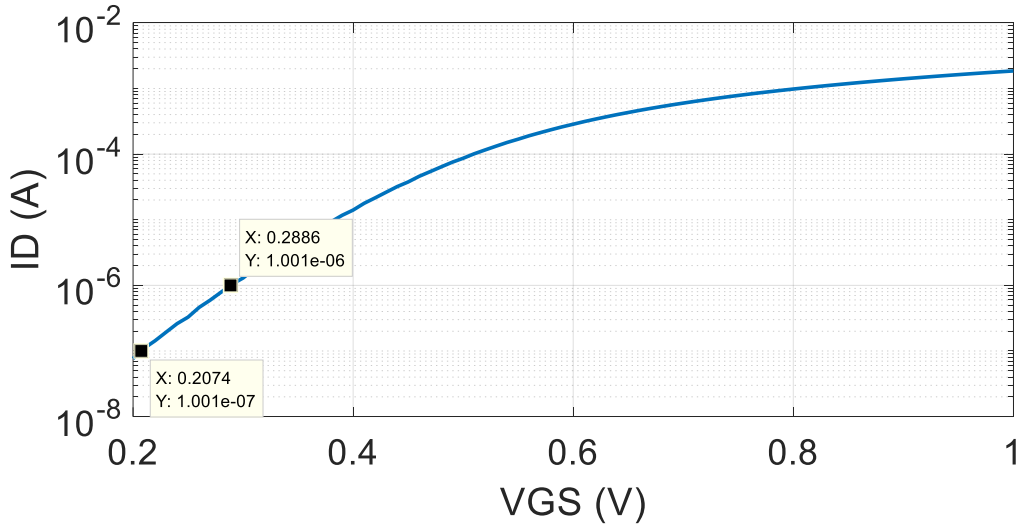
Subthreshold Slope (S)

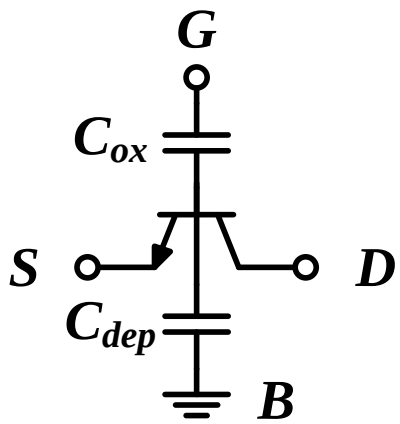
$$I_D = I_0 \frac{W}{L} e^{\frac{V_{GS}-V_{TH}}{nV_T}}$$

$$\log I_D = \log I_0 \frac{W}{L} e^{\frac{-V_{TH}}{nV_T}} + \frac{V_{GS}}{nV_T} \log e$$

$$S = \left(\frac{\partial \log I_D}{\partial V_{GS}}\right)^{-1} = \frac{nV_T}{\log e} = nV_T \ln 10 = n \times 60\ mV/decade$$

- Example: $S = 0.2886 - 02074 \approx 81mV/decade \rightarrow n \approx 1.35$





V^* in Weak Inversion

$$I_D = I_{Do}\frac{W}{L}e^{\frac{V_{GS}}{nV_T}}$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{nV_T} = \frac{2I_D}{V^*}$$

$$\boldsymbol{V^* = 2nV_T}$$

- At the boundary between exponential weak inversion (WI) and quadratic strong inversion (SI): a.k.a. the onset of strong inversion

$$V^* = V_{ov}$$

$$V_{ov} = 2nV_T \approx (1.2 \rightarrow 1.5) \times 52mV \approx 60 \rightarrow 80\ mV$$

- The region between WI (exponential behavior) and SI (square-law behavior) is referred to as **moderate inversion (MI)**
  - No simple models for this region (a.k.a. near-threshold operation)

Subthreshold Intrinsic Gain

$$g_m r_o = \frac{2I_D}{V^*} \cdot \frac{1}{\lambda I_D} = \frac{2}{\lambda V^*} = \frac{1}{\lambda n V_T} = \frac{V_A}{nV_T}$$

- Independent of V_{ov}
- Gain does not improve as we go deeper in subthreshold

Subthreshold Current Efficiency

$$\frac{g_m}{I_D} = \frac{2}{V^*} = \frac{1}{nV_T}$$

- Independent of V_{ov}
- Efficiency does not improve as we go deeper in subthreshold

Subthreshold Intrinsic Speed

$$f_T = \frac{g_m}{2\pi C_{gg}}$$
$$\approx \frac{1}{2\pi} \cdot \frac{2I_D}{V^*} \cdot \frac{1}{C_{gg}}$$
$$\approx \frac{I_D}{2\pi n V_T C_{gg}}$$

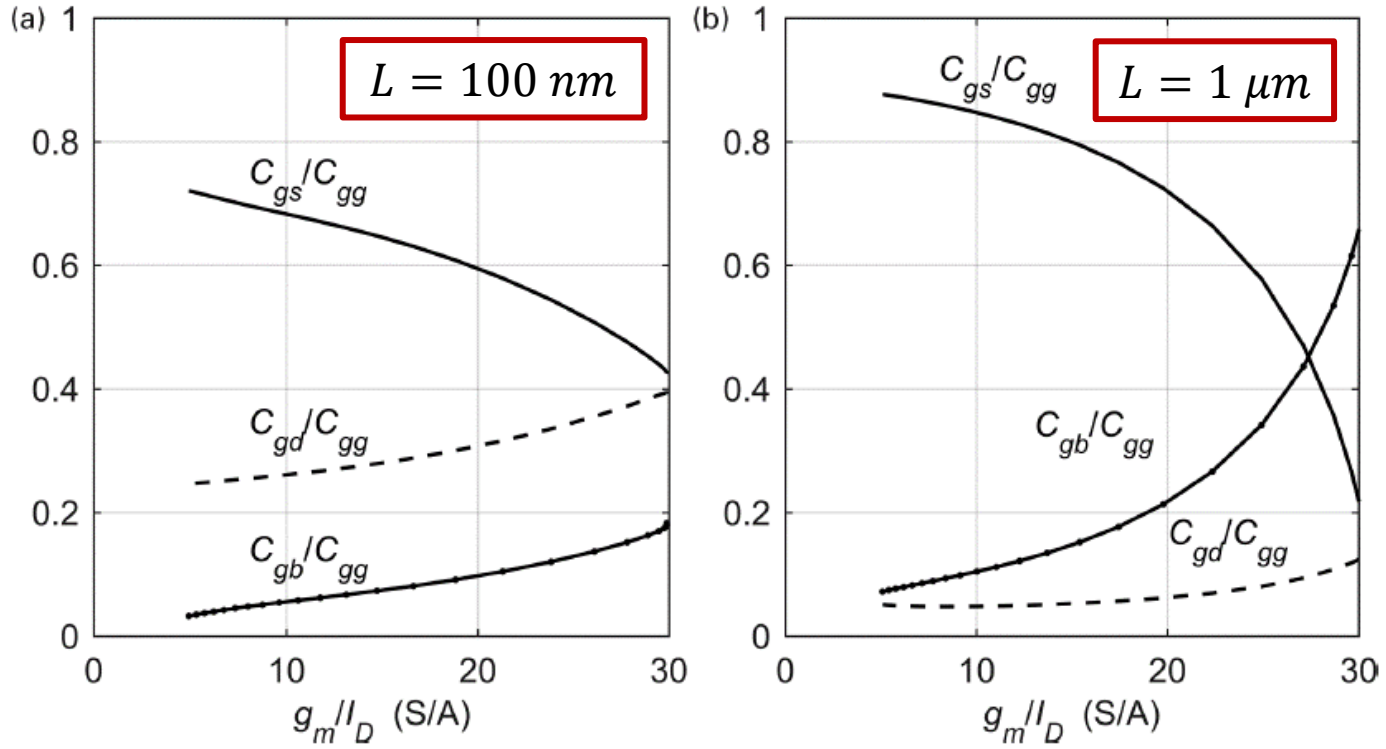
- Speed (f_T) continues to degrade as we go deeper in subthreshold
  - I_D decreases exponentially

Near-Threshold (MI) Biasing

- Operating the MOSFET in the near-threshold (moderate inversion) region is becoming increasingly popular.
  - We already reap most of WI benefits
    - Higher gain
    - Higher efficiency
    - Some degradation in speed (f_T is already very high for short L)
- Going deeper into WI is seldom useful
  - Minor/no benefit in gain
  - Minor/no benefit in efficiency
  - Exponential degradation in speed
  - Exponential increase in area and parasitics
  - But may be useful if we intentionally need very low I_D (ultra low power applications)

MOSFET Capacitance in WI vs SI

- For SI: $C_{gb} \approx 0, C_{gs} \gg C_{gd}$
- For WI: $C_{gb} \uparrow, C_{gs} \approx C_{gd}$
  - For long channel C_{gb} in WI is more significant
  - For short channel, source and drain still hide the bulk even in WI



[Jespers & Murmann, 2018]

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Don’t be a SPICE Monkey!

- In absence of a clear methodology for hand analysis, many designers tend to converge toward a “SPICE monkey” design methodology.
  - No hand calculations, iterate in SPICE until the circuit “somehow” meets the specifications
  - Typically results in sub-optimal designs, uninformed design decisions, etc.
- A SPICE monkey is someone who does not use hand analysis to figure out how to design a circuit, but rather plugs stuff into SPICE and uses whatever value works.

gm/ID Design Methodology

- Traditionally, square-law was used in hand analysis to obtain initial design point
  - But short channel and moderate/weak inversion devices do not obey the square law
  - Square law is seldom used in nowadays designs
- The popular approach nowadays is using gm/ID (or equivalently V*) design methodology
- Perform DC sweeps for both PMOS and NMOS to generate design charts vs gm/ID
  - Or use look-up tables (LUTs) and access them using any programming language (MATLAB, Python, etc.)
- Use these charts (LUTs) to design your circuit to meet required specs

The Design Problem

- MOSFET is a function of five variables
  - 3 (voltages) + 2 (sizing)
- Strictly: the designer needs to specify 5 DOF for every device in the circuit
  - (VGS, VDS, VSB, W, L)
- For analog IC design, MOS is usually biased in saturation (essentially a VCCS)
  - VGS is the primary voltage controlling the device behavior
  - VDS is of secondary importance: set to VDSAT + margin
  - VSB is of tertiary importance: usually imposed by circuit topology
- Practically: the designer worries about 3 DOF
  - (VGS, W, L)
- We usually set the device current (using current mirrors) rather than the device voltage
  - (ID, W, L)

DOFs in Conventional Design Flow

- While tweaking a circuit in the simulator, the designer plays with 3 DOFs
  - (ID, W, L)
  - Sweeping any DOF (ID, W, L) changes the bias point (inversion level) of the device
  - The “search-range” of W can be quite large (depends on both ID and L)

- The old fix:
  - Switch to (ID, Vov, L) instead of (ID, W, L)
  - But short channel and moderate/weak inversion devices do not obey the square law

- The new fix:
  - Switch to (ID, V*, L)

DOFs in gm/ID Design Methodology

- V* or gm/ID design methodology enables “orthogonal” DOFs
  - (ID, V*, L) or (ID, gm/ID, L)
  - gm/ID sets the inversion level independent of ID and L
  - When ID and/or L changes: Look up the new W in the LUTs (gm/ID kept unchanged)
  - Search-range of gm/ID is limited (typically 3 to 30)
  - gm/ID can be replaced by JD = ID/W for deep subthreshold design

gm/ID Design Methodology

- V_{ov} has a vague physical meaning and does not help the designer's intuition any more
- On the contrary
  - gm/ID is a key MOSFET FoM
  - gm/ID captures the relation between the basic function of the transistor (the transconductance) and the most valuable resource (the power consumption)
  - The range of gm/ID values doesn't differ much from one device to another and from one technology to another
  - gm/ID can be a thought as a normalized measure for the device inversion level
- Conclusion: use gm/ID as your primary design variable
  - Plot everything vs gm/ID

Quiz

- Assume $n = 1.5$ and $V_{ov} < 0.5V$.
- Assume square-law is valid in strong inversion.
- Calculate gm/ID range.
- Calculate the gm/ID at the sweet spot ($V^* = 200mV$).

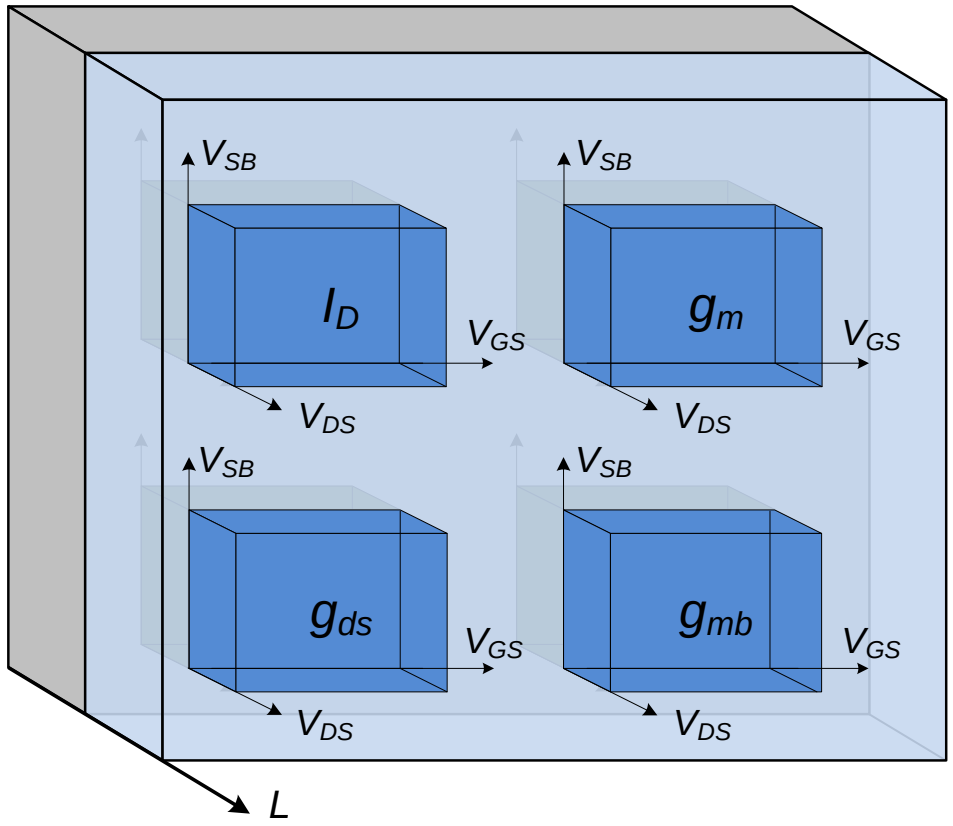
Quiz

- Assume $n = 1.5$ and $V_{ov} < 0.5V$.
- Assume square-law is valid in strong inversion.
- Calculate gm/ID range.
- Calculate the gm/ID at the sweet spot ($V^* = 200mV$).

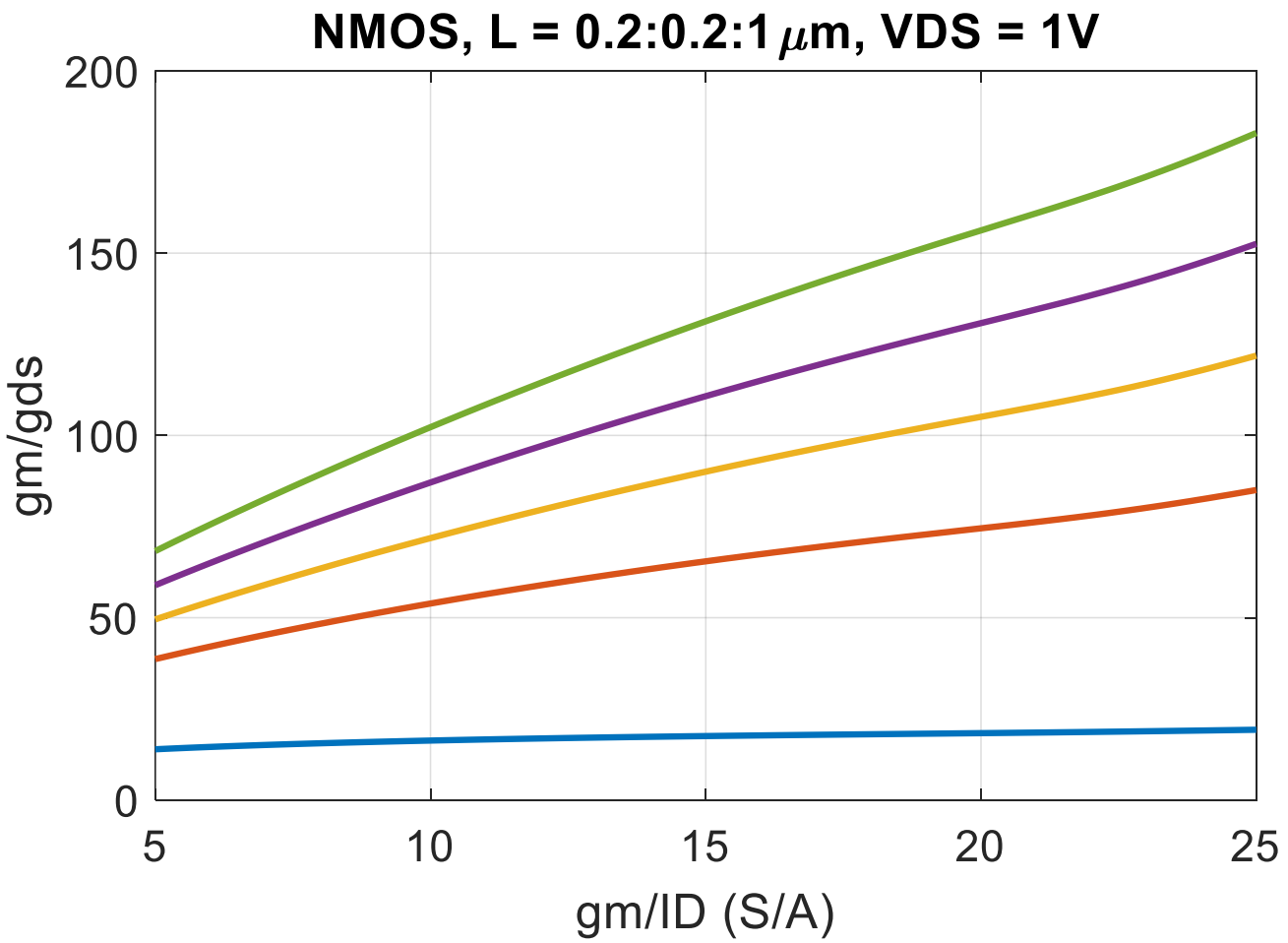
- $V^*_{max} = V_{ov,max} = 0.5V$
- $V^*_{min} = 2nV_T = 78m$
- $\frac{gm}{ID} = \frac{2}{V^*} = 4 \rightarrow 25$

The Lookup Table (LUT)

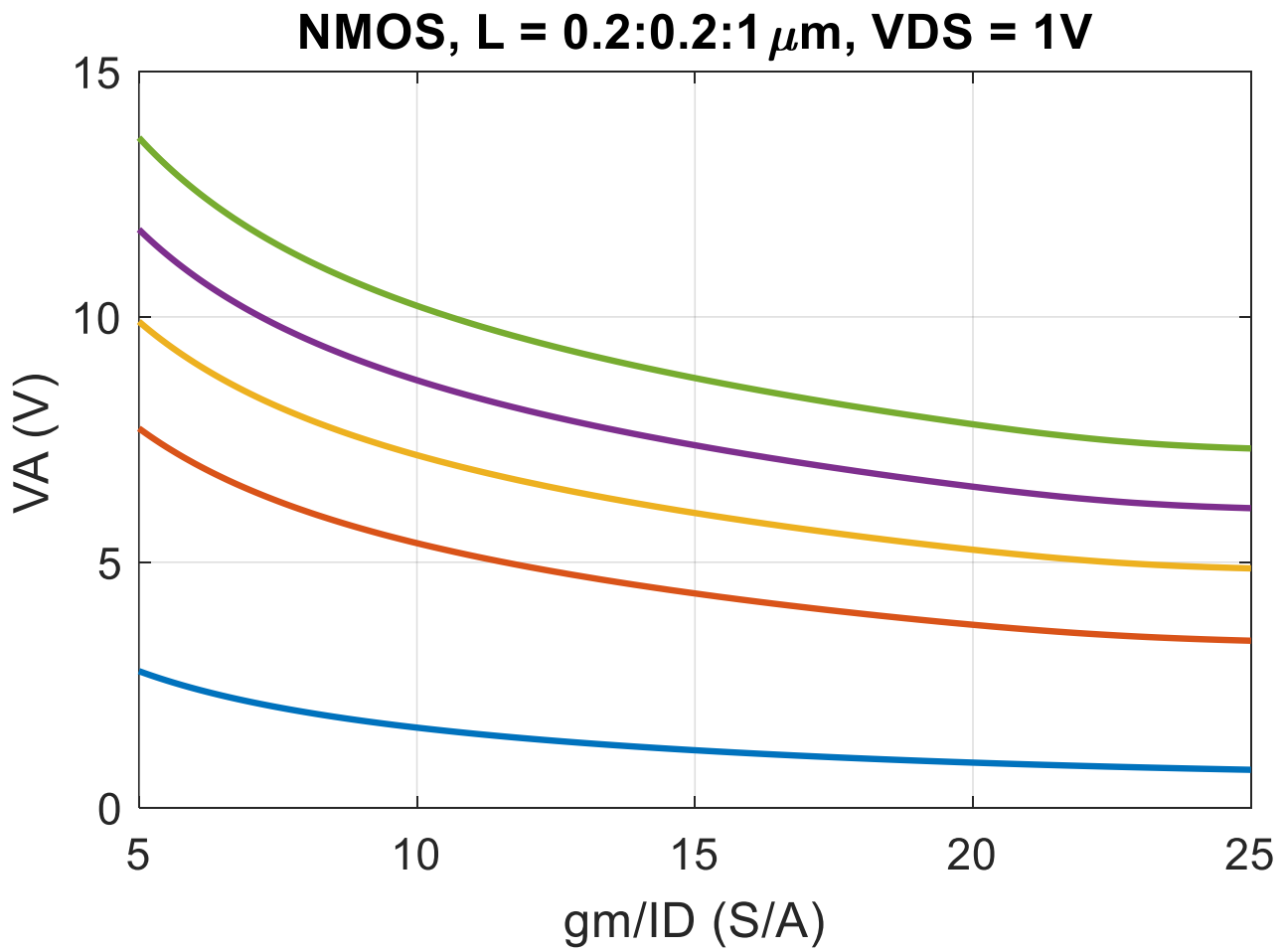
- MOSFET is a function of five variables
  - 3 (voltages) + 2 (sizing)
- All MOSFET parameters are proportional to width
  - Narrow-width effects ignored (not common in analog IC design)
  - Use normalized quantities (cross multiplication)
- Degrees of freedom (DOFs) reduced to 4
  - VGS, VDS, VSB, and L
- Simulate a reference device
  - Sweep the 4 DOFs
  - Construct a 4D LUT for every parameter
- May ignore VDS and VSB dependence to plot 2D parametric charts



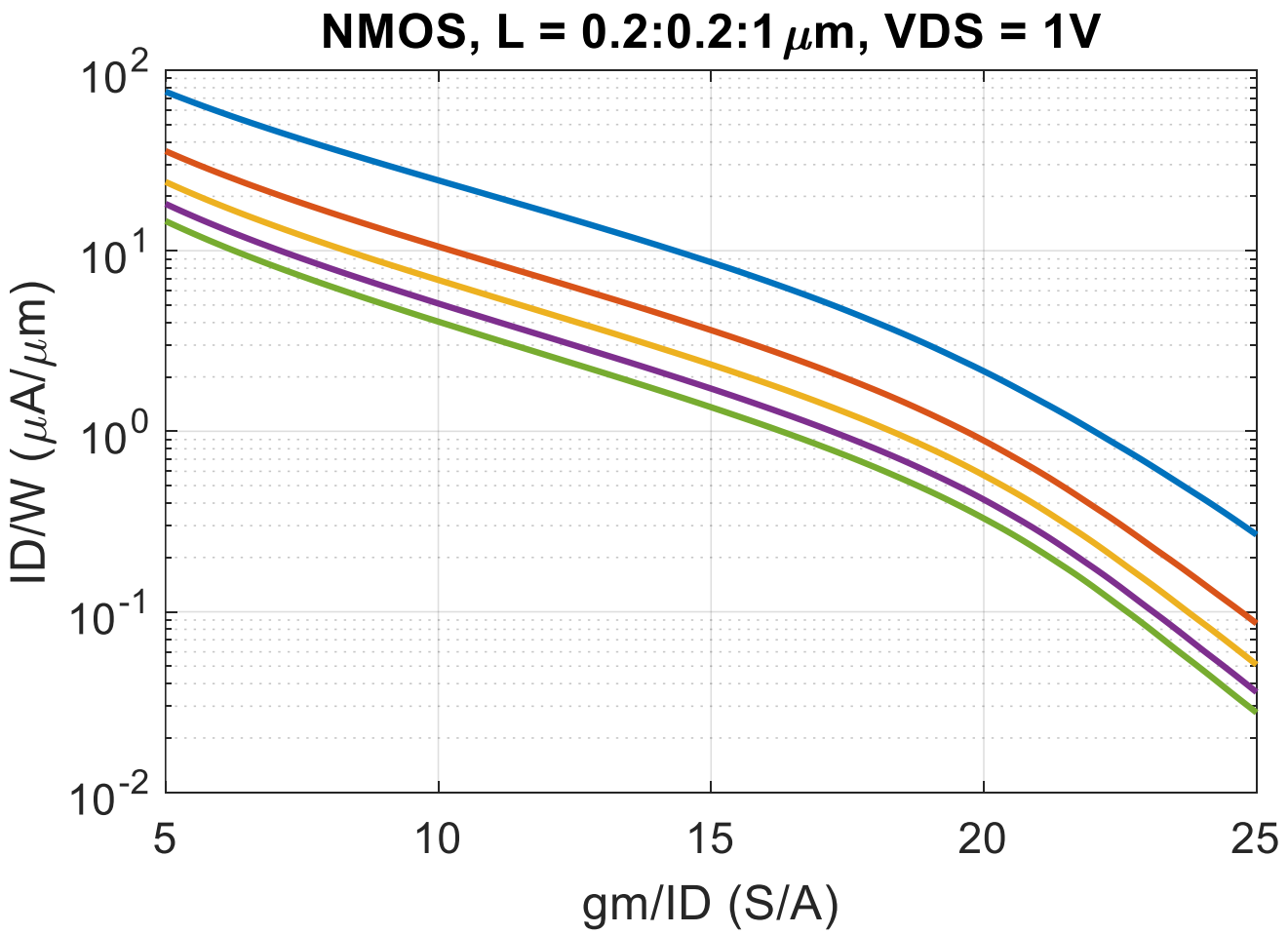
gm/ID Charts: $g_m r_o$



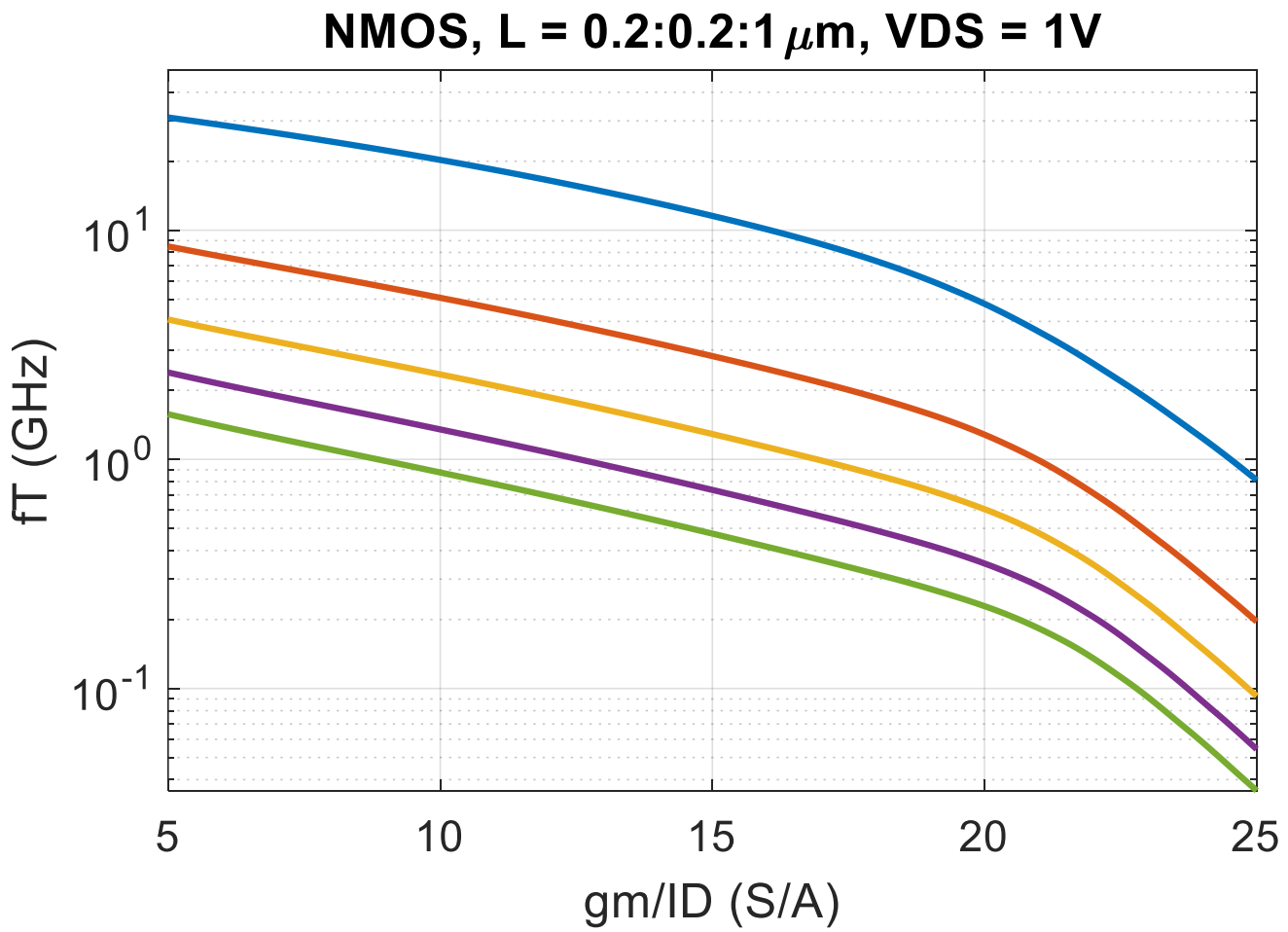
gm/ID Charts: V_A



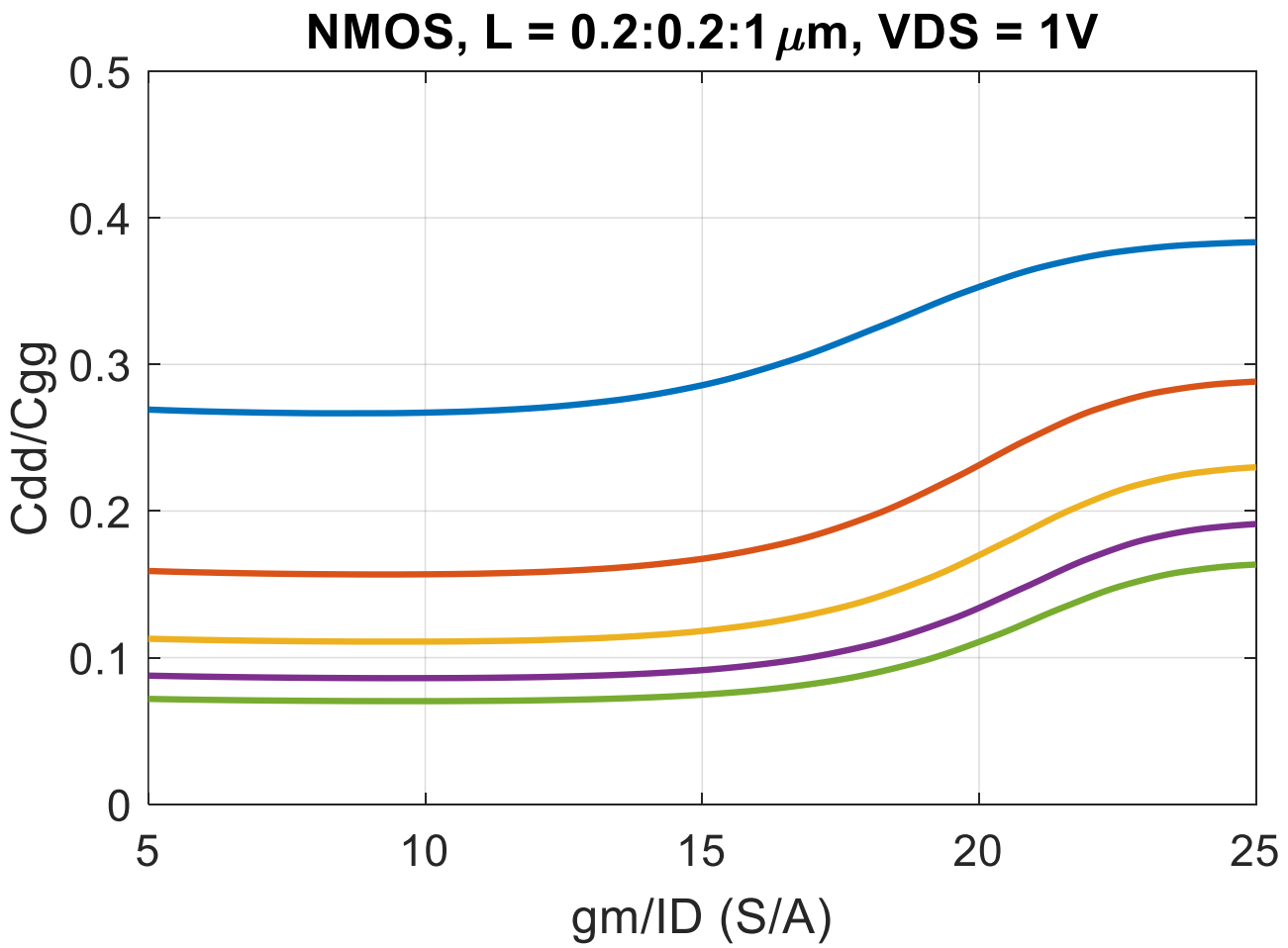
gm/ID Charts: I_D/W



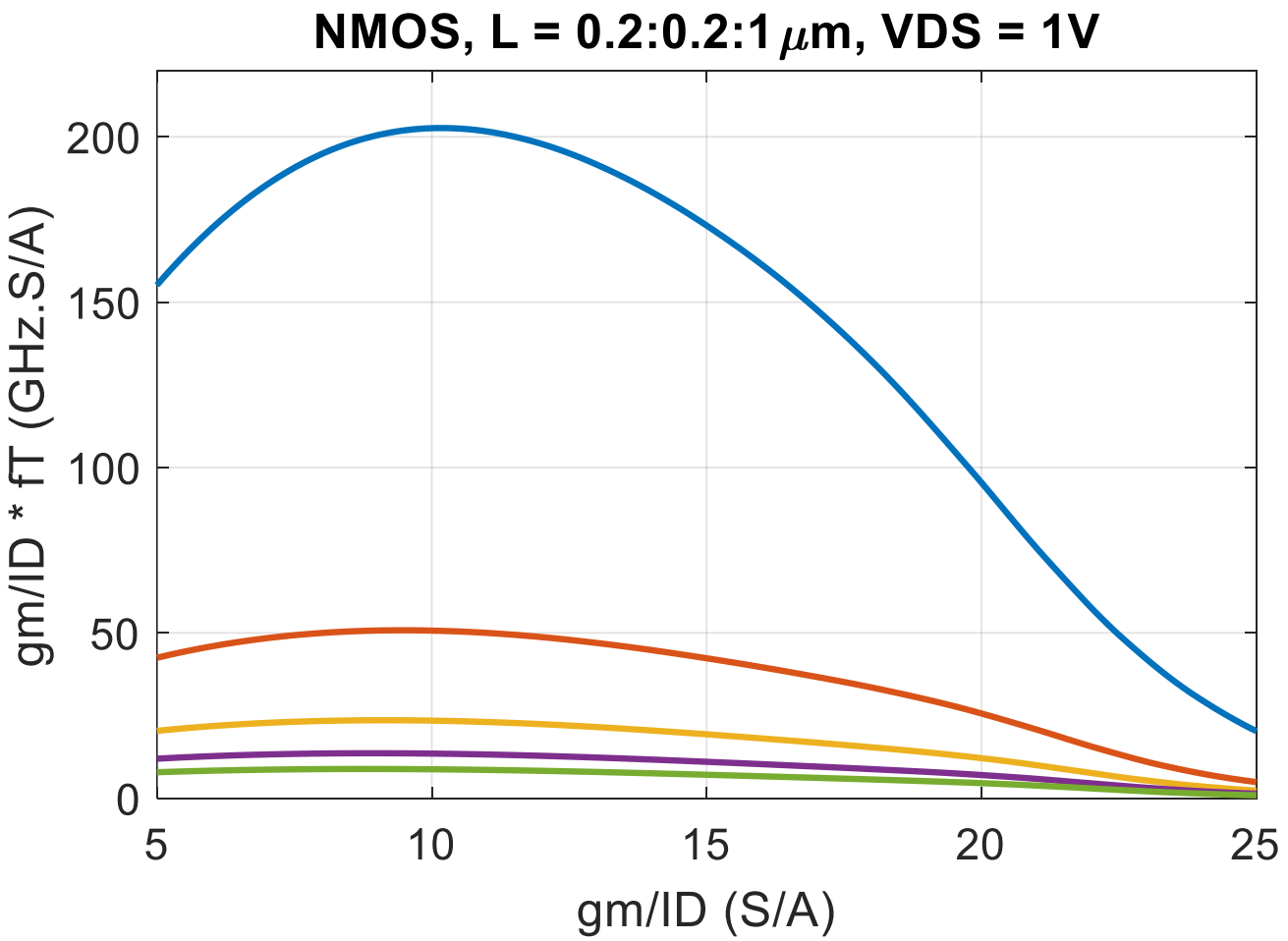
gm/ID Charts: f_T



gm/ID Charts: C_{dd}/C_{gg}



gm/ID Charts: $g_m/I_D \cdot f_T$



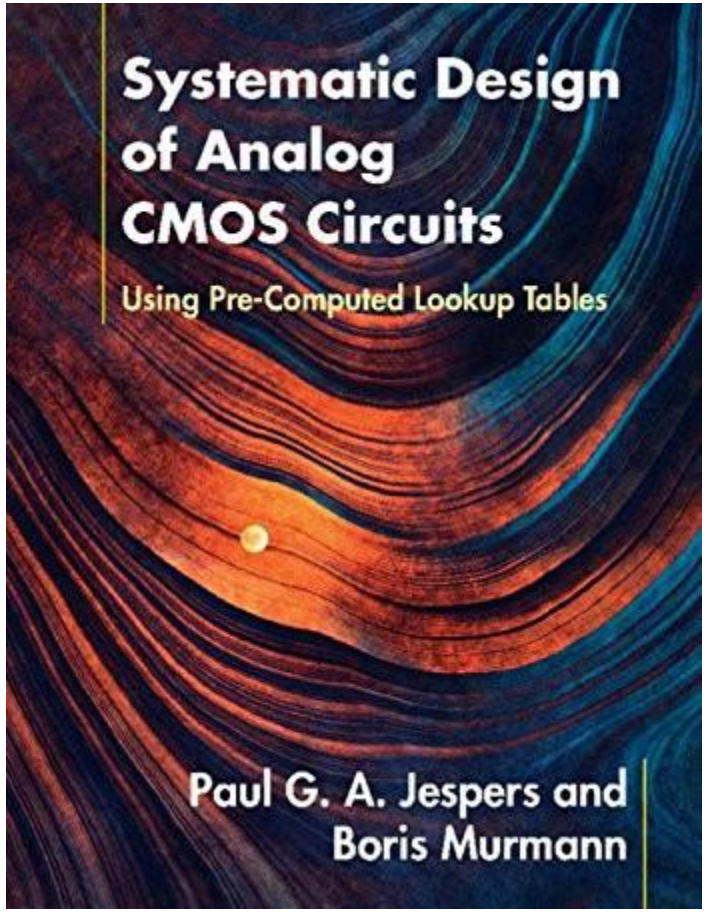
Analog Design Trade-offs

- There are always tradeoffs between gain, speed, and energy efficiency.
- The design knobs to control the tradeoffs: gm/ID and L.
- Choice of gm/ID
  - Large gm/ID: high efficiency (low power), large swing (low V*), high gain (low V*)
  - Small gm/ID: high speed, small area
- Choice of L
  - Long L: high r_o, good matching, low flicker noise (more later)
  - Short L: high speed, small area
- Finding the best compromise for design tradeoffs given required specs is your job as a designer.

Thank you!

References (1/3)

- P. Jespers and B. Murmann, Systematic Design of Analog CMOS Circuits Using Pre-Computed Lookup Tables, Cambridge University Press, 2017.



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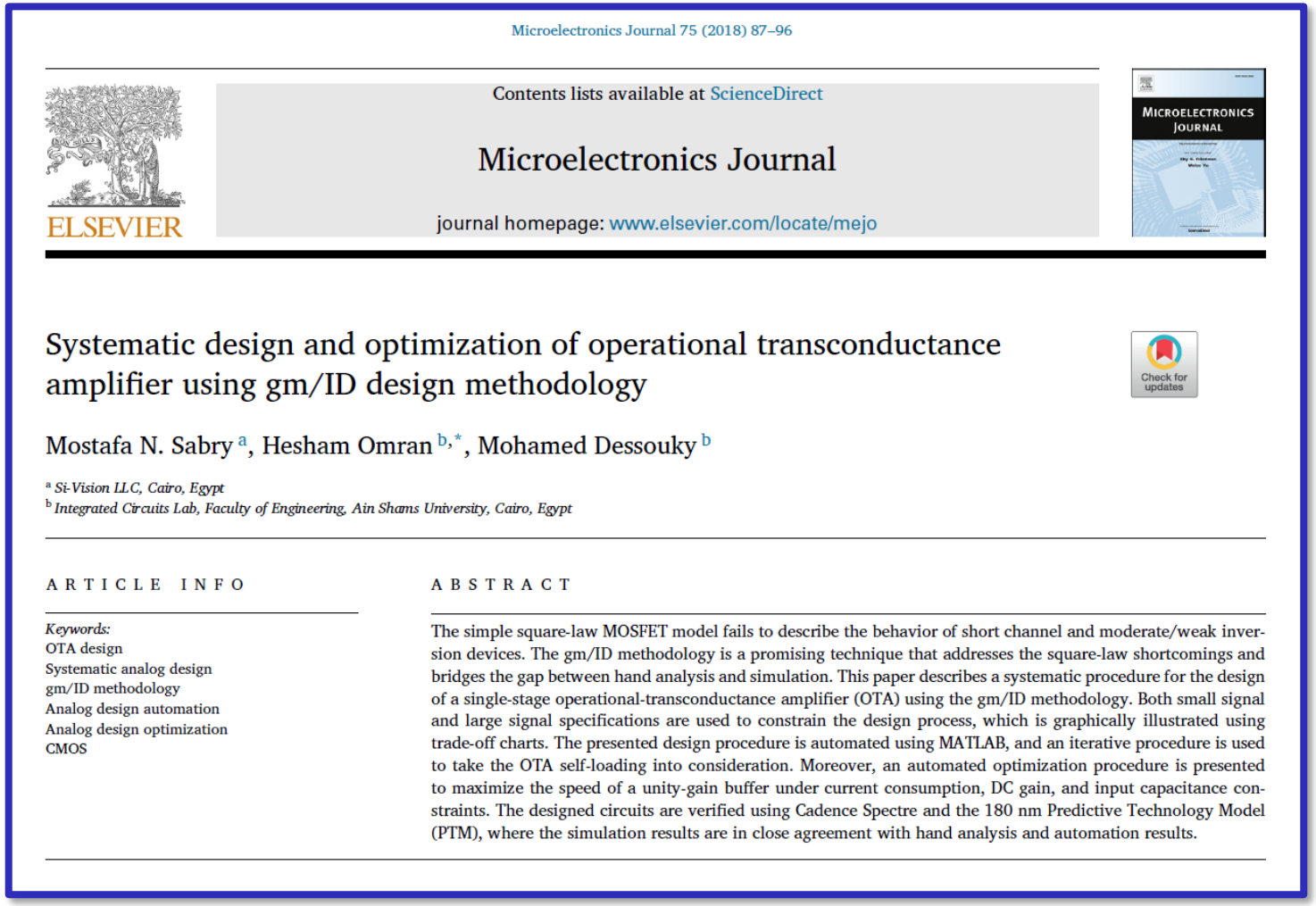
- M. N. Sabry, H. Omran and M. Dessouky, "Systematic design and optimization of operational transconductance amplifier using gm/ID design methodology," *Microelectronics Journal,* vol. 75, pp. 87-96, May 2018.



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Systematic design and optimization of operational transconductance amplifier using gm/ID design methodology

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ABSTRACT

The simple square-law MOSFET model fails to describe the behavior of short channel and moderate/weak inversion devices. The gm/ID methodology is a promising technique that addresses the square-law shortcomings and bridges the gap between hand analysis and simulation. This paper describes a systematic procedure for the design of a single-stage operational-transconductance amplifier (OTA) using the gm/ID methodology. Both small signal and large signal specifications are used to constrain the design process, which is graphically illustrated using trade-off charts. The presented design procedure is automated using MATLAB, and an iterative procedure is used to take the OTA self-loading into consideration. Moreover, an automated optimization procedure is presented to maximize the speed of a unity-gain buffer under current consumption, DC gain, and input capacitance constraints. The designed circuits are verified using Cadence Spectre and the 180 nm Predictive Technology Model (PTM), where the simulation results are in close agreement with hand analysis and automation results.

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