وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

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Analog IC Design (Xschem, Ngspice, ADT)
Lab 02
Common Source Amplifier

Intended Learning Objectives

In this lab you will:

- Design and simulate a common-source amplifier.
- Learn how to plot and use design charts.
- Investigate gain non-linearity; the variation of the gain with input signal amplitude.
- Study the maximum gain attainable for a resistive-loaded CS amplifier and the effect of supply scaling on max gain.
- Learn how to use feedback to reduce non-linearity (gain linearization).

PART 1: Sizing Chart

1) We would like to design a resistive loaded CS amplifier that meets the specifications below. The design process involves selecting the sizing of the transistor (W and L) and the resistive load (R_D).

Spec	Value
DC Gain	-10
Supply	$2.5V$
Current consumption	$10\mu A$

2) First, we want to check if the gain spec is feasible. We can show that the gain is given by

$$|A_v| \approx g_m R_D = \frac{2I_D}{V_{ov}} \times R_D = \frac{2V_{R_D}}{V_{ov}}$$

Interestingly, although the gain equals $g_m R_D$, it actually does not depend on R_D itself, but on the voltage drop across it $V_{R_D} = I_D \times R_D$. The gain depends on the ratio of V_{R_D} and V_{ov}. The choice of V_{R_D} is constrained by the output signal swing. Since we usually want to provide large output swing, we choose the common-mode (CM) output level (DC output level) close to $V_{DD}/2$. Thus, although increasing V_{R_D} increases the gain, but the choice is limited by the supply voltage which is aggressively scaled down in modern technologies. That's one reason it is difficult to get high gain in modern technologies.

Assume $V_{R_D} = 1V$, then to get $|A_v| = 10$ we need $V_{ov} = 0.2V$ which is a reasonable value. Thus, we deduce that the required gain spec is feasible.

3) To derive the gain expression we used $g_m = \frac{2I_D}{V_{ov}}$ which is based on the square-law. For a real MOSFET, if we compute V_{ov} and $\frac{2I_D}{g_m}$ they will not be equal. Let's define a new parameter called V-star (V^*) which is calculated from actual simulation data using the formula

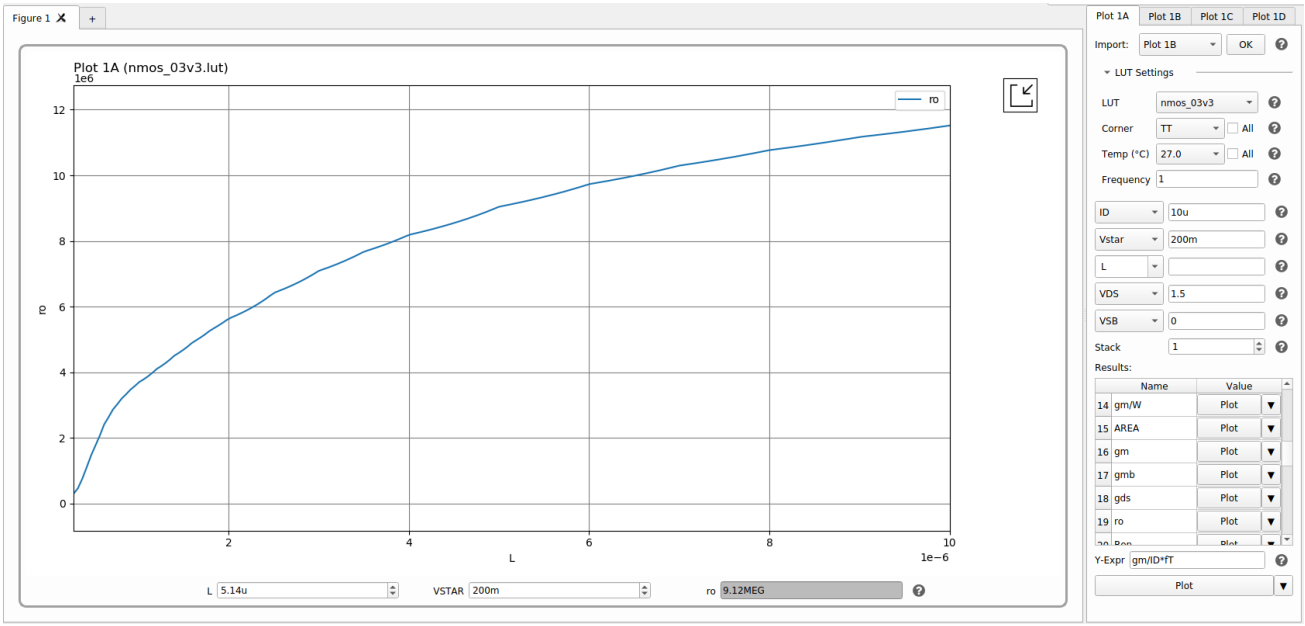
$$V^* = \frac{2I_D}{g_m} \leftrightarrow g_m = \frac{2I_D}{V^*}$$

For a square-law device, $V^* = V_{ov}$, however, for a real MOSFET they are not equal. The actual gain is now given by

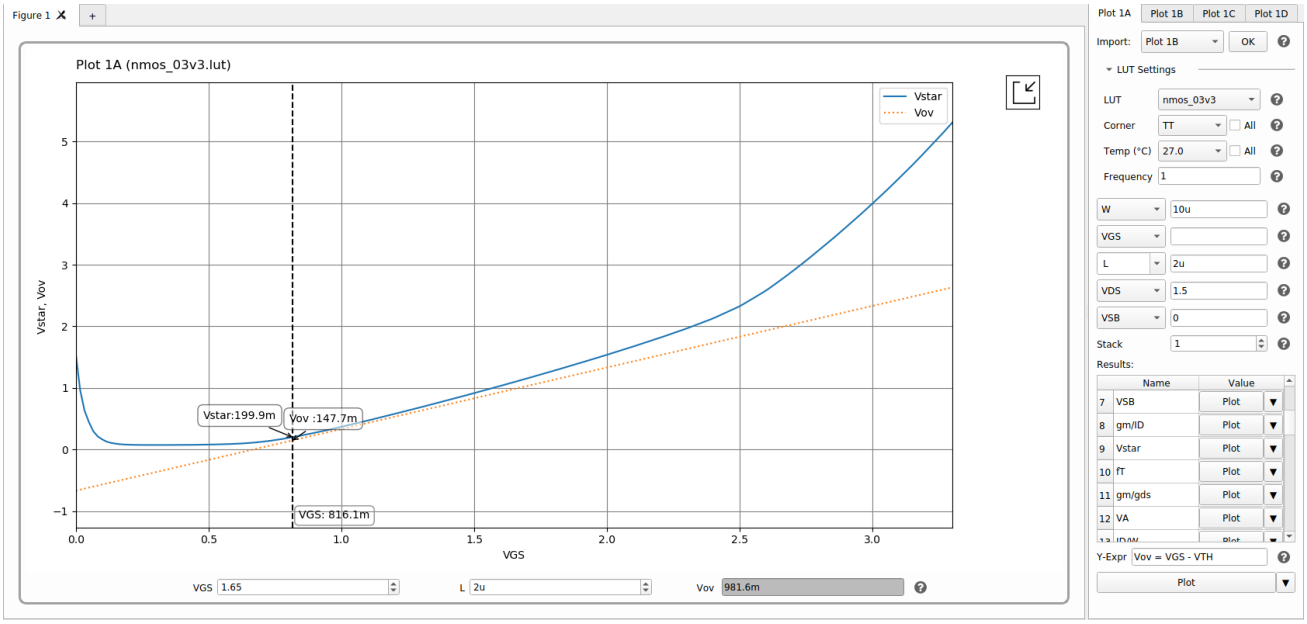
$$|A_v| \approx \frac{2V_{R_D}}{V^*}$$

Given A_v and V_{R_D}, calculate the required V^* (again note that $V^* \neq V_{ov}$ for a real MOSFET). Let's name this value V_Q^*.

4) The first design decision is to choose L. Since there is no spec on bandwidth (speed), we may choose a relatively long L to provide large r_o, i.e., $r_o \gg R_D \rightarrow r_o \geq 10R_D$. Note that r_o appears in parallel with R_D. Assume we will choose relatively long $L = 2\mu m$. We can also use the Sizing Assistant to visualize ro vs L to make sure our L is reasonable.



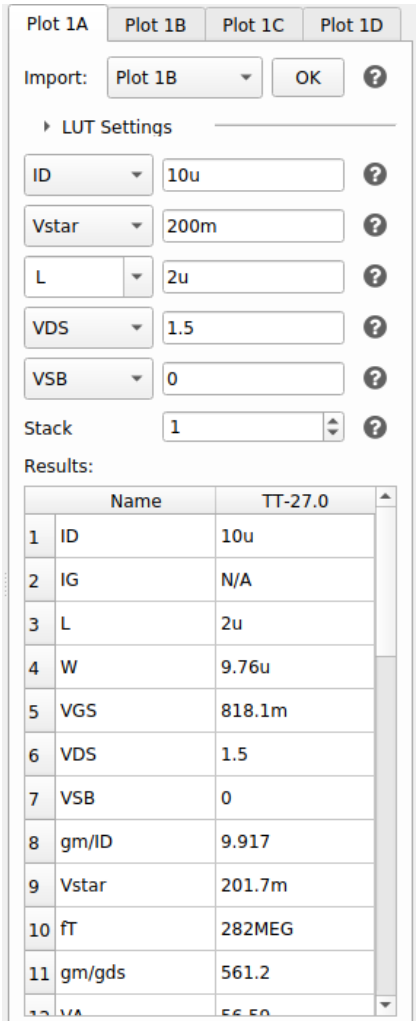
5) The remaining variable in the design is to calculate W. Since the square-law is not accurate, we cannot use it to determine the sizing. Instead, we will use a sizing chart generated from simulation. The Sizing Assistant can be used to plot the sizing charts.
6) Use ADT to compare $V^* = 2I_D/g_m$ and $V_{ov} = V_{GS} - V_{TH}$ by plotting them overlaid. Sweep VGS at at $W = 10\mu m, = 2\mu m, and\ V_{DS} = 1.5$. You will notice that at the beginning of the strong inversion region, V^* and V_{ov} are relatively close to each other (i.e., square-law is relatively valid). For deep strong inversion (large V_{ov}: velocity saturation and mobility degradation) or weak inversion (near-threshold and subthreshold operation) the behavior is quite far from the square-law (although we are using $L = 2\mu m$).



7) On the V^* chart locate the point at which $V^* = V_Q^*$. Find the corresponding V_{ovQ} and V_{GSQ}.
8) Plot I_D, g_m, and g_{ds} vs V_{GS} at $W = 10\mu m$. Find their values at V_{GSQ}. Let's name these values I_{DX}, g_{mX}, and g_{dsX}.
9) Now back to the assumption that we made that $W = 10\mu m$. This is not the actual value that we will use for our design. But the good news is that I_D is always proportional to W irrespective of the operating region and the model of the MOSFET (regardless square-law is valid or no). Thus, we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be $I_{DQ} = 100\mu A$ as given in the specs. Calculate W as shown below.

W	I_D
$\mathbf{10\mu m}$	I_{DX} @V_Q^* (from the chart)
?	$I_{DQ} = 10\mu A$ (from the specs)

10) Now we are almost done with the design of the amplifier. Note that g_m is also proportional to W as long as V_{ov} is constant. On the other hand, $r_o = 1/g_{ds}$ is **inversely** proportional to W (I_D) as long as L is constant. Before leaving this part, calculate g_{mQ} and g_{dsQ} using ratio and proportion (cross-multiplication) and double check that $A_v = -g_m(R_D||r_o)$ meet the required gain spec.
11) Instead of doing the cross multiplication manually, ADT can directly compute the device sizing and properties given its electrical parameters. Compare the results from ADT to the values you calculated in a table.

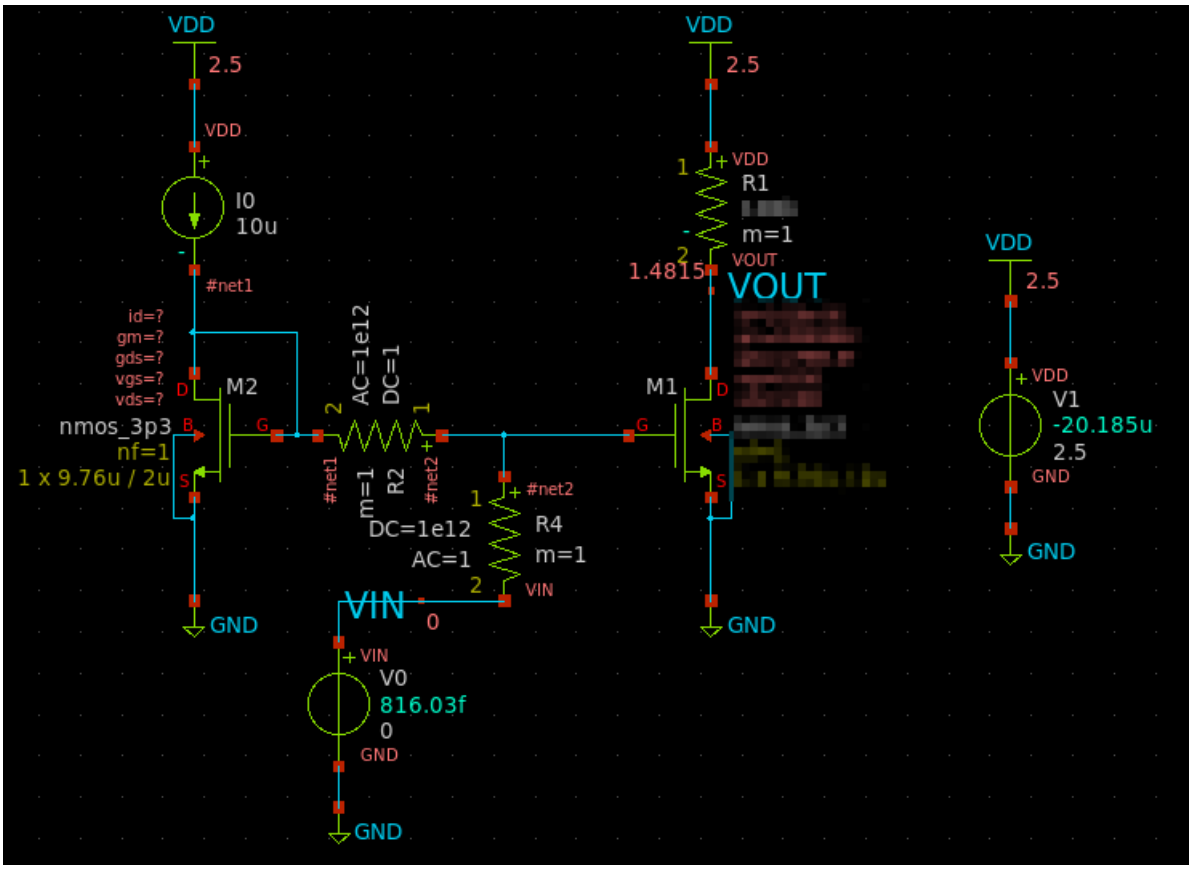


	Name	TT-27.0
1	ID	10u
2	IG	N/A
3	L	2u
4	W	9.76u
5	VGS	818.1m
6	VDS	1.5
7	VSB	0
8	gm/ID	9.917
9	Vstar	201.7m
10	fT	282MEG
11	gm/gds	561.2

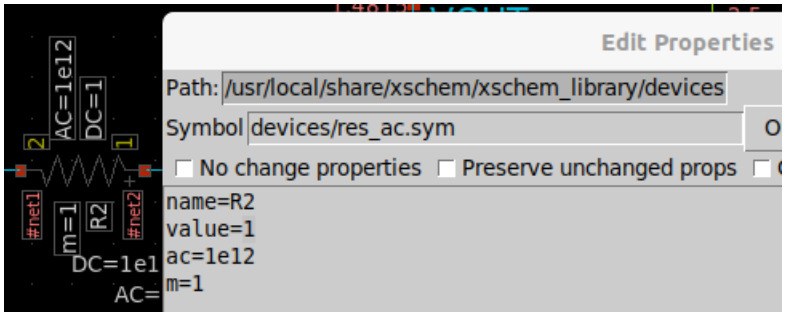
PART 2: CS Amplifier

1. OP Analysis

1) Create a new folder for Lab 02 work. Put the xschemrc initialization file in the new folder.
2) Create a new schematic testbench for the resistive loaded CS amplifier as shown above using the R_D, L, and W that you got from the previous part.



3) In the testbench, note the following:
   - We use replica biasing to generate VGSQ instead of applying it as a voltage source. M2 acts as I-to-V and M1 acts as V-to-I. We usually avoid voltage mode biasing (forcing VGS) in analog design because it will be very sensitive to VTH variations.
   - We use res_ac with different resistance values in DC/AC analysis so that it acts as s.c. or o.c. depending on the simulation type. For DC analysis, M1 gate will be connected to to the replica biasing. For AC analysis, it will be connected to VIN.



4) Simulate the DC OP. An example of a testbench commands to run OP analysis and save the properties of M1 is shown below.
   - ➔ Note: We run SPICE in interactive mode and use an explicit command to write the output raw file.
   - ➔ Note: Inside a .control block, the order of commands matters. A .control block is essentially a script that Ngspice executes sequentially, command by command. We must have the save cmd, then the op cmd, then the write cmd.

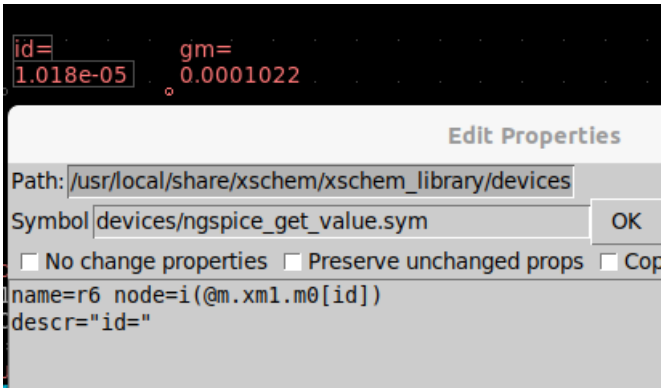
```
.control
```

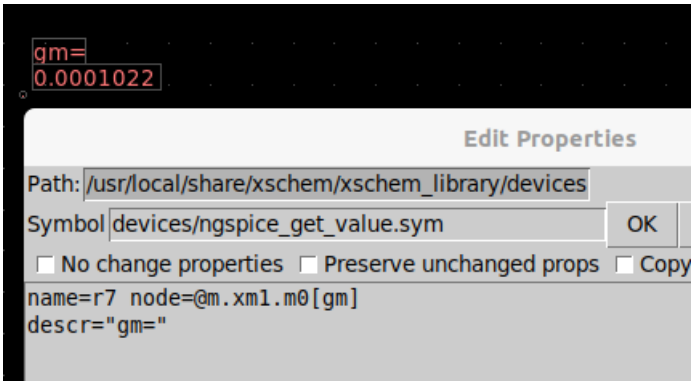
```
save all
save @m.xm1.m0[id]
save @m.xm1.m0[gm]
save @m.xm1.m0[gds]
save @m.xm1.m0[vgs]
save @m.xm1.m0[vds]
op
write lab_02.raw
.endc
```

5) We can use the following commands in SPICE interactive shell to print OP results.

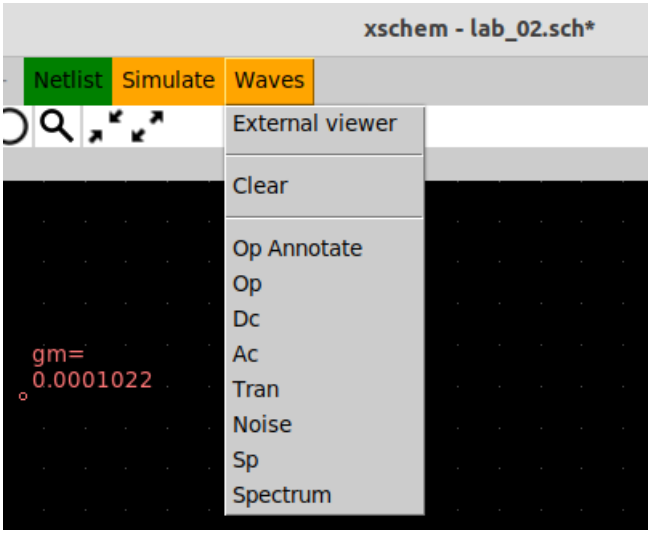
Ngspice command	Description
print all	Prints the voltage at every net
show all	Prints the operating point of all devices
print @m.xm1.m0[id]	Prints id for device M1. You can replace "m1" with the instance names of other transistors. You can replace id with other OP parameters.

6) We can also annotate the results in the schematic by using ngspice_get_value as shown in the examples below. Note that i( ) is used for currents and v( ) is used for voltages.

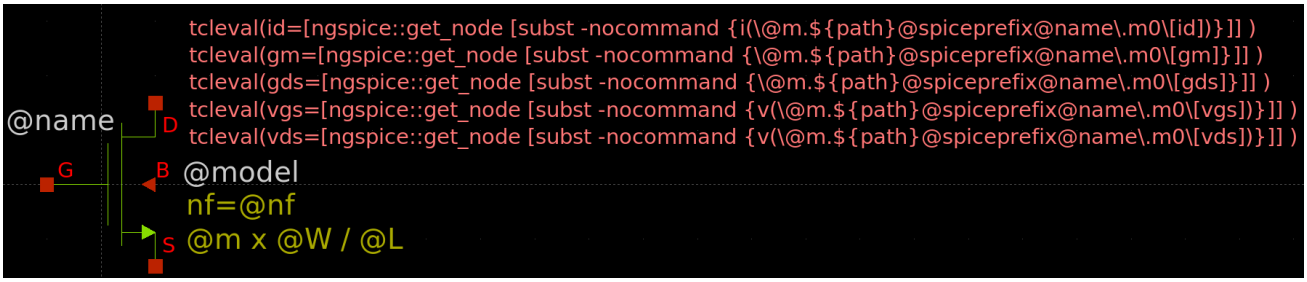




7) Choose Op Annotate from the Waves menu. Browse the sim output raw file.



8) We can also annotate the OP results just next to the device symbol. However we need to edit the symbol first.
   Right click the NMOS symbol -> Descend symbol. Edit the symbol as shown below. Note that i( ) is used for currents and v( ) is used for voltages. Note that each tcleval should be in a dedicated text object.
   ➔ **Note: The PDK should be READ ONLY and we should NEVER EDIT IT. What we do now (editing PDK symbol) is an exception because the default annotation in the symbol is not correct.**

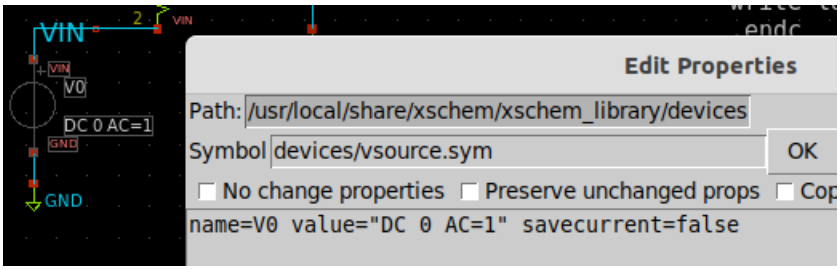



```
tcleval(id=[ngspice::get_node [subst -nocommand {i(\@m.${path}@spiceprefix@name\.m0\[id])}]])
tcleval(gm=[ngspice::get_node [subst -nocommand {\@m.${path}@spiceprefix@name\.m0\[gm]}]])
tcleval(gds=[ngspice::get_node [subst -nocommand {\@m.${path}@spiceprefix@name\.m0\[gds]}]])
tcleval(vgs=[ngspice::get_node [subst -nocommand {v(\@m.${path}@spiceprefix@name\.m0\[vgs])}]])
tcleval(vds=[ngspice::get_node [subst -nocommand {v(\@m.${path}@spiceprefix@name\.m0\[vds])}]])
```

9) Report a snapshot for the key operating point (OP) parameters. Compare the results with the results you obtained in Part 1. Since we used design charts, the results should agree well.
10) Compare r_o and R_D. Is the assumption of ignoring r_o justified in this case? Do you expect the error to remain the same if we use min L?
11) Calculate the intrinsic gain of the transistor.
12) Calculate the amplifier gain analytically. What is the relation ($\ll, <, \approx, >, \gg$) between the amplifier gain and the intrinsic gain?

2. AC Analysis

1) Create a new simulation configuration and run AC analysis (from 1Hz to 1GHz).

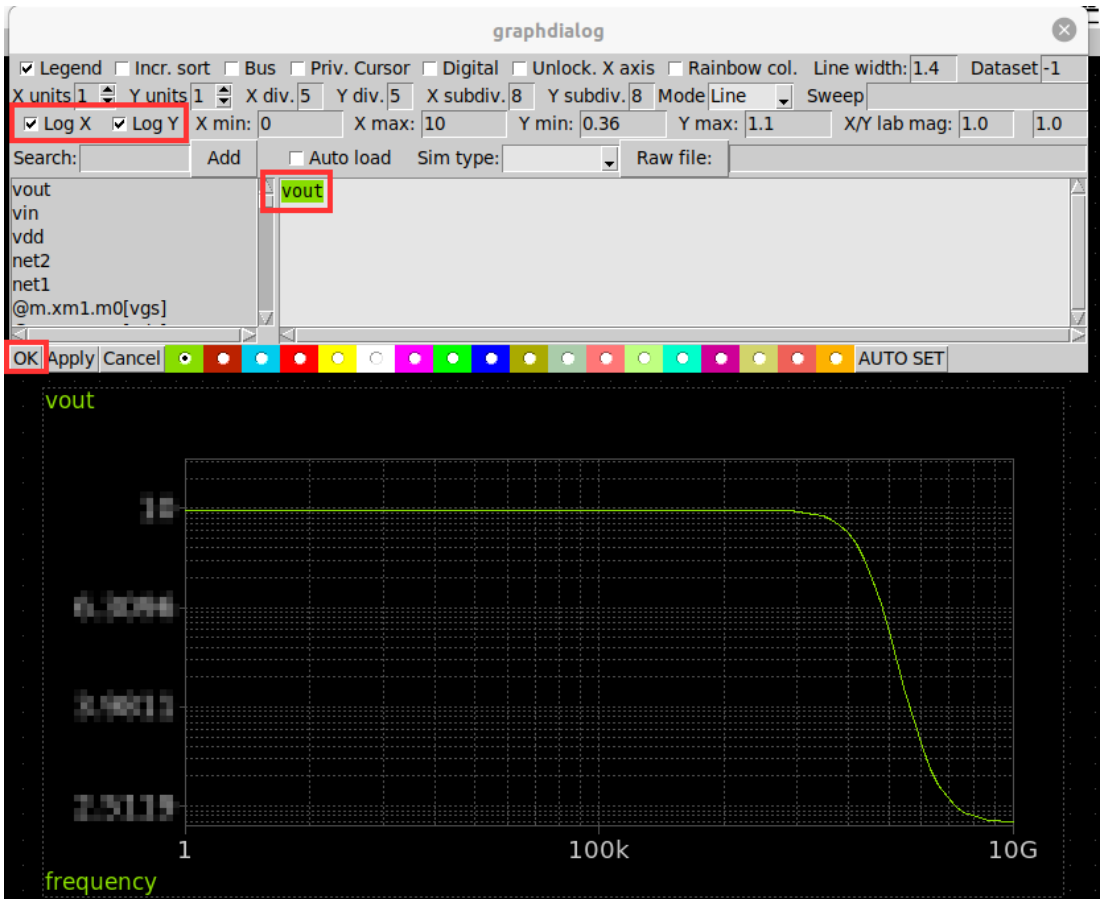



```
.control
save all
save @m.xm1.m0[id]
save @m.xm1.m0[gm]
save @m.xm1.m0[gds]
save @m.xm1.m0[vgs]
save @m.xm1.m0[vds]
*op
ac dec 10 1 10g
remzerovec
write lab_02.raw
.endc
```

2) You can use interactive spice commands to plot the gain magnitude or in dB.

```
plot mag(vout)
plot vdb(vout)
```

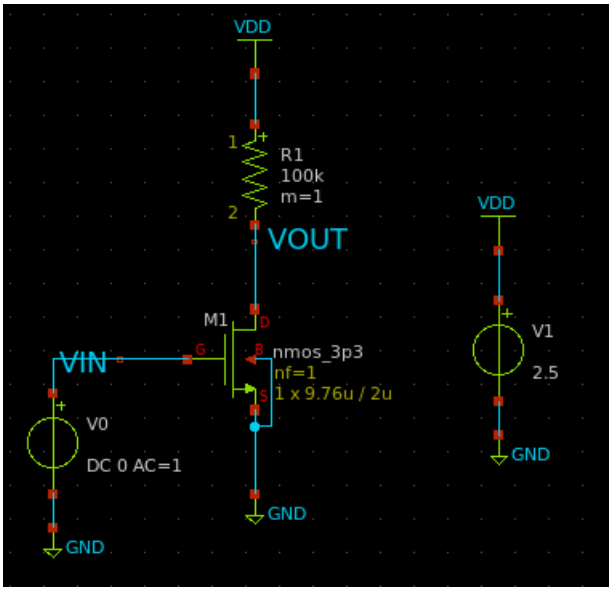
3) Alternatively, use the waveform graph to plot the results.



4) Report the gain vs frequency. Annotate the DC gain (use the a cursor by pressing a). and make sure it meets the spec.

3. Gain Non-Linearity (Large Signal Operation DC Sweep)

1) Copy your schematic to a new file lab_02_dc.sch.
2) Change the testbench to perform large signal input sweep. Here we want the DC input to be directly applied to the amplifier input.



3) Perform a DC sweep for the input voltage from 0 to V_{DD} with 10mV step.

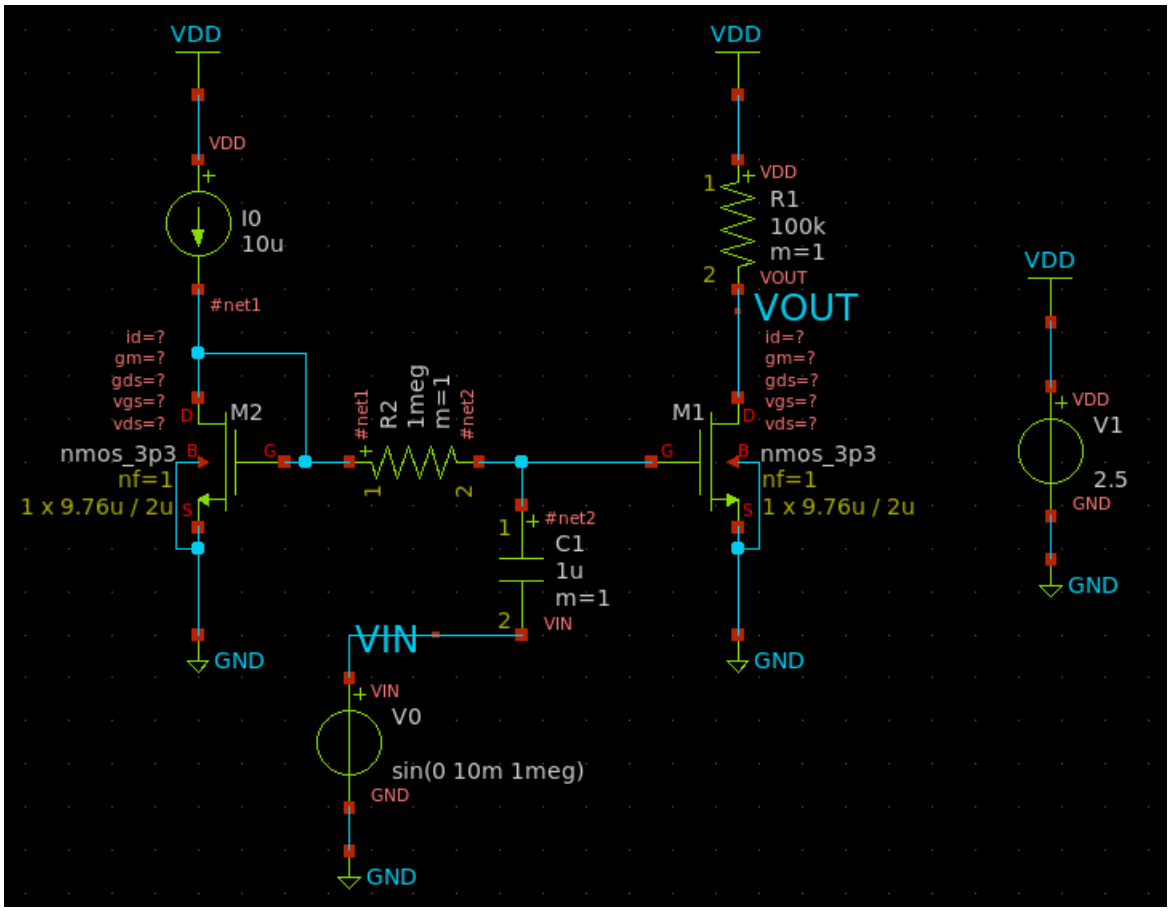
```
.control
save all
save @m.xm1.m0[id]
save @m.xm1.m0[gm]
save @m.xm1.m0[gds]
save @m.xm1.m0[vgs]
save @m.xm1.m0[vds]
*op
*ac dec 10 1 10g
dc V0 0 2.5 10m
remzerovec
write lab_02_dc.raw
```

4) Report VOUT vs VIN. Is the relation linear? Why?
5) Calculate the derivative of VOUT. Plot the derivative vs VIN. The derivative is itself the small signal gain. Is the gain linear (independent of the input, i.e., constant vs VIN)? Why?
   - ➔ Xschem: Use “vout deriv()” in the waveform graph to calculate the derivative.
   - ➔ Xschem: Use the a-cursor to annotate the OP point (gain = -10) in the reported graphs.

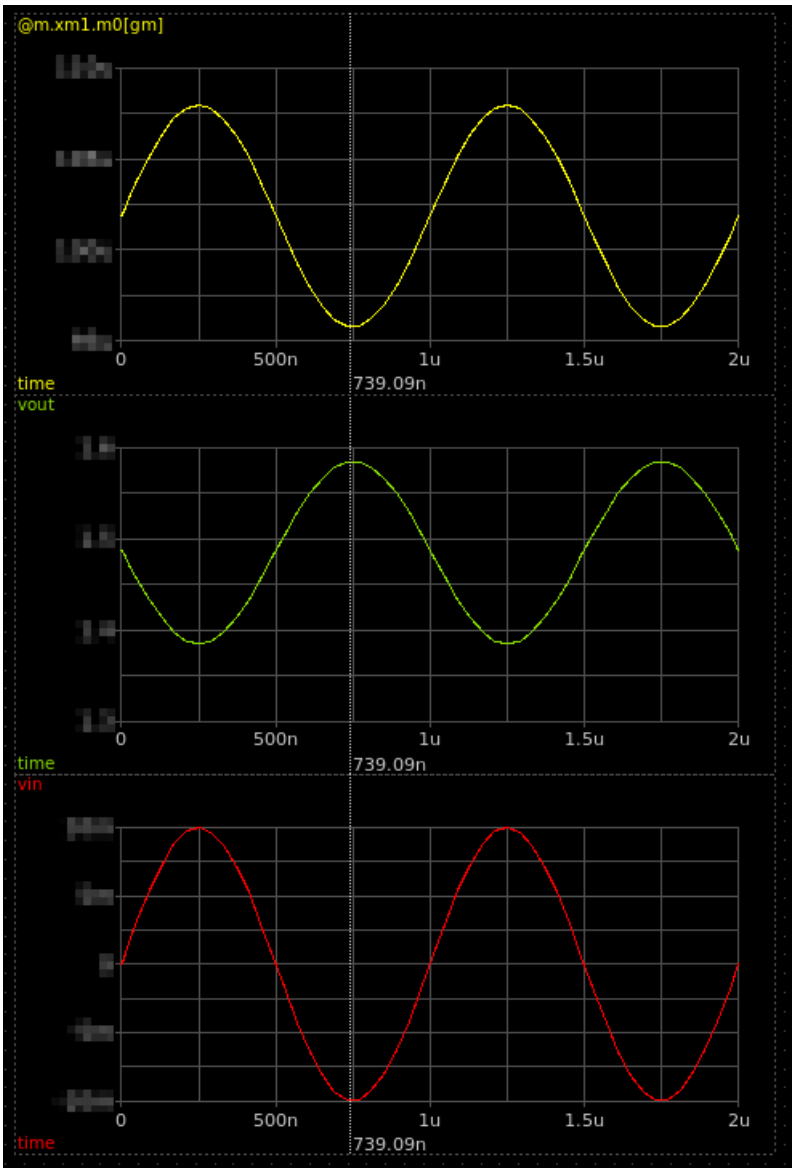
4. Gain Non-Linearity (Transient Analysis)

1) Copy the replica biasing schematic to a new file lab_02_tran.sch.
2) Change the schematic to apply a transient signal. We use a large resistance as an RF choke (RFC), i.e., to pass the DC biasing but block the AC signal. We also use a large capacitor to couple the input signal to the amplifier. This scheme is common in RF circuits, but the capacitor value needs to be in

the pF range to be integrated on-chip. The pF cap will act as AC short circuit if the input is in the GHz range.



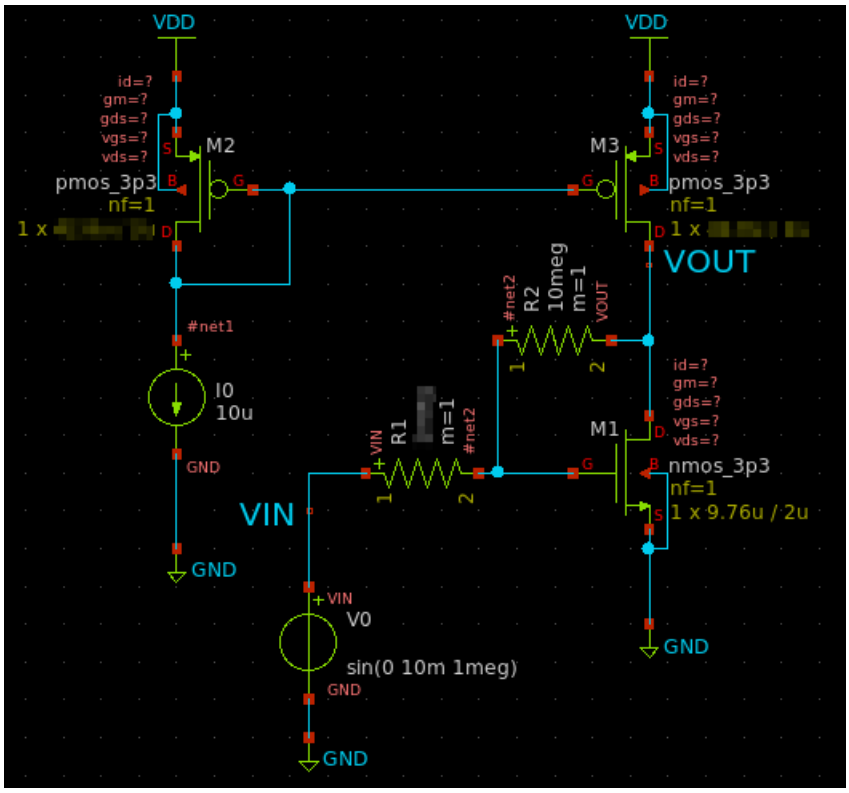
3) Set the properties of the voltage source to apply a transient stimulus (sine wave of 1MHz frequency and 10mV amplitude).
   sin(0 10m 1meg)
4) Create a new simulation configuration. Run transient simulation for two periods.
   .control
   save all
   save @m.xm1.m0[id]
   save @m.xm1.m0[gm]
   save @m.xm1.m0[gds]
   save @m.xm1.m0[vgs]
   save @m.xm1.m0[vds]
   *op
   *ac dec 10 1 10g
   tran 0.1u 2u
   remzerovec
   write lab_02_tran.raw
5) Report vin, vout, and gm vs time.



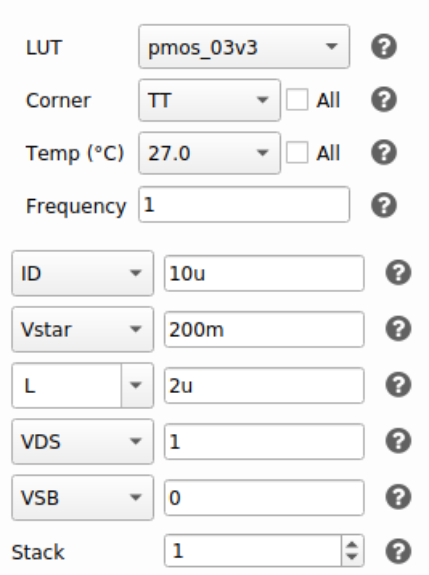
6) Does gm vary with the input signal? What does that mean? Is this amplifier linear? Comment.
   ➔ Xschem: You can annotate OP and use the b-cursor to show how the OP parameters vary with time.

5. Gain Linearization (Negative Feedback)

1) Copy the replica biasing schematic to a new file lab_02_feedback.sch.
2) Replace the resistive load with a PMOS current source (active load) as shown below.



3) From ADT find the sizing of the PMOS device. Note that the PMOS load must have the same bias current as the NMOS input device.

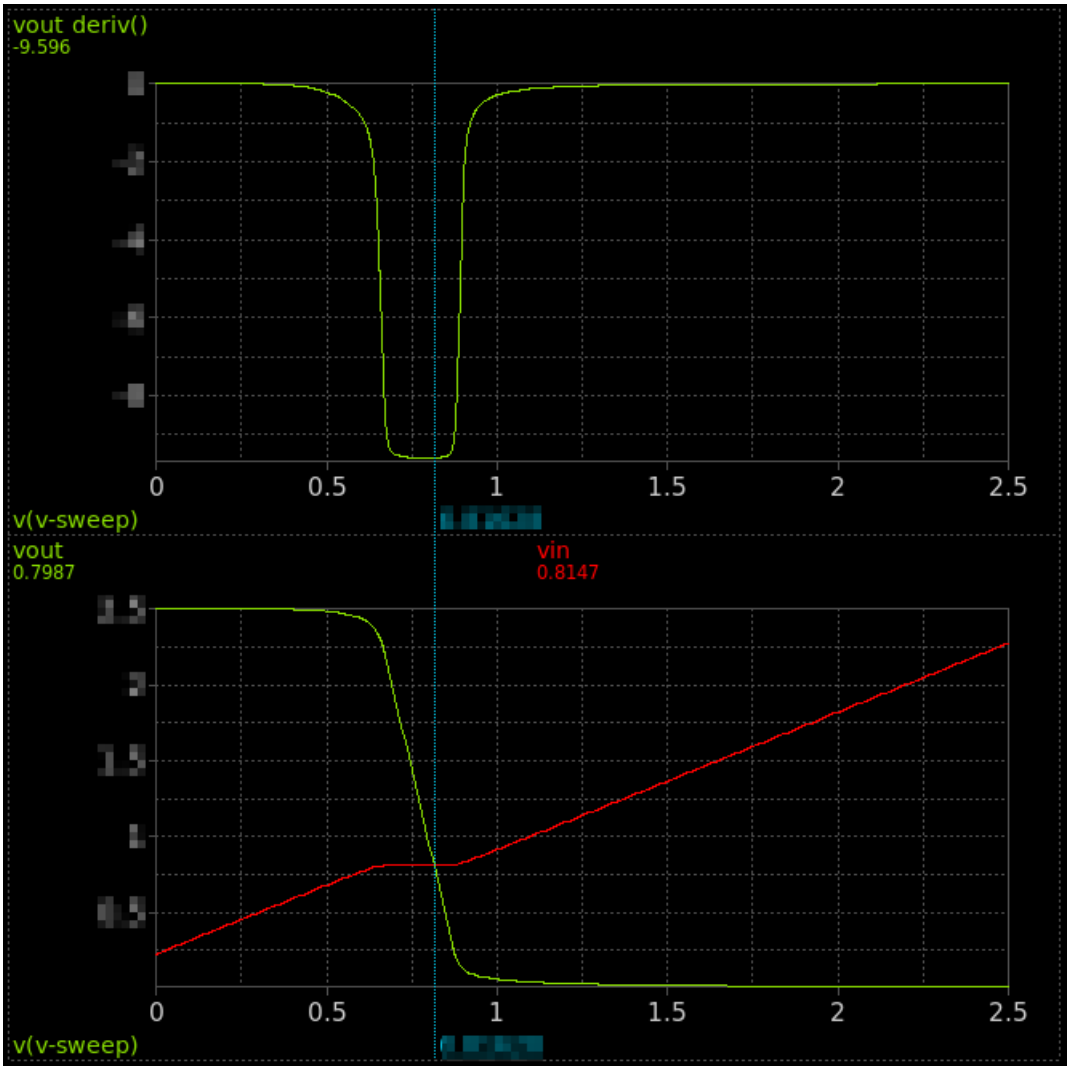


4) Add two resistors: the feedback resistor (R_f) should be larger than Rout to avoid reducing the amplifier open-loop gain, so we choose 10meg. Choose R_{in} to give a voltage gain approximately equal to $R_f/R_{in} = |A_v|$ as given in the specs.
5) Perform a DC sweep for the input voltage from 0 to V_{DD} with 10mV step.

```
.control
save all
save @m.xm1.m0[id]
save @m.xm1.m0[gm]
save @m.xm1.m0[gds]
```

```
save @m.xm1.m0[vgs]
save @m.xm1.m0[vds]
*op
*ac dec 10 1 10g
*tran 0.1u 2u
dc V0 0 2.5 10m
remzerovec
write lab_02_feedback.raw
.endc
```

6) Report VIN and VOUT vs VSIG (overlaid). At what voltage do the two curves cross? Why?
   ➔ Hint: Compare this voltage to VGS of M1. The quiescent point of the amplifier is itself VGS of M1. At this point VOUT is also equal to VIN because no current flows in the two resistors.
7) Is VOUT vs VSIG linear in the operating range of the amplifier? Why?
8) Report the derivative of VOUT vs VSIG. The derivative is itself the small signal gain. Is the gain linear (independent of the input) in the operating range of the amplifier? Why?



9) VIN is almost constant in the operating range of the amplifier. What is its value? Why?
10) Analytically calculate the DC input range over which the gain is linear. Compare your analysis with the simulation result.

➔ Hint: When VSIG deviates from V_{GS1} current flows and VOUT deviates. The amplifier fails when M1 or M2 gets out of saturation ($V_{DS} < V^*$). You can get the input range by dividing the output range by the gain $\approx \frac{V_{DD}-2V^*}{|A_v|}$.

11) Run a transient simulation and report gm vs time. Compare this plot to the plot you previously obtained from the resistive loaded open-loop amplifier.

Lab Summary

In Part 1 you learned:

- How to plot and use MOSFET design charts.
- How to design a resistive-loaded common-source amplifier.
- How the overdrive voltage of a MOS transistor deviates from the square law in different regions of operation.

In Part 2 you learned:

- How to do AC and DC simulations of a CS amplifier.
- How the gain of an amplifier changes with the input signal variations.
- How to use negative feedback to reduce gain non-linearity.

Acknowledgements

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