Lab 5

Current Mirrors

Part 1: Sizing Chart

Required Spec:

Parameter	
Current direction (source/sink)	Sink
Input Current	$10\mu A$
Output Current	$20\mu A$
% Change in Current for $\Delta Vout = 1V$	< 10%
Percent mismatch: $\sigma(Iout)/Iout$	≤ 2%
Compliance voltage	≤ $150mV$
Area	Minimize

2) Sinking Current Means?

NMOS Transistor

3) Required Lambda

$$I_D = \frac{K}{2} Vov^2 (1 + \lambda V_{DS}) \rightarrow \Delta I_D = \lambda \Delta V_{DS} \rightarrow \lambda = 0.1$$

5) Mismatch from ADT

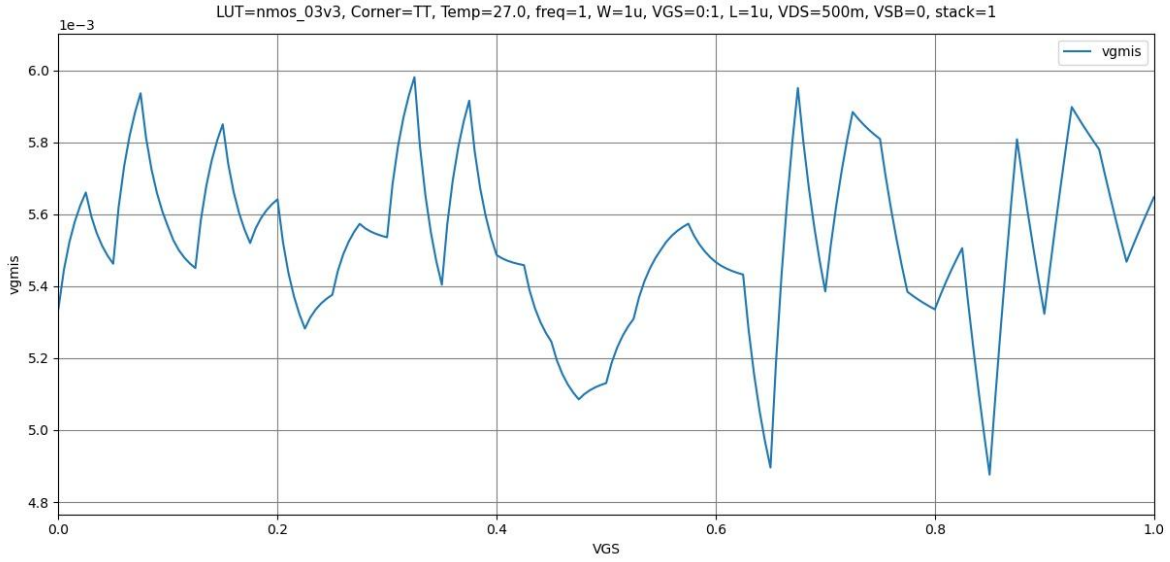


Figure 1 VGMIS vs VGS

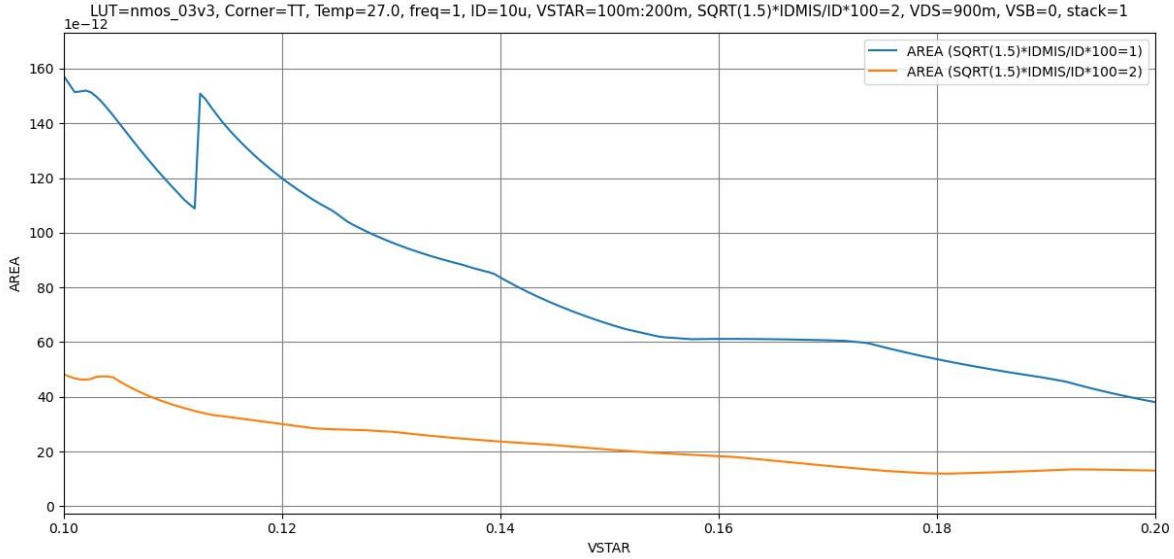
From the graph we can find the approximate value of $\sigma_{VT} \approx 5.4m$

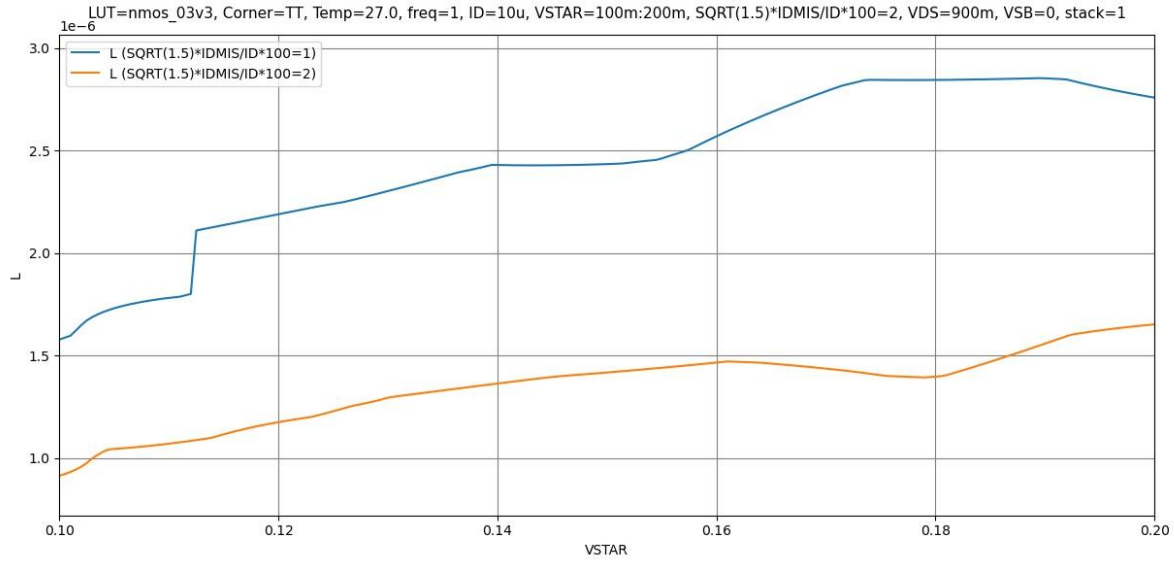
6) Mismatch from PDK

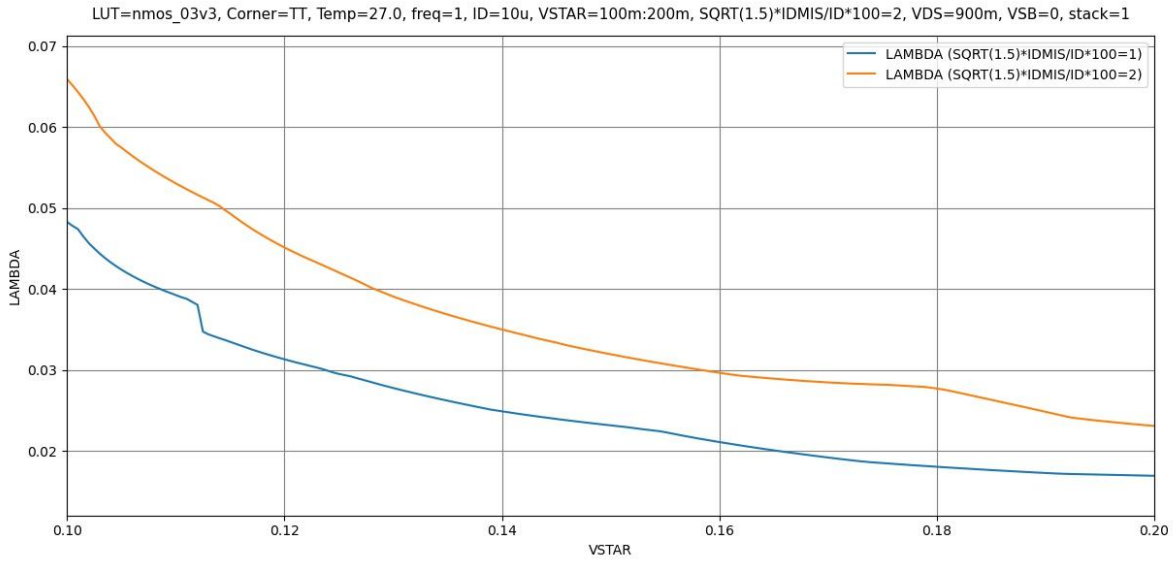
$$var_{vth} = 0.7071 * par_{vth} * \frac{10^{-6}}{\sqrt{WL}} \approx 5.0543m$$

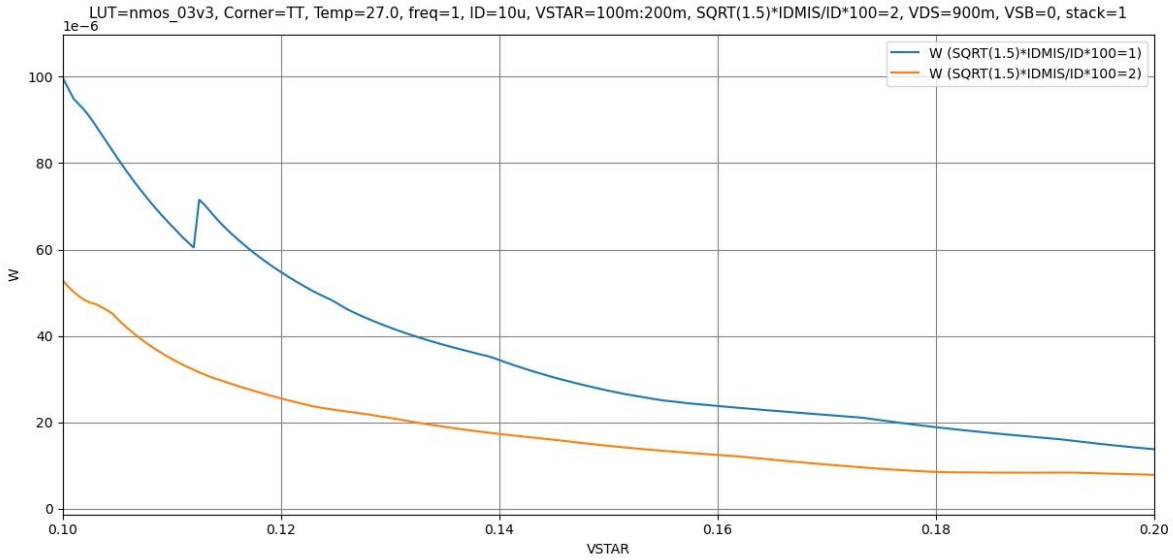
The value from ADT is slightly higher, this is possibly due to inaccuracies that occur when calculating and estimating random values.

7) Design Parameters vs vstar at different mismatch

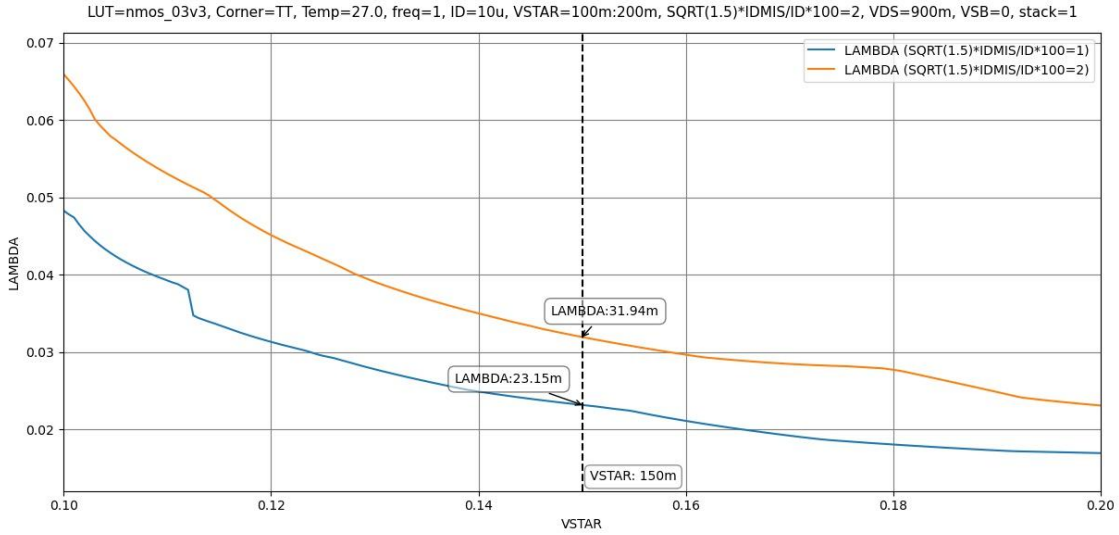


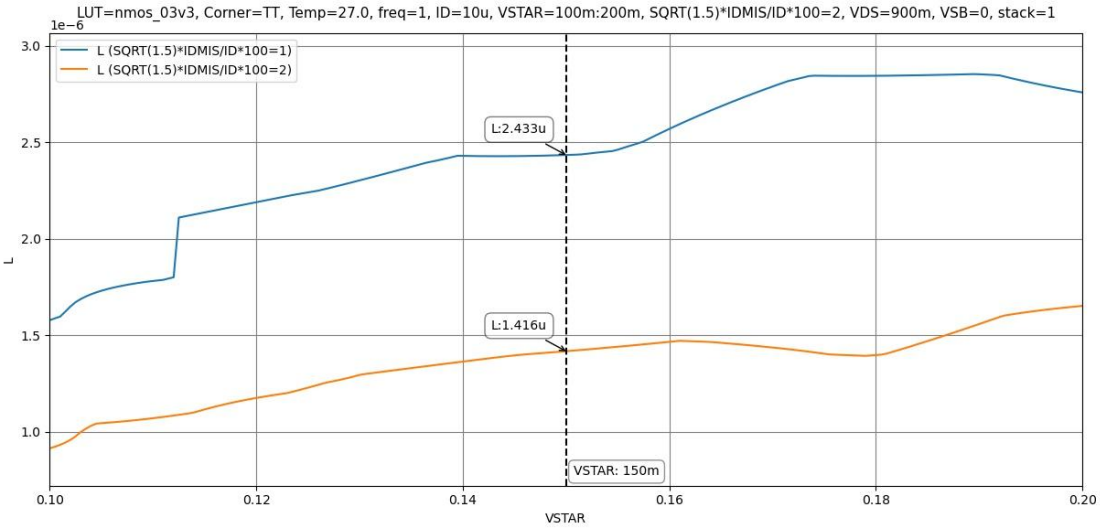


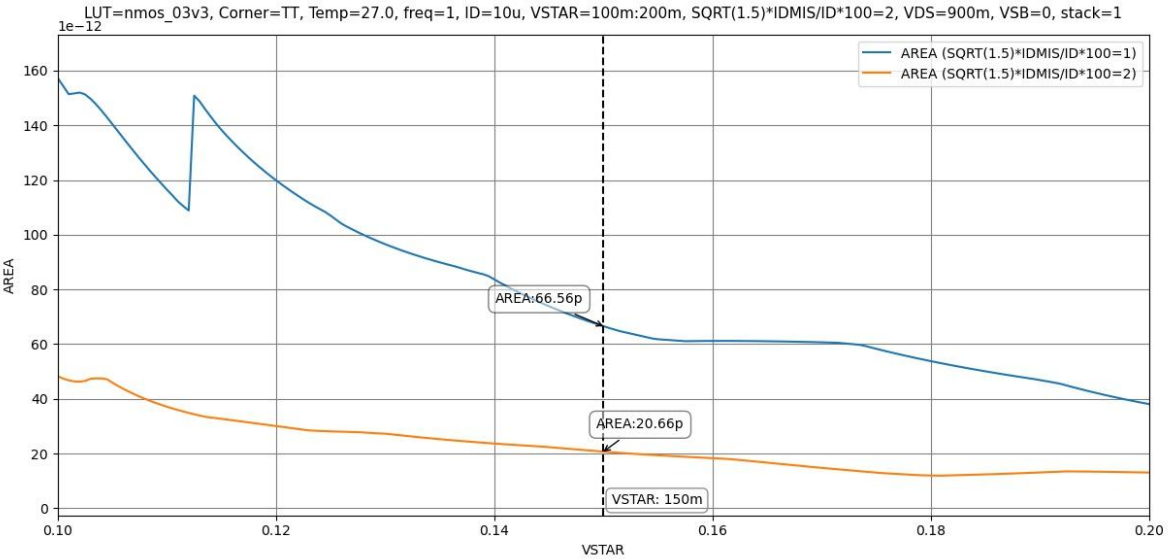


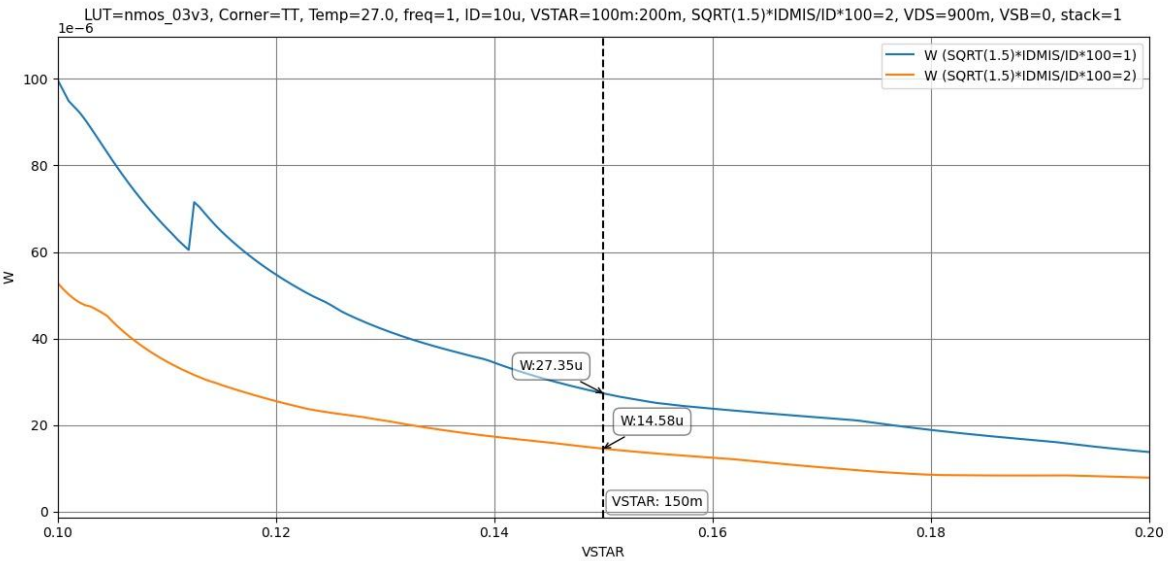


9) Design Parameters at required Vstar




LUT=nmos_03v3, Corner=TT, Temp=27.0, freq=1, ID=10u, VSTAR=100m:200m, SQRT(1.5)*IDMIS/ID*100=2, VDS=900m, VSB=0, stack=1
1e−6
L (SQRT(1.5)*IDMIS/ID*100=1)
L (SQRT(1.5)*IDMIS/ID*100=2)
L:2.433u
L:1.416u
VSTAR: 150m
L
VSTAR


LUT=nmos_03v3, Corner=TT, Temp=27.0, freq=1, ID=10u, VSTAR=100m:200m, SQRT(1.5)*IDMIS/ID*100=2, VDS=900m, VSB=0, stack=1
1e−12
AREA (SQRT(1.5)*IDMIS/ID*100=1)
AREA (SQRT(1.5)*IDMIS/ID*100=2)
AREA:66.56p
AREA:20.66p
VSTAR: 150m
AREA
VSTAR

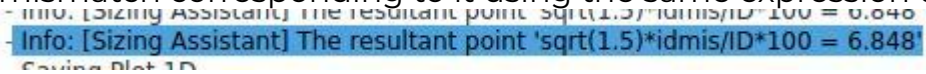

LUT=nmos_03v3, Corner=TT, Temp=27.0, freq=1, ID=10u, VSTAR=100m:200m, SQRT(1.5)*IDMIS/ID*100=2, VDS=900m, VSB=0, stack=1
1e−6
W (SQRT(1.5)*IDMIS/ID*100=1)
W (SQRT(1.5)*IDMIS/ID*100=2)
W:27.35u
W:14.58u
VSTAR: 150m
W
VSTAR

From the Graphs we notice both values of the mismatch current satisfy the Lambda Constraint $\lambda < 0.1$
Thus we will choose the dimensions corresponding with the mismatch value which has the lower area $Mismatch = 2\%$

$$\boldsymbol{L = 1.416\mu m \;\; W = 14.58\mu m}$$

9) What if Lambda constraints is not met?

By inputting the required exact value for lambda ($\lambda = 0.1$) we can calculate the mismatch corresponding to it using the same expression used before.



$$Required\ Mismatch \approx 6.848\%$$

11) Report Device Sizing and Mismatch percentage

Selected design points @ $V^* = 150mV$

$\sigma(I_{out})/I_{out}$	2%
L	1.42um
W	14.58um

Part 2: Current Mirror Simulation

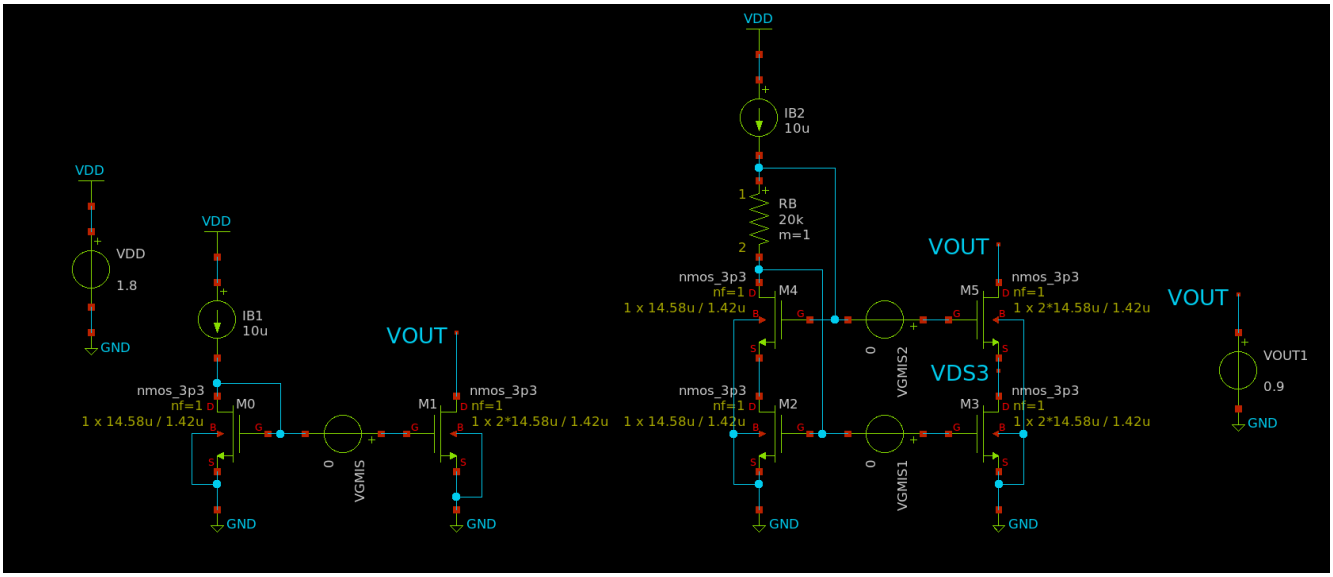


Figure 2 Current Mirror Schematic Testbench

Design and OP Analysis

1. Finding RB analytically

$$R_B = \frac{V_{GS4} + V_{DS2} - V_{GS2}}{I_B} \approx \frac{V_{DS2}}{I_B} = \mathbf{20K\Omega}$$

2. Finding RB through Simulation

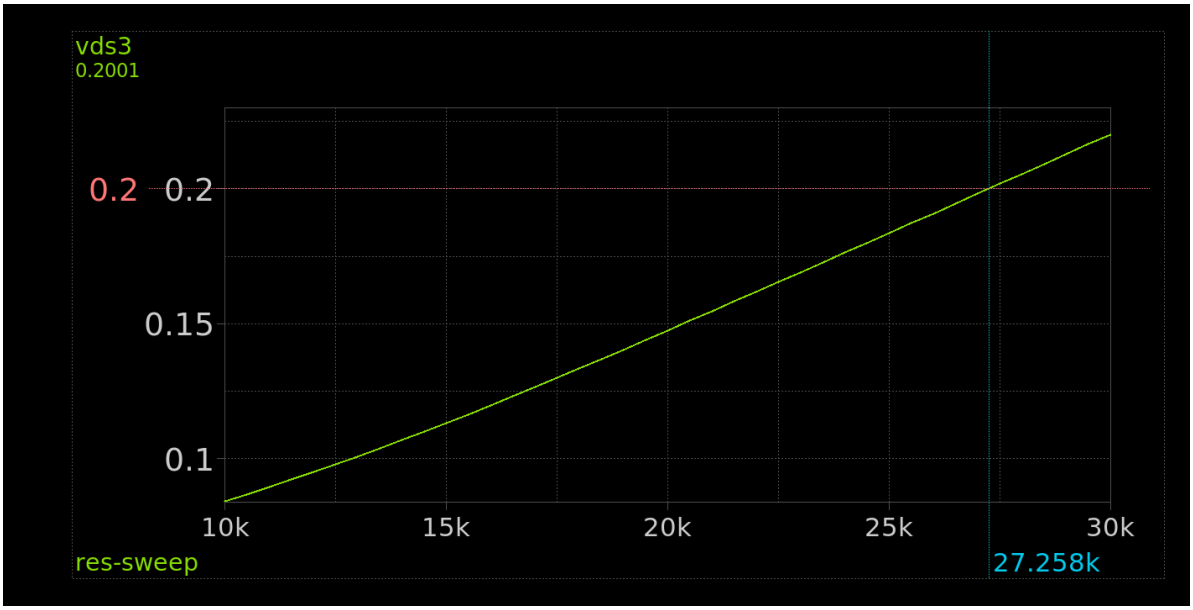


Figure 3 Value of RB from simulation

$$\boldsymbol{R_B = 27.258K\Omega}$$

The value of RB calculated from the simulation is larger than the one calculated analytically, this is due to the analytic solution not accounting for body effect which makes the difference in VGS have a value thus increasing the required RB.

3. OP Analysis

Op Analysis was done using the value of RB from the simulation

	M0	M1	M2	M3	M4	M5
gds	3.28E-07	6.30E-07	1.31E-06	2.60E-06	3.57E-07	6.57E-07
gm	1.34E-04	2.70ES-04	1.33E-04	2.67E-04	1.35E-04	2.69E-04
gmbs	5.24E-05	1.05E-04	5.20E-05	1.04E-04	4.76E-05	9.54E-05
ID	1.00E-05	2.01E-05	1.00E-05	2.00E-05	1.00E-05	2.00E-05
VDS	7.57E-01	9.00E-01	2.00E-01	2.00E-01	5.59E-01	7.00E-01
VDSAT	1.20E-01	1.20E-01	1.21E-01	1.21E-01	1.22E-01	1.22E-01
VGS	7.57E-01	7.57E-01	7.59E-01	7.59E-01	8.32E-01	8.32E-01
VTH	6.78E-01	6.78E-01	6.78E-01	6.78E-01	7.53E-01	7.53E-01

4. Do All Transistor operate in Saturation?

They all operate in saturation.

DC Sweep

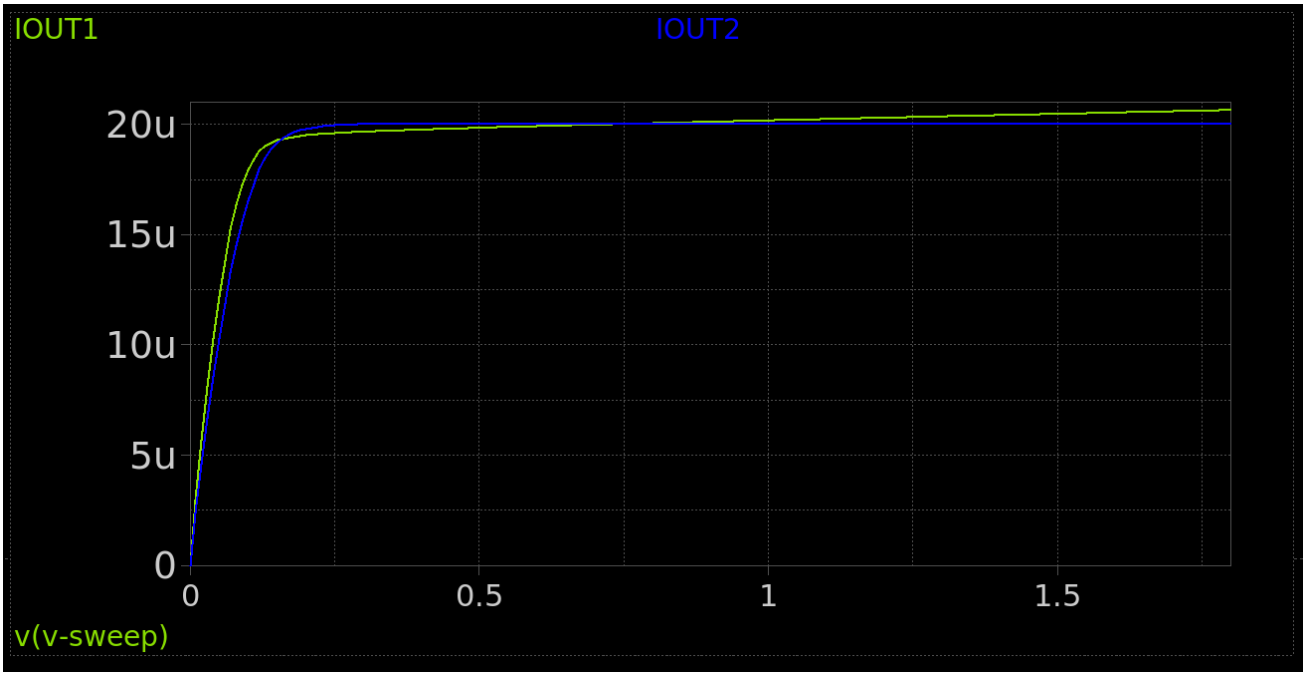


Figure 4 Iout for both CMs vs VOUT

The cascode IOUT is more consistent and always equal to IB*2 almost during the entire sweep, while an evident error is visible in IOUT1 from the simple CM as VDS increases.

Estimate V Compliance

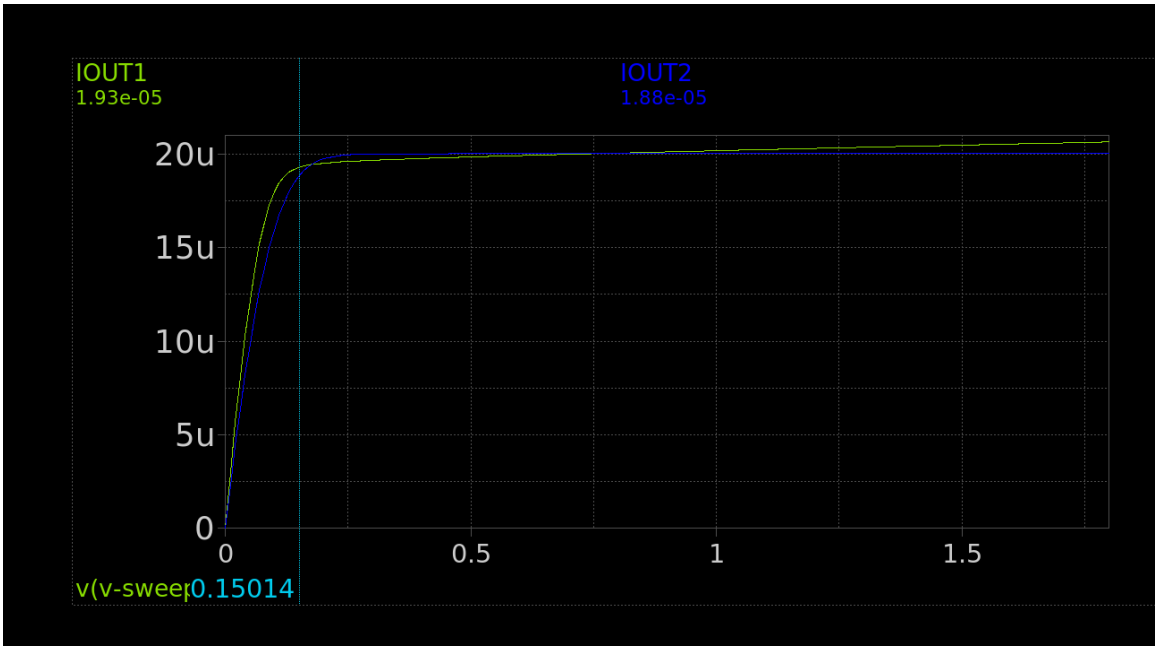


Figure 5 VCOMP of Simple CM

$$V_{comp1} \approx 150mV$$

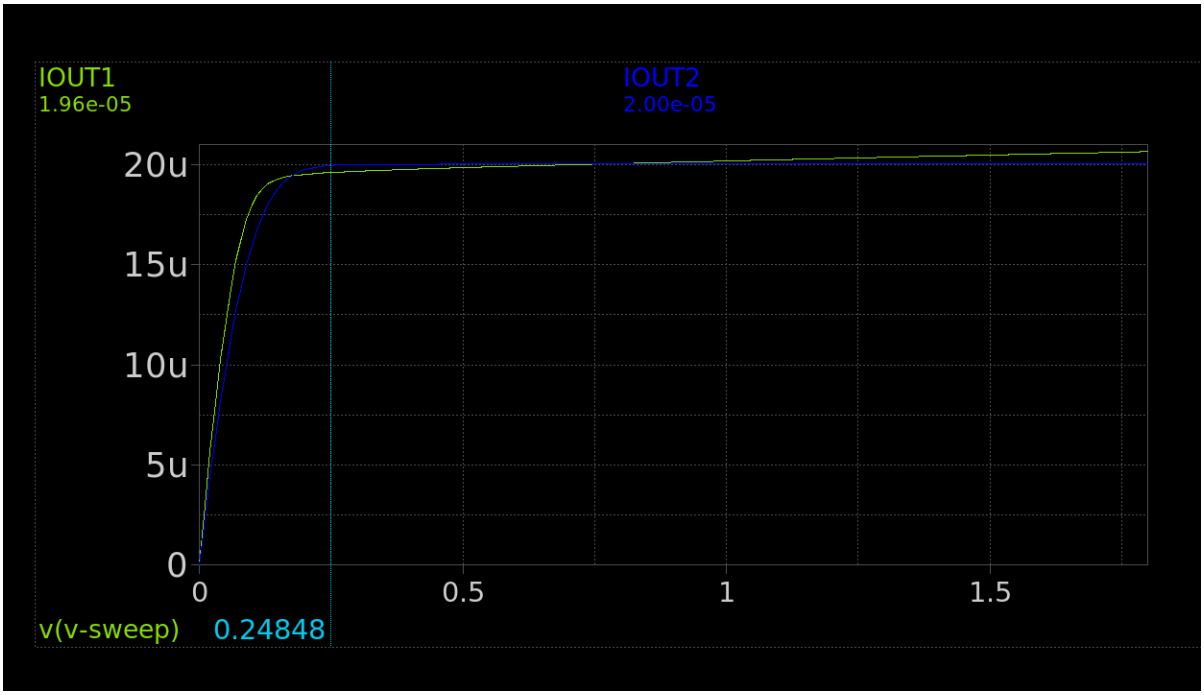


Figure 6 V compliance of Cascode Current Mirror

$$V_{comp2} \approx 250mV$$

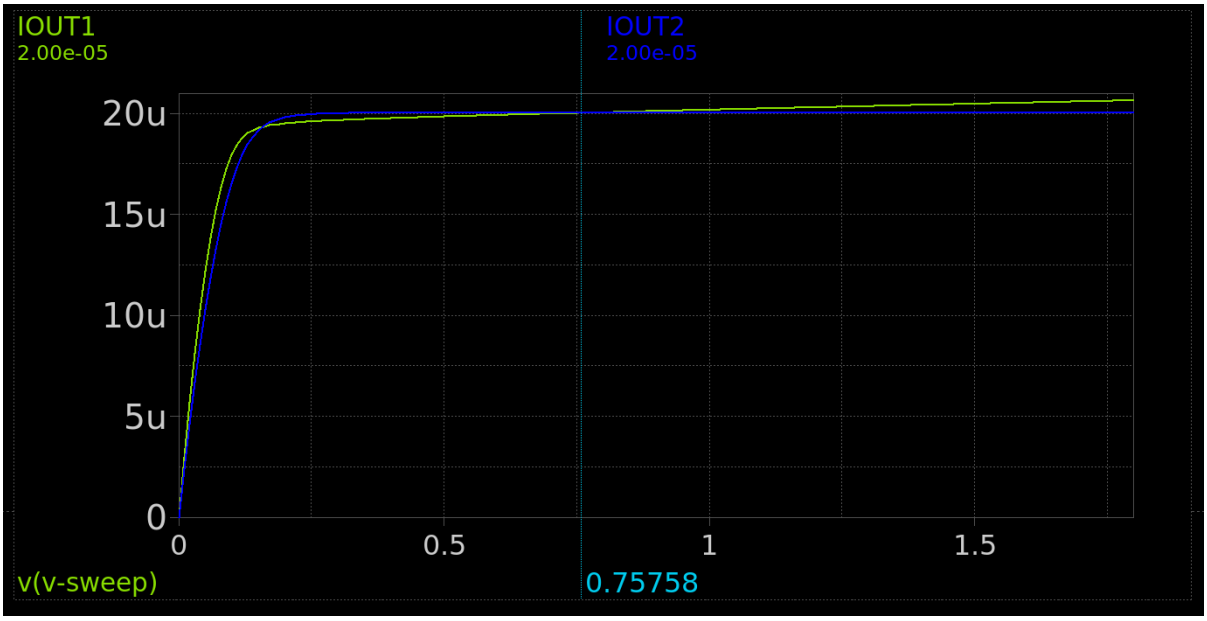


*Figure 7 Value at which Iout1 equals IB*2 Exactly*

Iout1 equals IB*2 exactly at around **0.75758mV** as this is the value at which VDS of both transistor are equal each other eliminating the error

2. Simple current Mirror Error

```
i1                    =   1.983372e-05
i2                    =   2.046570e-05
i_error = 3.159900e+00
```

Figure 8 Error Calculated in Simulation

$$\boldsymbol{I_{out}\%Error = 3.16\%}$$

The value is consistent with the results from Part one as it corresponds with the value calculated from ADT for Lambda $\lambda = 31.94m$

3. Percentage of Error for both CMs

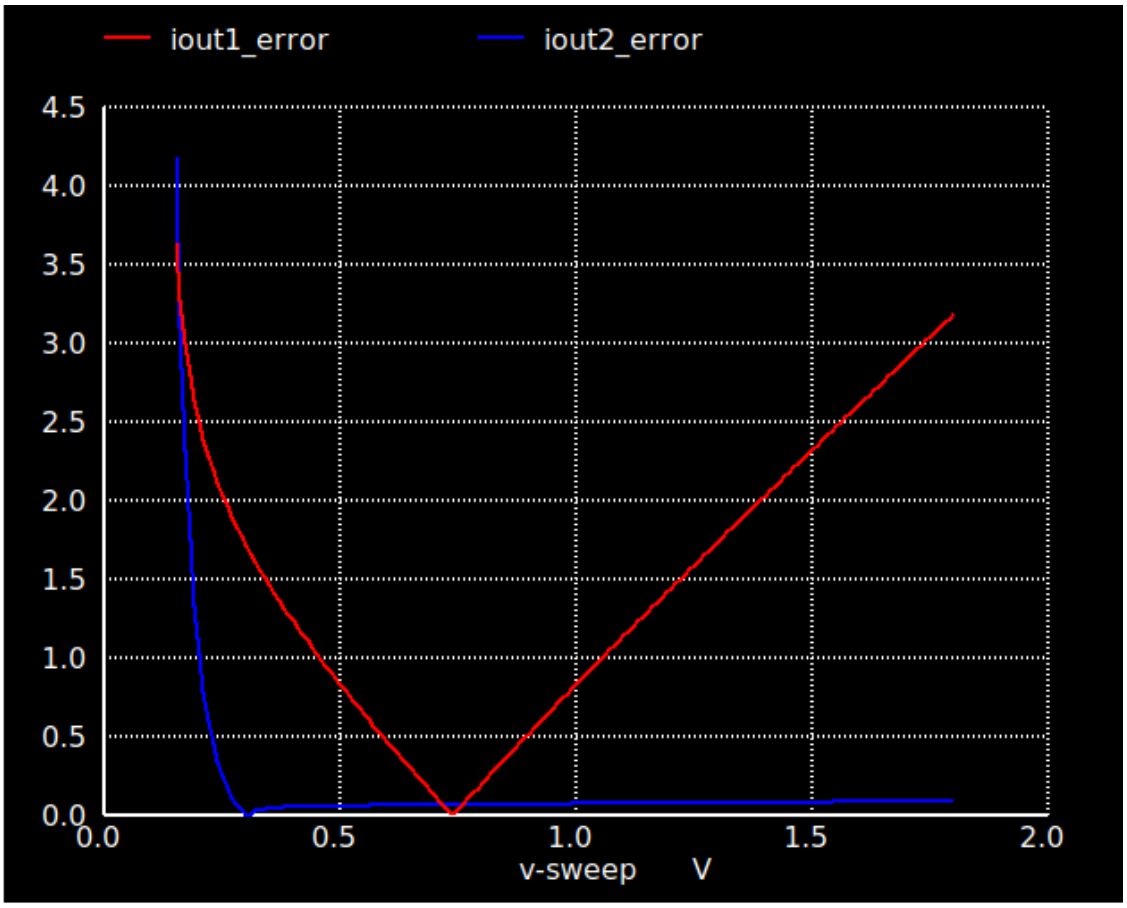


Figure 9 Current Error for both configurations

The error in the simple CM is fairly larger and fluctuates as VDS changes, it becomes zero at VDS0=VDS1 the same value calculated previously at which IOUT1=IB*2 exactly. While the cascode error is consistently zero throughout the sweep.

4. ROUT vs VOUT

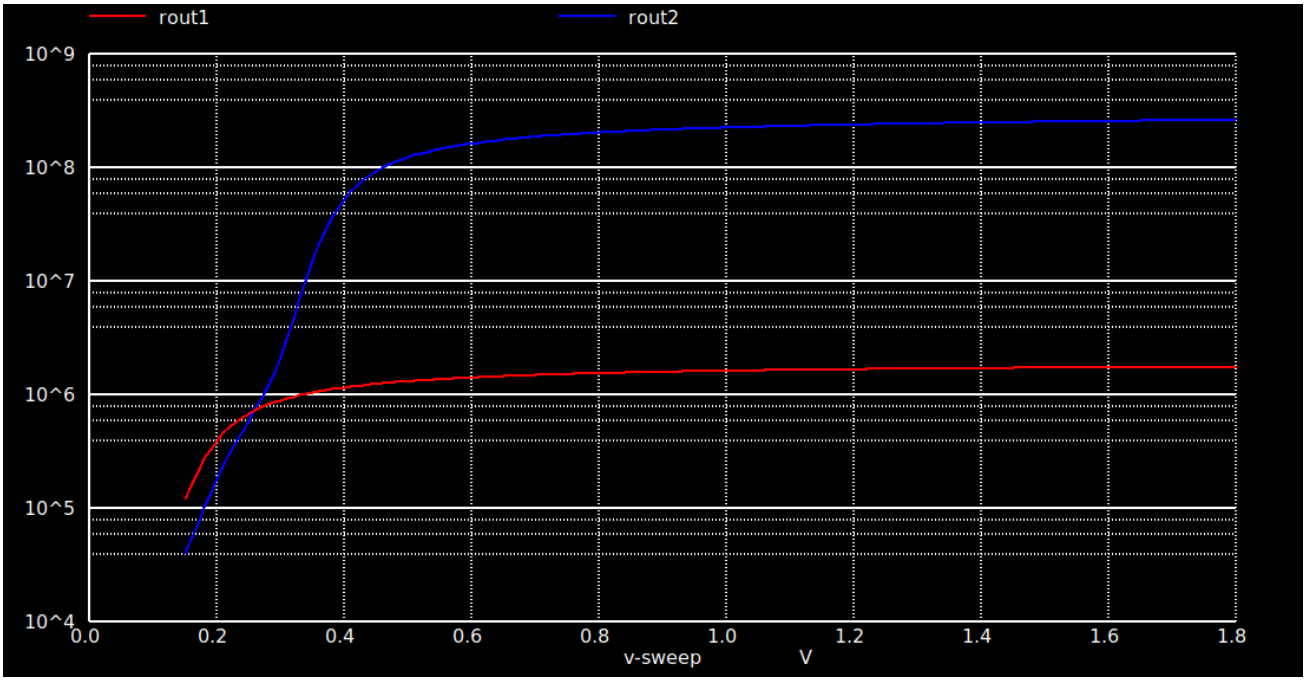


Figure 10 ROUT1 and ROUT2 vs VOUT

Cascode Current Mirror has significantly higher ROUT.
Yes Rout changing slightly with VOUT due to the change of operation regions of the transistors at the beginning of the sweep it has a much smaller value due to transistors operating in triode instead of saturation and even in saturation ROUT changes due to its dependance on VDS.

5. Analytic Calculation for ROUT

$$R_{OUT1} = ro = \frac{1}{g_{ds}} = \mathbf{1.586M\Omega}$$

$$R_{out2} = (gm_5 + gmbs_5)ro_5ro_3 = \mathbf{213.323M\Omega}$$

```
rout1_vdd_2          =   1.586116e+06
rout2_vdd_2          =   2.154332e+08
```

Figure 11 Simulator Results

	Analytic	Simulation
ROUT1	1.586M	1.586M
ROUT2	213.3M	215.43M

Analytic and simulation results agree with each other!

Mismatch:

Mismatch on VGMIS1:

```
i_percent_cm = 1.269855e+00
```

Figure 12 Error due to VGMIS1 in Simple CM

```
i_percent_1_cascode = 1.252949e+00
```

Figure 13 Error due to VGMIS1 in Cascode CM

$$Simple\ Current\ Mirror: I_{MIS1} = \mathbf{1.269\%}$$

$$Cascode\ Current\ MIrror: I_{MIS1} = \mathbf{1.252\%}$$

Hand Analysis

$$Simple\ Current\ Mirror: \%I_{MIS1} = \frac{V_{mis} * gm_1}{2 * IB} = 1.2717\%$$

$$Cascode\ Current\ Mirror: \%I_{MIS1} = \frac{V_{mis} * gm_3}{2 * IB} = 1.25757\%$$

Simulation and analytical results agree with each other!

Mismatch on VGMIS2:

```
i_percent_2 = 8.893605e-03
```

Figure 14 Mismatch due to VGMIS2 in Cascode CM

$$Cascode\ Current\ MIrror: I_{MIS2} = \mathbf{8.89 * 10^{-3}\% \approx 0\%}$$

Hand Analysis

$$Cascode\ Current\ Mirror: \%I_{MIS2} = \frac{\boldsymbol{gm_5 * V_{mis2}}}{\left(\mathbf{1} + \frac{\boldsymbol{gm_5 + gmbs_5}}{\boldsymbol{g_{ds3}}}\right)\mathbf{2} * \boldsymbol{I_B}} = \mathbf{8.975 * 10^{-3}\% \approx 0\%}$$

5) Which mismatch contribution is more pronounced? Why?

Mismatch due to VGMIS1 is significantly more pronounced in comparison with VGMIS2, This is because it is directly affecting the mirroring devices
While mismatching in VGMIS2 only affects the cascode devices which aren't directly responsible for the mirroring thus a way smaller errors in current is observed

6) Which design decision is better: setting the same W and L for the mirror and cascode devices? Or using larger W and L for the current mirror devices? Why

Using Larger W and L for the current mirror devices.
Because it improves mirroring as the devices are less affected by Channel Length Modulation and Process Variations and also improves the Output Resistance.

Monte Carlo Simulation:

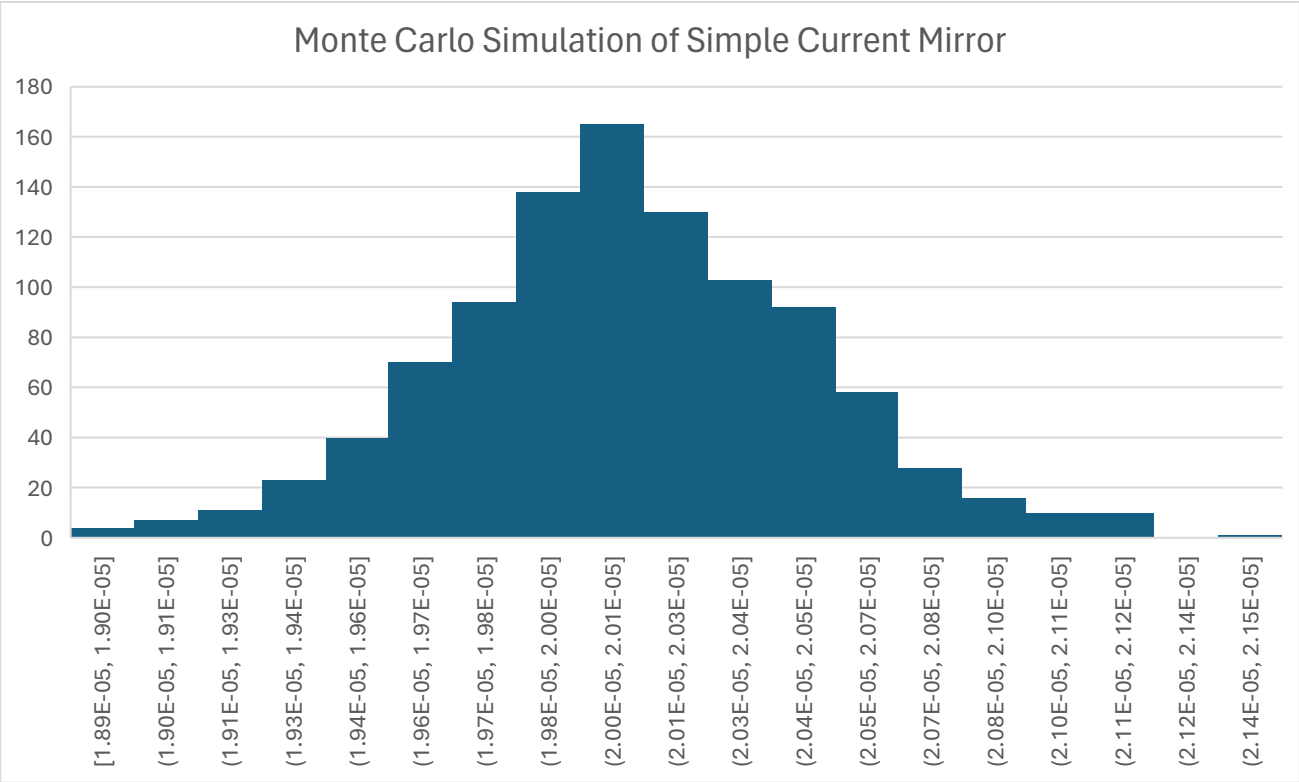


Figure 15 MC Simulation of Simple Current Mirror (1000 runs)

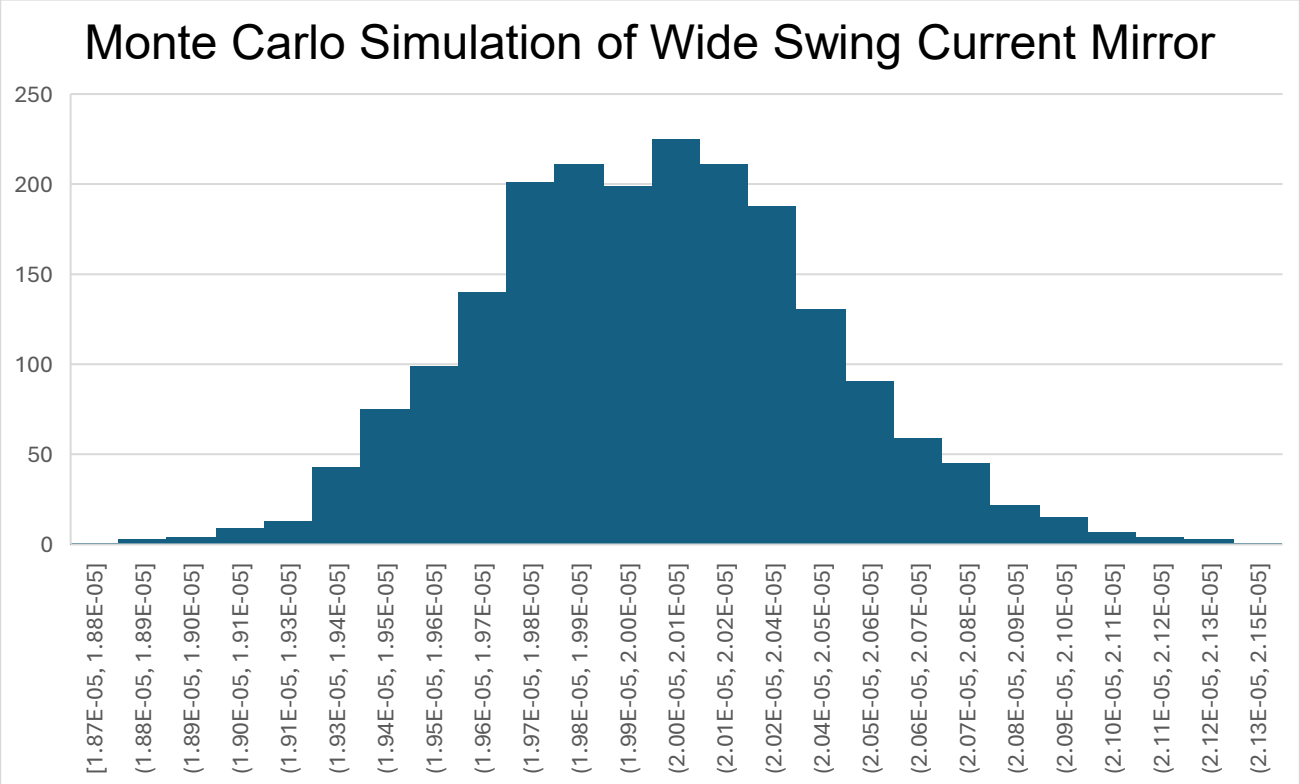


Figure 16 MC Simulation of Wide Swing Current Mirror (1000 runs)

Standard Deviation of Wide Swing Current Mirror: $\boldsymbol{\sigma_{wcm} = 3.83922E-07}$

$$\frac{\sigma(I_{out\,wcm})}{I_{out}} = \mathbf{1.9195\%}$$

Standard Deviation of Wide Swing Current Mirror: $\boldsymbol{\sigma_{cm} = 3.97013E-07}$

$$\frac{\sigma(I_{out\,cm})}{I_{out}} = \mathbf{1.985\%}$$

The results we achieved compare perfectly with the expected results from the specs and the analytical analysis done at the beginning, thus the current mirrors meet the spec