### وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا Dr. Hesham Omran

Ain Shams University – Master Micro LLC

### Analog IC Design (Xschem, Ngspice, ADT) Lab 04

### Common Drain Frequency Response

# **Intended Learning Objectives**

In this lab you will:

- Learn how to use the Sizing Assistant (SA) to size the transistors.
- Design and simulate a common-drain amplifier.
- Use PMOS input transistor to avoid body effect in a CD amplifier.
- Investigate the ringing and peaking problem in a capacitive-loaded CD amplifier with a large source resistance (Rsig) and learn how to solve it.

### Part 1: Device Sizing Using SA

1) From the square law, we have

$$g_m = \frac{2I_D}{V_{ov}} \to V_{ov} = \frac{2}{g_m/I_D}$$

For a real MOSFET, if we compute  $V_{ov}$  and  $\frac{2}{g_m/I_D}$  they will not be equal. We can define V-star  $(V^*)$ , which is calculated from actual simulation data using the formula

$$V^* = \frac{2}{g_m/I_D} \leftrightarrow g_m = \frac{2I_D}{V^*}$$

The lower the  $V^*$  the higher the  $g_m$ , but the larger the area and the lower the speed. An often used sweet-spot that provides good compromise between different trade-offs is  $V^* = 200mV$ .

2) Although the  $V^*$  is a nice parameter that is inspired by the square-law, it does not have an intuitive or a physical meaning (it is not an actual voltage in the circuit). We actually defined  $V^*$  in order to be able to define a relation between the  $g_m$  and  $I_D$ . Thus, the real parameter that we should care about is the  $g_m$  over  $I_D$  ratio  $(g_m/I_D)$ .

If the square-law is valid

$$g_m = \frac{2I_D}{V_{ov}} \to \frac{g_m}{I_D} = \frac{2}{V_{ov}}$$

Using  $V^*$ 

$$\frac{g_m}{I_D} = \frac{2}{V^*}$$

A small  $g_m/I_D$  means large  $V_{ov}$  (biasing in strong inversion) and a large  $g_m/I_D$  means small  $V_{ov}$  (biasing in weak inversion).

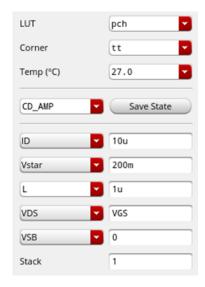
3) There are many good things about using the  $g_m/I_D$  as a design knob:

- The  $g_m/I_D$  gives a direct relation between the most important MOSFET parameter  $(g_m)$  and the most valuable resource  $(I_D)$ . For example, a  $g_m/I_D=10$  S/A means you get  $10~\mu S$  of  $g_m$  for every  $1~\mu A$  of bias current.
- The  $g_m/I_D$  is a normalized knob: it has a limited search range (typically from 5 to 25 S/A) independent of the technology or the device type.
- The  $g_m/I_D$  is intuitive because it tells you directly about the inversion level (bias point) and consequently all related trade-offs. For example,  $g_m/I_D=5\,S/A$  means strong inversion (SI),  $g_m/I_D=15\,S/A$  means moderate inversion (MI), and  $g_m/I_D=25\,S/A$  means weak inversion (WI).
- The  $g_m/I_D$  is an orthogonal knob: If we define the  $g_m/I_D$  then we define the inversion level (bias point). If you change  $I_D$  or L while keeping  $g_m/I_D$  fixed, then the inversion level (bias point) is kept fixed. The W is treated as an output variable instead of being treated as an input variable.
- The higher the  $g_m/I_D$  (the lower the  $V^*$ ) the higher the efficiency and the headroom (the available swing), but the larger the area and the lower the speed. An often used sweet-spot that provides good compromise between different trade-offs is  $g_m/I_D=10\ S/A\ (V^*=200mV)$ . Larger  $g_m/I_D$  is usually used for low-voltage and low-power designs.
- 4) We want to design a CD amplifier that has ideal current source load with the parameters below.

Parameter	
Input transistor	PMOS
$L^1$	1μm
<b>V</b> *	200mV
Quiescent (DC) input voltage	0 <i>V</i>
Supply	1.8V
Current consumption	10μΑ

- 5) We assume we use a PMOS transistor that is placed in a dedicated n-well to be able to connect the body and source terminals. This will avoid the degradation of the CD amplifier gain due to body effect.
- 6) Draw the amplifier schematic. Note that the load is connected to the source, not to the drain.
- 7) Since the square-law is not accurate, we cannot use it to calculate the sizing. Instead, we will use the Sizing Assistant (SA) which is a powerful analog calculator that uses LUTs that are pre-generated from the simulations. The input of SA is shown below. Note that since both the gate and the drain are connected to ground, we can set VDS = VGS.

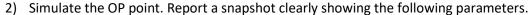
<sup>&</sup>lt;sup>1</sup> A relatively long L is intentionally used to be able to use the simplified frequency response expressions given in the lecture slides.

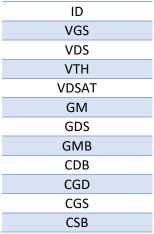


Part 2: CD Amplifier

#### 1. OP (Operating Point) Analysis

1) Create a new schematic for the CD amplifier (the schematic is not included in the lab document and is left for the student as an exercise). Use a PMOS transistor and use a  $10\mu A$  ideal current source load for biasing (note that the current source will be connected to the source terminal). Connect the source to the bulk. Use  $L=1\mu m$  and W as determined in Part 1. Use  $C_L=2pF$ , input source resistance  $R_{sig}=2M\Omega$ , and a DC input voltage = 0V.





3) Check that the transistor operates in saturation.

#### 2. AC Analysis

- 1) Perform AC analysis (1Hz:10GHz, logarithmic, 20points/decade) to investigate the frequency domain peaking.
- 2) Report the Bode plot magnitude.
- 3) Do you notice frequency domain peaking? How much is the peaking?
- 4) Analytically calculate the quality factor (use approximate expressions). Is the system underdamped or overdamped?
- 5) Perform parametric sweep: CL = 2p, 4p, 8p.
  - Report Bode plot magnitude overlaid on same plot.
  - Report the peaking vs CL.

- Comment on the results.
- 6) Perform parametric sweep: Rsig = 20k, 200k, 2M.
  - Report Bode plot magnitude overlaid on same plot.
  - Report the peaking vs Rsig.
  - Comment on the results.

#### 3. Transient Analysis

- 1) Use a pulse source as your transient stimulus and set it as follows: delay time = 2us, initial (zero value) = 0V, period = 8us, pulse (one value) = 100mV, fall time = 1ns, rise time = 1ns, pulse width = 4us.
- 2) Run transient analysis for 10us with 10ns step to investigate the time domain ringing.
- 3) Report Vin and Vout overlaid vs time.
- 4) Calculate the DC voltage difference (DC shift) between Vin and Vout.
  - What is the relation between the DC shift and VGS of the transistor?
  - How to shift the signal down instead of shifting it up?
- 5) Do you notice time domain ringing? How much is the overshoot?
- 6) Perform parametric sweep: CL = 2p, 4p, 8p.
  - Report Vout vs time overlaid on same plot.
  - Report the overshoot vs CL.
  - Comment.
- 7) Perform parametric sweep: Rsig = 20k, 200k, 2M.
  - Report Vout vs time overlaid on same plot.
  - Report the overshoot vs Rsig.
  - Comment on the results.

#### 4. $Z_{out}$ (Inductive Rise)

- 1) We want to simulate the CD amplifier output impedance. Replace CL with an AC current source with magnitude = 1. Remove the AC input signal.
- 2) Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade). The voltage across the AC current source is itself the output impedance.
- 3) Plot the output impedance (magnitude and phase) vs frequency. Do you notice an inductive rise? Why?
- 4) Does  $Z_{out}$  fall at high frequency? Why? Hint:  $C_{ad}$  appears in parallel with  $R_{sig}$ .
- 5) Analytically calculate the zeros, poles, and magnitude at low/high frequency for  $Z_{out}$ . Compare with simulation results in a table.

#### 5. [Optional] How to solve the peaking/ringing problem?

- 1) The simple solution is to place the input/output poles away from each other (as we did when we swept CL and Rsig).
- Alternatively, a compensation network can be used to compensate for the negative input impedance and prevent overshoots. Read [Johns and Martin, 2012] Section 4.4 and try to implement the compensation network.

## Lab Summary

#### In Part 1 you learned:

- How to find transistor sizing using the Sizing Assistant (SA).
- How to design a PMOS common-drain amplifier.

#### In Part 2 you learned:

- How to perform AC, DC and transient simulations of a CD amplifier.
- How the peaking in the frequency response of a CD amplifier changes with the load capacitor and source resistance.
- How the ringing in the transient response of a CD amplifier changes with the load capacitor and source resistance.
- How the output impedance of a CD amplifier shows inductive behavior.

# Acknowledgements