LAB 2

Part 1: Sizing Chart

Vrd required = VDD/2 = 1.8/2 = **0.9v**

V* required = 2*Vrd/Av = 2*0.9/8 = **0.225v**

Rd = Vrd/Idq = 0.9/100u = **9k ohm**

V* and Vov overlaid vs VGS:

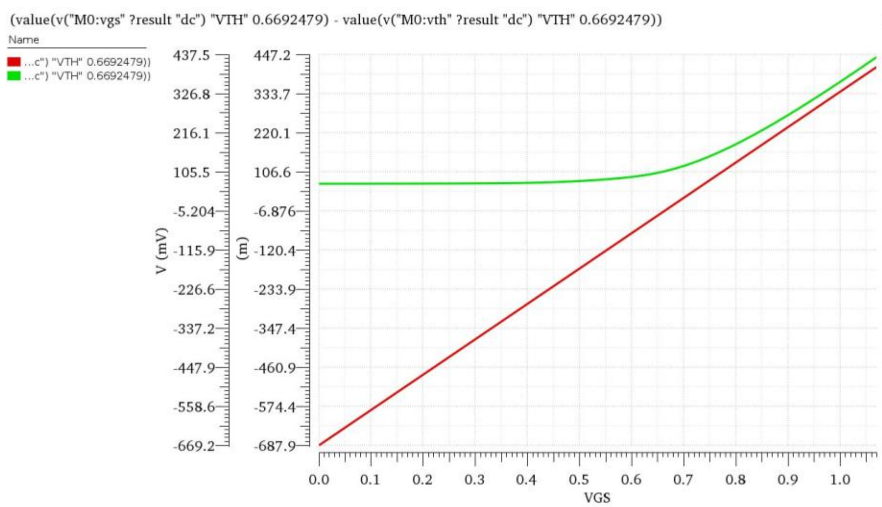


Figure 1 NMOS

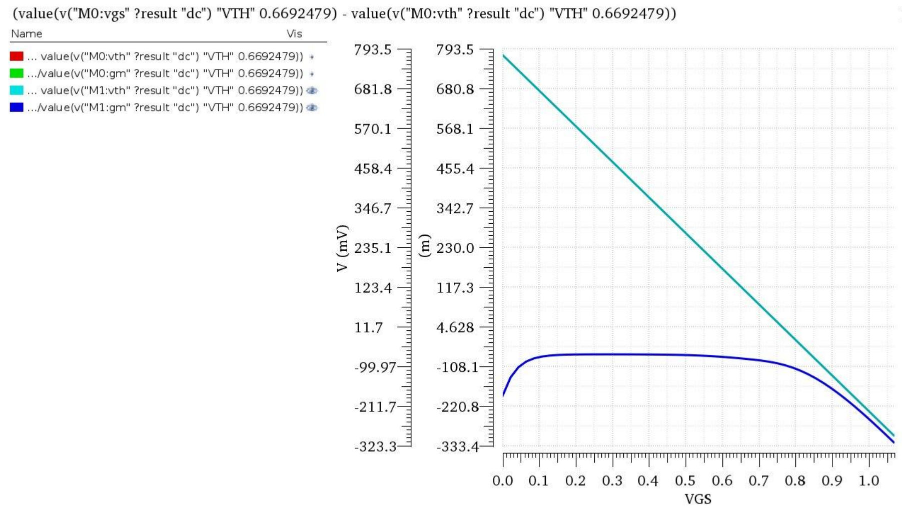
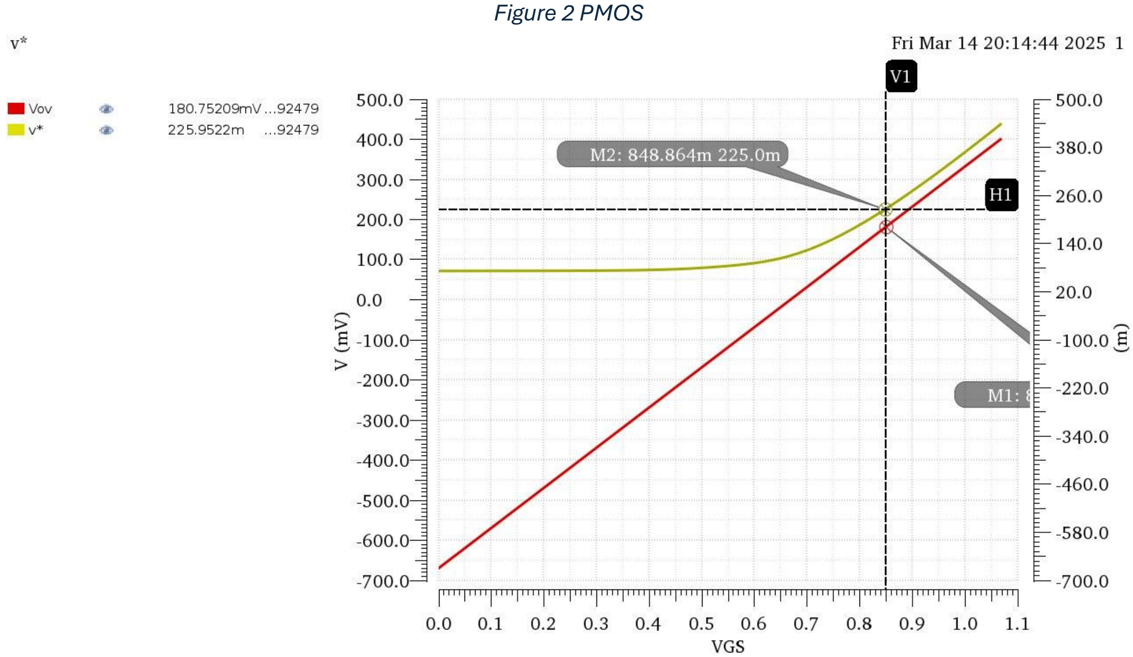
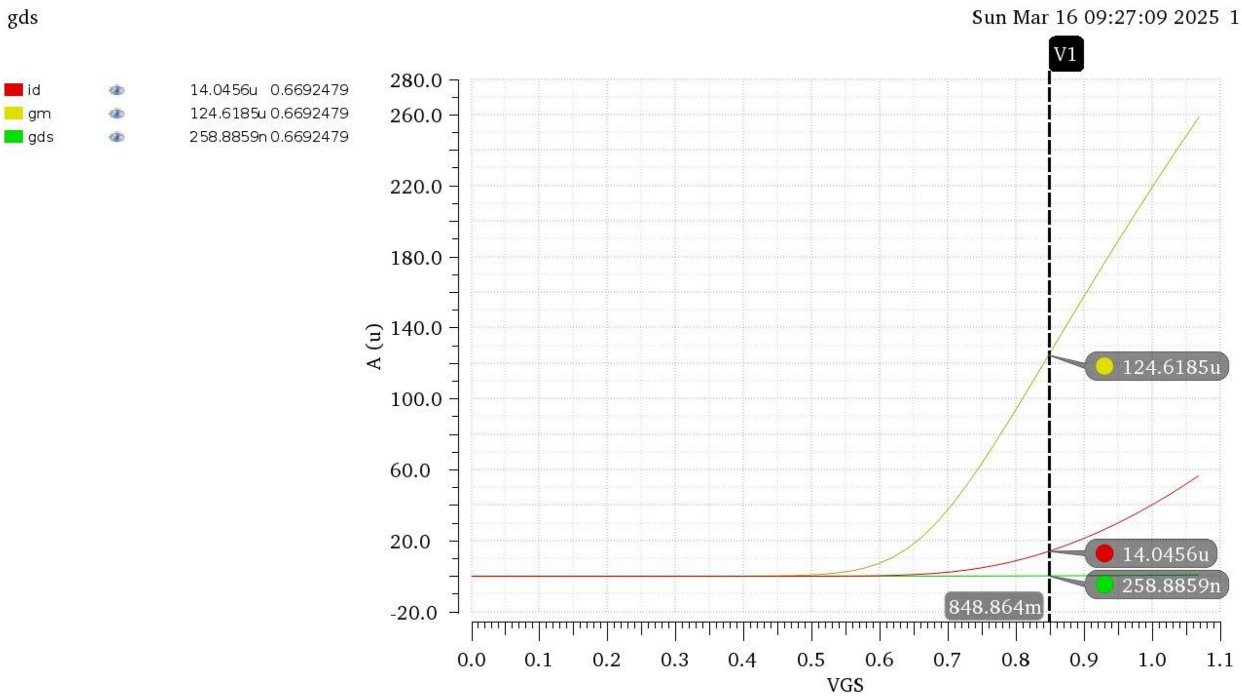


Figure 2 PMOS



Required Vgs = **848.864mV**

IdX	14.0456 uA
gmX	124.6185 uA/V
gdsX	258.8859 nA/V



Using cross multiplication to get Wq from Idq, as well as gmq and gdsq:

Wq	71.1966um
Gmq	887.2413 uA/v
gdsq	1843.17 nA/v

Part 2: CS Amplifier

2- DC Operating Point:

Output	Nominal
Ids	99.95e-6
Vgs	848.9e-3
Vds	900.4e-3
gm	888.8e-6
ro	542.3e3
region	2

Simulated resulted agree with the calculated results from the previous part.

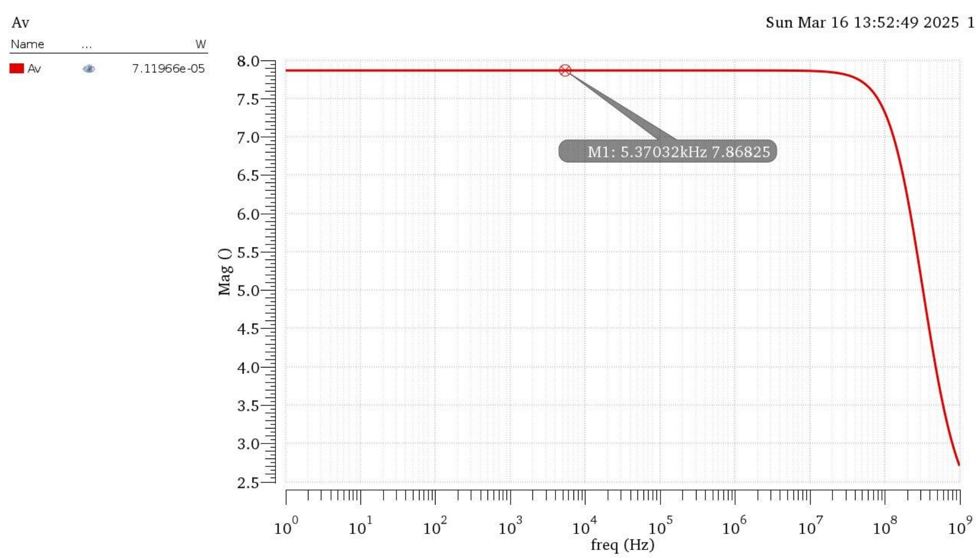
3- ro is significantly larger than Rd, neglecting it would be valid and won't change the results significantly.

4- Intrinsic Gain = -gm*ro = -888.8e-6 * 542.3e3 = -482.0287

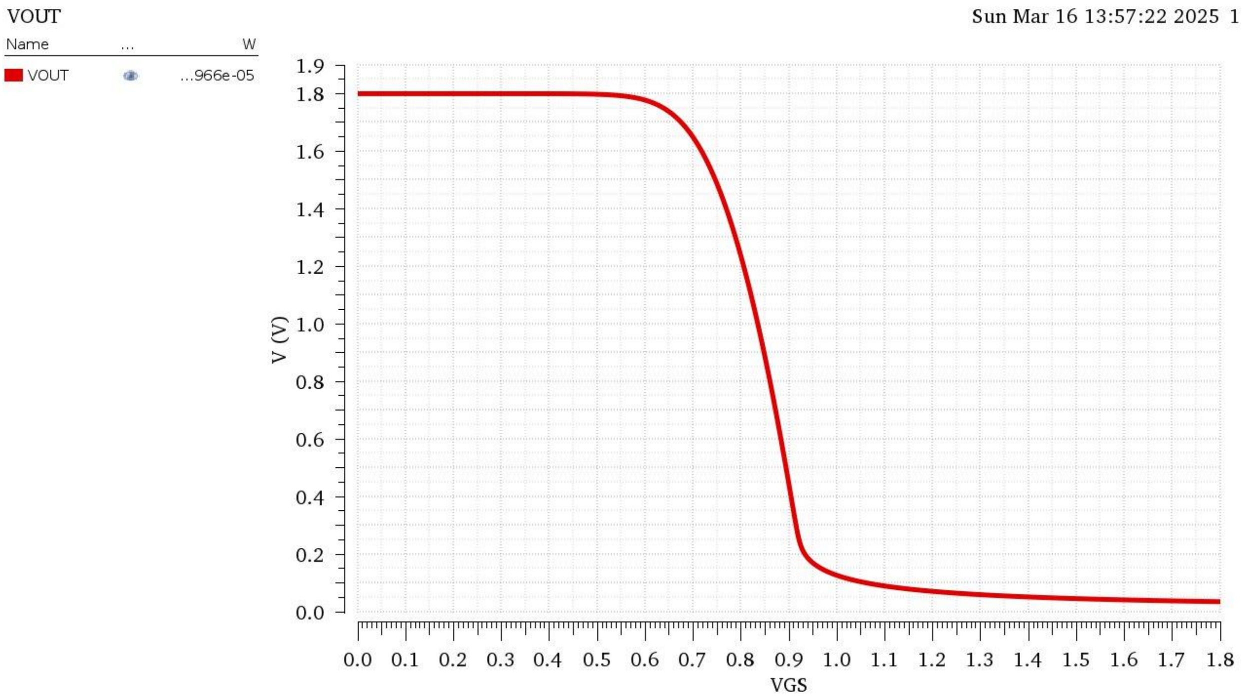
5- Amplifier Gain = -gm*(ro // Rd) = 7.868 < intrinsic gain

Intrinsic gain is the highest attainable gain by the amplifier.

6-

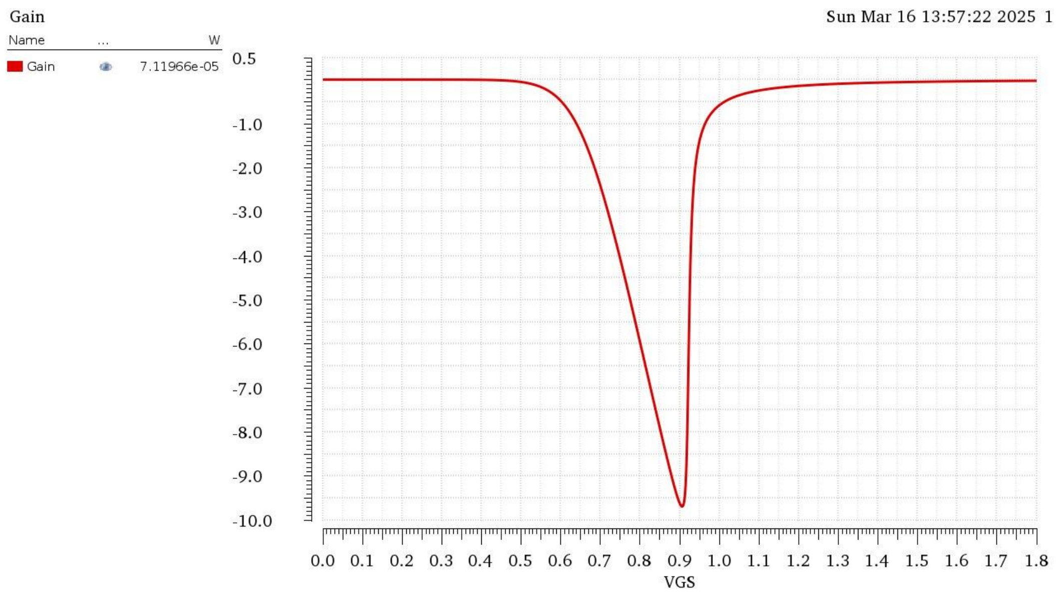


2- VOUT vs VIN:



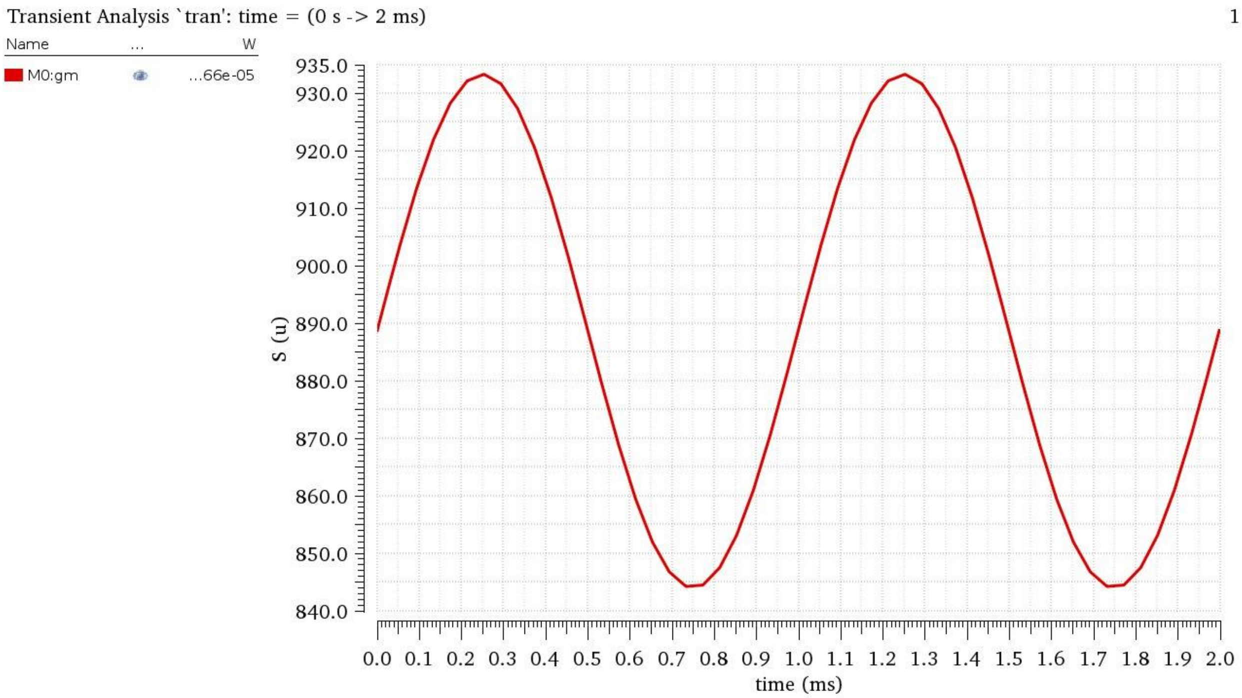
The relation is not linear as it depends on the square law, although towards the middle it seems more linear which is the best region to operate the amplifier in to get steady gain.

3-



The gain is not linear as the relation between the input and gm is not linear as well but it can observe linearity around its operating point.

5-



gm changes with time as it depends on the input voltage albeit the change is very small (0.1m peak to peak) and can be neglected for small signal analysis.

6- The CS Amplifier can be considered linear around its operating point as it meets the conditions.