Analog IC Design

Lecture 04
MOSFET Large Signal Model

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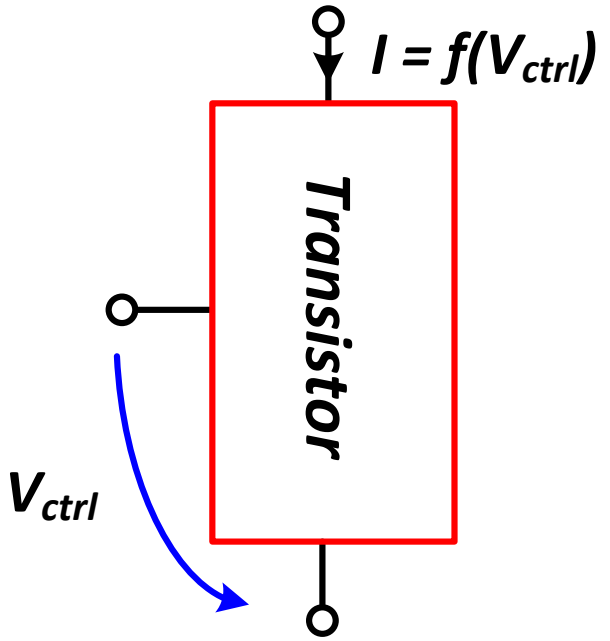
Outline

- Why is the Transistor Different?
- MOSFET Structure
- MOSFET Operation
  - Depletion
  - Inversion and Channel Formation
  - Linear and Triode Region
  - Saturation (Pinch-off) Region
- MOSFET IV Characteristics and Large Signal Model
- Channel Length Modulation
- Body Effect
- Short channel effects

Why is the Transistor Different?

- We are used to two-terminal devices
  - Resistors, capacitors, inductors, diodes
- The transistor is a three-terminal device
  - The voltage between two terminals controls the current flowing in the third terminal
  - Voltage controlled current source (VCCS)
- This feature enabled a multitude of applications that changed our life!
  - Analog signal amplification and processing
  - Digital logic and memory circuits



VCCS as an Amplifier

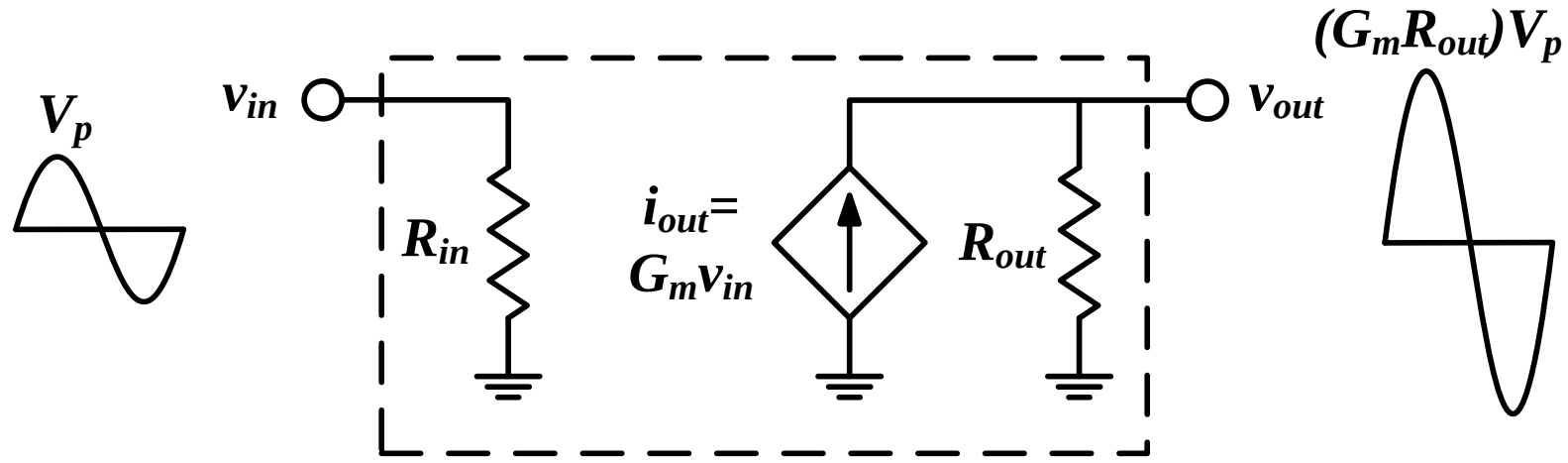
- Voltage controlled current source (VCCS): v_{in} controls i_{out}

$$Transconductance = \frac{i_{out}}{v_{in}} = G_m$$

$$v_{in} = V_p \sin(\omega t)$$

$$v_{out} = G_m v_{in} \times R_{out} = (G_m R_{out}) v_{in} = (G_m R_{out}) V_p \sin(\omega t)$$

$$Voltage\ Gain = A_v = \frac{v_{out}}{v_{in}} = G_m R_{out}$$

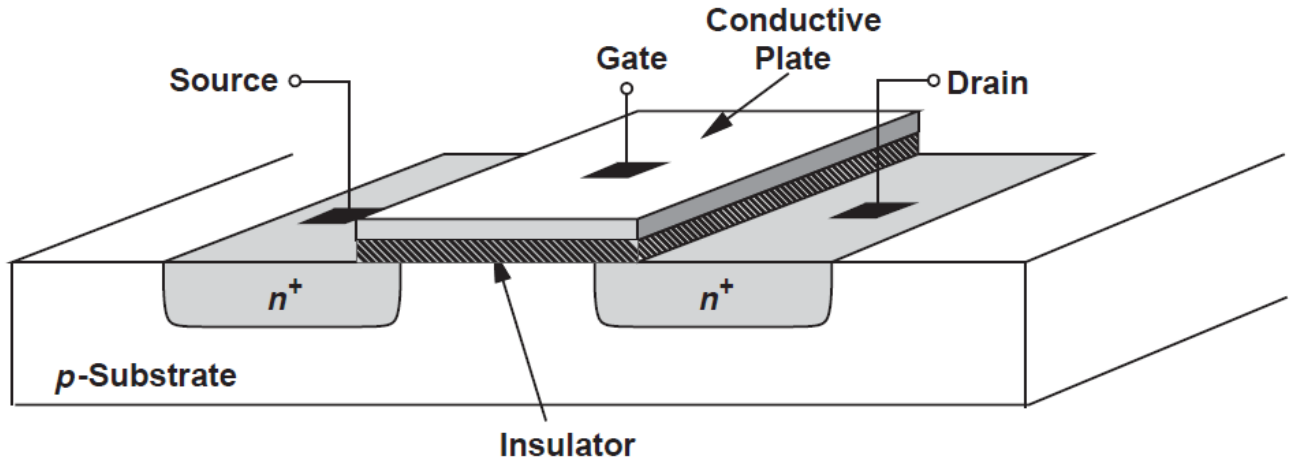


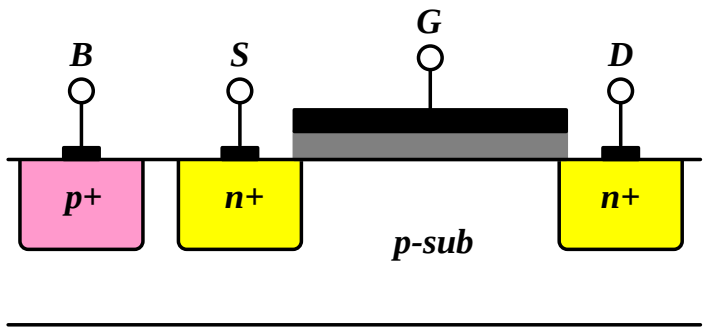
MOSFET

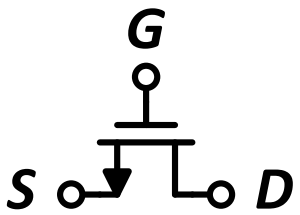
- MOSFET: Metal-oxide-semiconductor field-effect transistor
  - N-channel MOSFET: NMOS
  - P-channel MOSFET: PMOS
  - Complementary MOS (CMOS) technology: NMOS + PMOS
- A.k.a. insulated-gate FET or IGFET
- Simply, a VCCS
- The concept of MOSFET was patented in 1925
- But it was not successfully fabricated till 1960s
- CMOS technology became the dominant IC fabrication technology by the 1980s

N-Channel MOSFET Structure

- MOSFET: Metal-oxide-semiconductor field-effect transistor
- Three-terminal device: Gate (G), Source (S), and Drain (D)
- Substrate/Bulk/Body (S/B) can be treated as a fourth terminal



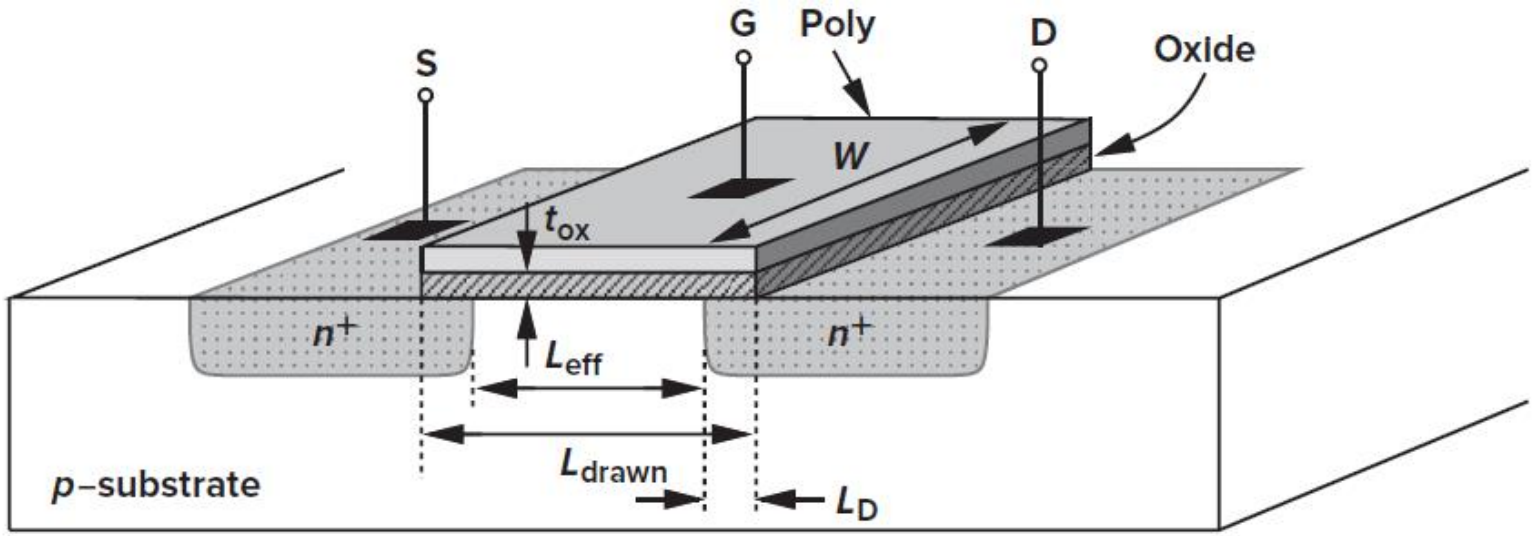




[Razavi, 2014]

MOSFET Dimensions

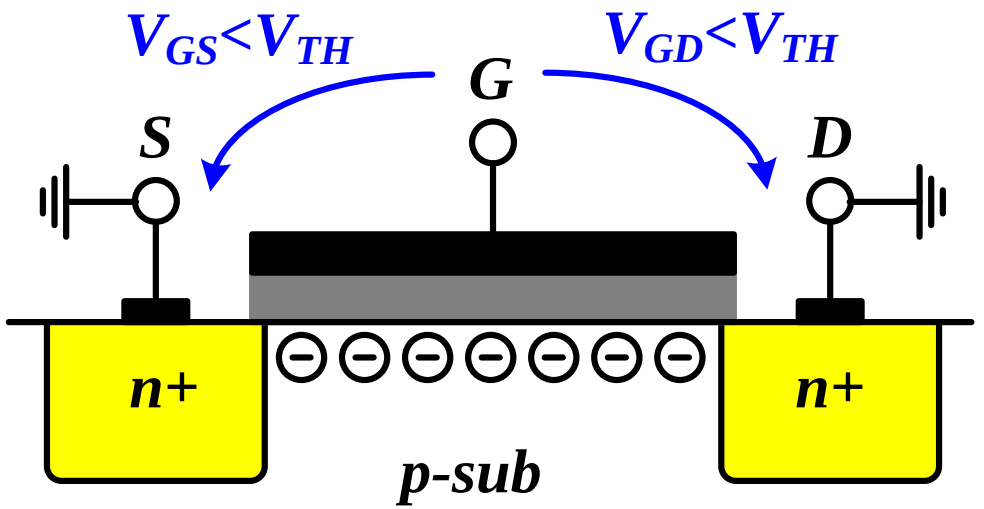
- Channel length: $L \sim 10nm - 10\mu m$
- Channel width: $W \sim 50nm - 100\mu m$
- Oxide thickness: $t_{ox} \sim 1nm - 10nm$
- Gate formed of metal or polysilicon



[Razavi, 2017]

Depletion

- The device acts as a capacitor: positive charge on the gate is mirrored by negative charge in the substrate
- The positive charge on the gate repels the holes in the substrate
  - Fixed negative ions are exposed (uncovered)
  - A depletion region is created



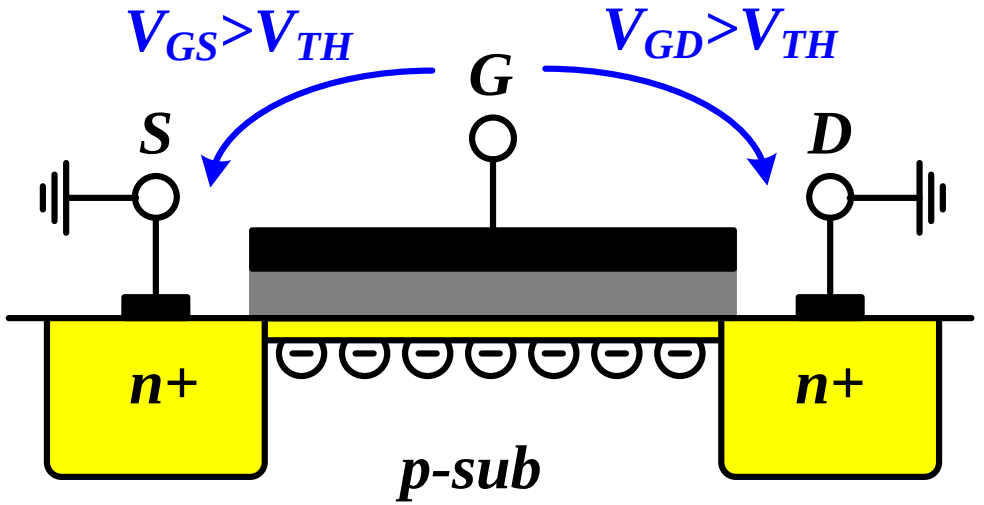
Inversion and Channel Formation

- N-type channel region (inversion layer) formed at

$$V_{GS} > V_{TH}$$

$$V_{GS} = V_{TH} + V_{ov}$$

  - Threshold voltage: $V_{TH} \sim 0.3V - 1V$
  - Overdrive voltage: $V_{ov} \sim 0V - 0.5V$ (for analog circuits)
  - Electrons are provided by the n+ source and drain regions



Charge in Channel

$$C_{gate} = \frac{\epsilon_{ox} A}{d} = \frac{\epsilon_{ox} WL}{t_{ox}} = C_{ox} WL$$

- For SiO_2

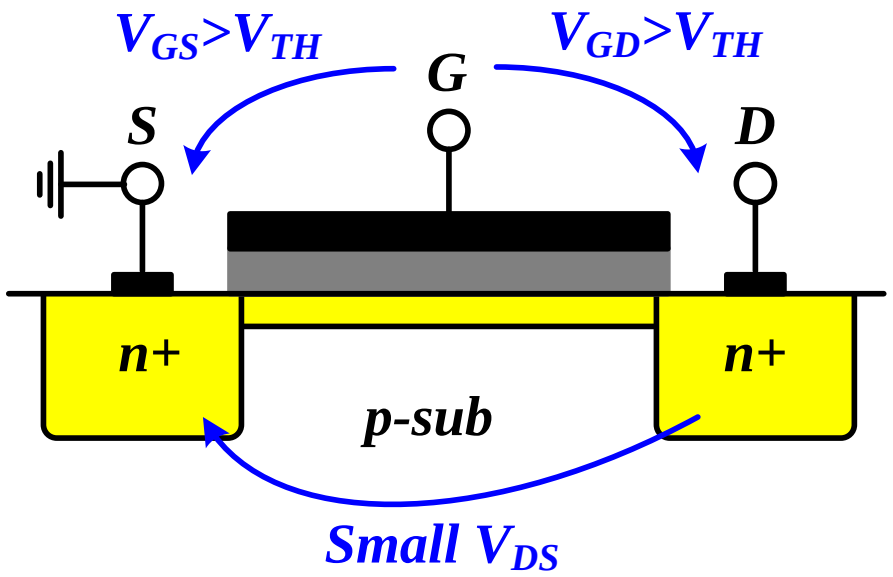
$$\epsilon_{ox} = \epsilon_r \epsilon_o = \mathbf{3.9} \times 8.854 \times 10^{-12} \frac{F}{m}$$

- Example: if $t_{ox} = 4nm \rightarrow C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \approx 8.6 \frac{fF}{\mu m^2}$

$$|Q| = CV = C_{ox} WL \cdot (V_{GS} - V_{TH}) = C_{ox} WL \cdot V_{ov}$$

Linear Region (Deep Triode)

- Small V_{DS}: We assume the channel is uniform
- MOSFET acts as a voltage controlled resistor (VCR)
  - Vertical field (V_{GS}) controls the channel depth (resistance value)
  - Lateral field (V_{DS}) controls the carrier acceleration (drift current)



Linear Region (Deep Triode)

$$|Q| = CV = C_{ox}WL \cdot (V_{GS} - V_{TH}) = C_{ox}WL \cdot V_{ov}$$

$$Electric\ Field = |E| = \frac{V_{DS}}{L}$$

$$Carrier\ Velocity = |v| = \mu_n |E| = \mu_n \frac{V_{DS}}{L}$$

$$Drain\ Current = I_D = \frac{Q}{t} = C_{ox}W\left(\frac{L}{t}\right) \cdot V_{ov} = C_{ox}W \cdot v \cdot V_{ov}$$

$$I_D = \mu_n C_{ox} \frac{W}{L} \cdot V_{ov} \cdot V_{DS} = \frac{V_{DS}}{R_{DS}}$$

$$R_{DS} = \frac{1}{\mu_n C_{ox} \frac{W}{L} \cdot V_{ov}} = \frac{1}{k_n' \frac{W}{L} V_{ov}} = \frac{1}{k_n V_{ov}} = \frac{1}{\beta_n V_{ov}}$$

$$Aspect\ Ratio = \frac{W}{L}$$

Linear Region (Deep Triode)

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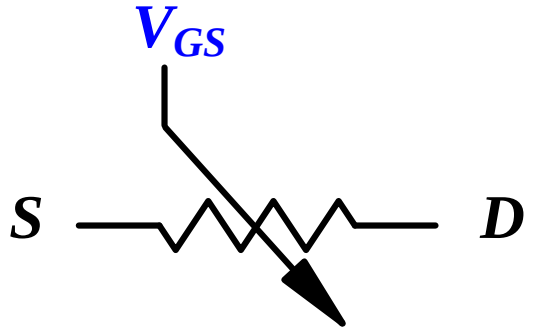
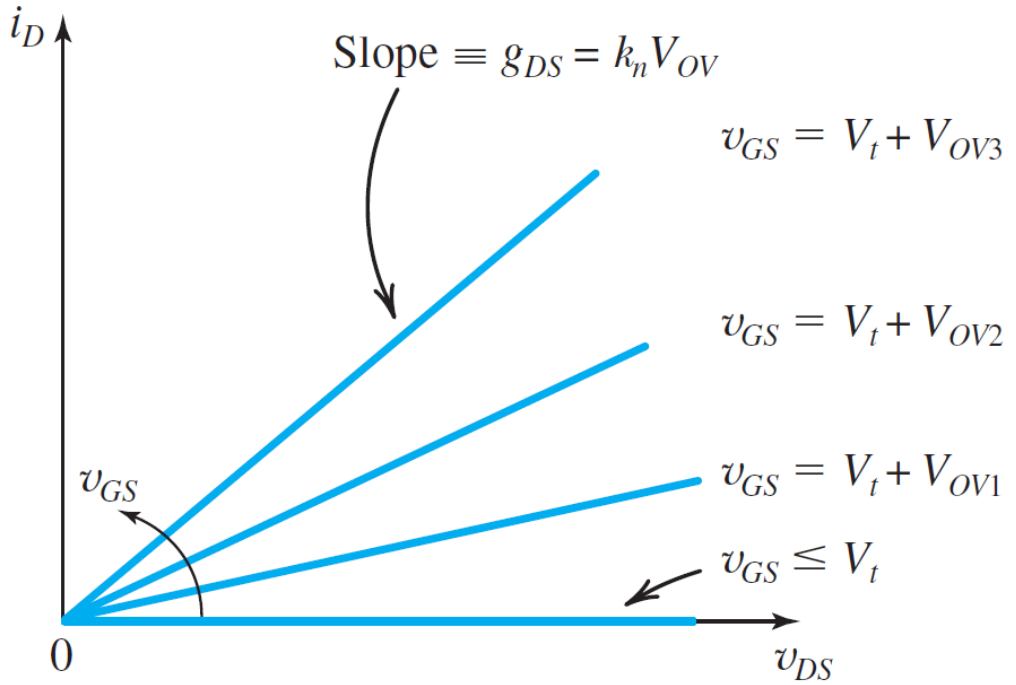


Linear Region (Deep Triode)

- MOSFET acts as a voltage controlled resistor (VCR)

$$R_{DS} = \frac{1}{G_{DS}} = \frac{1}{\mu_n C_{ox} \frac{W}{L} \cdot V_{ov}} = \frac{1}{k_n' \frac{W}{L} V_{ov}} = \frac{1}{k_n V_{ov}} = \frac{1}{\beta_n V_{ov}}$$

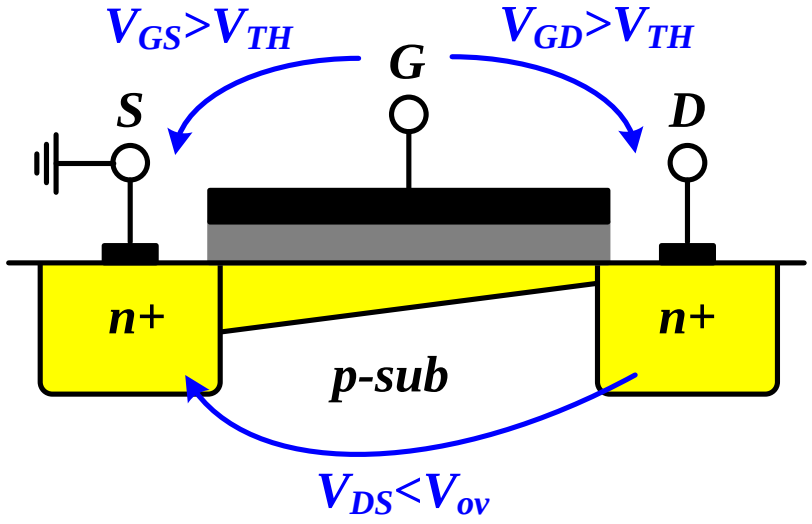
- Linear characteristics



[Sedra/Smith, 2015]

Triode Region

- V_{DS} increases: The channel becomes tapered
- Voltage at source side: $V_{GS} - 0 = V_{GS} = V_{TH} + V_{ov}$
  - If $V_{GS} > V_{TH}$ or $V_{ov} > 0$: The channel exists at source
- Voltage at drain side: $V_{GS} - V_{DS} = V_{GD} = V_{TH} + (V_{ov} - V_{DS})$
  - If $V_{GD} > V_{TH}$ or $V_{DS} < V_{ov}$: The channel exists at drain



Triode Region

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- Voltage at drain side: $V_{GS} - V_{DS} = V_{GD} = V_{TH} + (V_{ov} - V_{DS})$
  - If $V_{GD} > V_{TH}$ or $V_{DS} < V_{ov}$: The channel exists at drain
- Average overdrive voltage:

$$(V_{ov})_{average} = \frac{V_{ov} + (V_{ov} - V_{DS})}{2} = V_{ov} - \frac{V_{DS}}{2}$$

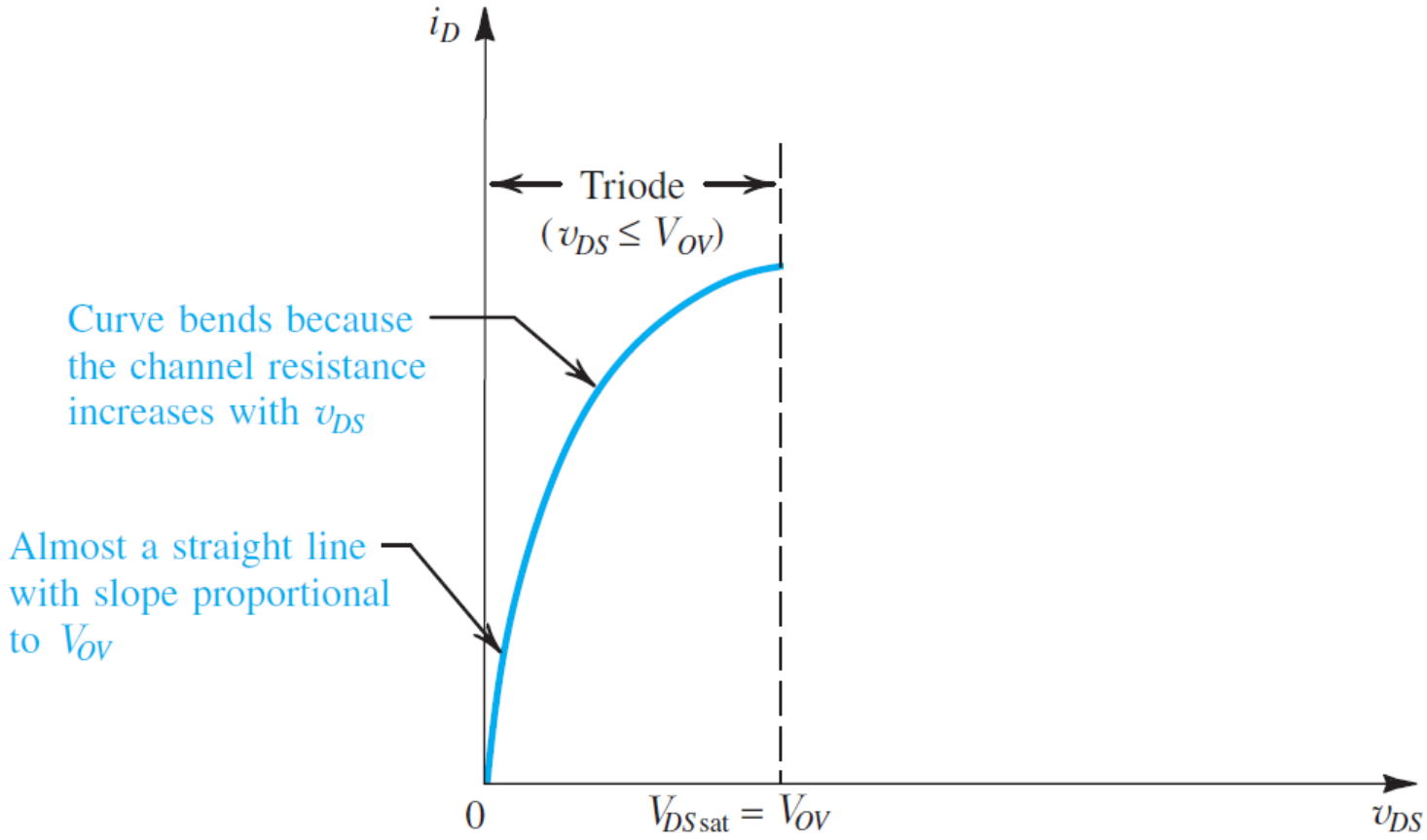
- Replace V_{ov} with $(V_{ov})_{average}$

$$I_D = \mu_n C_{ox} \frac{W}{L} \cdot \left(V_{ov} - \frac{V_{DS}}{2}\right) \cdot V_{DS} = \mu_n C_{ox} \frac{W}{L} \cdot \left(V_{ov} V_{DS} - \frac{V_{DS}^2}{2}\right)$$

Triode Region

- Inverted parabola

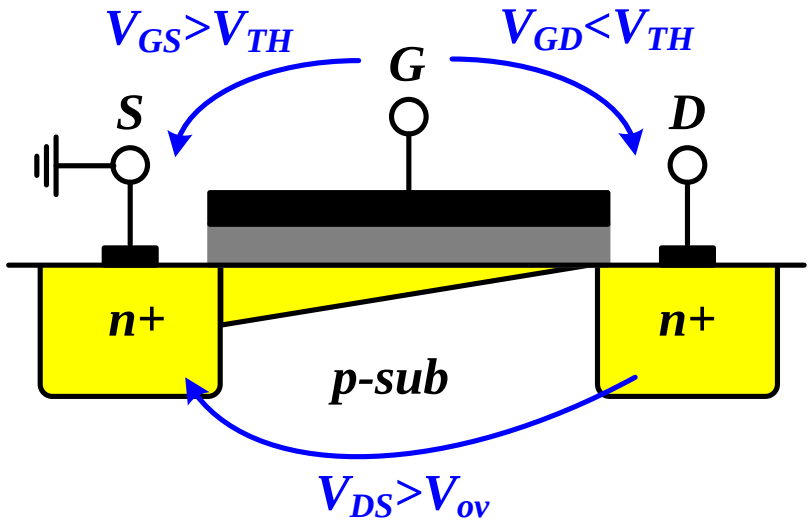
$$I_D = \mu_n C_{ox} \frac{W}{L} \cdot \left(V_{ov} V_{DS} - \frac{V_{DS}^2}{2} \right)$$



[Sedra/Smith, 2015]

Pinch-Off (Saturation)

- $V_{GD} = V_{GS} - V_{DS} \leq V_{TH}$ → $V_{DS} \geq V_{GS} - V_{TH} = V_{ov}$
  - No channel at drain side
  - V_{DS} has no more control on the shape and charge of the channel
- Average overdrive voltage: $(V_{ov})_{average} = \frac{V_{ov}+0}{2} = \frac{V_{ov}}{2} \neq f(V_{DS})$
- Voltage across channel is constant $= V_{GS} - V_{TH} = V_{ov} \neq f(V_{DS})$
  - Extra V_{DS} falls on the small region between channel and drain

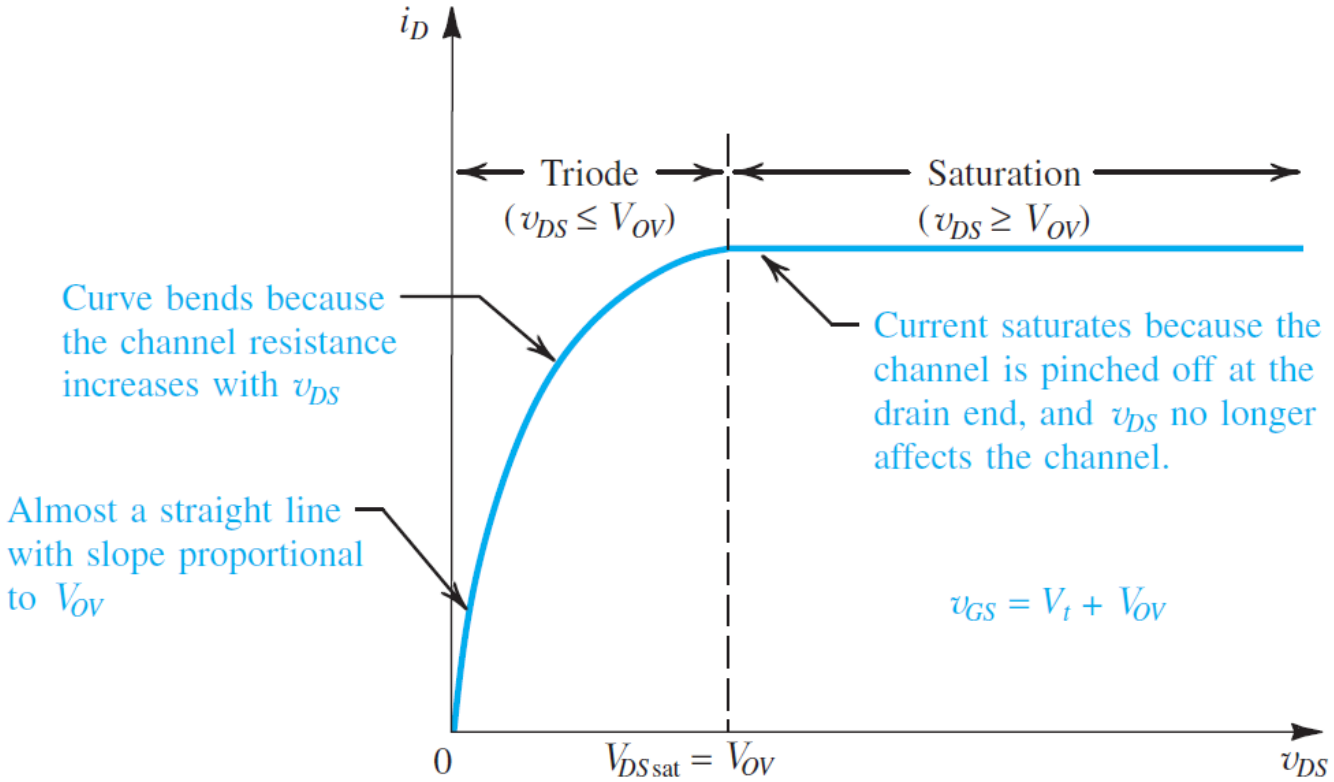


Pinch-Off (Saturation)

- Replace V_{ov} with $(V_{ov})_{average}$ and V_{DS} with V_{ov}

$$I_D = \mu_n C_{ox} \frac{W}{L} \cdot \frac{V_{ov}}{2} \cdot V_{ov} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \cdot V_{ov}^2 \neq f(V_{DS})$$

- Current remains constant (saturates) → **VCCS**



[Sedra/Smith, 2015]

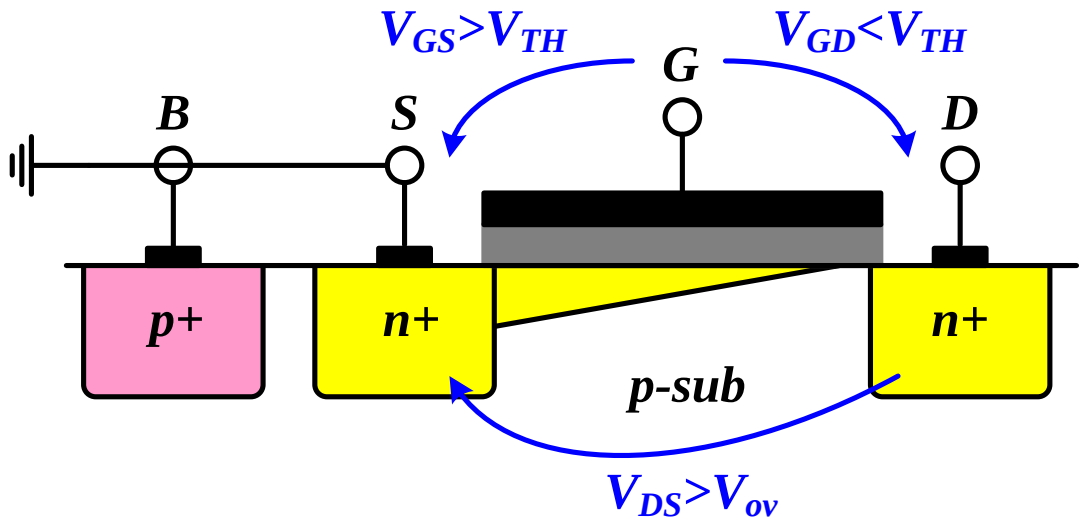
Pinch-Off (Saturation)

- The channel is pinched off if the difference between the gate and drain voltages is not sufficient to create an inversion layer

$$V_{GD} \leq V_{TH} \quad OR \quad V_{DS} \geq V_{ov}$$

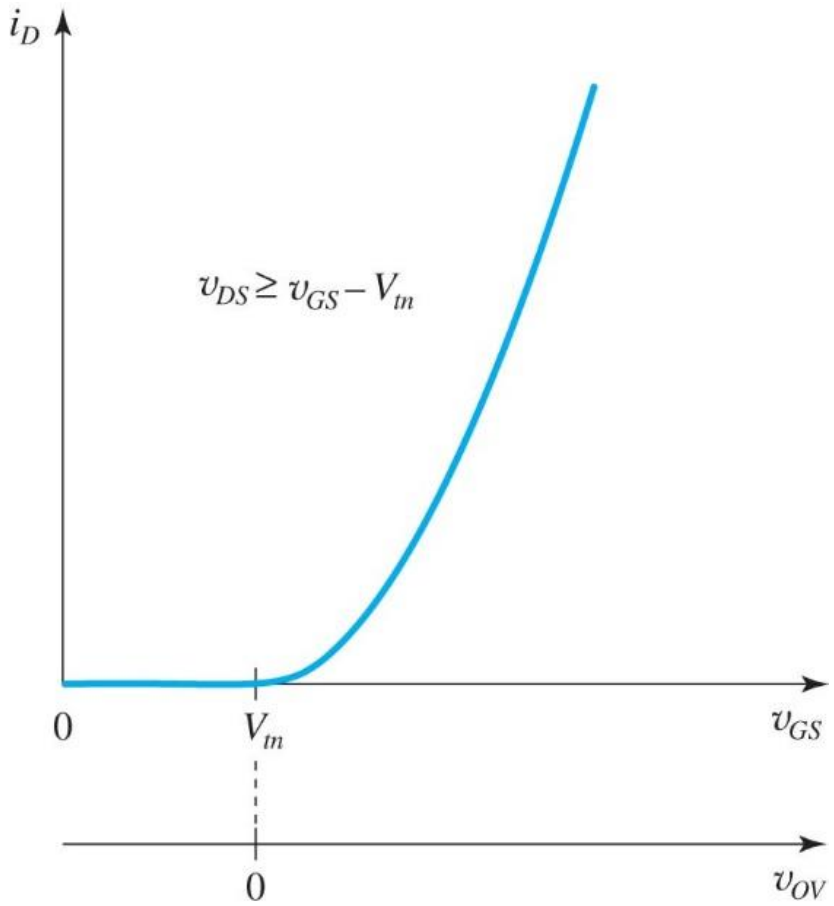
- Square-law (long channel MOS)

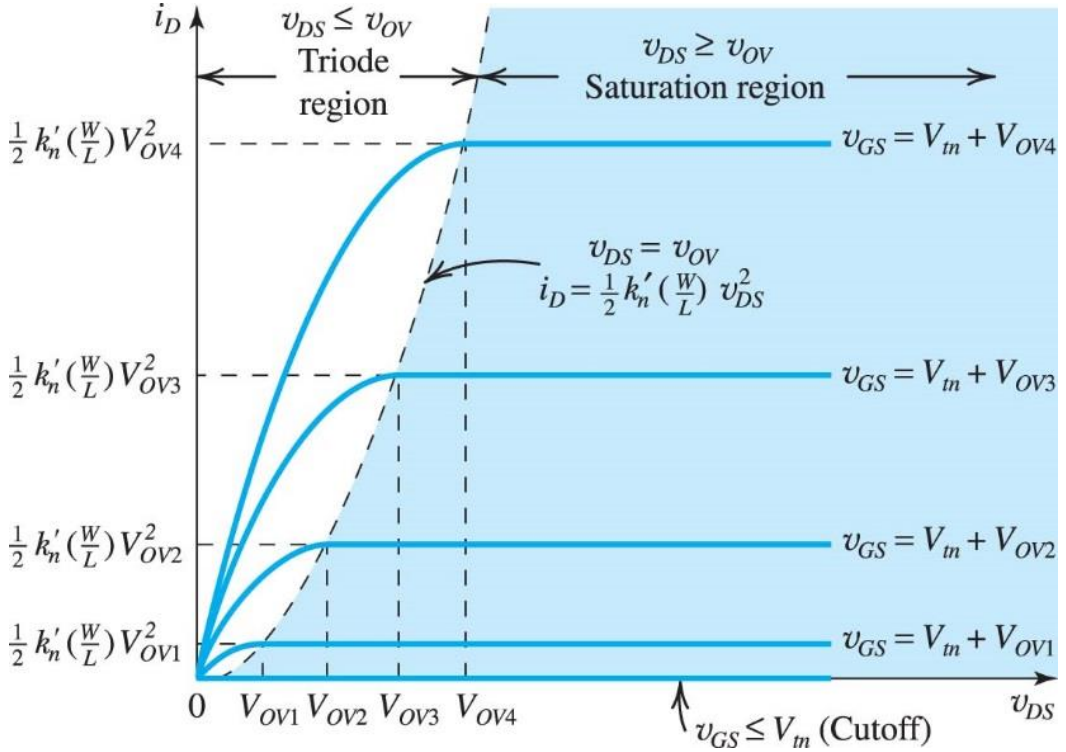
$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \cdot V_{ov}^2$$



IV Characteristics

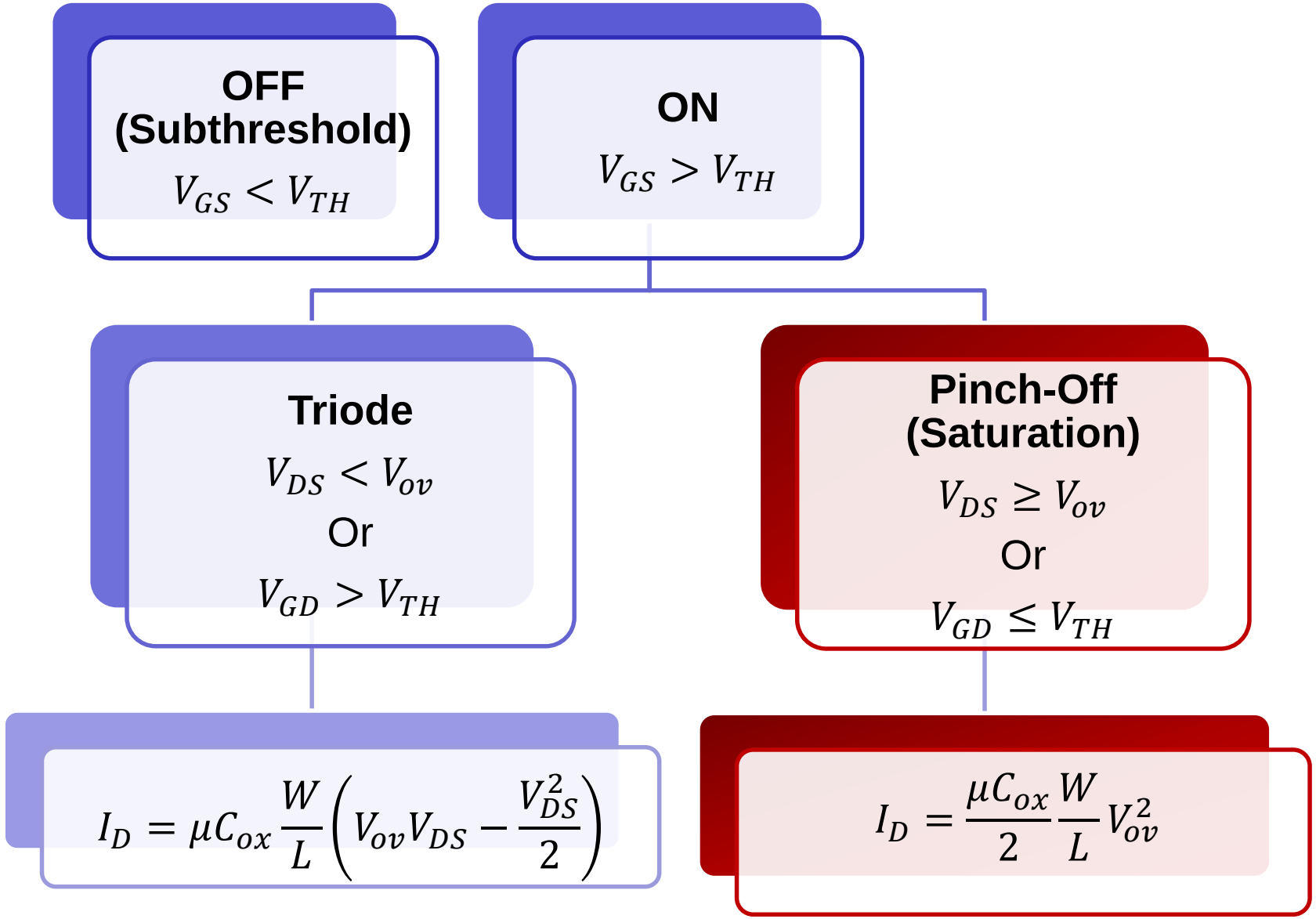
$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\cdot V_{ov}^2 = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\cdot (V_{GS} - V_{TH})^2$$





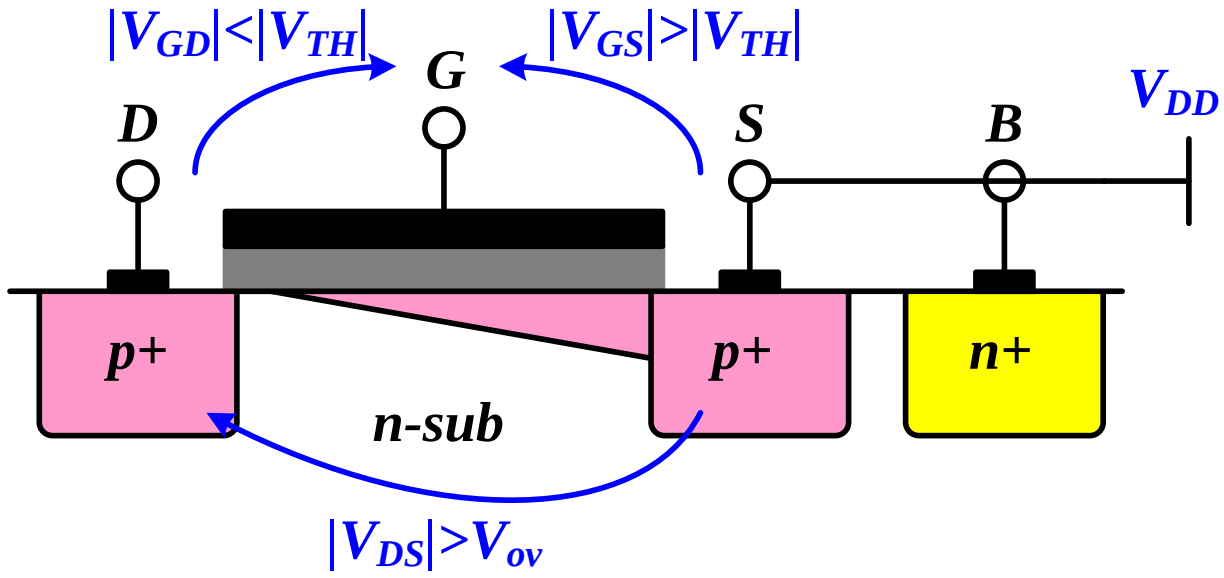
[Sedra/Smith, 2015]

Regions of Operation Summary



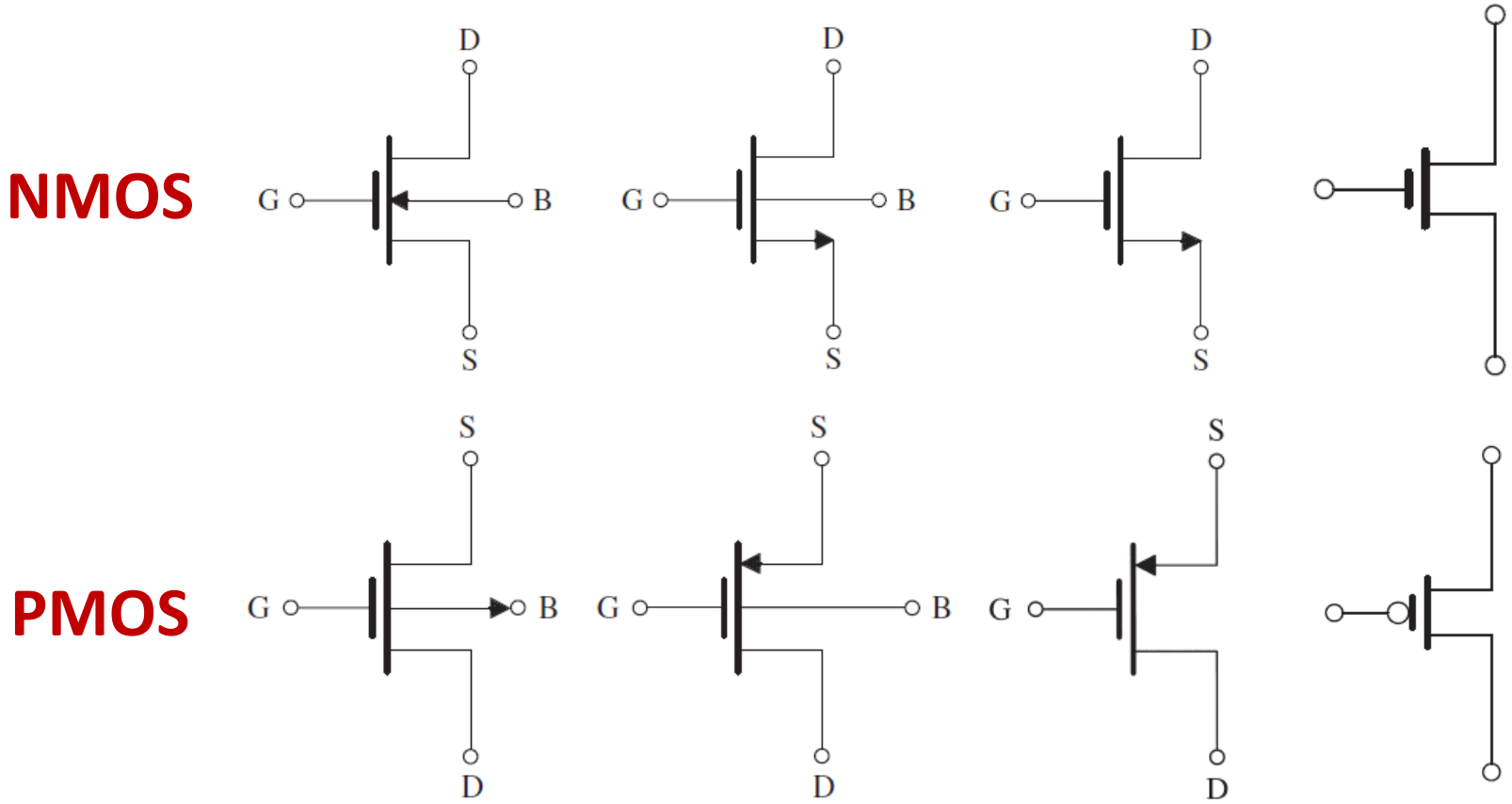
P-Channel MOSFET (PMOS)

- Electrons have higher mobility than holes (2 – 4 times)
- For same W/L and V_{ov}, NMOS current is 2 – 4 times higher than PMOS



MOSFET Symbols

- S/D junction diodes must be reverse-biased under all conditions
  - NMOS bulk connected to most negative potential (ground)
  - PMOS bulk connected to most positive potential (VDD)

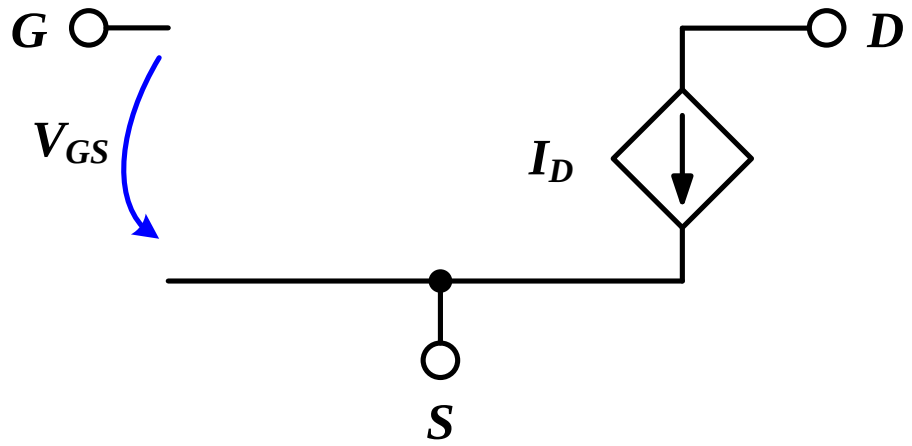


[Sedra/Smith, 2015]

Large Signal Model in Saturation

- Ideal VCCS: no dependence on V_{DS}

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L} \cdot V_{ov}^2 = \frac{\mu_n C_{ox}}{2}\frac{W}{L} \cdot (V_{GS} - V_{TH})^2$$

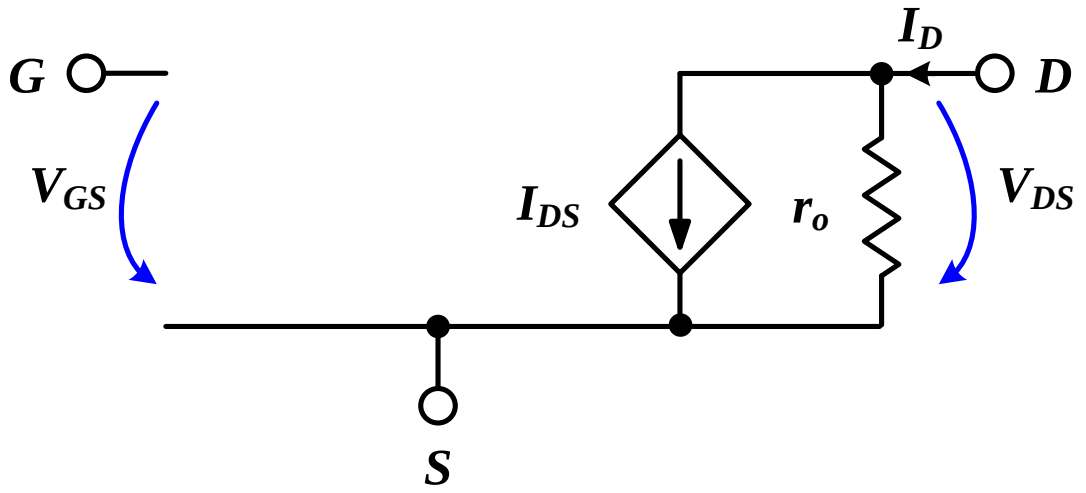


Large Signal Model with Finite Output Res

- The transistor is a VCCS
- The VCCS is not ideal: There is some dependence on V_{DS}

$$I_D = I_{DS} + \frac{V_{DS}}{r_o} = I_{DS}\left(1 + \frac{V_{DS}/I_{DS}}{r_o}\right)$$

$$I_{DS} = \frac{\mu C_{ox}}{2}\frac{W}{L}V_{ov}^2$$



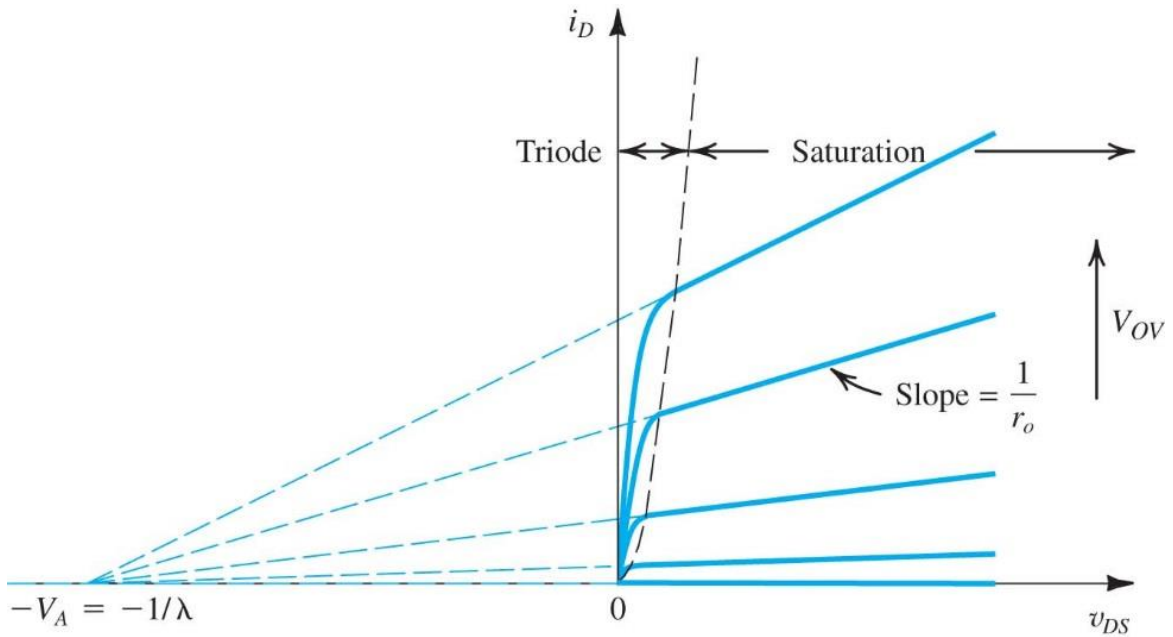
Channel Length Modulation (CLM)

- The VCCS is not ideal: There is some dependence on V_{DS}

$$r_o = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{\partial I_D / \partial V_{DS}} = \frac{1}{g_{ds}} = \frac{V_A}{I_{DS}} = \frac{1}{\lambda I_{DS}}$$

V_A: Early voltage ($V_A \propto L$) $\leftrightarrow$ λ: Channel length modulation coefficient ($\lambda \propto 1/L$)

$$I_D = I_{DS} + \frac{V_{DS}}{r_o} = I_{DS}\left(1 + \frac{V_{DS}/I_{DS}}{r_o}\right) = \frac{\mu C_{ox}}{2}\frac{W}{L}V_{ov}^2(1 + \lambda V_{DS})$$



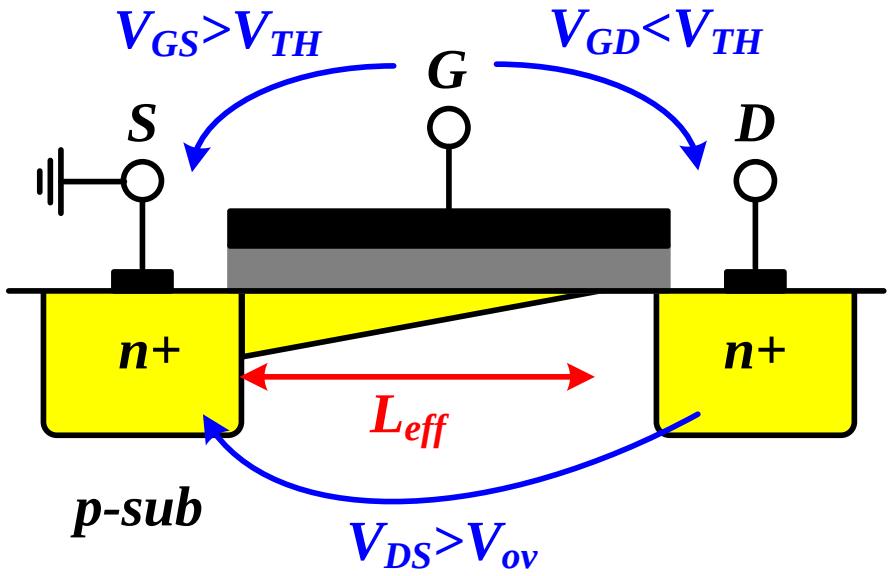
[Sedra/Smith, 2015]

Channel Length Modulation (CLM)

- L_{eff} decreases with V_{DS} → Shorter L gives more current
- V_A: Early voltage ($V_A \propto L$)
- λ: Channel length modulation coefficient ($\lambda \propto 1/L$)

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}V_{ov}^2(1+\lambda V_{DS}) \qquad r_o = \frac{V_A}{I_{DS}} = \frac{1}{\lambda I_{DS}}$$

- V_A increases with V_{DS}: higher r_o as we go deeper into saturation



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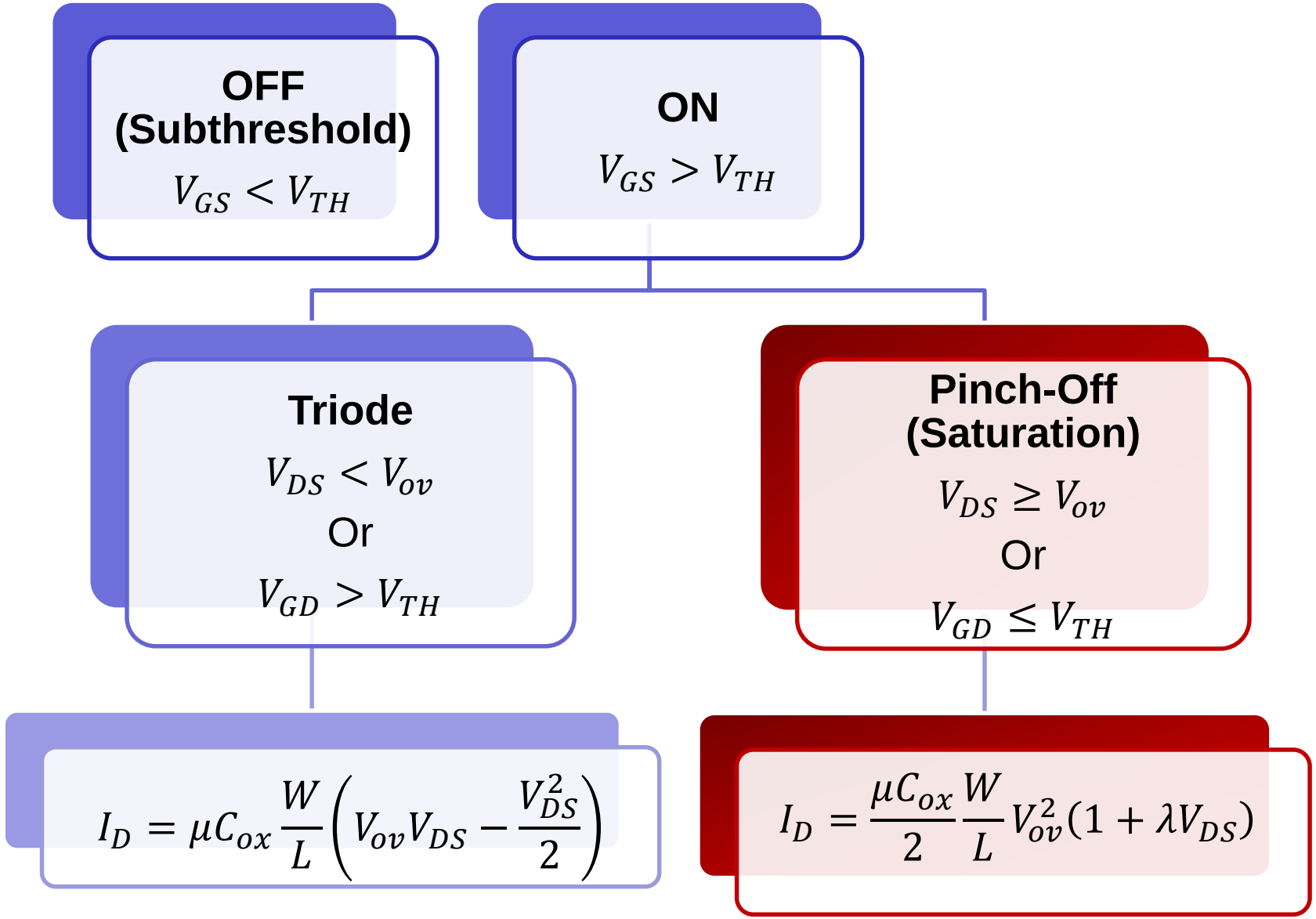
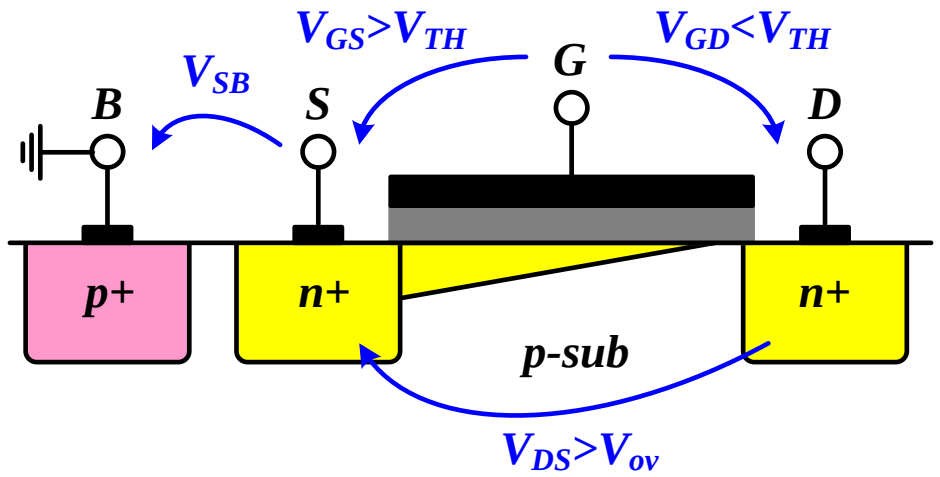


Body Effect

- V_{SB} affects the charge required to invert the channel
  - Increasing V_S or decreasing V_B increases V_{TH}

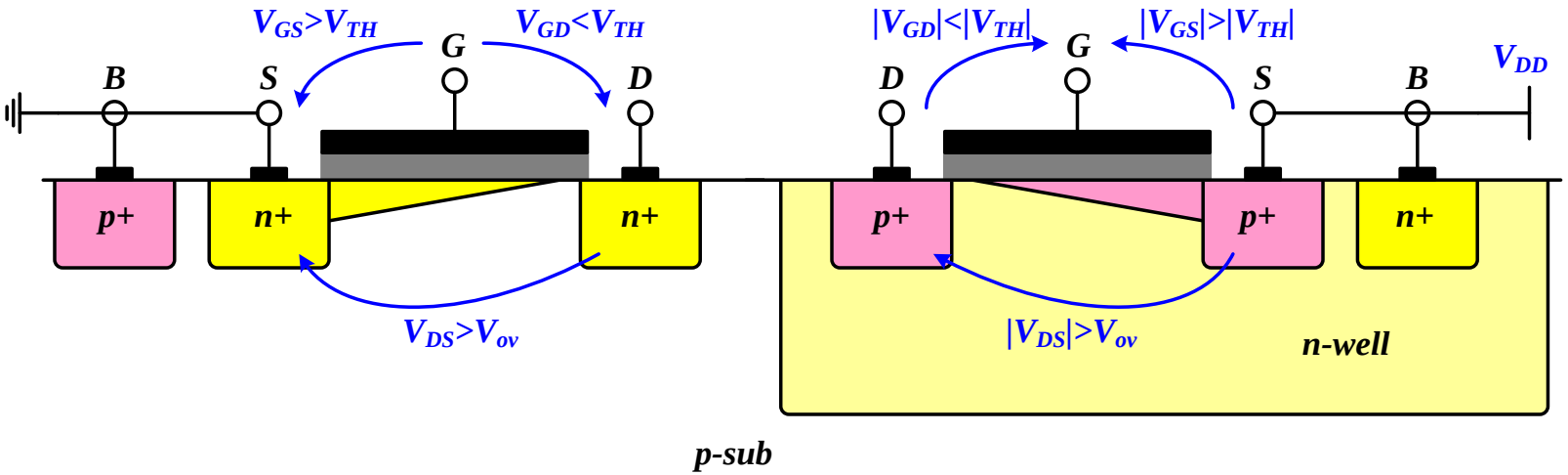
$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{|2\Phi_F|}\right)$$

  - Φ_F = surface potential at threshold
    - Depends on doping level and intrinsic carrier concentration n_i
  - γ = body effect coefficient
    - Depends on C_{ox} and doping



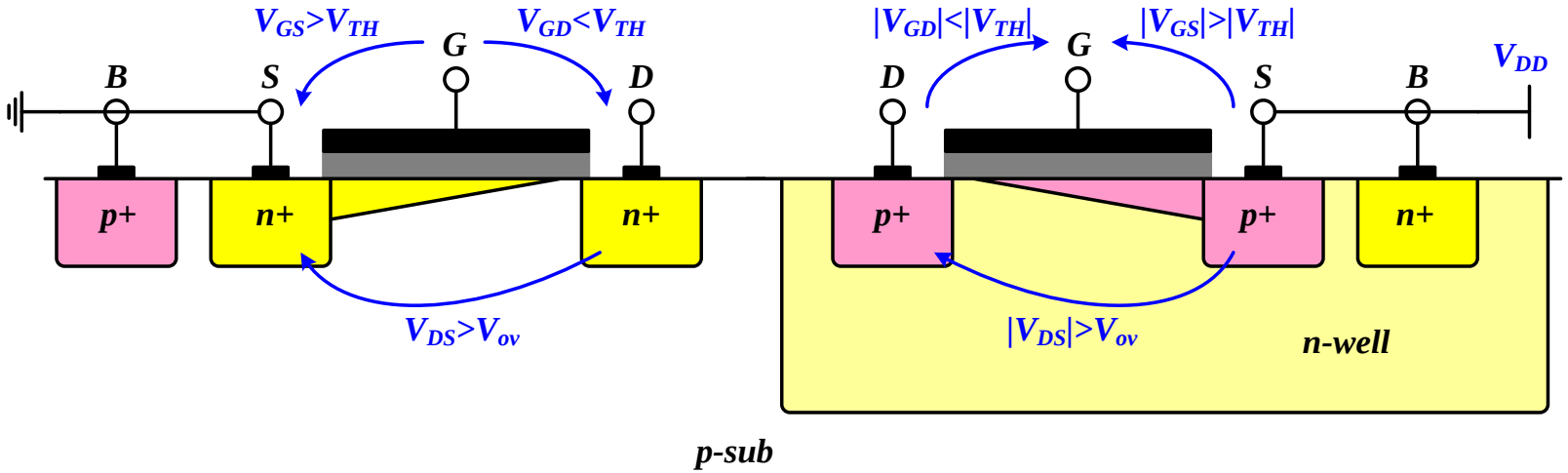
CMOS

- CMOS = NMOS + PMOS on the same substrate
- S/D junction diodes must remain reverse-biased
  - NMOS bulk connected to most negative potential (ground)
  - PMOS bulk connected to most positive potential (VDD)



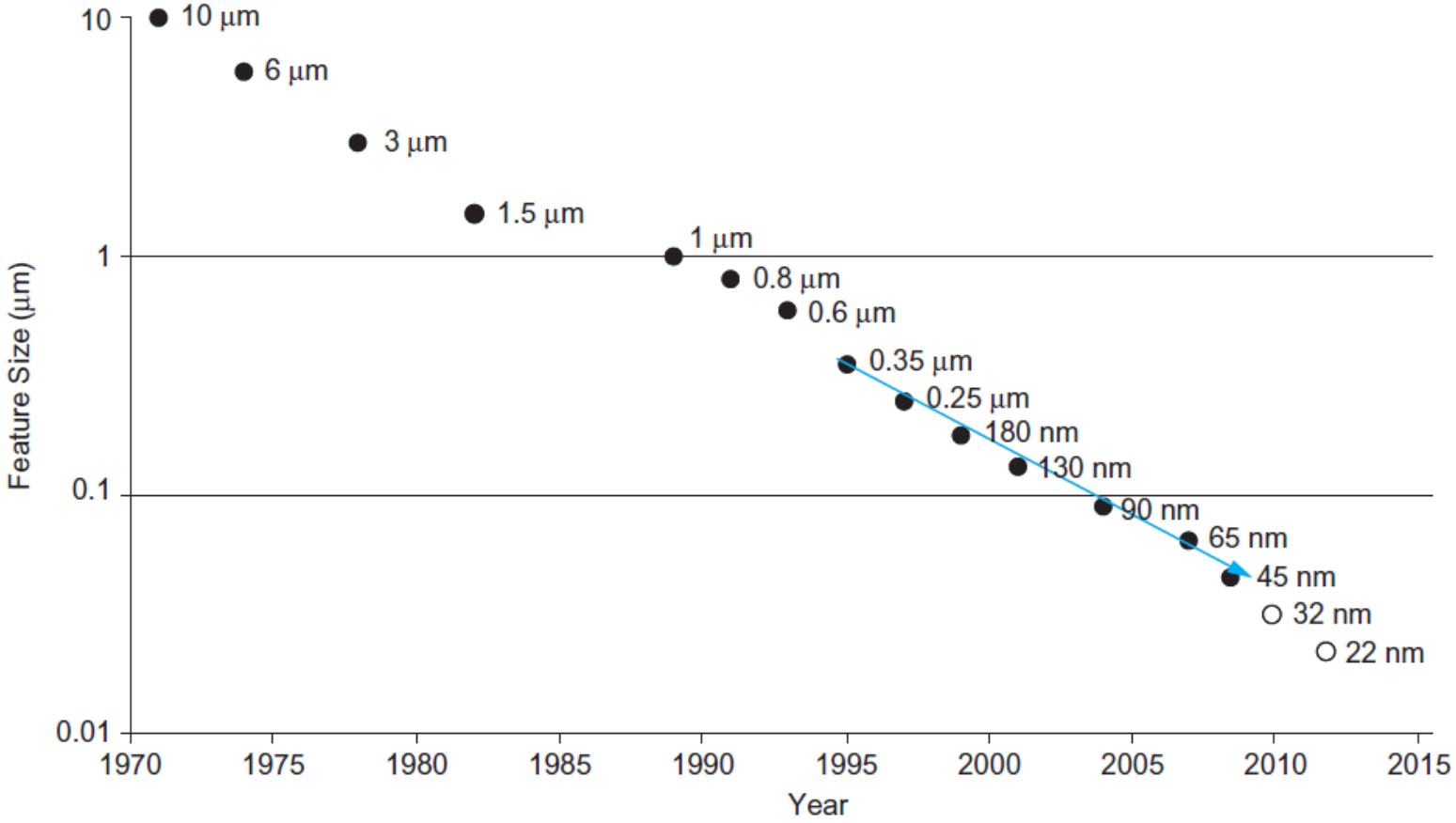
CMOS

- CMOS = NMOS + PMOS on the same substrate
- All NFETs share the same substrate
  - If source is floating then will have body effect
- Each PFET can have an independent n-well
  - Connect body to floating source to avoid body effect
- NFET can be placed in a “private” well in twin/triple-well technologies



CMOS Technology Scaling: Moore's Law

- Min feature size (L_{min}) shrinking 30% ($\approx 1/\sqrt{2}$) every 2-3 years
  - Transistor area (and cost) are reduced by a factor of 2
- Device scaling brings new challenges in circuit design



[Weste and Harris, 2010]

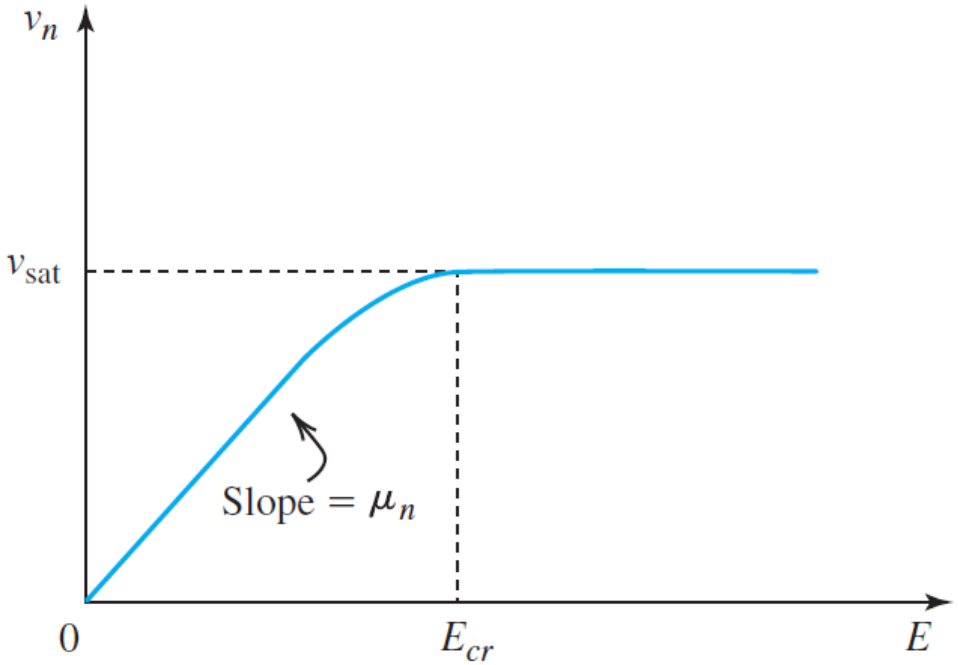
Short Channel Effects: Velocity Saturation

- For deep-submicron MOSFET with short channel length ($L < 0.25\mu m$) the lateral electric field is very high

$$E = \frac{V_{DS}}{L}$$

- @ $E = E_{cr}$ ($V_{DS} = V_{DSsat}$) the velocity of the carriers saturates

$$v_{sat} = \mu E_{cr} = \mu \frac{V_{DSsat}}{L} \approx 10^7 cm/s$$



[Sedra/Smith, 2015]

Velocity Saturation: IV Characteristics

- Long channel: Triode region

$$I_D = \mu_n C_{ox} \frac{W}{L} \cdot \left(V_{ov} - \frac{V_{DS}}{2} \right) \cdot V_{DS}$$

- Velocity sat happens before pinch-off if $V_{DSsat} < V_{ov}$
  - Replace V_{DS} with V_{DSsat} and $v = \mu_n \frac{V_{DS}}{L}$ with $v_{sat} = \mu_n \frac{V_{DSsat}}{L}$

$$I_D = \mu_n C_{ox} \frac{W}{L} \cdot \left(V_{ov} - \frac{V_{DSsat}}{2} \right) \cdot V_{DSsat} = C_{ox} W v_{sat} \cdot \left(V_{ov} - \frac{V_{DSsat}}{2} \right)$$

  - Including channel length modulation effect (the physical reason is different, but the effect on I_D is the same)

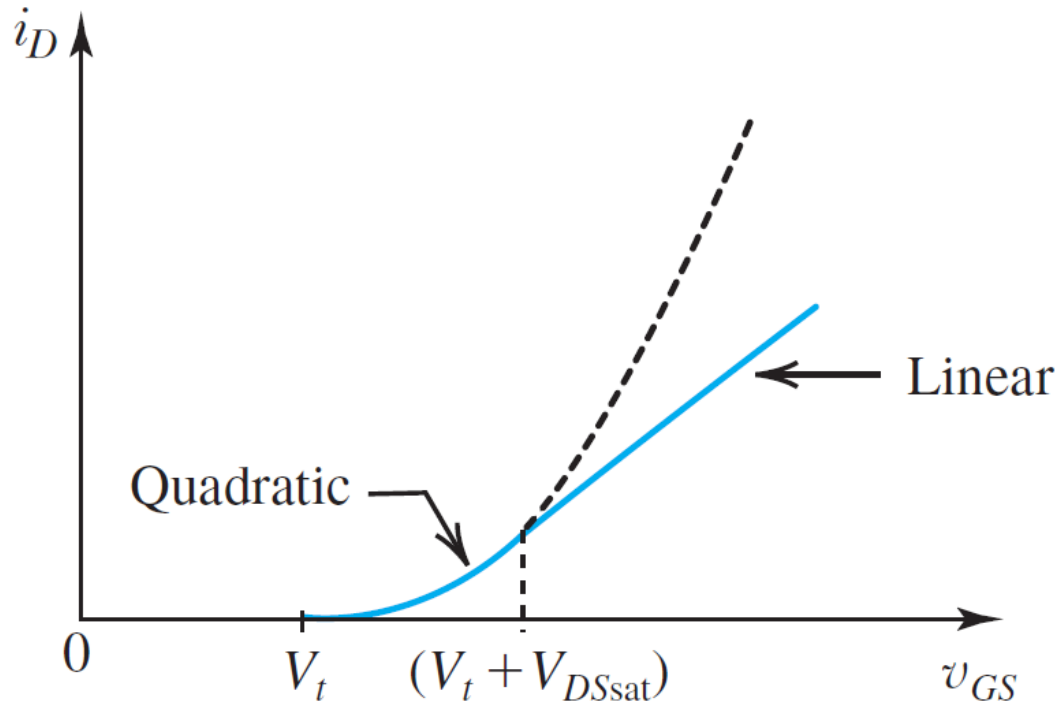
$$I_D = C_{ox} W v_{sat} \cdot \left(V_{ov} - \frac{V_{DSsat}}{2} \right) (1 + \lambda V_{DS})$$

  - (1) Current independent of L and (2) linear dependence on V_{ov}

Velocity Saturation: IV Characteristics

- Velocity sat happens before pinch-off if $V_{DSsat} < V_{ov}$

$$I_D = C_{ox} W v_{sat} \cdot \left(V_{ov} - \frac{V_{DSsat}}{2} \right) (1 + \lambda V_{DS})$$



[Sedra/Smith, 2015]

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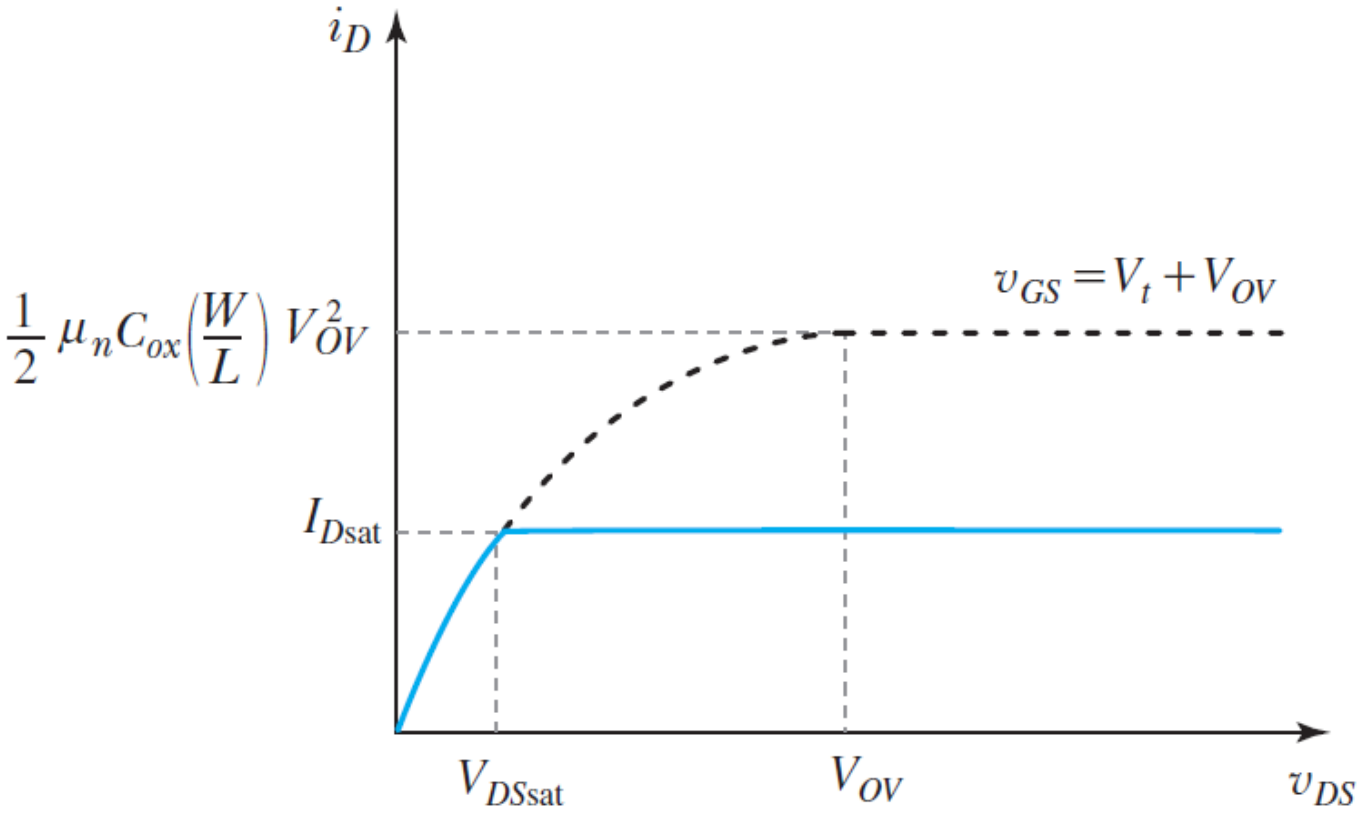

[Sedra/Smith, 2015]

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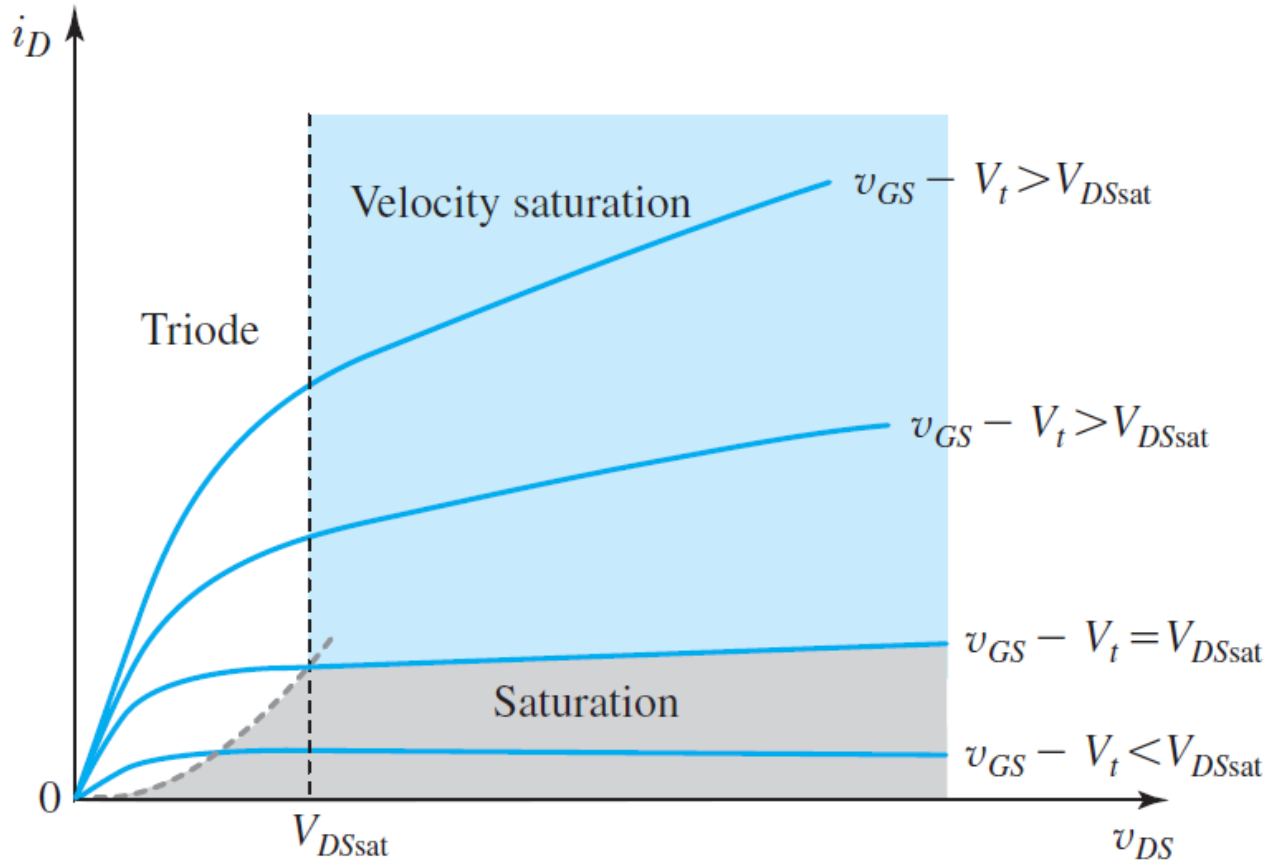


[Sedra/Smith, 2015]

Short Channel Effects: Mobility Degradation

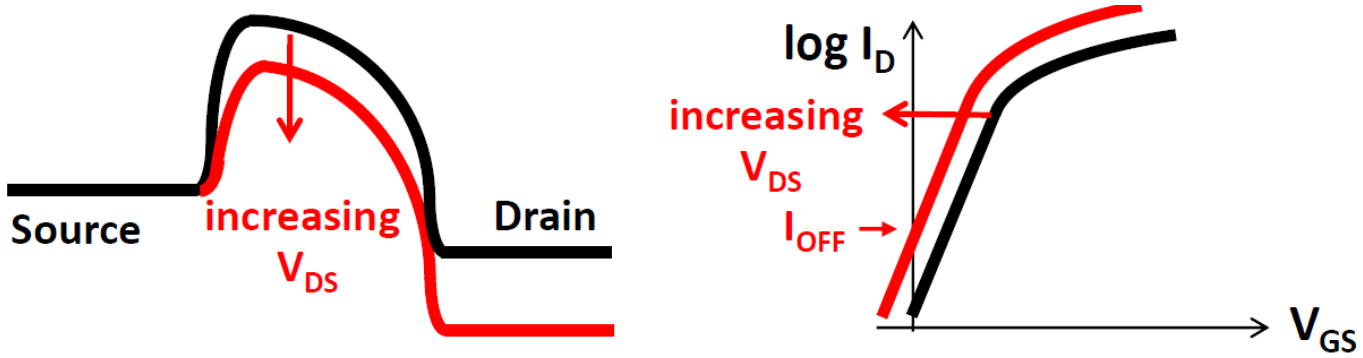
- Vertical electric field: $E_{vert} = V_{GS}/t_{ox}$
  - Attracts carriers into channel
  - Long channel: $Q_{channel} \propto E_{vert}$
- At high vertical field strengths (V_{GS}/t_{ox})
  - The carriers scatter off the oxide interface more often
  - Scattering slows carrier progress
  - Leads to less current than expected at high V_{GS}
- Mobility degradation can be modeled by replacing μ with a smaller μ_{eff} that is a function of V_{GS}

Short Channel Effects: DIBL

- DIBL: Drain-Induced Barrier Lowering
- Electric field from drain affects threshold voltage
  - More pronounced in short channel devices

$$V'_{TH} = V_{TH} - \eta V_{DS}$$

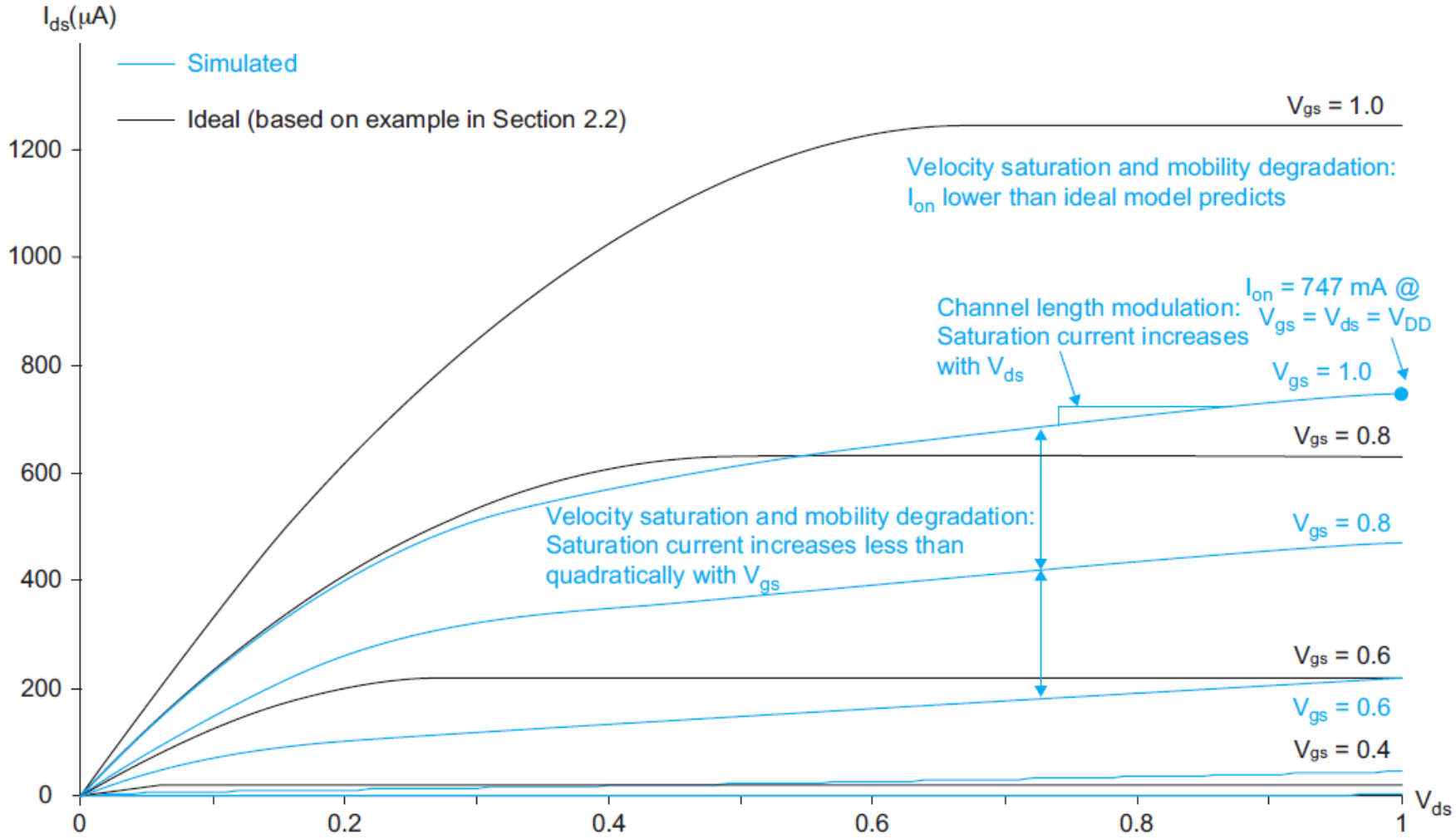
  - η: DIBL coefficient $\sim 100mV/V$
- High drain voltage causes current to increase (similar to channel length modulation)
- **Gate is losing control over the channel**



[Tsu-Jae King Liu, Berkeley, 2012]

Short-Channel MOSFET I-V Ccs

- 65 nm IBM process, V_{DD} = 1.0 V



[Weste & Harris, 2010]

Why Do We Still Learn Square-Law?

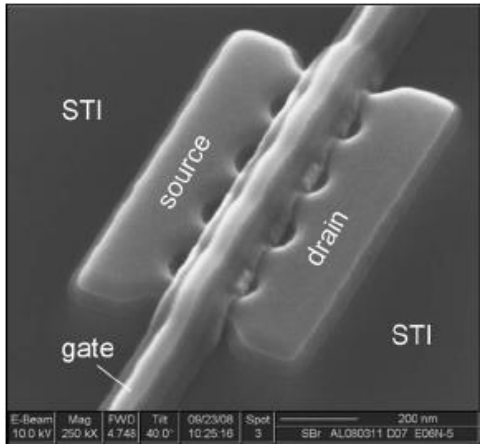
- For digital and RF, use min L
  - You care most about speed and power
- For analog, we use relatively long L
  - We care about matching, gain, and low-frequency noise
- For digital V_{ov} is large $= V_{DD} - V_{TH}$
  - Short channel effects (e.g., velocity sat.) are more pronounced
- For analog V_{ov} is relatively low
  - Short channel effects (e.g., velocity sat.) are less pronounced
- Simple model provides a great deal of intuition that is necessary in analog design
  - We must simulate the circuit to get more accurate results

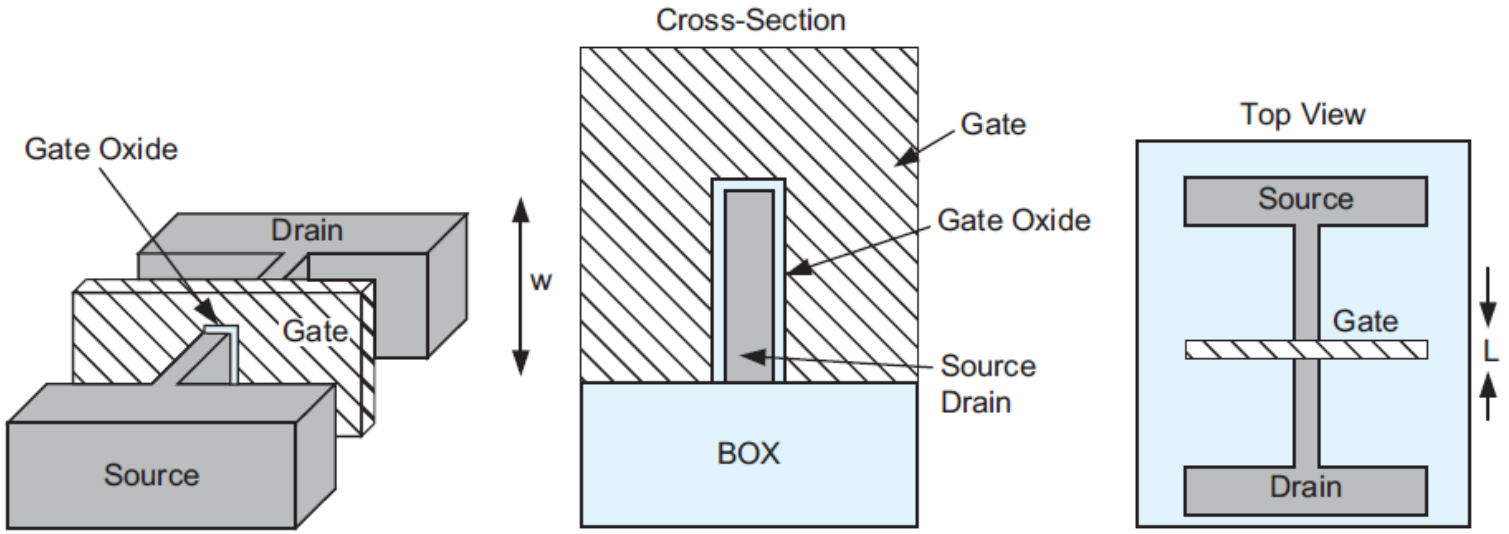
Is the Square-Law Still Valid?

- Valid "relatively" if
  - Relatively long channel length
  - Strong inversion, but not too strong (e.g., $V_{ov} \approx 100 - 300mV$)
    - For small and negative V_{ov}: moderate and weak inversion (subthreshold operation)
      - ID-VGS relation gradually becomes exponential
    - For large V_{ov}: velocity saturation happens before pinch-off
      - ID-VGS relation becomes linear
- If the above conditions are not valid
  - Use design charts or look-up tables, e.g., gm/ID design methodology (to be explained later)
- Actually, better to use gm/ID methodology even if the above conditions are valid!

FinFET

- Planar CMOS cannot be scaled below 20nm due to excess leakage current and severe short channel effects
- FinFET: gate has better control on the channel
  - Intel's version is called trigate FET
  - Generally: multigate transistor
- In the future: Gate-all-around





[Weste & Harris, 2010]

Thank you!

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- B. Razavi, “Fundamentals of Microelectronics,” Wiley, 2nd ed., 2014.
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