Lab 7

OTA Design

Part 1: gm/ID Design Charts

NMOS Charts:

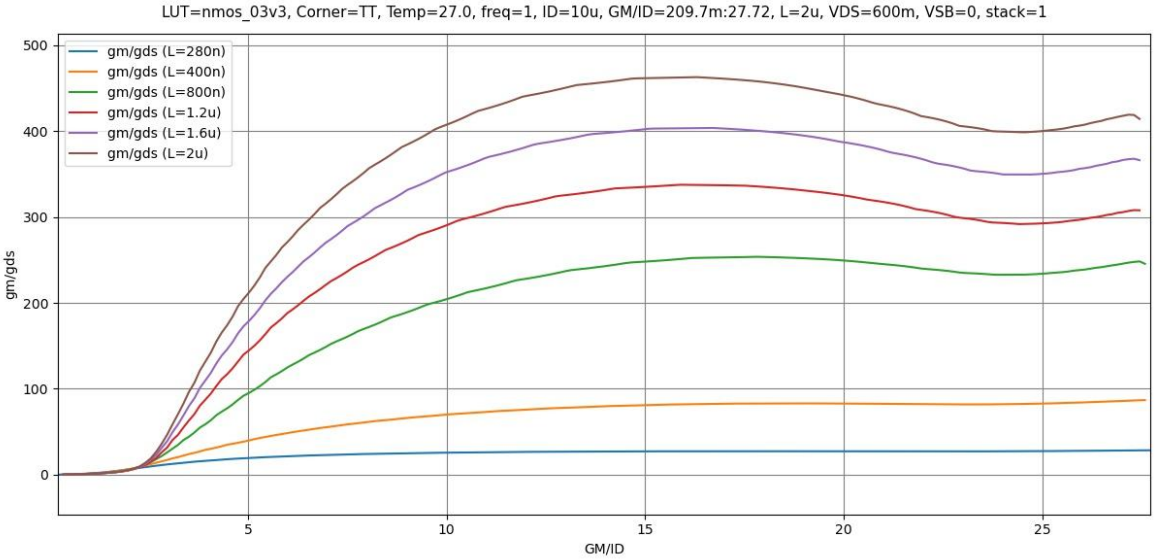


Figure 1 gm/gds vs gm/id

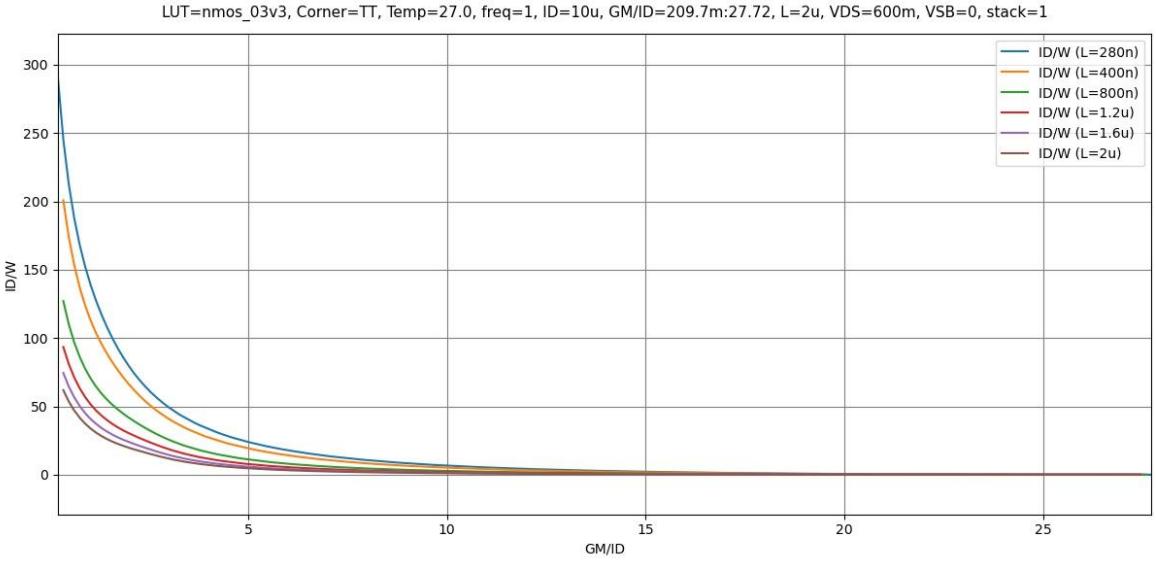


Figure 2 ID/W vs gm/ID

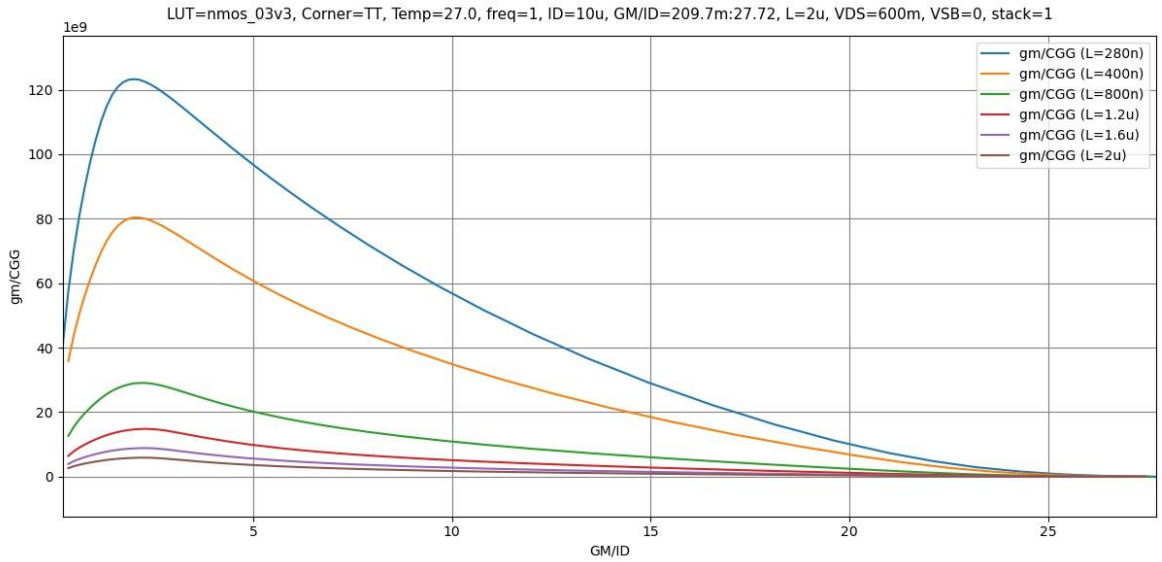


Figure 3 gm/Cgg vs gm/ID

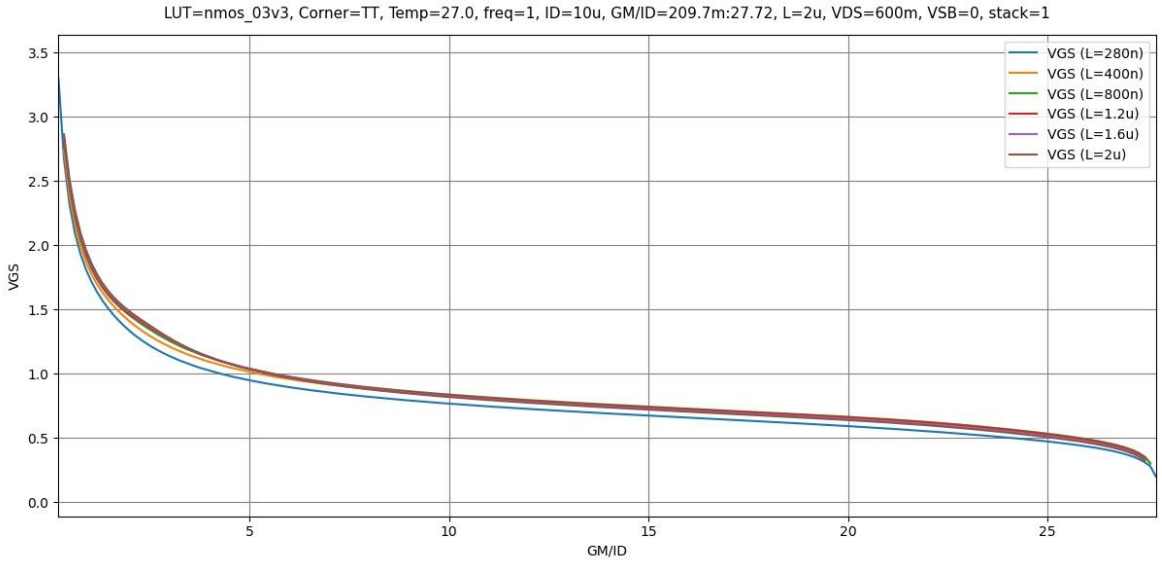


Figure 4 VGS vs gm/ID

PMOS Charts:

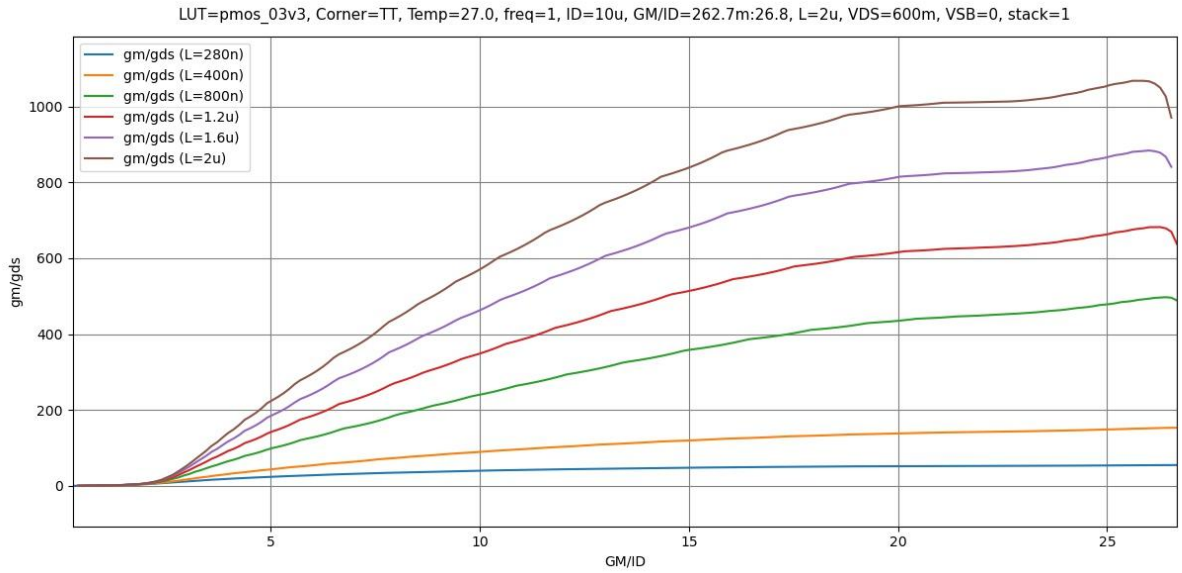


Figure 5 gm/gds vs gm/ID

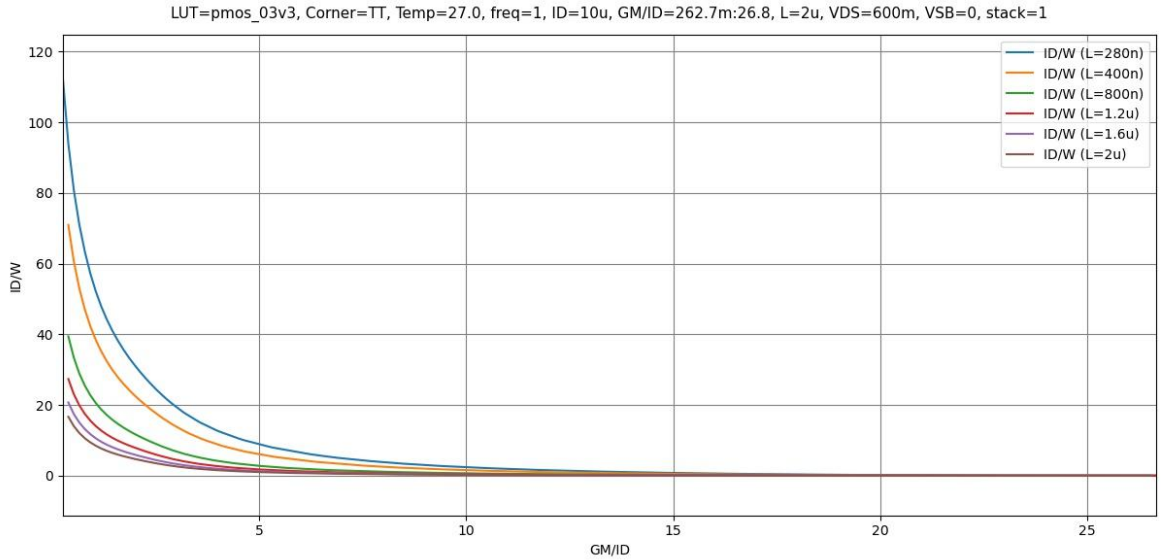


Figure 6 ID/W vs gm/ID

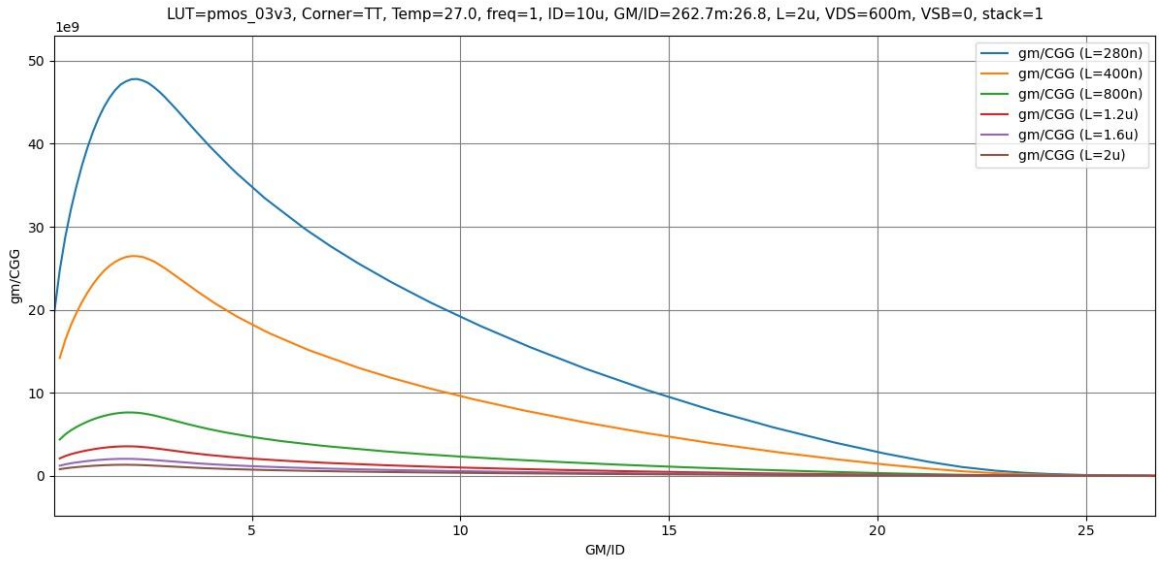


Figure 7 gm/Cgg vs gm/ID

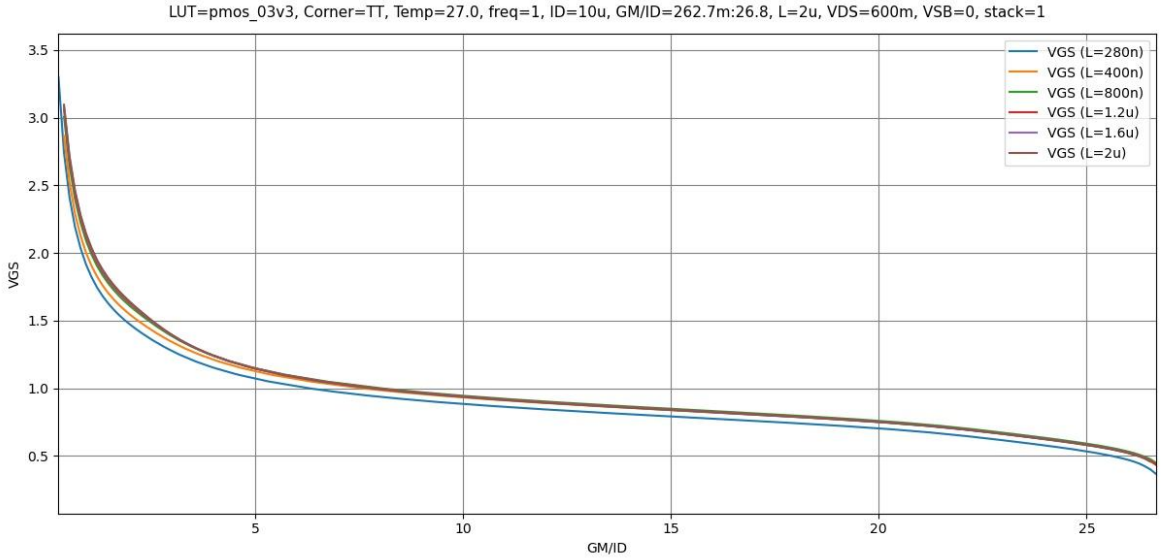


Figure 8 VGS vs gm/ID

Part 2: OTA Design

Required Specifications:

Technology	0.18um CMOS
Supply voltage	1.8V
Load	5pF
Open loop DC voltage gain	>= 34dB
CMRR @ DC1	>= 74dB
Phase margin	>= 70°
CM input range – low	<= 1V
CM input range – high	>= 1.5V
GBW	>= 10MHz

Design Observations:

- The Gain required isn't too large and easily achievable using a single stage OTA
- The CMIR required is close to the Supply Rail, Thus an NMOS input stage is preferred.
- The specification can be met using a 5T-OTA topology

We have to size 3 pairs of MOSFETS.

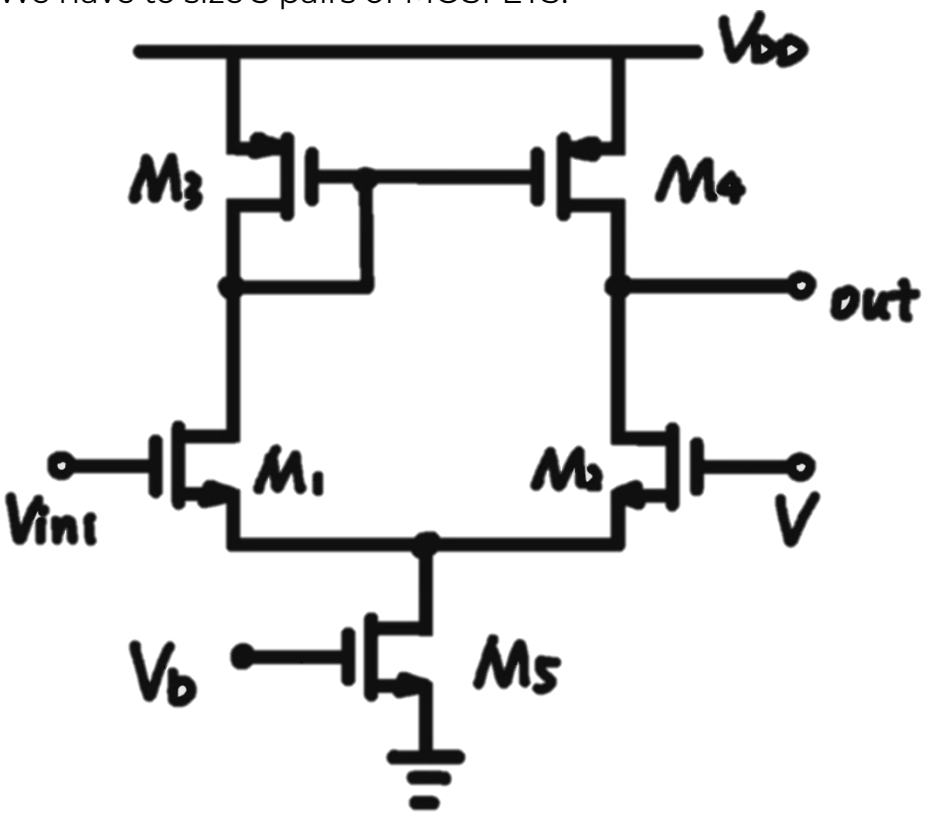


Figure 9 5T OTA Topology

Input Transistors:

$$GBW \approx \frac{GM}{C_L} = \frac{gm_{1,2}}{2\pi C_L} = 10MHz \rightarrow gm_{1,2} = 314.16\mu s \approx \mathbf{320\mu s}$$

$$A_{OL} \geq 34dB \rightarrow 50.11 \approx \frac{gm_{1,2}ro}{2} (Assuming\ Both\ NMOS\ and\ PMOS\ have\ the\ same\ gds)$$

$$\rightarrow \boldsymbol{ro = 312.5K\Omega}$$

$$Assume\ \frac{gm}{I_D} = 15\ In\ Monderate\ Conversion \rightarrow I_D = 21.3\mu A \approx \mathbf{20\mu A}$$

Assuming the Voltage Drop is divided equally across all 3 transistors in branch, VDS of each transistor = 0.6V
M1,2 Experience Body Effect, thus VSB = 0.6
We may assume a lesser voltage drop at the bottom transistor to 0.3 thus Vds = 0.9V

Using these three parameters we can get the width and length of the input pair quickly using ADT:

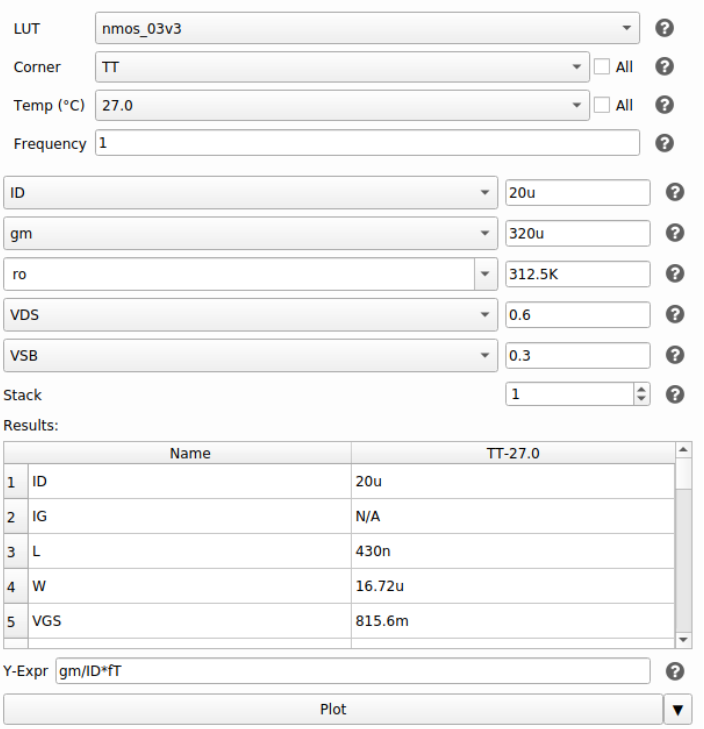


Figure 10 Intial Values for the input pair from SA

$$\boldsymbol{L = 430nm} \quad , \quad \boldsymbol{W = 16.72\mu m}$$

These are acceptable values for the Input Pair and decent for initial design!

PMOS Current Mirror Load:

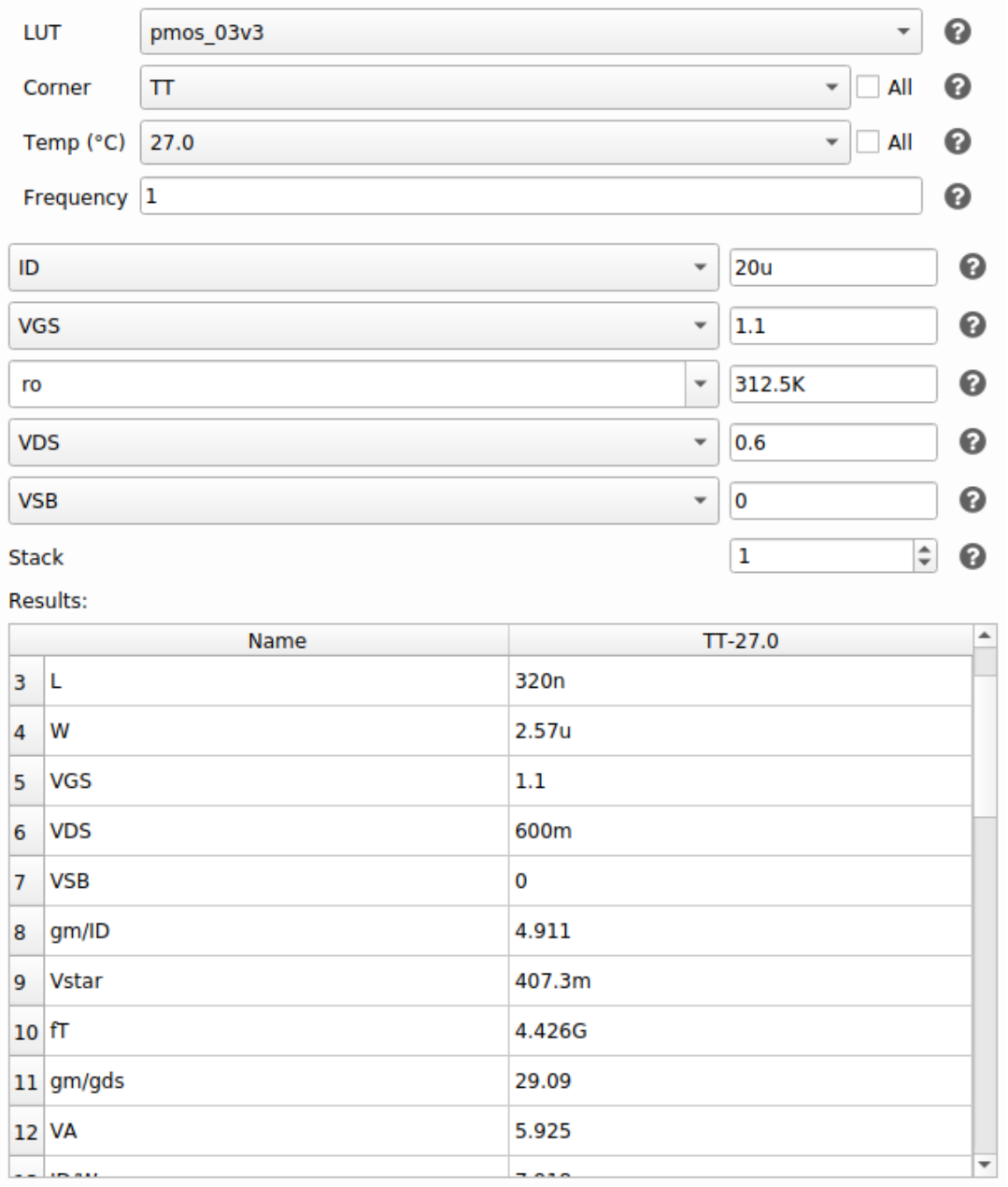
Using CMIR-Max:

$$CMIR_{MAX} = 1.5 = V_{DD} + Vth_{1,2} - Vgs_{3,4}\ (Using\ Value\ of\ Vth_{,2}\ from\ SA)$$
$$\rightarrow\ Vgs_{3,4} = 1.09 \approx 1.1V$$

Using assumptions from the previous part:

$$ro = 312.5K\Omega \quad , \quad V_{DS} = 0.6V \quad , \quad I_D = 20\mu A$$

Plugging in these Values in ADT SA we get:



	Name	TT-27.0
3	L	320n
4	W	2.57u
5	VGS	1.1
6	VDS	600m
7	VSB	0
8	gm/ID	4.911
9	Vstar	407.3m
10	fT	4.426G
11	gm/gds	29.09
12	VA	5.925

Figure 11 Initial Values for the PMOS Current Mirror Load Pair from SA

$$\boldsymbol{L = 320nm \quad , \quad W = 2.57\mu m}$$

These are acceptable values for the Input Pair and decent for initial design!

Tail Current Mirror Sizing:

For the purposes of this design, I will use a simple current mirror at the tail.

Using the spec for CMRR:

$$CMRR = 74dB = A_d - A_{CM} \rightarrow A_{CM} = -40dB$$

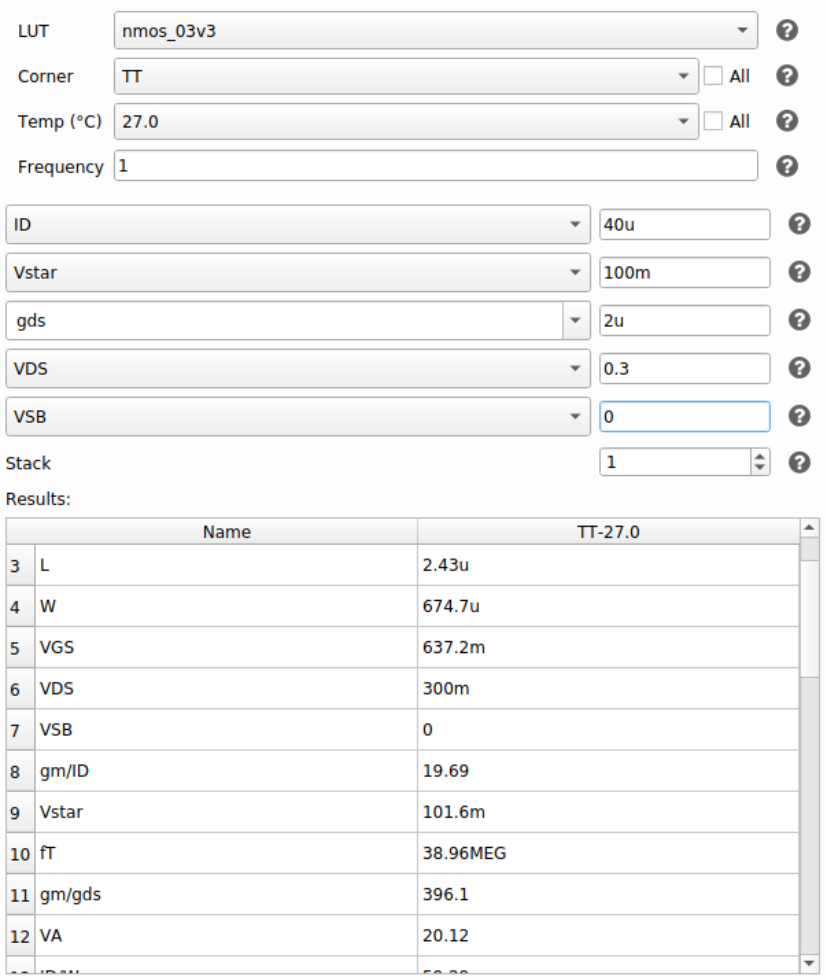
$$\rightarrow A_{CM} = 0.01 \approx \frac{1}{2gm_{3,4}ro_5} \rightarrow \frac{1}{ro_5} = gds_5 \approx \mathbf{2\mu s}\ (Using\ Values\ of\ gm_{3,4}\ from\ SA)$$

Using the Spec for CMIR-Low:

$$CMIR_{Low} = 1V = Vgs_{1,2} + V_5^* \rightarrow V_5^* = 100mV\ (Extremely\ Low)$$

$$ID = 40\mu s \rightarrow From\ previous\ assumption, twice\ the\ current\ flows\ in\ the\ tail\ source$$

Plugging in these Values into ADT SA:



	Name	TT-27.0
3	L	2.43u
4	W	674.7u
5	VGS	637.2m
6	VDS	300m
7	VSB	0
8	gm/ID	19.69
9	Vstar	101.6m
10	fT	38.96MEG
11	gm/gds	396.1
12	VA	20.12

Figure 12 Initial Values for the Tail Current Mirror Load Pair from SA

$$\boldsymbol{L = 2.43\mu m} \quad , \quad \boldsymbol{W = 674.7\mu m}$$

The Value for the width is extremely high especially considering I need to multiply it by 4 for the mirroring ratio.
Thus I will assume an initial Value of W of 40um and slightly increase the Width of M1,2 then iterate the design till I reach acceptable Values for the transistor that satisfy the specifications.

Initial Design Point:

	M1,2	M3,4	M5,6
W	16.72um	320nm	40um
L	430nm	2.57um	2.43um
ID	20uA	20uA	40uA
gm/ID	16	20	9.2
VDsat	101.4mV	62.6mV	169.5mV
Vov	25.91mV	-22.39mV	170.8mV
Vstar	125mV	100mV	217.4mV

Simulation and Design Iteration:

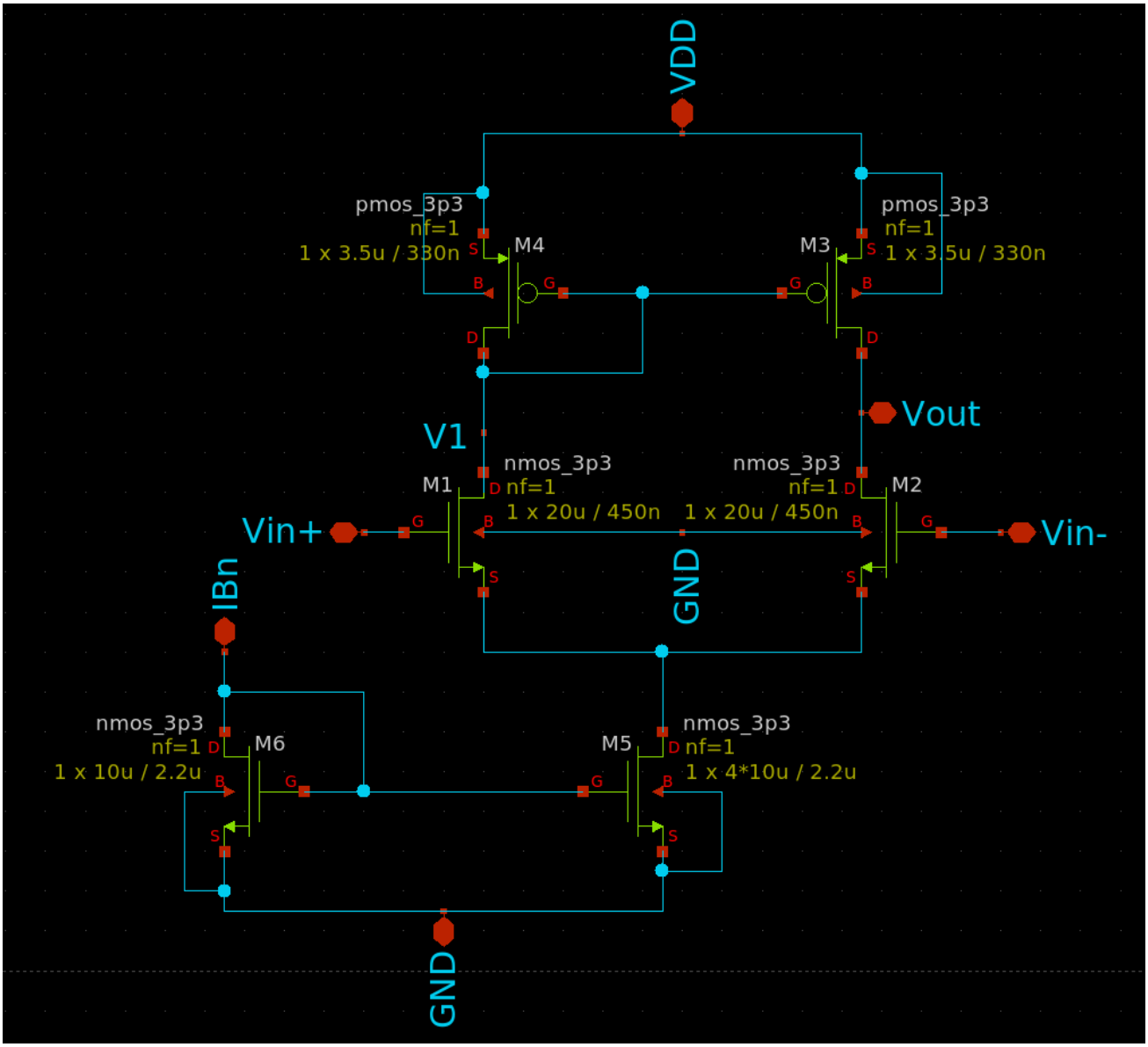


Figure 13 5T OTA Schematic After Iterations

After very Few iterations these are the values, I reached for all transistors that satisfy all specs.

Final Design Point:

	M1,2	M3,4	M5,6
W	20um	3.5um	40um
L	450nm	330nm	2.2um
ID	20uA	20uA	40uA
gm/ID	11	5	5
VDsat	156.1mV	303.9mV	300mV
Vov	131.5mV	307.3mV	389.2mV
Vstar	181.8mV	389.5mV	422mV

These values were calculated at different VDS and VSB values matching the assumptions we did during the design stage but they differ greatly when doing the simulation as we'll see in the following results.

Simulation and Results:

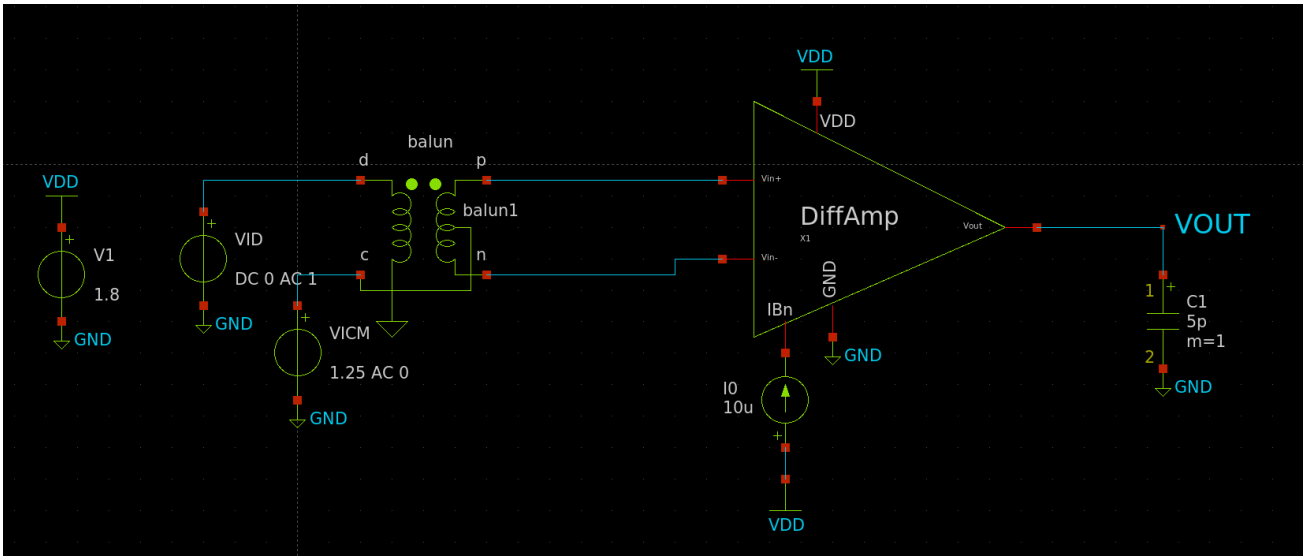


Figure 14 Testbench Schematic for first part

OP Analysis:

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm6.m0	m.x1.xm5.m0	m.x1.xm3.m0
model	nmos_3p3.10	nmos_3p3.14	pmos_3p3.8
id	1e-05	3.96813e-05	1.98407e-05
gm	9.78173e-05	0.000388802	0.000118359
gmbs	3.84057e-05	0.000152628	4.48114e-05
gds	1.92449e-07	1.1972e-06	2.12881e-06
vgs	0.822205	0.822205	1.04297
vth	0.667182	0.667182	0.755456
vds	0.822204	0.405529	1.04297
vdsat	0.161448	0.161448	0.28813

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm4.m0	m.x1.xm2.m0	m.x1.xm1.m0
model	pmos_3p3.8	nmos_3p3.12	nmos_3p3.12
id	1.98407e-05	1.98407e-05	1.98407e-05
gm	0.000118359	0.000324666	0.000324666
gmbs	4.48114e-05	8.88576e-05	8.88576e-05
gds	2.12881e-06	3.83417e-06	3.83417e-06
vgs	1.04297	0.844467	0.844467
vth	0.755456	0.828147	0.828147
vds	1.04297	0.351485	0.351485
vdsat	0.28813	0.097195	0.097195

Figure 15 OP Analysis Results for all transistors

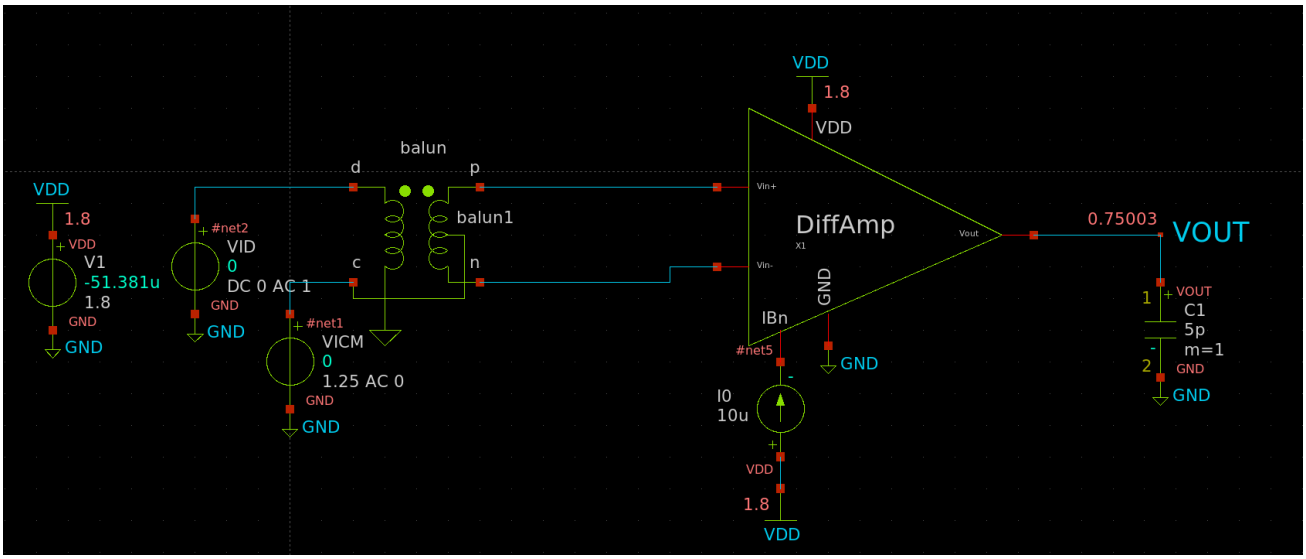


Figure 16 DC Voltages Annotated in Testbench

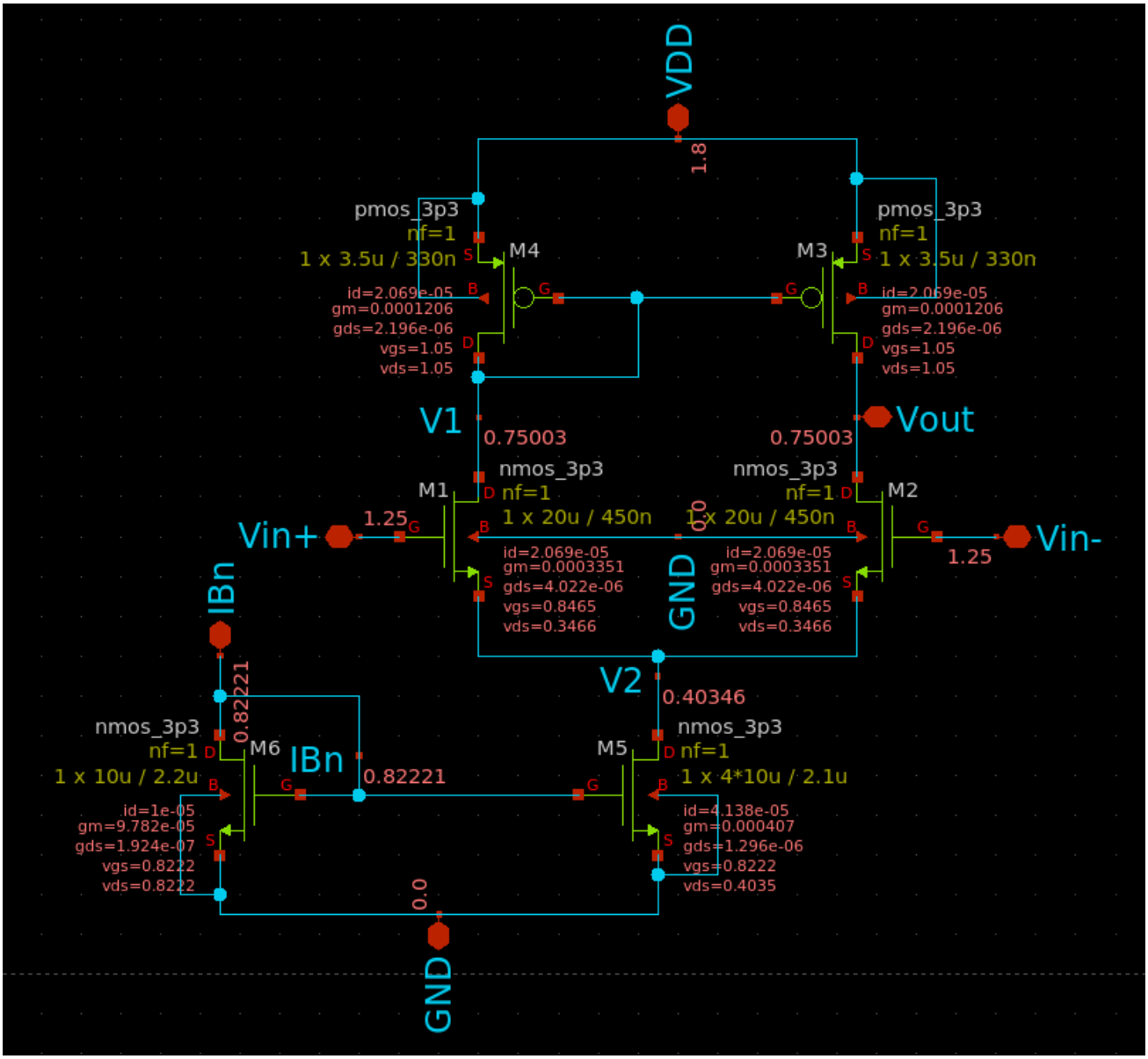


Figure 17 Voltages Annotated on 5T OTA Schematic

- **Is the current (and gm) in the input pair exactly equal?**

Yes, the current is exactly equal in both transistors of the input pair.

- **What is DC voltage at VOUT? Why?**

$$V_{out} = 0.75003$$

$$V_{out} = V_{DD} - V_{GS3,4} = 1.8 - 1.05 = \mathbf{0.75V}$$

There's a virtual short-circuit between the drain and gate of M3 cause both Vout and V1 to have the same voltage.

Differential Small Signal:

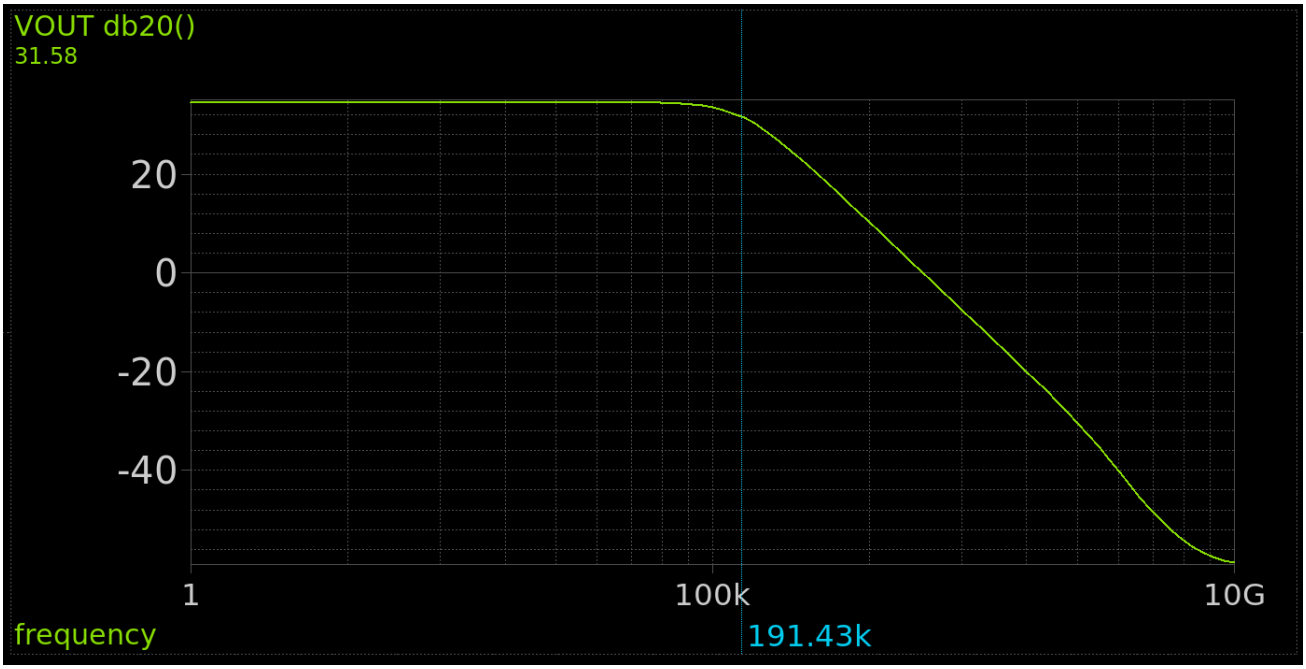


Figure 18 Diff Gain (dB)vs Frequency

```
gain                    =   5.341524e+01
gain_db = 3.455330e+01
```

Figure 19 Diff Gain Values

Hand Analysis:
Using Values from OP Analysis:

$$|A_{vd}| = gm_{1,2}(ro_{1,2} // ro_{3,4}) = 54.46 \rightarrow 34.7213\ dB$$

	Simulation	Hand Analysis
Gain	53.415	54.46
Gain (dB)	34.55	34.7213

Hand analysis and simulation results agree with each other and satisfy the required spec.

CM Small Signal:

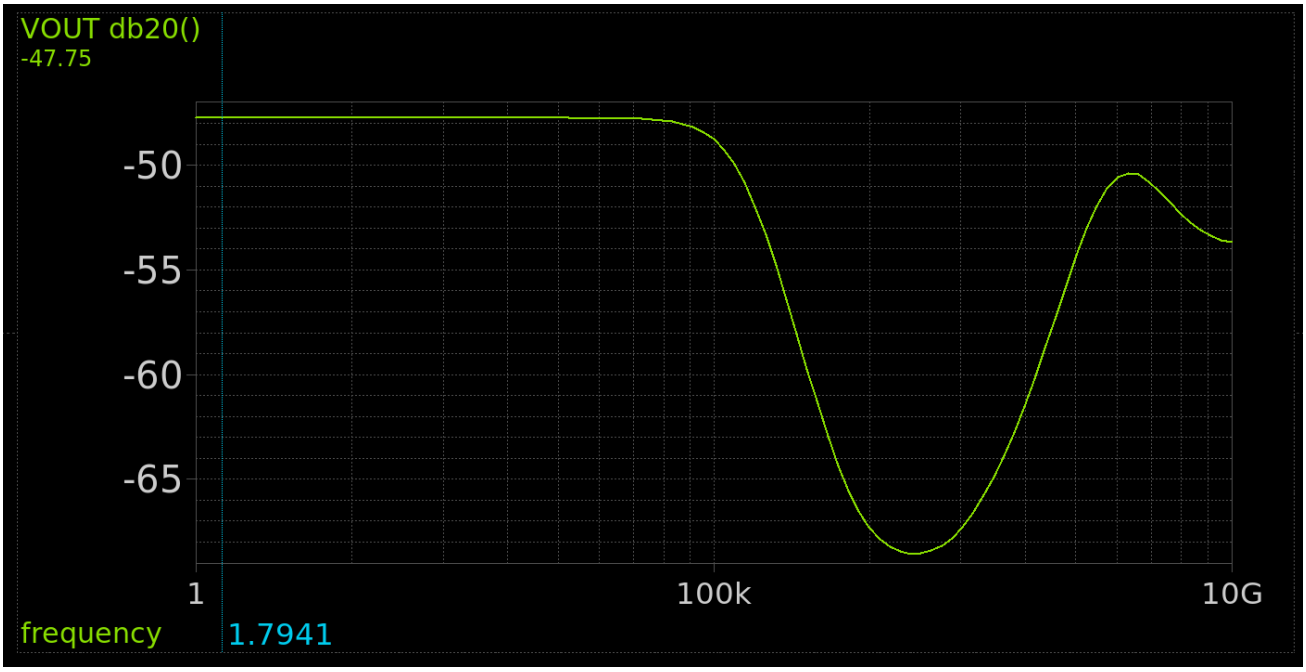


Figure 20 CM Gain (dB) vs Frequency

```
gain                =  4.095015e-03
gain_db = -4.77549e+01
```

Figure 21 CM Gain Values

Hand Analysis:

Using Values from OP Analysis:

$$|A_{vCM}| = \frac{1}{2gm_{3,4}R_{SS}} = \frac{1}{2gm_{3,4}ro_5} = 5.0578 \times 10^{-3} \rightarrow -45.92\ dB$$

	Simulation	Hand Analysis
Gain	4.095e-3	5.0578e-3
Gain (dB)	-47.75	-45.92

Hand analysis and simulation results agree with each other.

CMRR:

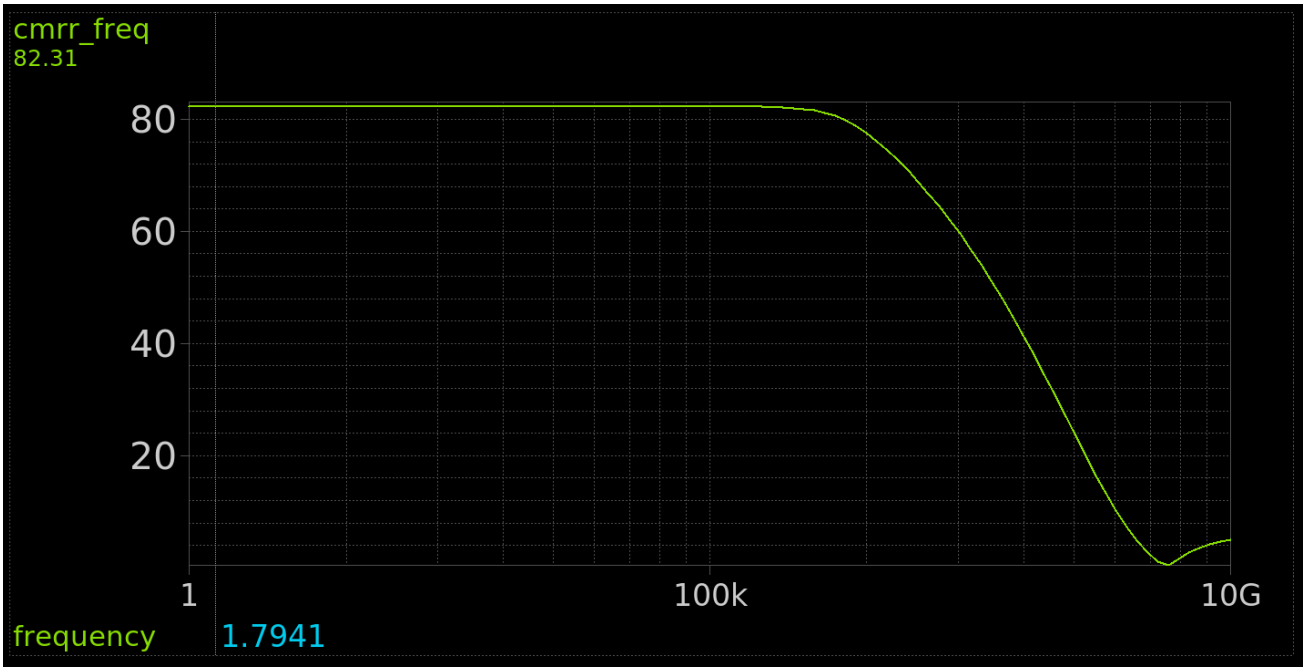


Figure 22 CMRR vs Freq from simulation

Hand Analysis:
Using Diff and CM gain values from last 2 parts:

$$CMRR = A_{vd}(dB) - A_{vCM}(dB) = \mathbf{80.6413\ dB}$$

	Simulation	Hand Analysis
Gain (dB)	82.31	80.6413

Hand analysis and simulation results agree with each other and satisfy the required spec.

Diff Large Signal:

Figure 23 VOUT vs Vid

What is the value of Vout at VID = 0? Why?

$\boldsymbol{Vout_{@Vid=0} = 0.75,}$ Same Value as Vout calculated During OP Analysis, This is the Quiescent point of the amplifier

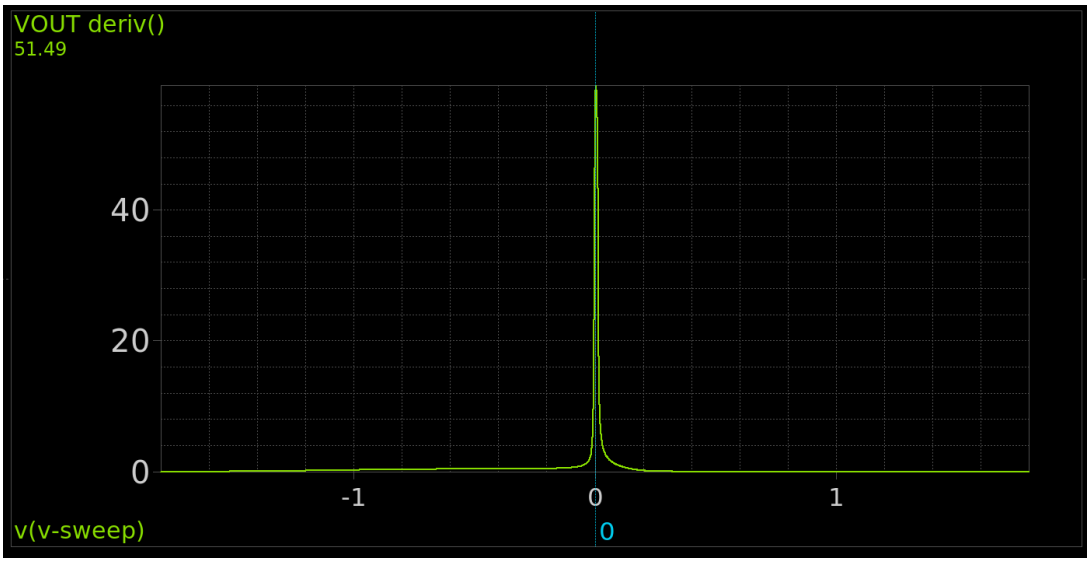


Figure 24 Derivates of Vout vs Vid

```
peak                    =   5.887698e+01 at=   4.000000e-03
```

Figure 25 Value at the Peak

The Value of the derivative of Vout vs Vid is the DC Gain, the value at the peak=**58.87** is observed to be slightly higher than Avd=**53.415** but still comparable to it

CM Large Signal:

```
min_vincm = 8.608995e-01
max_vincm = 1.516314e+00
cmir = 6.554145e-01
```

Figure 26 CMIR From Simulation

$$VCM_{LOW} = 0.8609V,\ VCM_{HIGH} = 1.516V$$

The result meets the required spec

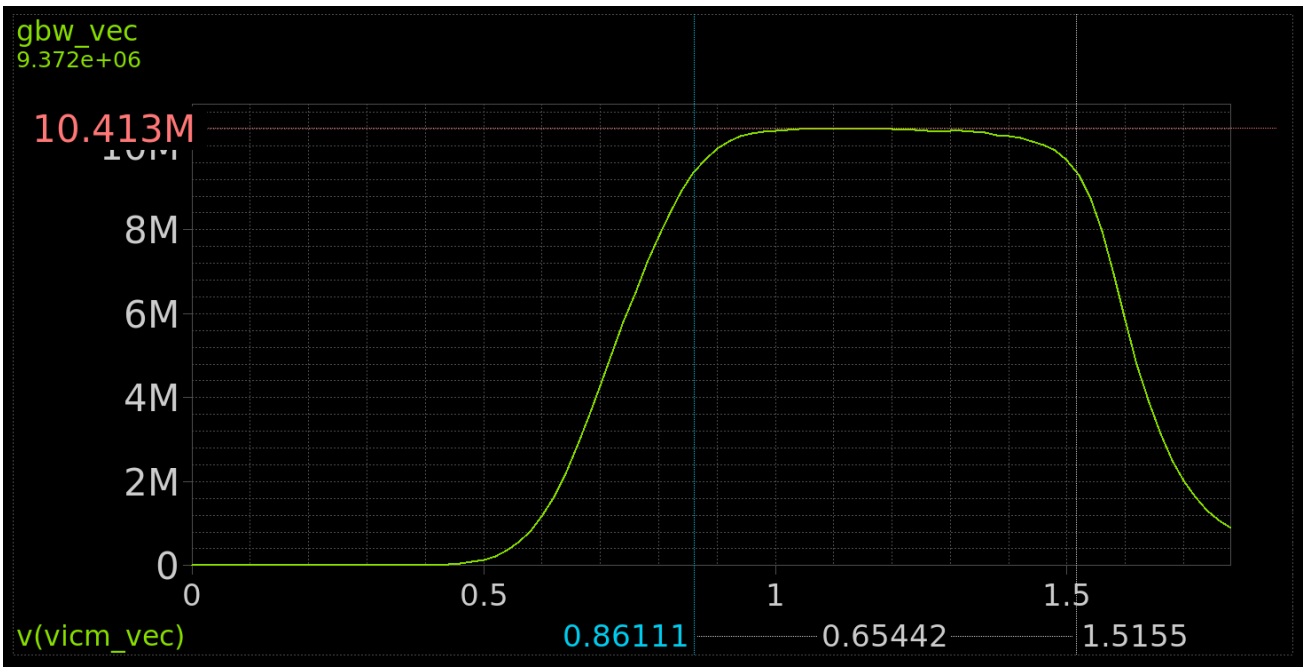


Figure 27 GBW vs VCIM wiht VCIM Annotated

The result for GBW meets the required specifications inside the input range!

If you are using NMOS input pair, body effect may cause CMIR to extend till VDD (why?).
As $VICM_{MAX} = VDD + V_{TH1,2} - V_{GS3,4}$ Increasing the VSB of M1,2 Transistors can increase the Maximum to be higher than VDD also increasing the width of M3,4 decreases their VGS thus increasing the VICM-Max as well

Part 4: Closed Loop OTA Simulation:

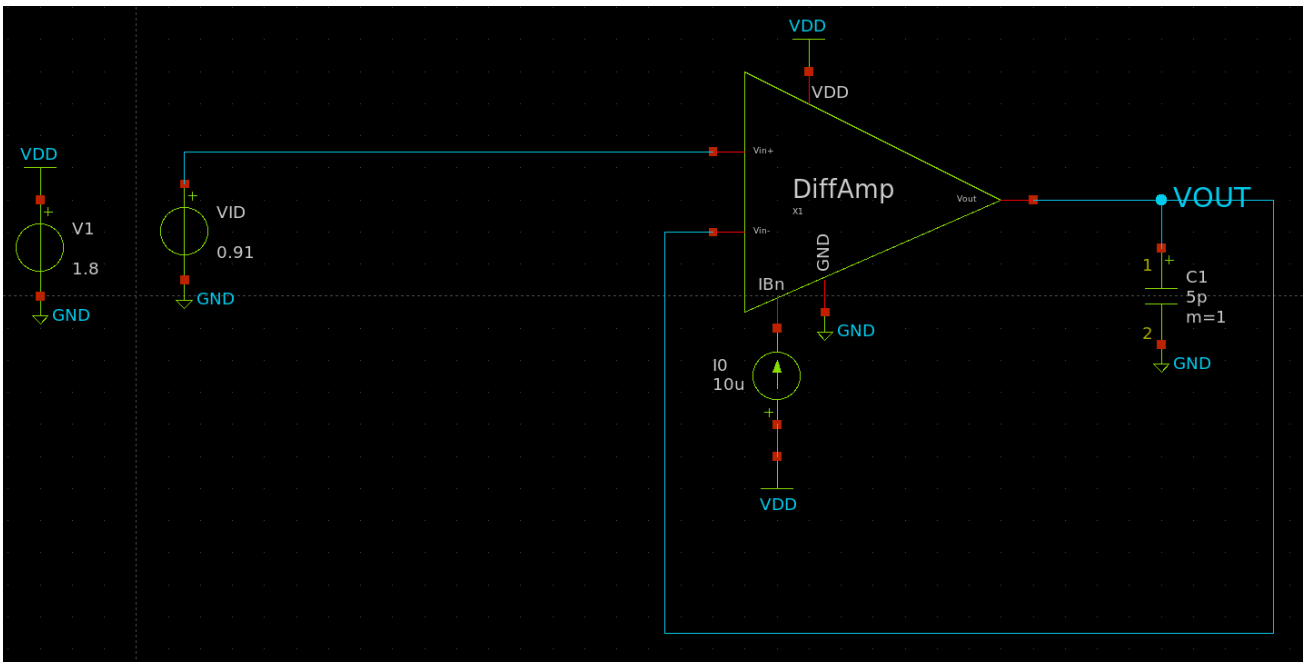


Figure 28 Closed Loop Testbench

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm6.m0	m.x1.xm5.m0	m.x1.xm3.m0
model	nmos_3p3.10	nmos_3p3.14	pmos_3p3.8
id	1e-05	3.91602e-05	1.94154e-05
gm	9.78173e-05	0.000349102	0.000116439
gmbs	3.84057e-05	0.000137761	4.41489e-05
gds	1.92449e-07	6.73433e-05	2.28334e-06
vgs	0.822205	0.822205	1.04218
vth	0.667182	0.668168	0.756427
vds	0.822204	0.144526	0.892294
vdsat	0.161448	0.161665	0.286699

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm4.m0	m.x1.xm2.m0	m.x1.xm1.m0
model	pmos_3p3.8	nmos_3p3.12	nmos_3p3.12
id	1.97448e-05	1.94154e-05	1.97448e-05
gm	0.000118099	0.00032091	0.00032495
gmbs	4.47105e-05	9.98597e-05	0.000101132
gds	2.12122e-06	2.67513e-06	2.89281e-06
vgs	1.04218	0.763162	0.76547
vth	0.755461	0.752227	0.752587
vds	1.04217	0.763161	0.613285
vdsat	0.28748	0.0935059	0.0944818

Figure 29 OP Point in Feedback Configuration

· **Is the current (and gm) in the input pair exactly equal? Why?**
No, there is a slight mismatch between them. As the output node voltage deviates from its CM value to match the input value resulting in a non zero differential input causing a mismatch

· **Calculate the mismatch in ID and gm.**

$$ID_{mis} = \Delta I_D = 0.325\mu A$$
$$gm_{mis} = \Delta gm = 4.04\mu s$$

Loop Gain:

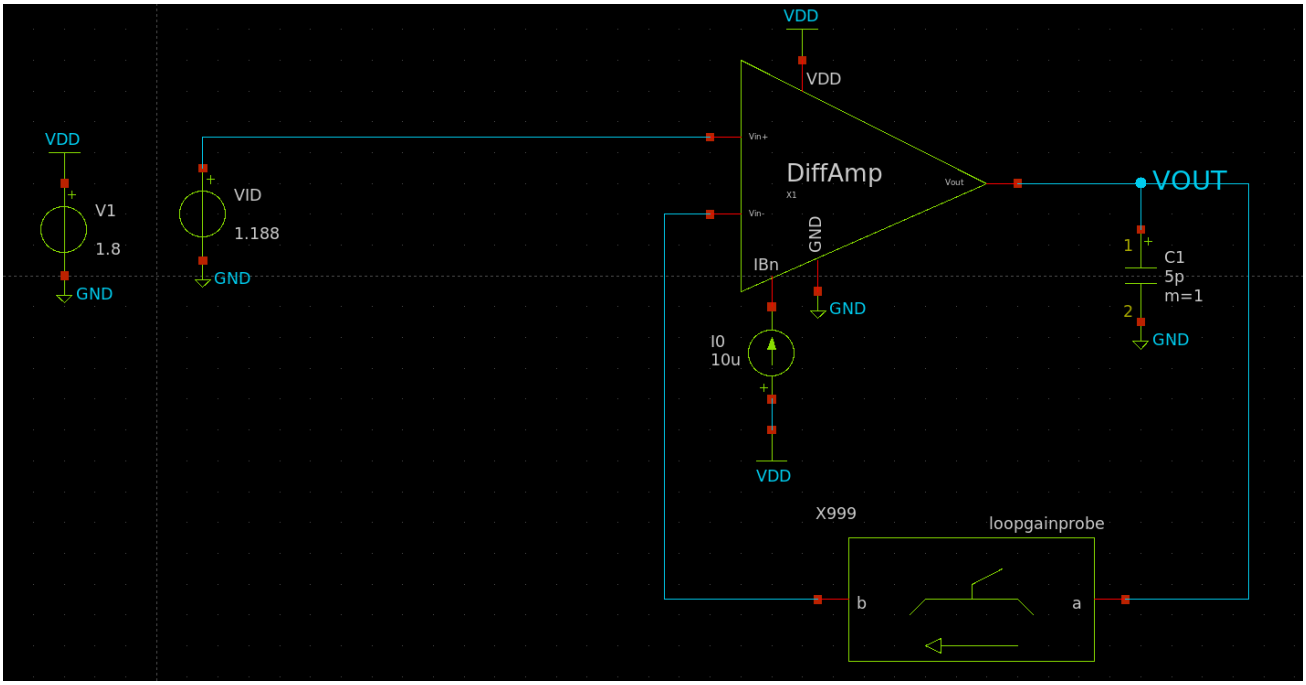


Figure 30 STB Simulation Testbench

```
gain_crossover_freq =  9.799207e+06
phaseatzerogain     =  9.028357e+01
pm = 8.971643e+01
```

Figure 31 STB Simulation Results

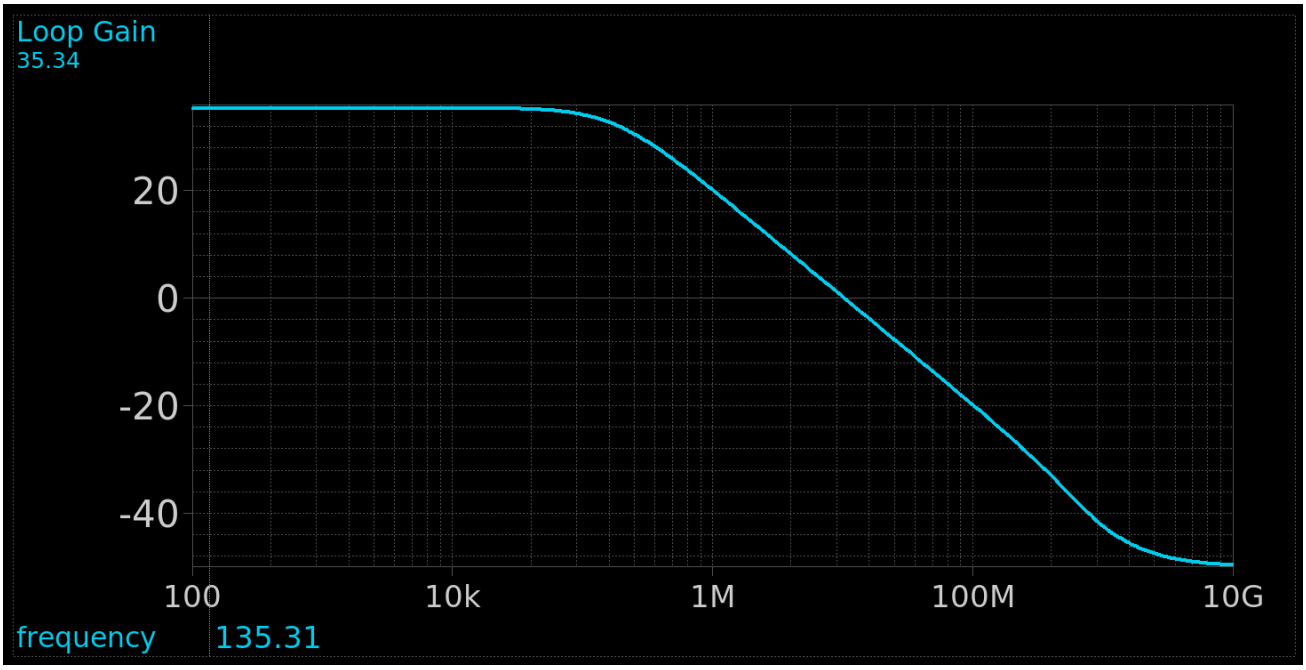


Figure 32 Loop Gain (dB) vs Frequency

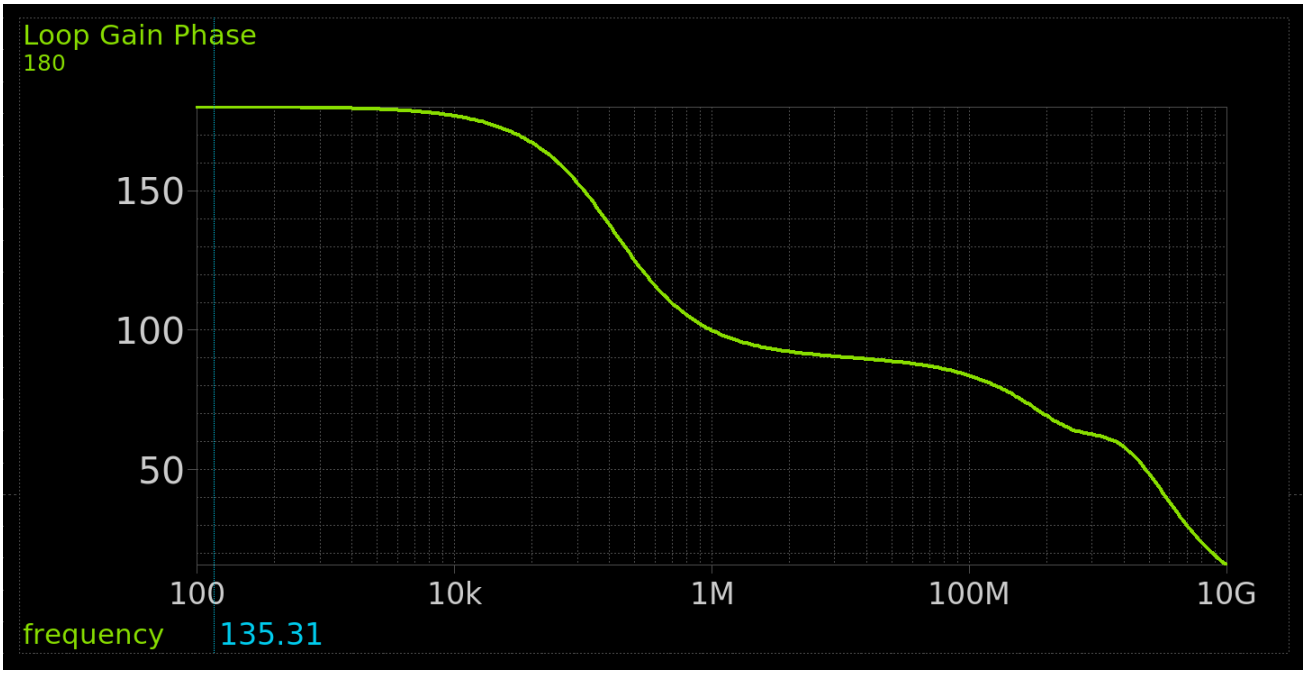


Figure 33 Loop Gain Phase vs Frequency

$$Loop\ Gain = \mathbf{35.34}\boldsymbol{dB}$$

Compare DC gain and GBW with those obtained from open-loop simulation

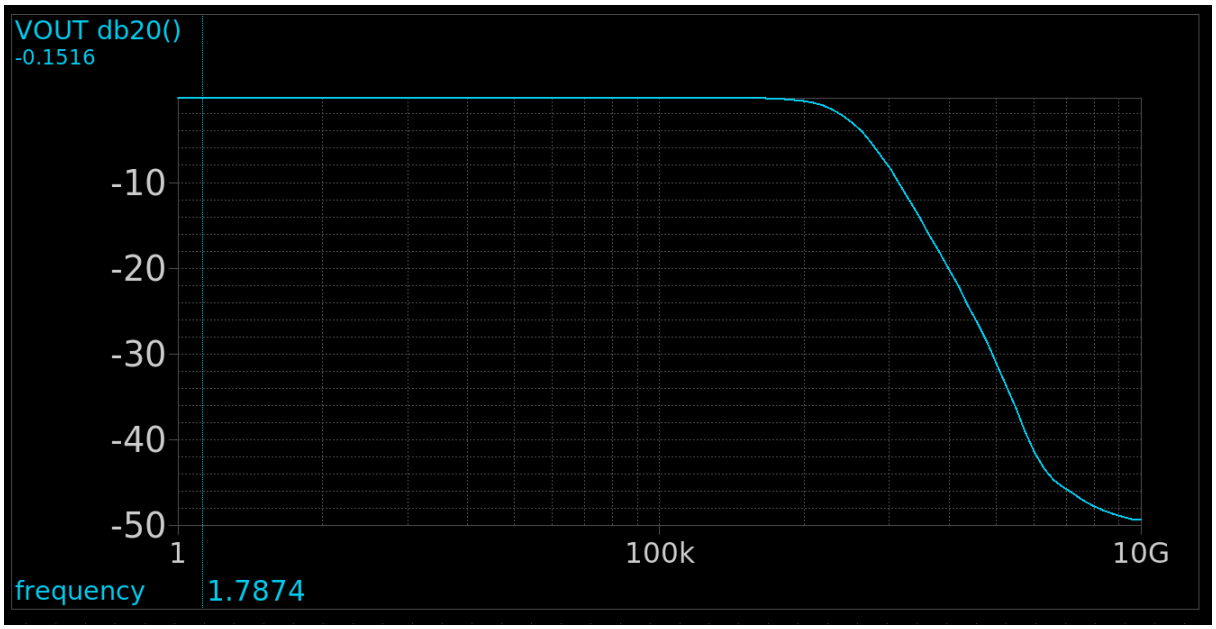


Figure 34 Closed Loop Gain in dB vs Frequency

The Amplifier work as a buffer in this configuration thus the gain is approximately equal to 0dB (Unity Gain).

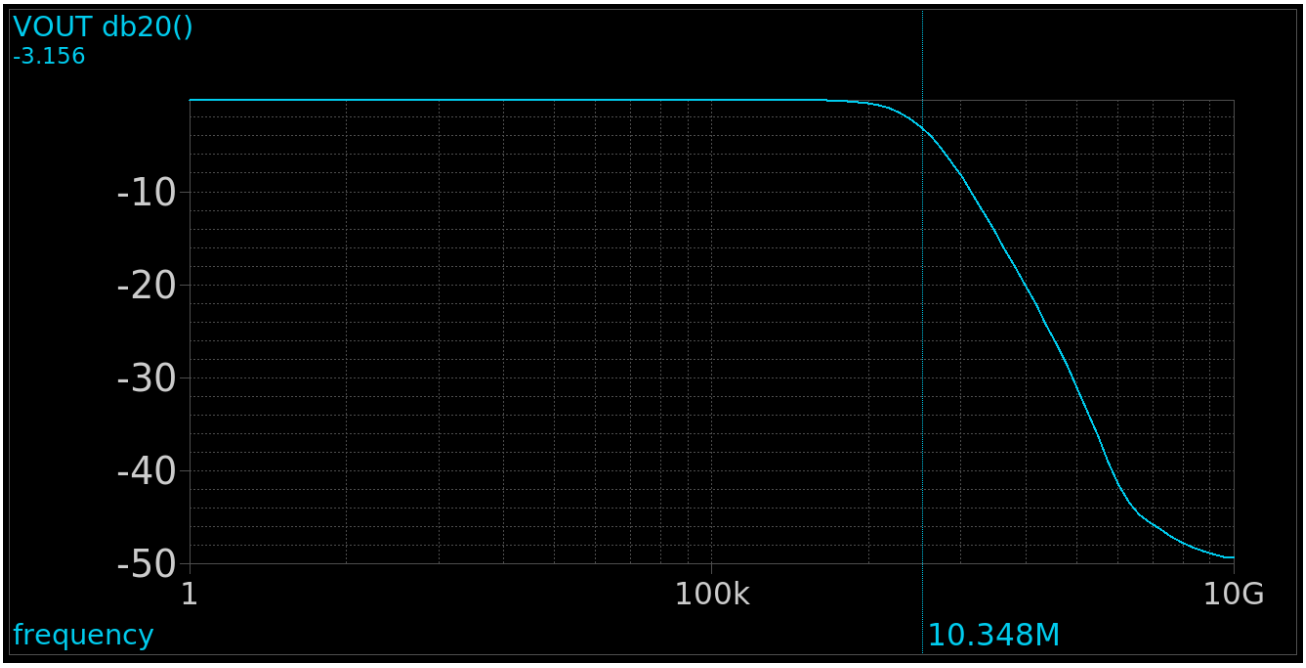


Figure 35 Closed Loop Bandwidth

$$GBW_{CL} \approx BW_{CL} \approx \mathbf{10.348MHz}$$

Compared to open loop simulation the closed loop gain here is unity but we can see the GBW is approximately the same, this is because the BW from the open loop simulation was increased by a factor of $(1 + Loop\ Gain)$ which is approximately equal to A_{OL} multiplied by the unity gain of this configuration gives us equivalent GBW for both Open Loop and Closed Loop.

Hand Analysis:

$$\beta = 1 \quad , \quad A_{OL} = 53.395\ (From\ Open\ Loop\ Simulation)$$
$$Loop\ Gain = \beta A_{OL} = \mathbf{53.395} \rightarrow 34.55\ dB$$
$$A_{CL} = \frac{A_{OL}}{1 + \beta A_{OL}} = \mathbf{0.9816} \rightarrow \mathbf{-0.1611\ dB}$$

	Simulation	Hand Analysis
Beta	1	1
Loop Gain	53.395	58.479
Loop Gain (dB)	34.55	35.34
Closed Loop Gain	0.9827	0.9816
Closed Loop Gain (dB)	-0.1516	-0.1611

The Open Loop gain in this configuration is slightly higher than the open loop gain from the simulation in the previous part this is due to the slight mismatch changing the q-point and increasing the gain a little bit close to the Maximum. Other than that, Analytic Results agree with Hand Analysis for the most part.

Conclusion:

Comparing Achieved Spec with Required:

Specification	Required	Achieved
Supply voltage	1.8V	1.8V
Load	5pF	5pF
Open loop DC voltage gain	>= 34dB	34.55
CMRR @ DC	>= 74dB	82.31
Phase margin	>= 70°	89.7°
CM input range – low	<= 1V	0.86V
CM input range – high	>= 1.5V	1.516
GBW	>= 10MHz	10.413MHz

Using the gm/Id Methodology and a little bit of fine tuning via iterations I was able to achieve the required specification with the minimum area.