Analog IC Design

Lecture 14
OTA Design Example

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Analog Design Trade-offs

- There are always tradeoffs between gain, speed, and energy efficiency.
- The design knobs that you use to control the tradeoffs are gm/ID and L.
- Choice of gm/ID
  - Large gm/ID: high efficiency (low power), large swing (low V*), high gain (low V*)
  - Small gm/ID: high speed, small area
- Choice of L
  - Long L: high gain, good matching, low flicker noise (more later)
  - Short L: high speed, small area
- Finding the best compromise for design tradeoffs given required specs is your job as a designer.

Outline

- ❑ OTA required specifications
- ❑ Topology selection
- ❑ Tradeoffs Matrix
- ❑ Design of input pair
- ❑ Design of current mirror load
- ❑ Design of tail current source
- ❑ Sizing and simulation results

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OTA Design Example

- Design a diff input SE output OTA that meets the following specs.

Technology	180 nm CMOS
Supply voltage	1.8 V
Load	5 pF
Open loop DC voltage gain	>= 32 dB
Phase margin	>= 70^{o}
Reference Current	10 uA
OTA current consumption	<= 20 uA
CM input range – low	<= 0.2 V
CM input range – high	>= 1.1 V
GBW	5 MHz
CMRR @DC	70 dB

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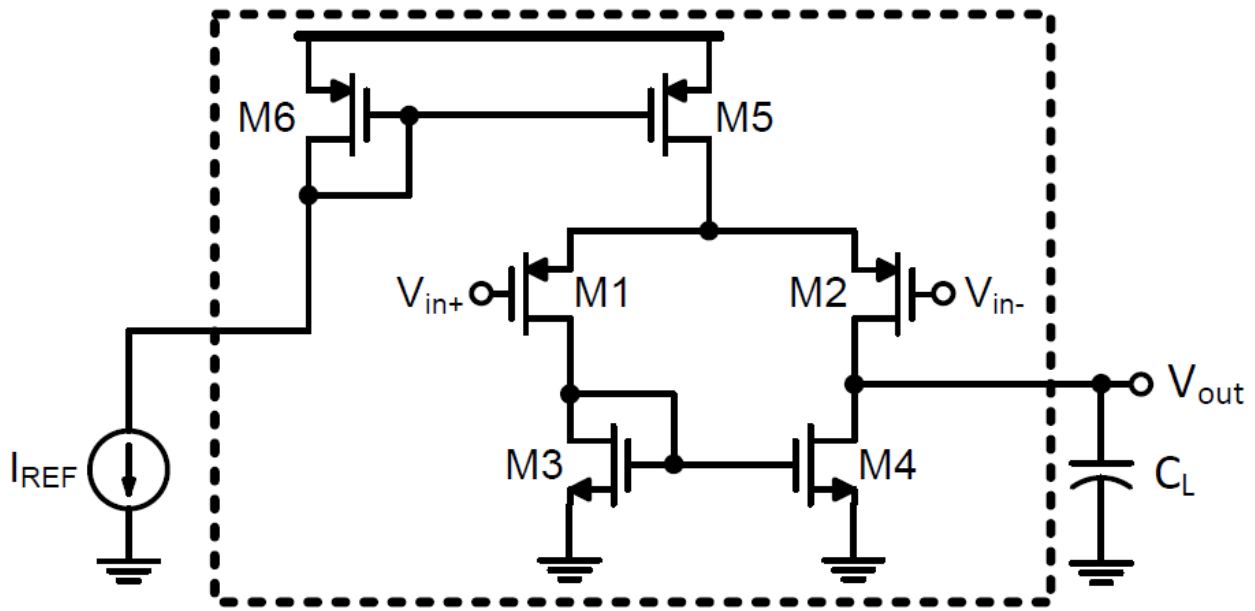
Topology Selection

- The required gain is not high (only 32 dB = 40) so it can be achieved by a simple single stage OTA
  - If the gain is high, we must use cascode or two stage OTA
- Since the required CMIR is close to the ground rail, we need to use a PMOS input stage
- PMOS input stage has other advantages as well
  - PMOS input transistors can be placed in a separate well so they don't suffer from body effect
  - PMOS has lower flicker noise

Topology Selection

- Single stage OTA has a single dominant pole, so we don't need to worry about phase margin
  - For two-stage you must use compensation network
- Use simple current mirror for biasing
  - The reference current is 10 uA
  - Doubled by the mirror such that 20 uA goes to the diff pair



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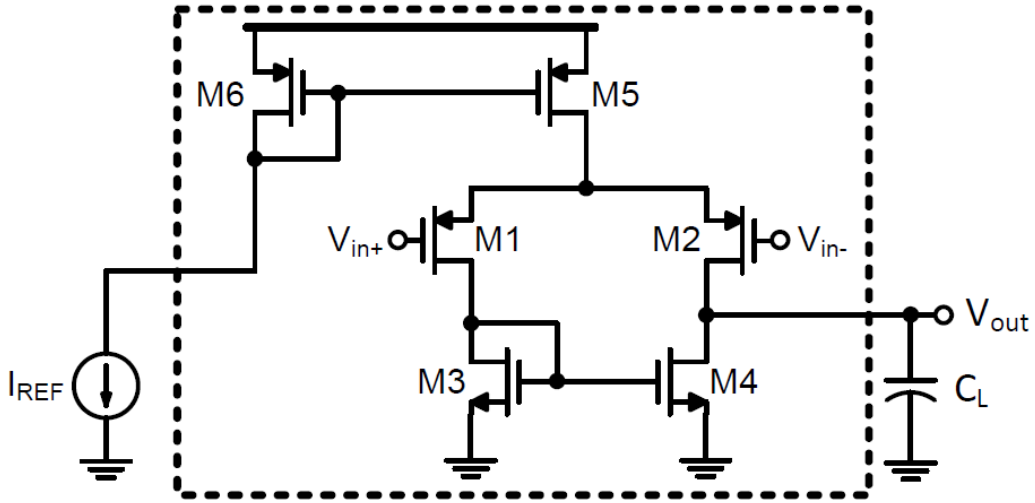
Trade-offs Matrix

Spec	I_{SS}	L_{12}	$\left(\frac{g_m}{I_D}\right)_{12}$	L_{34}	$\left(\frac{g_m}{I_D}\right)_{34}$	L_5	$\left(\frac{g_m}{I_D}\right)_5$
DC gain ↑							
CMIR – low ↓							
CMIR – high ↑							
GBW ↑							
CMRR @DC ↑							



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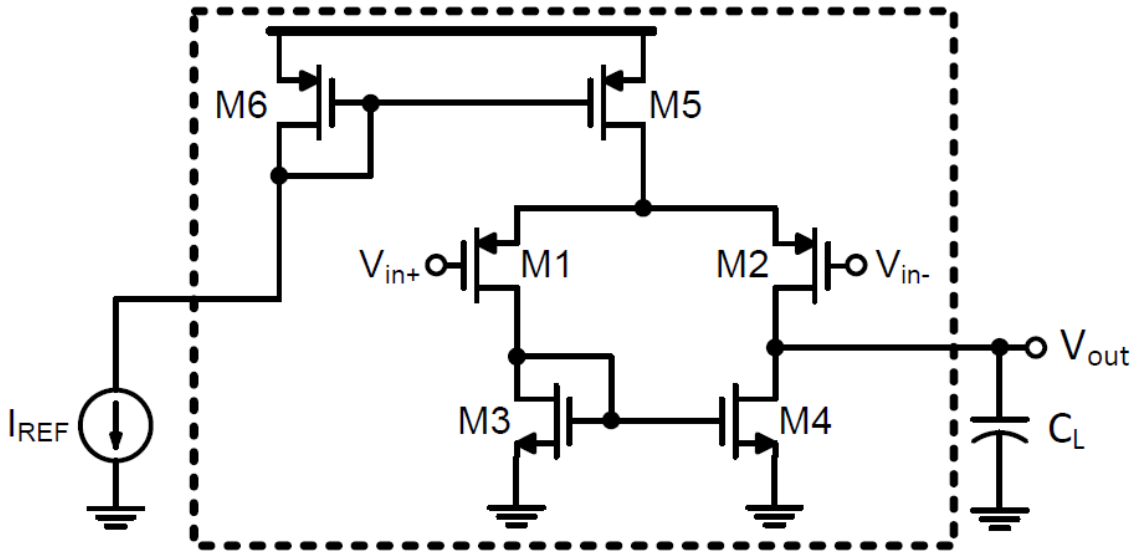
PMOS Input Stage (1/3)

- $GBW = \frac{g_m}{2\pi C_L}$
- $g_m = 2\pi \times 5\,p \times 5\,M \approx 160\,\mu S$
- $I_D = \frac{20\,\mu}{2} = 10\,\mu A$
- $\frac{g_m}{I_D} = 16\,S/A$



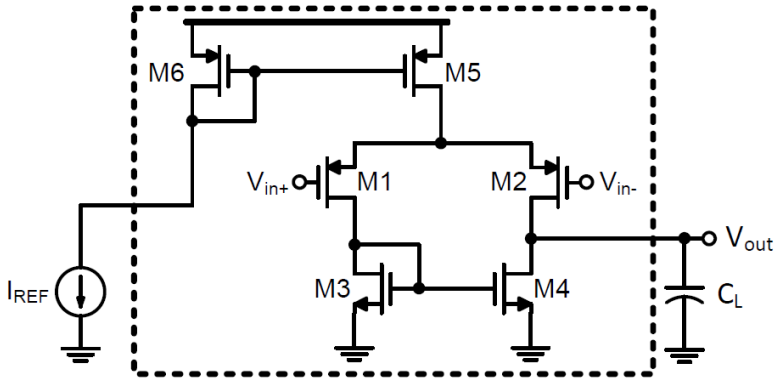
PMOS Input Stage (2/3)

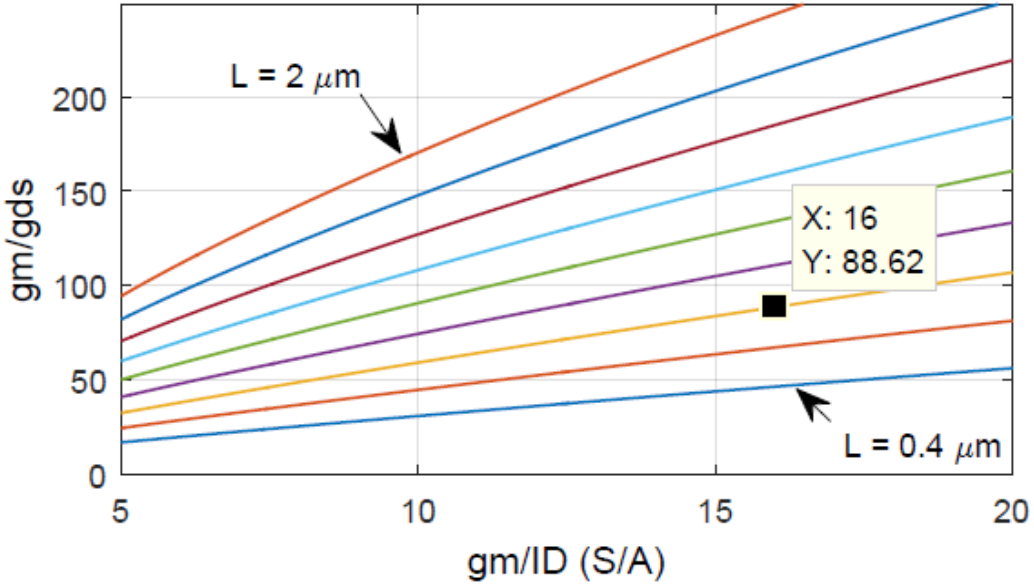
- Next, we need to find the channel length to get the required gain
- For simplicity, assume PMOS and NMOS have same g_{ds}

$$A_v = \frac{g_m r_o}{2} > 40 \quad \rightarrow \quad Let: \; g_{ds2} = g_{ds4} < 2\,\mu S$$

$$A_v = \frac{g_m r_o}{2} \rightarrow \frac{g_m}{g_{ds}} > 80$$

- From the design chart, we find that required length is **L = 0.8 um**

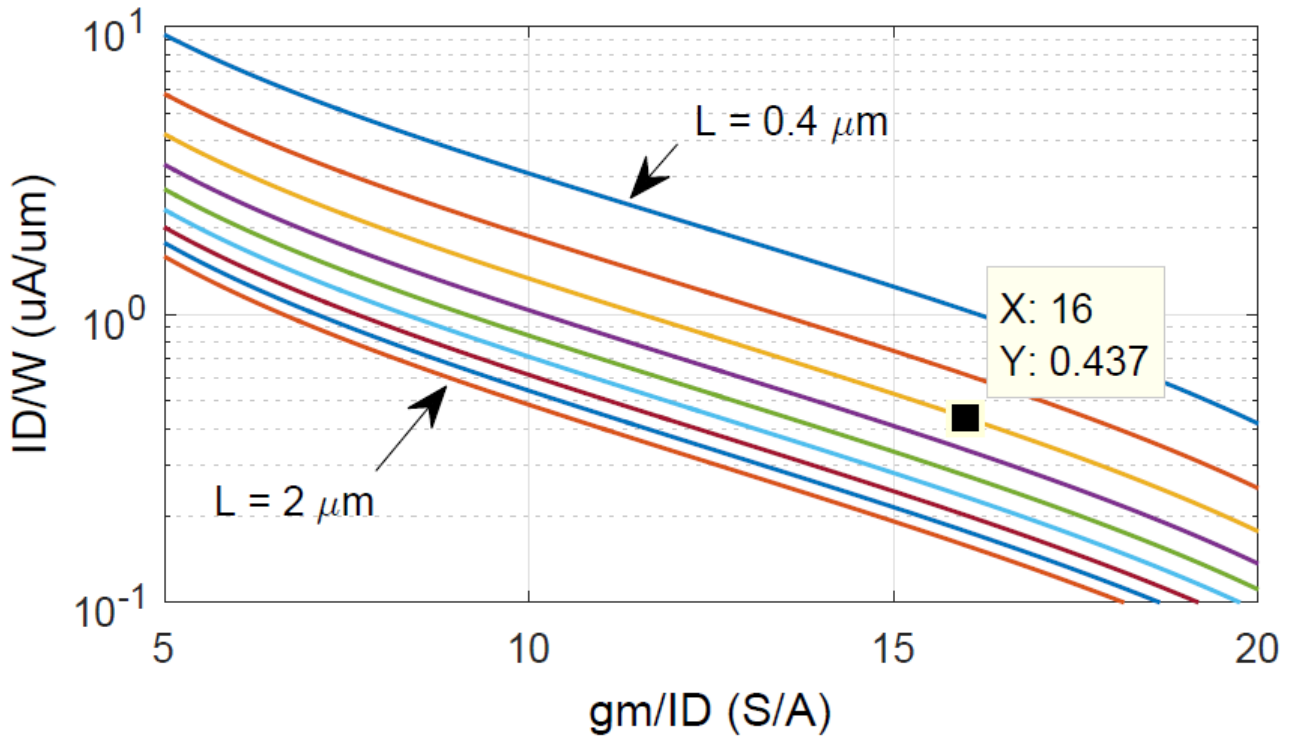




PMOS Input Stage (3/3)

- Going to the ID/W chart

$$\frac{I_d}{W} = 0.44 \rightarrow W = \frac{10}{0.44} \approx 24\ \mu m$$



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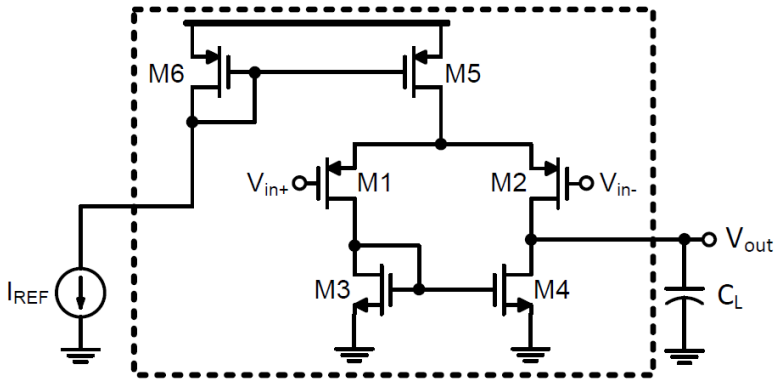
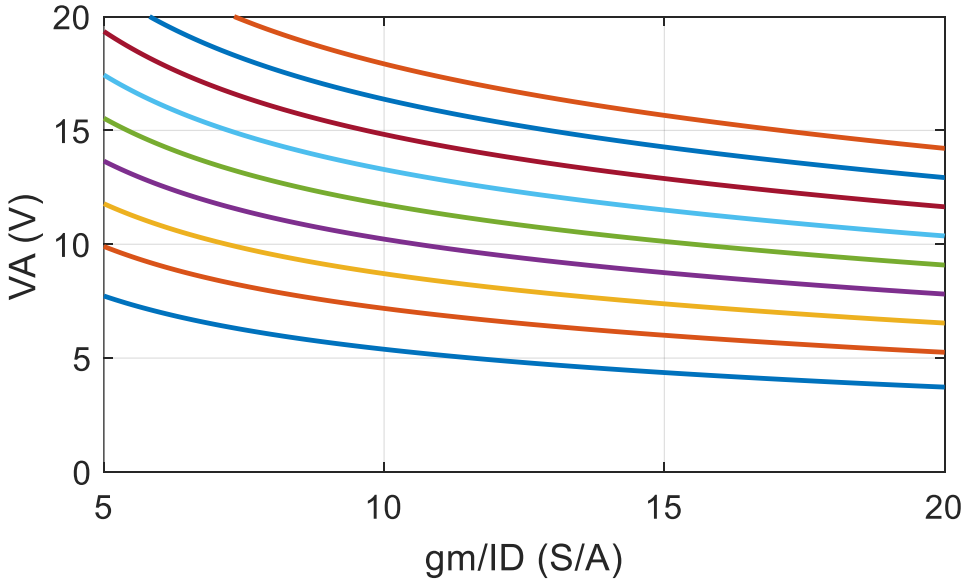
NMOS Current Mirror Load (1/6)

- From the DC gain spec select the length of the current mirror load

$$g_{ds4} = \frac{I_D}{V_A} < 2\ \mu S \ \rightarrow V_A > 5\ V$$

- $V_A = I_D r_o$ slightly decreases with gm/ID (weak dependence)
- Assume an arbitrary but large gm/ID, e.g., gm/ID = 15





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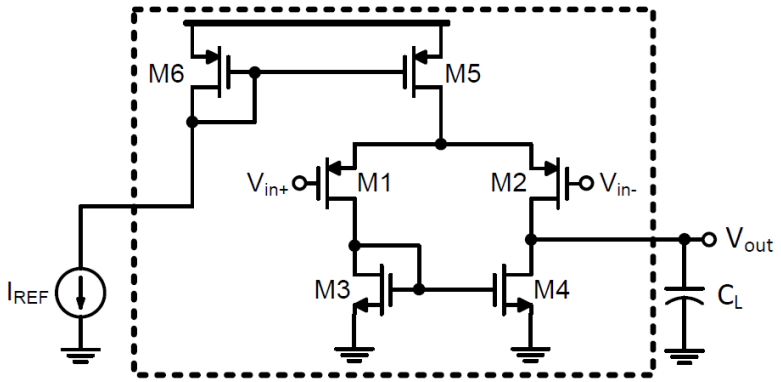
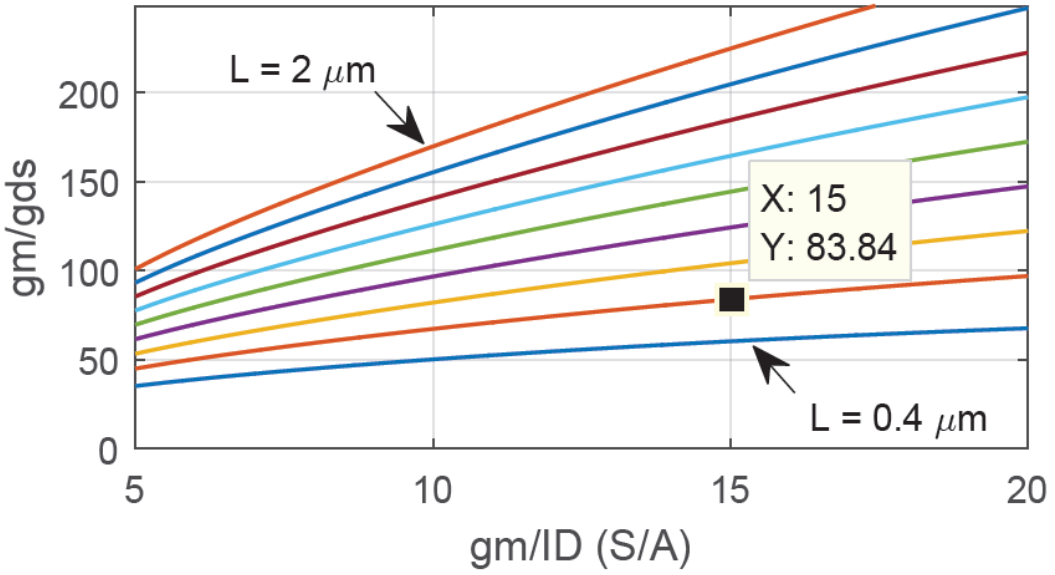
- $V_A = I_D r_o$ slightly decreases with gm/ID (weak dependence)
- Assume an arbitrary but large gm/ID, e.g., gm/ID = 15

$$\frac{g_m}{I_D} = 15 \ \rightarrow g_m = 150\ \mu S \ \rightarrow \frac{g_m}{g_{ds}} = 75 \ \rightarrow L = 0.6\ \mu m$$





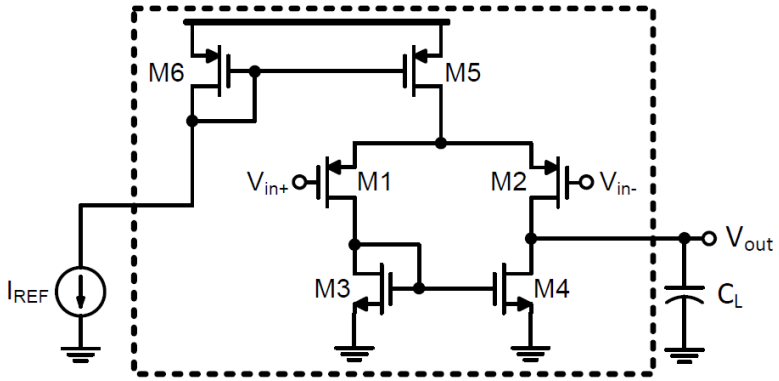
NMOS Current Mirror Load (2/6)

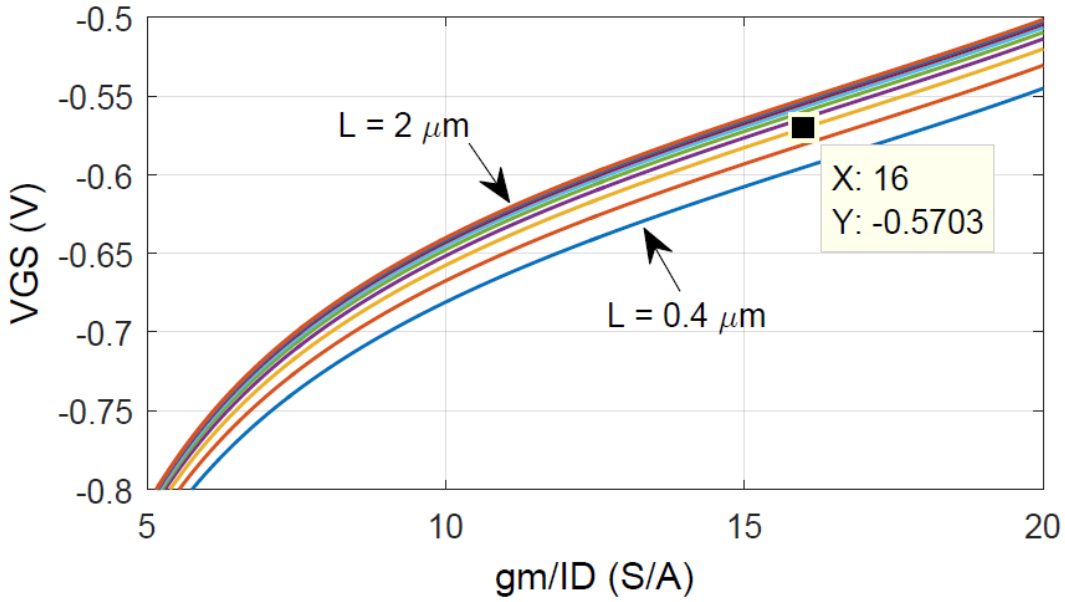
- The design of the current mirror load is determined by CMIR, noise, and output swing specs

$$CMIR_{LOW} = -|V_{GS1}| + |V_{dsat1}| + V_{GS3} < 0.2\ V$$

- Get V_{GS1} and V_{dsat1} (or use $V_1^* = 0.125\ V$)

$$0.2 = -0.57 + |V_{dsat1}| + V_{GS3,max}$$





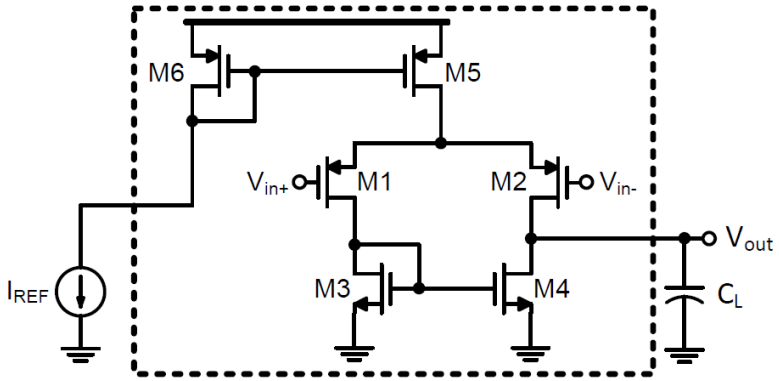
NMOS Current Mirror Load (3/6)

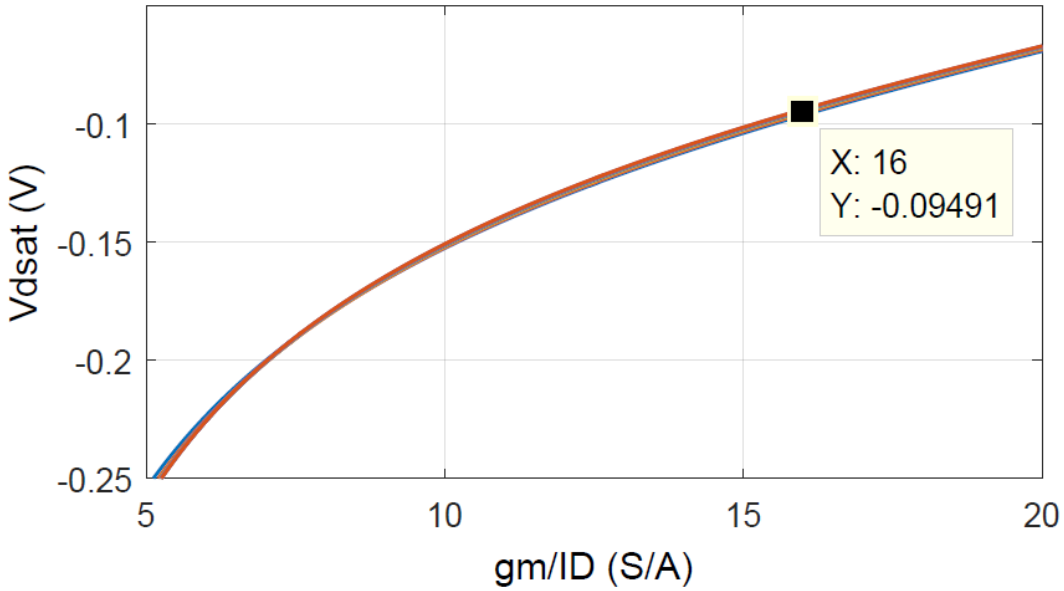
- The design of the current mirror load is determined by CMIR, noise, and output swing specs

$$CMIR_{LOW} = -|V_{GS1}| + |V_{dsat1}| + V_{GS3} < 0.2\ V$$

- Get V_{GS1} and V_{dsat1} (or use $V_1^* = 0.125\ V$)

$$0.2 = -0.57 + 0.1 + V_{GS3,max}$$



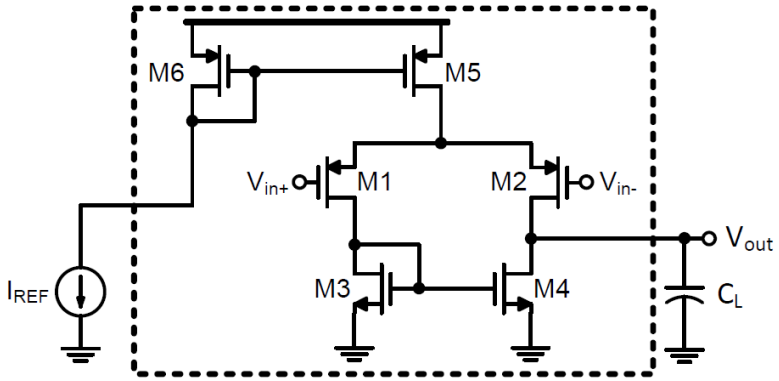


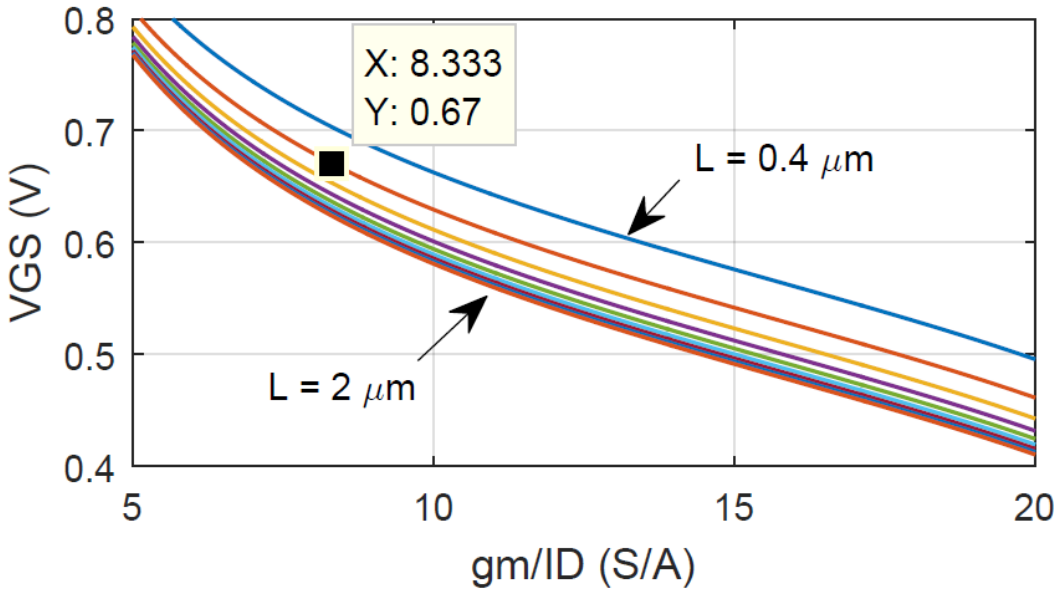
NMOS Current Mirror Load (4/6)

- The design of the current mirror load is determined by CMIR, noise, and output swing specs

$$V_{GS3,max} = 0.67\ V$$

$$\left(\frac{g_m}{I_D}\right)_{min} = 8.33$$





NMOS Current Mirror Load (5/6)

- The design of the current mirror load is determined by CMIR, noise, and output swing specs

$$V_{GS3,max} = 0.67\ V$$

$$\left(\frac{g_m}{I_D}\right)_{min} = 8.33$$

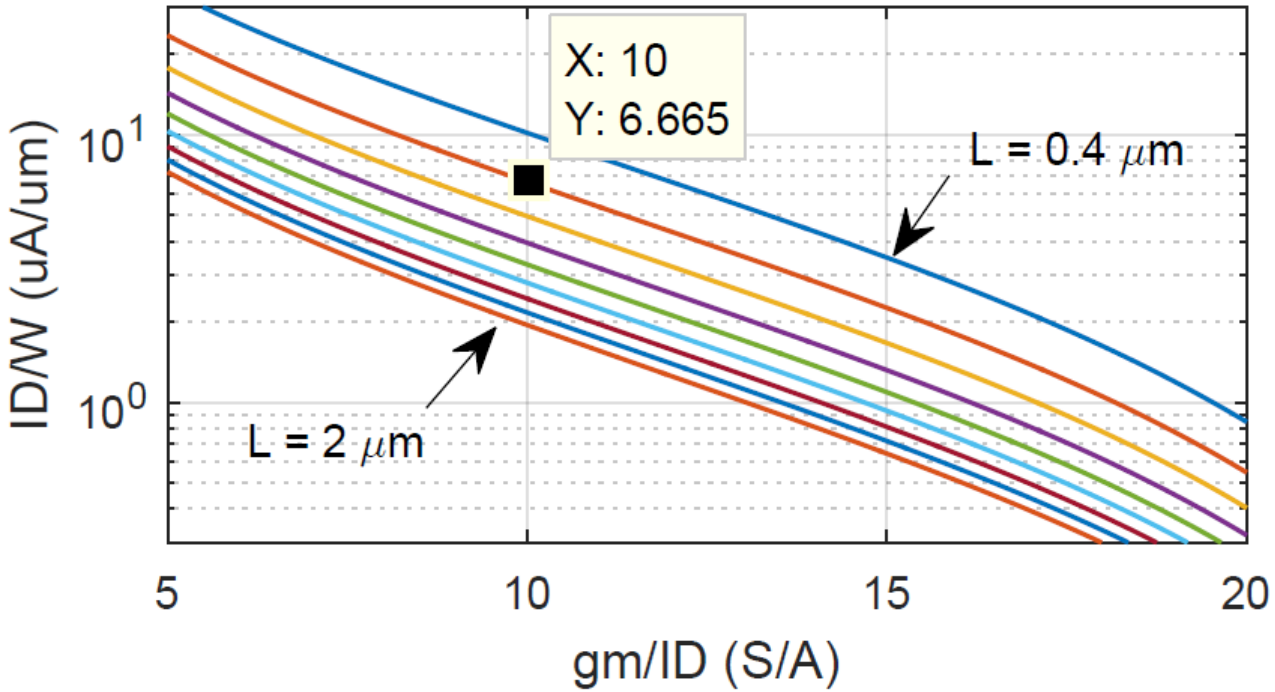
- Given no strict noise specification (to be discussed later), and to avoid placing M1,2 at edge of saturation, select a bit larger gm/ID

$$\frac{g_m}{I_D} = 10$$

NMOS Current Mirror Load (6/6)

- Assume minimum finger width is $2\ \mu m$
- Going to the ID/W chart

$$\frac{I_d}{W} = 6.7 \rightarrow W = 2\ \mu m$$



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Tail Current Source (1/4)

$$A_{vCM} = \frac{V_{out}}{V_{iCM}} \approx -\frac{1}{2g_{m3,4}R_{SS}}$$

$$CMRR = \frac{A_v}{A_{vCM}} \approx g_{m1,2}(r_{o2}//r_{o4}) \cdot 2g_{m3,4}R_{SS}$$

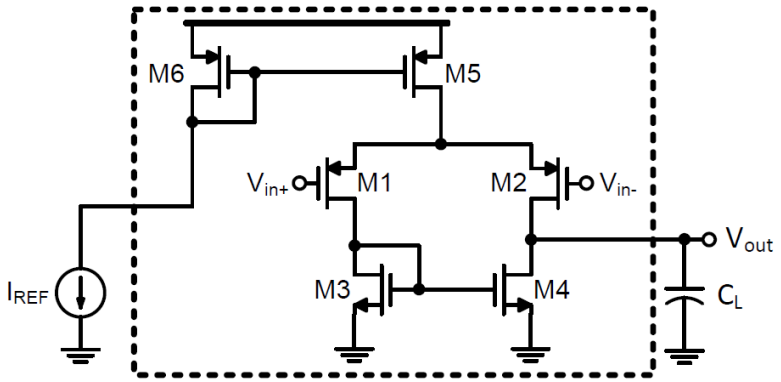
- Long channel length means large output resistance: good CMRR @DC and good mirroring (less CLM)
  - But large area → large parasitic cap: CMRR degrade at high frequencies
- Large gm/ID (small V*): wide CMIR and wide swing
  - But large area → large parasitic cap: …
  - And more sensitivity to systematic V_{GS} errors (e.g., IR drops)

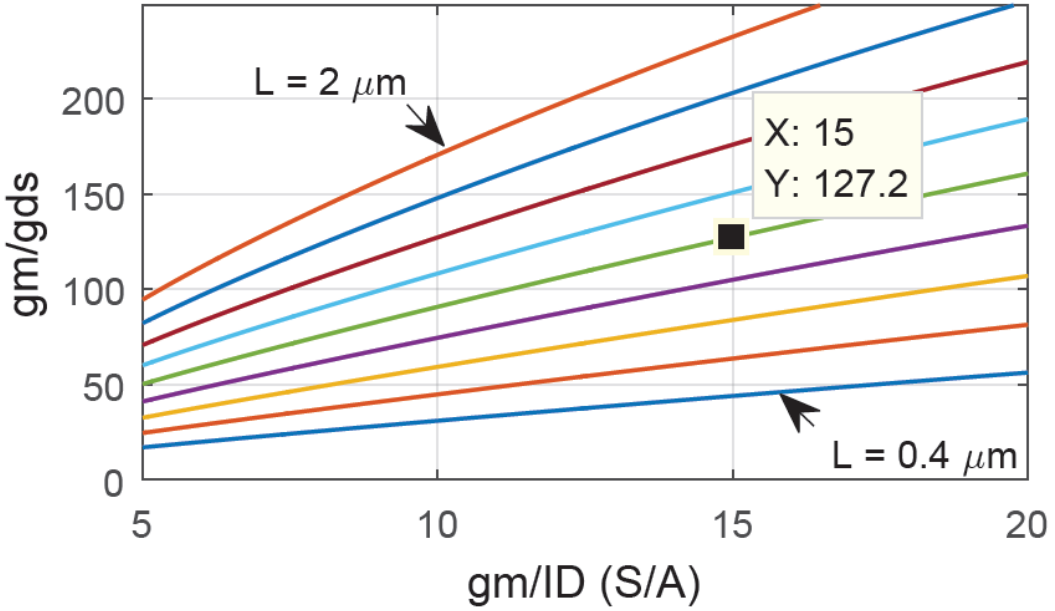
Tail Current Source (2/4)

$$|A_{vCM}| = \left|\frac{V_{out}}{V_{iCM}}\right| \approx \left|-\frac{1}{2g_{m3,4}R_{SS}}\right| = -38\,dB \;\rightarrow\; g_{ds5} < 2.6\,\mu S$$

- $V_A = I_D r_o$ slightly decreases with gm/ID (weak dependence)
- Assume an arbitrary but large gm/ID, e.g., gm/ID = 15

$$\frac{g_m}{I_D} = 15 \rightarrow g_m = 300\,\mu S \rightarrow \frac{g_m}{g_{ds}} > 115 \rightarrow L = 1.2\,\mu m$$



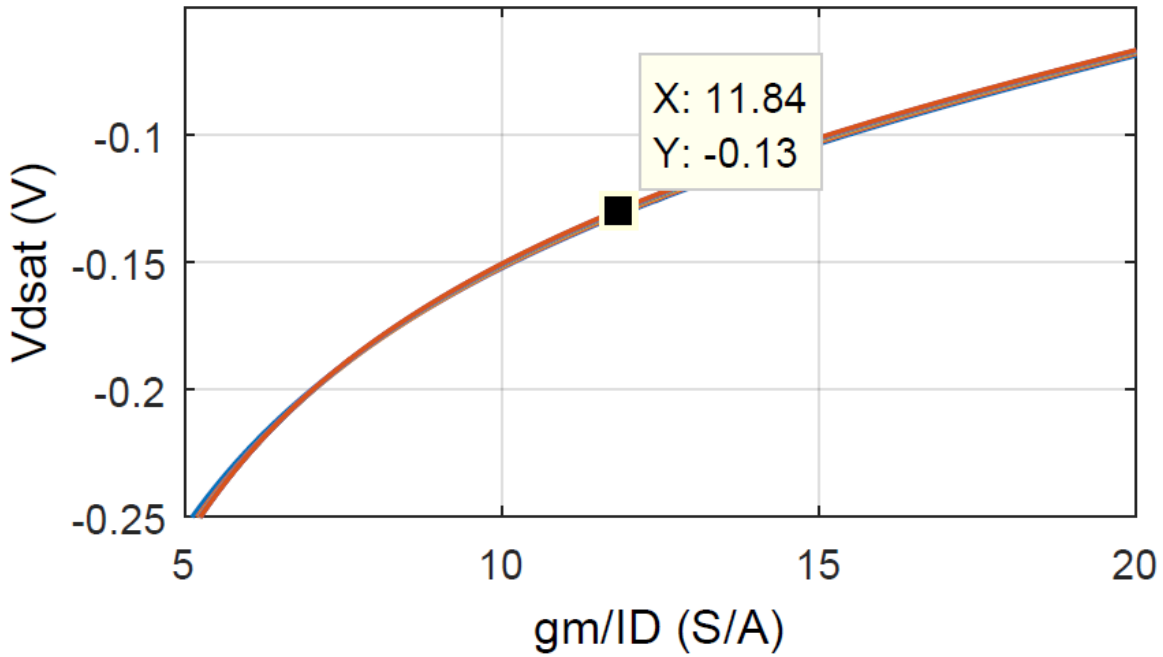


Tail Current Source (3/4)

- The design is completed by CMIR spec (use V_{dsat5} or V_5^*)

$$CMIR_{HIGH} = V_{DD} - |V_{GS1}| - |V_{dsat5}| > 1.1\ V$$
$$|V_{dsat5}| < 130\ mV$$

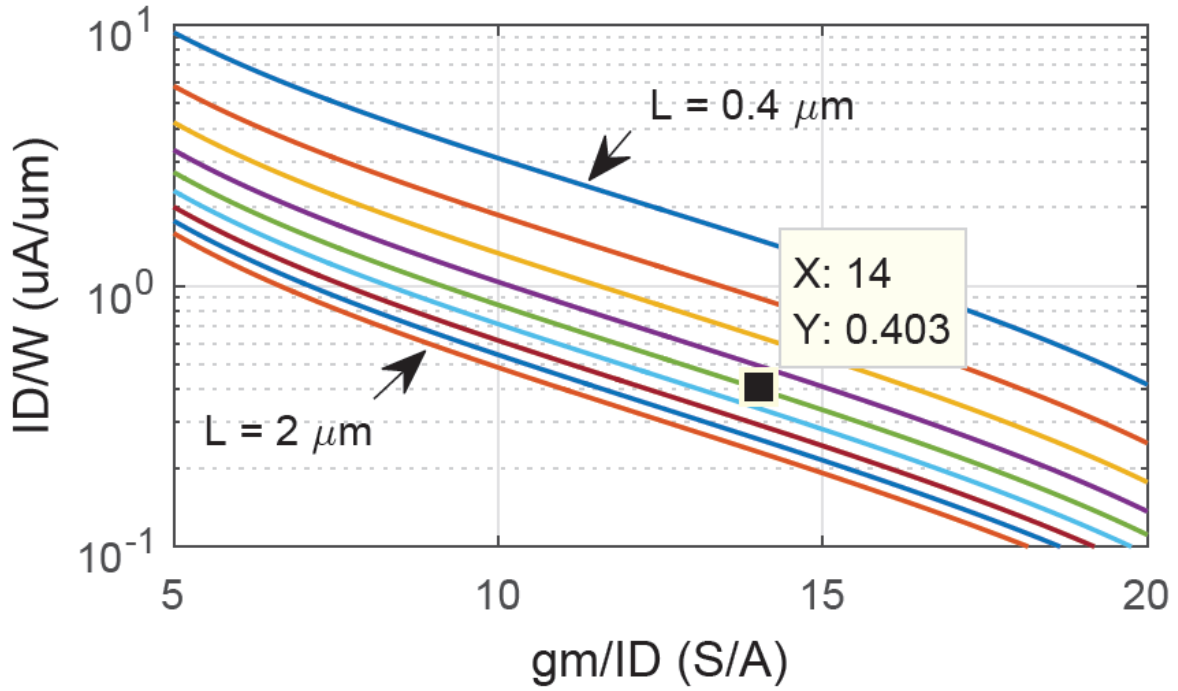
$$\frac{g_m}{I_D} > 11.8 \quad \rightarrow \quad \text{keep some margin and use} \quad \frac{g_m}{I_D} = 14$$



Tail Current Source (4/4)

- Note that the tail current source has double the current
- Going to the ID/W chart

$$\frac{I_d}{W} = 0.4 \rightarrow W \approx 52\ \mu m$$



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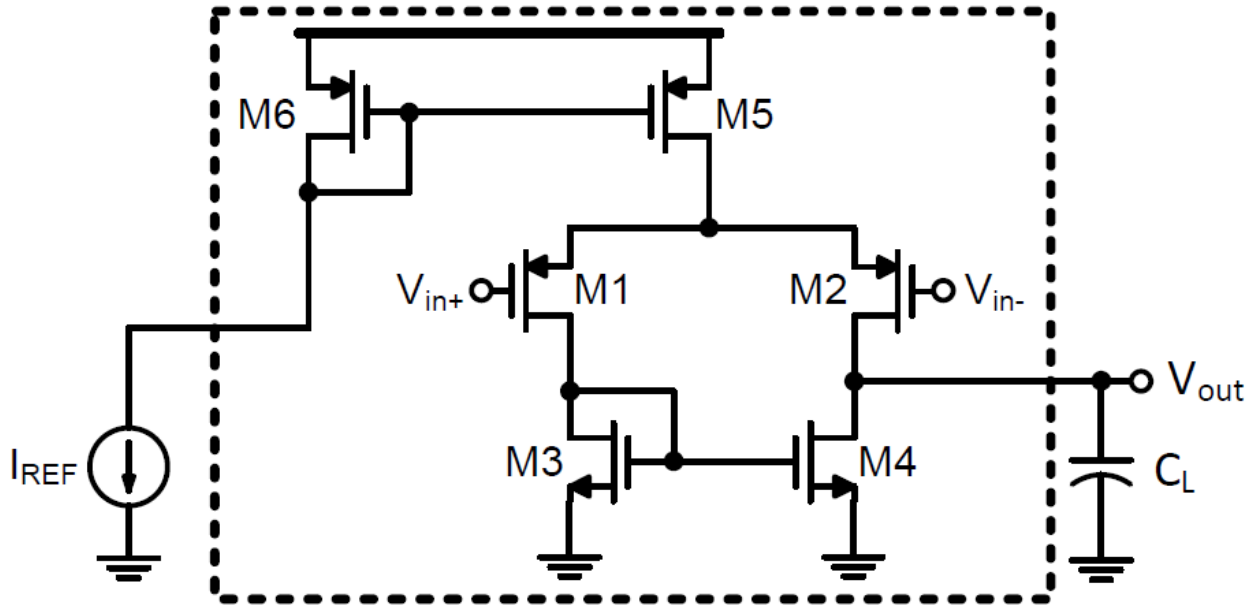
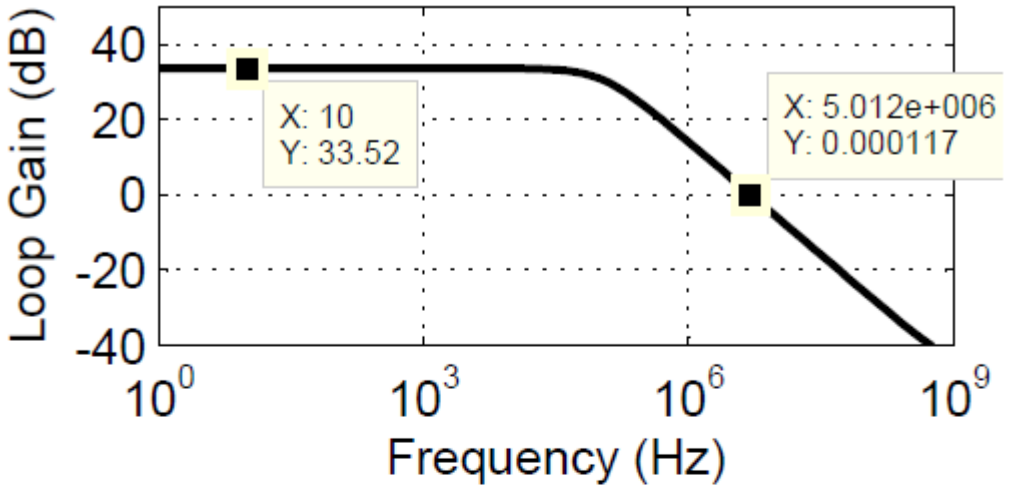
Sizing Results

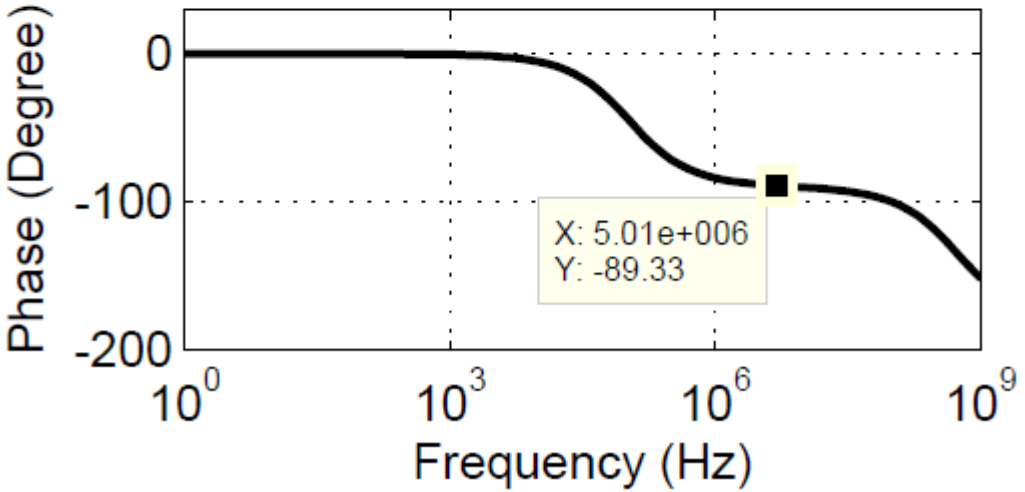
Transistor	g_m / I_D	Length	Width	Function
M1 and M2	16	$0.8\,\mu m$	$24\,\mu m$	Input pair
M3 and M4	10	$0.6\,\mu m$	$2\,\mu m$	Current mirror load
M5 and M6	14	$1.2\,\mu m$	$52\,\mu m$ and $26\,\mu m$	Bias current mirror



Simulation Results (1/4)

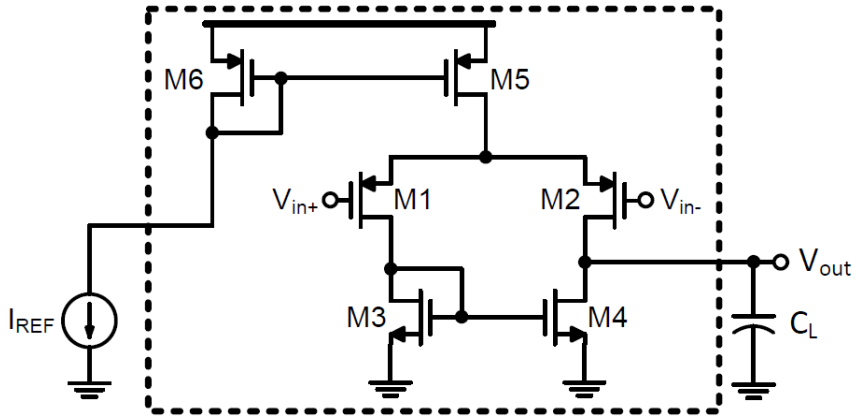


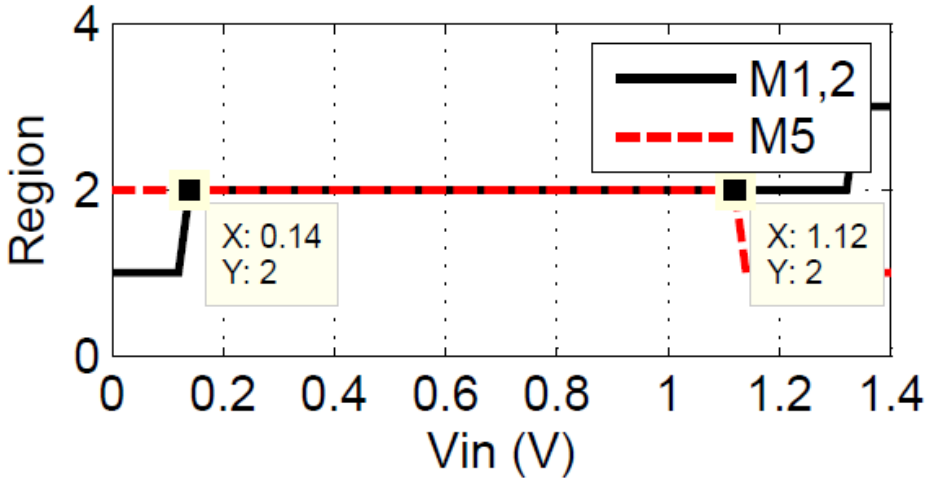
(a)



(b)

Simulation Results (2/4)





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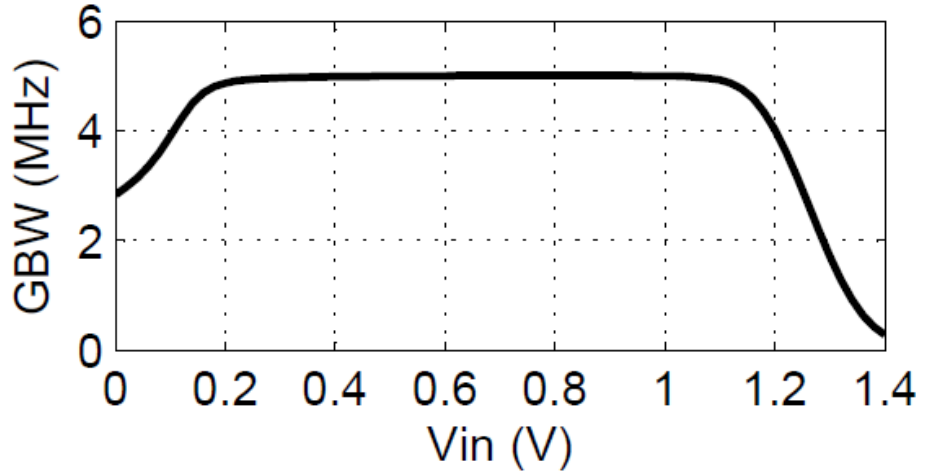

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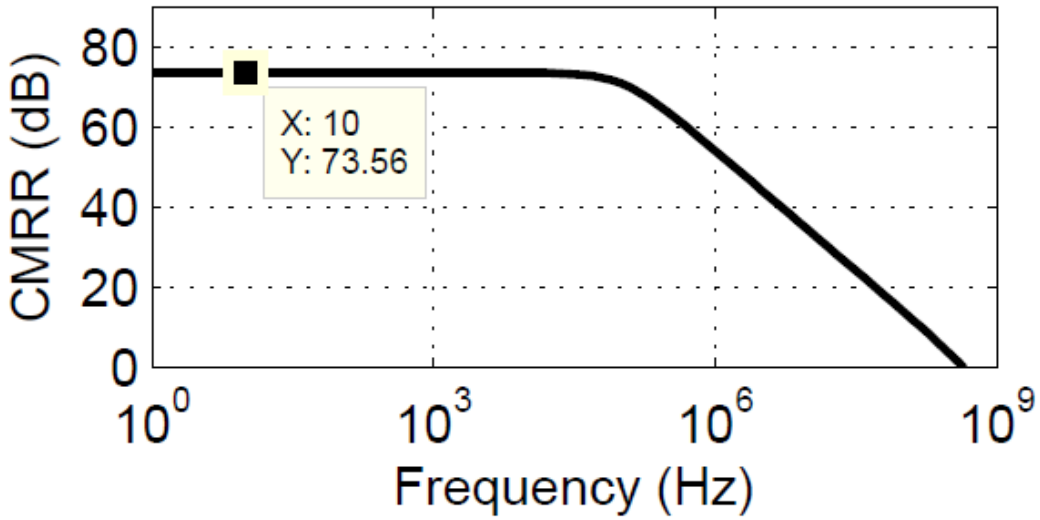
Simulation Results (3/4)



Simulation Results (4/4)

Specification	Required	Achieved
OTA Current Consumption	$20\,\mu A$	$20\,\mu A$
GBW	$5\,MHz$	$5\,MHz$
Phase Margin	70^o	90^o
Open Loop DC gain	$32\,dB$	$33.5\,dB$
Total Integrated Thermal Noise	$50\,\mu Vrms$	$48.6\,\mu Vrms$
Input Range	$0.2\,V - 1.1\,V$	$0.14\,V - 1.12\,V$
CMRR	$70\,dB$	$73.6\,dB$

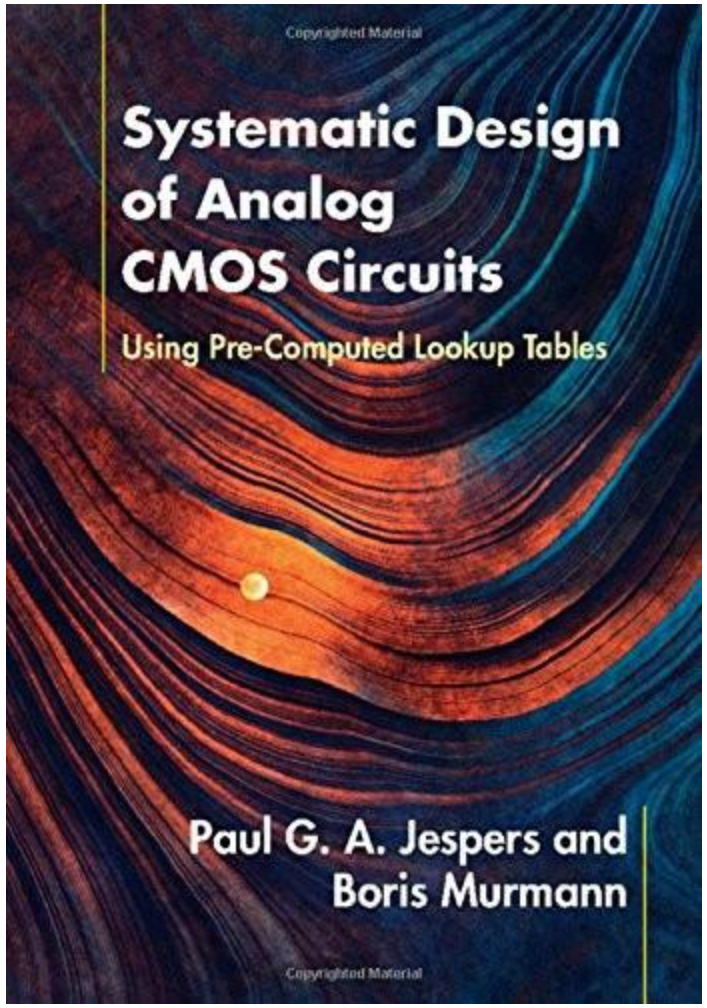
Notes

- The design charts (especially gm/gds) depend on V_{DS}
  - We neglected this dependence for simplicity
- We neglected body effect (should be considered if input pair is NMOS)
- We did not consider OTA self-loading
- We did not consider process variations, mismatch, and noise
- Taking the above points into account (and even more)
  - The design procedure becomes a bit complicated iterative procedure
  - But it is still “systematic”
  - Thus can be automated using a computer program!

Thank you!

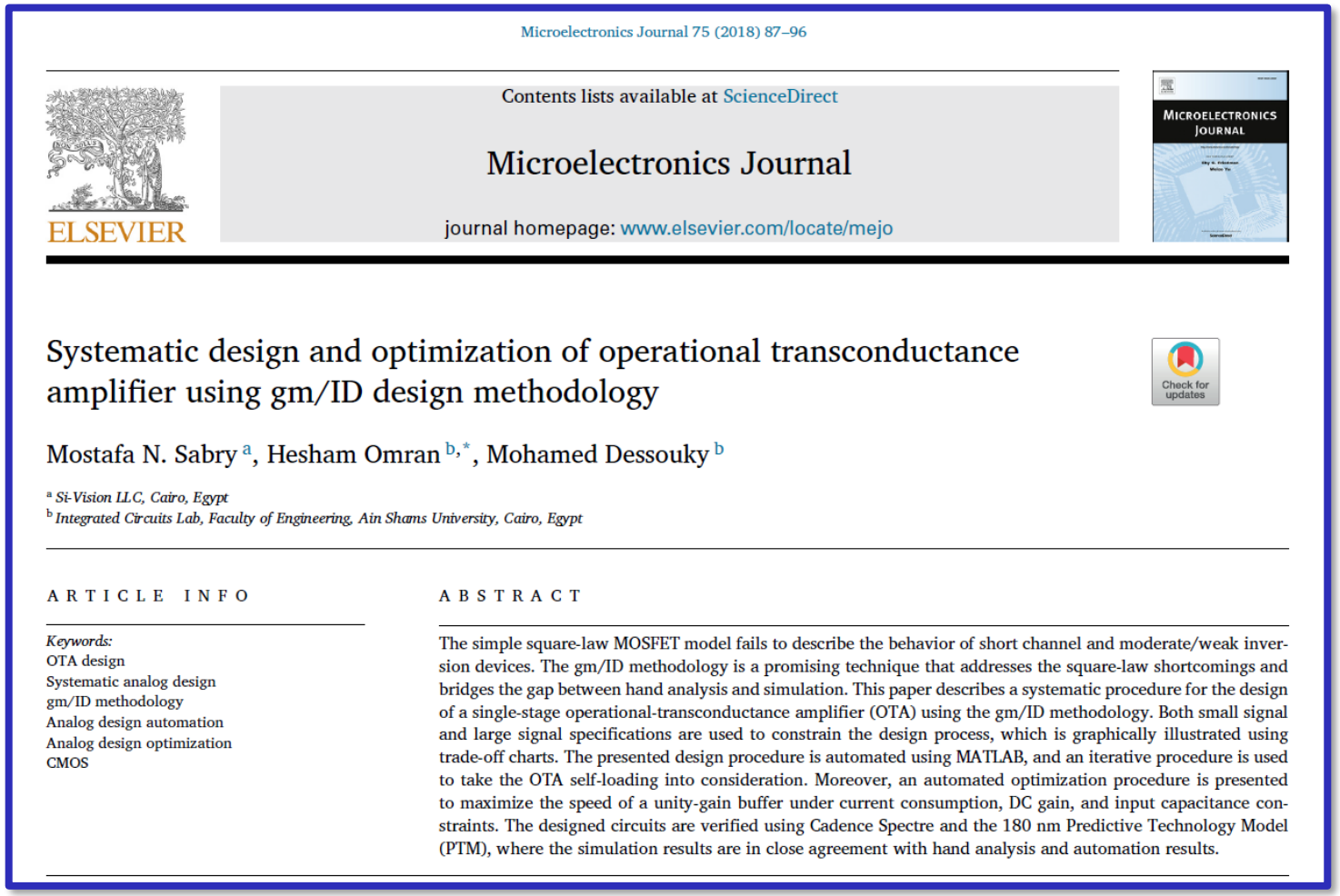
References (1/3)

- P. Jespers and B. Murmann, Systematic Design of Analog CMOS Circuits Using Pre-Computed Lookup Tables, Cambridge University Press, 2017.



References (2/3)

- M. N. Sabry, H. Omran and M. Dessouky, "Systematic design and optimization of operational transconductance amplifier using gm/ID design methodology," *Microelectronics Journal,* vol. 75, pp. 87-96, May 2018.



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Systematic design and optimization of operational transconductance amplifier using gm/ID design methodology

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Analog design optimization
CMOS

ABSTRACT

The simple square-law MOSFET model fails to describe the behavior of short channel and moderate/weak inversion devices. The gm/ID methodology is a promising technique that addresses the square-law shortcomings and bridges the gap between hand analysis and simulation. This paper describes a systematic procedure for the design of a single-stage operational-transconductance amplifier (OTA) using the gm/ID methodology. Both small signal and large signal specifications are used to constrain the design process, which is graphically illustrated using trade-off charts. The presented design procedure is automated using MATLAB, and an iterative procedure is used to take the OTA self-loading into consideration. Moreover, an automated optimization procedure is presented to maximize the speed of a unity-gain buffer under current consumption, DC gain, and input capacitance constraints. The designed circuits are verified using Cadence Spectre and the 180 nm Predictive Technology Model (PTM), where the simulation results are in close agreement with hand analysis and automation results.

References (3/3)

- B. Murmann, Gm/ID Starter Kit. [Online]. Available: https://web.stanford.edu/~murmann/gmid
- B. Murmann, EE214B Course Reader, Stanford University.
- B. Razavi, “Design Of Analog CMOS Integrated Circuit,” 2nd ed., McGraw-Hill, 2017.
- T. C. Carusone, D. Johns, and K. W. Martin, “Analog Integrated Circuit Design,” 2nd ed., Wiley, 2012.