Analog IC Design

Lecture 20
Common-Mode Feedback (CMFB)

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Outline

- Well-defined and Ill-defined output level
- Common-mode feedback (CMFB) loop
- Discrete-time CMFB
- CMFB loop practical aspects and examples
- Fully-differential OTA simulation example

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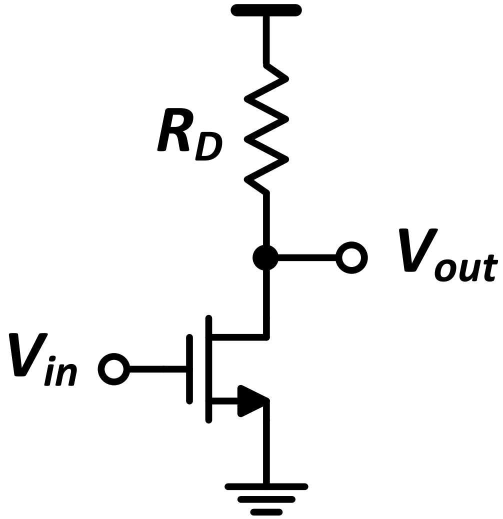
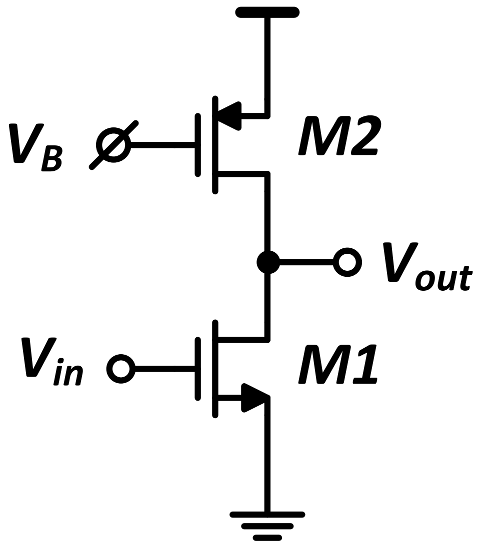
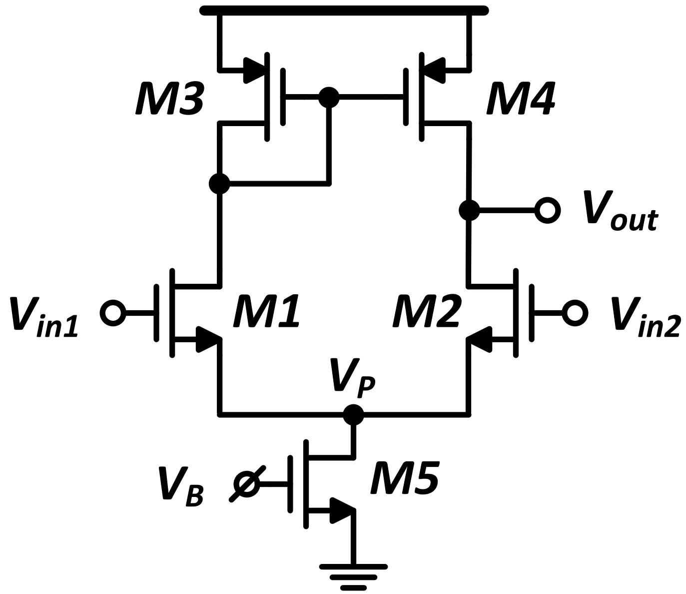
Well-Defined Output Level



Ill-Defined Output Level



Is This Output Well-Defined?



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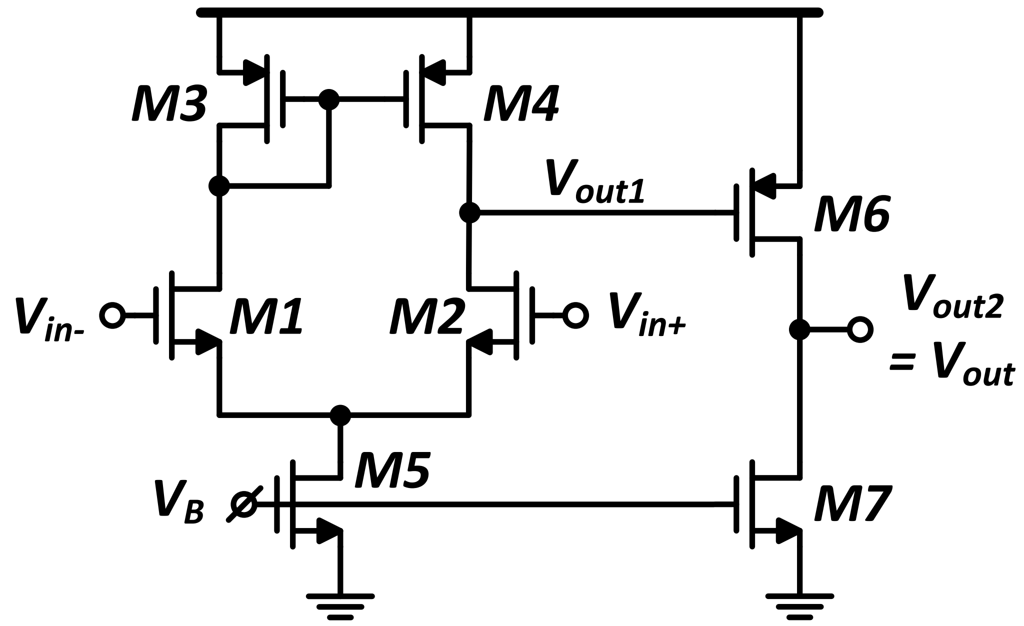
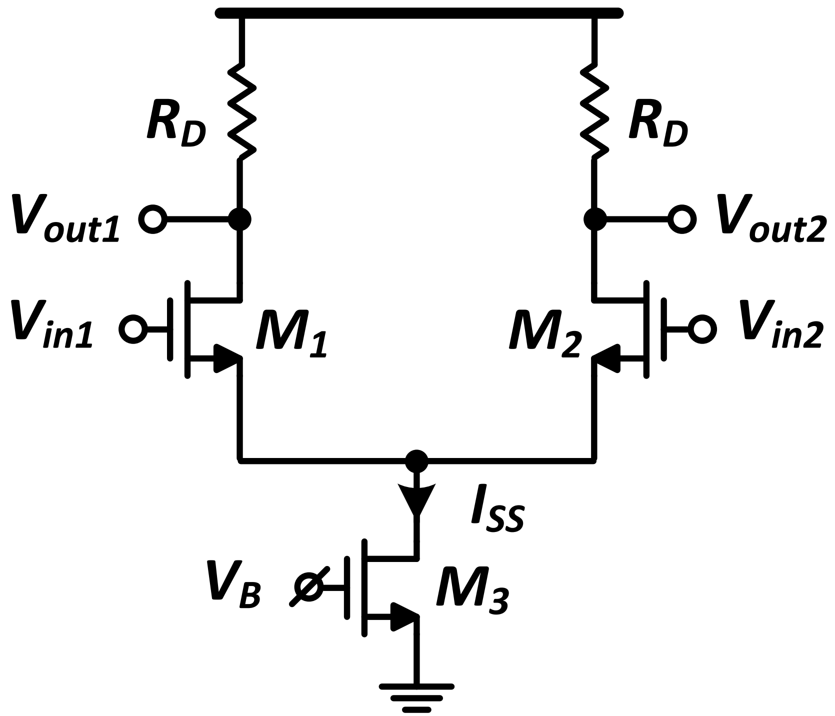
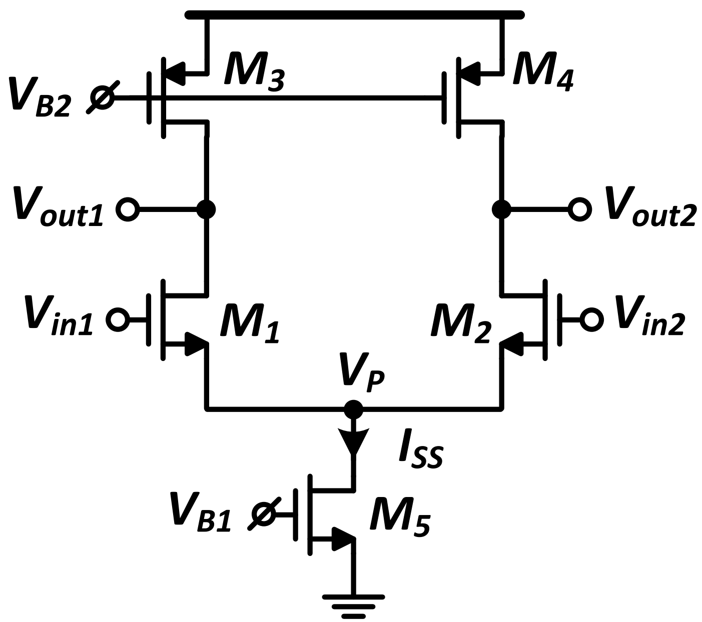


Well-Defined CM Level



Ill-Defined CM Level

- Mismatches ALWAYS create a finite error between $I_{D3,4}$ and $I_{SS}/2$
- $I_{D3,4} > I_{SS}/2$
  - $V_{out1,2}$ rise → $I_{D3,4}$ fall to $I_{SS}/2$ → M3 and M4 enter triode
- $I_{D3,4} < I_{SS}/2$
  - $V_{out1,2}$ fall → $I_{SS}/2$ fall to $I_{D3,4}$ → M1, M2, and M5 enter triode



Why Fully Differential Circuits

- Fully differential vs diff input SE output
  - Larger output swing
  - No mirror poles (higher speed)
  - Better CMRR and PSRR
  - Better SNR
  - Better linearity (lower distortion)
  - Easy to analyze!
- But common-mode feedback (CMFB) circuit is required…

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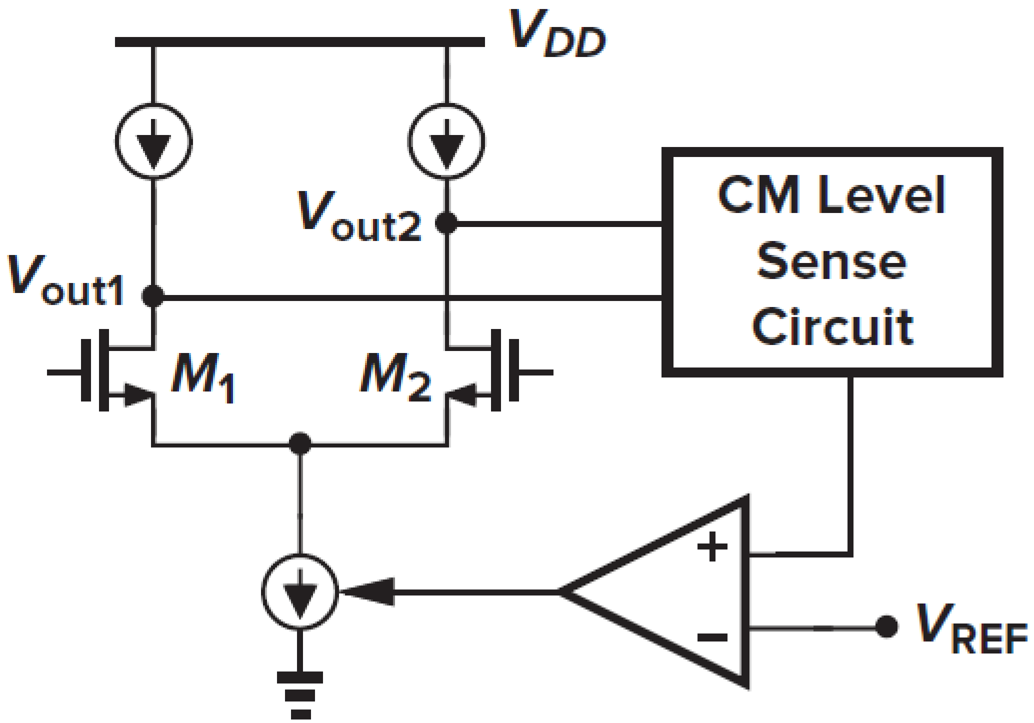
Common-Mode Feedback (CMFB)

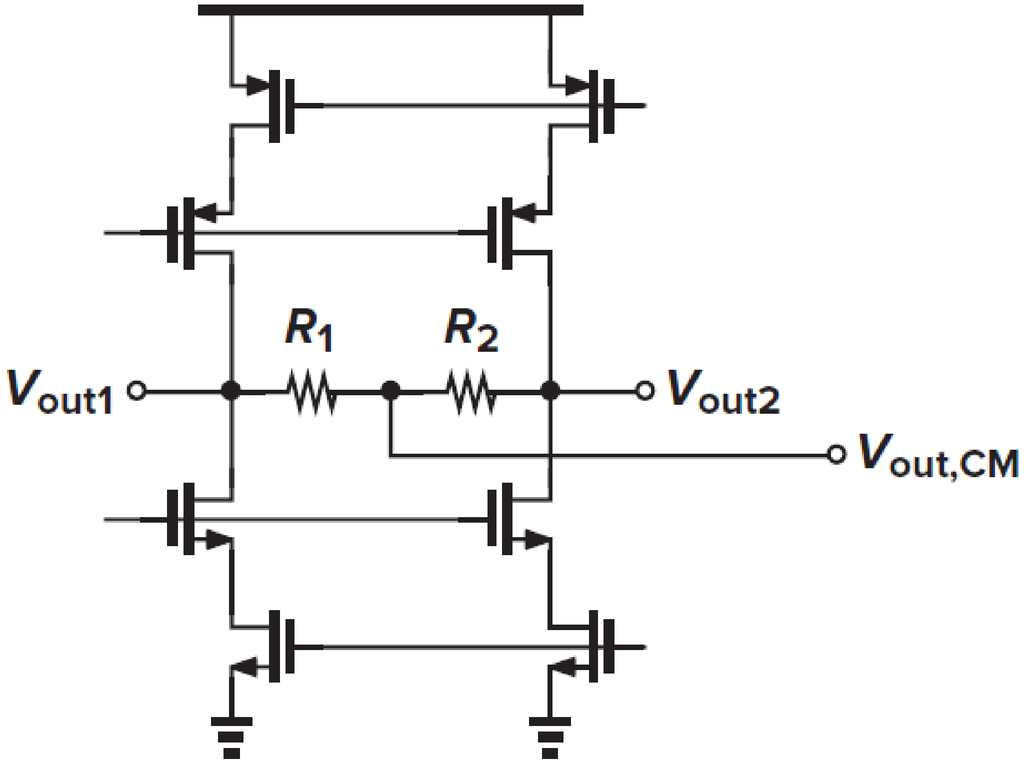
- Negative FB system
  1. Sense CM level
  2. Compare it to a reference
  3. Return the error to the bias circuit



[Razavi, 2017]

CM Sensing: Resistive Sensing

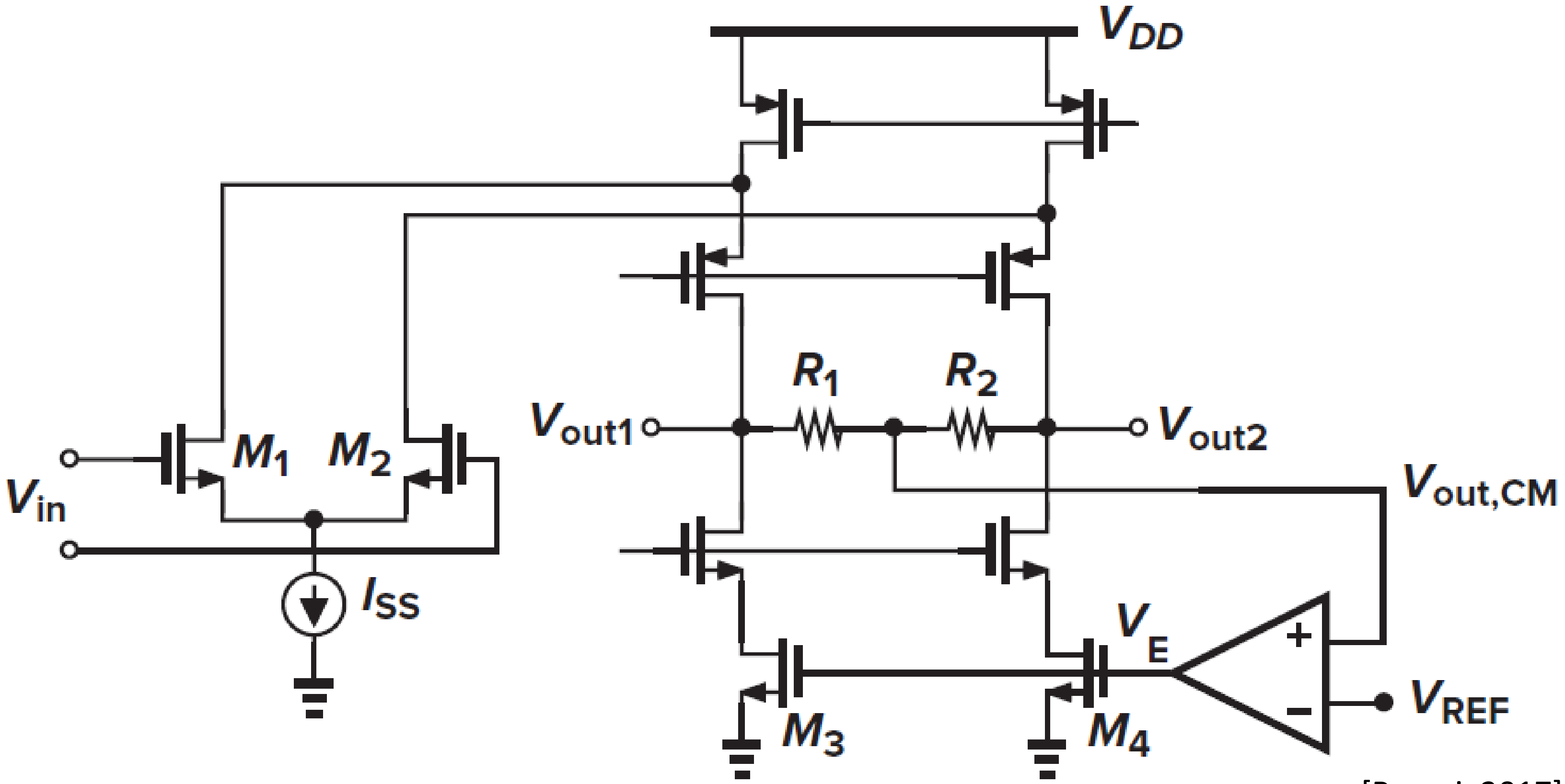
- Small R will degrade the gain
- Large R occupies large area and has large parasitic capacitors
  - May degrade the CMFB loop stability!



[Razavi, 2017]

CMFB Loop Example

- Resistive sensing
- The feedback network forces the CM level of Vout1 and Vout2 to approach VREF



[Razavi, 2017]

CMFB Loop Example

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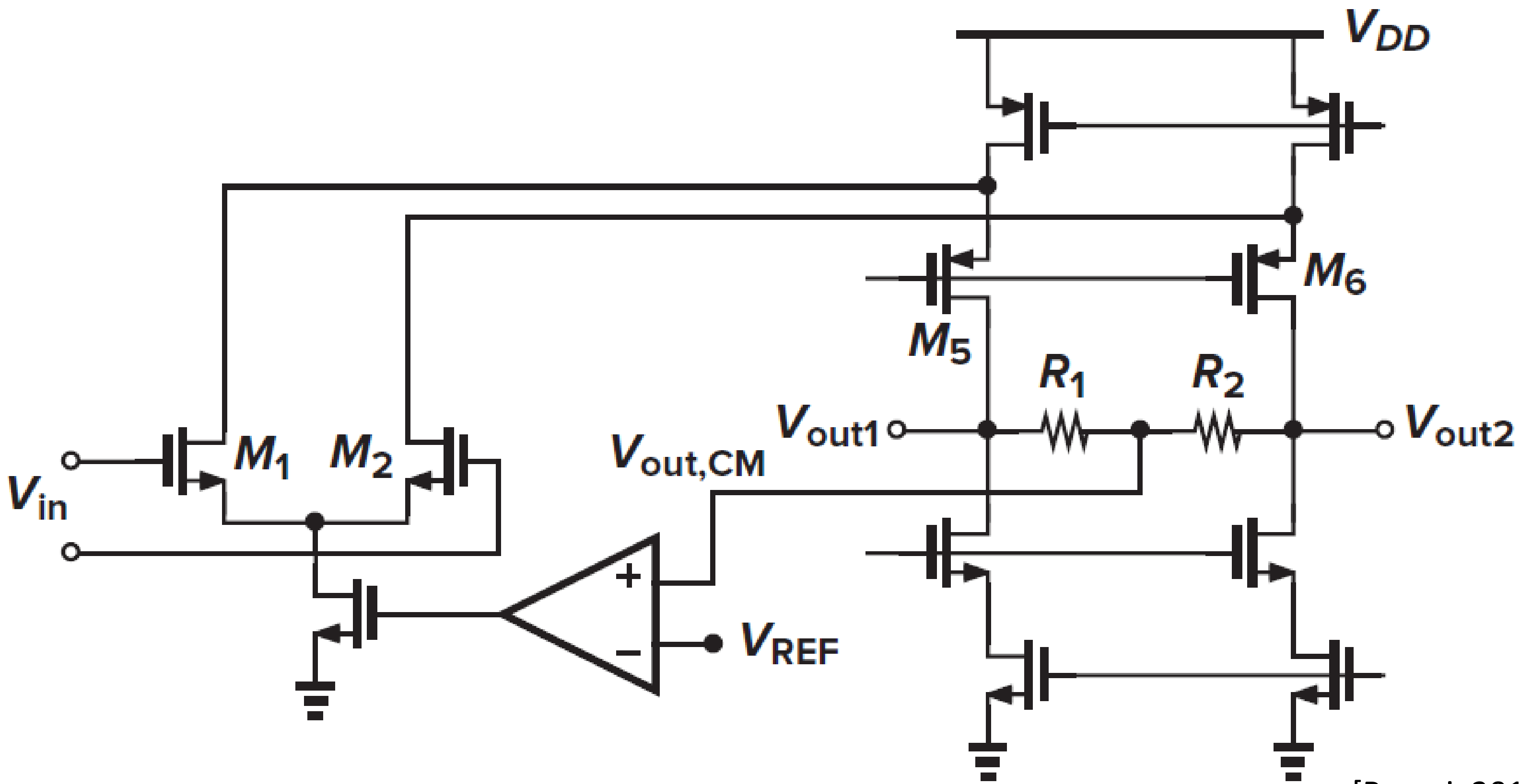
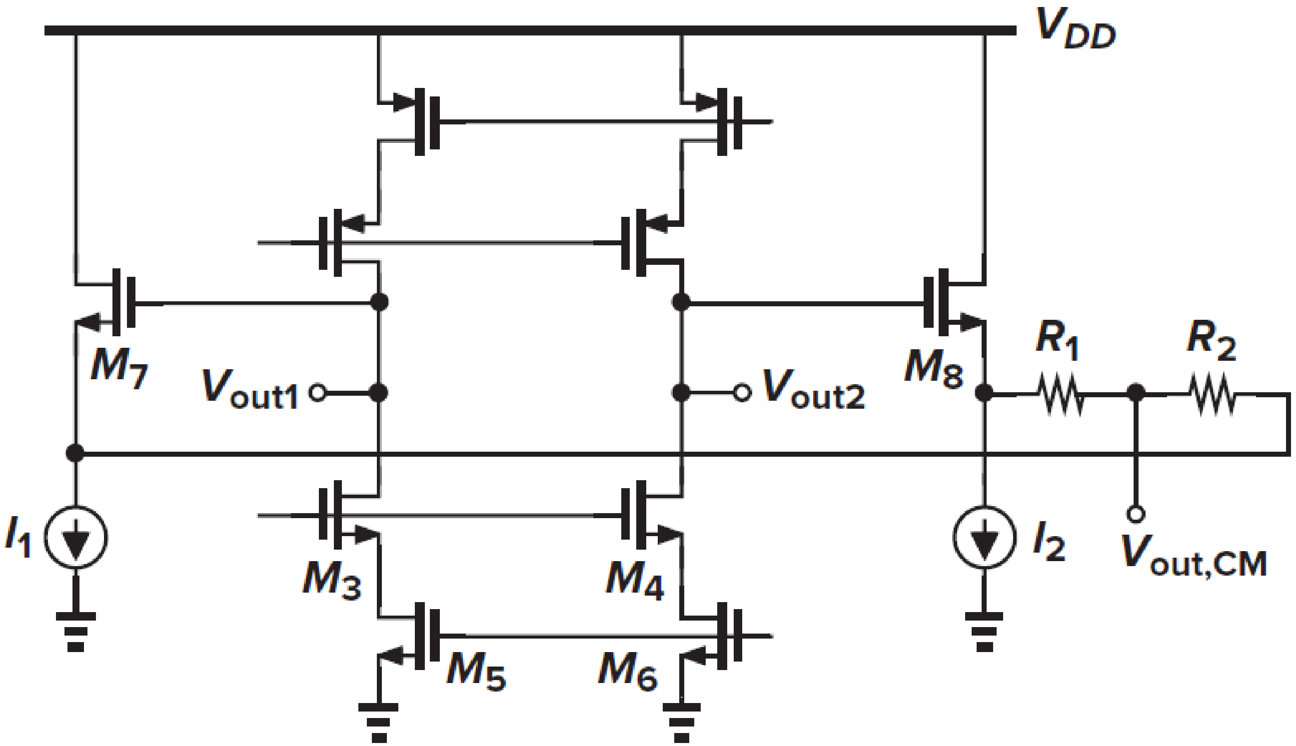


[Razavi, 2017]

CM Sensing: Source Followers

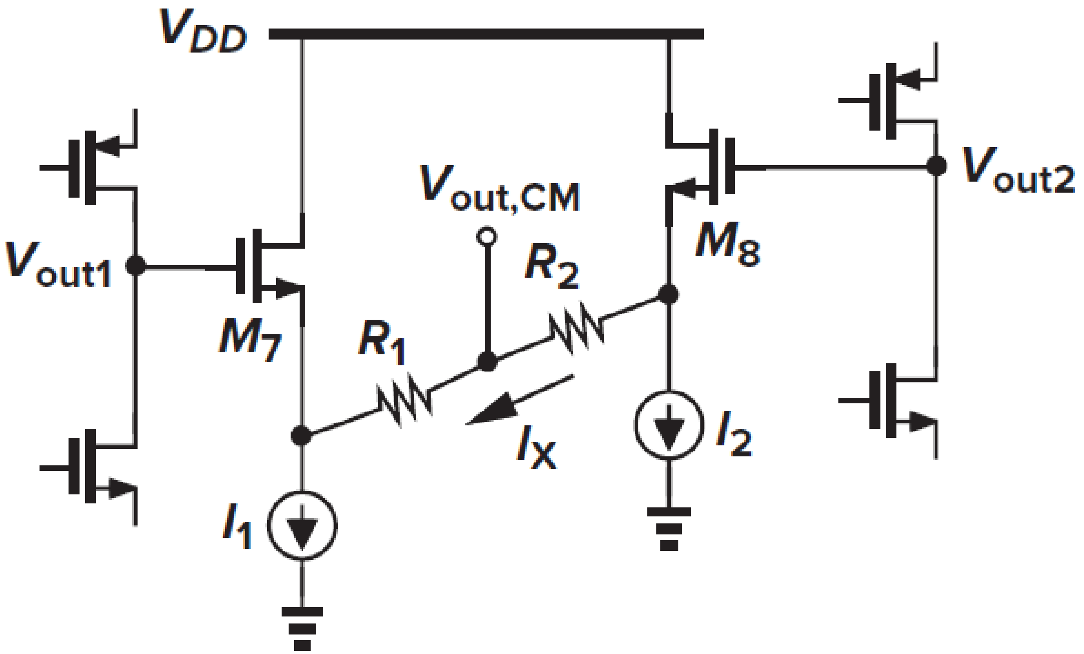
- The CD stage introduces DC shift
  - Should be considered in the comparison step



[Razavi, 2017]

CM Sensing: Source Followers

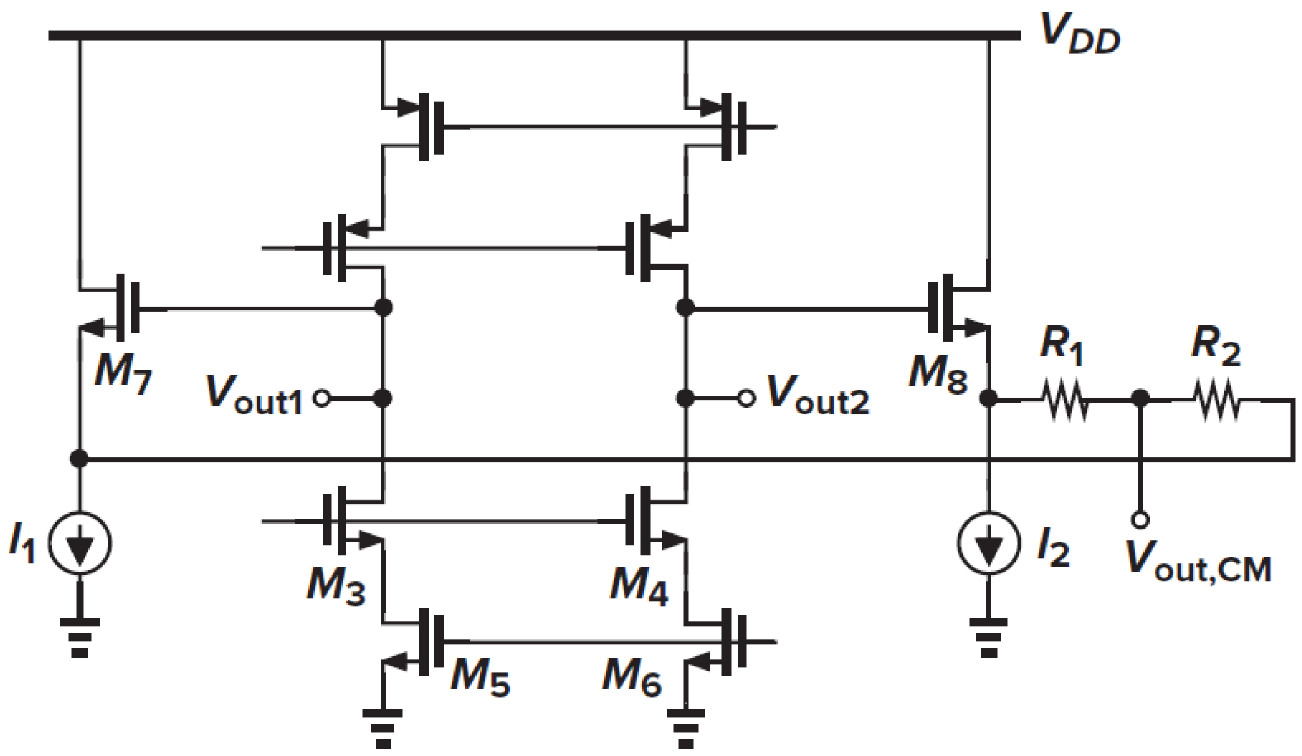
- If Vout2 > Vout1
  - I_1 must sink both $I_X \approx$ (Vout2 − Vout1)/(R1 + R2) and I_{D7}.
  - If (R1 + R2) or I_1 are not sufficiently large: I_{D7} drops to zero
- Large $R_{1,2}$: more area and more capacitance
- Large $I_{1,2}$: more power consumption



[Razavi, 2017]

CM Sensing: Source Followers

- Output swing is reduced
  - Without CMFB: $V_{out,min} = V_{ov3} + V_{ov5}$
  - With CMFB: $V_{out,min} = V_{TH} + V_{ov7} + V_{I1}$



[Razavi, 2017]

Continuous Time CMFB Summary

- Resistive sensing → Low voltage gain
- Source followers → Limited linear range and high power
- Other techniques exist
  - But also suffer from limited linear range
- Designing continuous-time (CT) CMFB circuits that are both linear and operate with low power-supply voltages is not an easy task
  - It is an area of continuing research!

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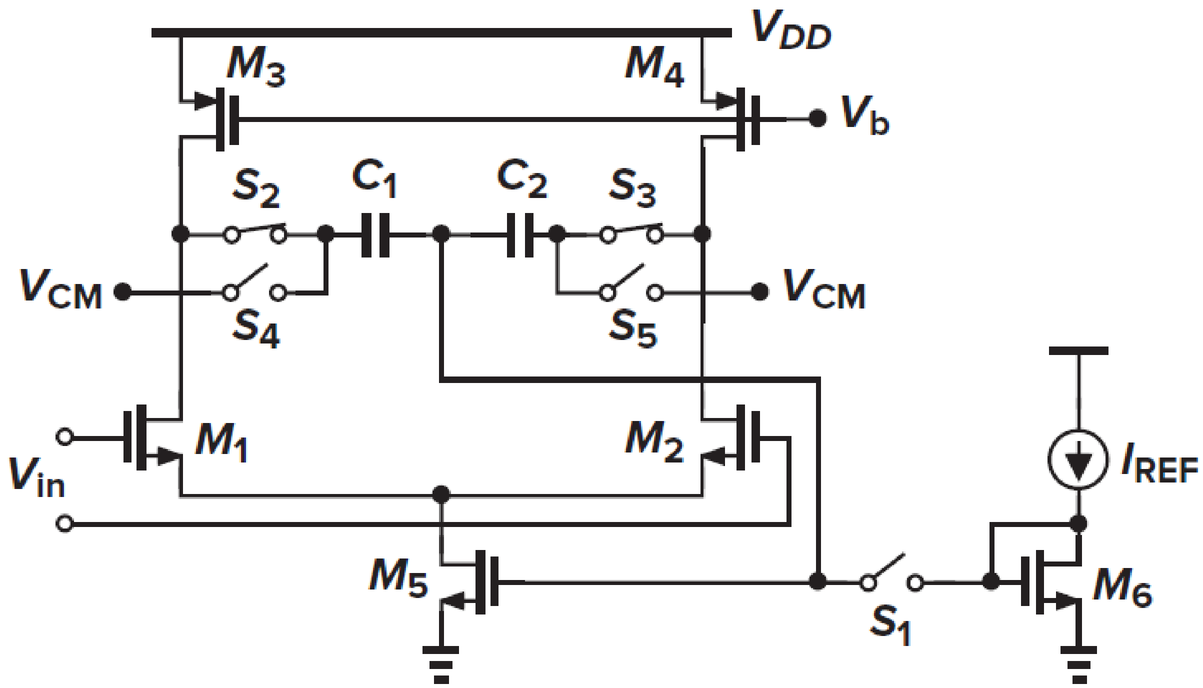
Discrete Time CMFB

- Another popular CMFB technique is discrete-time switched-capacitor CMFB
  - Uses switches and capacitors
  - The circuit must be refreshed periodically
  - Suitable for discrete-time switched-capacitor circuits

Switched-Capacitor CMFB

- Reset phase: S1, S4, and S5 close
  - Capacitor charged: $V_C = V_{CM} - V_{GS6}$
- Amplification phase: S2 and S3 close
  - $V_{outCM} = V_C + V_{GS5} = V_{CM} - V_{GS6} + V_{GS5} \approx V_{CM}$



[Razavi, 2017]

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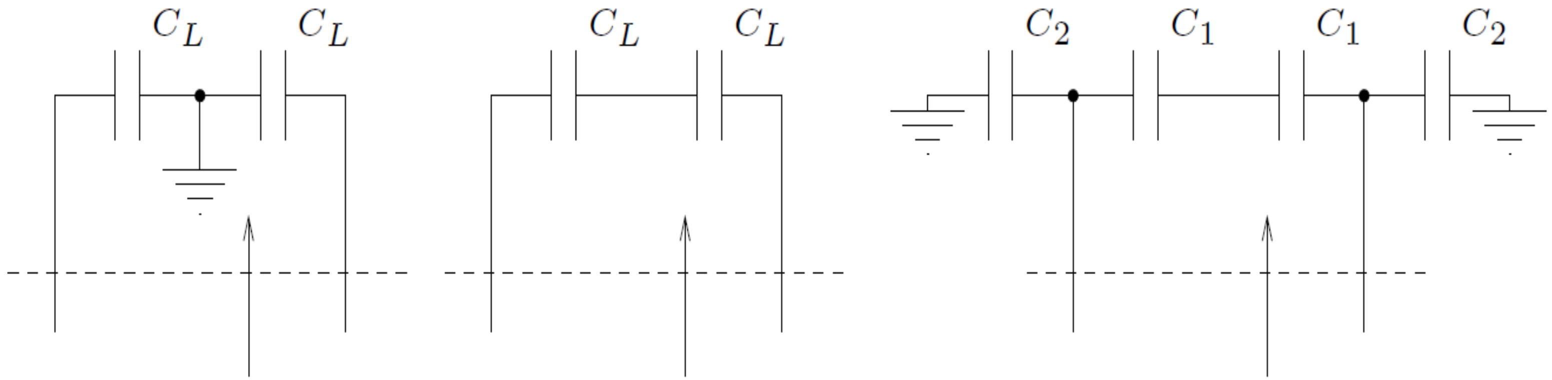
CMFB Loop Practical Aspects

- CMFB loop must be carefully analyzed
  - Draw small-signal model (use half-circuit principle)
  - Find LG, GX, PM, etc.
- We don’t need high DC LG for CMFB loop (why?)
- Ideally CMFB loop BW should be close to differential loop BW
  - Recover quickly from CM disturbance (e.g., supply and coupling noise)
  - But this means high power consumption
- Practically set CMFB bandwidth to 30% of differential loop BW
  - For $10\tau_{diff}$ of differential settling, CM loop will have $3\tau_{CM}$
  - $\sim 95\%$ of CM disturbance is removed

CMFB Loop Capacitive Loading

- Single-stage OTAs are compensated by large C_L
- The same C_L can be used to compensate the CMFB loop
- **CAUTION:** The differential and CM capacitive loading are not necessarily the same!



$Y_{cm} = 2sC_L$
$Y_{diff} = sC_L/2$

$Y_{cm} = 0$
$Y_{diff} = sC_L/2$

$Y_{cm} = 2sC_2$
$Y_{diff} = s(C_1 + C_2)/2$

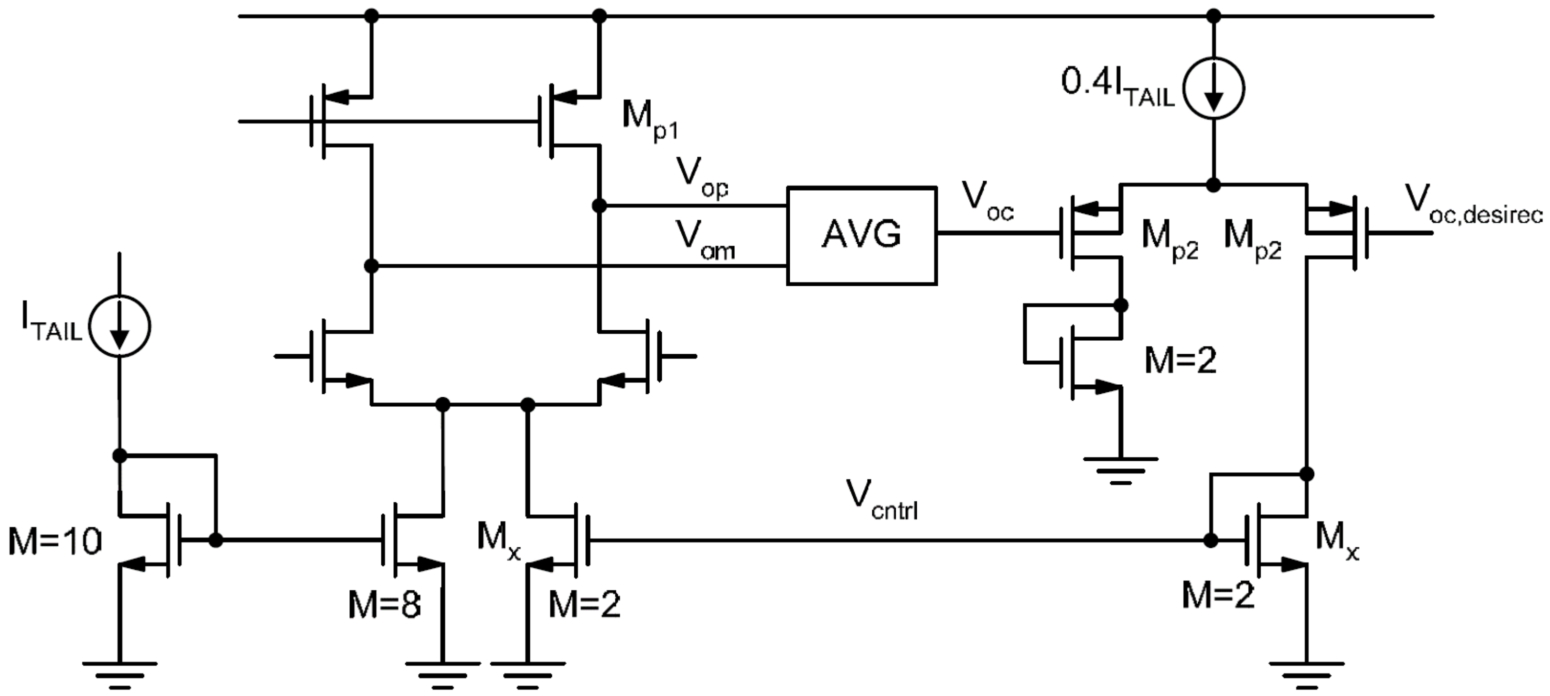
[N. Krishnapura, EE539]

CMFB Loop Example

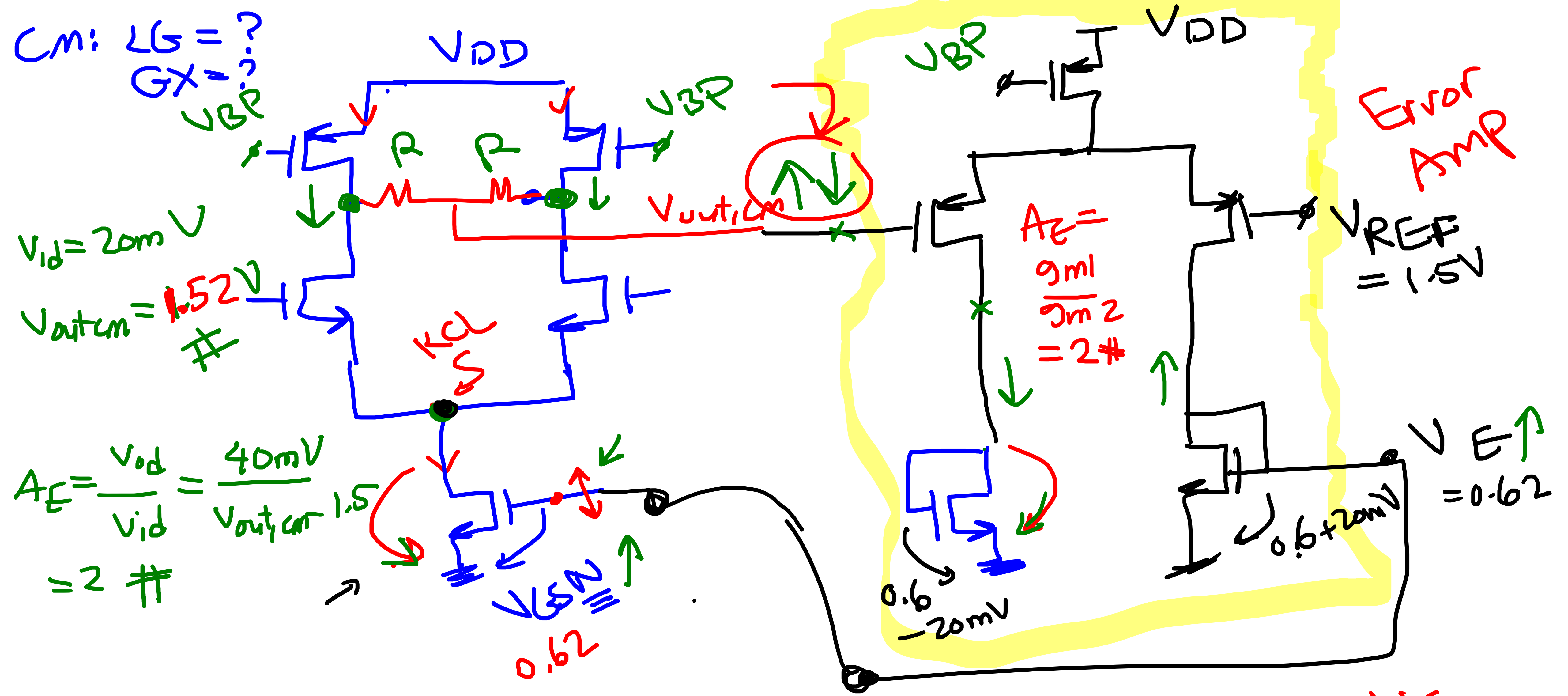
- Typically the CMFB loop tunes 20% of the tail current (Mx)

$$LG_{o,CM} \approx \frac{1}{2} \times g_{mx} \times r_{op1} \times \frac{g_{mp2}}{g_{mx}} \times \frac{1}{2}$$

$$\omega_{u,CM} \approx LG_{o,CM} \times \frac{1}{r_{op1} C_L}$$



[B. Murmann, EE214]



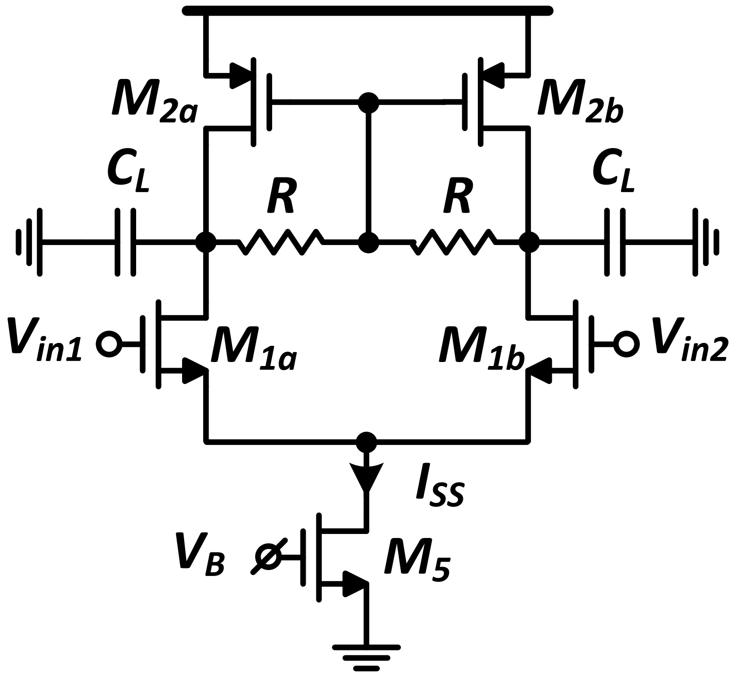
$$v_{id} = \frac{\Delta V_E}{A_E}$$

$$V_{EQ} = V_{GSNQ}$$

$$V_E = V_{EQ} + \Delta V_E$$

CMFB Loop Example

- Error amplifier replaced by a wire
- V_{CM} pinned to $V_{DD} - V_{GS2}$
- Max pk-to-pk diff swing $\sim 4V_T$



$$LG_{o,CM} \approx g_{m2} r_{o2}$$

$$LG_{o,diff} \approx g_{m1}(r_{o1}||r_{o2}||R)$$

$$\omega_{u,CM} \approx LG_{o,CM} \times \frac{1}{r_{o2}C_L} = \frac{g_{m2}}{C_L}$$

$$\omega_{u,diff} \approx LG_{o,diff} \times \frac{1}{(r_{o1}||r_{o2}||R)C_L} = \frac{g_{m1}}{C_L}$$

$$\omega_{p2,cm} \approx \frac{1}{RC_{gg2}}$$

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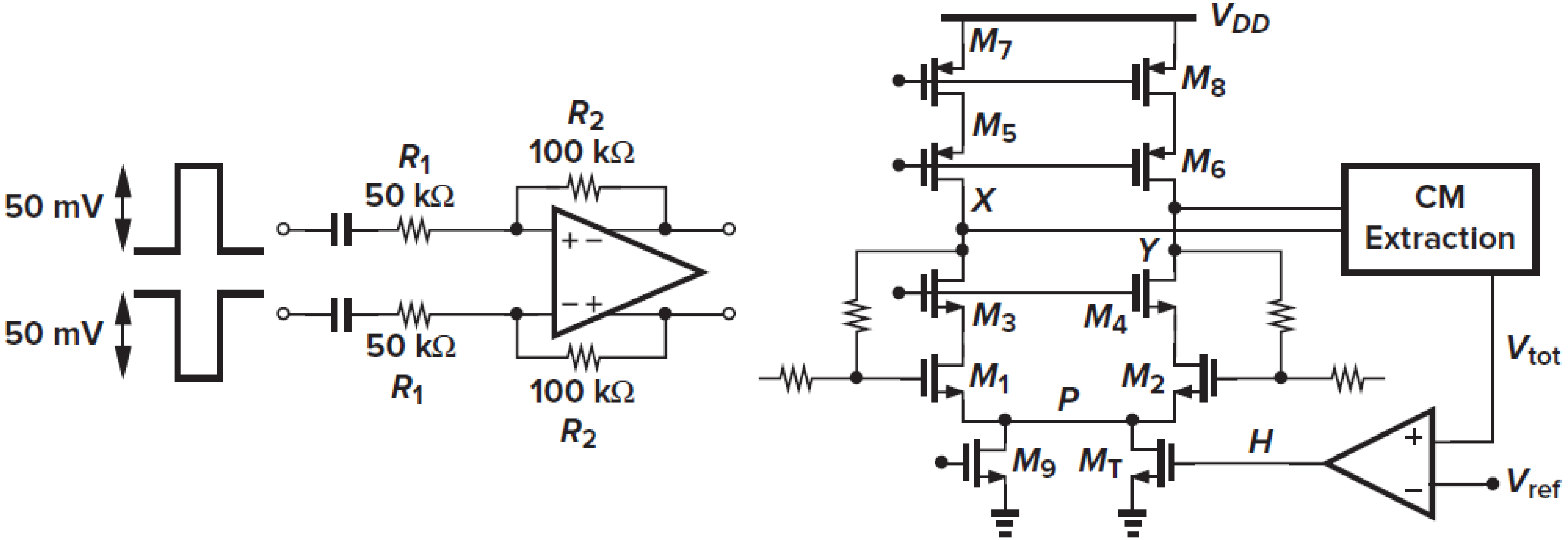
Fully-Differential OTA

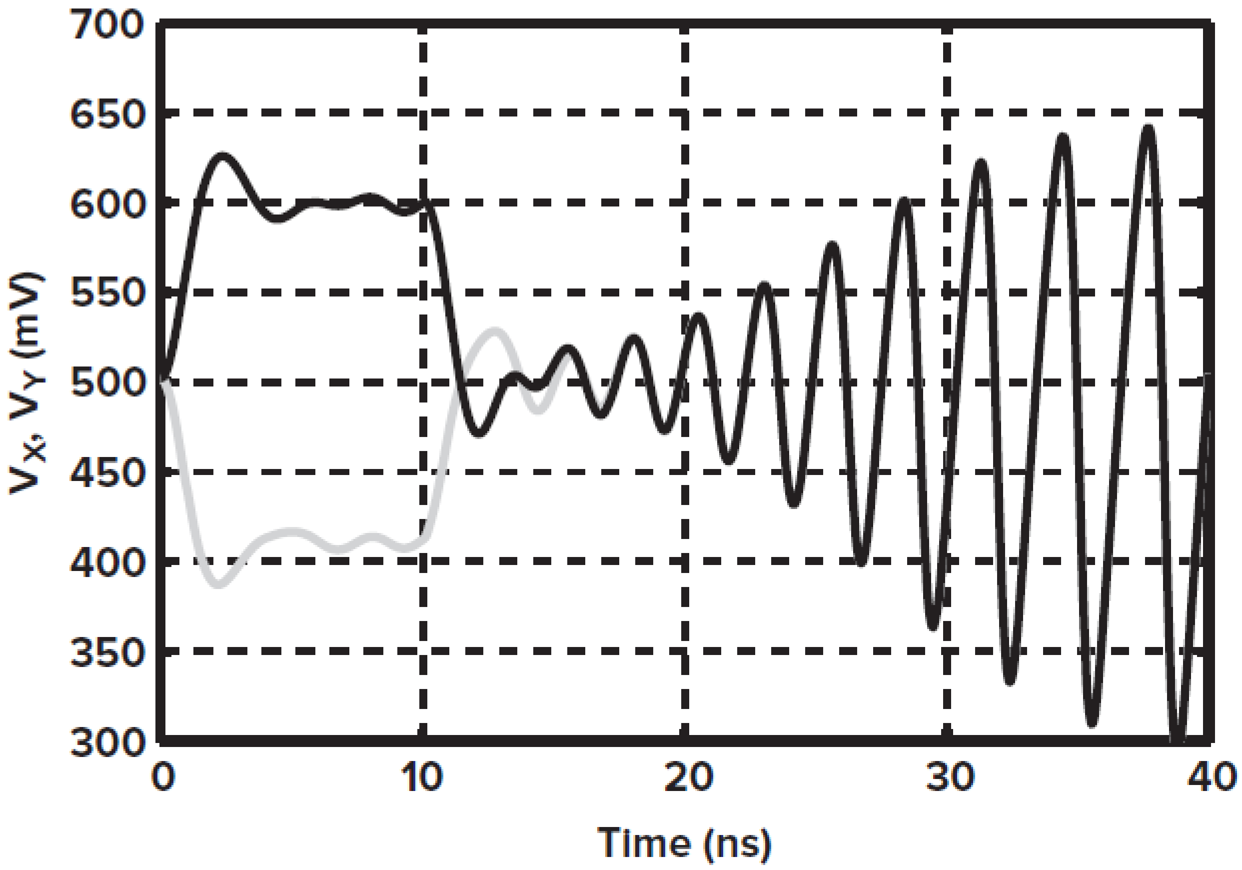
- Typically M9 carries 80% of I_{SS} → CMFB tunes 20% in MT
- Capture large signal effects on differential and CMFB loop stability
  - Place the OTA in a closed-loop feedback system
  - Apply differential pulses (transient analysis)



[Razavi, 2017]

Stability Analysis: Step Response

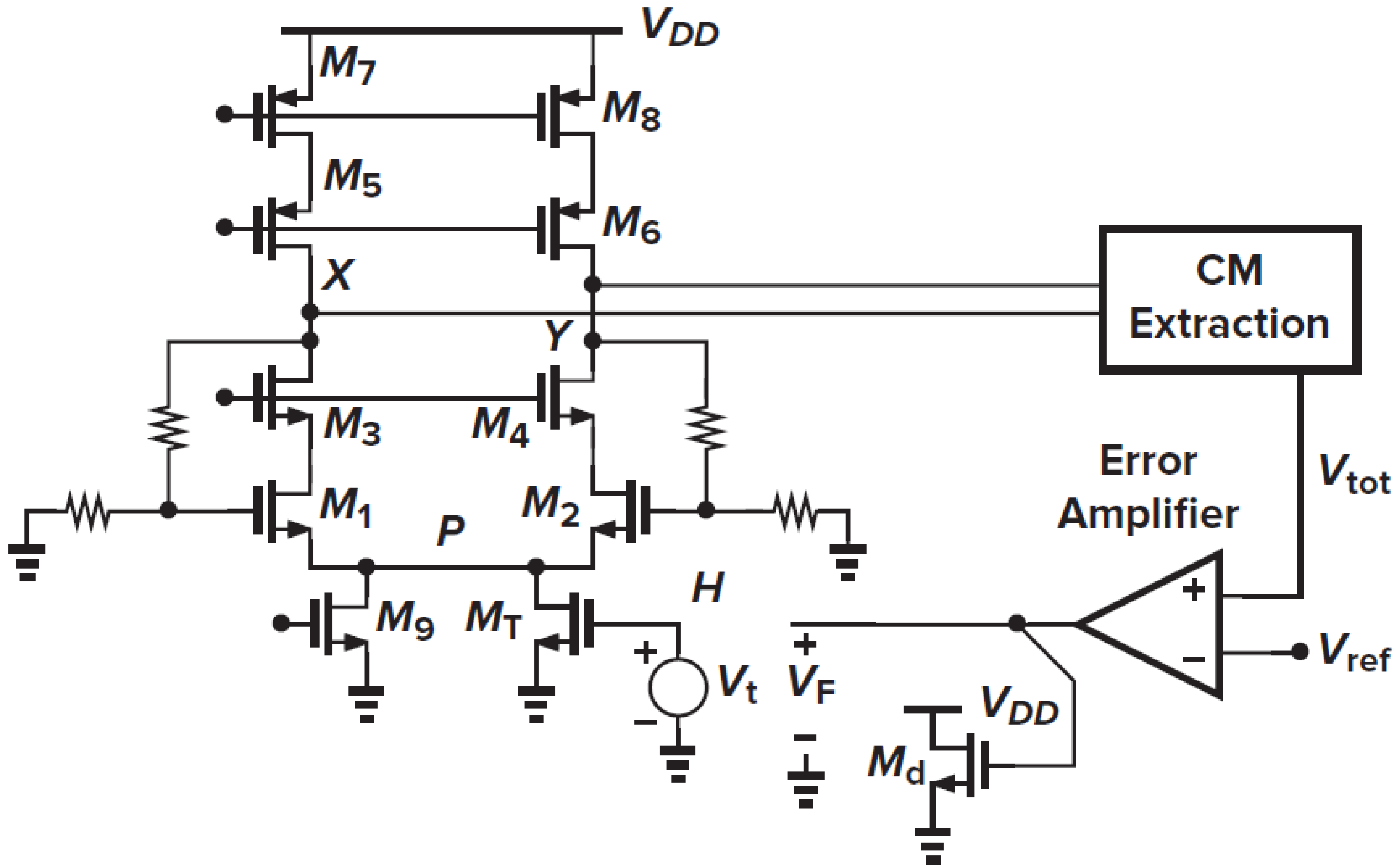
- The CMFB loop is unstable!
  - Requires compensation



[Razavi, 2017]

CMFB Loop Gain

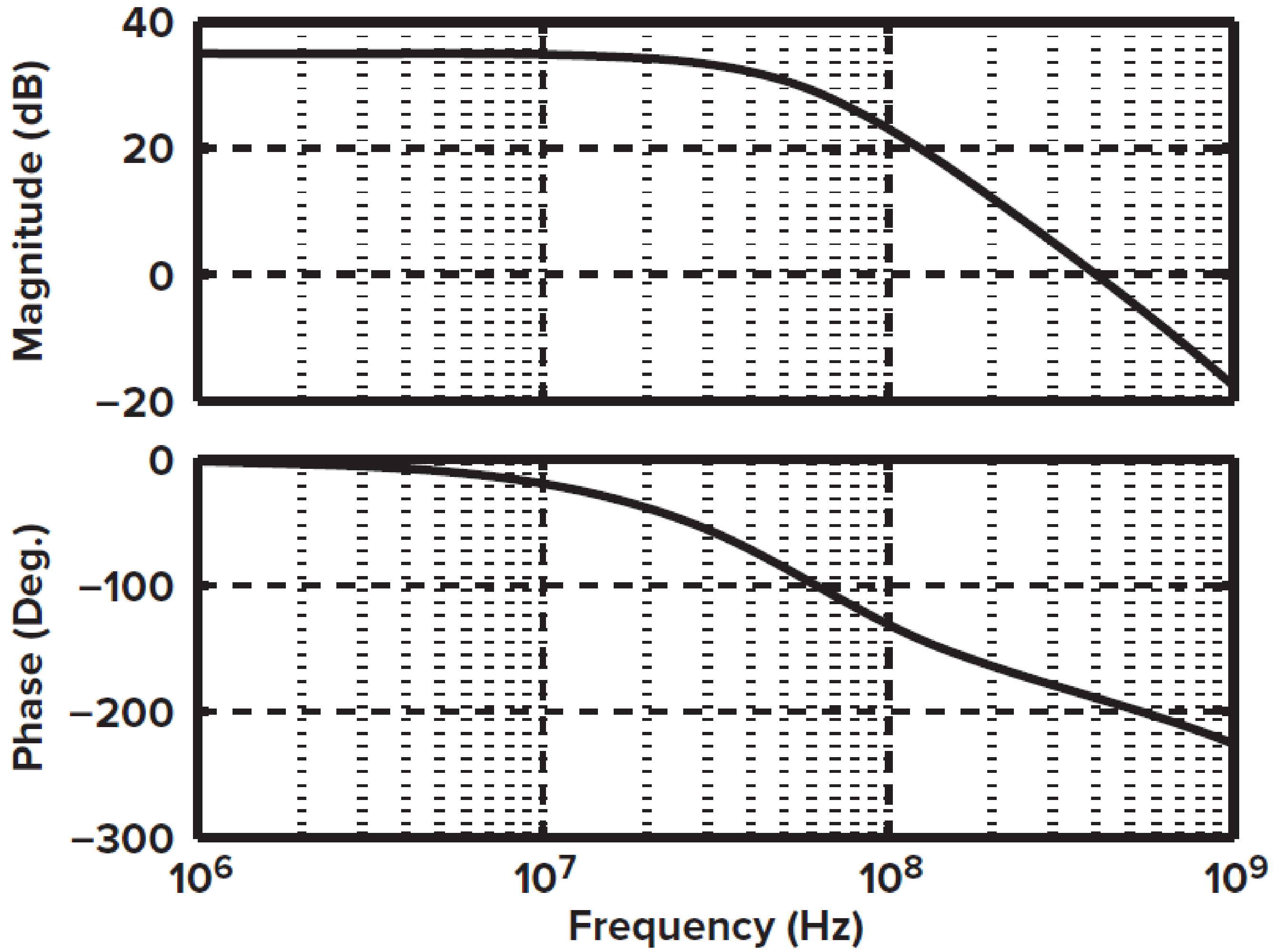
- Hand analysis: Break the loop to analyze the CMFB loop gain
- Simulation: Better to use STB analysis (loading and bilateral effects considered)



[Razavi, 2017]

Stability Analysis: LG

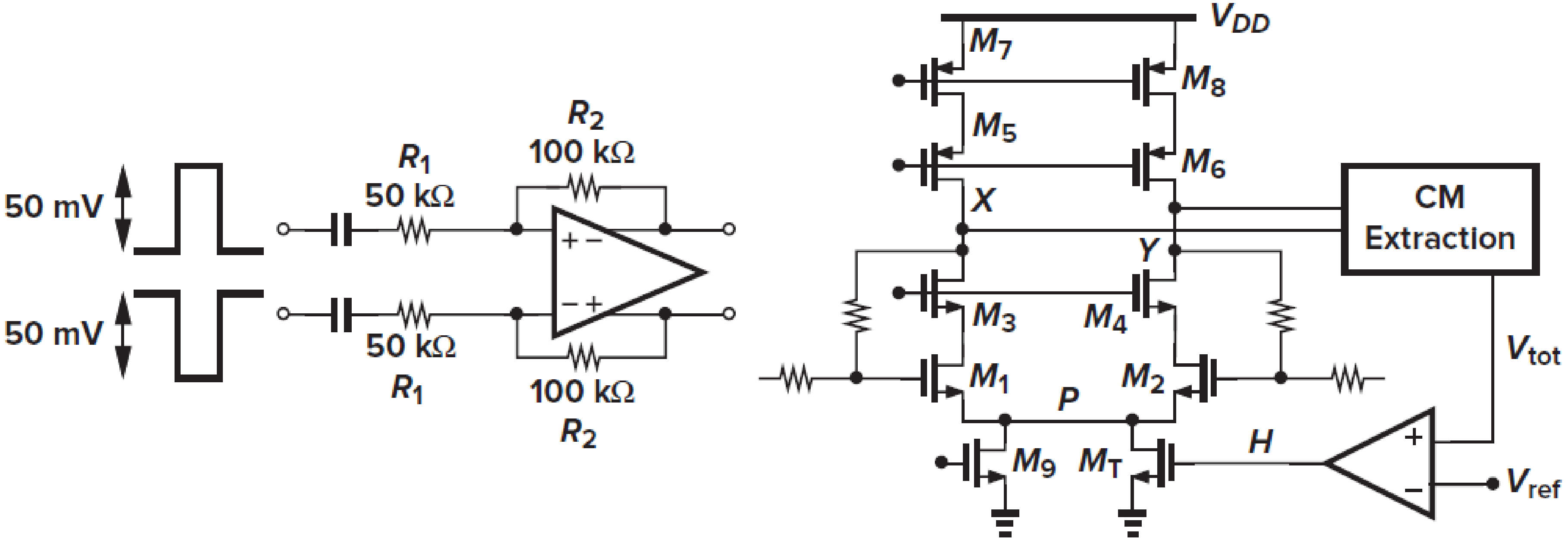
- PM = -10°



[Razavi, 2017]

CMFB Loop Compensation

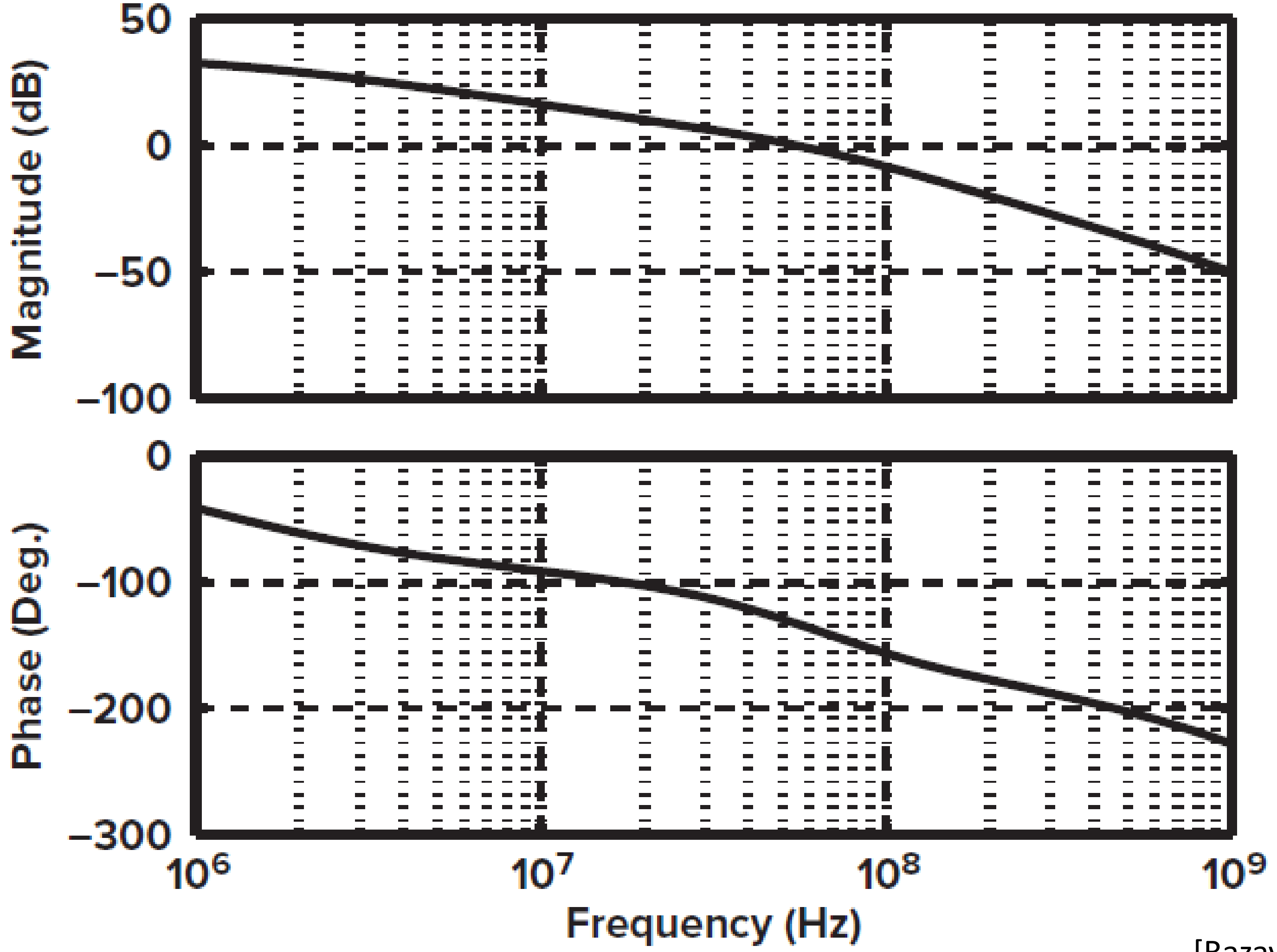
- Add 3pF to the error amplifier output
  - Not the best design decision…



[Razavi, 2017]

CMFB Loop Compensation

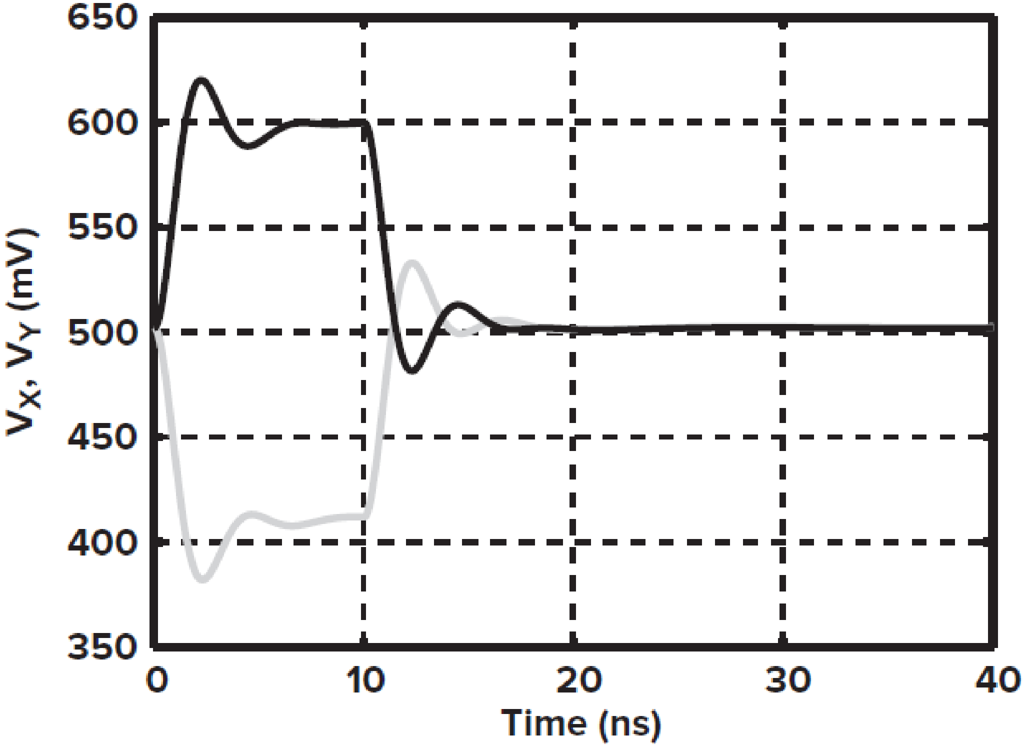
- PM = 50°



[Razavi, 2017]

Stability Analysis: Step Response

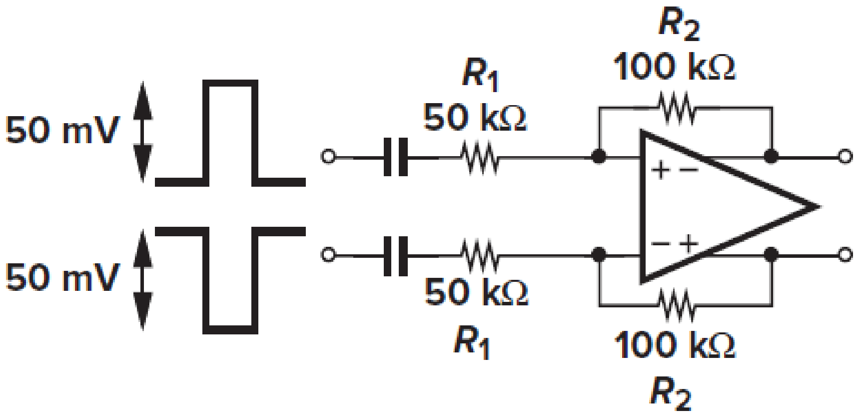
- CMFB loop is stable
  - But the CMFB loop is not fast enough
- But there is differential ringing
  - The differential loop PM is not sufficient

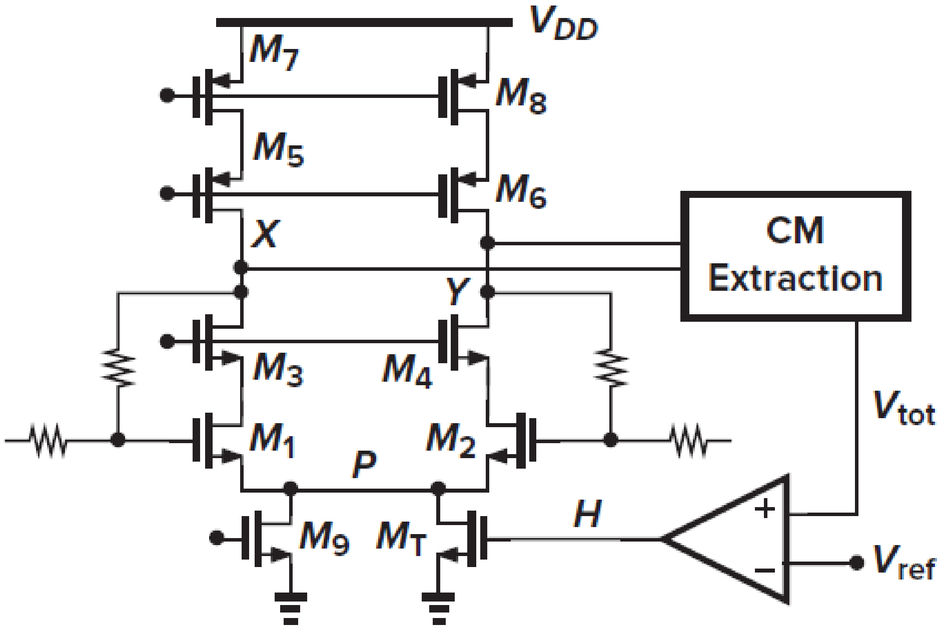


[Razavi, 2017]

Differential Loop Compensation

- The feedback resistance and the OTA input cap add a pole
- Fixed by adding small cap parallel with the large feedback resistance
  - Usually required when using large feedback resistance

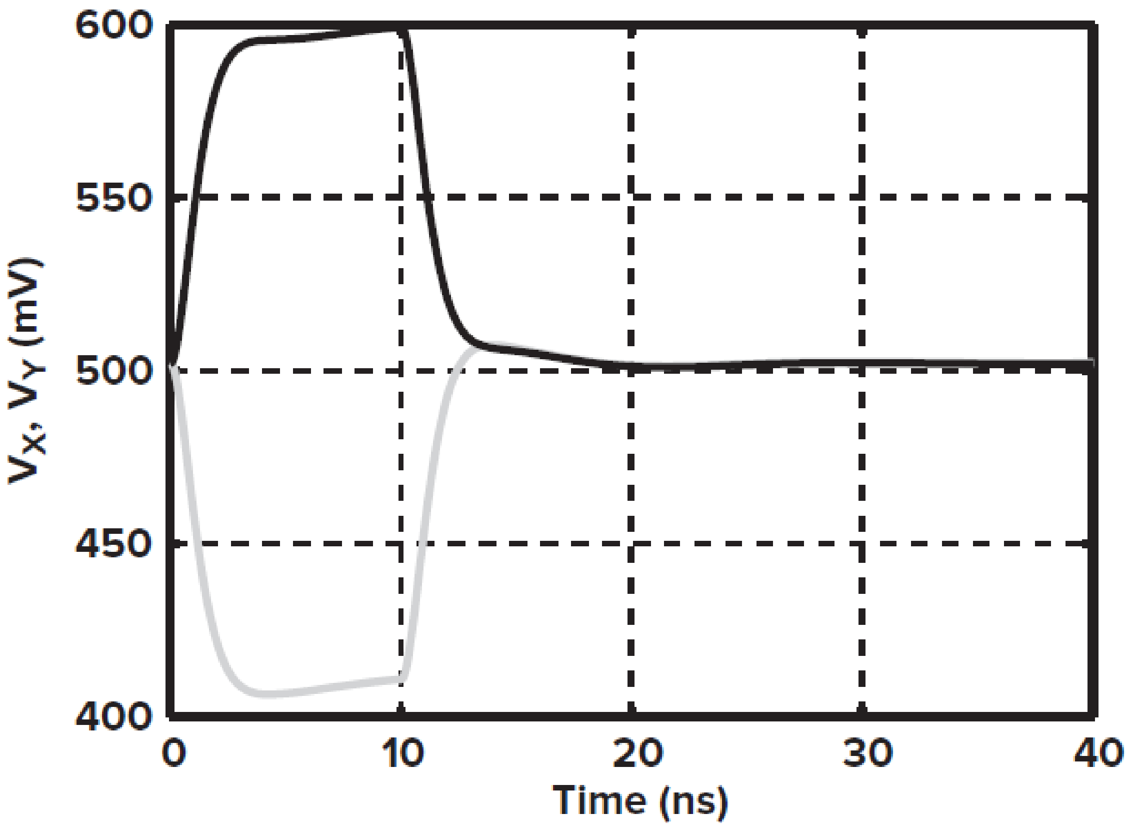




[Razavi, 2017]

Stability Analysis: Step Response

- Differential ringing disappeared
  - But the CMFB loop is not fast enough



[Razavi, 2017]

Thank you!

References

- B. Razavi, “Design of Analog CMOS Integrated Circuits,” McGraw-Hill, 2nd ed., 2017.
- T. C. Carusone, D. Johns, and K. W. Martin, “Analog Integrated Circuit Design,” 2nd ed., Wiley, 2012.
- B. Murmann, EE214 Course Reader, Stanford University.
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