Lab 6

Differential Amplifier

Part 1: Sizing Chart

Required Spec:

Parameter	
Supply (VDD)	$1.8V$
Bias current (ISS)	$40\mu A$
Differential gain	8
CM output level1	$VDD/3$
Load capacitance	$1pF$
Supply (VDD)	$1.8V$
Bias current (ISS)	$40\mu A$

Input Pair Sizing:

$$Required\ R_D:\quad V_{RD} = 0.6 \rightarrow R_D = \frac{V_{RD}}{I_D} = \frac{0.6}{20\mu} = \mathbf{30K\Omega}$$

$$|Av| \approx 0.91 \times gmR_D = 0.91 \times \frac{2ID}{V^*} \times RD = \frac{1.82V_{RD}}{V^*} = 8$$

$$V^* = \frac{1.82V_{RD}}{|A_v|} \approx \mathbf{136mV} \quad (Assuming\ ro = 10 * R_D)$$

From SA: $\boldsymbol{L = 350nm}$, $\boldsymbol{W = 30.79\mu m}$

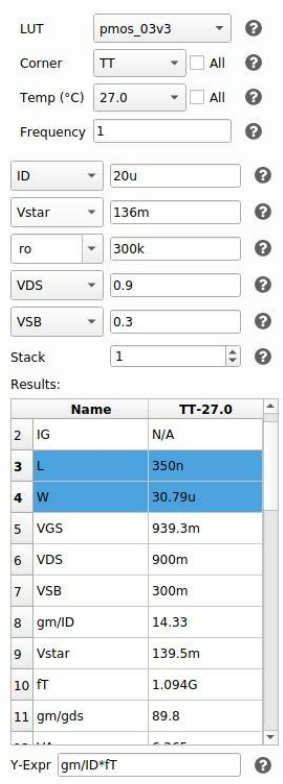

Figure 1 Input Pair Dimensions from Sizing Assistant

8) The SA assumes VDS at 0.9V

Thus $V_{CM} = VDD - VGS_{4,3} - VDS_1 = \mathbf{0.56V}$

Current Mirror Sizing:

Parameter	
Input current	$20\mu A$
Percent mismatch: $\sigma(Iout)/Iout$	≤ 2%
Compliance voltage	≤ $200mV$
Area	Minimize

Using the equation supplied in the Lab manual for mismatch we can draw the following graphs

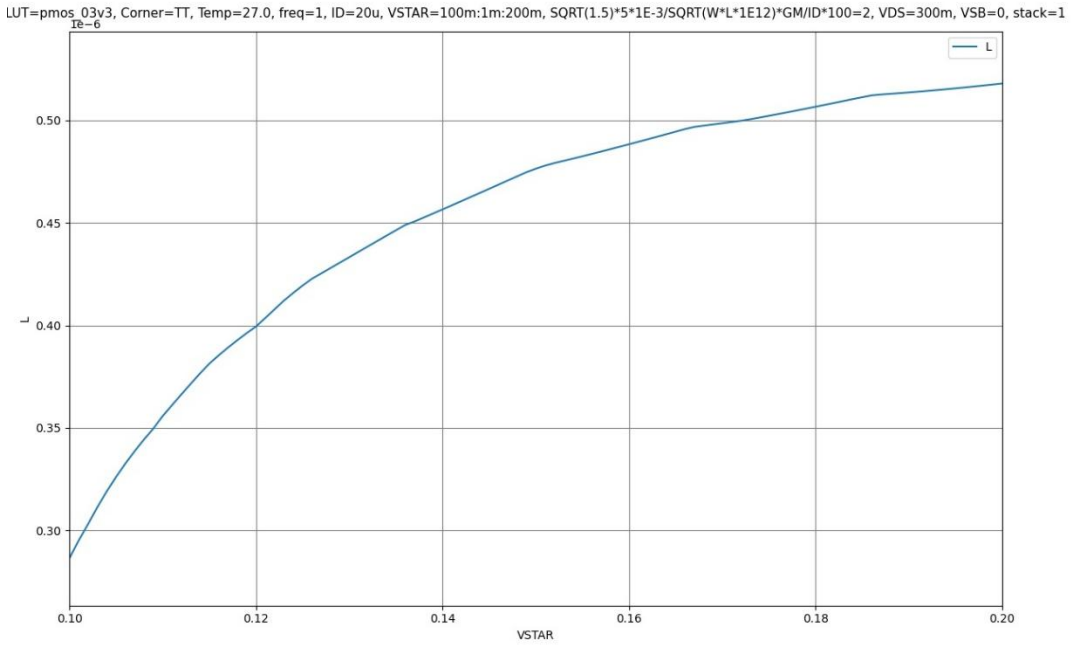

Figure 2 L vs Vstar

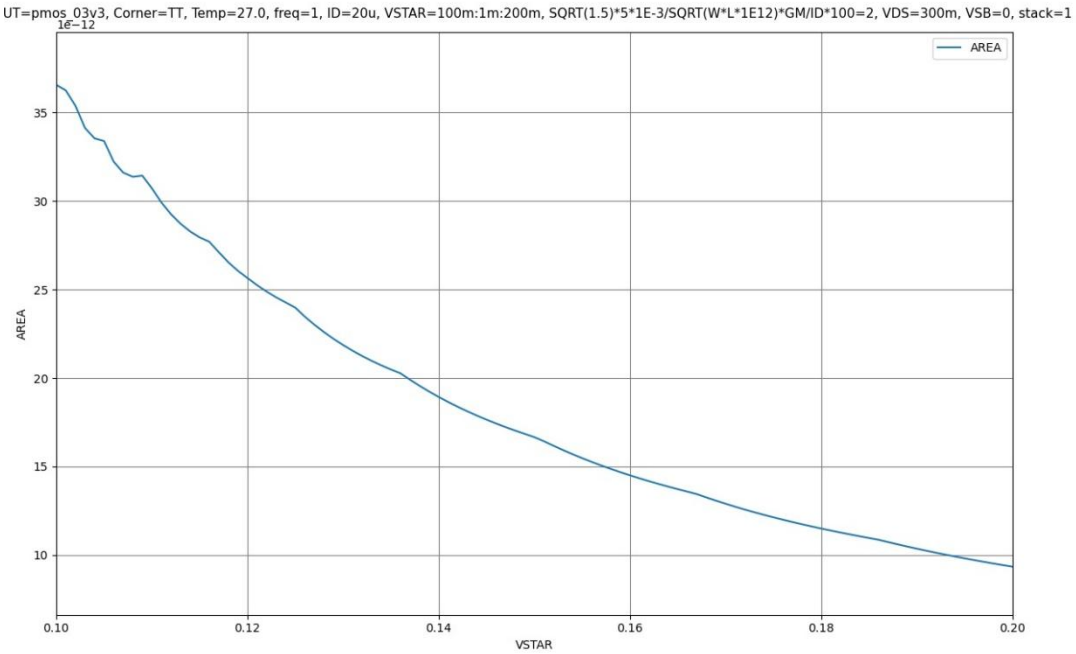

Figure 3 Area vs Vstar

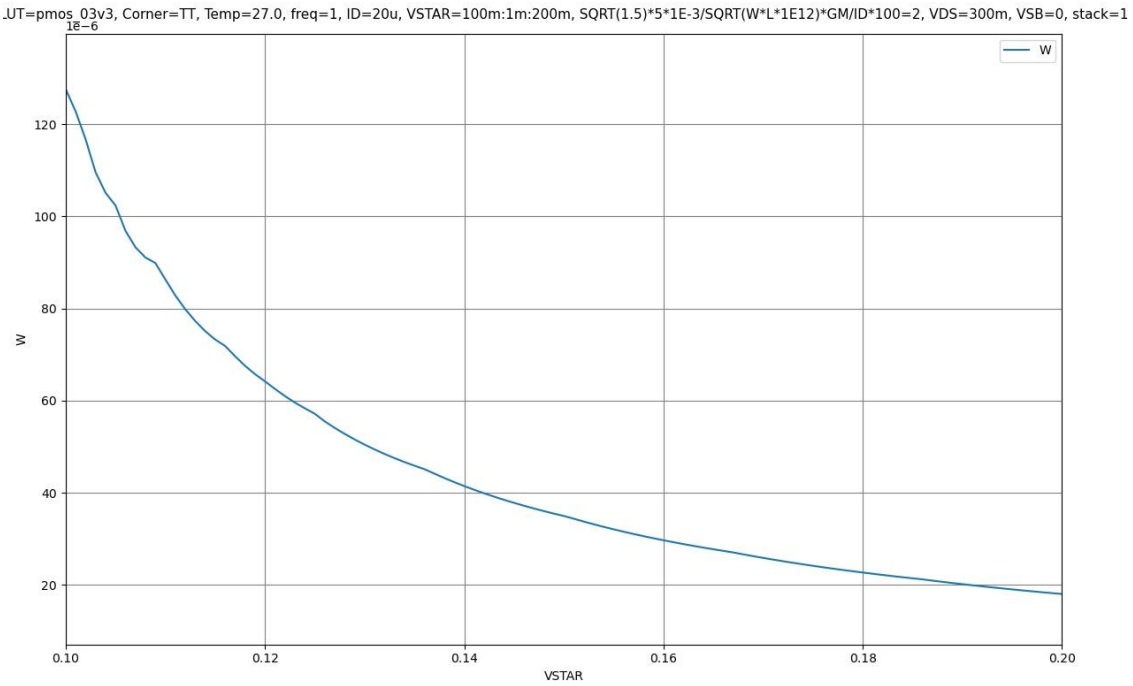

Figure 4 W vs Vstar

Smallest area can be found at the largest acceptable value for V Compliance (200mV)

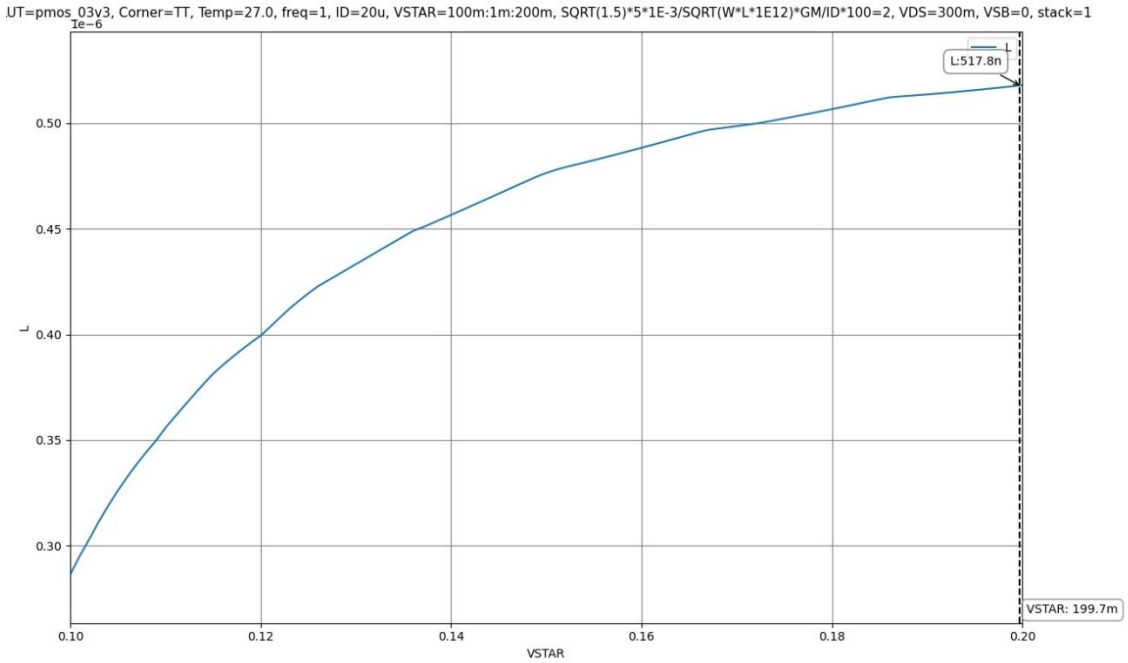

Figure 5 L at Required Vstar

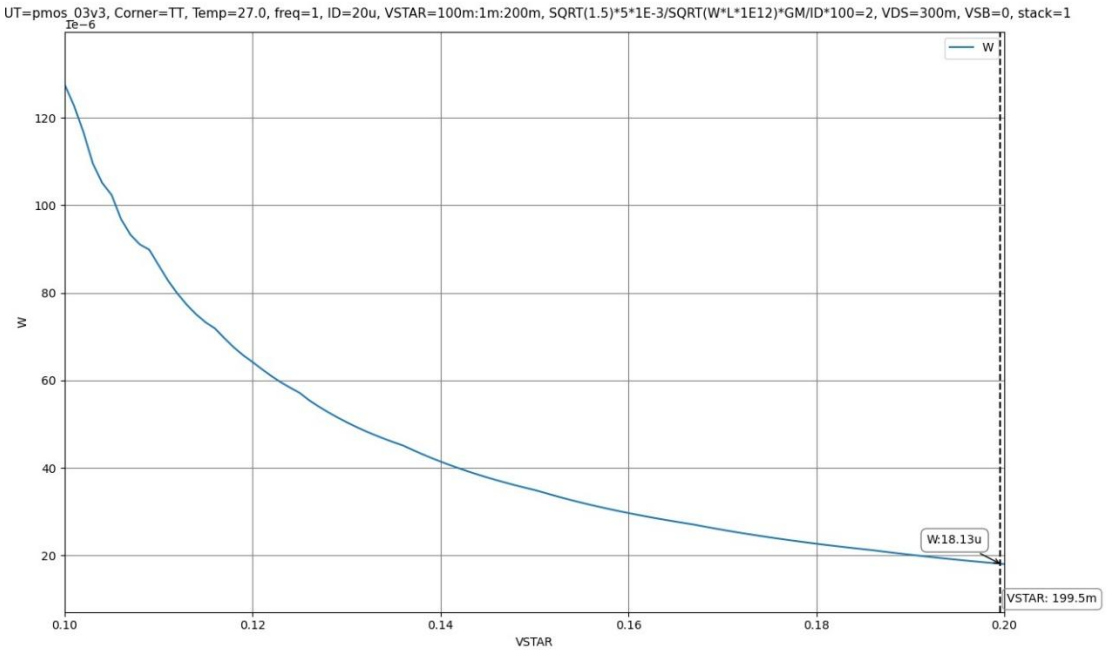

Figure 6 W at Required Vstar

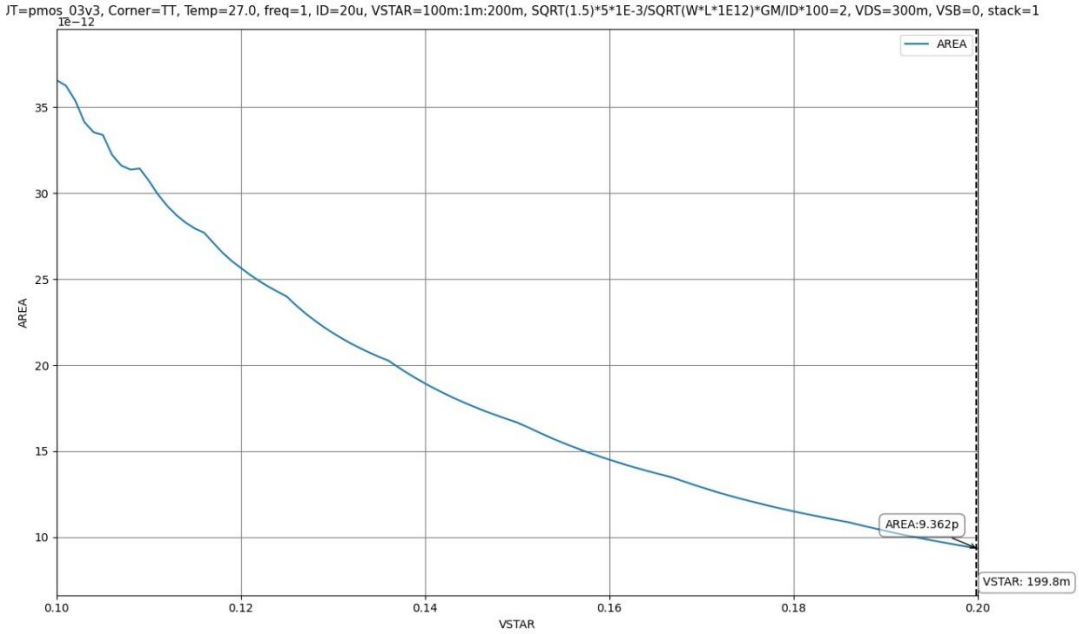

Figure 7 Area at Required Vstar

$$L = 517.8nm \quad , \quad W = 18.13\mu m$$

CM Input Level:

$$VICM_{MAX} = V_{DD} - VGS_4 - V_1^* = 0.66V$$

$$VICM_{MIN} = 0.6 - VTH_4 = -0.27V$$

The chosen VICM is a little close to the max input but has enough headroom, ideally though it should be at the average between the Max and Min

Part 2: Differential Amplifier

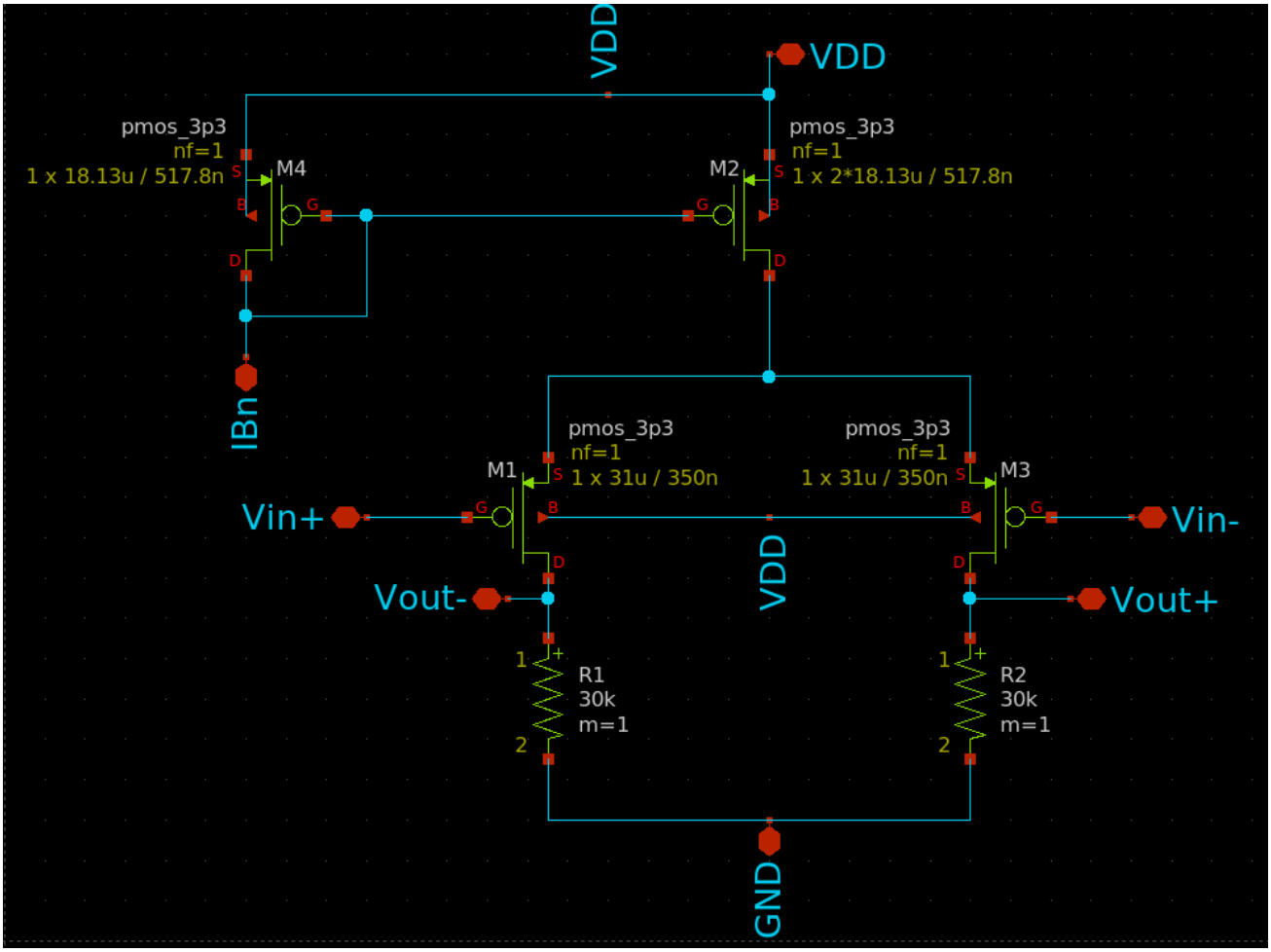

Figure 8 Differential Amplifier Schematic

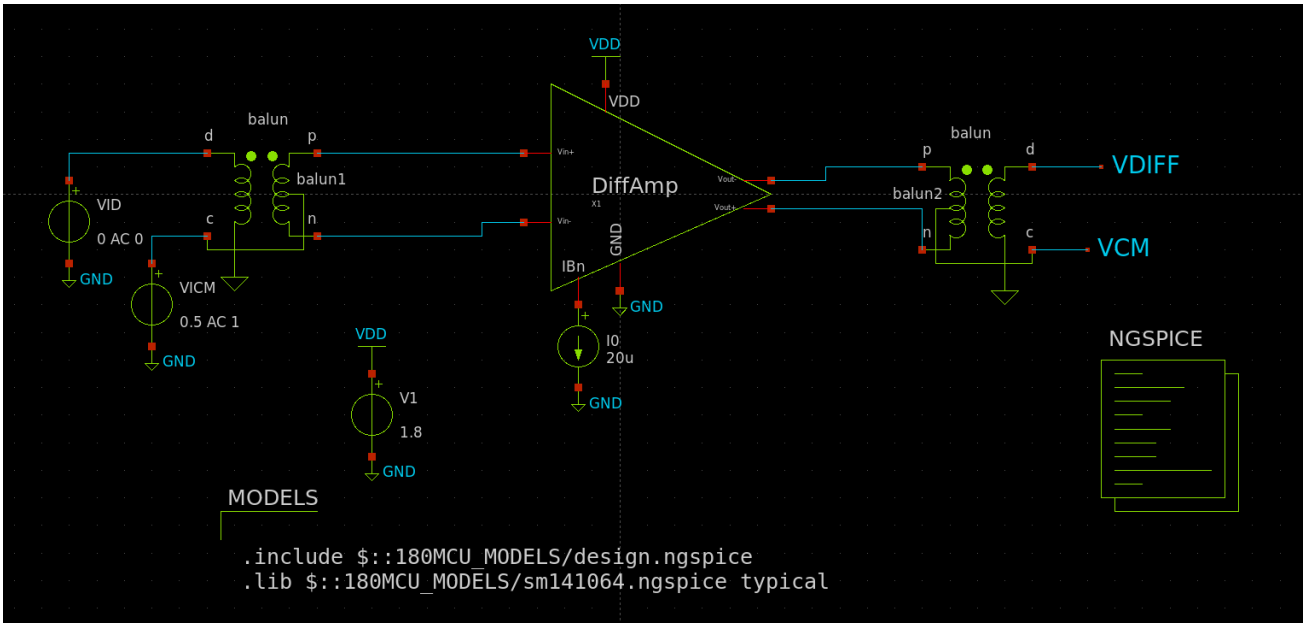

Figure 9 Testbench Schematic

OP Simulation:

```
BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x1.xm2.m0          m.x1.xm1.m0          m.x1.xm3.m0
     model           pmos_3p3.13          pmos_3p3.13          pmos_3p3.12
        id                 2e-05          3.84363e-05          1.92122e-05
        gm          0.000205671          0.000392872          0.000284521
       gds           1.0154e-06          5.81319e-06          3.09947e-06
       vgs             0.940662             0.940662             0.937446
       vth             0.790503             0.790148              0.87411
       vds             0.940661              0.30255             0.921078
     vdsat             0.165849             0.166111              0.11699

BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x1.xm4.m0
     model           pmos_3p3.12
        id           1.92241e-05
        gm          0.000284646
       gds          3.10138e-06
       vgs             0.937446
       vth             0.874068
       vds             0.920722
     vdsat             0.117017
```

Figure 10 Operating Point of All Transitors

Note: xschem doesn't have support for the region variable.
All transistors appear to be in Saturation!

Diff Small Signal CCS:

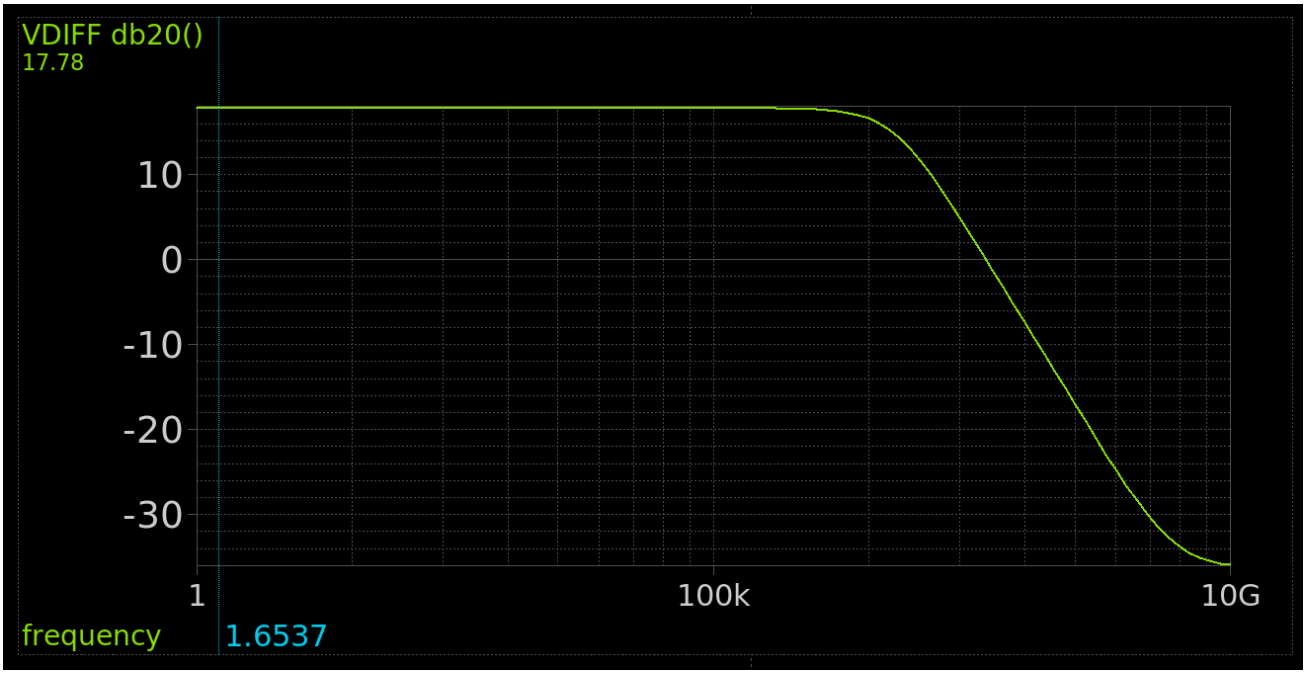

Figure 11 Bode Plot of Diff Gain

```
gain                =   7.742132e+00
bw                  =   5.669427e+06
```

Figure 12 Gain and BW from Simulation

Analytical Solution: $A_v = 0.91 gmR_D = \mathbf{7.769} \rightarrow \mathbf{17.8\ dB}$

$$BW = \frac{1}{\tau} = \frac{1}{2\pi R_D C_L} = \mathbf{5.3MHz}$$

	Analytical	Simulation
Diff Gain	7.769	7.742
Diff Gain (dB)	17.8 dB	17.78 dB
BW	5.3MHz	5.66MHz

CM Small Signal CCS:

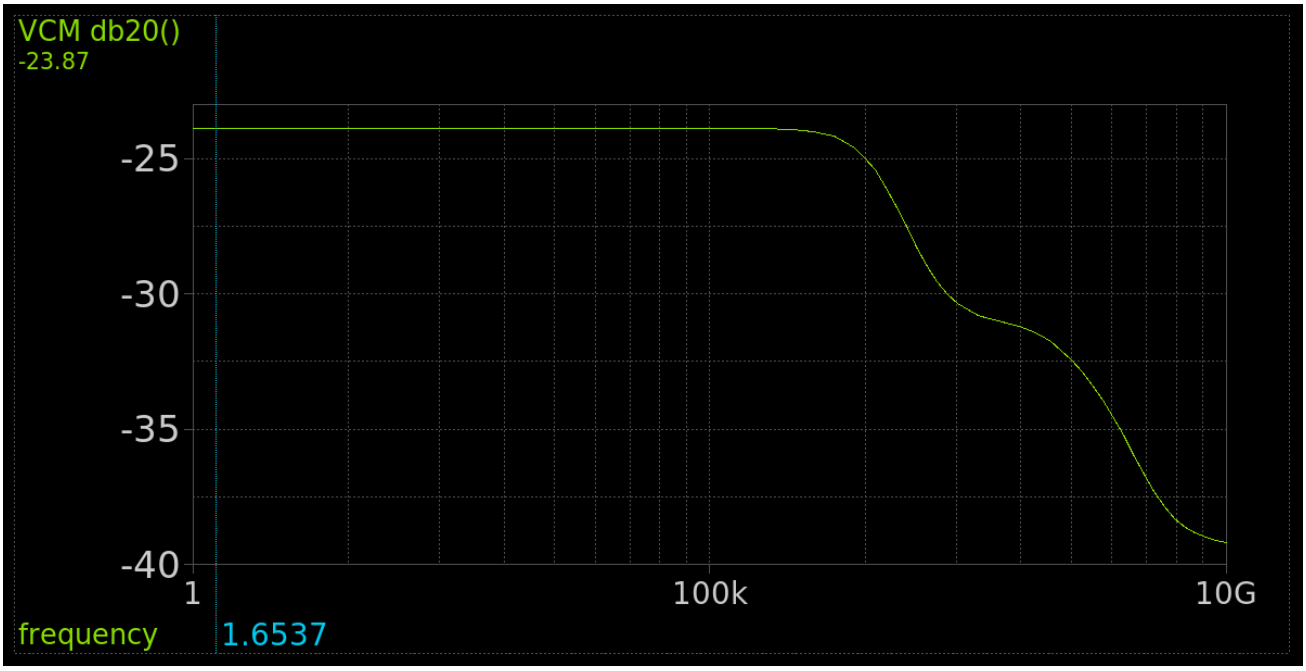

Figure 13 AvCM Bode Plot

```
cmgain              =   6.401523e-02
```

Figure 14 CM gain from Simulation

Analytical Solution:

$$A_{vCM} = \frac{gmR_D}{1 + 2(gm + gmb)R_{SS}} = 6.53 * 10^{-2}$$

	Analytical	Simulation
CM Gain	6.53e-2	6.4e-2
CM Gain (dB)	-23.69 dB	-23.87 dB

The common mode gain experiences a Pole then a Zero then another Pole at very high frequencies, the Pole caused by the high impedance node at the current source node causes it to fall till it reaches the zero also caused by the same node due to the parasitic capacitances seen at it (CP).

CMRR:

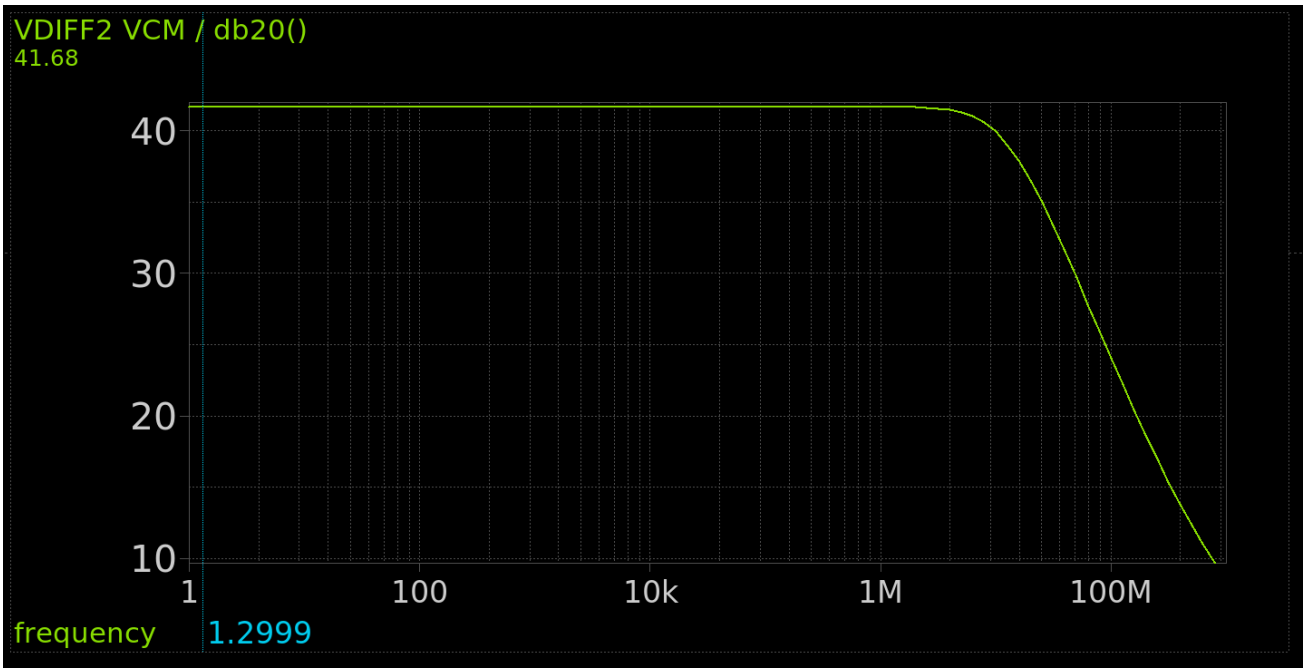

Figure 15 CMRR vs Frequency Bode Plot

```
cmgain                =  6.401523e-02
diffgain              =  7.767959e+00
cmrr_val = 1.213455e+02
```

Figure 16 CMRR Value from Simulation

Analytical Solution:

$$CMRR = 1 + 2(gm + gmbs)_{1,2}R_{SS} = \mathbf{130.5} \rightarrow \mathbf{42.27}\boldsymbol{dB}$$

	Analytical	Simulation
CMRR	130.5	42.27
CMRR	121.3	41.68 dB

At high frequencies parasitic capacitances at the RSS node cause it to short significantly decreasing CMRR as we increase frequency.

Diff Large Signal CCS:

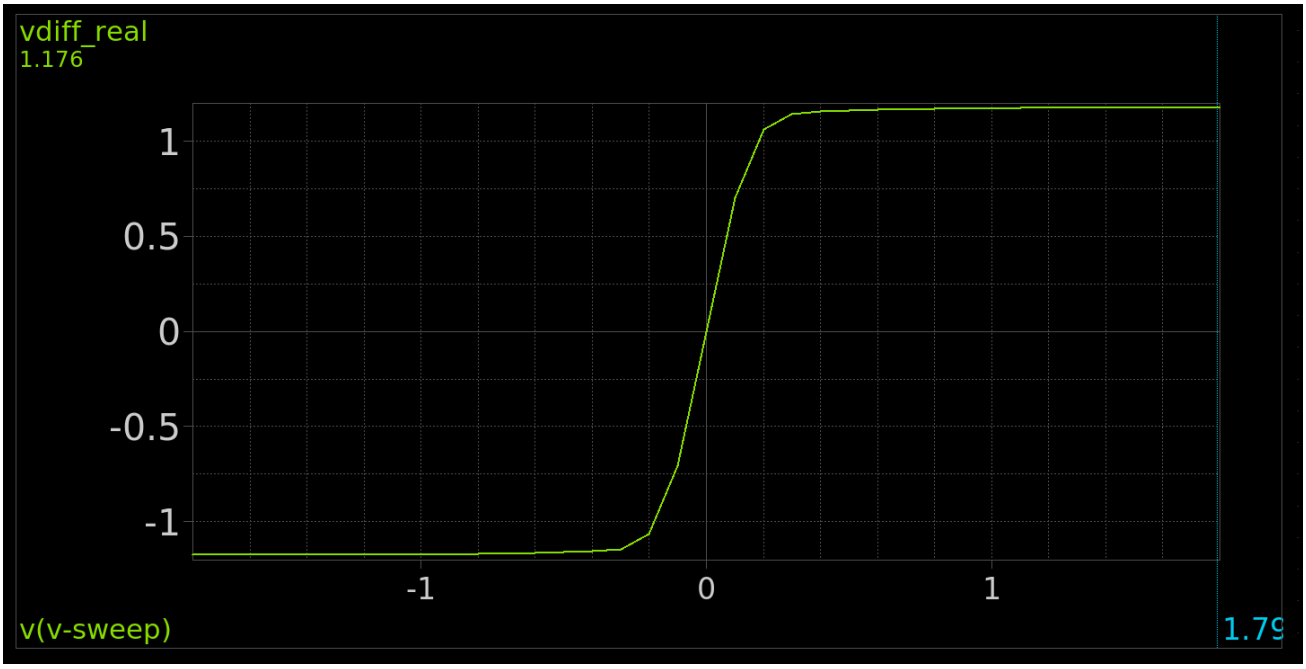

Figure 17 VODIFF vs VIDIFF

Analytical Solution:

At Extreme points current is steered completely into one of the two transistors while the other turns off thus Vodiff = Vpos only or Vneg only

$$VODIFF_{MAX} = I_D R_D = \mathbf{1.2V}$$

	Analytical	Simulation
VODIFF Extreme	1.2	1.76

The simulation result is slightly less than the Analytical result due to current mirror errors, the current steered into the transistor is slightly less than 40uA as used in the calculations resulting in slightly less voltage.

CM Large Signal CCS:

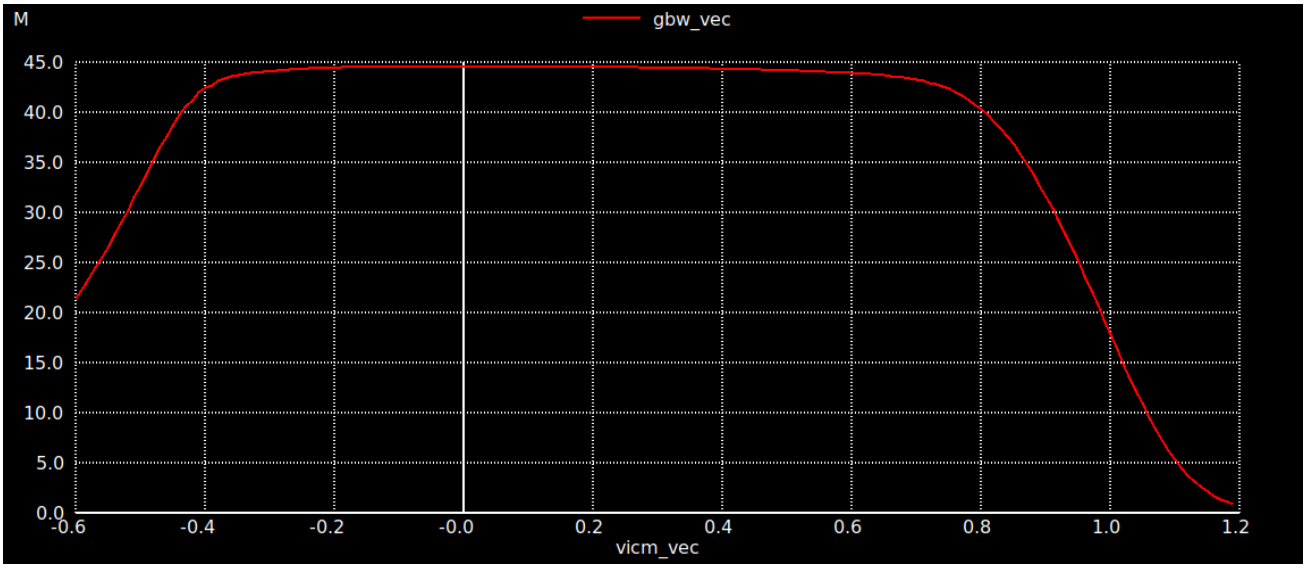

Figure 18 GBW vs VICM

```
vicmmax = 8.000000e-01
vicmmin = -4.40000e-01
```

Figure 19 VINCM Range from Simulation

Analytic Solution:

Using the same expressions derived during sizing we can find the the input range but using the results from the OP analysis

$$VICM_{MAX} = V_{DD} - VGS_4 - V_{DSAT\,1} = 0.689V$$

$$VICM_{MIN} = ID_4 * R_D - VTH_4 = -0.303V$$

	Analytical	Simulation
VINCM Minimum	-0.303	-0.44
VINCM Maximum	0.689	0.8