

**Analog IC Design – Xschem and Master Micro Tools****Lab 06****Differential Amplifier****Intended Learning Objectives**

In this lab you will:

- Design a differential amplifier circuit using the Sizing Assistant (SA).
- Learn how to simulate the small-signal differential characteristics of a differential amplifier.
- Learn how to simulate the small-signal common-mode characteristics of a differential amplifier.
- Learn how to simulate the large-signal differential characteristics of a differential amplifier.
- Learn how to simulate the large-signal common-mode characteristics of a differential amplifier.

**Part 1: Differential Amplifier Design**

- 1) We want to design a resistive loaded differential amplifier with the specifications below.

**NOTE:** that the bias current is split between two transistors; each transistor gets  $I_D = 20\mu A$ .

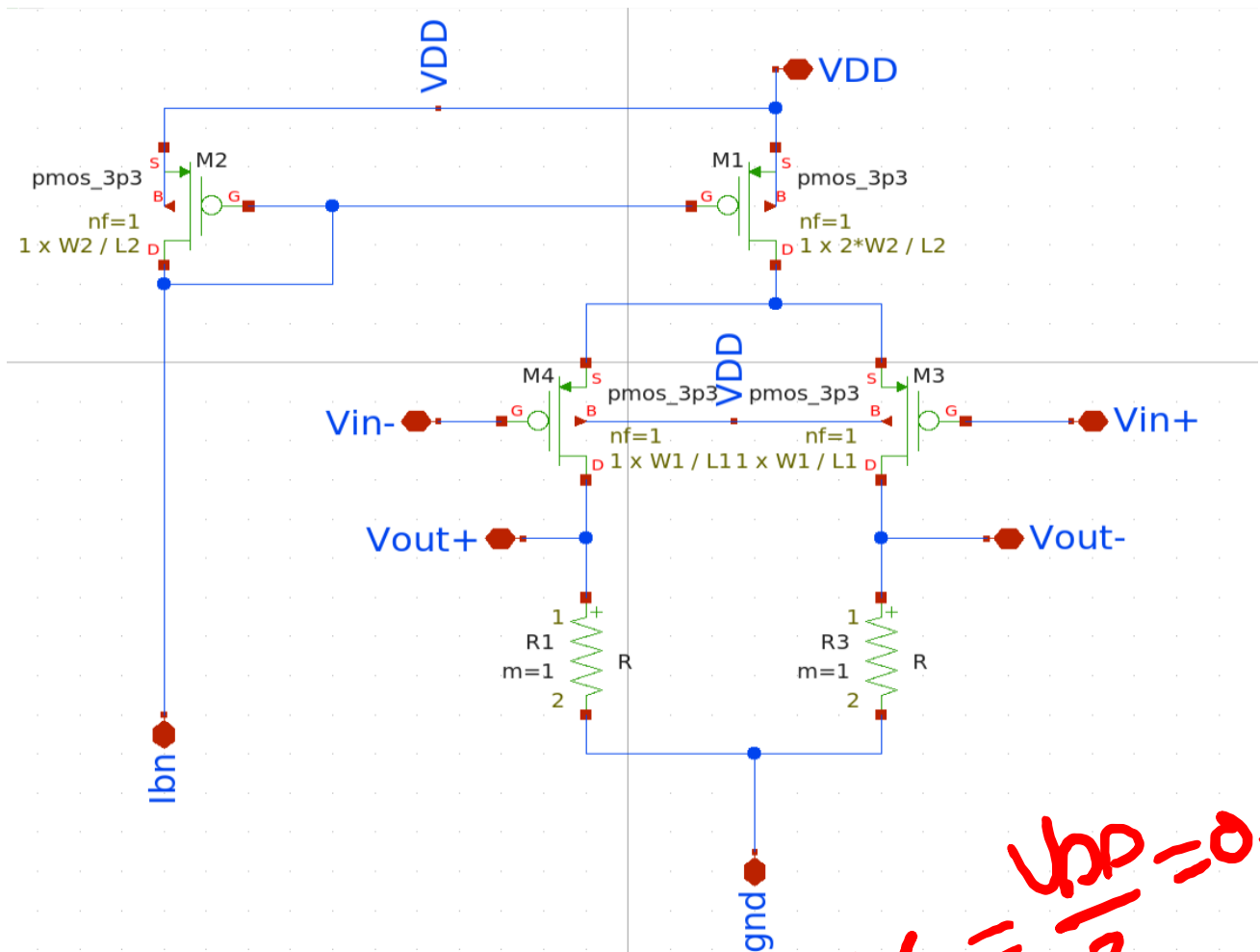
Parameter	
Supply ( $V_{DD}$ )	1.8V
Bias current ( $I_{SS}$ )	40 $\mu A$
Differential gain	8
CM output level <sup>1</sup>	$V_{DD}/3$
Load capacitance	1pF

*Spec*

- 2) Since the required output level is closer to the ground rail, we will use a PMOS input stage. Assume the PMOS will not be placed in a dedicated well to save the area -Body cannot be connected to floating source-. Assume we will use a simple current mirror for biasing. The design schematic is shown below.

→ Xschem Hint: You can add labels (names) to nets (wires) using the hotkey "Alt+l" and create ports using the hotkey "shift + l → devices → iopin".

<sup>1</sup> The supply voltage is divided between the tail current source, the input stage, and the resistive load. The tail current source needs a good voltage drop ( $V_{DS}$ ) for higher output resistance and good CMRR. The input stage needs a good voltage drop ( $V_{DS}$ ) for higher output resistance and to allow good signal swing. The resistive load needs a good voltage drop to allow a good swing and to give higher gain. Note that  $I_{SS}R_D = 2V_{out-CM}$  must be smaller than  $(V_{DD} - V_{dsat-tail})$  for proper large signal characteristics (why?).



- ✓ 3) Choose  $R_D$  to meet the CM output level spec.  $\rightarrow V_{RD} = \frac{V_{DD}}{3} = 0.6V$
- 4) The differential amplifier gain is given by  $|A_v| \approx g_m(R_D || r_o)$
- ✓ 5) We will choose  $L$  to set  $r_o \gg R_D \rightarrow r_o = 10 \times R_D$
- ✓ 6) Choose  $V^*$  to meet the differential gain spec.  $|A_v| \approx 0.91 \times g_m R_D = 0.91 \times \frac{2I_D}{V^*} \times R_D = \frac{1.82V_{RD}}{V^*} \rightarrow R_D = 30k$
- ✓ 7) Assume we will set  $V_{DS}$  of the tail current source to  $300mV$  to allow more output swing. Report the input pair sizing using SA.  $V^* = \frac{1.82V_{RD}}{|A_v|} \rightarrow = 136m$

✓

ID	20u	?
Vstar	136m	?
ro	30*10k	?
VDS	0.9	?
VSB	0.3	?

0.6V

- 8) Given the above assumption for  $V_{DS}$  of the tail current source, **calculate** the required CM input level.
- 9) The tail current source has the following specifications:

Parameter	
Input current	$20\mu A$
Percent mismatch: $\sigma(I_{out})/I_{out}$	$\leq 2\%$
Compliance voltage	$\leq 200mV$
Area	Minimize

- 10) Use SA to plot the sizing at a constant  $\sigma(I_{out})/I_{out}$ .

$$\frac{\sigma(I_{out})}{I_{out}} = \frac{\sqrt{1 + \frac{1}{m}} \times \frac{A_{VT}}{\sqrt{WL}} \times mg_m}{mI_D} \times 100$$

Where  $m$  is the mirroring ratio,  $A_{VT} = 5mV \cdot \mu m$  is Pelgrom's coefficient, and the  $\sqrt{1 + \frac{1}{m}}$  factor is due to taking the difference between two random variables ( $V_{TH}$  of the two current mirror transistors).

From VM were open ADT

1. Open a terminal in the directory: "/home/tare/ADT\_Working\_Directory"
  2. Run the command: "./start\_adt.sh"
- Load LUTs files (file - load LUT - open nmos\_3p3).
  - Open Sizing Assistant and set the parameters as shown below.
  - to plot the sizing at a constant  $\sigma$

$$\text{sqrt}(1.5) * 5 * 1E-3 / \text{sqrt}(W * L * 1E12) * gm / ID * 100$$

LUT settings

LUT: pmos\_03v3

Corner: TT

Temp (°C): 27.0

Frequency: 1

Stack: 1

ID: 20u

Vstar: 100m:1m:200m

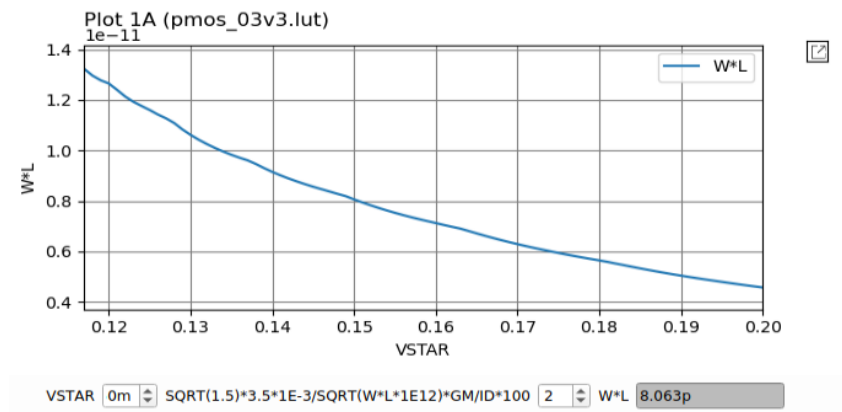
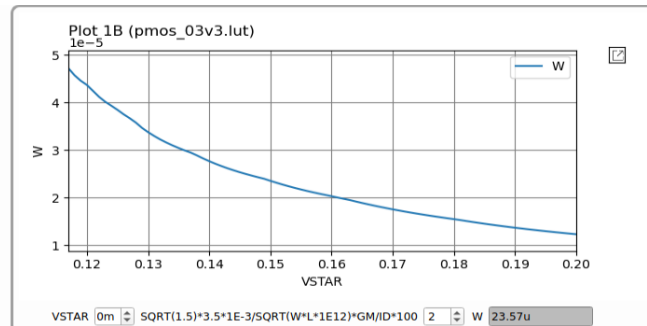
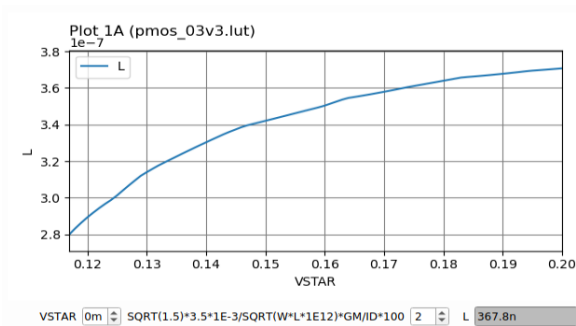
/ID\*100: 2

VDS: 0.3

VSB: 0

ADT S.S

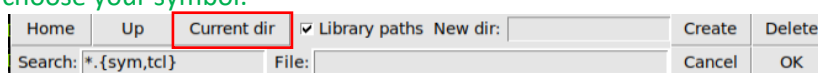
- ADT Hint: If the LUT contains mismatch data, we can directly use the parameter idmis in SA to get the standard deviation of the current random variations ' $\text{idmis}_{\%} = \text{sqrt}(1.5) * \text{idmis} / ID * 100$ '. The mismatch data can be added to any LUT using ADT by using an appropriate Monte Carlo mismatch model file.

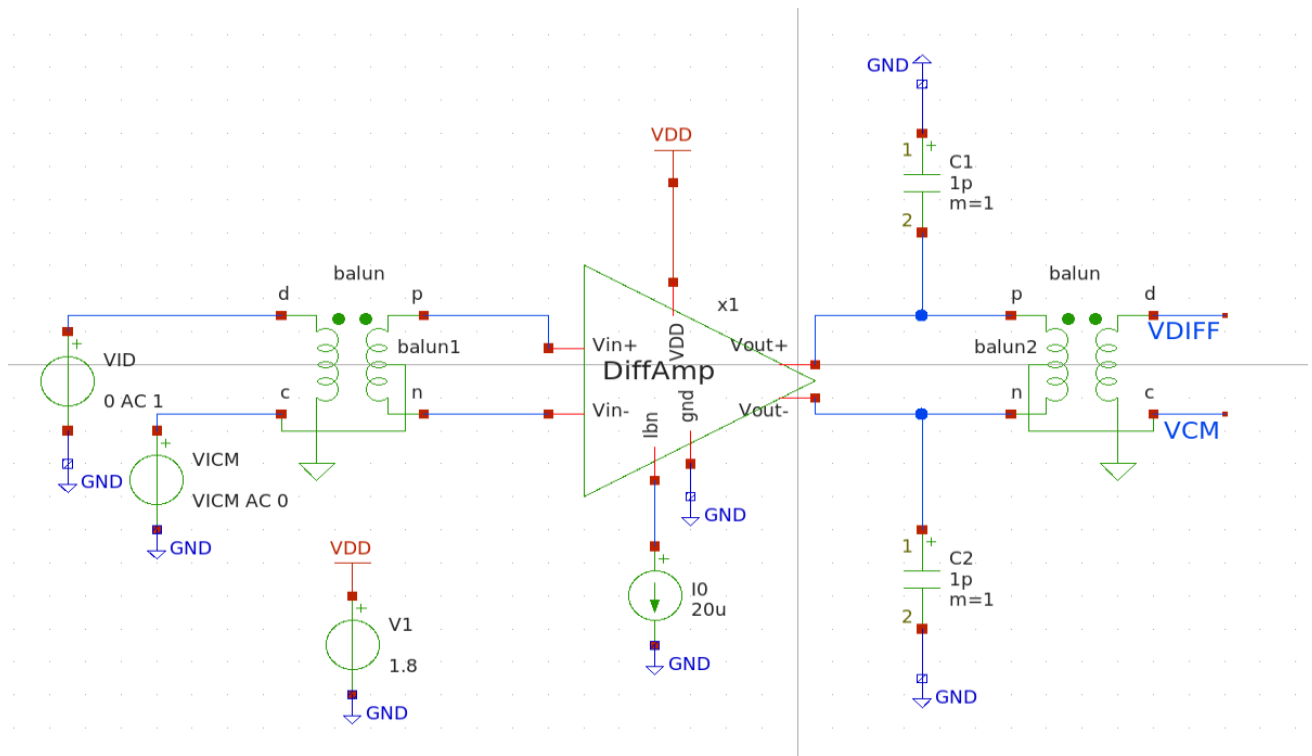


- 11) As seen in the plot above, for a given mismatch requirement, the minimum area is achieved at the max  $V^*$ . Similarly, for a given area requirement, the minimum mismatch is achieved at the max  $V^*$ . That's why current mirrors are commonly biased in strong inversion.
- 12) The plot also shows that at a given  $V^*$  (compliance voltage), going for lower mismatch necessitates longer  $L$ , which also gives lower  $\lambda$  (higher  $r_o$ , although the effect of  $L$  on  $\lambda$  is limited at low  $V_{DS}$ ). However, this comes at the expense of area.
- 13) Given the compliance voltage spec, **report** the above figure with a cursor added to the selected design point.
- 14) **Calculate** the min and max CM input levels. Is the previously selected CM input level in the valid range?

## Part 2: Differential Amplifier Simulation

- 1) Create the schematic of a differential amplifier "lab\_06\_diff\_amp".
- 2) Create a symbol for the diff pair. Edit the symbol to look as shown below in the testbench schematic.
  - ➔ Xschem Hint: We will put the circuit under test in a schematic, create a symbol using hot key "A", then create a new schematic for the testbench.
  - ➔ Xschem Hint: To edit the symbol shape press file open then press current dir then choose your symbol -note you should choose <name>.sym to edit symbol-.
- 3) Create a new cell for the testbench "lab\_06\_diff\_amp\_tb". Create the testbench schematic as shown below.
  - ➔ Xschem Hint: To Place your symbol into the testbench use "Shift + I" then press current dir then choose your symbol.





→ Xschem Hint: To add Balun:

1- download the following 3 files into your machine into the same folder as your schematic.

<https://drive.google.com/drive/folders/1CeNCPqHtC3S5WrG-pIEf9yIG7et6GVgo?usp=sharing>

2- Press "Shift + I" → current dir → balun.sym

3- Set the transistor sizing and Vicm as designed in Part 1. Unless otherwise stated, set Vid = 0 (this is the large signal differential input voltage).

**NOTE:** Use IB = 20uA (the CM multiplies this by 2, so each half in the diff pair gets IB).

## Report the following:

1) OP simulation.

```
.control
save all
op
show m : id : gm : gds : vgs : vth : vds : vdsat
.endc
```

• Report a snapshot clearly showing the following parameters.

ID
VGS
VDS
VTH
VDSAT
GM
GDS
GMB
Region

- ✓ Check that all transistors operate in saturation.

2) Diff small signal ccs:

- ✓ Use AC magnitude = 1 for the diff source (and AC magnitude = 0 for the CM source).
- ✓ Run AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).
- ✓ Report the Bode plot of small signal diff gain.
- ✓ Compare the DC diff gain and BW with hand analysis in a table.

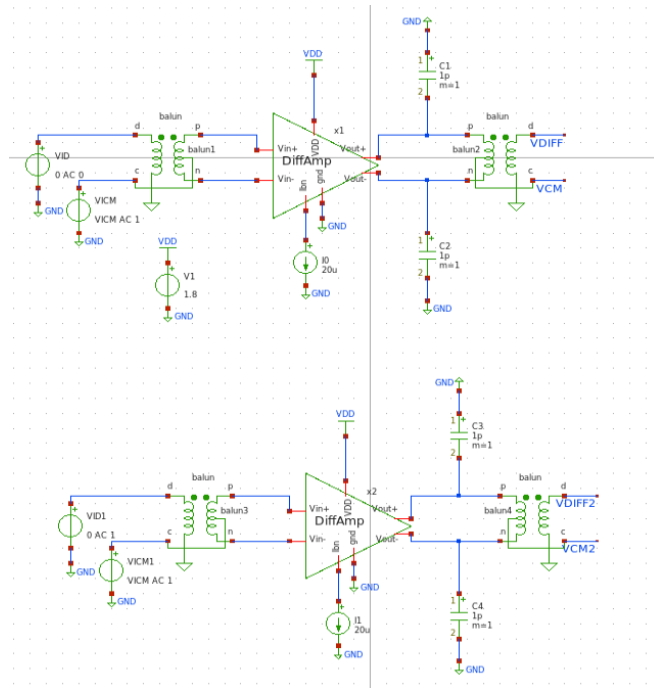
```
.control
save all
op
ac dec 10 1 10G
meas ac Gain MAX vmag(VDIFF) FROM=1 TO=10G
let ff2=Gain*0.707
meas ac BW WHEN vmag(VDIFF)=ff2 FALL =1
save v(VDIFF)
remzerovec
write lab6_ac.raw
.endc
```

3) CM small signal ccs:

- ✓ Use AC magnitude = 1 for the CM source (and AC magnitude = 0 for the diff source).
- Run AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).

```
.control
save all
op
ac dec 10 1 10G
meas ac CMGain MAX vmag(VCM) FROM=1 TO=1k
remzerovec
write lab6_ac.raw
.endc
```

- ✓ Report the Bode plot of small signal CM gain.
- ✓ Compare the DC CM gain with hand analysis in a table. Is it smaller than "1"? Why?
- ✓ Justify the variation of  $A_{vcm}$  vs frequency.
- ✓ Plot  $A_{vd}/A_{vcm}$  in dB. Compare  $A_{vd}/A_{vcm}$  @ DC with hand analysis in a table.



```
.control
save all
op
ac dec 10 1 1G
meas ac CMGain MAX vmag(VCM) FROM=1
TO=1MEG
meas ac DiffGain MAX vmag(VDIFF2) FROM=1
TO=1MEG
let CMRR_val = DiffGain / CMGain
print CMRR_val
let CMRR = v(VDIFF2) / v(VCM)
save CMRR
remzerovec
write lab6_ac_CM.raw
.endc
```

➔ Xschem Hint: To calculate CMRR we will use two duplicate of the design one with Diff in and the other with CM input.

- Justify the variation of  $A_{vd}/A_{vcm}$  with frequency.

**CMRR is proportional to RSS and RSS decreases with frequency due to  $C_p$**

4) Diff large signal ccs:

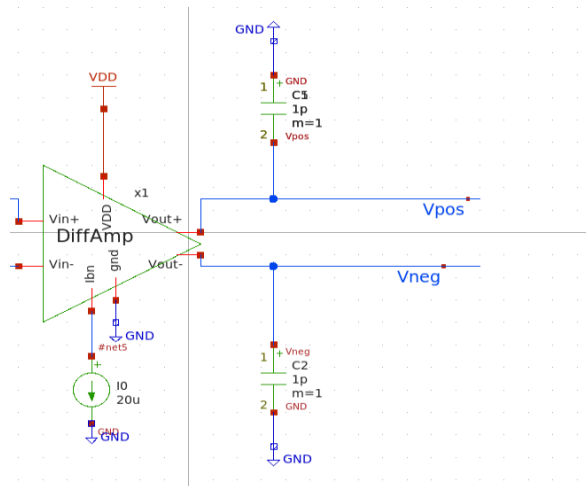
- Use dc sweep (not parametric sweep) for  $V_{id} = -V_{DD}:10m:V_{DD}$ .

```

.control
save all
dc VID -1.8 1.8 0.1
let VDIFF_real= Vpos - Vneg
save VDIFF_real
plot VDIFF_real
remzerovec
write lab6_ID.raw
.endc

```

→ Xschem Hint: in the following parts we need to remove the output Balun and rename the output nodes.



✓ Report diff large signal ccs (VODIFF vs VIDIFF). Compare the extreme values with hand analysis in a table.



5) CM large signal ccs (GBW vs Vicm):

```
.control
let Vstart=0 -
let Vstop=1.8 -
let Vstep=10m -
let Vact=Vstart -
let VICMmax=0 -
let VICMmin=0 -
save all ✓
while Vact le Vstop
  alter VICM Vact ✓
  ac dec 10 1 100G → sim diff output
  let vx = Vpos - Vneg
  meas ac DiffGain MAX vx FROM=1 TO=100MEG
  let ff1=DiffGain*0.707
  meas ac f3db WHEN vx = ff1 FALL =1 → 3db
  let GBW = DiffGain*f3db → GBW
  save GBW ✓
  let vx = Vact
  let VICMact = Vact + VICM
  save VICMact
  set appendwrite
  remzerovec
  write Lab6_param.raw

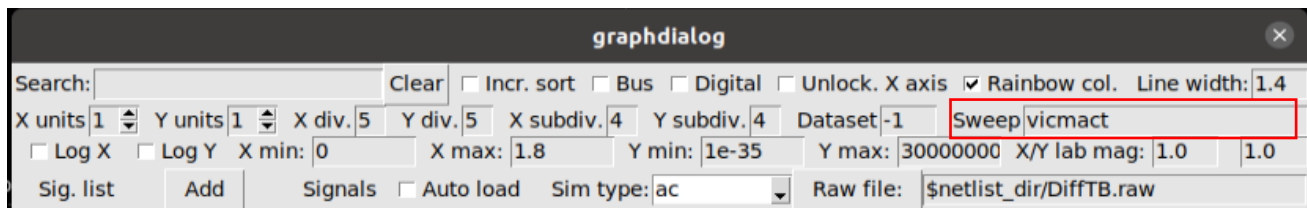
  if (GBW > 27MEG)
    let VICMmax = Vact
  endif

  if (GBW < 27MEG)
    if (Vact<0.5)
      let VICMmin = Vact
    endif
  endif

  let Vact=Vact+Vstep
end
print VICMmax
print VICMmin
.endc
```

- ✓ We will use parametric sweep on AC analysis to get GBW.
- ✓ Report CM large signal ccs (GBW vs VICM). Assume the valid range for Vicm (CMIR) is defined by the condition that Avd is within 90% of the max gain, i.e., 10% drop in gain.
- Find the CM input range (CMIR). Compare with hand analysis in a table.

- Xschem Hint: To plot gbw vs VICMact write in sweep VICMact. Note that you can plot vs Vx both stores VICM values.



## Lab Summary

- In Part 1 you learned:
  - How to design a resistive-loaded differential amplifier.
- In Part 2 you learned:
  - How to use an ideal balun to test a differential amplifier.
  - How to simulate the small-signal differential gain of a differential amplifier.
  - How to simulate the small-signal common-mode gain of a differential amplifier.
  - How to simulate the large-signal differential characteristics of a differential amplifier.
  - How to simulate the large-signal common-mode characteristics of a differential amplifier.

## Acknowledgements

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