Lab 1

RC Filter and MOSFET Characteristics

(NGSpice, XSchem & ADT)

Part 1: RC Filter

$$\tau = R * C = 1ns \qquad C = \frac{1ns}{1K\Omega} = \mathbf{1pF}$$

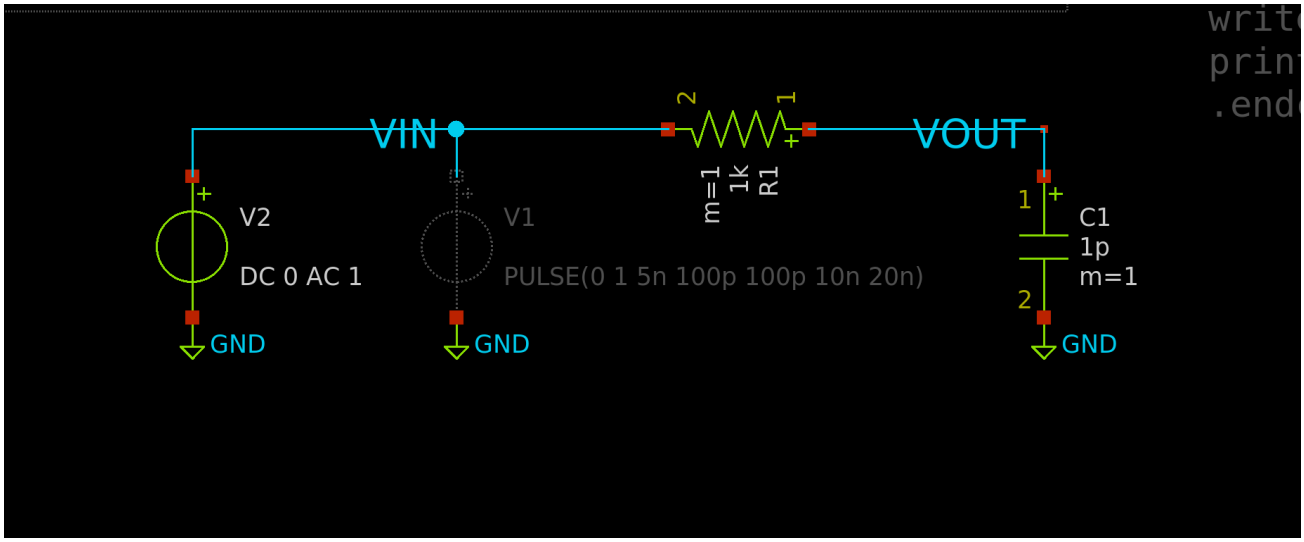

Figure 1 RC Filter Schematic Testbench

1. Transient Analysis:

```
Transient Simulation

 .control
 tran 100p 40n
 save all
 meas tran t_rise TRIG v(vout) VAL=0.1 RISE=1 TARG v(vout) VAL=0.9 RISE=1
 meas tran t_fall TRIG v(vout) VAL=0.9 FALL=1 TARG v(vout) VAL=0.1 FALL=1
 write rc_ckt.raw
 print t_rise t_fall >> tran.txt
 .endc
```

Figure 2 Output Setup

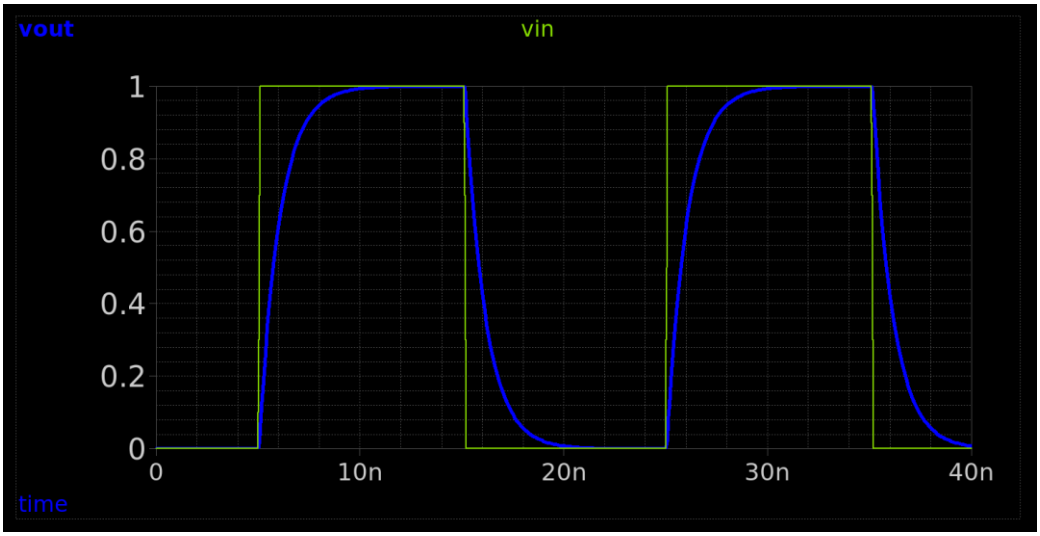

Figure 3 Two Periods of the Filter

```
t_rise                =   2.195534e-09
t_fall                =   2.196488e-09
```

Figure 4 Rise and Fall Time simulation Results

Analytic Calculation for Rise and Fall Time:

Charging: $V(t) = V_0\left(1 - e^{\frac{-t}{RC}}\right)$ $\quad\quad$ $\mathbf{V_0 = 1V}$

Discharging: $V(t) = V_0 . e^{\frac{-t}{RC}}$ $\quad\quad$ $\mathbf{V_0 = 1V}$

$$At\ V(t_1) = 0.1 \cdot V0 \Rightarrow t1 = -RC \cdot \ln(0.9) \qquad At\ V(t_2) = 0.9 \cdot V0 \Rightarrow t2 = -RC \cdot \ln(0.1)$$

$$t_{rise} = t_2 - t_1 \approx 2.2 \cdot RC \qquad t_{rise} \approx t_{fall} \approx 2.2 \cdot RC = \mathbf{2.2ns}$$

1.1 Rise and Fall Time Comparison:

Test	Output	Simulation	Analytic
ITI_Analog:Lab1_RC:1	Fall Time	2.196E-09	2.2e-09
ITI_Analog:Lab1_RC:1	Rise Time	2.1955E-09	2.2e-09

1.2 Parametric Sweep:

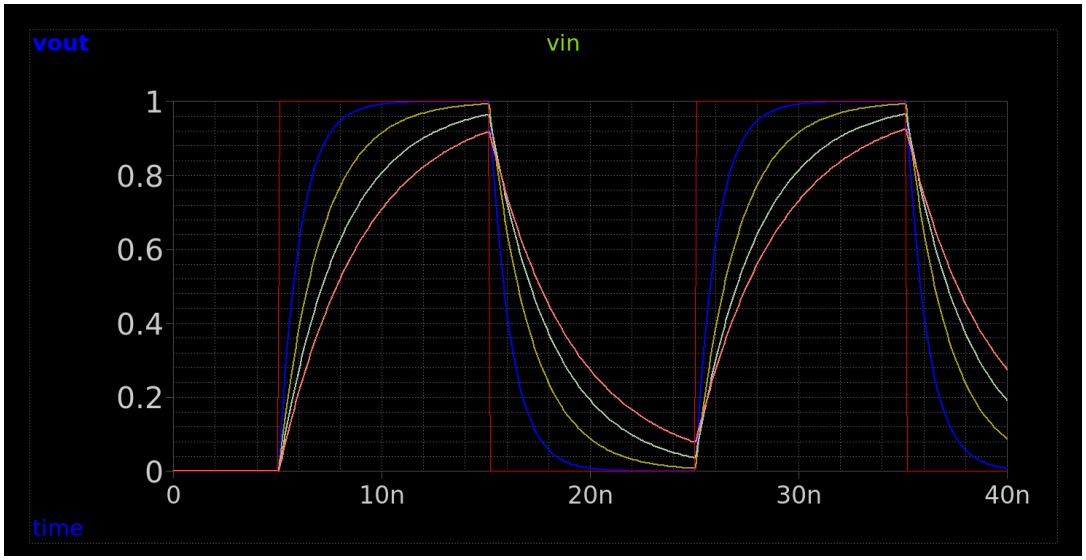

Figure 5 R Parametric Sweep

Comment: Increasing the R increases the time constant thus increasing the rise and fall time, making the square wave less pronounced as R increases and the rise and fall times increase.

2. AC Analysis:

AC Sim Code

```
.control
ac dec 10 1 10G
save all
meas ac MAX_GAIN MAX vmag(vout) from=1 to=10G
meas ac BW when vmag(vout)=0.707 fall = 1
write rc_ckt_ac.raw
set appendwrite
touch ac_results.txt
print MAX_GAIN BW > ac_results.txt
.endc
```

Figure 6 AC Simulation Code

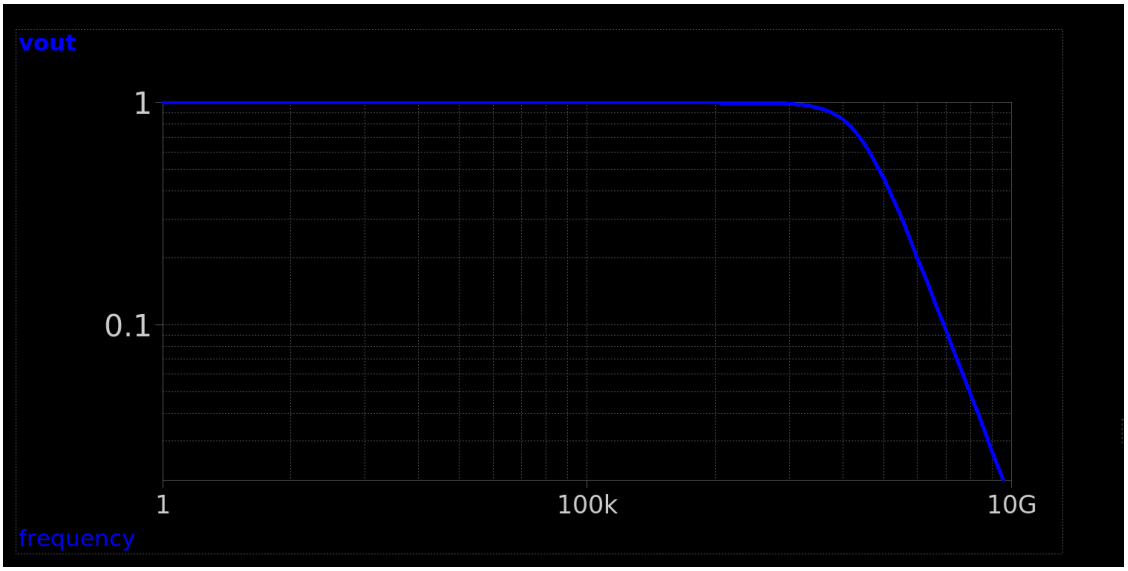

Figure 7 RC Filter Bode Plot (Mag)

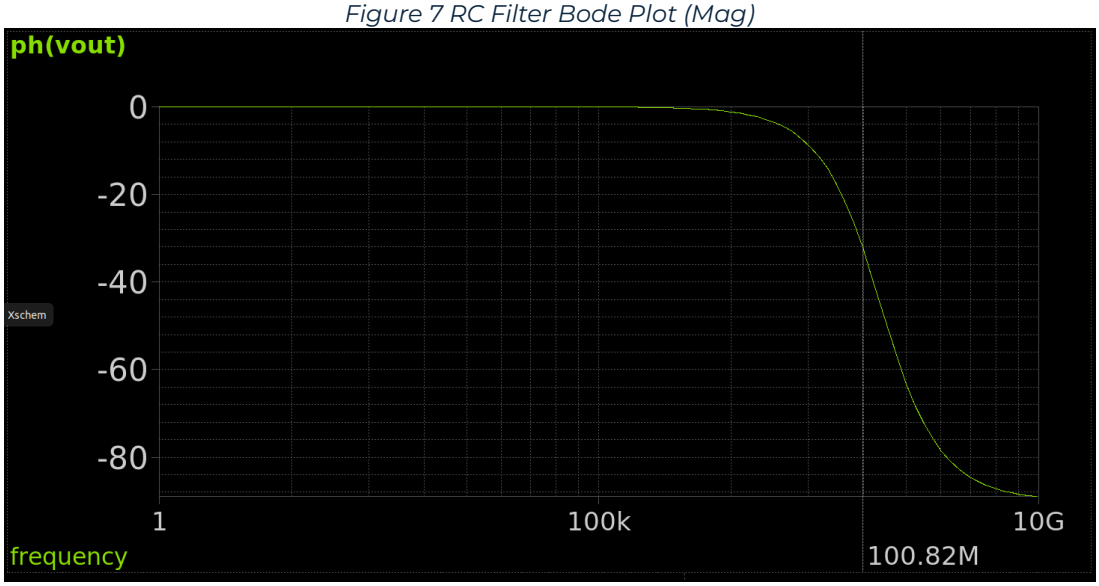

Figure 8 RC Filter Bode Plot (Phase in Degree)

```
max_gain                =   1.000000e+00
bw                      =   1.592554e+08
```

Figure 9 Max gain and BW from Simulation

Analytic Calculation for DC gain and BW:

DC Gain = 1 Cap is O.C in DC, VIN = VOUT

Bandwidth: $\omega_p = \frac{1}{RC}$ $f_p = \frac{1}{2\pi \times RC} \approx 159.155MHz$Type equation here.

Test	Output	Simulation	Analytic
ITI_Analog:Lab1_RC:1	Bandwidth	159.255MHz	159.155MHz
ITI_Analog:Lab1_RC:1	Gain	1	1

Parametric Sweep for R = 1, 10, 100, 1000KΩ

Parametric AC Sim Code

```
.control

save all

let R_val = 1k
let R_stop = 1meg
let R_mult = 10

while R_val le R_stop
alter R1 R_val
ac dec 10 1 10g

meas ac MAX_GAIN MAX vmag(vout) FROM=1 TO=10G
meas ac BW WHEN vmag(vout)=0.707 FALL=1

print MAX_GAIN BW >> ac_result.txt
write rc_ckt_2.raw
set appendwrite
let R_val = R_val * R_mult
end

.endc
```

Figure 10 Parametric AC Sweep Code

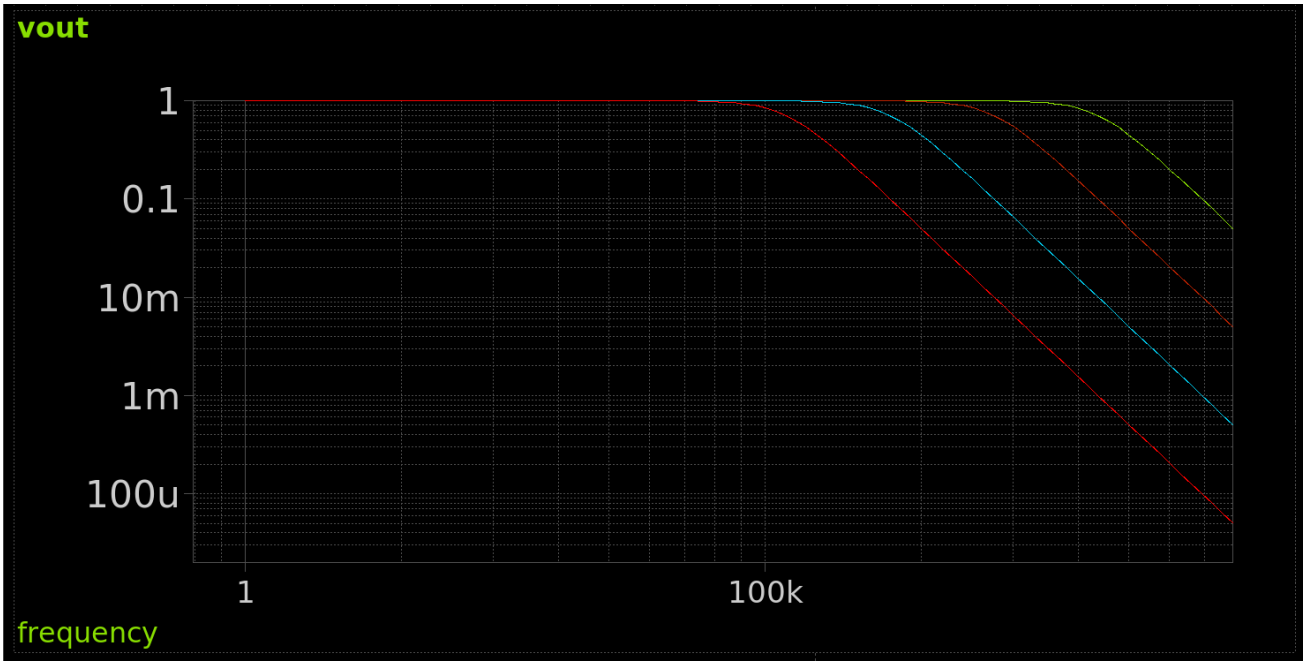

Figure 11 Parametric AC Sweep Bode Plot (Mag)

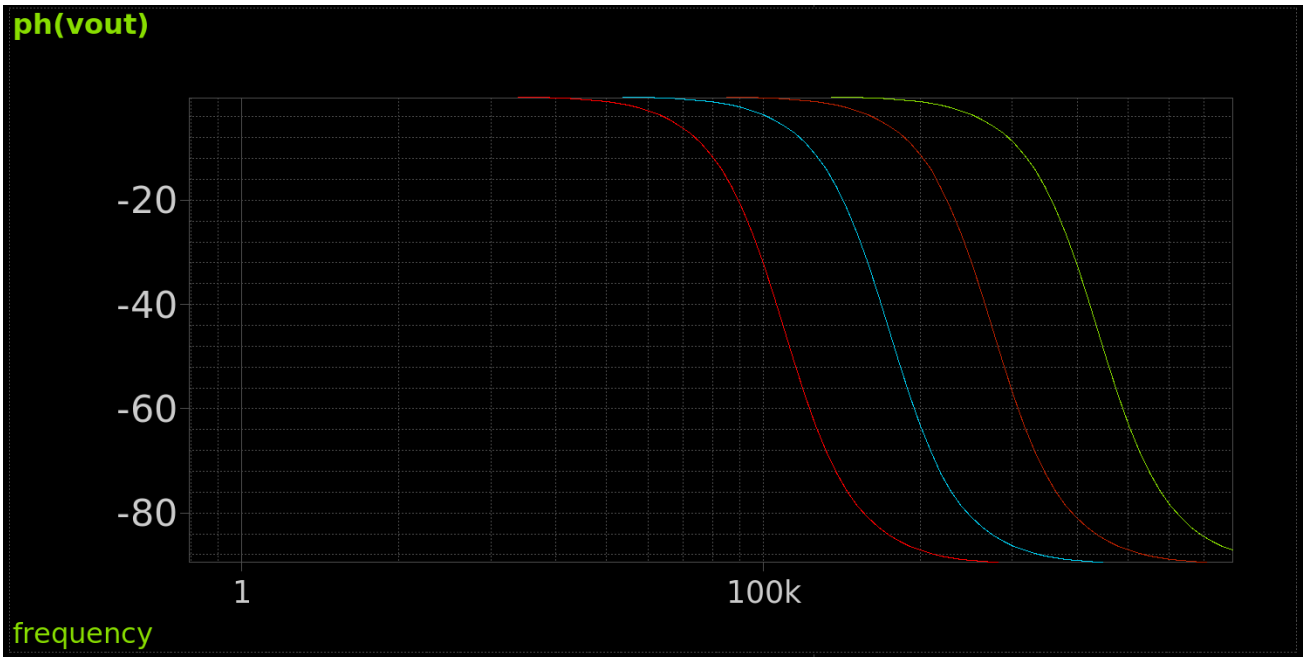

Figure 12 Parametric AC Sweep Bode Plot (Phae in Degrees)

Comment: Increasing The Resistance gradually increases the Time Constant this lowering the 3dB cut off frequency decreasing the bandwidth and causing a noticeable shift for both Bode Plot graphs.

DC gain is not affected though as it does not depend on the Time Constant rather on the circuit itself.

Part 2: MOSFET Characteristics

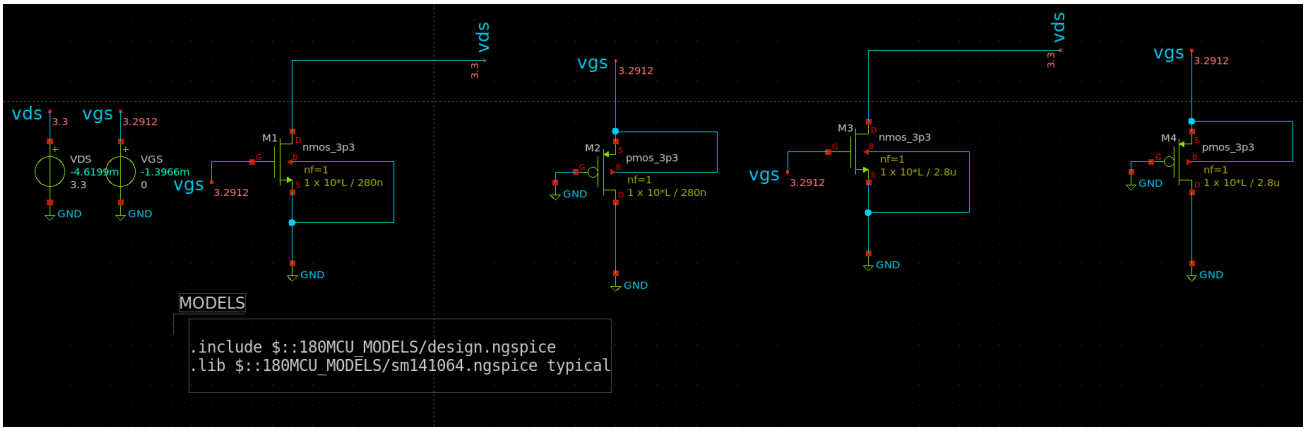

Figure 13 MOSFET Characteristics Schematic Testbench on XSchem

Using **VDD = 3.3v,** Short-Channel: **W/L = 10*2802/280n,** Long-Channel: **W/L = 10*2.8u/2.8u**

The schematic was set this way to allow for sweeping VGS and get correct results for NMOS and PMOS at the same time

DC Sim Code

```
.control

save all
+ @m.xm1.m0[id] @m.xm1.m0[gm]
+ @m.xm2.m0[id] @m.xm2.m0[gm]
+ @m.xm3.m0[id] @m.xm3.m0[gm]
+ @m.xm4.m0[id] @m.xm4.m0[gm]
dc vgs 0 3.3 1m
*dc vd 0 2 0.01 vg 0 2 0.2
write test_mos.raw

.endc
```

Figure 14 DC Sim Code in XSchem

1. ID vs VGS

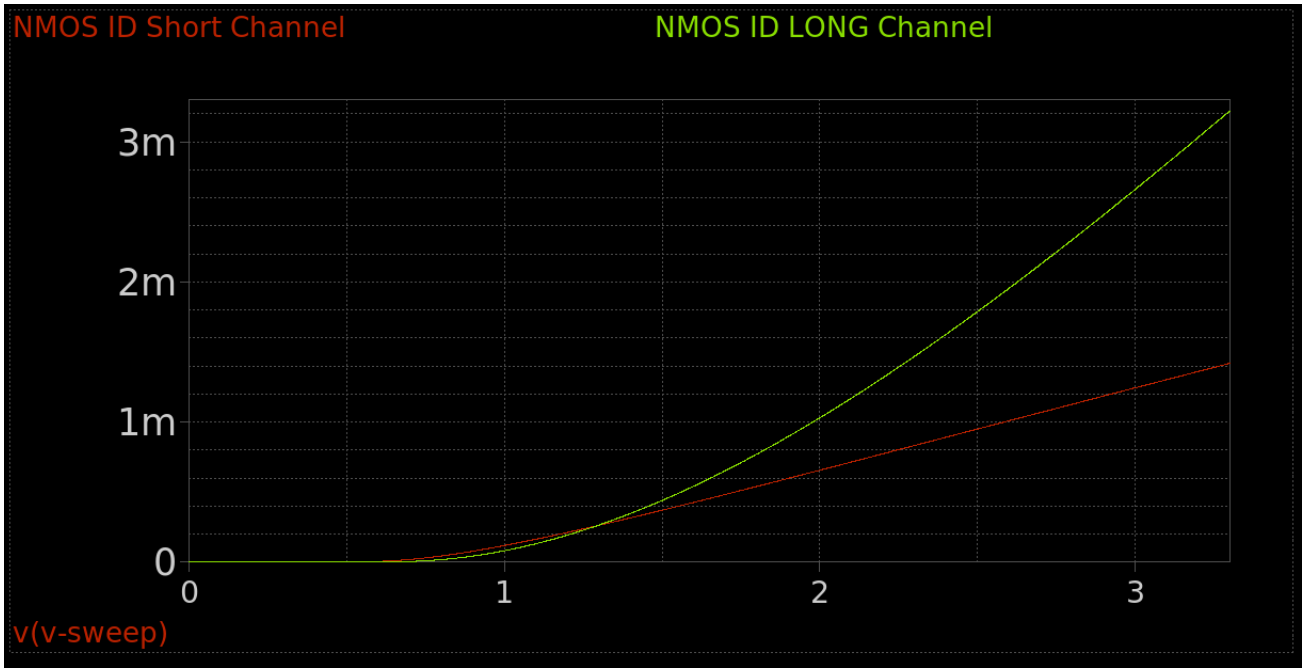

Figure 15 NMOS ID vs VGS, Green: Long-Channel, Red: Short-Channel

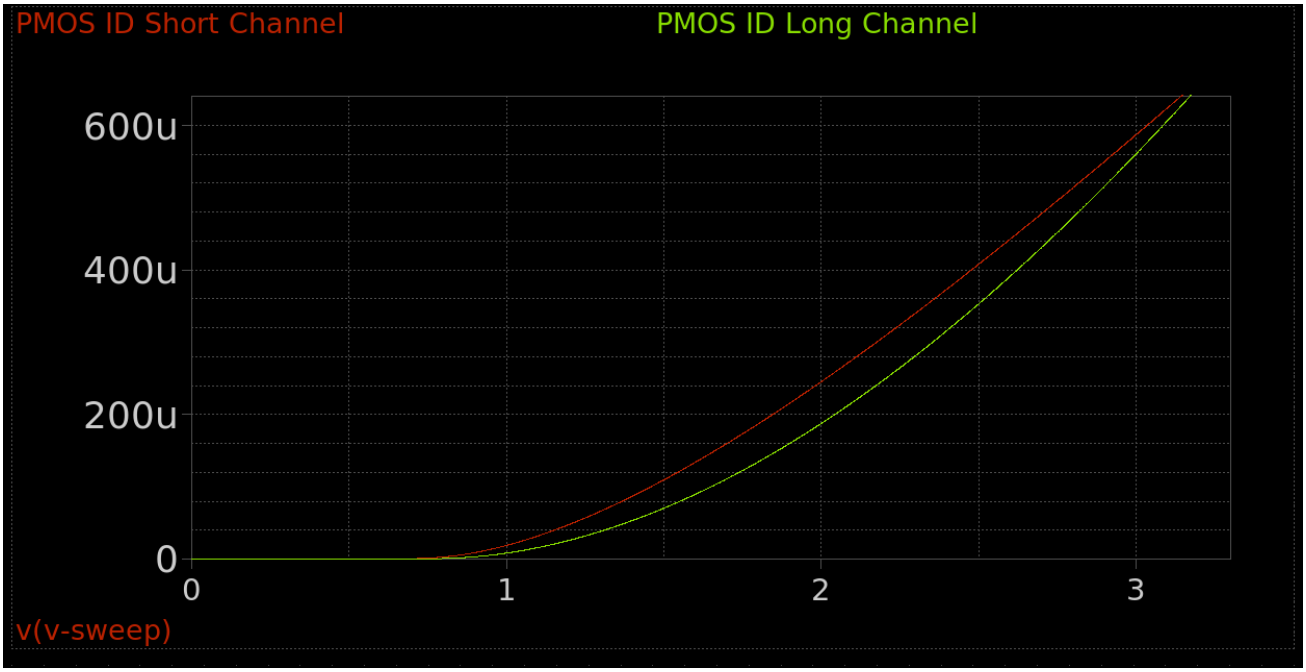

Figure 16 PMOS ID vs VGS, Yellow: Long-Channel, Red: Short-Channel

Comment on the differences between short channel and long channel results.

• Which one has higher current? Why?

The Long Channel Device has higher current, due to the lower electric field in the channel allowing carriers to move more freely, While in short-channel the carriers' velocity saturates limiting the current.

The effect is more noticeable in NMOS devices due to the higher carrier mobility.

• Is the relation linear or quadratic? Why?

Long-Channel: Has a quadratic relation as per the square-law Id = K*Vov^2/2

Short-Channel: Has a linear relation as per the velocity saturation law.

Comment on the differences between NMOS and PMOS.

• Which one has higher current? Why?

NMOS, due to the higher mobility of electrons (Majority Carrier).

• What is the ratio between NMOS and PMOS currents at VGS = VDD?

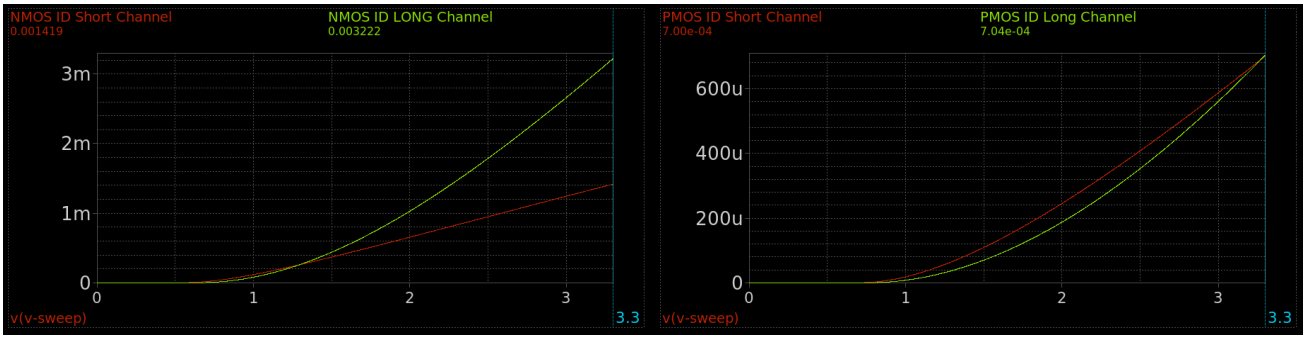

Figure 17 Values of ID at VDD for both NMOS and PMOS

Long-Channel Current Ratio: $ratio = \frac{0.003222}{7.04e{-}04} = \mathbf{4.576}$

Short-Channel Current Ratio: $ratio = \frac{0.001419}{7e{-}04} = \mathbf{2.027}$

• Which one is more affected by short channel effects?

NMOS is more affected, due to the electrons (NMOS Majority Charge Carrier) having a higher mobility than Holes (PMOS Majority Charge Carrier).

2. gm vs VGS

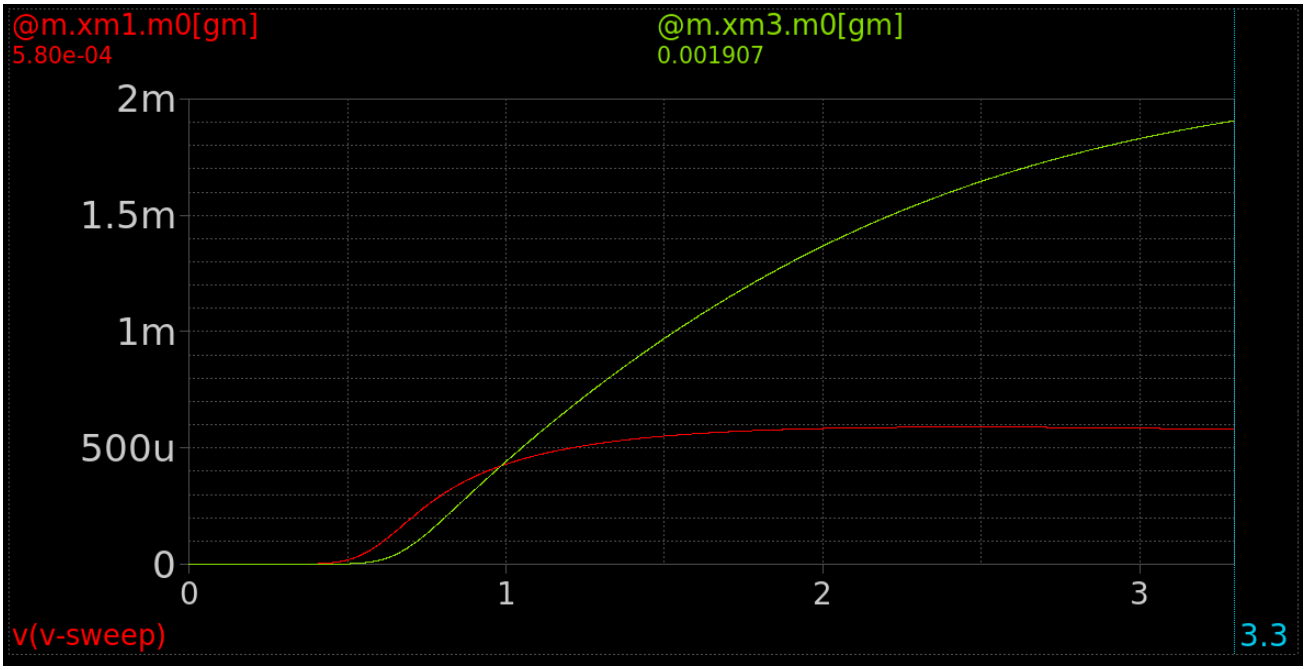

Figure 18 NMOS gm vs VGS, Green: Long-Channel, Red: Short-Channel (XSchem)

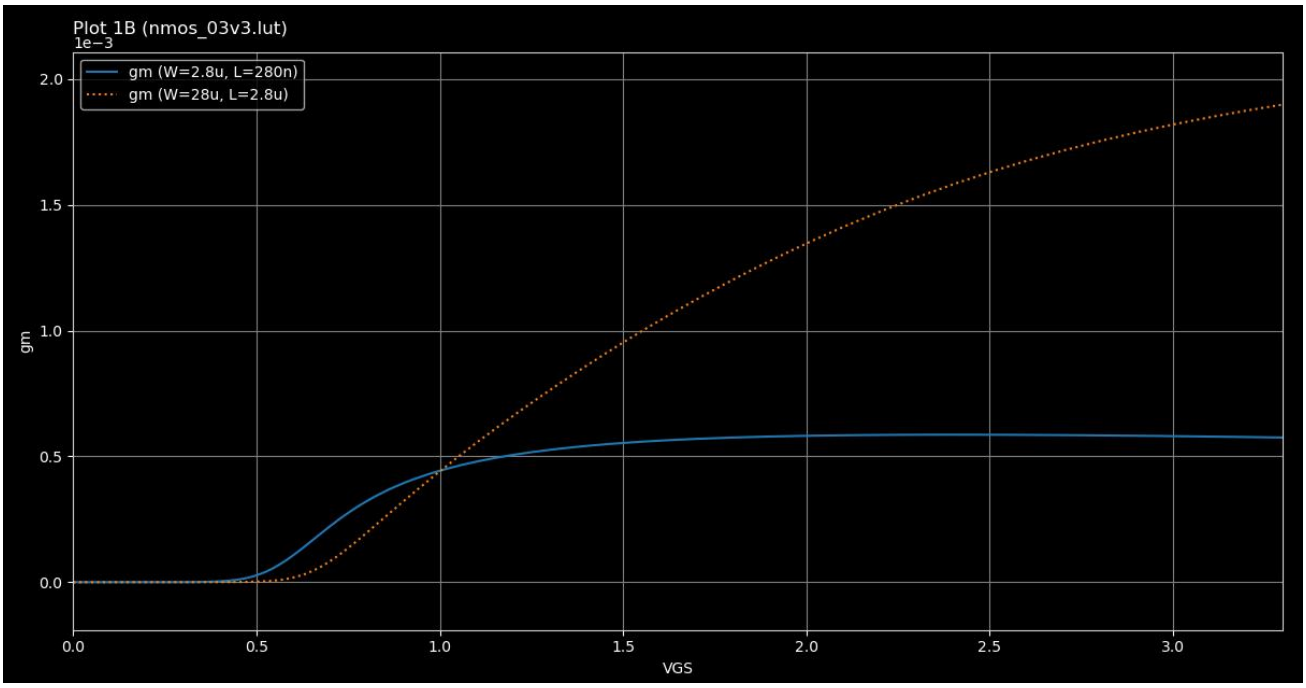

Figure 19 NMOS gm vs VGS, Orange: Long-Channel, Blue: Short-Channel (ADT)

Comment on the differences between short channel and long channel results.

- **Does gm increase linearly? Why?**

As the device turns on when VGS = Vth, gm starts increasing approximately linearly in both short and long channel as gm = k * (Vgs – Vov), but in short channel the linear increase stops early.

- **Does gm saturate? Why?**

It Does saturate, as Vov increases past VD_{SAT}, gm starts to saturate, its value can be evaluated via $gm = \frac{\partial I}{\partial V_{gs}}$

3. IDS vs VDS

Sweeping over: **V_{DS} = 0:V_{DD}**, and **V_{GS} = 1:1:3**

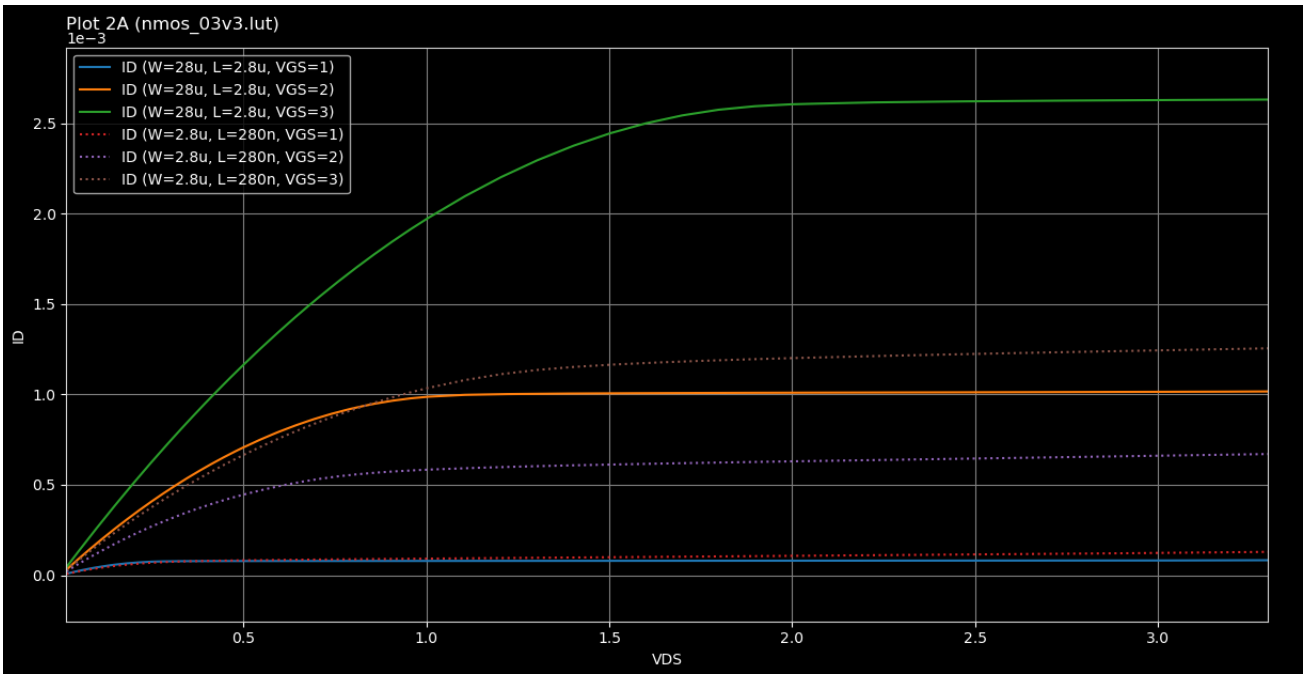

Figure 20 NMOS IDS vs VDS – Long and Short Channels

Comment on the differences between short channel and long channel results.

- **Which one has higher current? Why?**

Long-Channel has noticeably higher current, This is due to it operating in Pinch-Off saturation which has a quadratic relation for the current as opposed to the Short-Channel NMOS which operate in Velocity Saturation which has a linear relation for the current.

- **Which one has higher slope in the saturation region? Why?**

Short-Channel has a higher slope in the saturation region, Due to the effect of ro.

As the length of the channel decreases the resistance between the drain and source decreases and becomes more noticeable in the short channel device.

But in the long channel device this resistance is very large, approximately infinite. resulting in no slope appearing in the saturation region.