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وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

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Analog IC Design (Xschem, Ngspice, ADT)
Lab 05
Simple vs Wide Swing (Low Compliance) Cascode Current Mirror

Intended Learning Objectives

In this lab you will:

- Explore current mirror sizing trade-offs using Sizing Assistant (SA).
- Bias a cascode device using a series resistance.
- Design and simulate simple and wide swing (low-voltage) current mirrors.
- Compare simple and wide swing current mirrors.
- Investigate the effect of mismatch on a wide swing current mirror.

Part 1: Exploring Sizing Tradeoffs Using SA

1) We want to design a simple current mirror with the following specs.

Parameter	
Current direction (source/sink)	Sink
Input Current	$10\mu A$
Output Current	$20\mu A$
% Change in Current for $\boldsymbol{\Delta V_{out} = 1V}$	$< 10\%$
Percent mismatch: $\boldsymbol{\sigma(I_{out})/I_{out}}$	$\leq 2\%$
Compliance voltage	$\leq 150mV$
Area	Minimize

2) Sinking current means which device type? NMOS or PMOS?
3) The % Change in current translates to a spec on the $\lambda = 1/V_A$ of the device. How much is the required λ?
4) The current mirror bias point trade-offs are summarized in the table below.

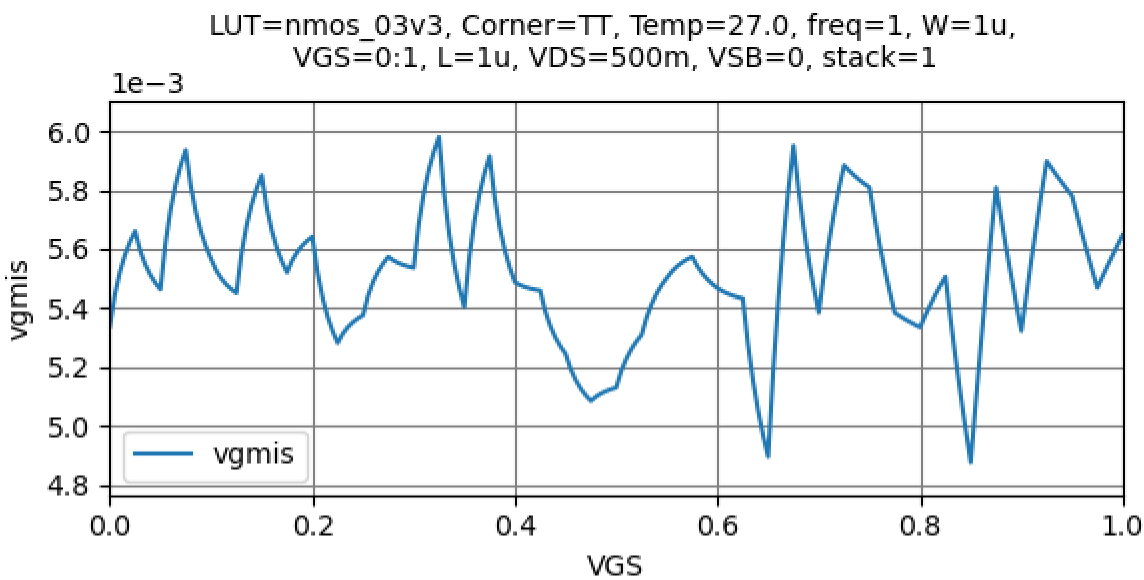
Parameter	Higher gm/ID (lower V^*)	Lower gm/ID (higher V^*)
Area	☹	😊
Dependence on $\boldsymbol{V_{DS}}$ (output resistance, $\boldsymbol{\lambda = 1/V_A}$)	☹	😊

Random mismatch	☹	☺
Systematic mismatch	☹	☺
Compliance voltage (headroom)	☺	☹

5) The most important mismatch effect is the VTH mismatch, which is modeled by Pelgrom's equation:

$$\sigma_{VT} = \frac{A_{VT}}{\sqrt{W \times L}}$$

Set a device that has WxL = 1um2 so that $\sigma_{VT} = A_{VT}$. Plot vgmis vs VGS in SA. Note the random variations because vgmis is extracted from a Monte Carlo (MC) simulation that has finite no. of samples (finite population), so this is an estimate of the standard deviation, not the true one. If the mismatch is characterized using dcmatch simulation (not always supported by the model), the results will be smooth and more accurate.



6) From the model file, calculate σ_{VT} (var_vth at WxL = 1um2) and compare it to the value in ADT. Which one is higher, why?

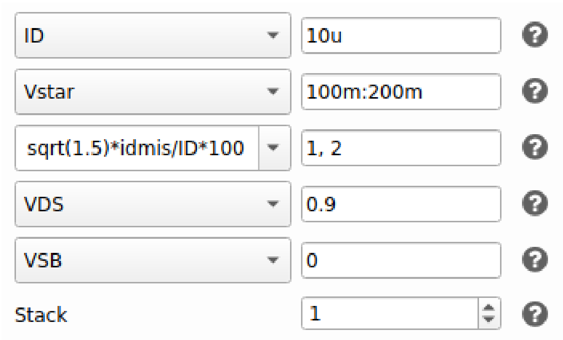
```
gedit ~/pdk/gf180mcuC/libs.tech/ngspice/ sm141064.ngspice &
```

```
.lib fets_mm
.subckt nmos_3p3 d g s b w=1e-5 l=2.8e-7
+ as=0 ad=0 ps=0 pd=0 nrd=0 nrs=0 par=1 dtemp=0
+ sa=0 sb=0 nf=1 sd=0 m=1

.param
+ par_vth=0.007148
+ par_k=0.007008
+ par_l=1.5e-7
+ par_w=-1e-7
+ par_leff='l-par_l'
+ par_weff='par*(w-par_w)'
+ p_sqrtarea='sqrt((par_leff)*(par_weff))'

.param
+ var_k='0.7071*par_k* 1e-06 / p_sqrtarea'
+ mis_k=agauss(0,var_k,1)

.param
+ var_vth='0.7071*par_vth* 1e-06 / p_sqrtarea'
+ mis_vth=agauss(0,var_vth,1)

m0 d g s b nmos_3p3 w=w l=l as=as ad=ad ps=ps pd=pd nrd=nrd nrs=nrs
+delvto='mis_vth*sw_stat_mismatch'  sa=sa sb=sb nf=nf sd=sd
.ends nmos_3p3
*-----------------------------------------------------------------
```

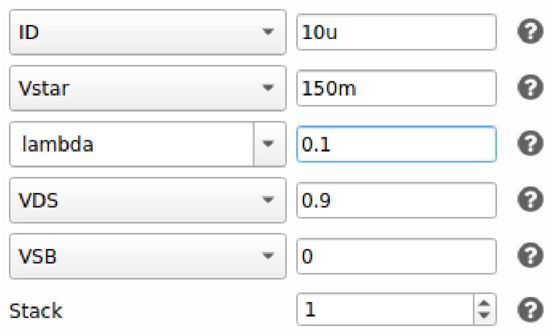
7) Examine these trade-offs using SA. Use SA to plot the sizing at a constant $\boldsymbol{\sigma(I_{out})}/I_{out}$ which is given by

$$\frac{\boldsymbol{\sigma(I_{out})}}{\boldsymbol{I_{out}}} = \frac{\sqrt{\boldsymbol{1+\frac{1}{m}}} \times \boldsymbol{idmis}}{I_D} \times \mathbf{100}$$

The $\sqrt{1+\frac{1}{m}}$ factor is due to taking into account the effect of two random variables (V_{TH} of the two current mirror transistors).
Plot L, W, AREA, and λ. The results will not be smooth due to the bumpy mismatch data in the LUT.



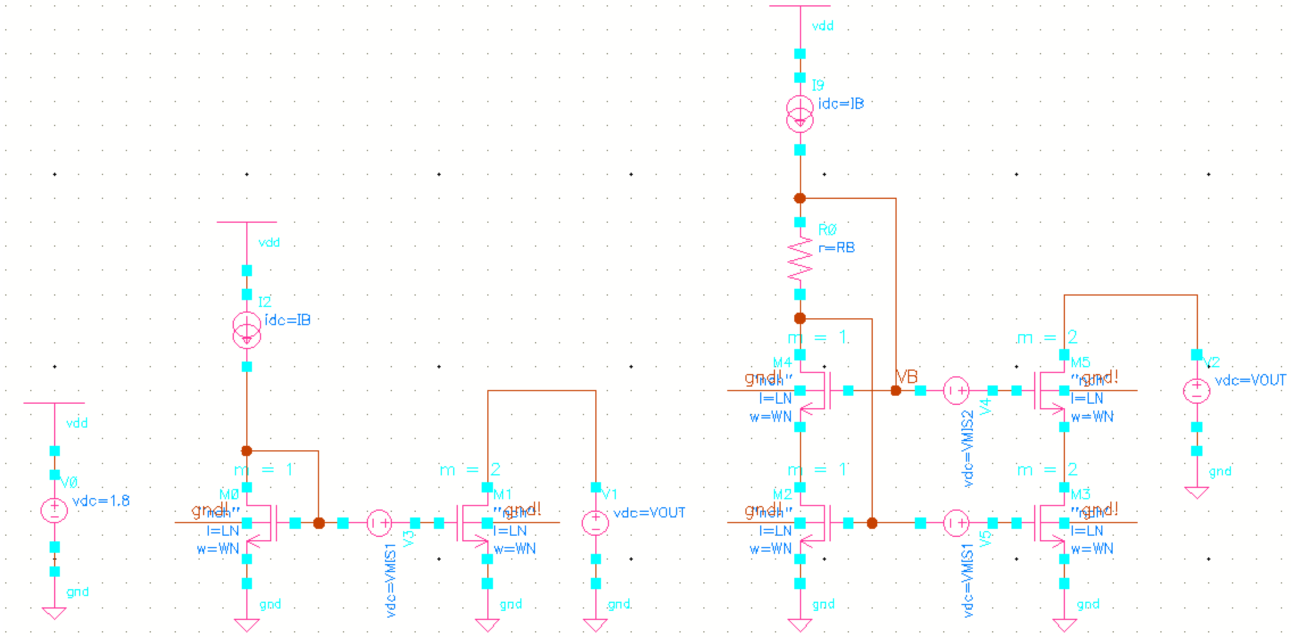
8) The above results mean that the highest V^* is desirable from the perspective of mismatch, area, and λ. Thus, V^* will be limited by the required compliance voltage.
NOTE: We assume that the compliance voltage $\approx V_{DSsat} \approx V^*$.
9) **Report** the above plot with a cursor added at the required V^*. Does this point satisfy the mismatch and λ constraints?
10) If the λ constraint is not satisfied at $\boldsymbol{\sigma(I_{out})}/I_{out} = 2\%$, i.e., it needs a longer L, we can use SA to find the required design point as shown below.
Note: Lambda is defined in ADT expression manager.



11) **Report** the device sizing and $\boldsymbol{\sigma(I_{out})}/I_{out}$ at the selected design point.

Part 2: Current Mirror Simulation

1) Create a new schematic. Construct the circuit shown below.



2) The current mirror takes input current IB and generates output current = 2*IB (note the multiplier setting in the output branch).
3) Instead of using a wide-swing bias transistor (a magic battery) to generate VB, we use a resistor RB in series with the input branch.
4) Unless otherwise stated, set VOUT = VDD/2 and VMIS1 = VMIS2 = 0.

1. Design and OP (Operating Point) Analysis

1) Assume we want to set a $50mV$ saturation margin for M2 and M3, i.e., $V_{DS2} \approx V_{DS3} \approx V^* + 50mV$. Ignore the body effect and **calculate** a rough value for RB.
   Hint: $R_B = \frac{V_{GS4}+V_{DS2}-V_{GS2}}{I_B} \approx \frac{V_{DS2}}{I_B}$
   Hint: The purpose of doing rough analysis is not to reach a final design point, but to calculate a value that makes sense and can be used to determine a reasonable range for a simulator sweep.
2) Perform DC sweep (not parametric sweep) for RB. Choose a reasonable sweep range given the rough value computed in the previous step. **Report** V_{DS3} vs R_B. **Choose** R_B to satisfy the $50mV$ saturation

margin requirement. Is the selected R_B value larger or smaller than the rough analytical value? Why?

➔ Hint: The DC sweep is performed in a simulator inner loop, so it is very fast and takes small disk space. The parametric sweep is an outer loop repetitive calling of the simulator, so it is much slower and takes much larger disk space.

3) Simulate the OP point. Report a snapshot clearly showing the following parameters.

ID
VGS
VDS
VTH
VDSAT
GM
GDS
GMB

4) Do all transistors operate in saturation?

2. DC Sweep (I_{out} vs VOUT)

1) Perform DC sweep (not parametric sweep) using VOUT = 0:10m:VDD. Report I_{out} vs VOUT for the two CMs overlaid in the same plot.
   - Comment on the difference between the two circuits.
   - From the plot, find an estimate for the compliance voltage of each current mirror.
   - I_{out} of the simple CM is exactly equal to IB*2 at a specific value of VOUT. Why?
2) For the simple current mirror, calculate the percent change in I_{out} when VOUT changes from 0.5V to 1.5V (i.e., 1V change). Compare the result to the value expected from Part 1.
3) Report the percent of error in I_{out} vs VOUT (ideal I_{out} should be IB*2) for the two CMs in the current mirror operating region (VOUT $\approx V^*$to VDD) overlaid in the same plot.
   Hint: Calculate percent of error as (simulated – ideal)/ideal * 100
   - Comment on the difference between the two circuits.
4) Report Rout vs VOUT (take the inverse of the derivative of I_{out} plot) for the two CMs in the current mirror operating region (VOUT $\approx V^*$to VDD) overlaid in the same plot. Use log scale on the y-axis. Add a cursor at VOUT = VDD/2.
   - Comment on the difference between the two circuits.
   - Does Rout change with VOUT? Why?

   ➔ Hint: Rout can also be simulated using AC analysis. The value we used here should be similar to the AC analysis result at low frequencies.
5) Analytically calculate Rout of both circuits at VOUT = VDD/2. Compare with simulation results in a table.

3. Mismatch

NOTE: Usually we study the mismatch using Monte Carlo simulation as will be shown in the next section. However, in this section, we will manually add mismatch in the circuit.

1) Perform DC sweep for VMIS1 from 0 to sqrt(1.5)*3.5m/sqrt(W*L*1e12) and set VMIS2 = 0. This models the standard deviation of the mismatch in V_{TH} for the current mirror devices. Find the percent change in I_{out}.
2) Analytically calculate the percent change in I_{out} and compare it to the simulation result.

Hint: The voltage change at the gate can be considered as a small signal. Thus, the change in the current can be calculated using the G_m of the circuit. In this case, the circuit can be considered as a cascode amplifier.

3) Set VMIS1 = 0 and perform DC sweep for VMIS2 from 0 to sqrt(1.5)*3.5m/sqrt(W*L*1e12). This models the standard deviation of the mismatch in V_{TH} for the cascode devices. Find the percent change in I_{out}.
4) Analytically calculate the percent change in I_{out} and compare it to the simulation result.
Hint: The voltage change at the gate can be considered as a small signal. Thus, the change in the current can be calculated using the G_m of the circuit. In this case, the circuit can be considered as a ***degenerated*** common source amplifier.
5) Which mismatch contribution is more pronounced? Why?
6) Which design decision is better: setting the same W and L for the mirror and cascode devices? Or using larger W and L for the current mirror devices? Why?

4. Monte Carlo (MC) Simulation

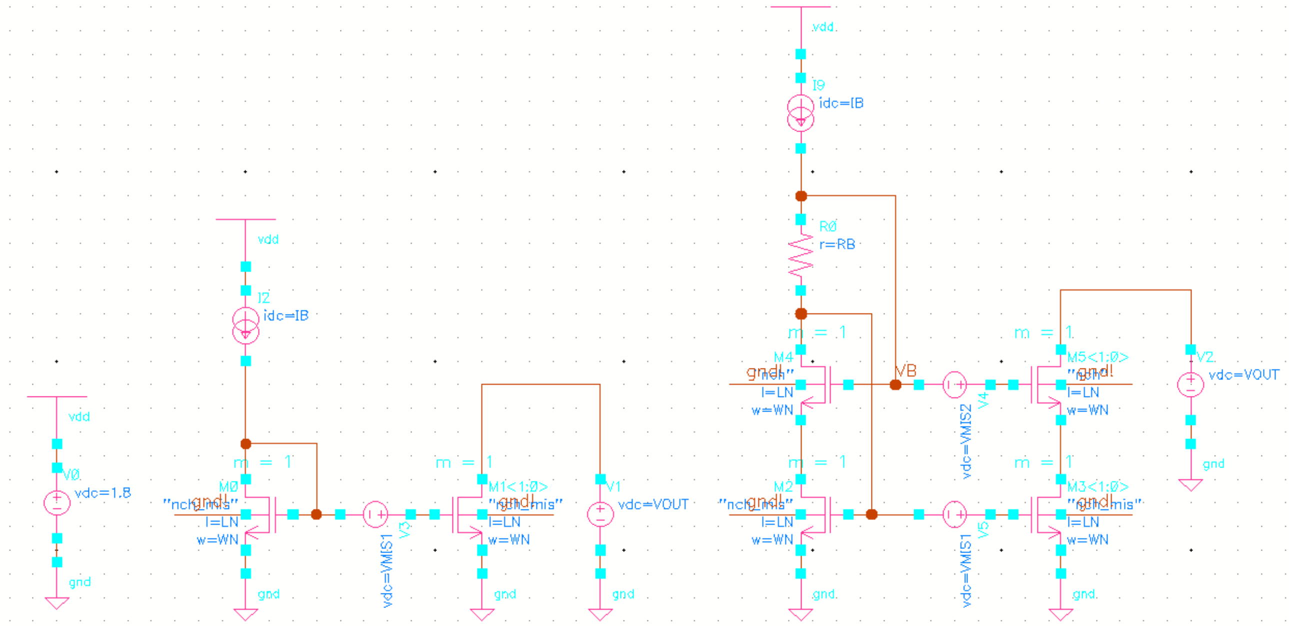
Note: Enable Monte Carlo in the model file.

```
gedit ~/pdk/gf180mcuC/libs.tech/ngspice/design.ngspice &
```

```
** MonteCarlo and matching simulation setting:
** -----------------------------------------
** sw_stat_global
** sw_stat_mismatch
**
**   -------------------------------------------------------------------------
**   |        setting         |  sw_stat_global=0      |  sw_stat_global=1       |
**   -------------------------------------------------------------------------
**   |  sw_stat_mismatch=0    | No statistical         | Global variation is on, |
**   |                        |  modeling              | but mismatch is off.    |
**   -------------------------------------------------------------------------
**   |  sw_stat_mismatch=1    | mismacth is on,        | Most realistic          |
**   |                        | global variation off   | distribution.           |
**   -------------------------------------------------------------------------
**
**
**   (default) - sw_stat_global=1 and sw_stat_mismatch=1
**   This setting provides the most complete representation of the
**   statistical variations during chip manufacturing.
**   Global process variations are determined by random distributions.
**   Mismatch is differentiated from global variation in that mismatch only
**   includes intra-die variation, and it is especially critical for analog matching applications.
**
**   mc_skew is the monte-carlo simulation variation control.
**
**
** -----------------------------------------
**       Flicker noise corner setting:
** -----------------------------------------
**
**        "fnoicor" switch is added for user to select between the best- or worst-case
**         flicker noise simulation options
**         fnoicor = 0  : (default) as-extracted simulation
**         fnoicor = 1  : worst case simulation
**
** ****************************************************************************
**
** Switches
**
*********** Default mc switches **********
**
.param
+  sw_stat_global = 1
+  sw_stat_mismatch = 1
```

Note: Using the multiplier parameter can give wrong mismatch results for the given model file because the errors from the parallel devices will be correlated. Thus, set m = 1, and name the device as an array of two devices ‘Mx<1:0>’ as shown in the schematic below. Check this article for more information.

Note: In this section we will set both VMIS1 and VMIS2 to zero.



1) Set up MC simulation by using a loop similar to the code given below.
   Note: Test and debug with 10 runs, then do the real simulation with 100 or 200 runs.

```
let mc_runs = 10
let run = 1
dowhile run <= mc_runs
      * run op analysis
      * print Iout in a text file
      ...
      let run = run + 1
end
```

2) Copy the printed Iout to Excel or Matlab and plot the histogram of I_{out}.
3) Calculate the standard deviation percentage $\boldsymbol{\sigma(I_{out})}/I_{out}$.
4) Compare the MC simulation result to the expected analytical result.

Lab Summary

In Part 1 you learned:

- How to use SA to examine current mirror design trade-offs.
- How to design a simple current mirror.

In Part 2 you learned:

- How to design a wide swing (low-voltage) current mirror.
- How the behavior of a simple current mirror changes with the output voltage.
- How the behavior of a wide swing current mirror changes with the output voltage.
- The effect of mismatch on a wide swing current mirror.
- How to perform Monte Carlo simulations for a current mirror circuit.

Acknowledgements

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