Analog IC Design

Lecture 01
Introduction

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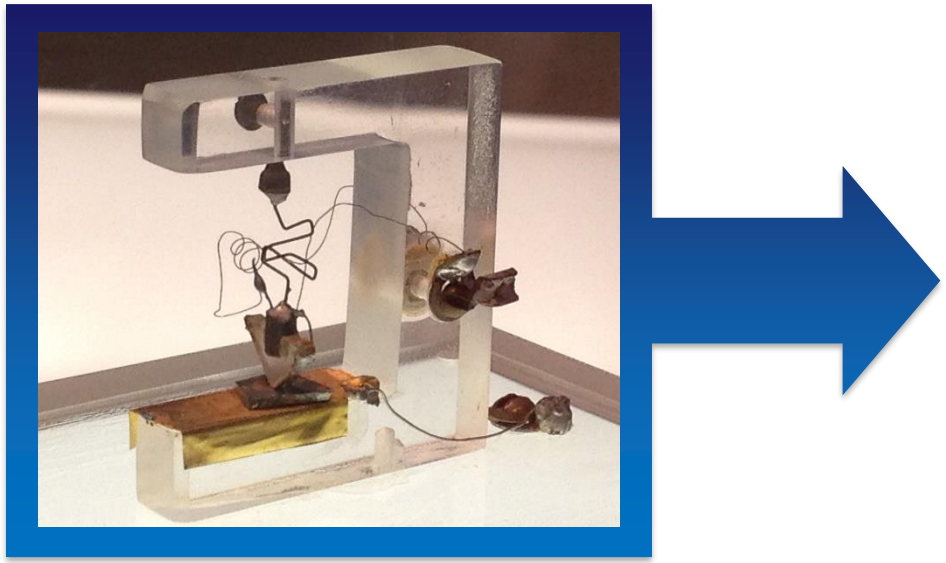
Introduction

ENIAC, U.S. Army, 1946
Size → Large hall (> 150m^2)
Power Consumption ≈ 150kW

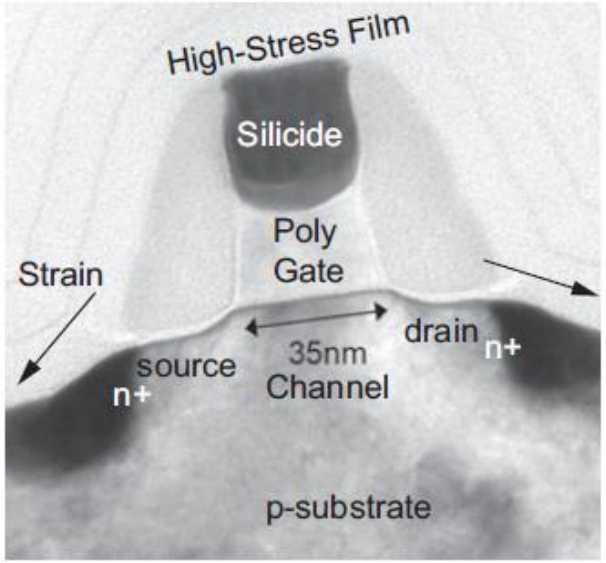
Smart phone
Size → Your pocket
Power consumption < 1W

Electronics All Around Us

Transistor Evolution



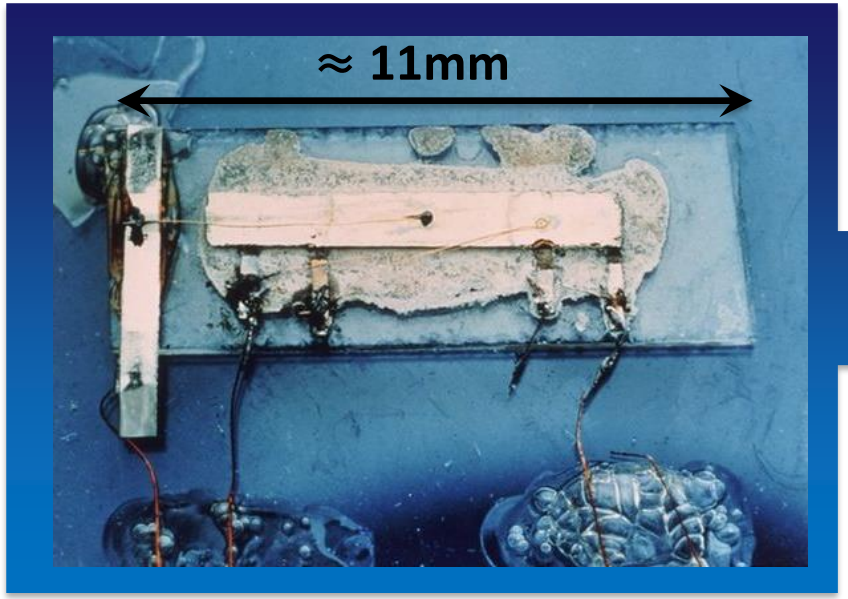
First transistor
Emitter and Collector contacts
separation ≈ 100µm
Bell Labs, 1947



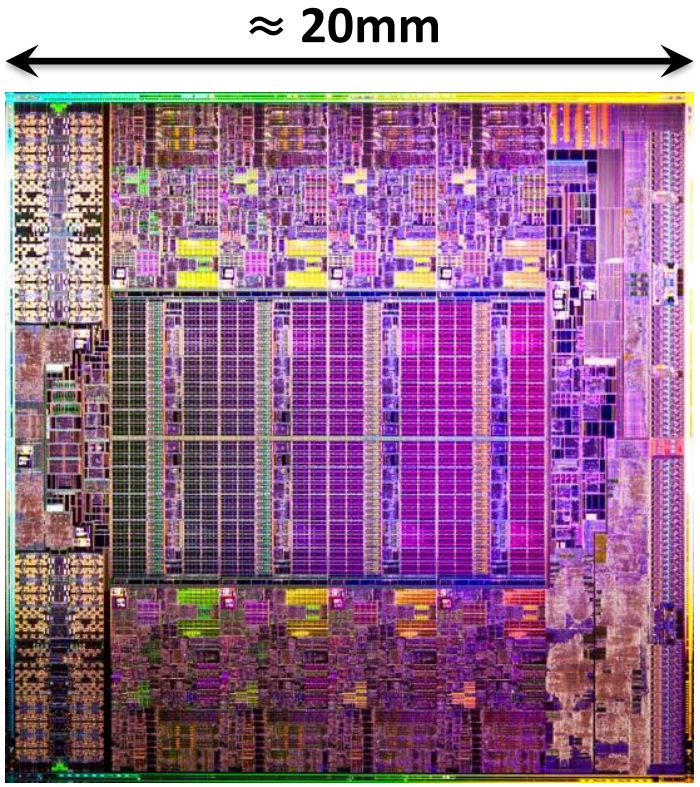
Modern MOSFET
Effective channel
length ≈ 35nm
Intel, 2006

[Weste and Harris, 2010]

Integrated Circuit Evolution

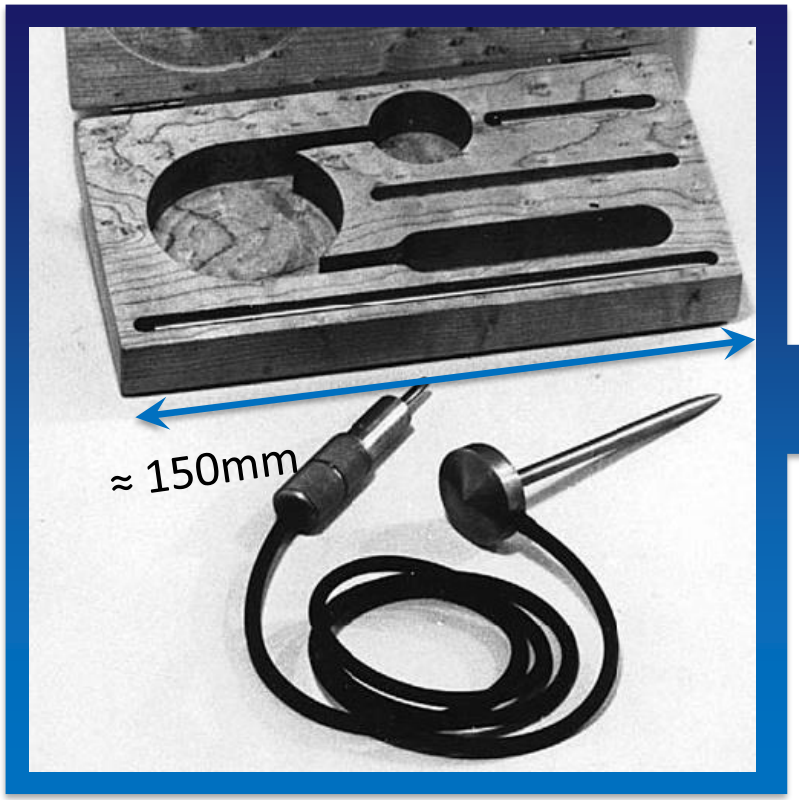


First IC
Only one transistor (+ R + C)!
Texas Instruments (TI), 1958

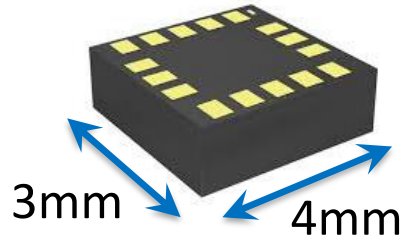


Xeon E5 Microprocessor
2.26 billion transistors!
Intel, 2012

Sensing Microsystems



First accelerometer
B&K, 1940s
Simple bulky transducer
Acceleration → Voltage



ADXL350
Analog Devices, 2012
Complete system on a tiny chip

- 3-axis MEMS* accelerometer
- Interface electronics
- Analog-to-digital conversion
- Memory
- Control logic
- Power management
- Digital interface

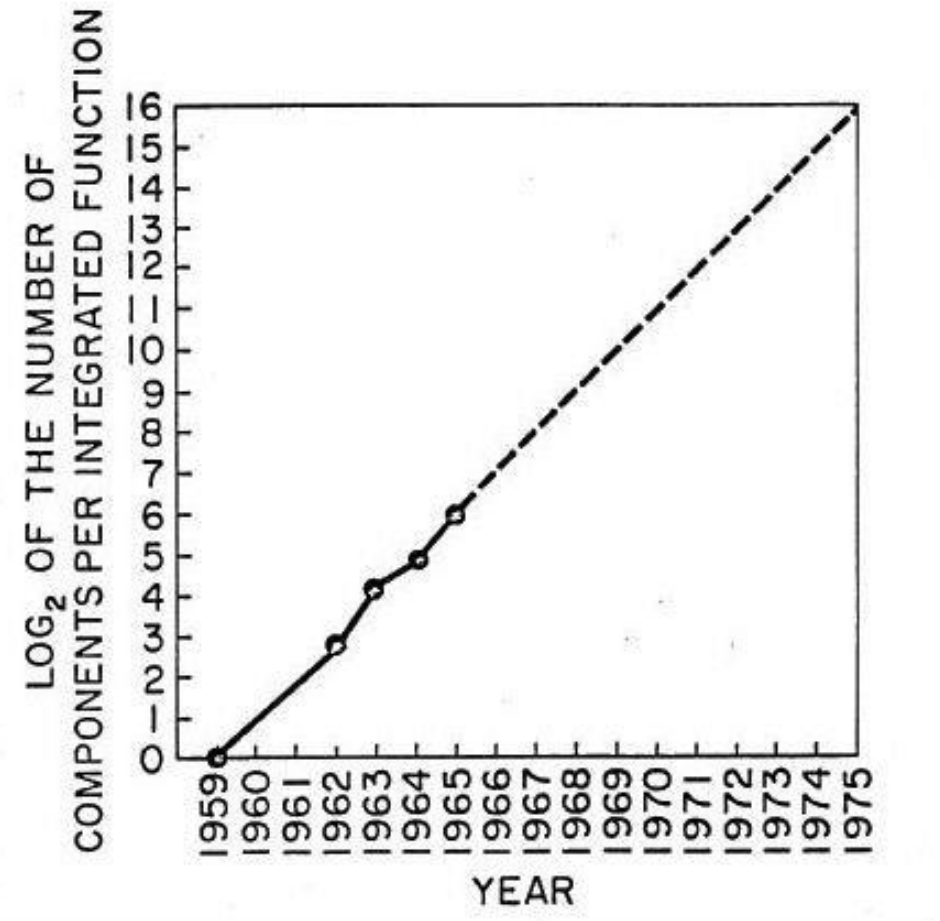
*MEMS = Micro-Electro-Mechanical Systems

Moore's Law

- Moore's law [1965]: Transistor count doubles every year

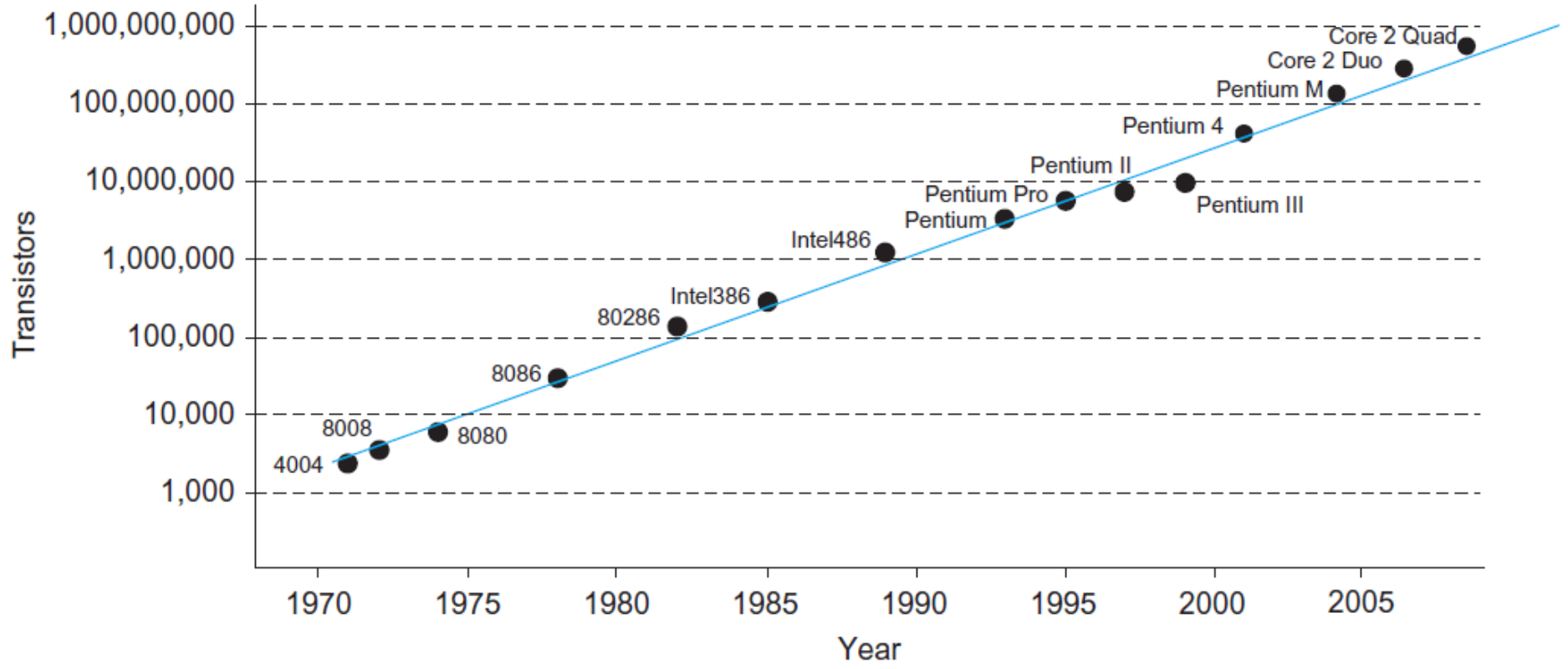
"The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years."

[Gordon Moore, Electronics Magazine, 1965]



Moore's Law

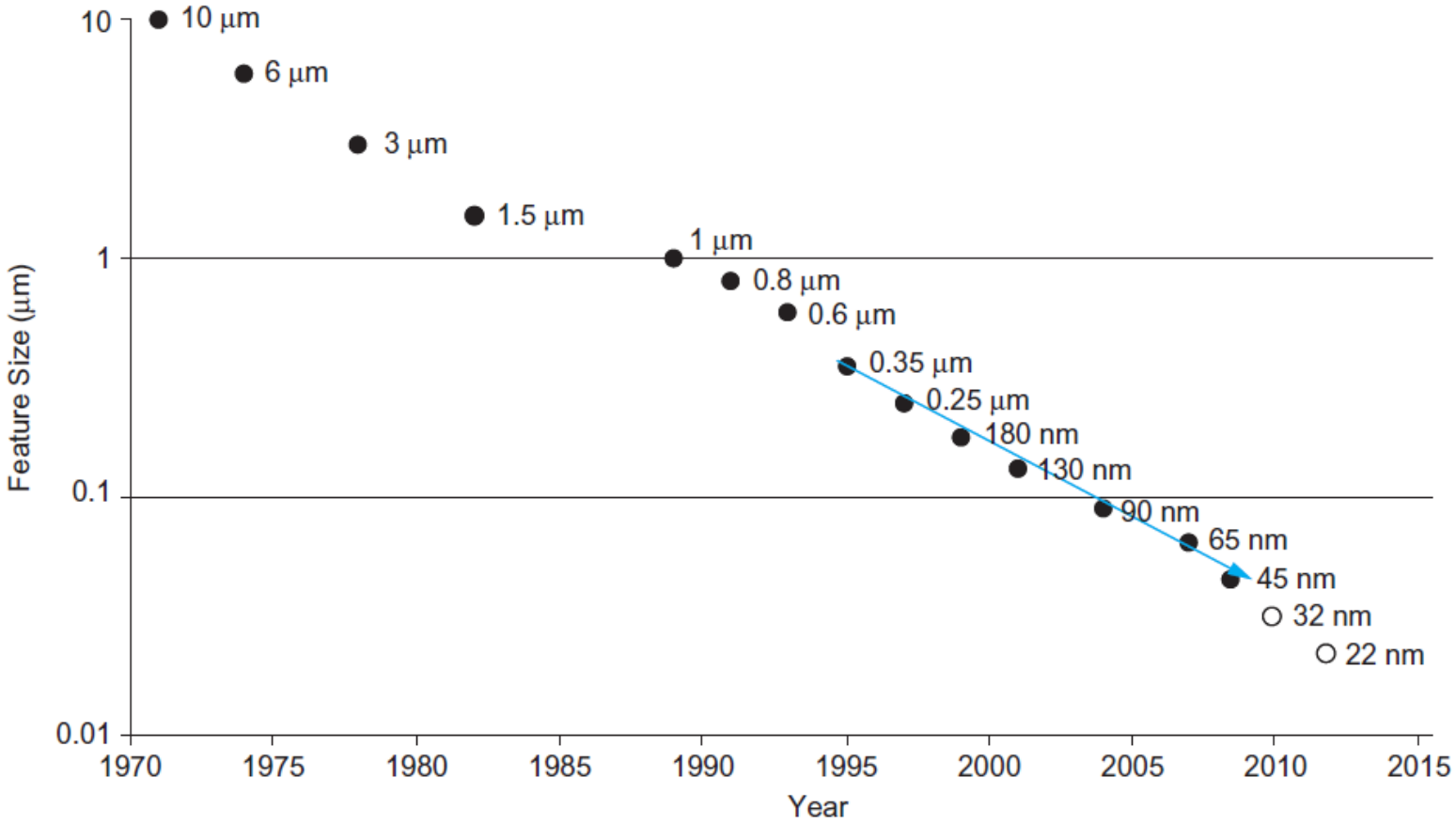
- Moore's law [1965]: Transistor count doubles every year
- Practically: It doubled every 2-3 years since the 4004 [1970s]
- At the end of the day: It is exponential!



[Weste and Harris, 2010]

Technology Minimum Feature Size

- Minimum feature size shrinking 30% ($\approx 1/\sqrt{2}$) every 2-3 years
  - Transistor **area and cost** are reduced by a factor of 2
- Device scaling brings new opportunities and challenges!



[Weste and Harris, 2010]

EE Times

MY CART

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Kiss CMOS scaling goodbye, IBM says

By Anthony Cataldo 06.18.1999 0

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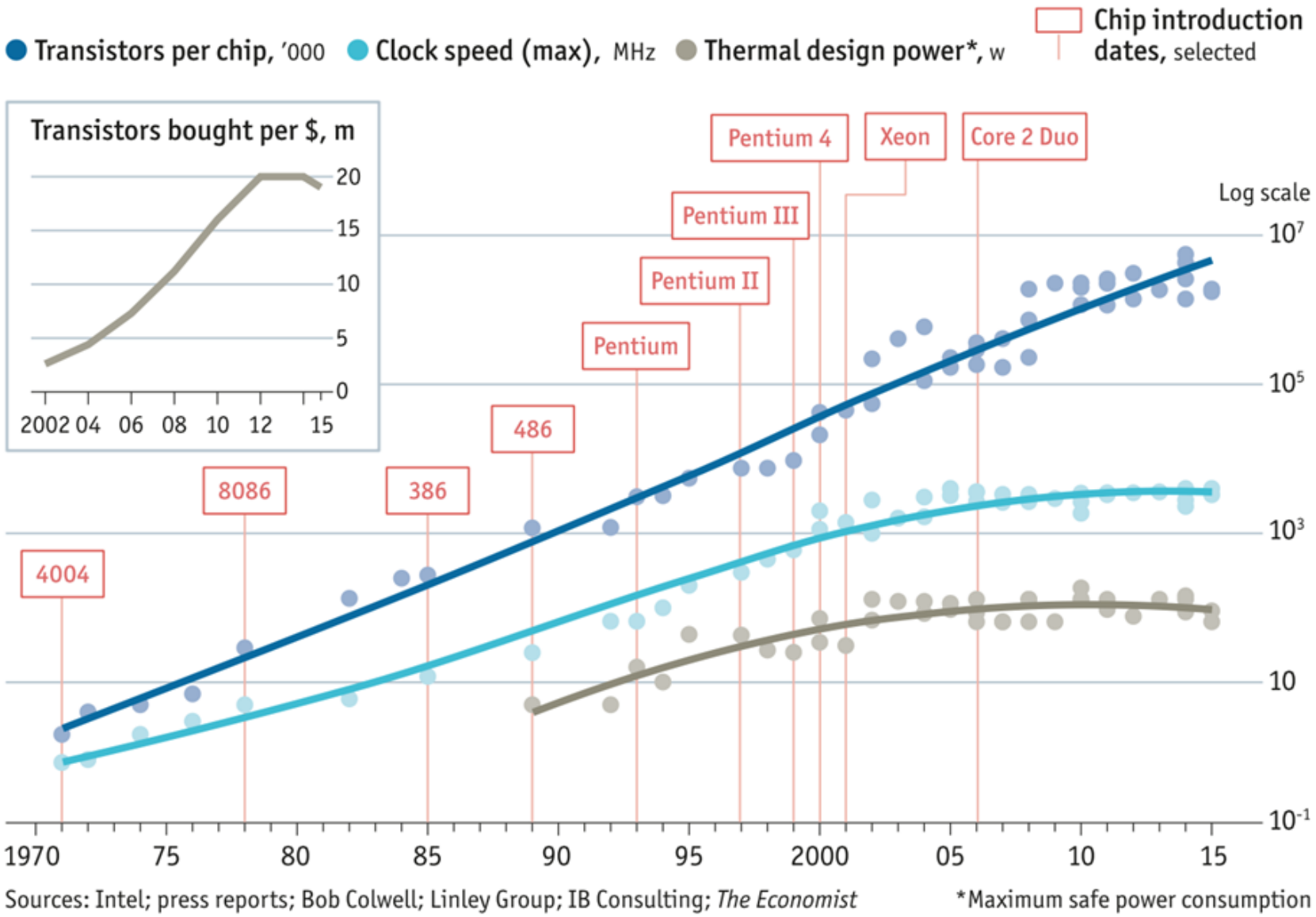
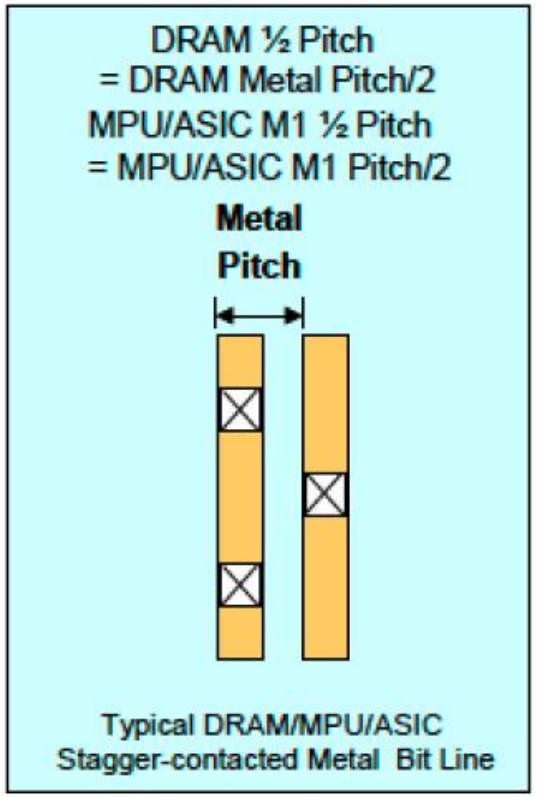
KYOTO, Japan — Engineers will bump smack up against some of the limits of CMOS process technology in the next five years, a senior IBM semiconductor researcher told the Symposium on VLSI Circuits this past week. Coming atop a growing body of commentary about the confines of the fundamental technology underlying mainstream chip manufacturing, the warning from Bijan Davari served to raise the question of whether the heady days of digital CMOS voltage scaling — and the performance gains it brought during the latter half of the 1990s — might soon be over.

The End of Moore's Law?



Technology Node

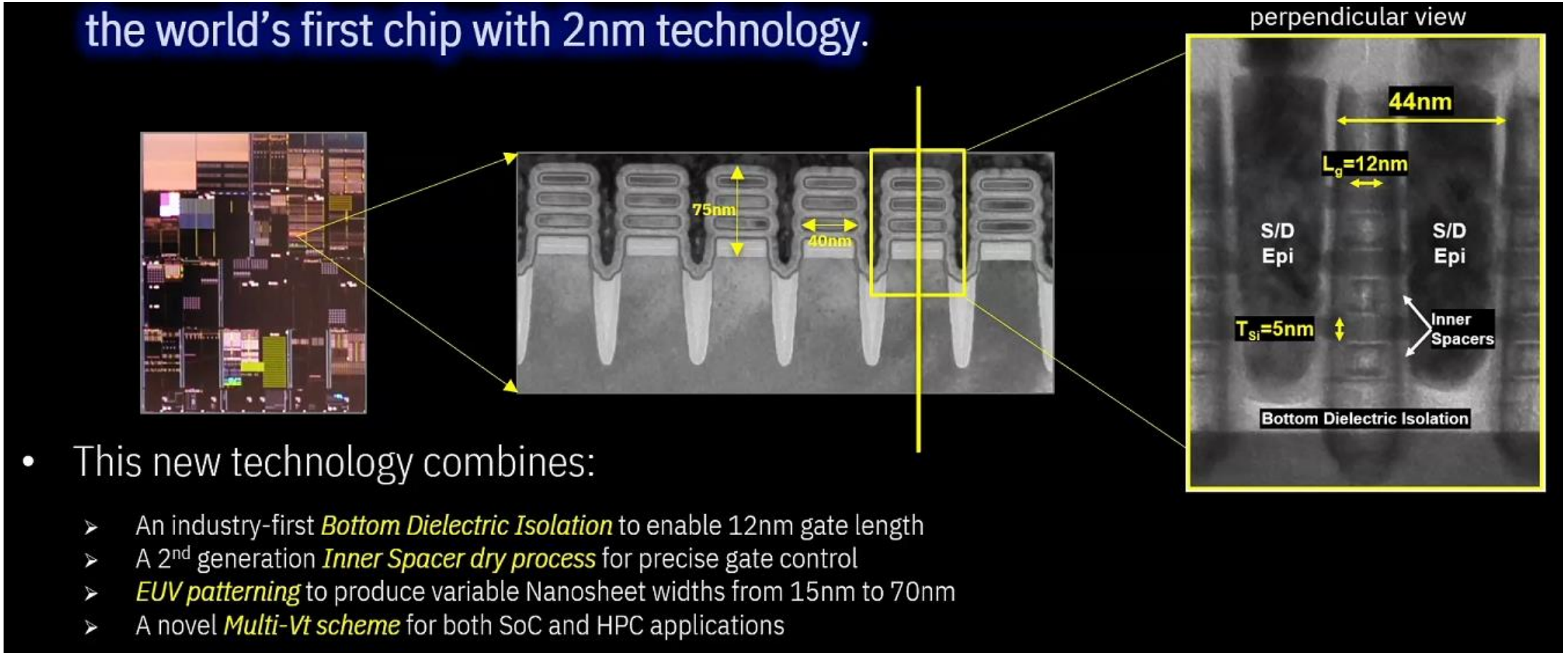
- Historically, the process node name referred to the transistor gate length (same as M1 half-pitch).
- Most recently, due to various marketing and discrepancies among foundries, the number itself has lost its exact meaning.
- Gate length has not scaled proportionately with device pitch (0.7x per generation) in recent generations.
- Recent technology nodes (22 nm and below) does not correspond to any gate length or half pitch!
  - Just 70% of whatever the name of the node of the previous generation was!



[https://en.wikichip.org/wiki/technology_node]
[IRDS ES, 2020]

IBM 2nm Technology

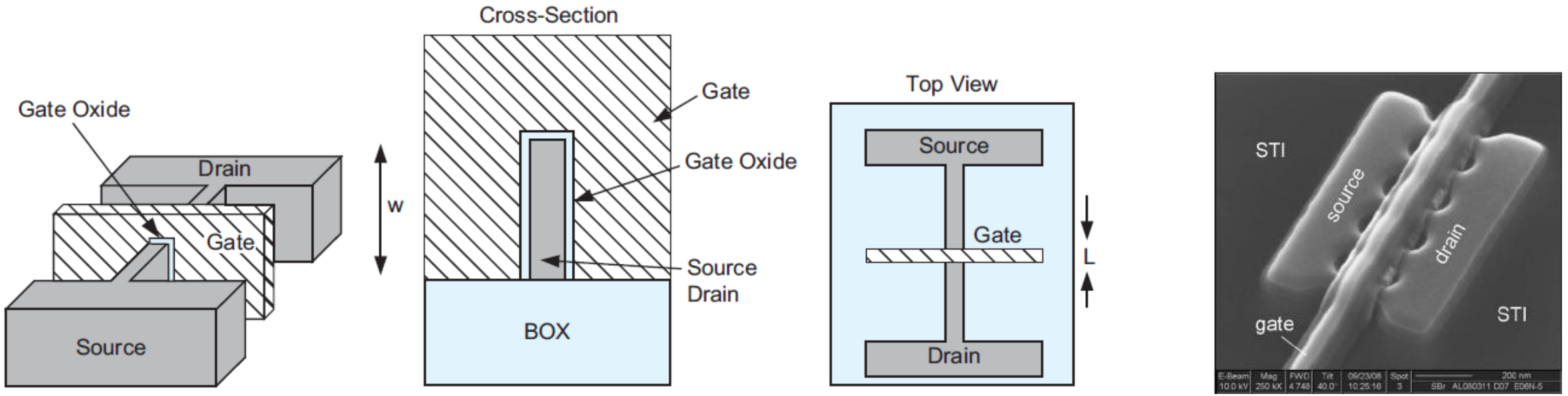
- IBM announcement of 2nm technologies does not correspond to 2nm feature size!
  - The individual nanosheets are 5nm in height, separated from each other by 5 nm.



[https://www.anandtech.com/show/16656/ibm-creates-first-2nm-chip]

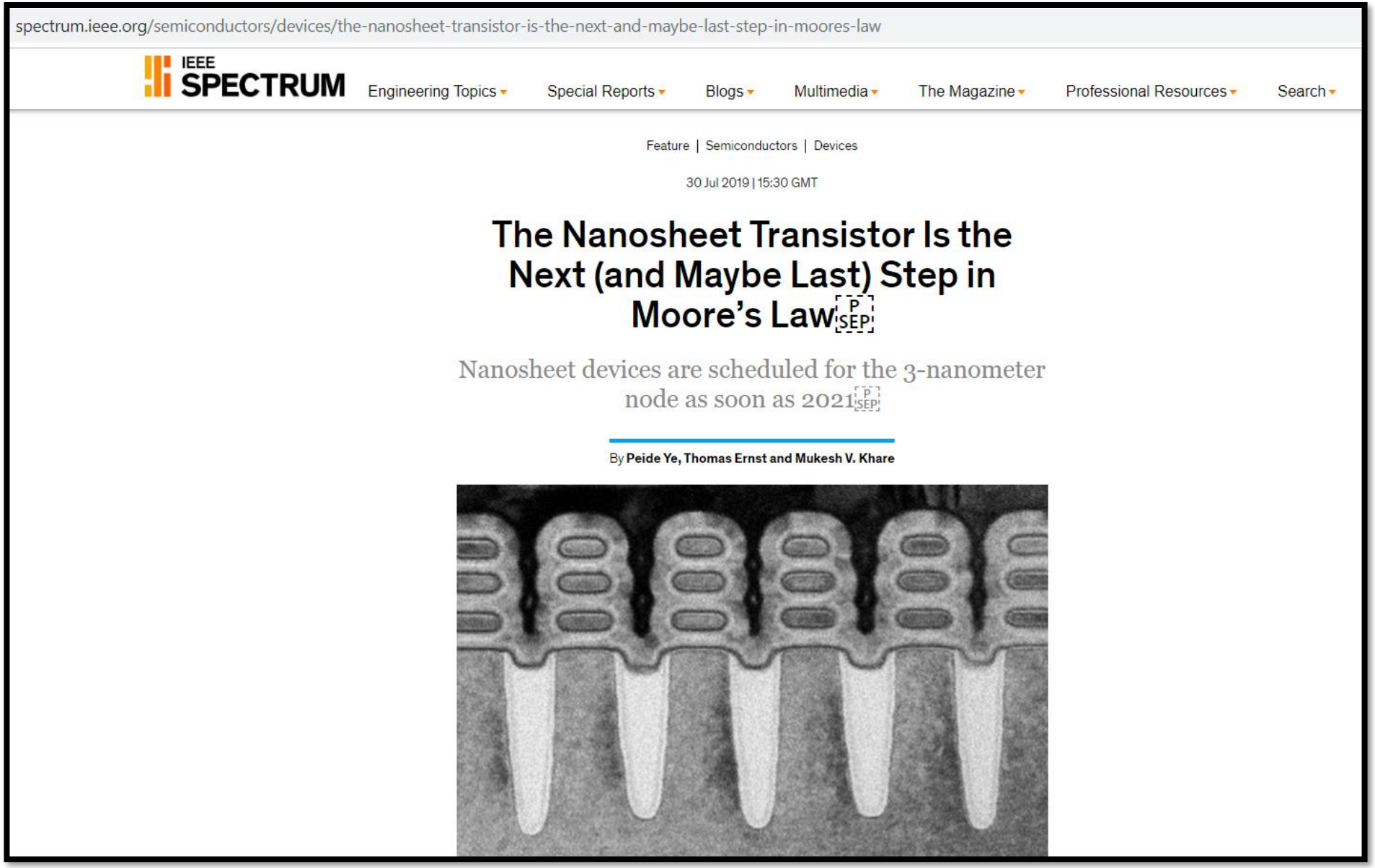
FinFET

- Planar CMOS cannot be scaled below 20nm due to excess leakage current and severe short channel effects.
- FinFET: Gate has better control on the channel
  - Intel's version is called trigate FET
  - Generally: Multigate transistor



[Weste and Harris, 2010]

The Last Step?



spectrum.ieee.org/semiconductors/devices/the-nanosheet-transistor-is-the-next-and-maybe-last-step-in-moores-law

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30 Jul 2019 | 15:30 GMT

The Nanosheet Transistor Is the Next (and Maybe Last) Step in Moore's Law

Nanosheet devices are scheduled for the 3-nanometer node as soon as 2021

By **Peide Ye, Thomas Ernst and Mukesh V. Khare**

Or The Next Step?

spectrum.ieee.org/nanoclast/semiconductors/devices/intels-stacked-nanosheet-transistors-could-be-the-next-step-in-moores-law

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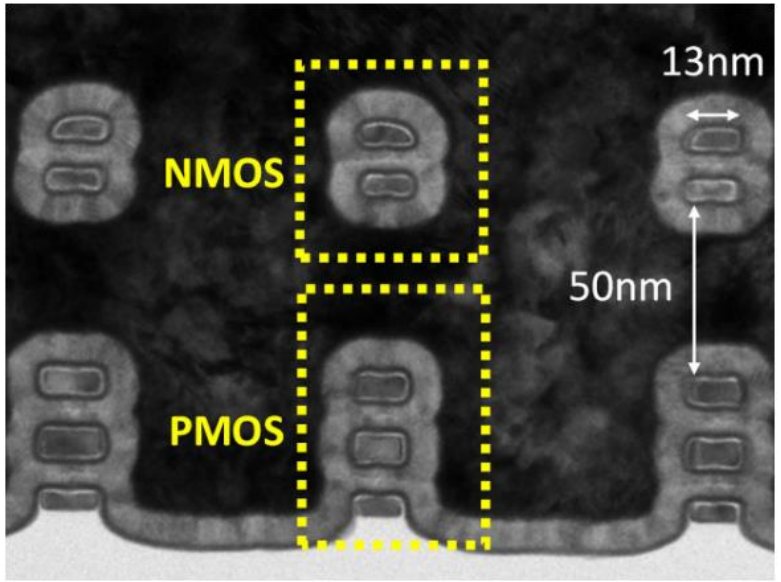
29 Dec 2020 | 16:00 GMT

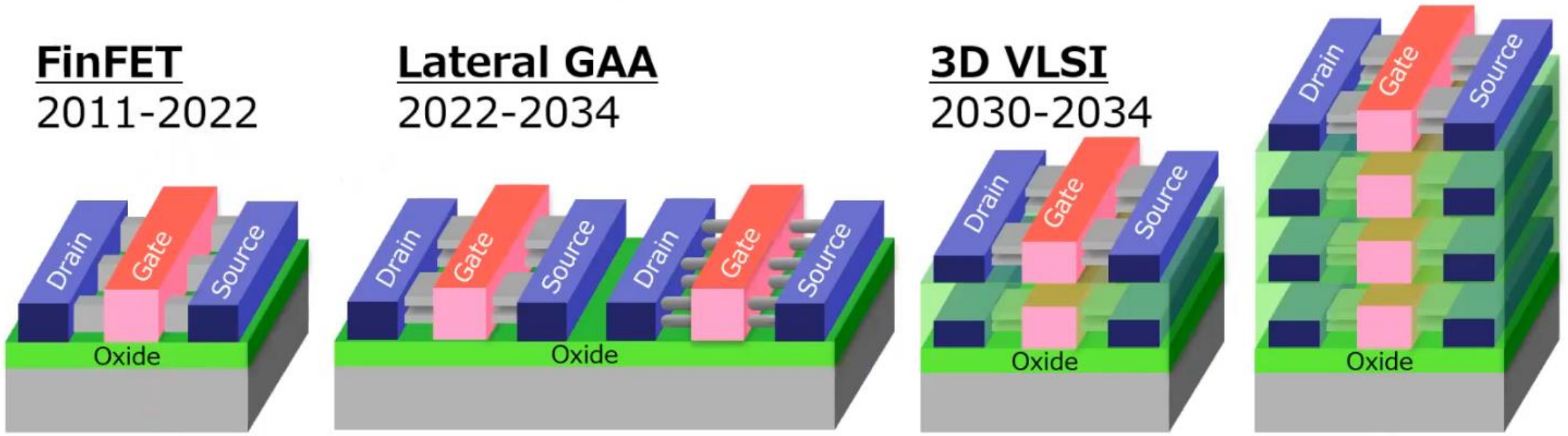
Intel's Stacked Nanosheet Transistors Could Be the Next Step in Moore's Law

Process that builds two transistors—one directly atop the other—will boost chip density

By **Samuel K. Moore**



Still Too Many Steps! – IRDS 2021



- Increasing drive by taller fin
- Better channel control for better perf-power

- Increasing drive by stacked devices
- Better channel control for better perf-power
- Reduced footprint stdcell

- Sequential integration/fine-pitch stacking (e.g. logic, memory, NVM, analog, IO, RF, sensors)

IO: Input/Output
RF: Radio Frequency

Source; IRDS 2021 Edition, More Moore

IEEE

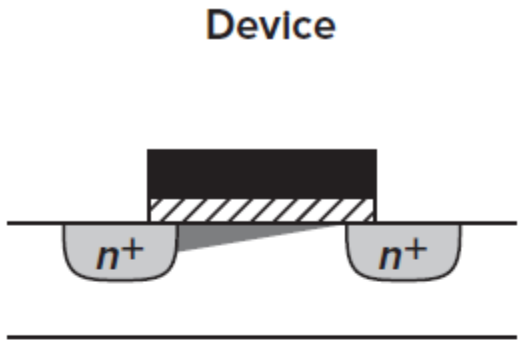
[https://irds.ieee.org/images/files/pdf/2020/2020IRDS_BC.pdf]

The different Ages of Scaling

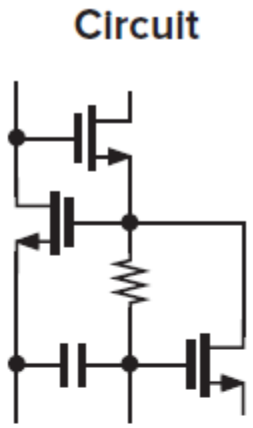
- 1975 – 2000: Geometrical scaling
  - Reduction of horizontal and vertical dimensions
  - Improved performance of planar transistors
- 2000 – 2025: Equivalent scaling
  - Reduction of only horizontal dimensions
  - Introduction of new materials and new physical effects
  - New vertical structures replace the planar transistor
- 2025 – 2040: 3D scaling
  - Transition to complete vertical device structures
  - Heterogenous integration
- Our current bag of innovations can keep CMOS alive till 2040!

[P. Gargini, IRDS, Intel]

Levels of Abstraction



(a)



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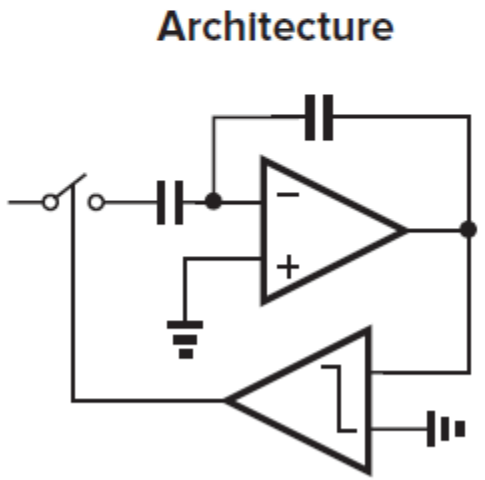

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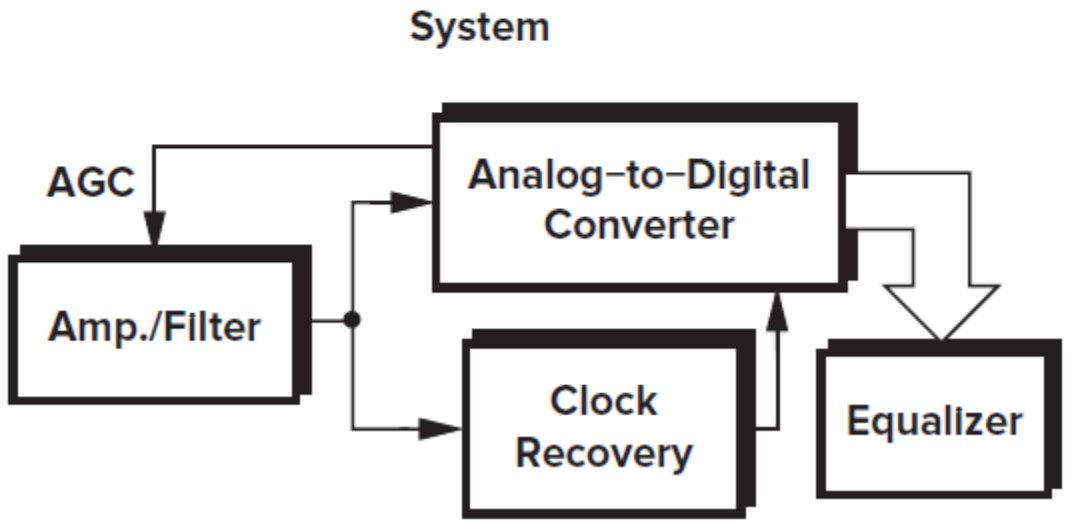


(d)

[Razavi, 2017]

IC Industry in Egypt

Mentor Graphics

SIEMENS

Si-WARE SYSTEMS

Si-VISION INNOVATIVE IC SOLUTIONS

GOODiX

ANALOG DEVICES

Wasiela

Axxcelera BROADBAND WIRELESS

life.augmented

infinilink

PULSAR microelectronics

Seamless Waves Semiconductors

MEMS VISION

ScenariO your brain extension

Cpedia

mixel Mixed-Signal Excellence

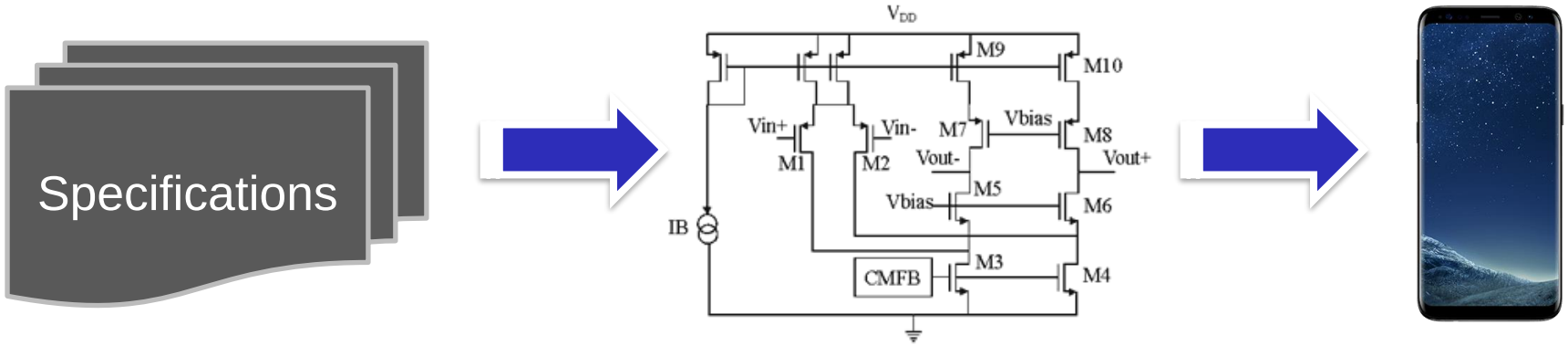
MASTER MICRO

Pearl Semiconductor

vidatronic egypt

Course Objective

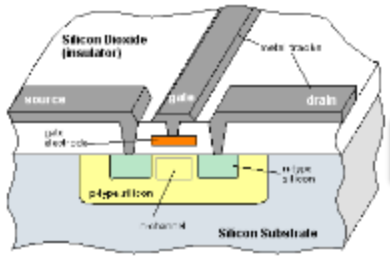
- To teach the basic knowledge required for
  - Analog IC analysis and design using CMOS technology
  - Moving from specifications (specs) to block design
  - **Simulating analog ICs using professional CAD tools**



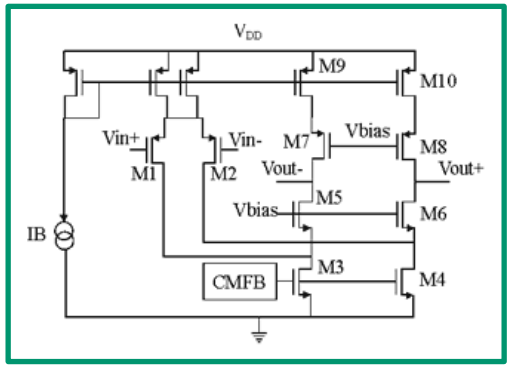
Your Learning Journey

Material

Devices

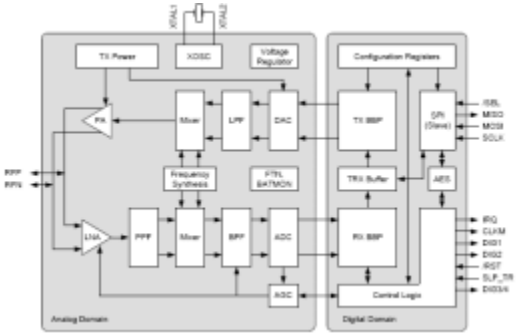


Circuits



Product

System



Course Prerequisites

- You should be familiar with
  - Analysis of electrical circuits
  - Basic semiconductor physics
  - Basic MOSFET operation and physics
  - MOSFT large signal and small signal models
  - Basic analysis of transistor amplifiers
- A review will be provided for all of the above topics
  - But you will struggle if you have never heard about these topics before

References

- Textbook
  - B. **Razavi**, "Design of analog CMOS integrated circuits," 2nd ed., McGraw-Hill Ed., 2017.

- References for beginners
  - A. **Sedra** and K. **Smith**, "Microelectronic circuits," 7th ed., Oxford University Press, 2015.
  - T. **Floyd,** "Electronics Fundamentals, Circuits, Devices, and Applications," 8th ed., Pearson, 2014.
  - B. **Razavi**, "Fundamentals of microelectronics," 2nd ed., Wiley, 2014.

References

- References for professionals
  - T. C. **Carusone**, D. **Johns**, and K. W. **Martin,** "Analog integrated circuit design," 2nd ed., Wiley, 2012.
  - P. **Gray**, P. Hurst, S. Lewis, and R. **Meyer**, "Analysis and design of analog integrated circuits," 5th ed., Wiley, 2009.
  - P. **Jespers** and B. **Murmann**, "Systematic design of analog CMOS circuits using pre-computed lookup tables," Cambridge University Press, 2017.
  - R. J. **Baker**, "CMOS circuit design," 3rd ed., Wiley, 2010.
  - W. **Sansen**, "Analog design essentials," Springer, 2006.

Canvas

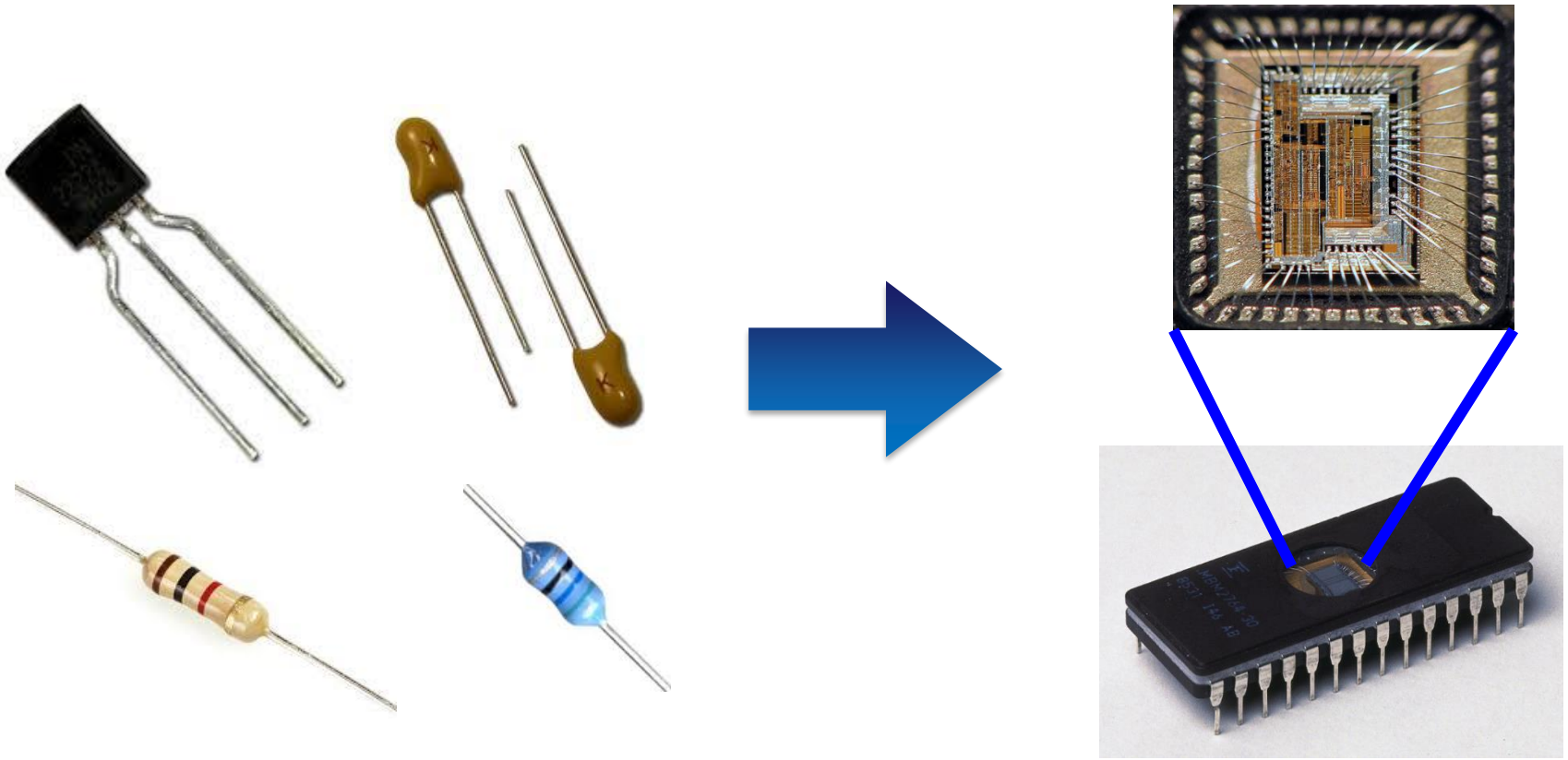
- Canvas is a learning management system (LMS) used in many universities in the US and around the world
- We will use Canvas for
  - Posting lectures, notes, etc.
  - Questions and answers
  - Announcements and discussions
  - Quizzes
  - Submitting and grading assignments, reports, etc.
  - And more!
- **Every student must register at Canvas today!**
- Contact me through Canvas, only in emergency contact me by email: Hesham.Omran@eng.asu.edu.eg

Feedback

- Don’t hesitate to send me feedback to improve the course quality.
- Avoid two common misconceptions
  1. Feedback should NOT wait to the end of the course!
     - It will be too late to improve anything!
     - But anyway, you may still help next generations ☺
  2. Feedback should NOT be always negative!
     - Too much negative feedback leads to zero output!
     - Too much positive feedback causes oscillation!
     - Be balanced!

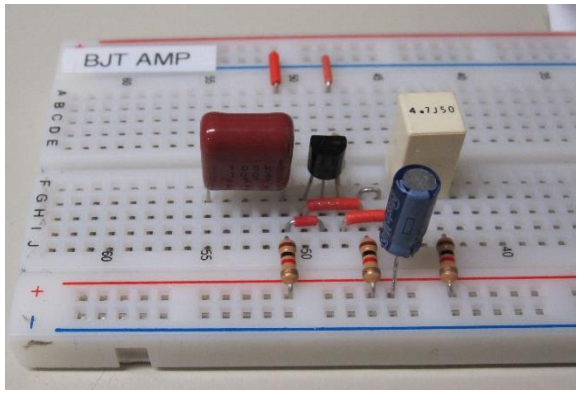
What is an Integrated Circuit (IC)?

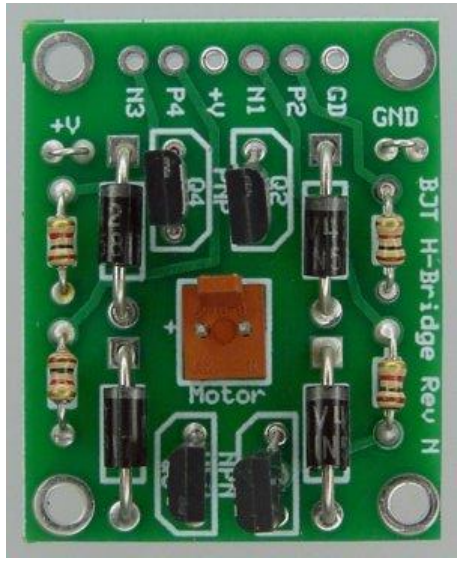
- Various circuit elements: transistors, capacitors, resistors, and even small inductances can be integrated on one chip

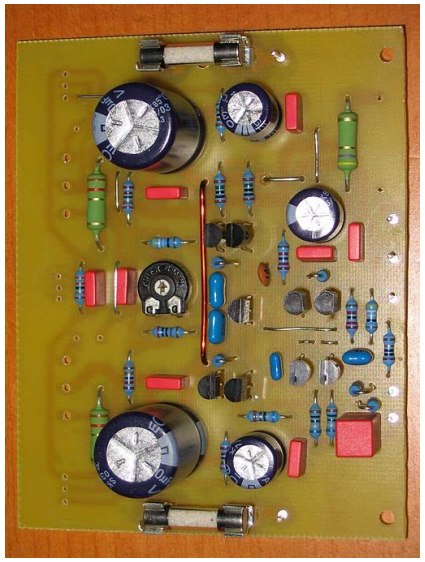


Discrete vs. Integrated Electronics

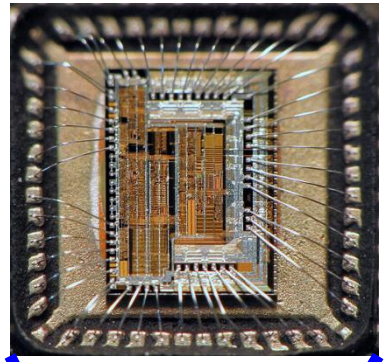
Circuits using discrete components

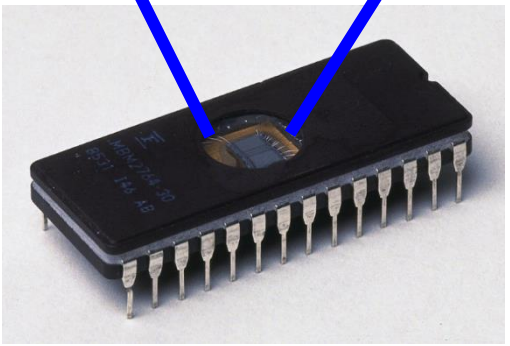






Integrated circuit



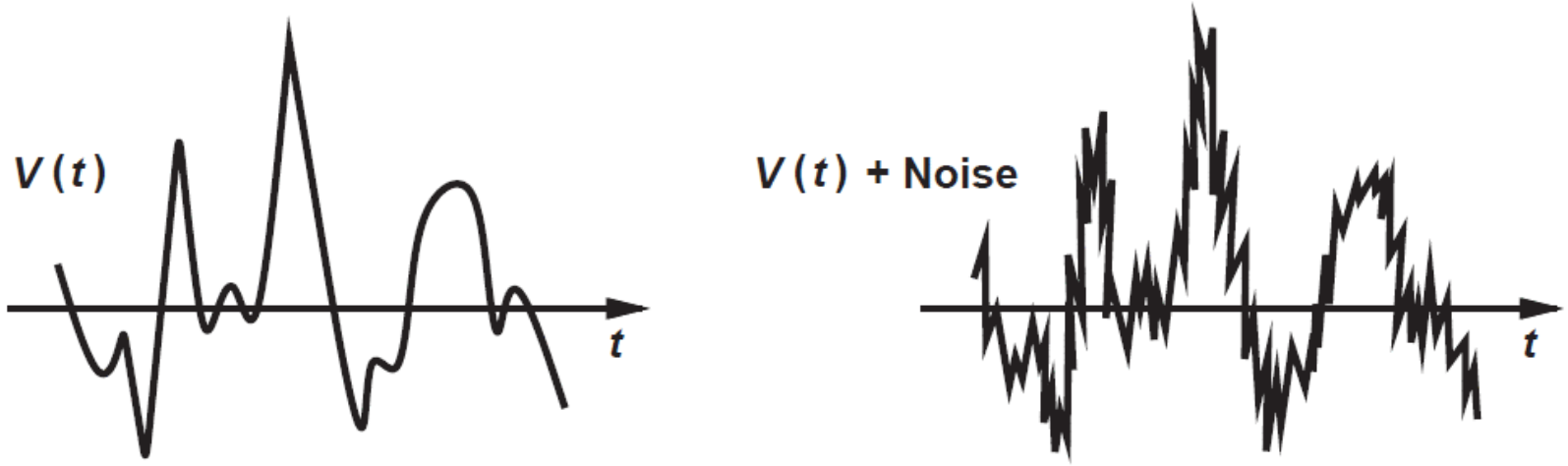


Integrated Circuit Components

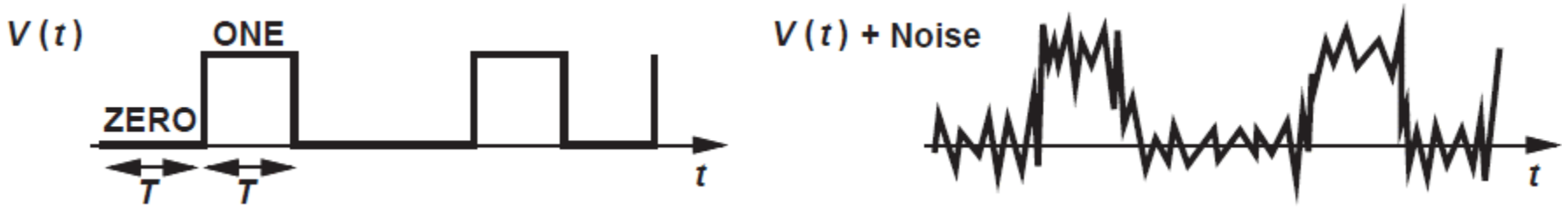
- Transistors:
  - Billions of tiny transistors can be integrated on the same chip
  - Very Large Scale Integration (VLSI): > 10,000 transistors
- Capacitors:
  - Capacitors as large as 100s of pF can be integrated on-chip
  - But they consume a lot of chip area → Use sparingly
- Resistors:
  - Resistors as large as few MOhms can be integrated on-chip
  - But they consume a lot of chip area → Use sparingly
- Inductors:
  - Small inductors (few nH) can be integrated on-chip
  - But they consume a lot of area with relatively poor performance → Use only in high frequency circuits (e.g., RFICs, serial links, etc.)

Analog vs Digital Signals

- Analog: continuous in time and amplitude



- Digital: discrete in time and amplitude



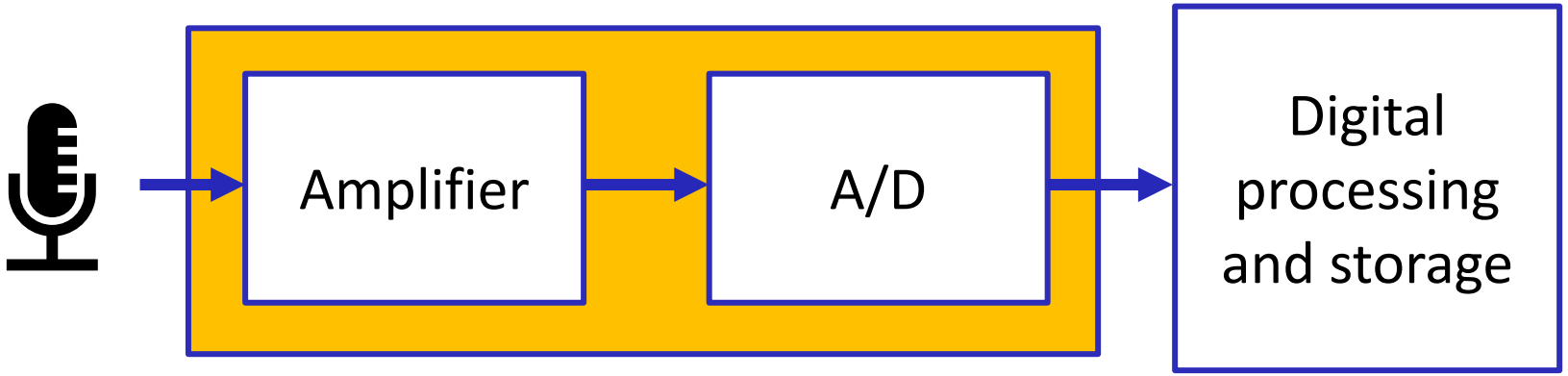
[Razavi, 2014]

Why Digital?

- Digital circuits are
  - Less sensitive to noise (robust)
  - Easier to store (digital memories)
  - Easier to process (digital signal processing: DSP)
  - Amenable to automated design
  - Amenable to automated testing
  - Easier to port from one technology to another
  - Direct beneficiary of Moore's law (down-scaling)

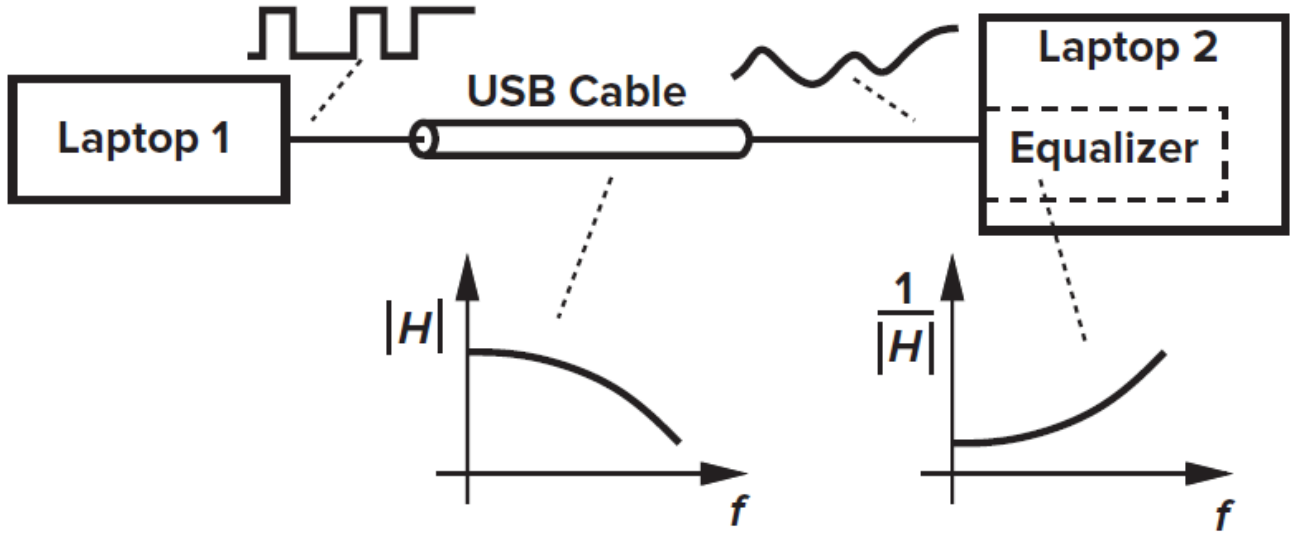
Why Analog?

- All the physical signals in the world around us are analog
  - Voice, light, temperature, pressure, etc.
- We (will) always need an “analog” interface circuit to connect between our physical world and our digital electronics
- There will always be jobs for analog/mixed-signal/RF designers ☺



Why Analog?

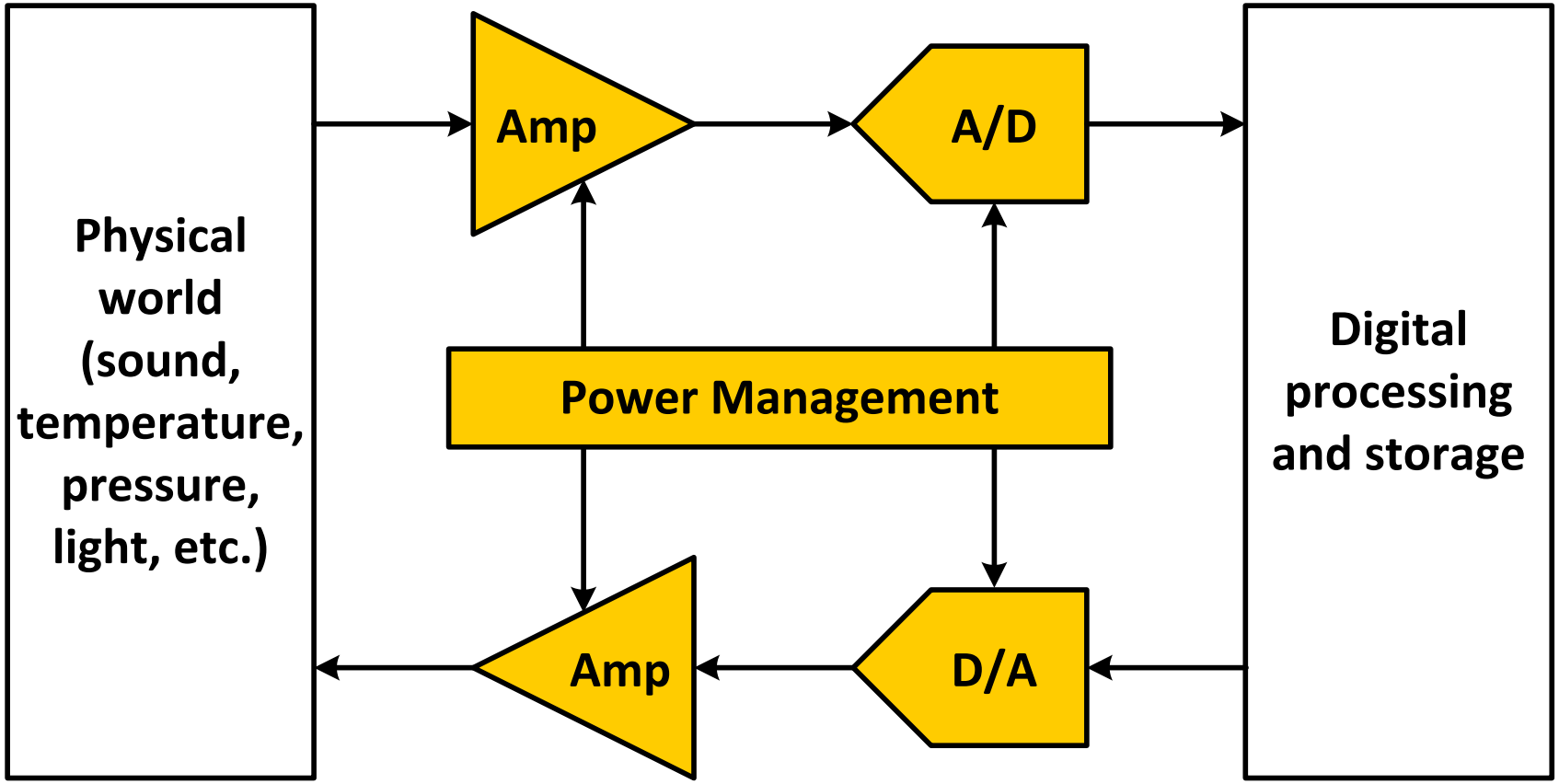
- High speed digital design is actually analog design!
- At low speeds, we may directly digitize the signal and perform the signal processing in the digital domain.
- At high speeds, signal processing in the analog domain is much more energy efficient.
- The boundary between high and low speed has risen over time.



[Razavi, 2017]

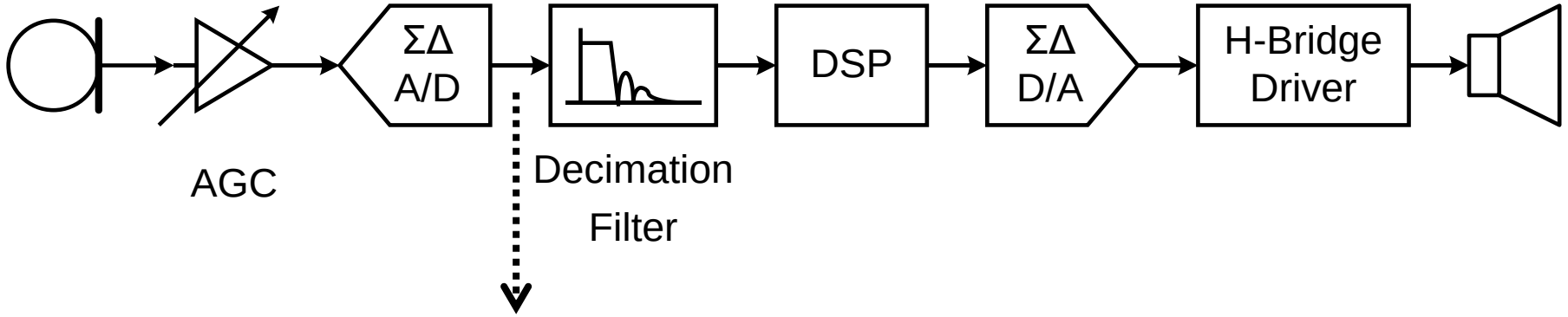
Signal Processing Chain

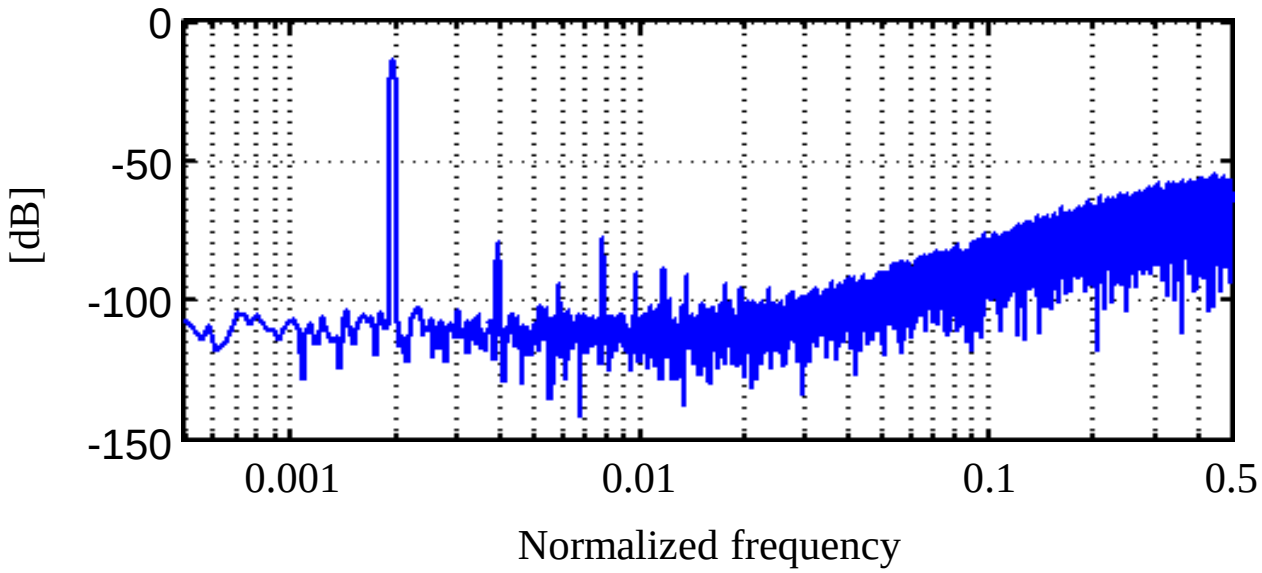
- There will always be jobs for analog/mixed-signal/RF designers ☺



Example: Mixed-Signal Hearing Aid

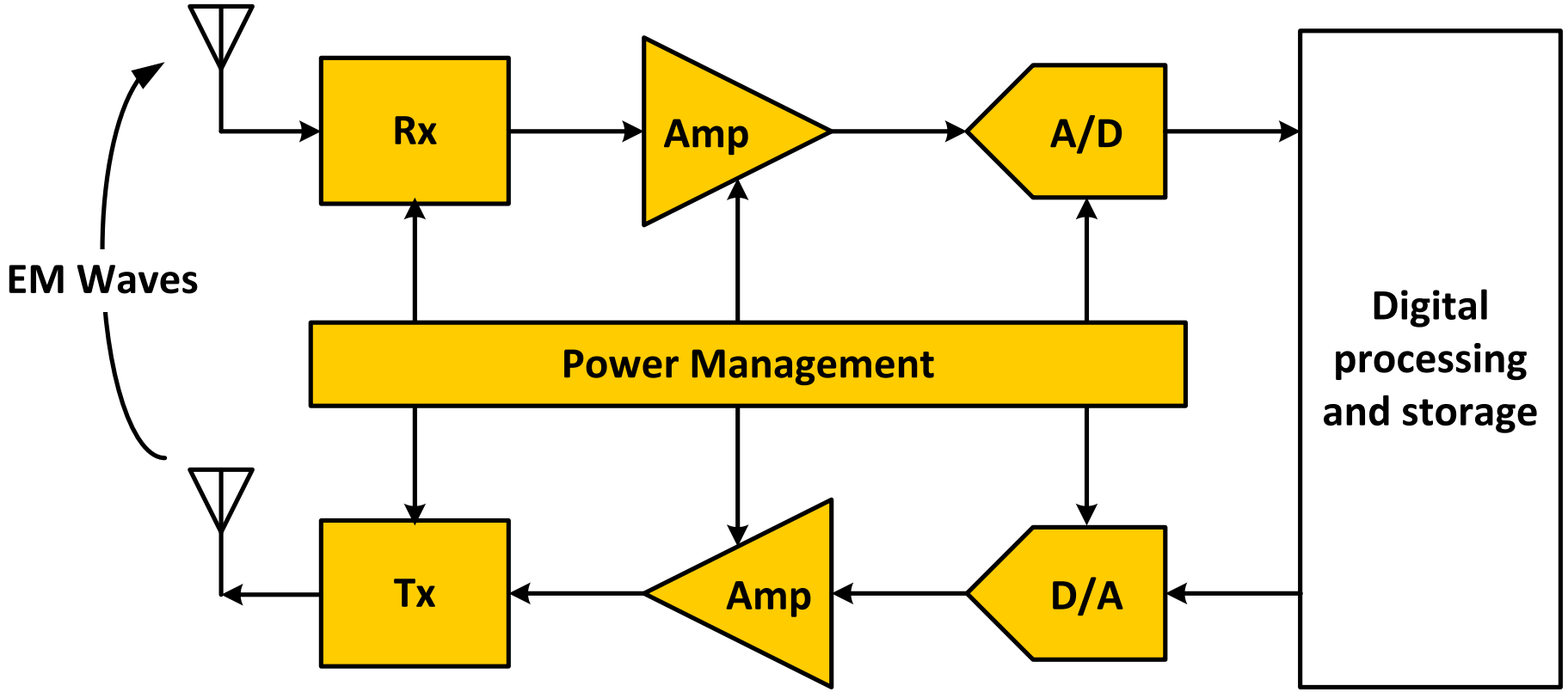
- There will always be jobs for analog/mixed-signal/RF designers ☺





Wireless Signal Processing Chain

- There will always be jobs for analog/mixed-signal/RF designers ☺



Why CMOS?

- Early integrated circuits primarily used bipolar transistors (BJTs)
- CMOS technologies dominated the digital market since the 1980s

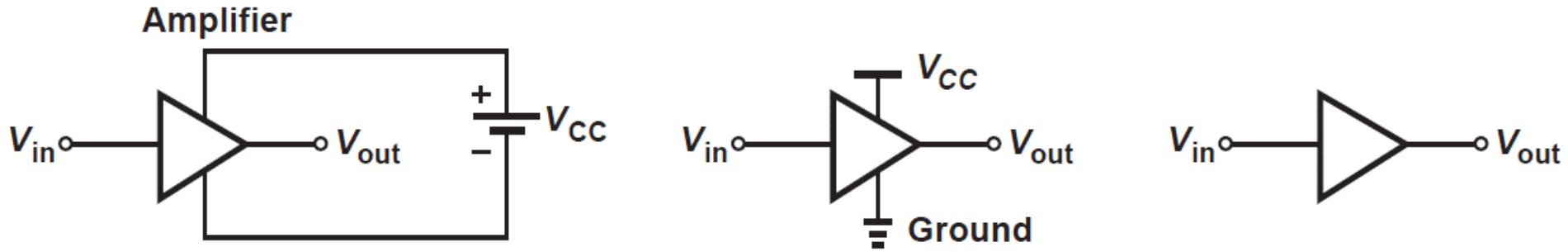
  → CMOS = Complementary MOS = NMOS + PMOS

  1. Consumed negligible static power
     - Was indeed negligible in the past
     - But not negligible any more…
  2. Required very few devices per gate
  3. Can be scaled down more easily
  4. Lower fabrication cost
- For analog design, BJTs used to be much better than MOSFETs
  - Faster, less noisy, less variations, more energy efficient, higher gain
- Then why analog CMOS?

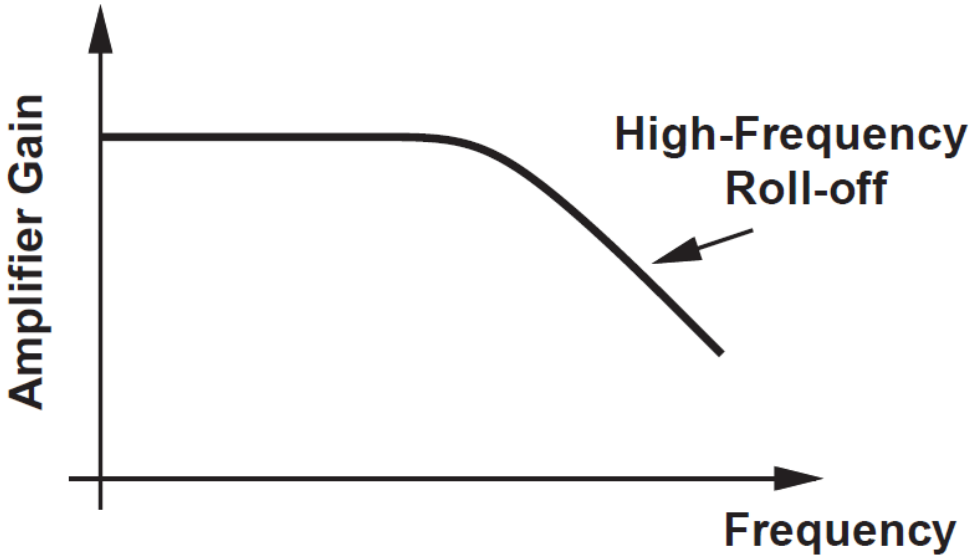
Why Analog CMOS?

- ICs market is driven primarily by memories and microprocessors
  - The analog designer needs to survive in a digital driven market
- We want to integrate analog and digital on the same chip
  - Mixed-signal design and system-on-a-chip
- BJTs used to be faster, but with continuous scaling, MOSFET speed exceeded BJT
- MOSFET can operate with lower supply voltage

Analog Amplifier



- The amplifier has finite gain ($A_v = \frac{v_{out}}{v_{in}}$) and finite bandwidth (speed)



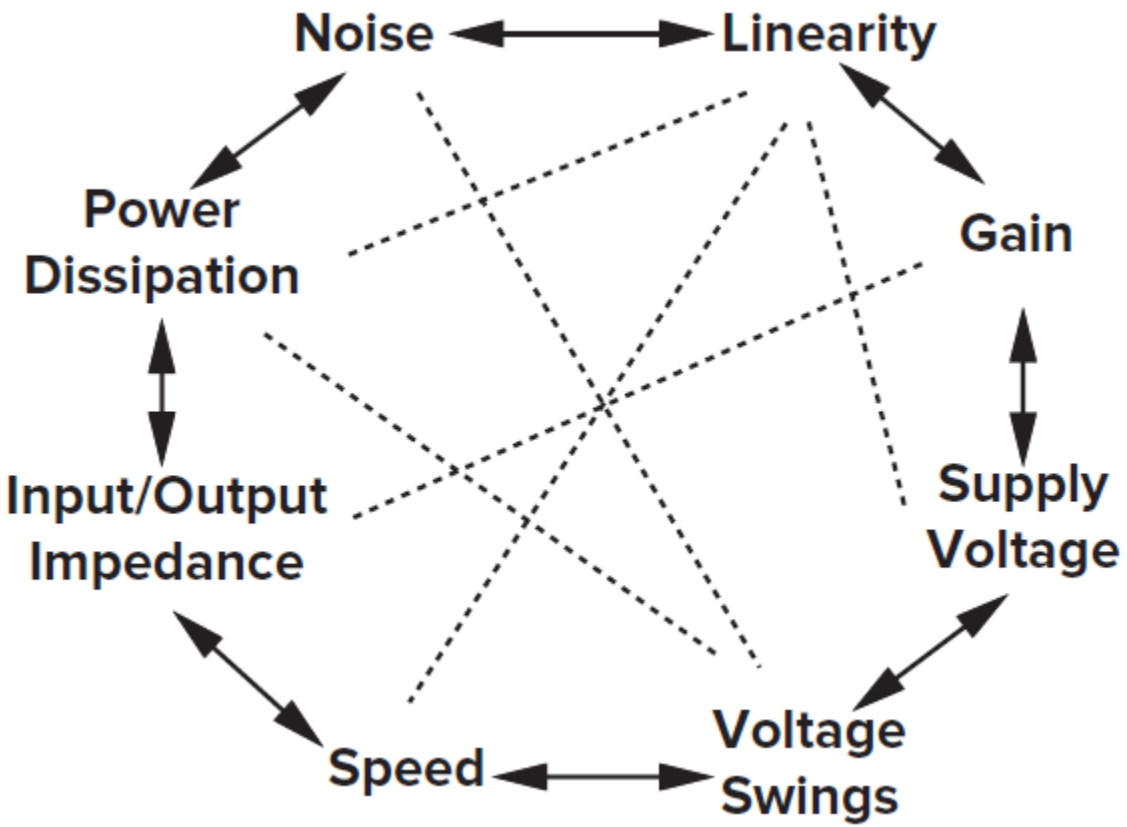
[Razavi, 2014]

Analog IC Design Challenges

- Device scaling
  - Transistors become faster, but the gain declines
- Supply voltage scaling
  - From 12V in 1970s to less than 1V nowadays
- Low power consumption
  - Increase battery lifetime, decrease cost and heat emissions
- Complexity
  - Continuous increase in transistor count and system complexity
- PVT variations
  - Tolerate large process, voltage, and temperature variations
- New applications
  - Wireless standards, wearables, IoT, serial links (e.g., USB), power management

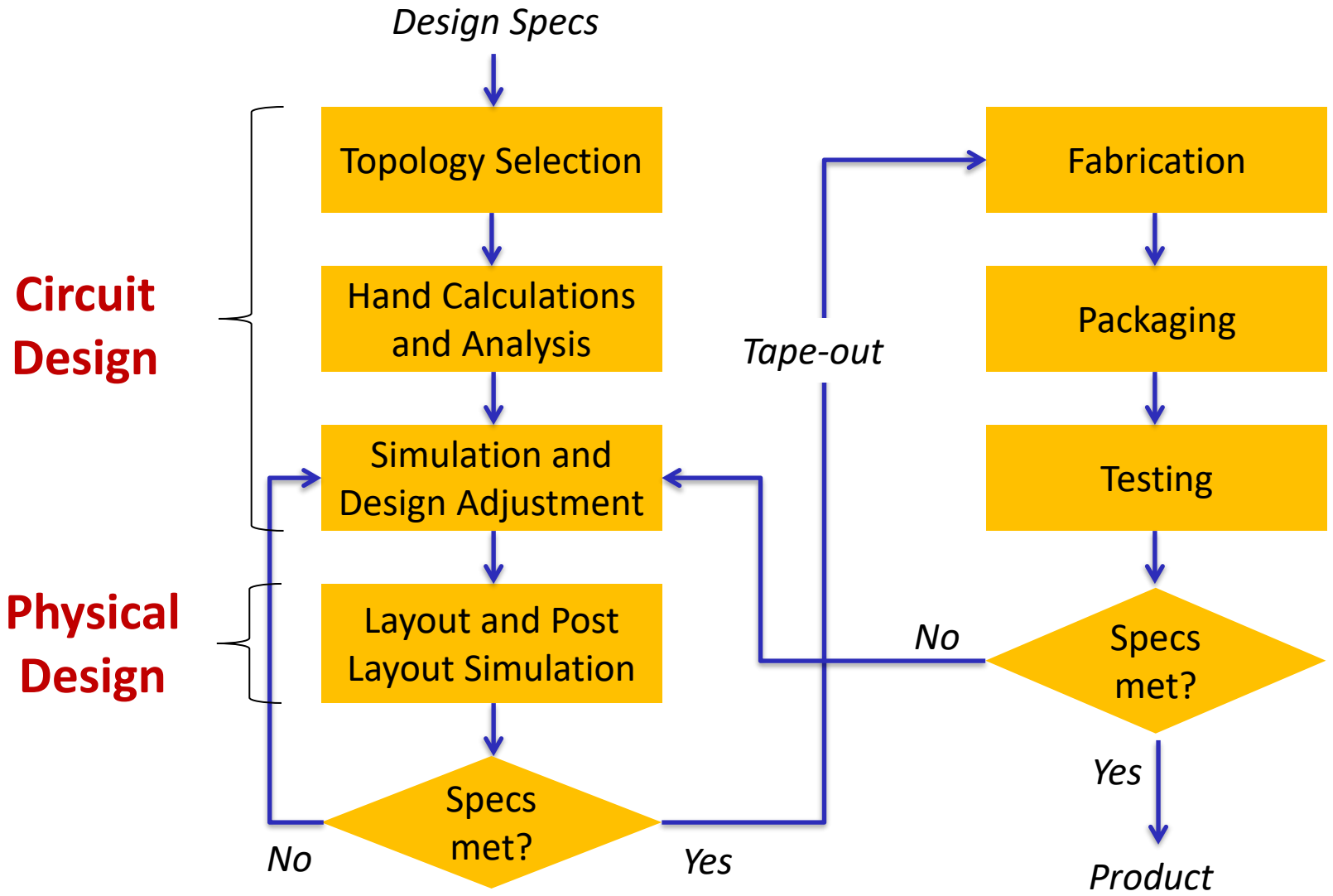
Analog IC Design Challenges

- In digital we have PPA
- In analog, we need to worry about many more things
  - Analog design automation is a difficult task



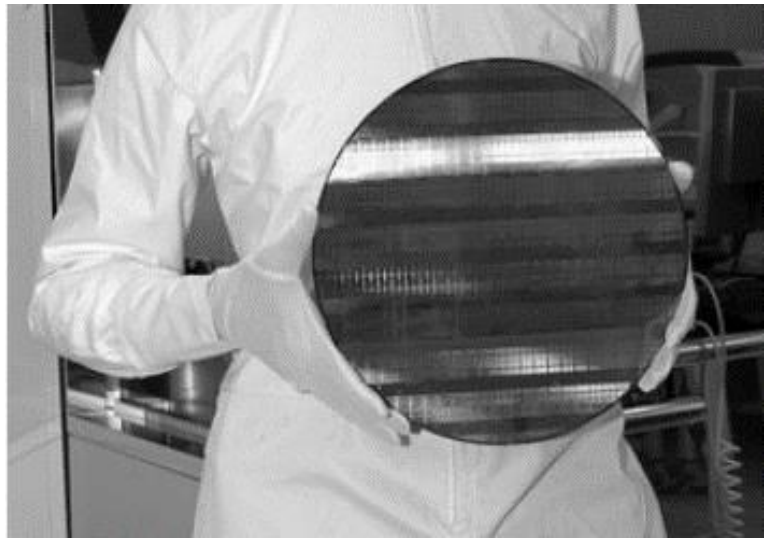
[Razavi, 2017]

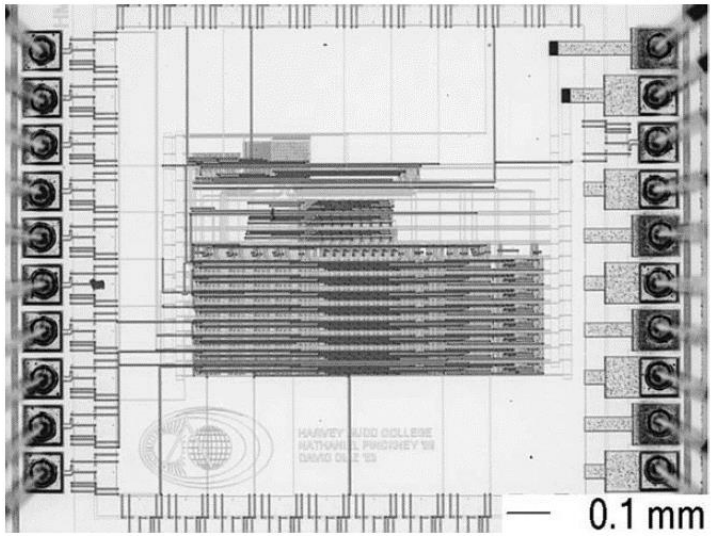
Analog IC Design Flow (Simplified)



Tape-Out

- The layout is sent to the fab in a format called GDS II
  - Previously it was sent on a magnetic tape → tape-out
  - Now by email (small design) or FTP (large design)

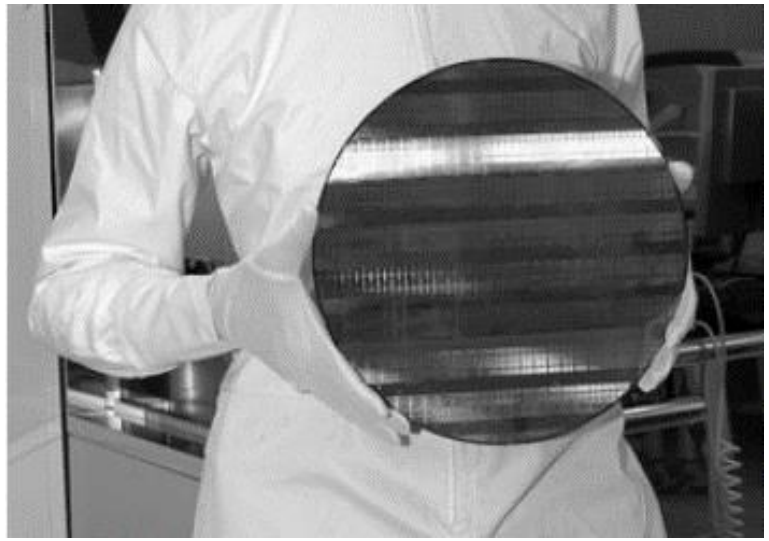


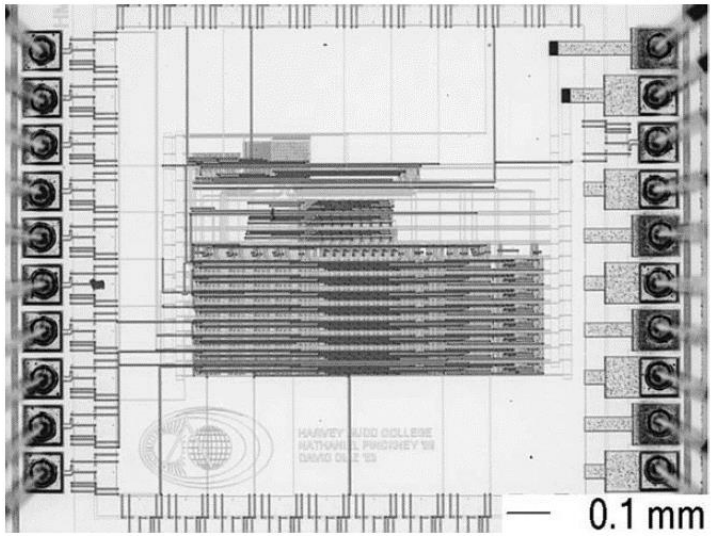


[Weste and Harris, 2010]

MPW

- ICs are fabricated on silicon wafers
  - Turnaround time ~ 3months
- A fabrication run in 65nm process costs about $3 million
  - Cost sharing using MPW (multi-project wafer)
    - US: MOSIS
    - Europe and MENA: Europractice





[Weste and Harris, 2010]

MPW Example

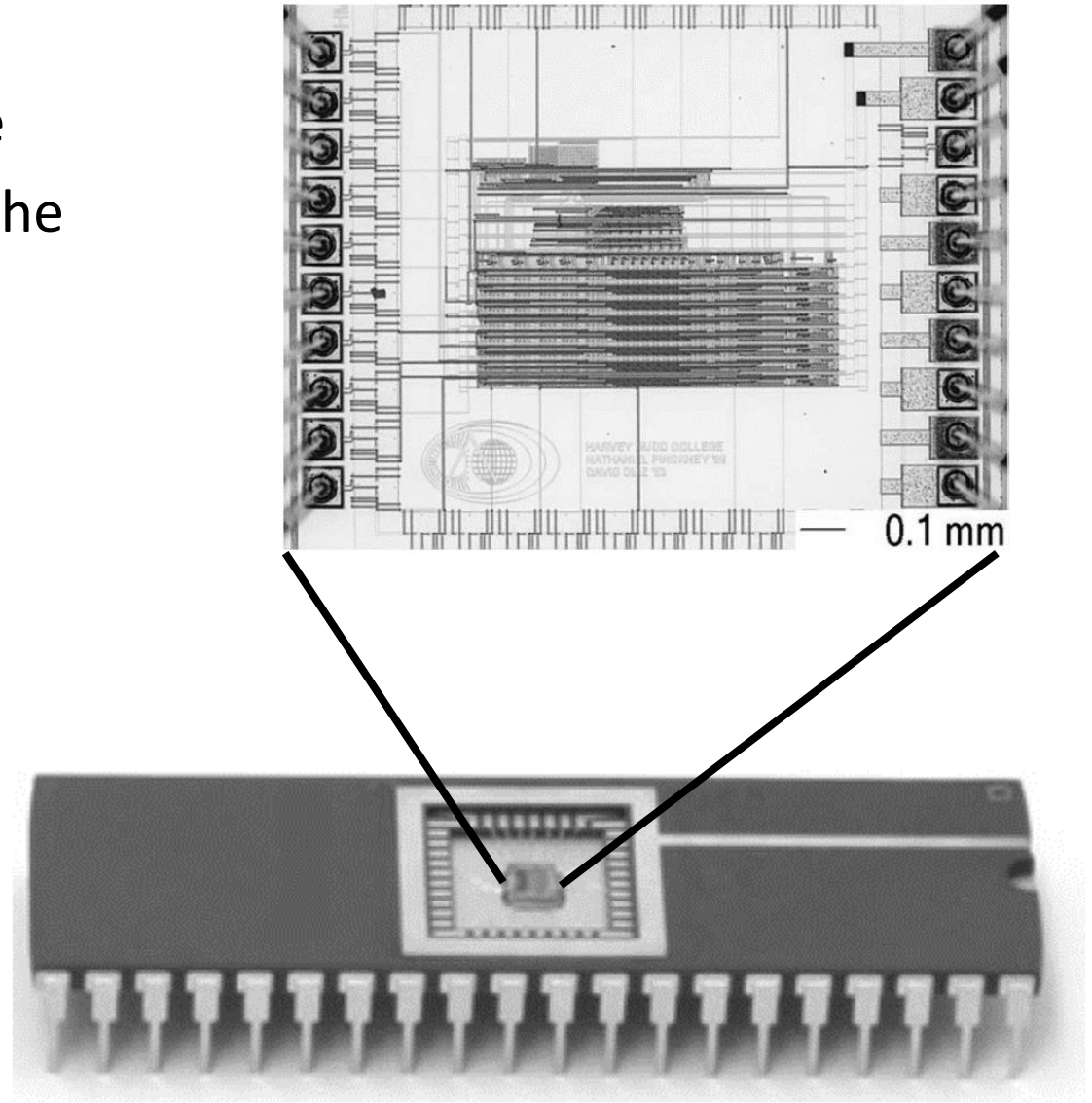
- Link: http://www.europractice-ic.com/general_runschedule.php
- Foundries include TSMC, UMC, GLOBALFOUNDRIES, …
- < 50 samples only!
- Example:

GLOBALFOUNDRIES	J	F	M	A	M	J	J	A	S	O	N	D
GLOBALFOUNDRIES 130nm BCDlite	2		5	30			2		3		5	
GLOBALFOUNDRIES 130 nm LP	2		5	30			2		3		5	
GLOBALFOUNDRIES 55 nm LPe/LPx-NVM/LPx-RF	8		12		14		9		10		12	
GLOBALFOUNDRIES 40 nm LP/LP-RF/RF-mmWave	29			3		4		6		1		3
GLOBALFOUNDRIES 28 nm SLP/SLP-RF		5			2			6			5	
GLOBALFOUNDRIES 22 nm FDSOI	8	12	12	16	14	11	16	13		8	12	17

GLOBALFOUNDRIES	STANDARD Price/mm^2
GLOBALFOUNDRIES 130 nm BCDlite	1500 [11]
GLOBALFOUNDRIES 130 nm LP	1500 [11]
GLOBALFOUNDRIES 55 nm LPe/LPx-NVM/LPx-RF	4000 [11]
GLOBALFOUNDRIES 40 nm LP/LP-RF/RF-mmWave	5000 [11]
GLOBALFOUNDRIES 28 nm SLP-RF	10200 [11]
GLOBALFOUNDRIES 22 nm FDX FDSOI	14000 [11]

Packaging and Testing

- Wafer diced into dies
- Gold bond wires from die I/O pads to package
- Packaging is now much more advanced than the simple DIP (dual inline package)



[Weste and Harris, 2010]

Thank you!

References

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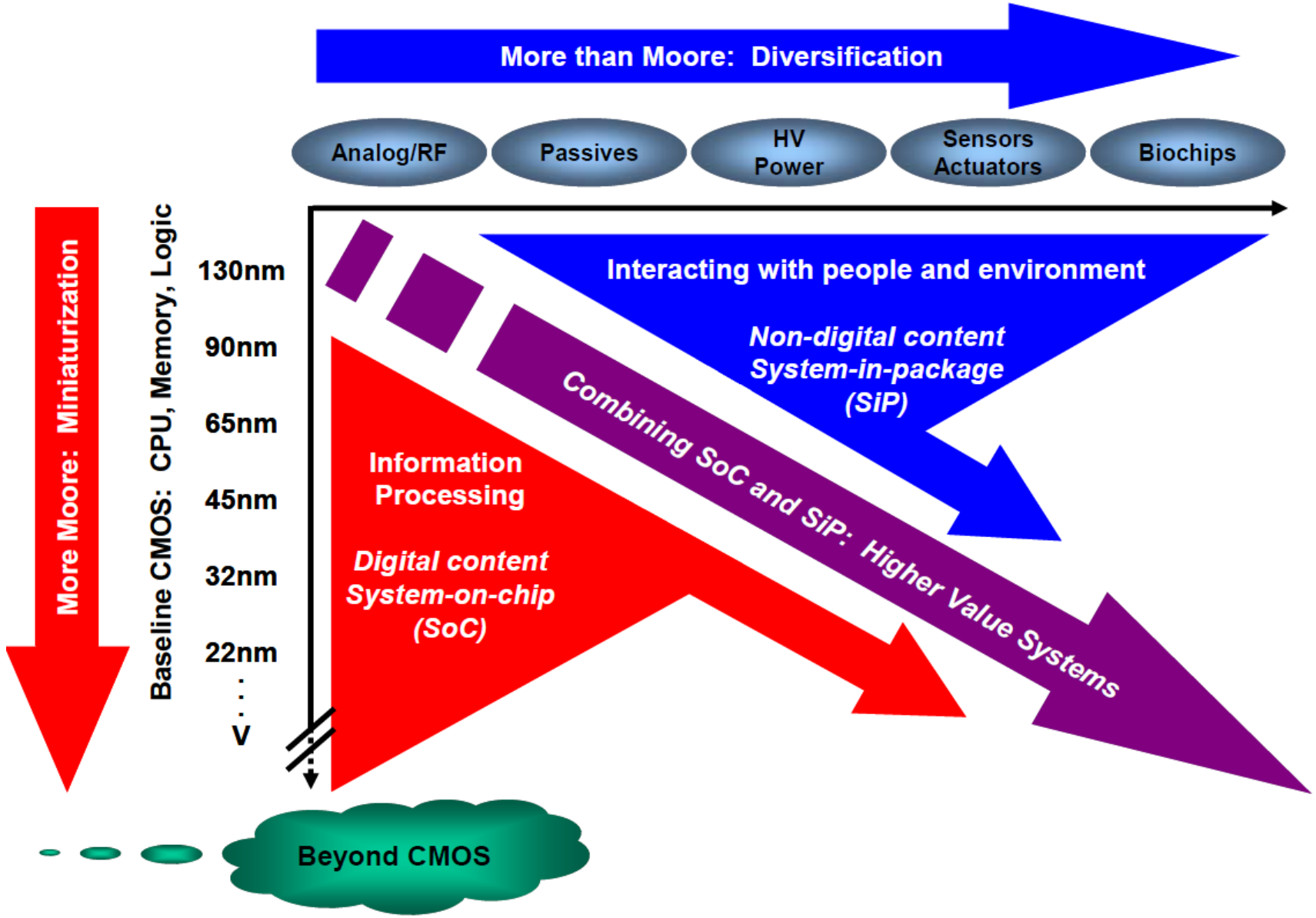
- B. Razavi, “Fundamentals of Microelectronics,” Wiley, 2nd ed., 2014.
- B. Razavi, “Design of Analog CMOS Integrated Circuits,” McGraw-Hill, 2nd ed., 2017.
- N. Weste and D. Harris, “CMOS VLSI Design,” Pearson, 4th ed., 2010.

Modern “Moore” Concepts

- **More Moore**
  - Further miniaturization of transistor as per Moore’s law
  - New materials for performance enhancement (HK, SOI, III-V)
  - We are approaching the “physical limits” of the transistor
- **More than Moore**
  - Adding functionalities **not** associated with transistor scaling to increase device value (sensors, MEMS, bio, passives, etc.)
  - 3D integrated circuits
- **Beyond Moore (Beyond CMOS)**
  - Exploring new device architectures
  - Gate-all-around transistors, nanowires (NW-FET), nanotubes (CNT), memristors, spin electronics, graphene, etc.

Modern “Moore” Concepts



[Wolfgang Arden et. al., ITRS]

IC Technology Generations

- Early integrated circuits primarily used bipolar transistors (BJTs)
- 1960s: MOS ICs became attractive for their low cost
  - MOS transistor occupied less area
  - The fabrication process was simpler
  - Early commercial processes used only PMOS transistors and suffered from poor performance, yield, and reliability
- 1970s: Processes using only NMOS transistors became common
- Digital circuits in all the previous technologies have quiescent power
  - Power is dissipated when the circuit is idle, i.e., not switching
  - This limits the maximum number of transistors that can be integrated on one die

IC Technology Generations (Cont'd)

- 1980s: The VLSI era
  - Power consumption became a major issue
  - CMOS processes were widely adopted and replaced NMOS and bipolar processes for nearly all digital logic applications

    → CMOS = Complementary MOS = NMOS + PMOS
  - A key advantage for "digital" CMOS is that it has negligible idle (static) power consumption
- Nowadays:
  - With aggressive scaling and billions of transistors, CMOS idle leakage current is not negligible any more
  - But no better technology is available yet…

How to Design a Billion Transistor Chip?

1. Abstraction
   - Hiding details until they become necessary
2. Structured design
   - Hierarchy: Block, sub-blocks, … → Tree structure (from root to leaf cells)
   - Regularity: Min no. of different blocks → Block reuse (e.g., standard cells)
   - Modularity: Blocks are black boxes that have well-defined interfaces → Combine to build larger system without surprises!
3. CAD Tools
   - Automation, automation, automation!
   - Analog automation is way behind digital automation

CAD/EDA

- **Analog design**
  - **Design entry (schematic), simulation, layout**
  - **Verification (LVS: layout vs schematic, DRC: layout design rule check, parasitic extraction, post-layout simulation)**
- Digital design
  - Design entry (e.g., HDL) and simulation
  - Automated synthesis (from HDL to gates)
  - Automated place and route (from gates to transistor layout)
  - Verification
- System design
  - Behavioral modeling and high level simulation/verification
- EM simulation, process simulation, device simulation, etc.