وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

Analog IC Design

Lecture 21
Slew Rate (SR) and Power Supply Rejection (PSR)

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Outline

- Linear and non-linear settling
- SR examples
- Power supply rejection
- PSRR examples

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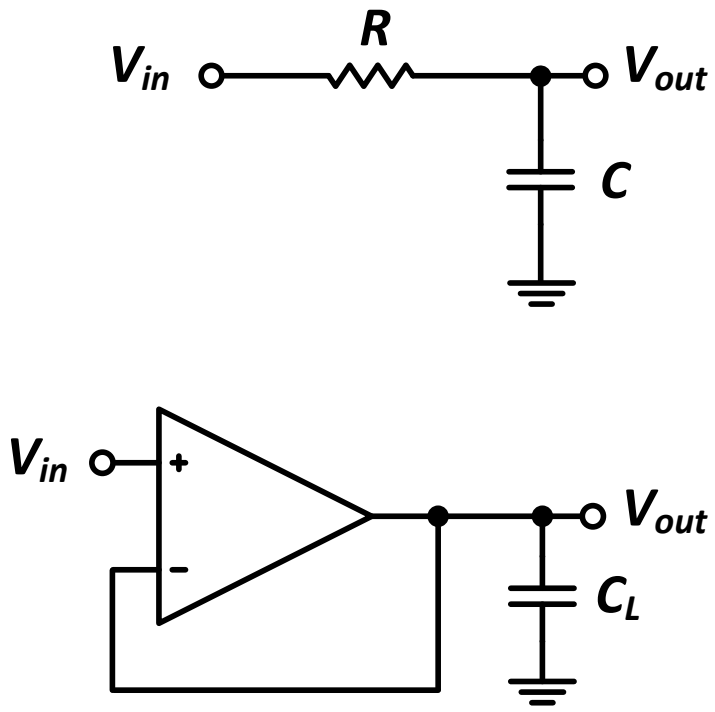
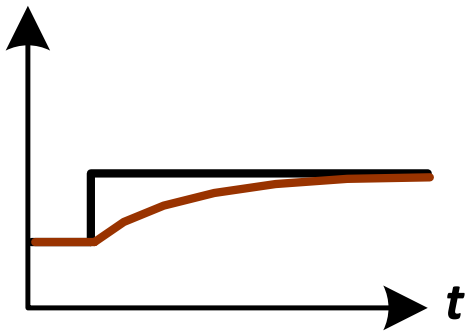
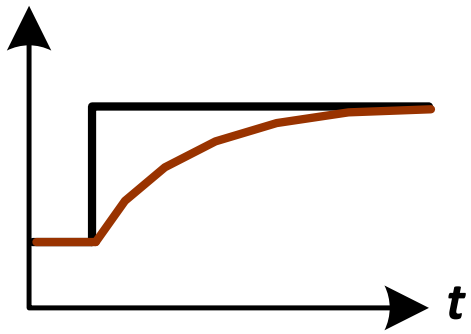
- Linear and non-linear settling
- SR examples
- Power supply rejection
- PSRR examples

Linear System

- One important property of linear systems: doubling the input doubles the output
  - More generally: scaling the input scales the output

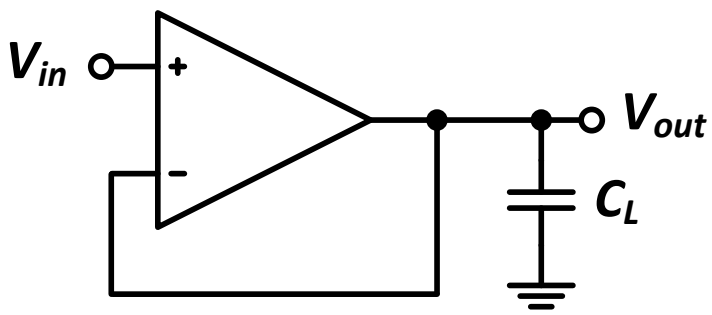


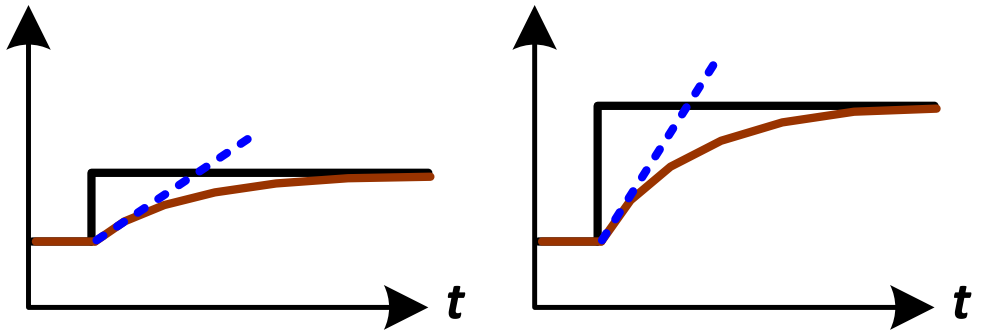




Linear Settling

- The system time constant (τ) do not depend on the input level
  - Need to settle to a higher voltage in the same time
  - Need larger slope
  - Need higher current!
- For linear systems: doubling the input doubles the output
  - The slope is also doubled!
- Linear settling: Scaling the input scales the output slope





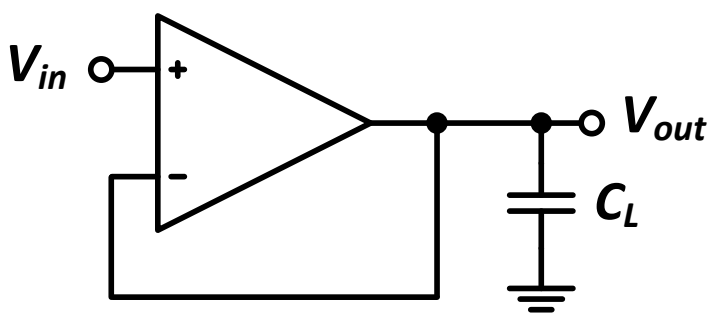
Linear Settling

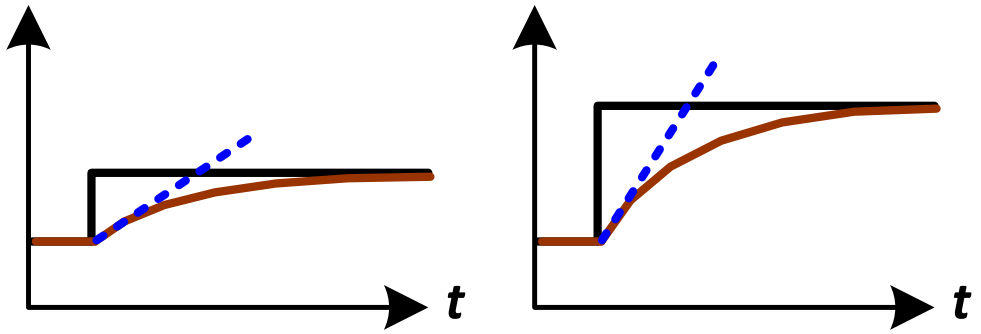
- **Linear settling:** Output slope and charging current ∝ input

$$V_{out} = V_{step}\left(1 - e^{-\frac{t}{\tau}}\right)$$

$$\frac{dV_{out}}{dt} = V_{step}\left(\frac{1}{\tau}e^{-\frac{t}{\tau}}\right) \quad \rightarrow \quad \frac{dV_{out}}{dt} \propto V_{step}$$

$$I_{out} = C_L\frac{dV_{out}}{dt} \quad \rightarrow \quad I_{out} \propto V_{step}$$



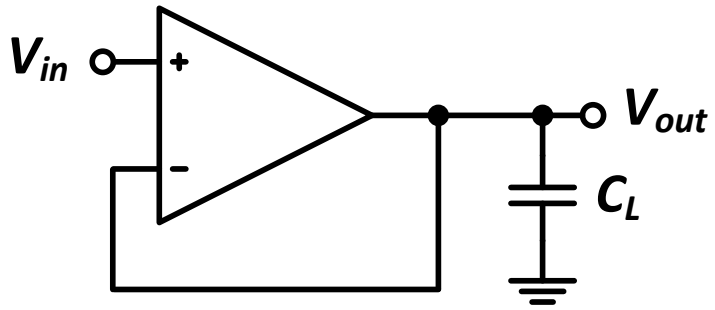


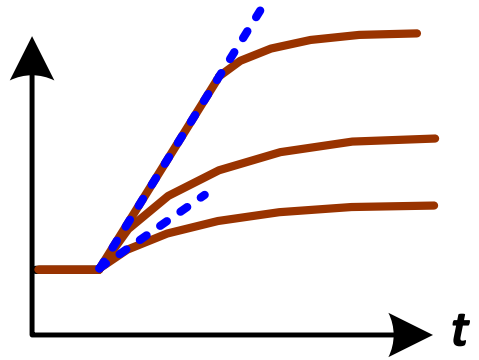
Non-linear Settling: Slewing

- **Non-linear settling:** Output slope and current **NOT** ∝ input
  - Output is linear ramp → finite constant slope
- Slew Rate (SR): the maximum possible slope of the op-amp output
- Linear ramp → constant current charging a capacitor

$$I_{out} = C_L \frac{dV_{out}}{dt} \quad \rightarrow \quad SR = \left(\frac{dV_{out}}{dt}\right)_{max} = \frac{I_{out,max}}{C_L} = const.$$

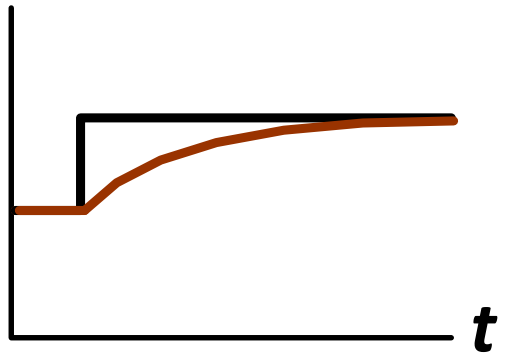
- Slope independent of the input level → non-linear behavior

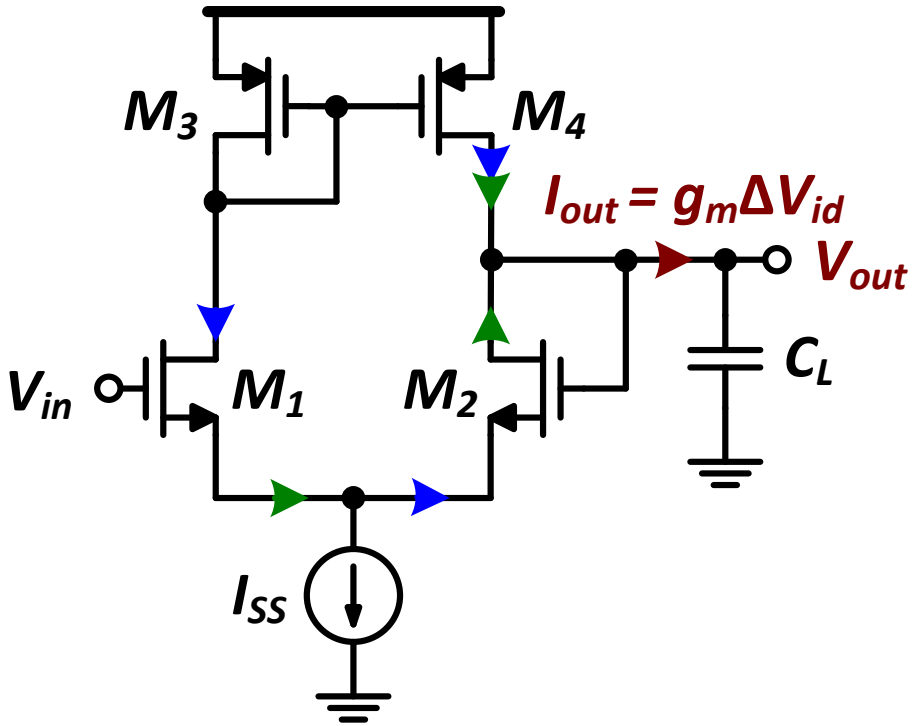




Small Input Step: Linear Settling

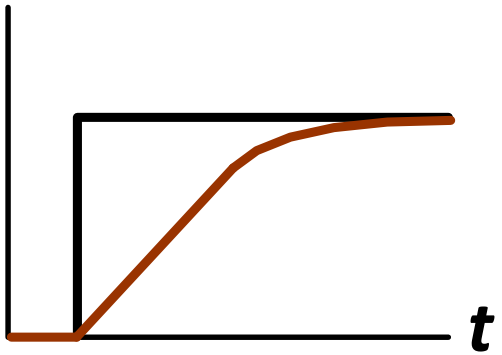
- **Linear settling:** Output slope and charging current ∝ input
- Output voltage has exponential settling behavior
- When the output settles → $\Delta V_{id} = V_{in} - V_{out} \approx 0$

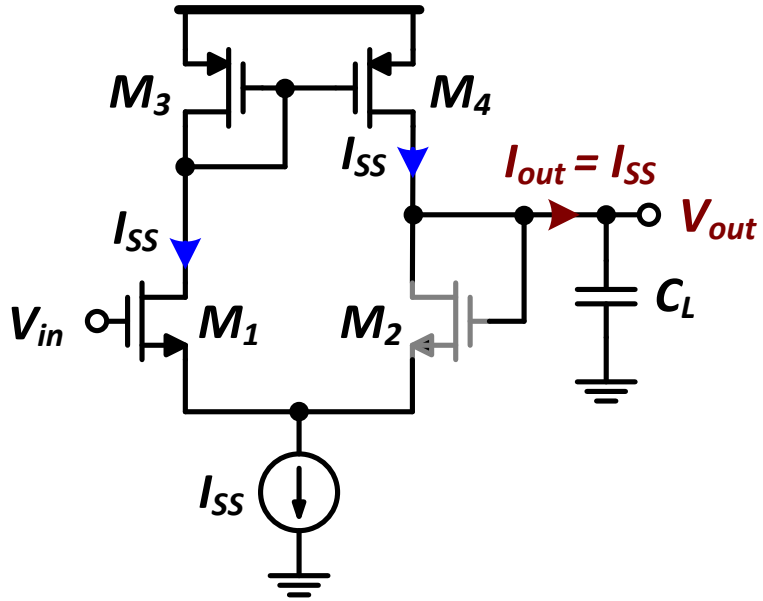




Large Input Step: Slewing

- M2 OFF, I_{SS} is fully steered to M1 → M3 → M4 then to C_L
- **Nonlinear settling:** output slope and charging current **NOT** ∝ input
  - Linear ramp → constant current (I_{SS}) charging a capacitor
- As V_{out} approaches V_{in} the circuit resumes linear settling (exp)
- $SR = \frac{I_{SS}}{C_L}$
- Efficiency ~ 100%



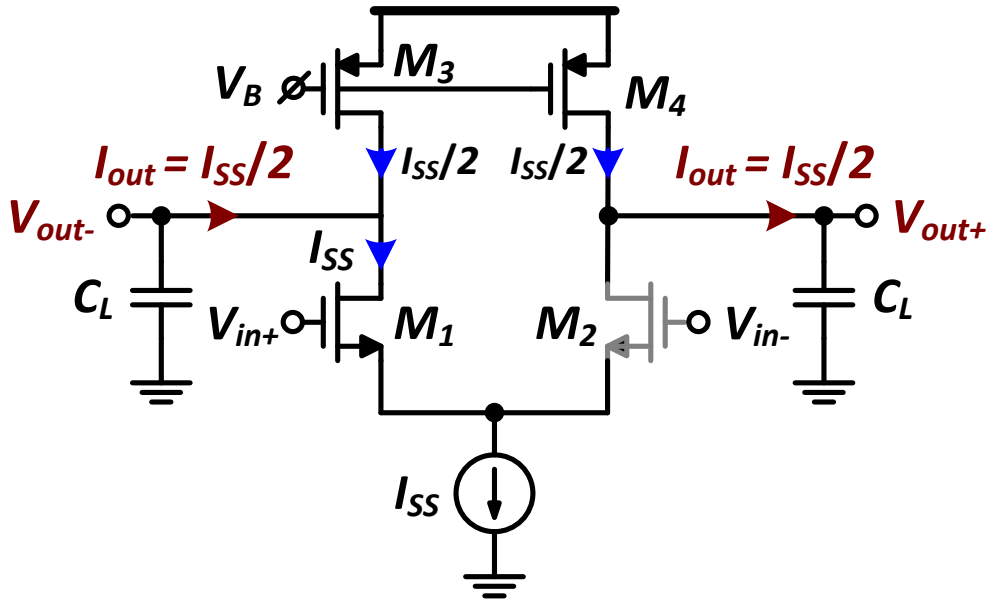


Outline

- Linear and non-linear settling
- SR examples
- Power supply rejection
- PSRR examples

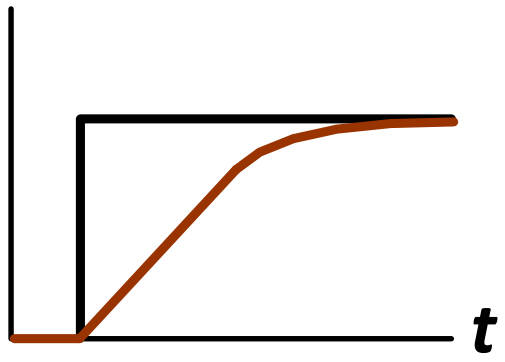
SR of FD OTA

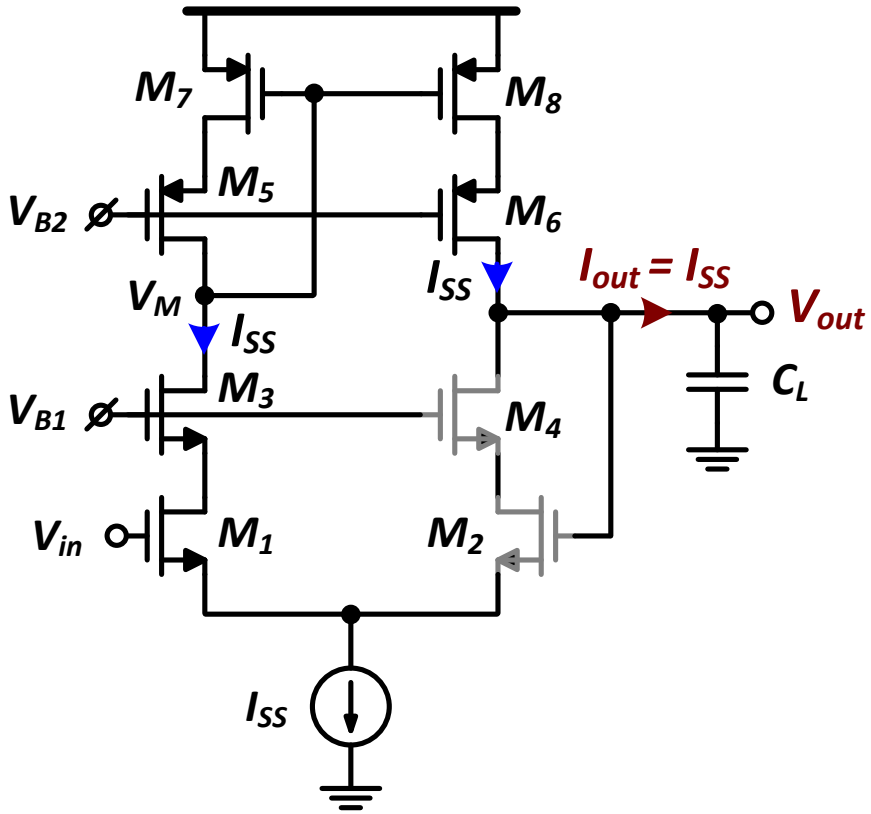
- $V_{out-}: SR = \frac{I_{SS}}{2}/C_L$
- $V_{out+}: SR = \frac{I_{SS}}{2}/C_L$
- $V_{outd} = V_{out+} - V_{out-}: SR = I_{SS}/C_L$
- Symmetrical slewing → Necessary to maintain constant CM level



SR of Telescopic Cascode

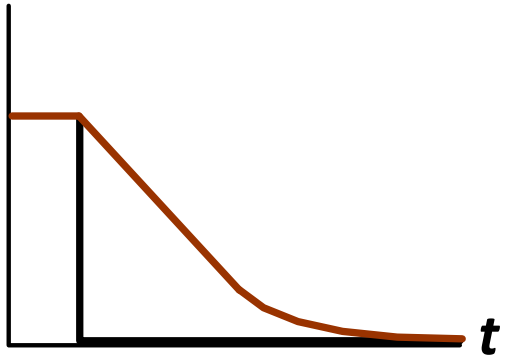
- $SR = \frac{I_{SS}}{C_L}$
- Efficiency ~ 100%

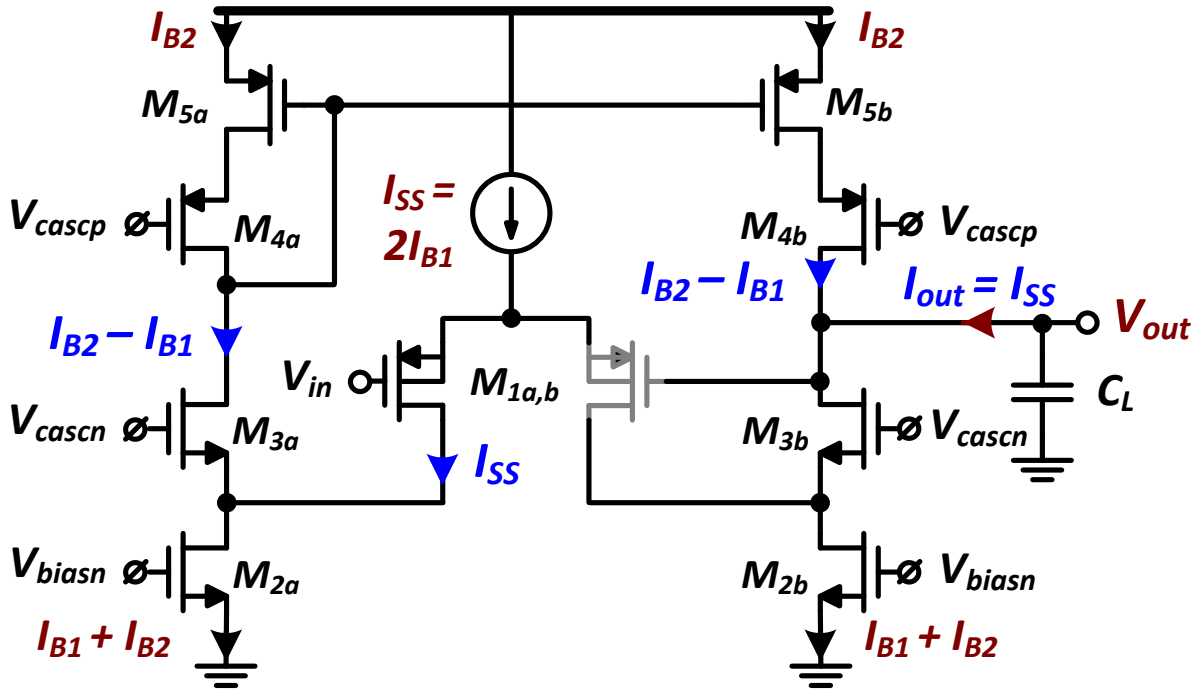




SR of Folded Cascode

- At equilibrium: Usually set $I_{DQ,CS} = I_{DQ,CG} \rightarrow I_{B1} = I_{B2}$
- At slewing: $I_{B2} \rightarrow I_{B2} - I_{B1} \approx 0$
- $SR = I_{SS}/C_L$
- Efficiency $\approx 50\%$





SR of Two-Stage Miller OTA

- I_{B2} is usually much larger than I_{B1}
  - SR usually limited by I_{B1}
- Internal slewing limits output slewing
- Positive slewing

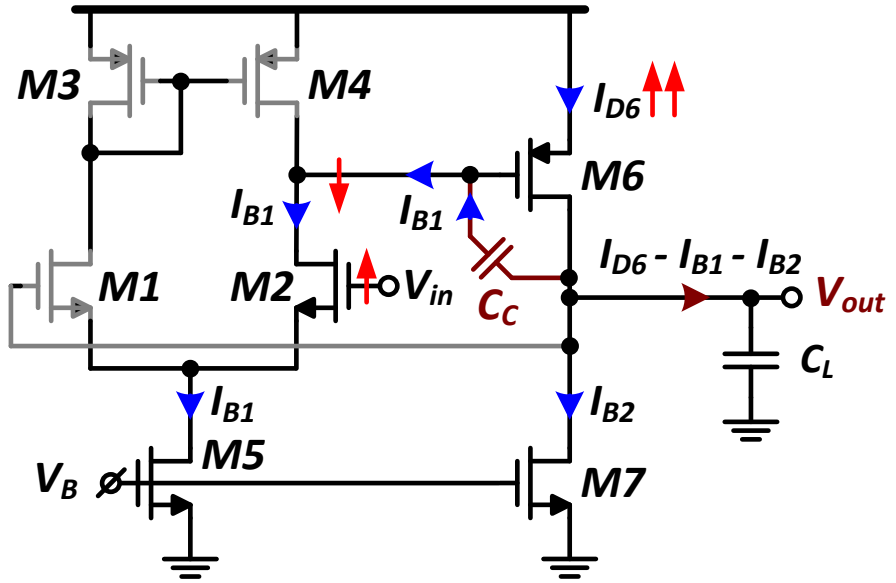
$$\frac{I_{D6} - I_{B1} - I_{B2}}{C_L} > \frac{I_{B1}}{C_1 + C_C}$$

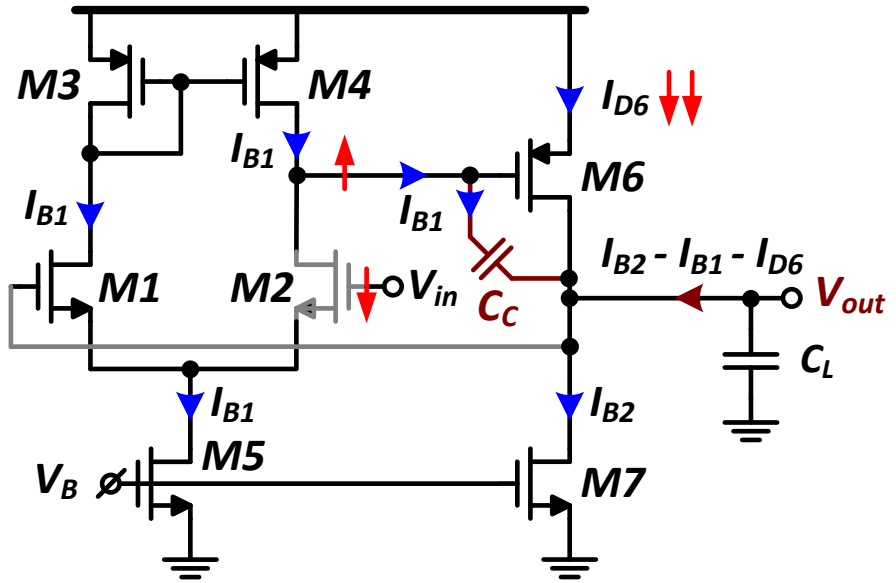
$$SR_+ \approx \frac{I_{B1}}{C_1 + C_C}$$

- Negative slewing

$$\frac{I_{B2} - I_{B1}}{C_L} > \frac{I_{B1}}{C_1 + C_C}$$

$$SR_- \approx \frac{I_{B1}}{C_1 + C_C}$$





SR of Fully-Differential Miller OTA

- Must design the circuit such that $SR_+ = SR_-$
  - Both should be limited by I_{B1}
- Otherwise the slewing is asymmetric
  - Causes a shift in CM output
  - Slow transients if the CMFB network is slow

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- Linear and non-linear settling
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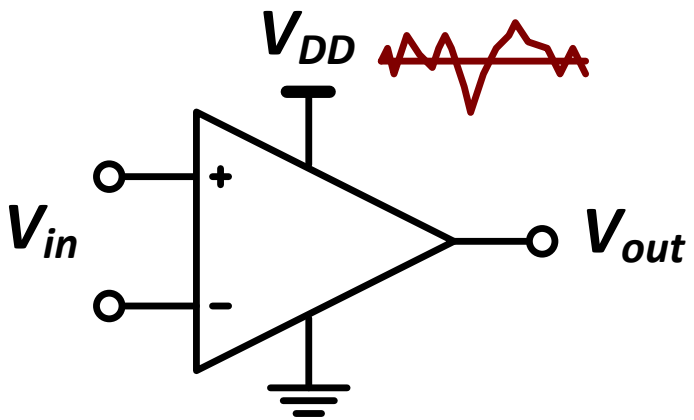
Power Supply Rejection (PSR)

- Supply lines carry noise from regulators, digital loads, etc.
- We don't want V_{out} to be affected by V_{DD} noise

$$PSR = \frac{1}{v_{out}/v_{DD}}$$

$$PSRR = \frac{v_{out}/v_{in}}{v_{out}/v_{DD}} = A_{vd} \cdot PSR$$

- Both PSR and PSRR usually reported in dB

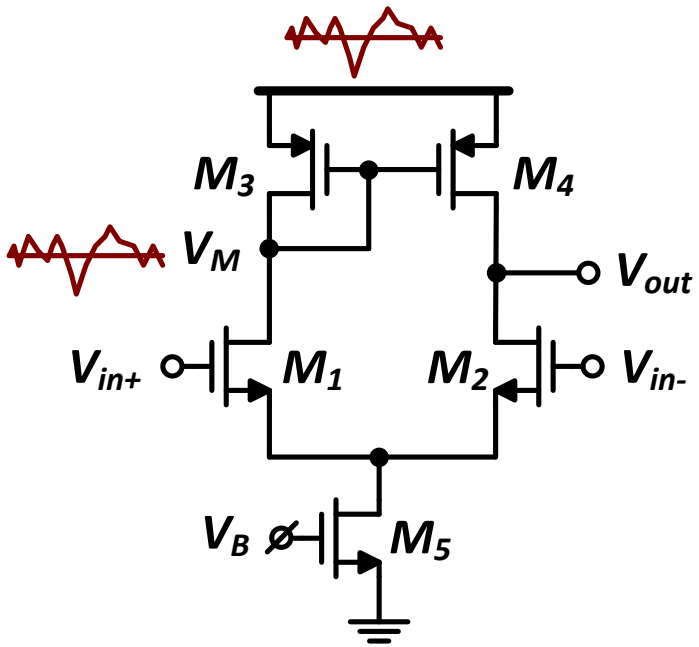


Power Supply Rejection Ratio (PSRR)

- The diode-connected device "clamps" V_M to VDD
- V_M and V_{out} experience approximately the same change as VDD

$$PSR = \frac{1}{v_{out}/v_{dd}} \approx 1$$

$$PSRR = \frac{v_{out}/v_{in}}{v_{out}/v_{dd}} = A_{vd} \cdot PSR \approx \frac{g_{m1,2}(r_{o2}||r_{o4})}{1}$$



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Quiz: PSRR of 5T OTA

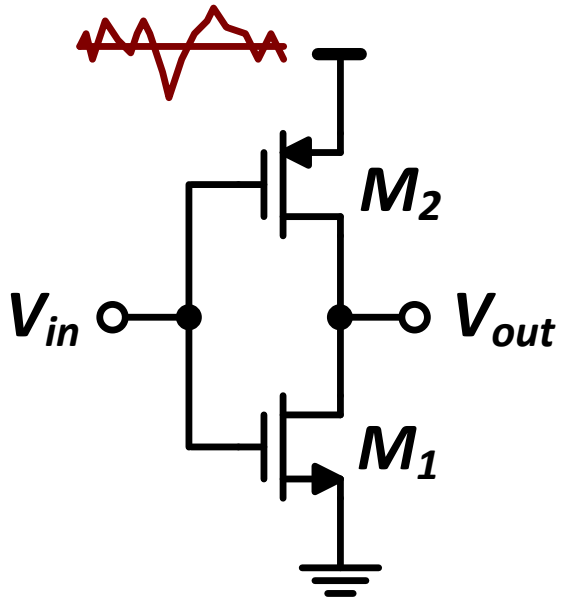
- Derive the PSRR for a 5T OTA with PMOS input pair
  - Assume the tail current source is generated by a simple current mirror
- What is the relation between the PSRR you derived and the CMRR?

Quiz: PSRR of Complementary CS

- Find the PSRR of the complementary CS amplifier (inverter-based amplifier)

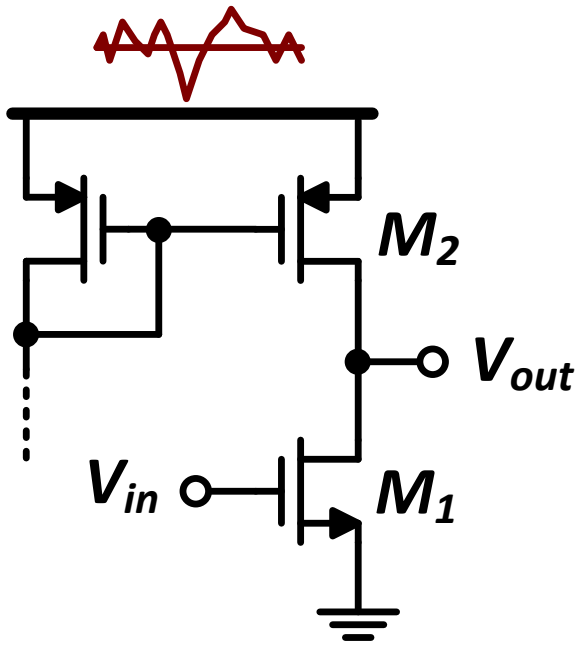
$$PSRR = \frac{v_{out}/v_{in}}{v_{out}/v_{dd}}$$

- Very poor PSRR!



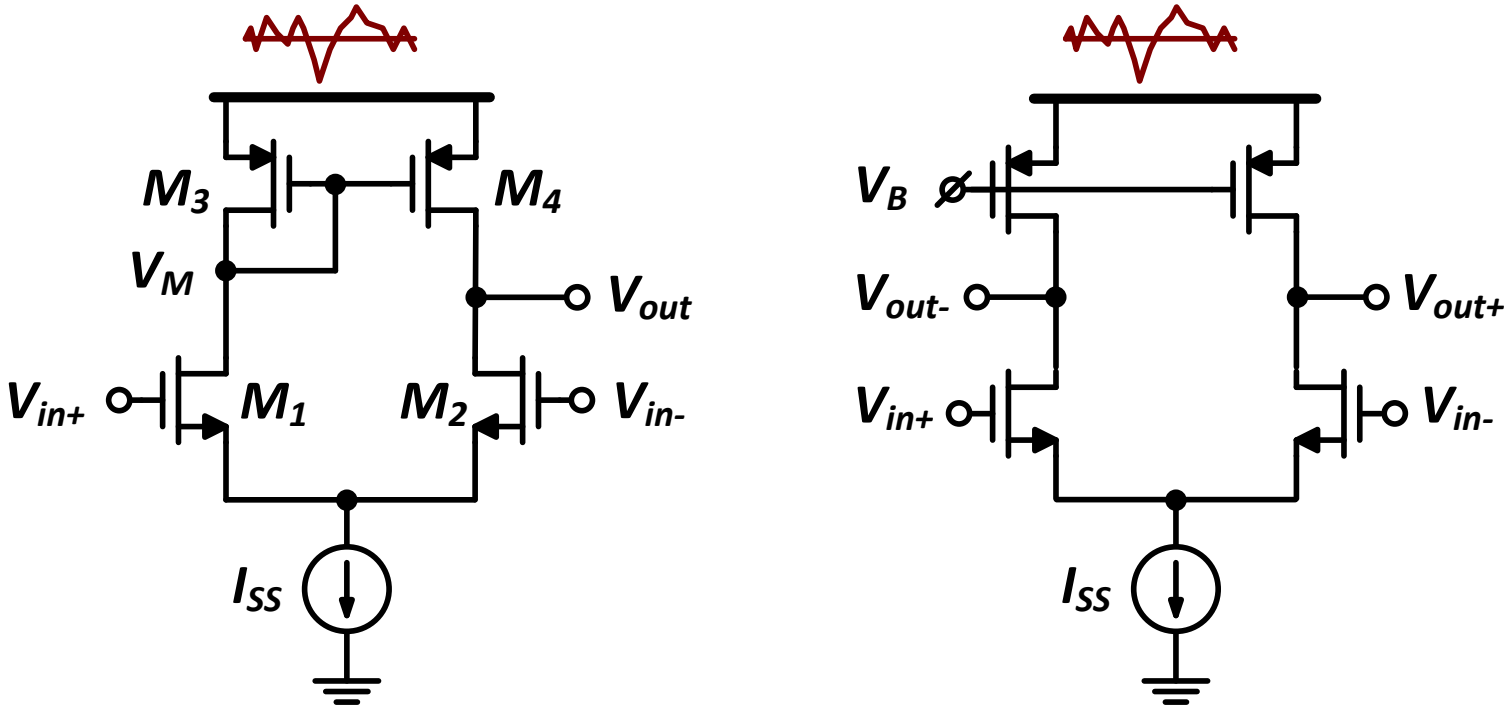
Quiz: PSRR of CS with Active Load

- Assume all transistors have the same g_m and r_o
- Note: The gate of the active load is **NOT** ac ground



PSRR: SE Output vs Fully Differential

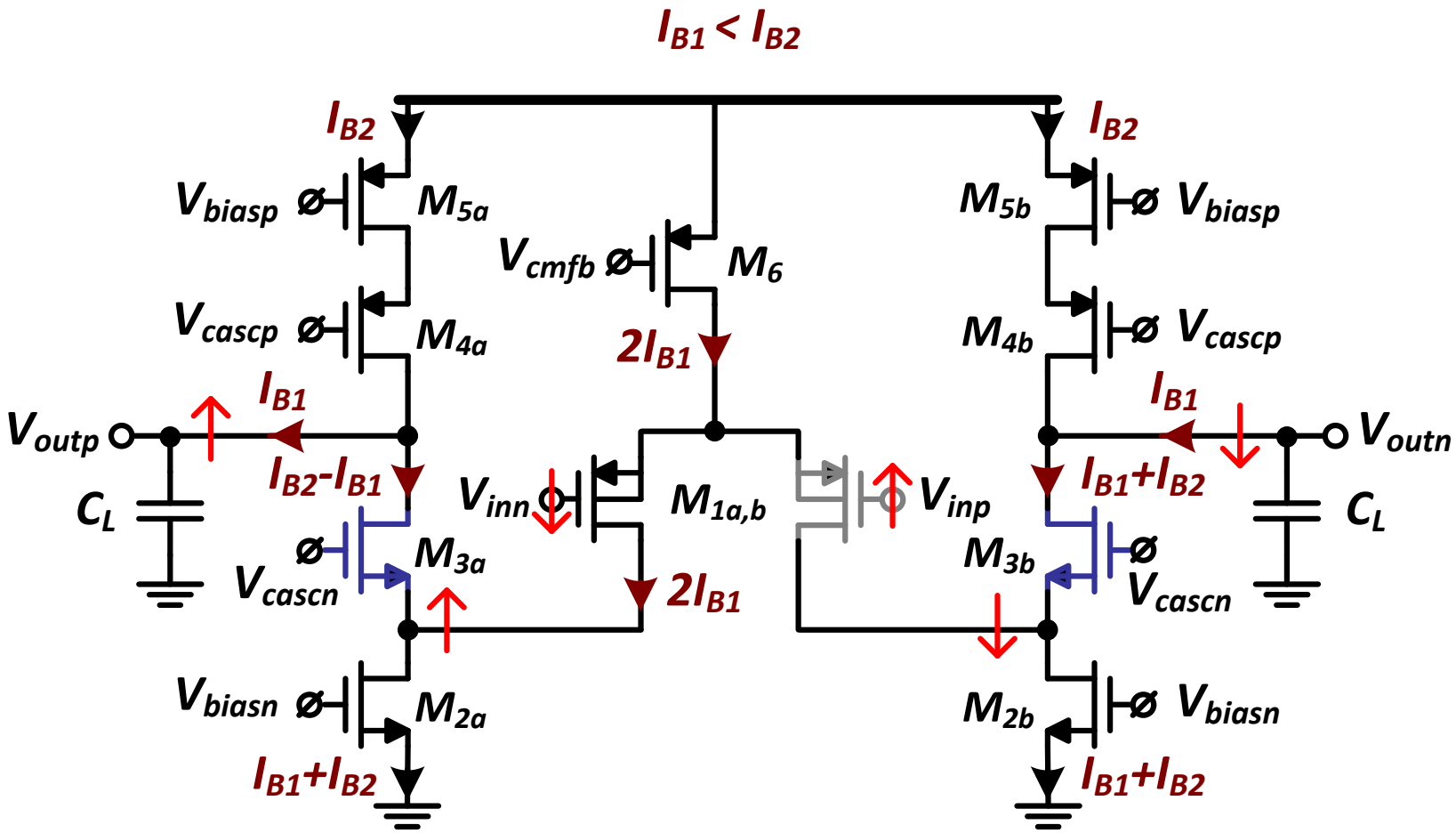
- In both cases ΔV_{DD} gets transferred to the output
  - But for the fully diff amp, the differential output is not affected



Thank you!

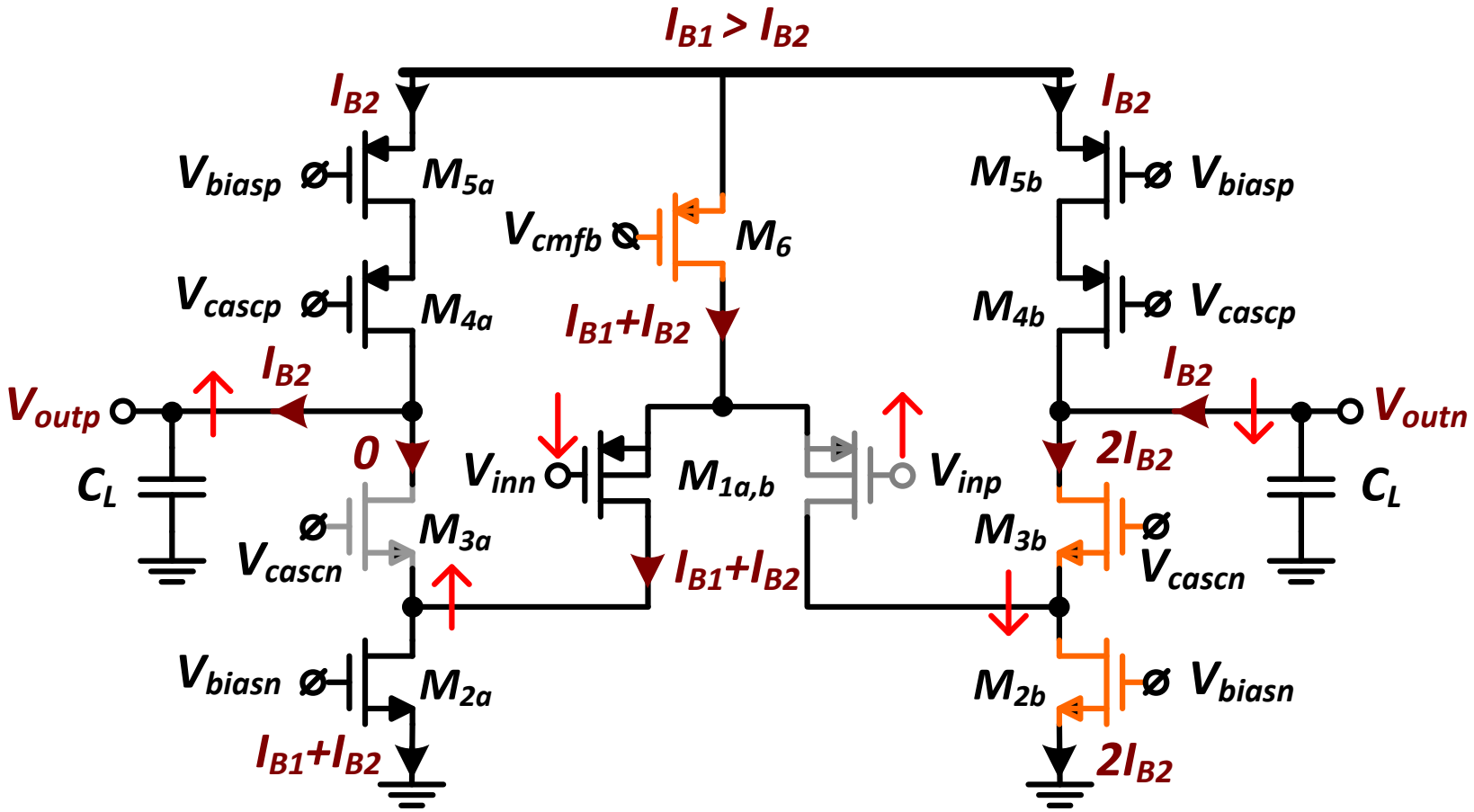
Folded Cascode Slewing (IB1 < IB2)

- The slewing is always symmetrical independent of the speed of the CMFB network.
  - This is an advantage for driving slightly more current in the output branch.



Folded Cascode Slewing (IB1 > IB2)

- Assume a fast CMFB network that forces a constant CM (symmetrical slewing).



Folded Cascode Slewing (IB1 > IB2)

- Assume a slow CMFB network (non-symmetrical slewing).