**Lab 4**

Common Drain Amplifier

Part 1: Sizing Chart

Required Spec:

|  |  |
| --- | --- |
| L | 1um |
| V\* | 200mV |
| Quiescent (DC) Input Voltage | 0 𝑉 |
| Supply Voltage | 1.8 𝑉 |
| Bias Current | 10 uA |

A screenshot of a computer

AI-generated content may be incorrect.Analytic Calculations:

Sizing Using ADT:

Inputting the Design parameters into ADT SA we get:

Figure 1 Sizing Using ADT

Part 2: Common Drain Amplifier

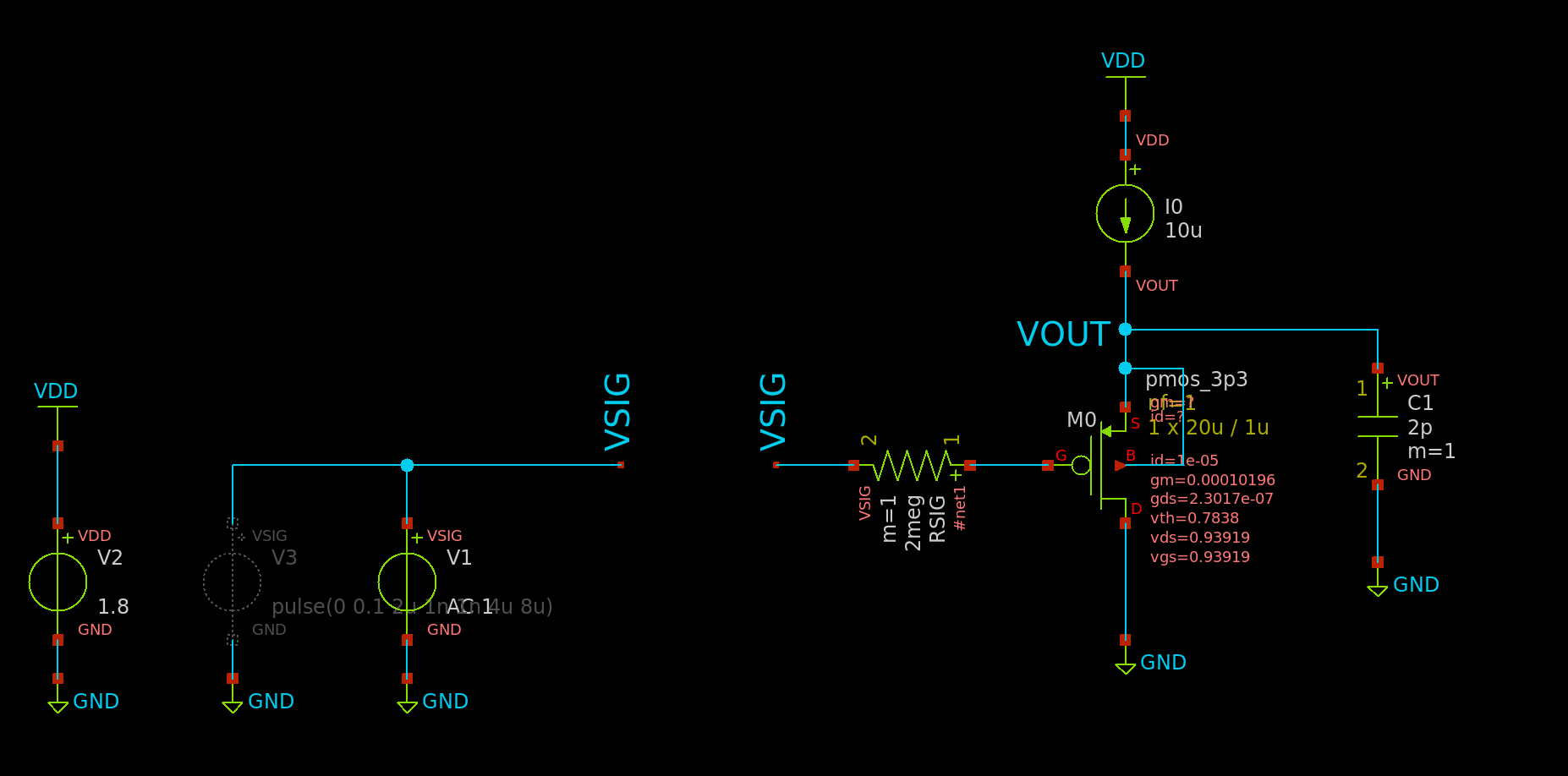


Figure 2 Testbench Schematic for both AC and Tran Analysis

Operating Point:

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | id | vgs | vds | vth | vdsat | gm | gds | gmbs | Cdb | Cgd | Cgs | Csb |
| M0 | 10uA | 0.94V | 0.94V | 0.785V | 0.153V | 102uS | 230nS | 48.2uS | 9.97fF | 14.2aF | 51.1fF | 14.9fF |

Transistor Operates in Saturation!

Values of Capacitances from ADT:

Calculating the capacitance value from ADT instead of Xschem as it is more accurate for hand analysis.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Cdb | Cgd | Cgs | Csb |
| M0 | 8.969fF | 3.073fF | 51.1fF | 14.9fF |

AC Analysis:

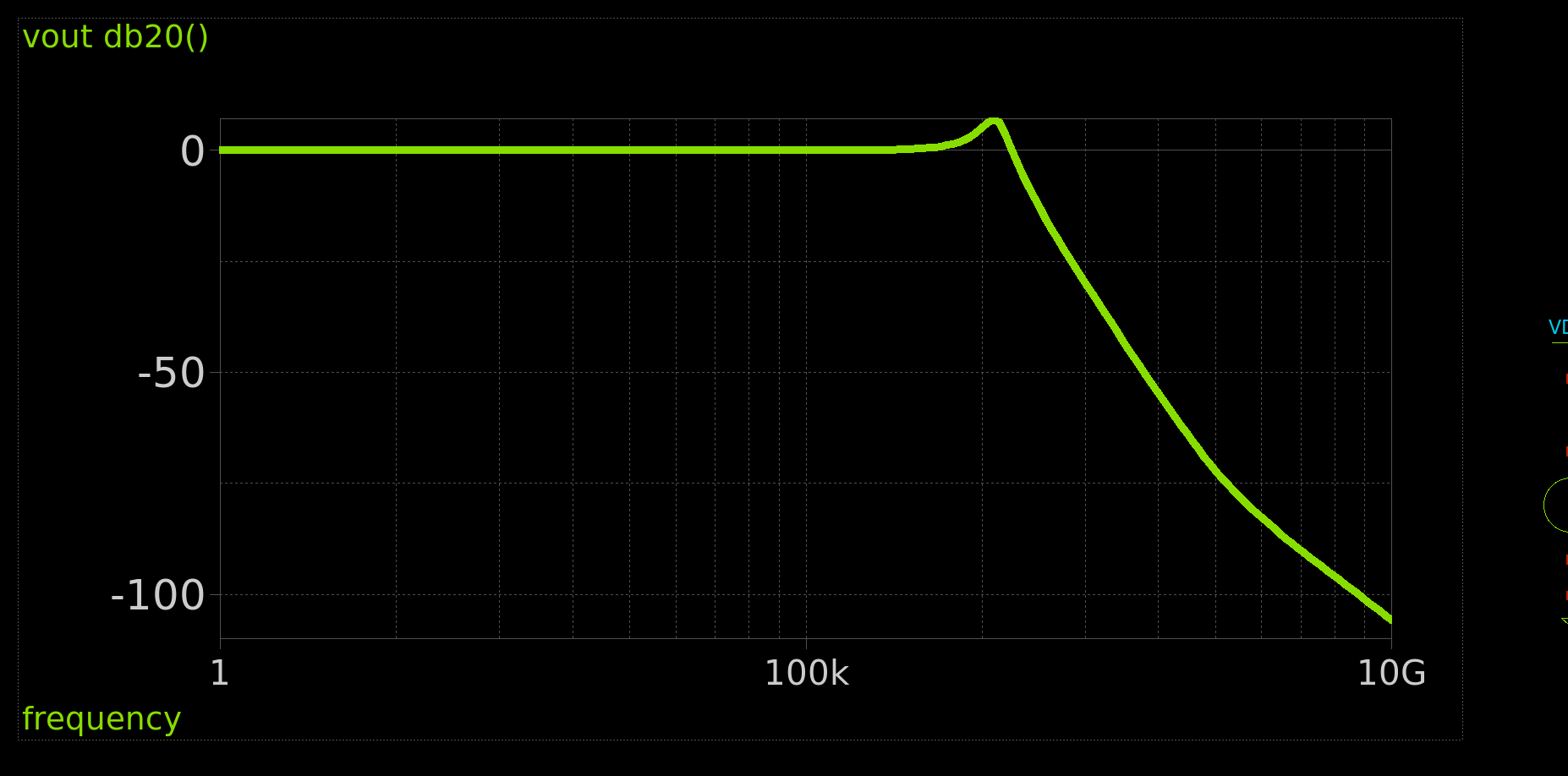
**Outputs:** 

Figure 3 Bode Plot of Common Drain Amplifier

* Do you notice frequency domain peaking? How much is the peaking?

Yes, there is peaking. Its value is about **2 in magnitude** or around **6dB**



Figure 4 Value of Peaking from Simulation

Quality Factor Calculation:

The System is Underdamped!

* Parametric sweep: CL = 2p, 4p, 8p:

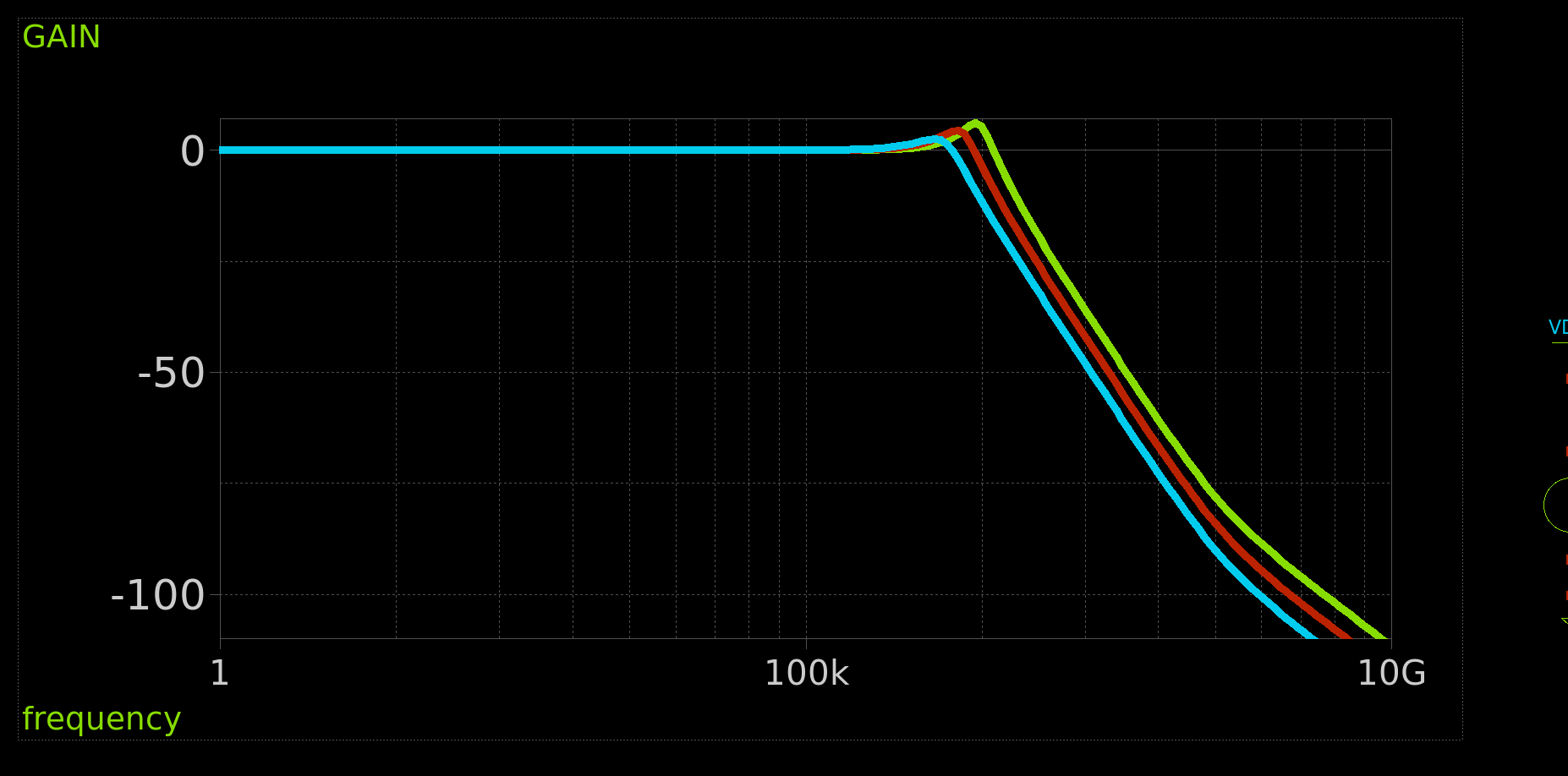


Figure 5 AC Analysis Parametric Sweep of CL

|  |  |  |  |
| --- | --- | --- | --- |
| **CL Value** | 2pF | 4pF | 8pF |
| **Peaking** | 2.0161 | 1.667 | 1.3358 |

Peaking vs CL:

Peaking decreases as we increase the Value of CL

Comment:

Increasing CL decreases Q closer to 0.5 thus reducing the Peaking and making the system overdamped.

* Parametric sweep: Rsig = 20K, 200K, 2M:

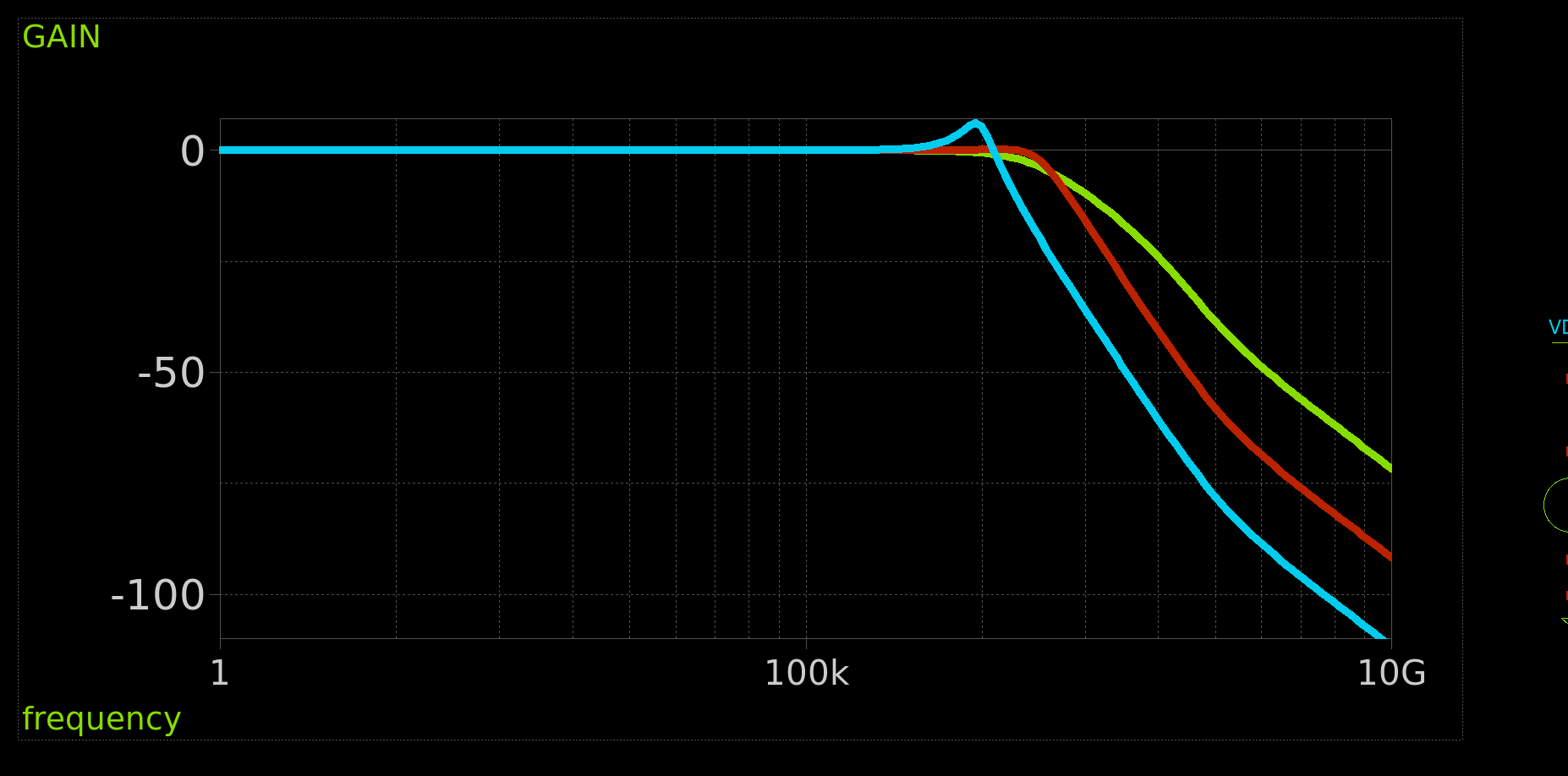


Figure 6 AC Analysis Parametric Sweep of Rsig

|  |  |  |  |
| --- | --- | --- | --- |
| **Rsig Value** | 20K | 200K | 2M |
| **Peaking** | 0.997 | 1.021 | 2.0161 |

Peaking vs Rsig:

Peaking increases as we increase the value of Rsig

Comment:

Increasing Rsig Increases Q thus increasing the peaking and underdamping the system.

Transient Analysis:

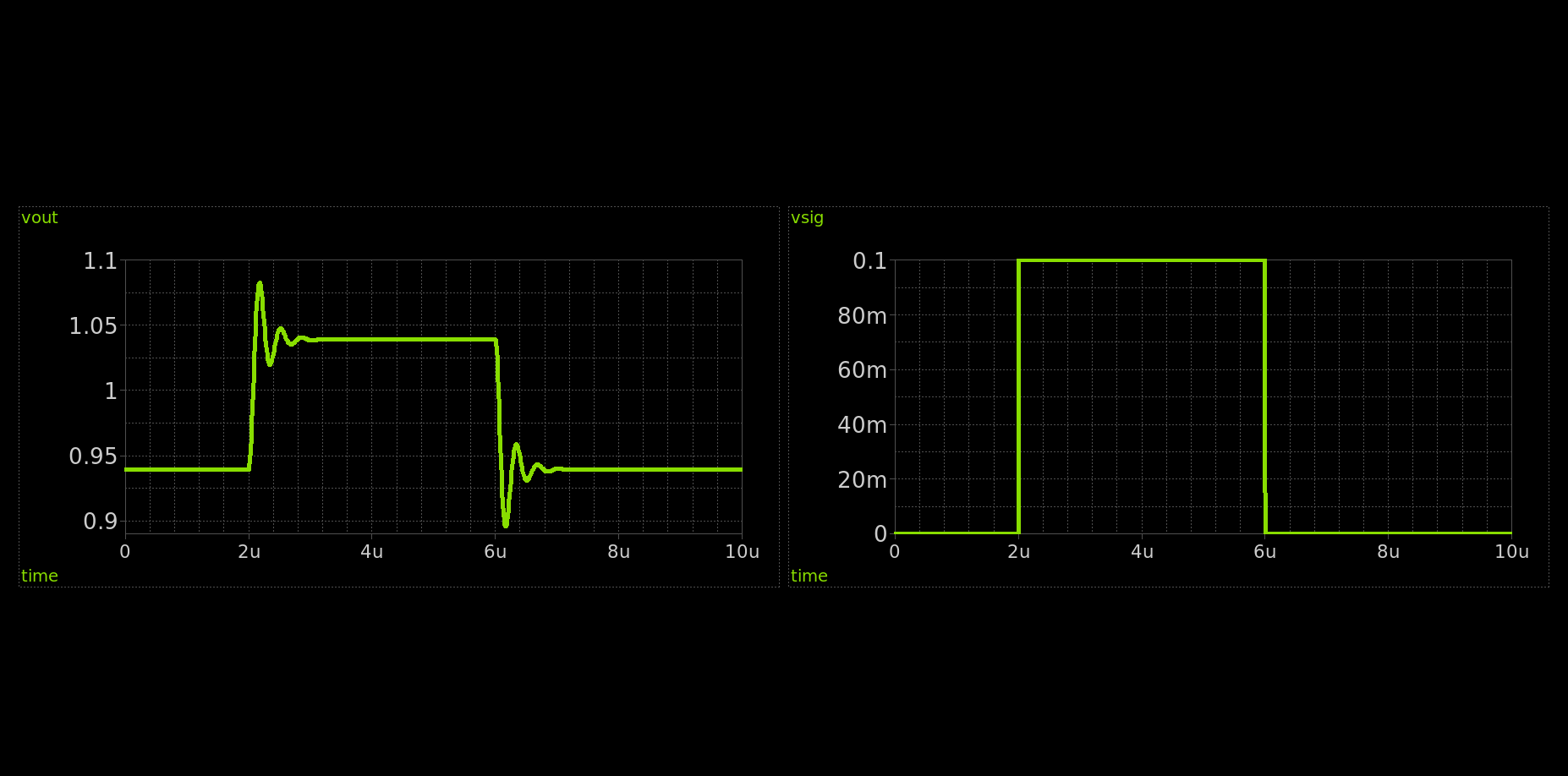
**Outputs:** 

Figure 7 VIN and VOUT vs Time (Transient Analysis)

* DC Voltage difference:

A black background with white and yellow lines

AI-generated content may be incorrect.

Figure 8 Values of VOUT from simulation

The DC shifted up about **0.94V**, the minimum value of Vin is 0 and the Minimum value of Vout is 0.94V.

**How to shift the signal down instead of shifting it up?**

By using an NMOS CD configuration instead of the PMOS configuration.

* Do you notice time domain ringing ? How much is the overshoot?

Yes, there is an overshoot of about **43.45%**



Figure 9 Value of overshoot from Simulation

Parametric sweep: CL = 2p, 4p, 8p:

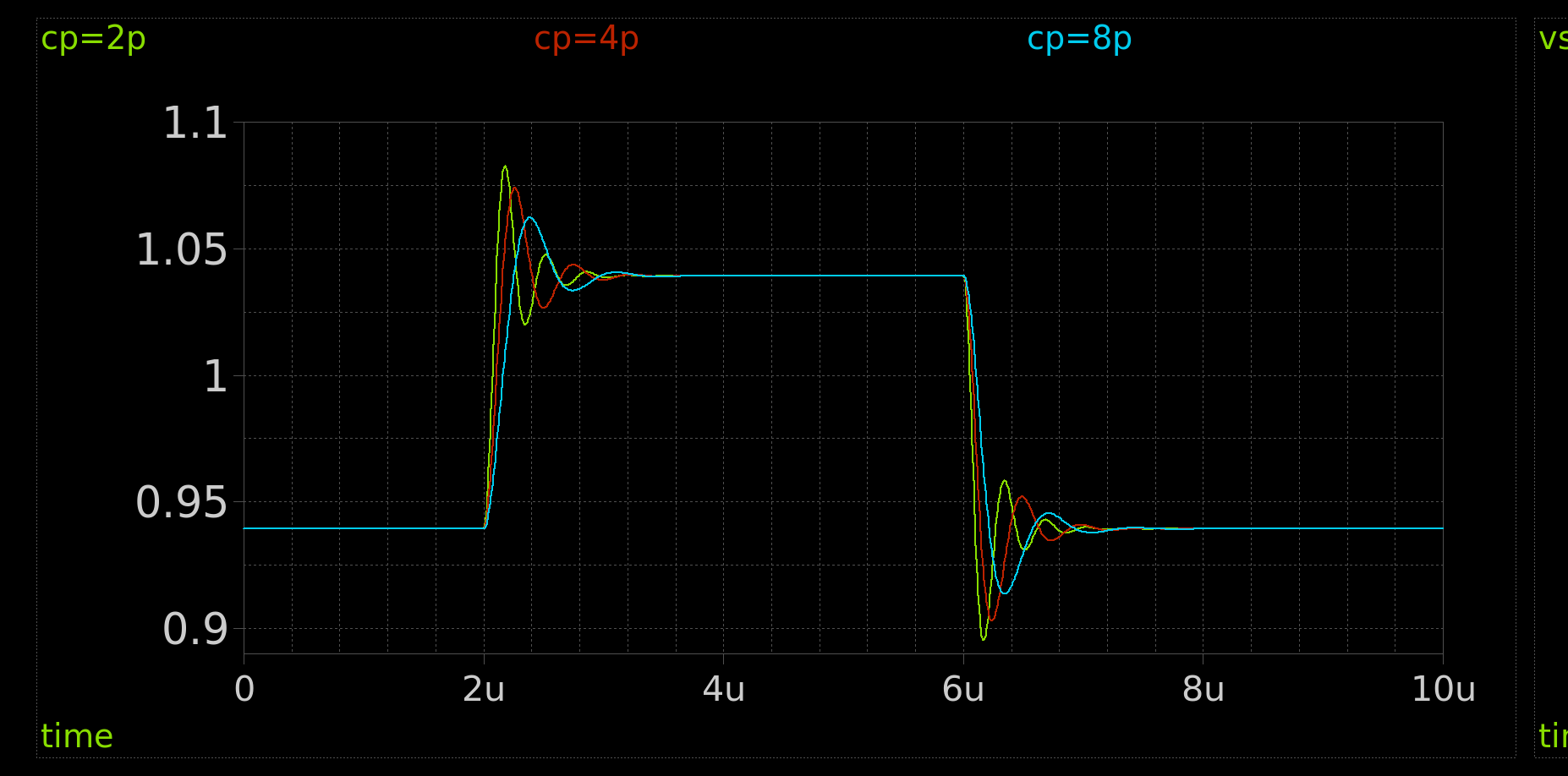


Figure 10 Transient Analysis Parametric Sweep of CL

|  |  |  |  |
| --- | --- | --- | --- |
| **CL Value** | 2pF | 4pF | 8pF |
| **Peaking** | 43.456% | 34.77% | 23.2% |

Peaking vs CL:

Overshoot decreases as we increase the Value of CL

Comment:

Increasing CL decreases Q closer to 0.5 thus reducing the ringing and making the system overdamped.

* Parametric sweep: Rsig = 20K, 200K, 2M:

A graph of a graph

AI-generated content may be incorrect.

Figure 11 AC Analysis Parametric Sweep of Rsig

|  |  |  |  |
| --- | --- | --- | --- |
| **Rsig Value** | 20K | 200K | 2M |
| **Peaking** | 0.997 | 1.021 | 2.0161 |

Peaking vs Rsig:

Peaking increases as we increase the value of Rsig

Comment:

Increasing Rsig Increases Q thusincreasing the peaking and underdamping the system.

* Parametric sweep: Rsig = 20K, 200K, 2M:

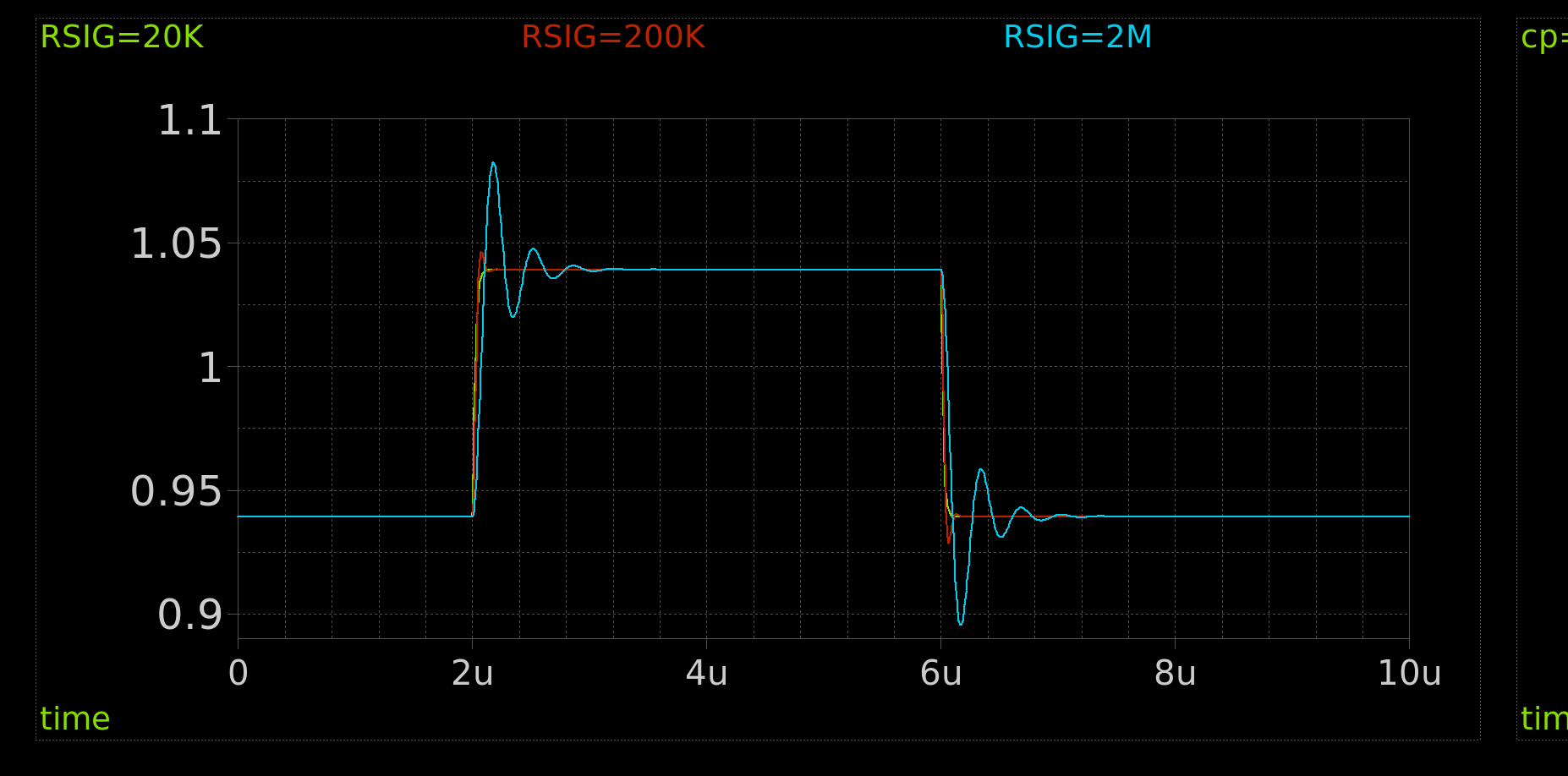


Figure 12 Transient Analysis Parametric Sweep of Rsig

|  |  |  |  |
| --- | --- | --- | --- |
| **Rsig Value** | 20K | 200K | 2M |
| **Peaking** | 0% | 7.23% | 43.456% |

Peaking vs Rsig:

Ringing increases massively as we increase the value of Rsig

Comment:

Increasing Rsig Increases Q thus increasing the ringing and underdamping the system.

Zout Inductive Rise:

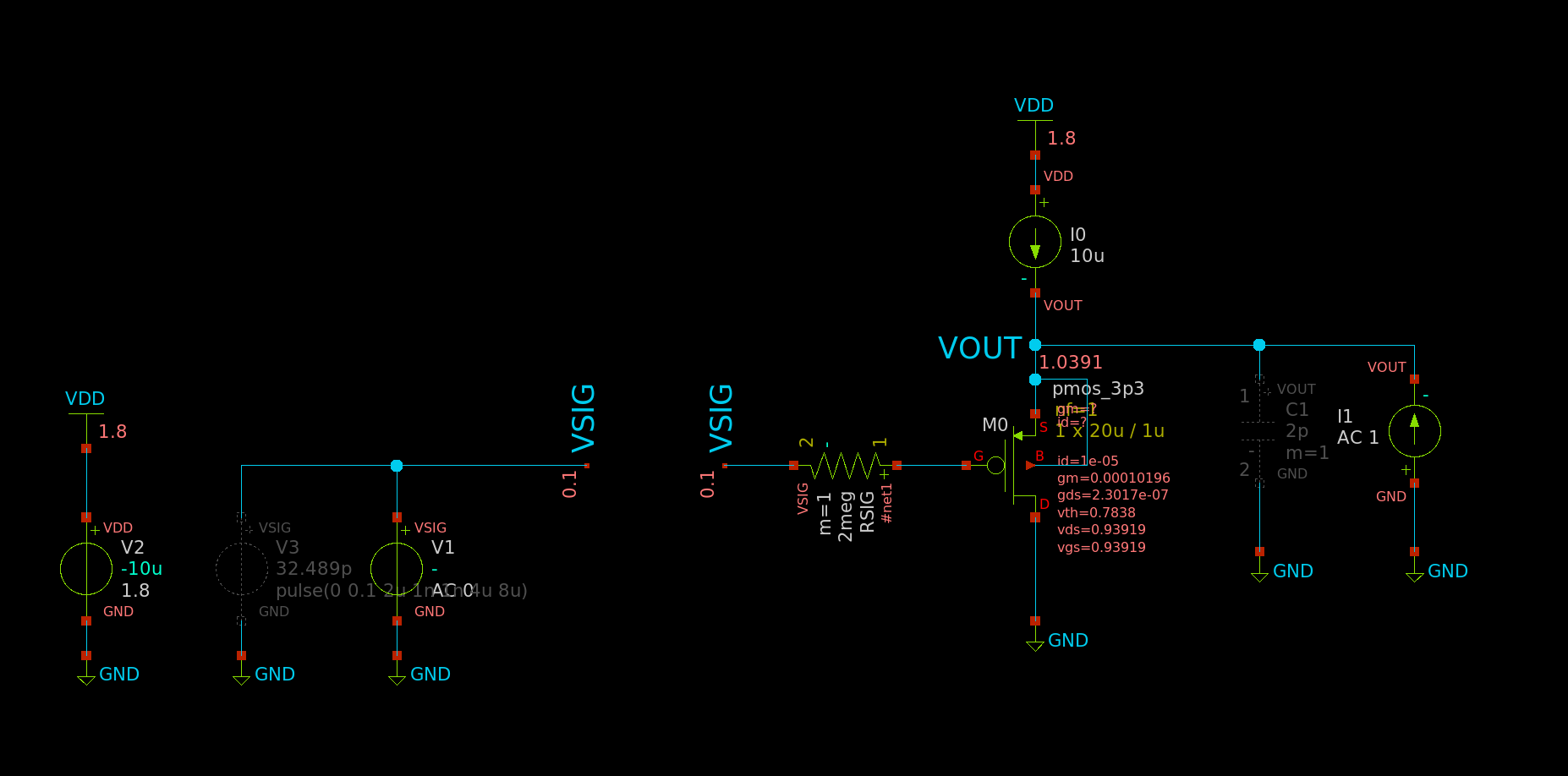


Figure 13 Modified Testbench to Calculate Zout

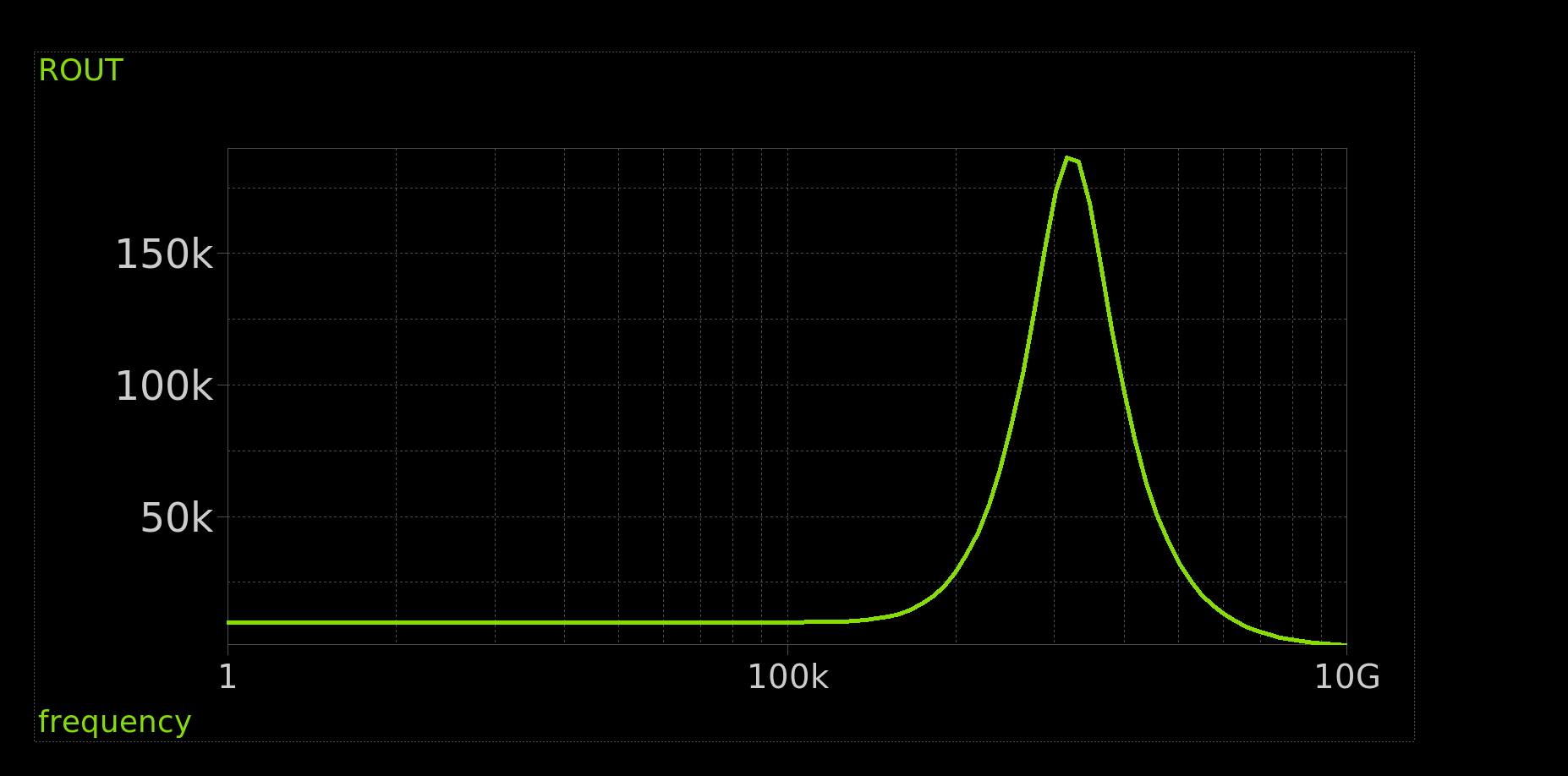


Figure 14 ZOUT vs Frequency



Figure 15 Zout at High and Low Frequencies

* Do you notice an inductive rise? Why?

Yes, because at high frequencies, Cgs is shorted so Zout becomes equal to Rsig.

But in the simulation the it does not quite reach Rsig this is due to Cgd taking over before Cgs can short completley

* Does 𝑍𝑜𝑢𝑡 fall at high frequency? Why?

Due to the Pole generated by Cgs Zout falls quickly.

* Analytically calculate the zeros, poles, and magnitude at low/high frequency for 𝑍𝑜𝑢𝑡. Compare with simulation results in a table.

**Poles and Zeros Analytically:**

Simulation Results:

A graph with lines and numbers

AI-generated content may be incorrect.

Figure 16 Zero Location @ 1.1MHz