**Lab 5**

Current Mirrors

Part 1: Sizing Chart

Required Spec:

|  |
| --- |
| Parameter |
| Current direction (source/sink) | Sink |
| Input Current | 10𝜇𝐴 |
| Output Current | 20𝜇𝐴 |
| % Change in Current for 𝚫𝑽𝒐𝒖𝒕 = 𝟏𝑽 | < 10% |
| Percent mismatch: 𝝈(𝑰𝒐𝒖𝒕)/𝑰𝒐𝒖𝒕 | ≤ 2% |
| Compliance voltage | ≤ 150𝑚𝑉 |
| Area | Minimize |

2) Sinking Current Means?

NMOS Transistor

3) Required Lambda

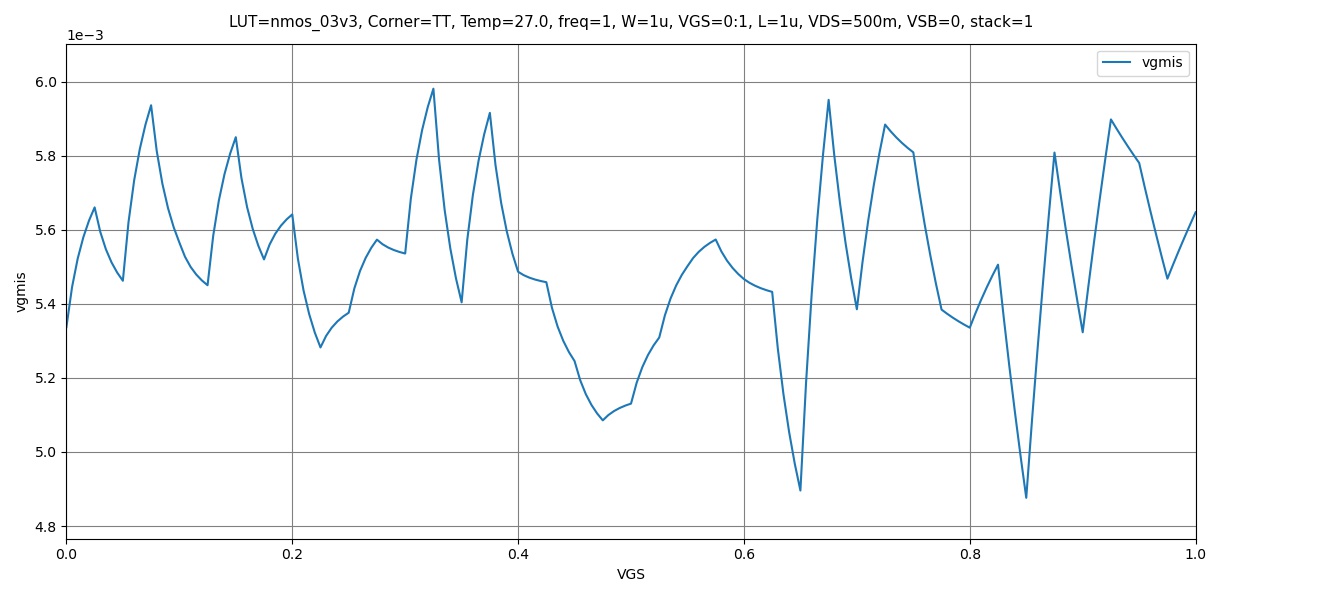
5) Mismatch from ADT

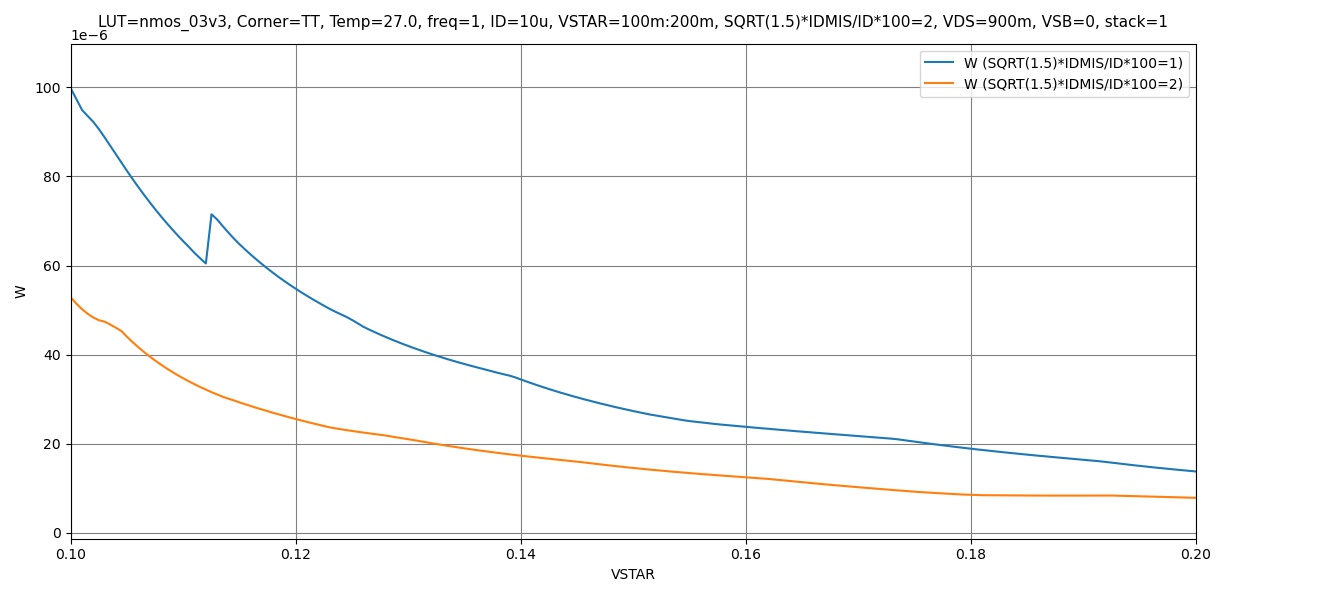
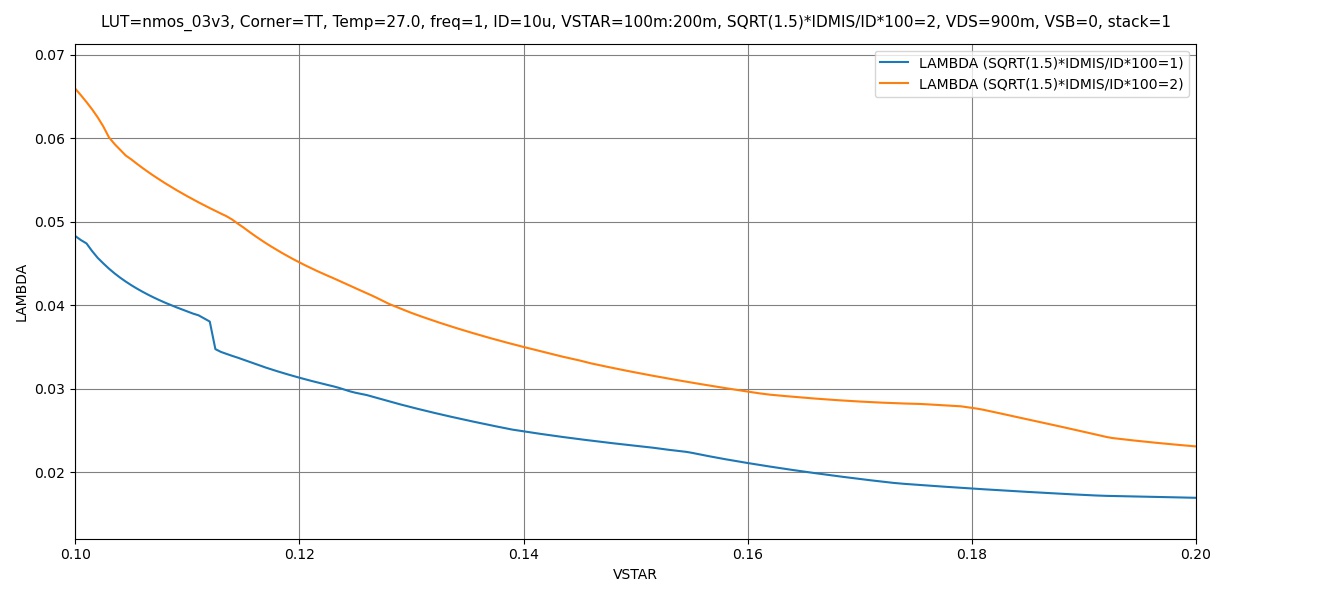
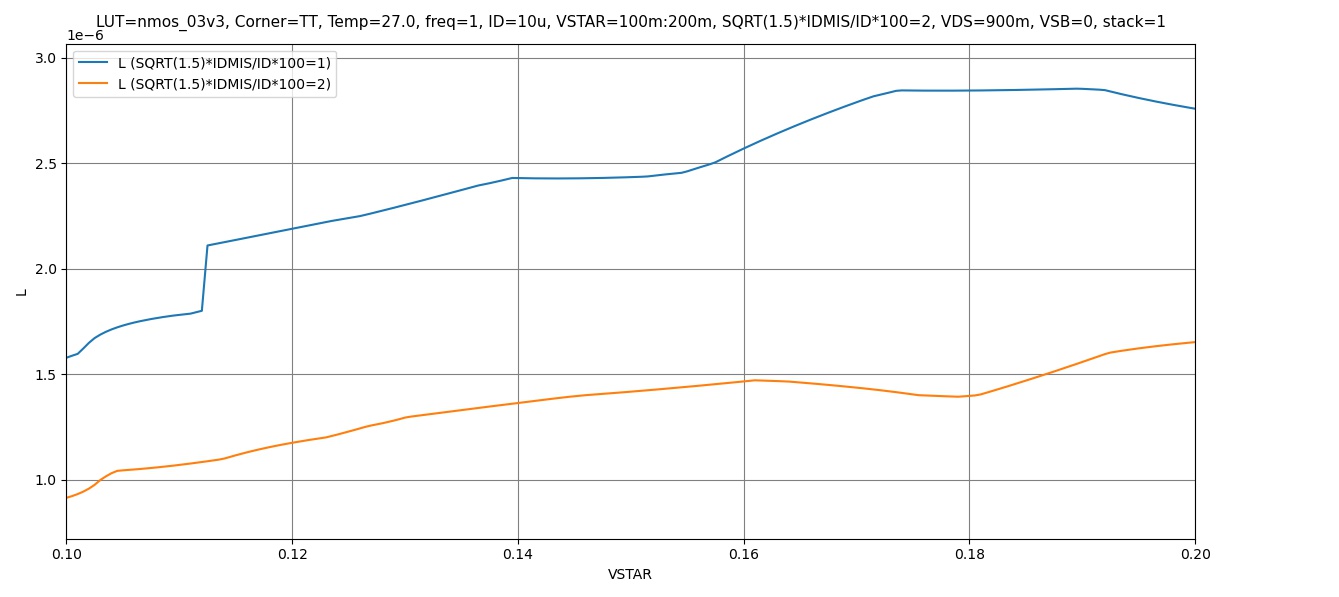
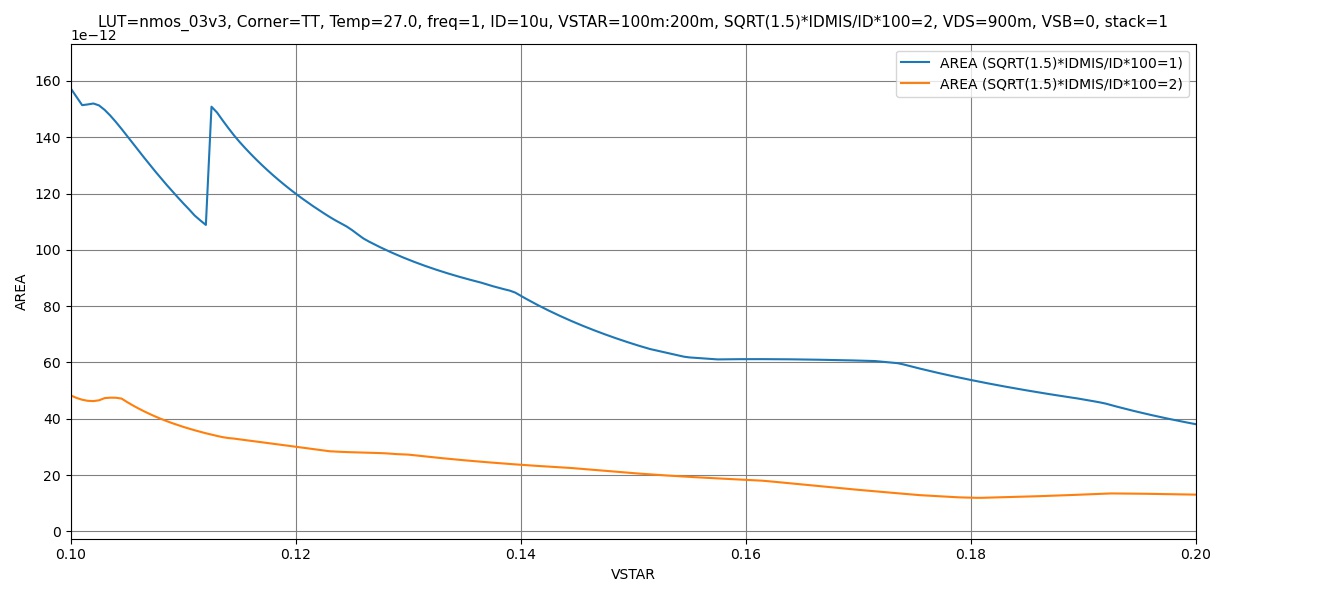
Figure 1 VGMIS vs VGS

From the graph we can find the approximate value of

6) Mismatch from PDK

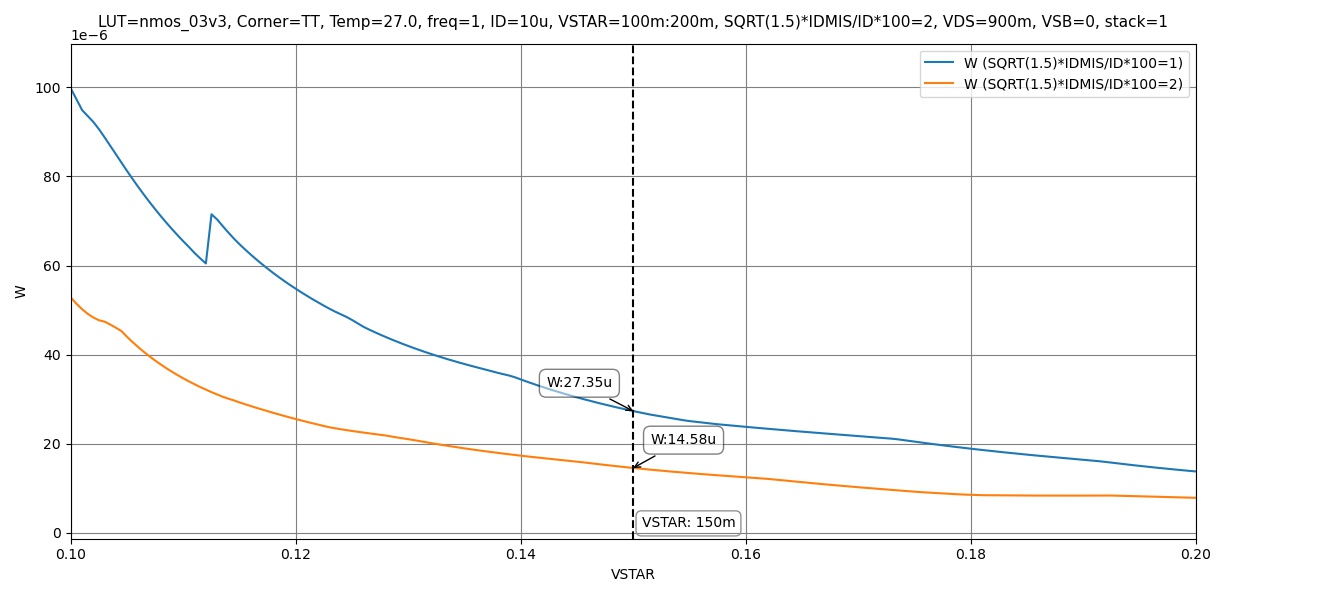
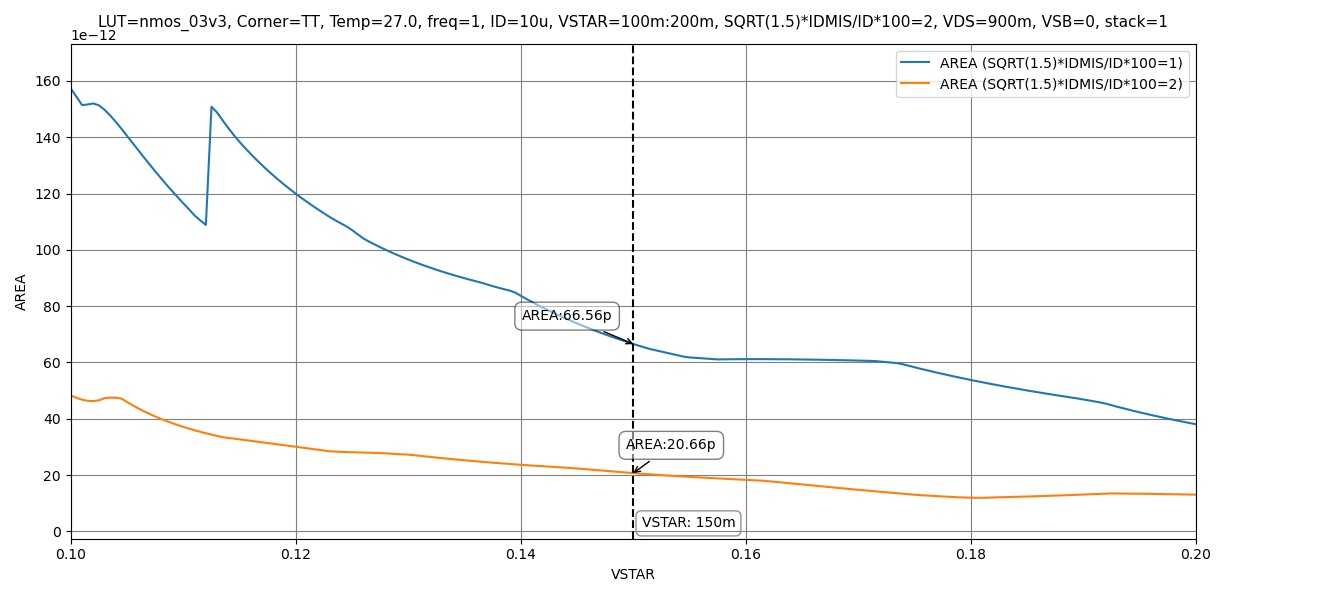
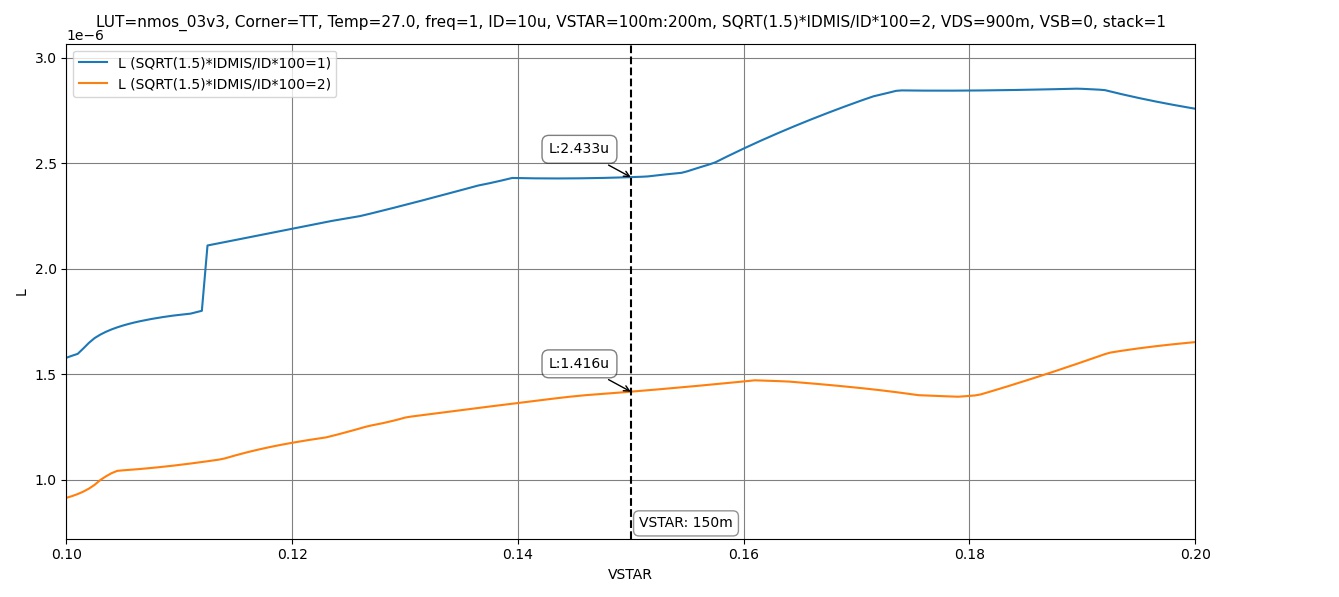
The value from ADT is slightly higher, this is possibly due to inaccuracies that occur when calculating and estimating random values.

7) Design Parameters vs vstar at different mismatch



9) Design Parameters at required VstarA graph with lines and numbers

AI-generated content may be incorrect.



From the Graphs we notice both values of the mismatch current satisfy the Lambda Constraint

Thus we will choose the dimensions corresponding with the mismatch value which has the lower area

9) What if Lambda constraints is not met?

By inputting the required exact value for lambda () we can calculate the mismatch corresponding to it using the same expression used before.



11) Report Device Sizing and Mismatch percentage

Selected design points @

|  |  |
| --- | --- |
|  | 2% |
| L | 1.42um |
| W | 14.58um |

Part 2: Current Mirror Simulation

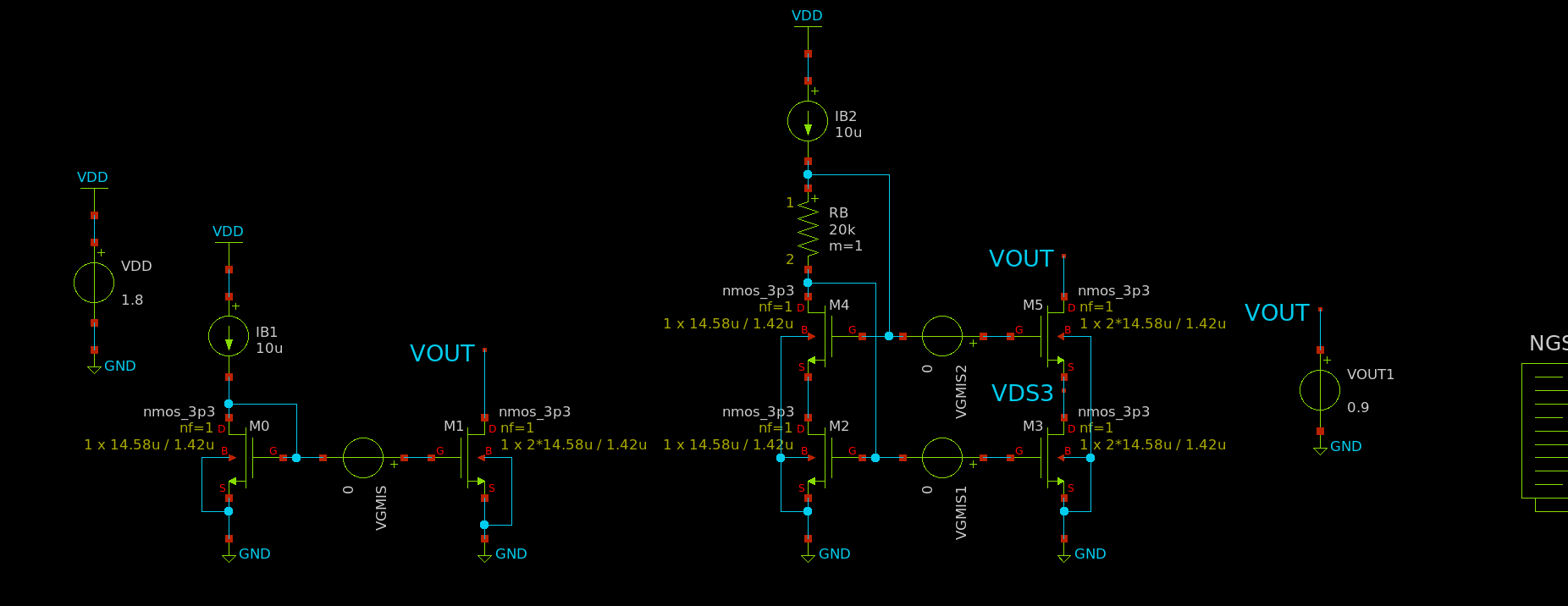


Figure 2 Current Mirror Schematic Testbench

Design and OP Analysis

1. Finding RB analytically
2. Finding RB through Simulation

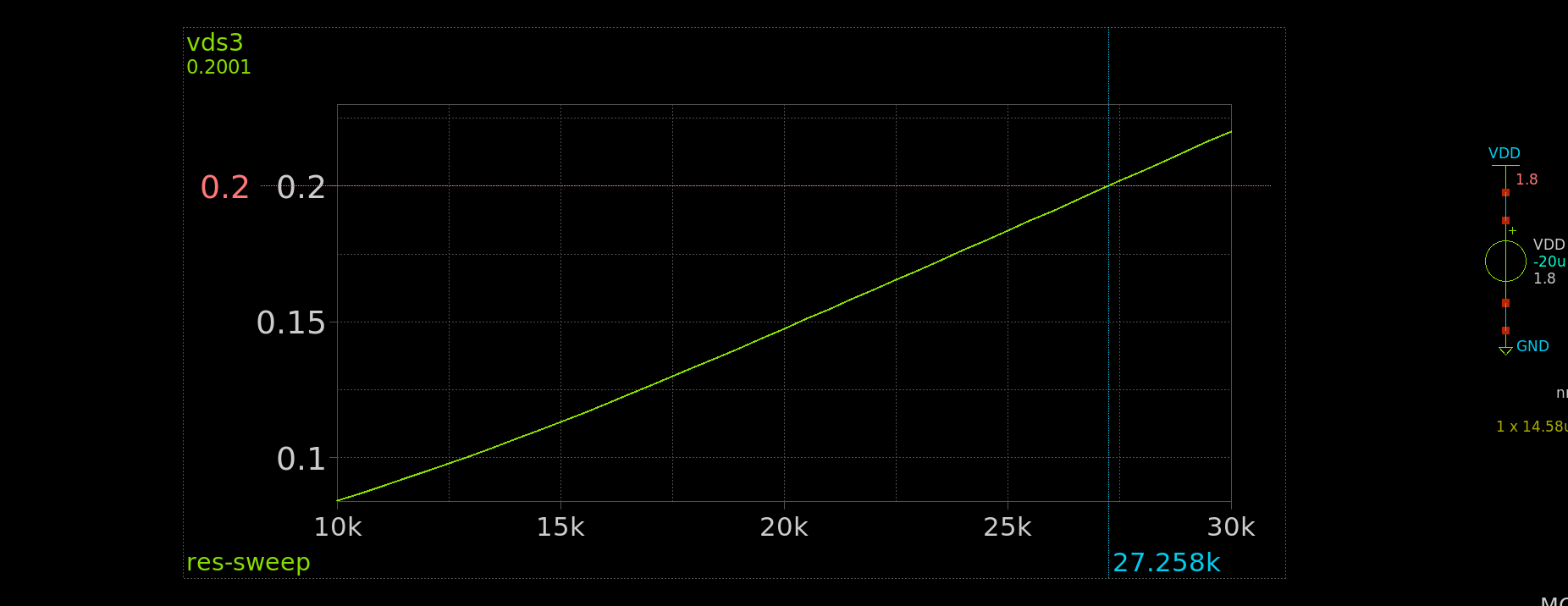


Figure 3 Value of RB from simulation

The value of RB calculated from the simulation is larger than the one calculated analytically, this is due to the analytic solution not accounting for body effect which makes the difference in VGS have a value thus increasing the required RB.