**Lab 6**

Differential Amplifier

Part 1: Sizing Chart

Required Spec:

|  |
| --- |
| Parameter |
| Supply **(𝑽𝑫𝑫)** | 1.8𝑉 |
| Bias current **(𝑰𝑺𝑺)** | 40𝜇𝐴 |
| Differential gain | 8 |
| CM output level**1** | 𝑉𝐷𝐷/3 |
| Load capacitance | 1𝑝𝐹 |
| Supply **(𝑽𝑫𝑫)** | 1.8𝑉 |
| Bias current **(𝑰𝑺𝑺)** | 40𝜇𝐴 |

A screenshot of a computer

AI-generated content may be incorrect.Input Pair Sizing:

From SA:

8) The SA assumes VDS at 0.9V

Thus

Figure 1 Input Pair Dimensions from Sizing Assistant

Current Mirror Sizing:

|  |  |
| --- | --- |
| Parameter |  |
| Input current | 20𝜇𝐴 |
| Percent mismatch: 𝝈(𝑰𝒐𝒖𝒕)/𝑰𝒐𝒖𝒕 | ≤ 2% |
| Compliance voltage | ≤ 200𝑚𝑉 |
| Area | Minimize |

Using the equation supplied in the Lab manual for mismatch we can draw the following graphs

A graph with a line going up

AI-generated content may be incorrect.

Figure 2 L vs Vstar

A graph with a line

AI-generated content may be incorrect.

Figure 3 Area vs Vstar

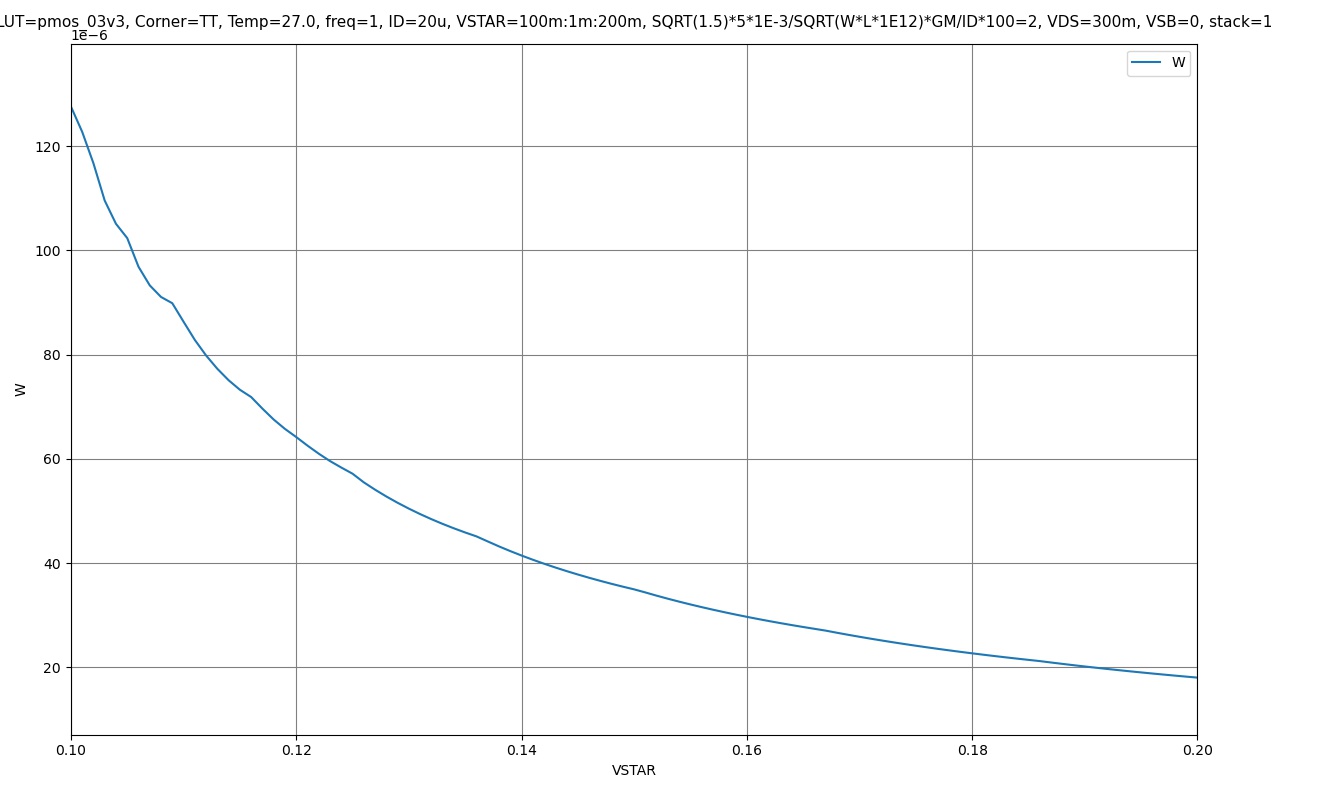


Figure 4 W vs Vstar

Smallest area can be found at the largest acceptable value for V Compliance (200mV)

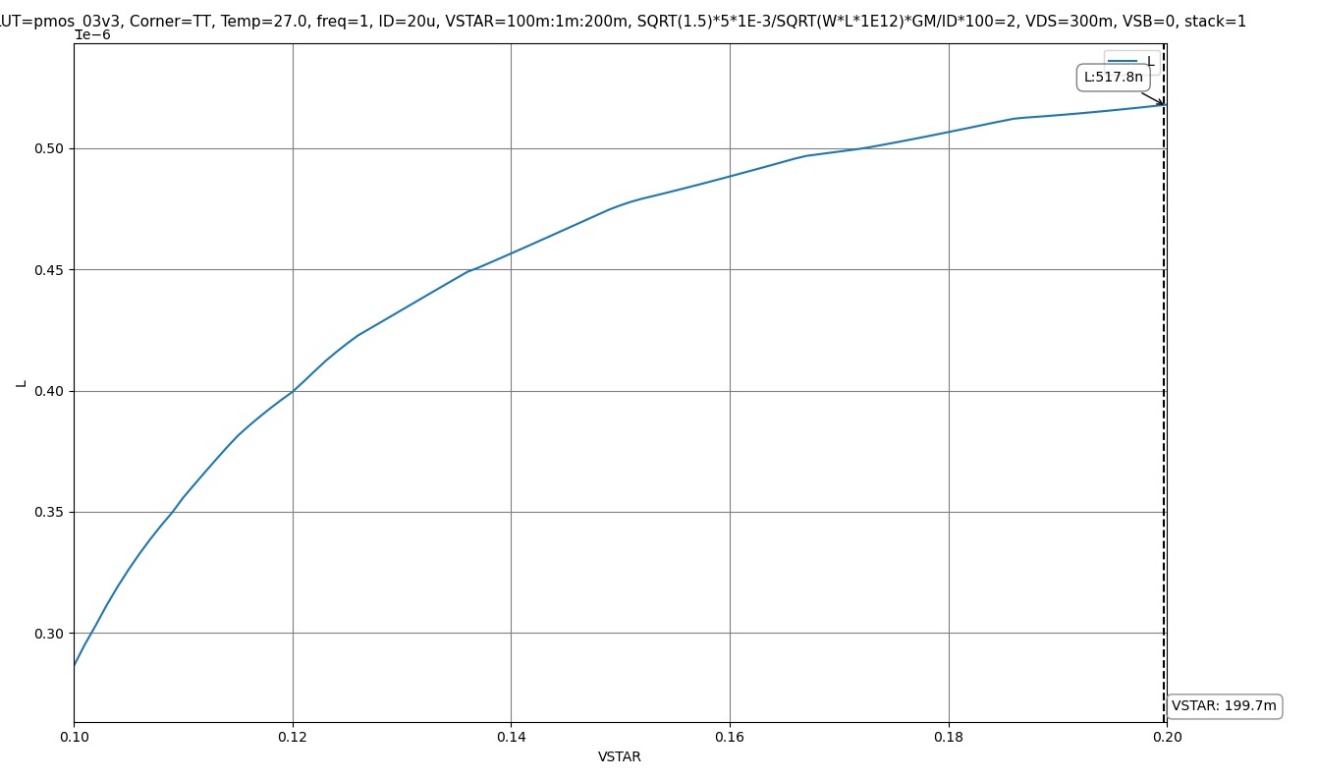


Figure 5 L at Required Vstar

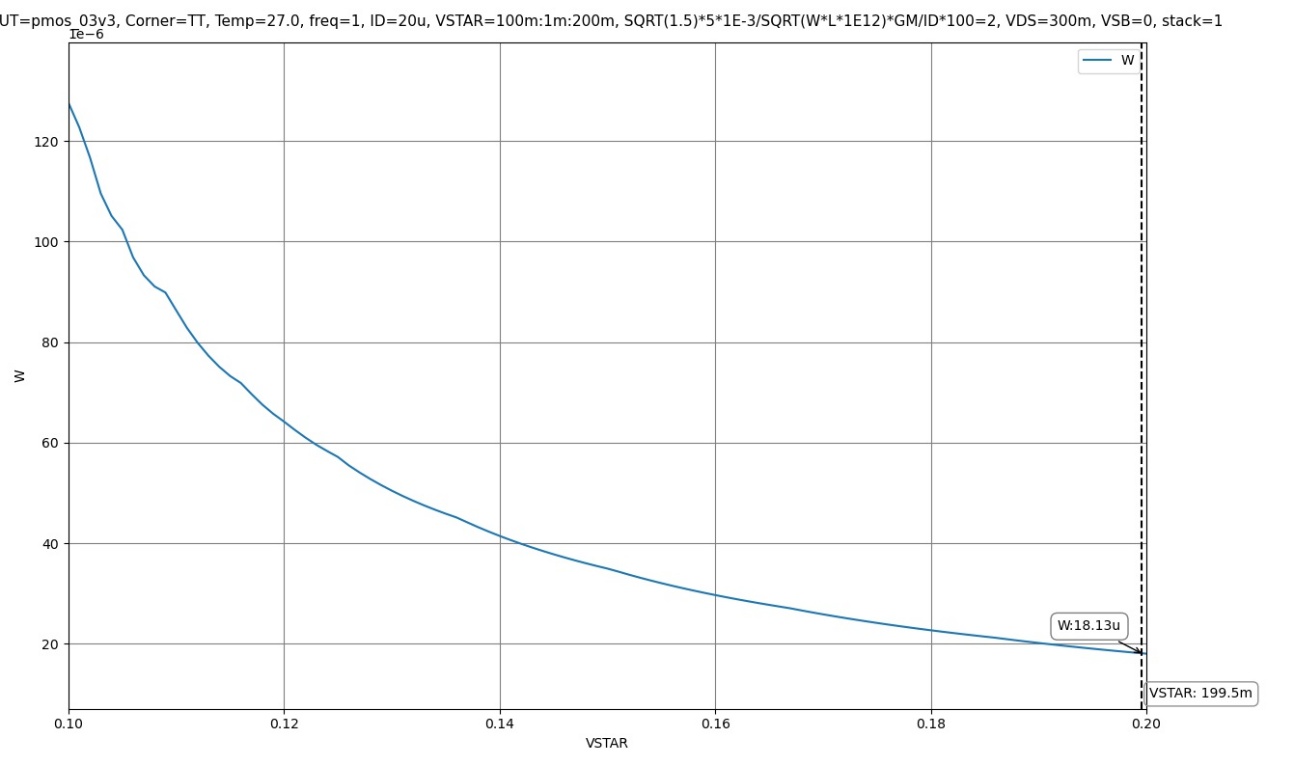


Figure 6 W at Required Vstar

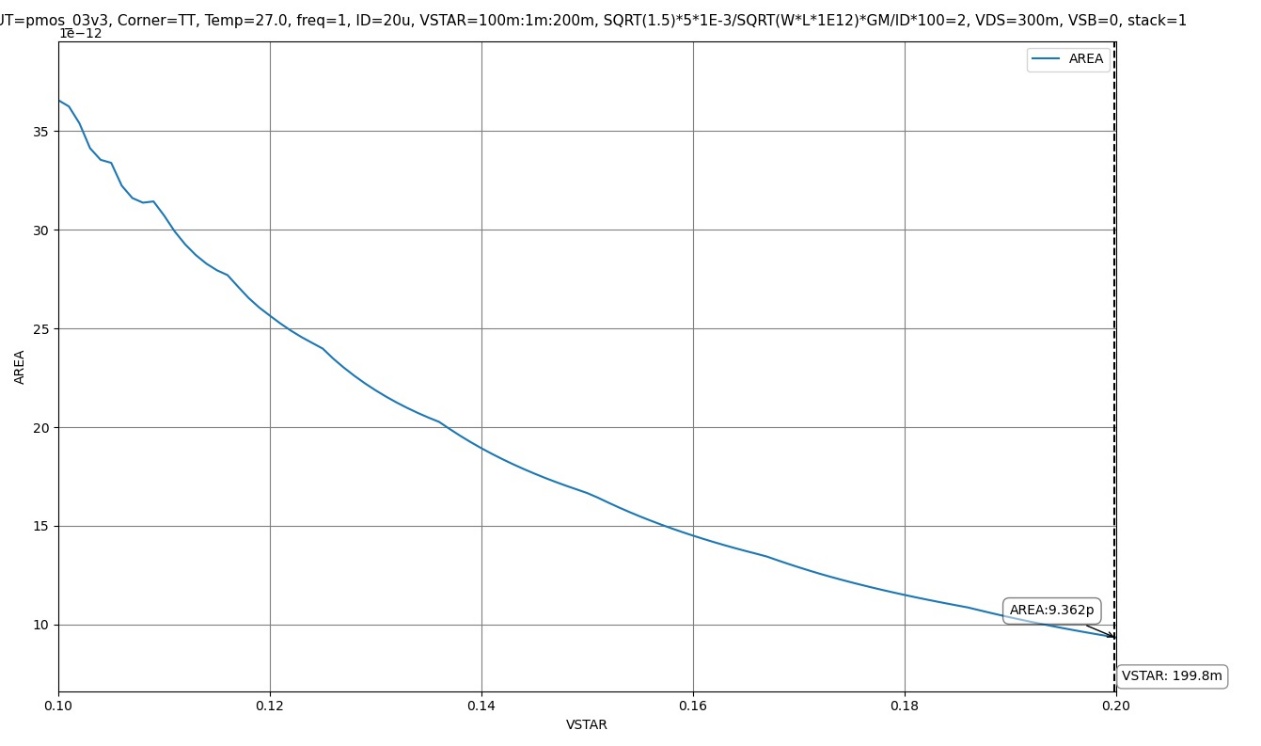


Figure 7 Area at Required Vstar

CM Input Level:

The chosen VICM is a little close to the max input but has enough headroom, ideally though it should be at the average between the Max and Min

Part 2: Differential Amplifier

A computer screen shot of a computer circuit

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Figure 8 Differential Amplifier Schematic

A screenshot of a computer

AI-generated content may be incorrect.

Figure 9 Testbench Schematic

OP Simulation:  
A screenshot of a computer

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Figure 10 Operating Point of All Transitors

Note: xschem doesn’t have support for the region variable.

All transistors appear to be in Saturation!

Diff Small Signal CCS:

A screen shot of a graph

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Figure 11 Bode Plot of Diff Gain

A black screen with blue and white dots

AI-generated content may be incorrect.

Figure 12 Gain and BW from Simulation

**Analytical Solution**:

|  |  |  |
| --- | --- | --- |
|  | Analytical | Simulation |
| Diff Gain | 7.769 | 7.742 |
| Diff Gain (dB) | 17.8 dB | 17.78 dB |
| BW | 5.3MHz | 5.66MHz |

CM Small Signal CCS:

A screen shot of a graph

AI-generated content may be incorrect.

Figure 13 AvCM Bode Plot



Figure 14 CM gain from Simulation

**Analytical Solution:**

|  |  |  |
| --- | --- | --- |
|  | Analytical | Simulation |
| CM Gain | 6.53e-2 | 6.4e-2 |
| CM Gain (dB) | -23.69 dB | -23.87 dB |

The common mode gain experiences a Pole then a Zero then another Pole at very high frequencies, the Pole caused by the high impedance node at the current source node causes it to fall till it reaches the zero also caused by the same node due to the parasitic capacitances seen at it (CP).



CMRR:

A graph with green lines

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Figure 15 CMRR vs Frequency Bode Plot

A black background with white numbers

AI-generated content may be incorrect.

Figure 16 CMRR Value from Simulation

Analytical Solution:

|  |  |  |
| --- | --- | --- |
|  | Analytical | Simulation |
| CMRR | 130.5 | 42.27 |
| CMRR | 121.3 | 41.68 dB |

At high frequencies parasitic capacitances at the RSS node cause it to short significantly decreasing CMRR as we increase frequency.

Diff Large Signal CCS:

A graph with green lines

AI-generated content may be incorrect.

Figure 17 VODIFF vs VIDIFF

Analytical Solution:

At Extreme points current is steered completely into one of the two transistors while the other turns off thus Vodiff = Vpos only or Vneg only

|  |  |  |
| --- | --- | --- |
|  | Analytical | Simulation |
| VODIFF Extreme | 1.2 | 1.76 |

The simulation result is slightly less than the Analytical result due to current mirror errors, the current steered into the transistor is slightly less than 40uA as used in the calculations resulting in slightly less voltage.

CM Large Signal CCS:

A graph on a black background

AI-generated content may be incorrect.

Figure 18 GBW vs VICM

A number on a black background

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Figure 19 VINCM Range from Simulation

Analytic Solution:  
Using the same expressions derived during sizing we can find the the input range but using the results from the OP analysis

|  |  |  |
| --- | --- | --- |
|  | Analytical | Simulation |
| VINCM Minimum | -0.303 | -0.44 |
| VINCM Maximum | 0.689 | 0.8 |