**Lab 7**

OTA Design

Part 1: gm/ID Design Charts

NMOS Charts:

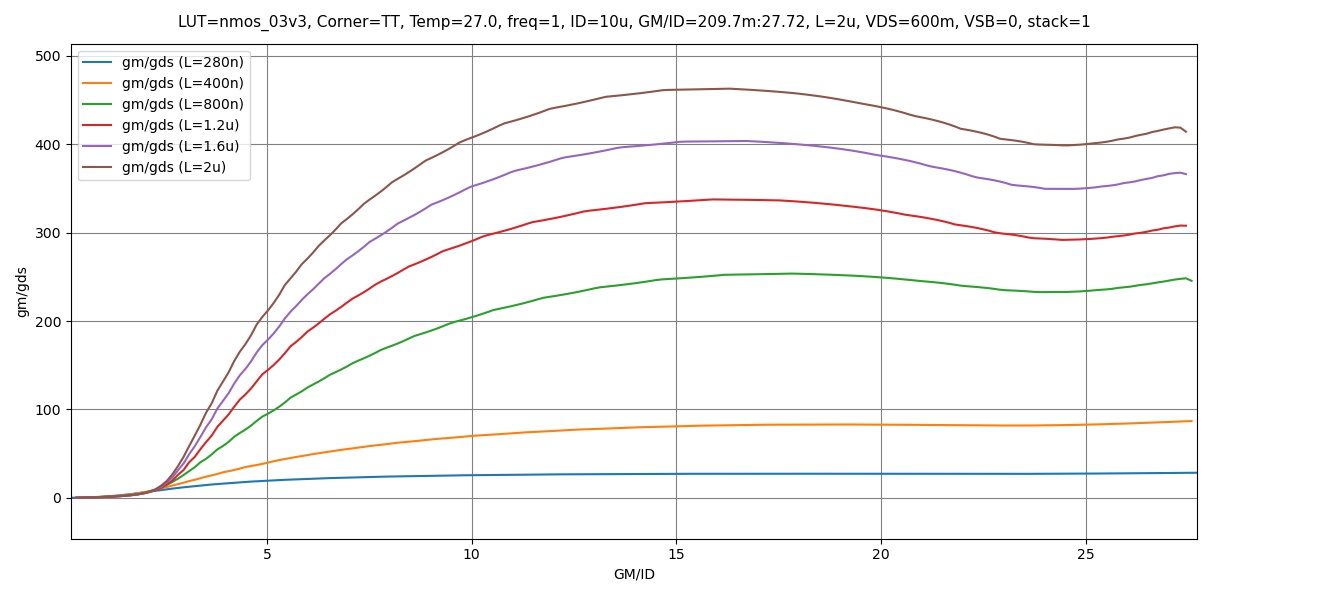


Figure gm/gds vs gm/id

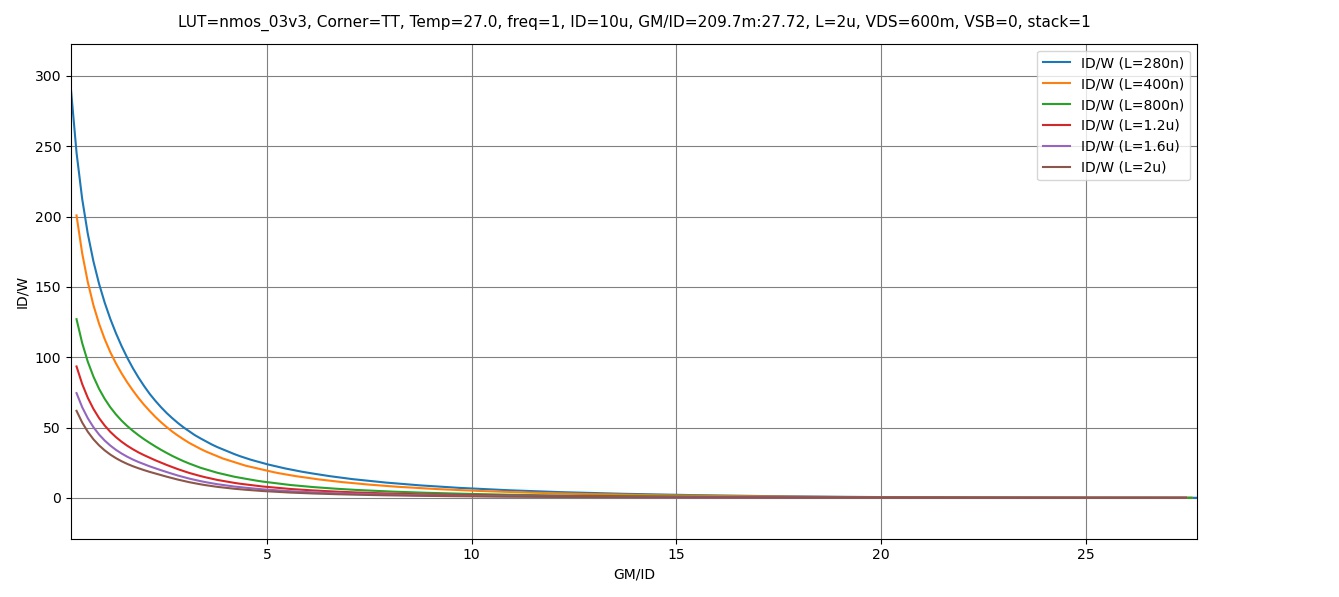


Figure ID/W vs gm/ID

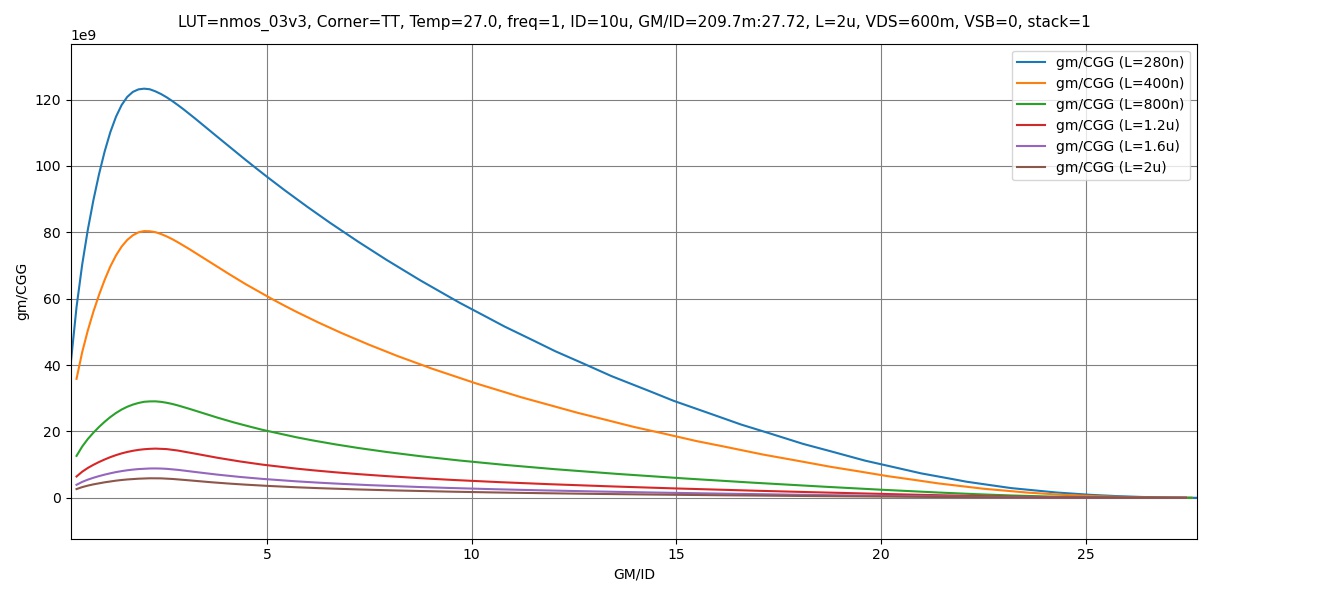


Figure gm/Cgg vs gm/ID

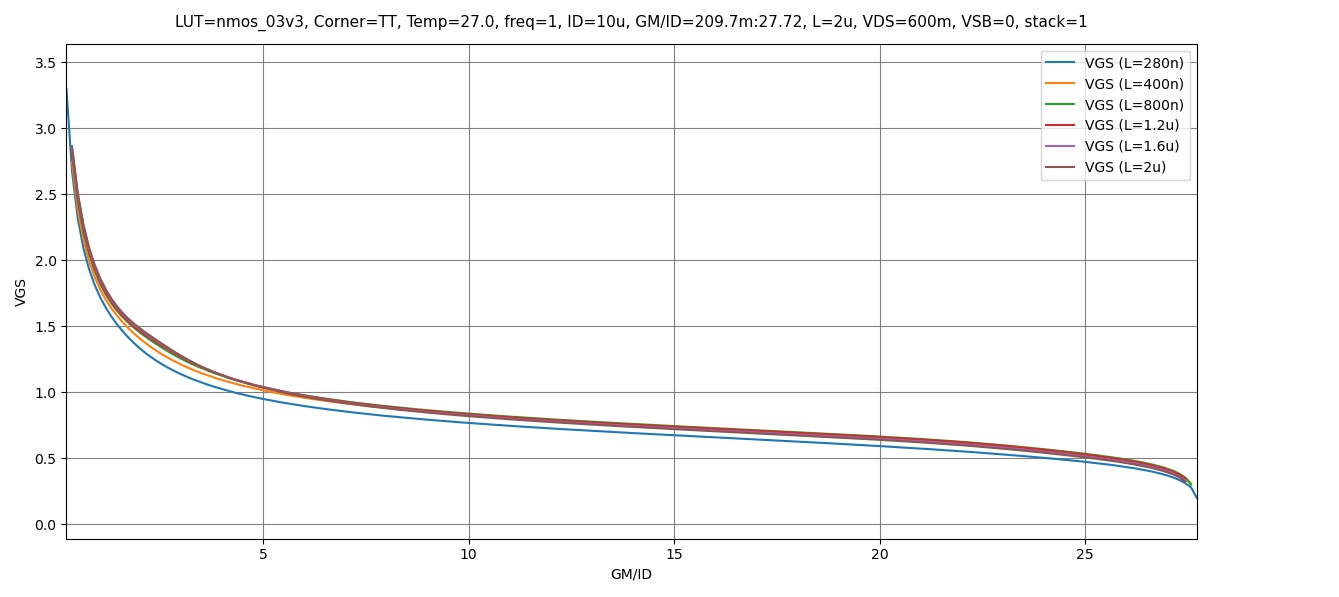


Figure VGS vs gm/ID

PMOS Charts:

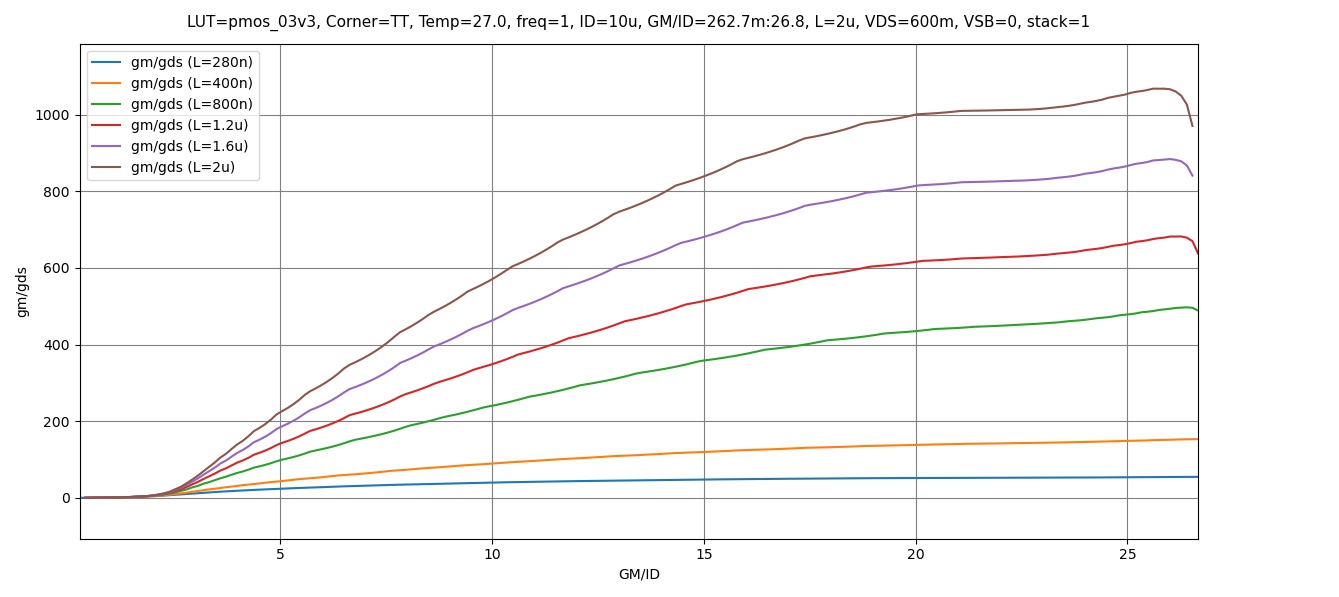


Figure gm/gds vs gm/ID

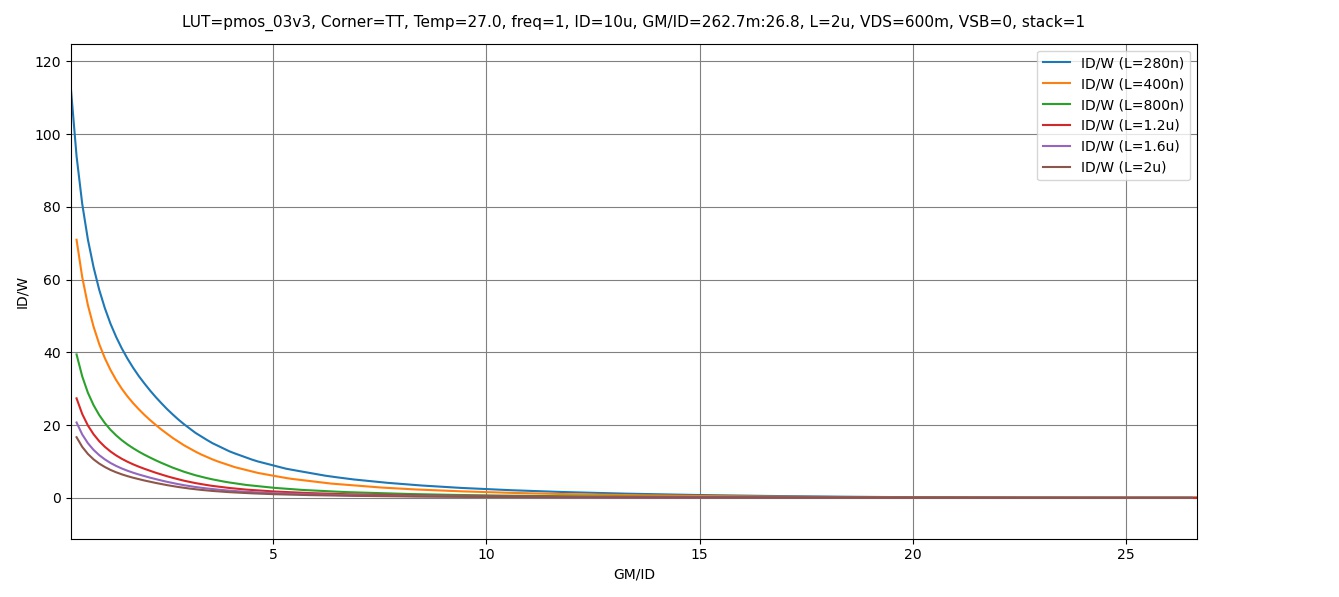


Figure ID/W vs gm/ID

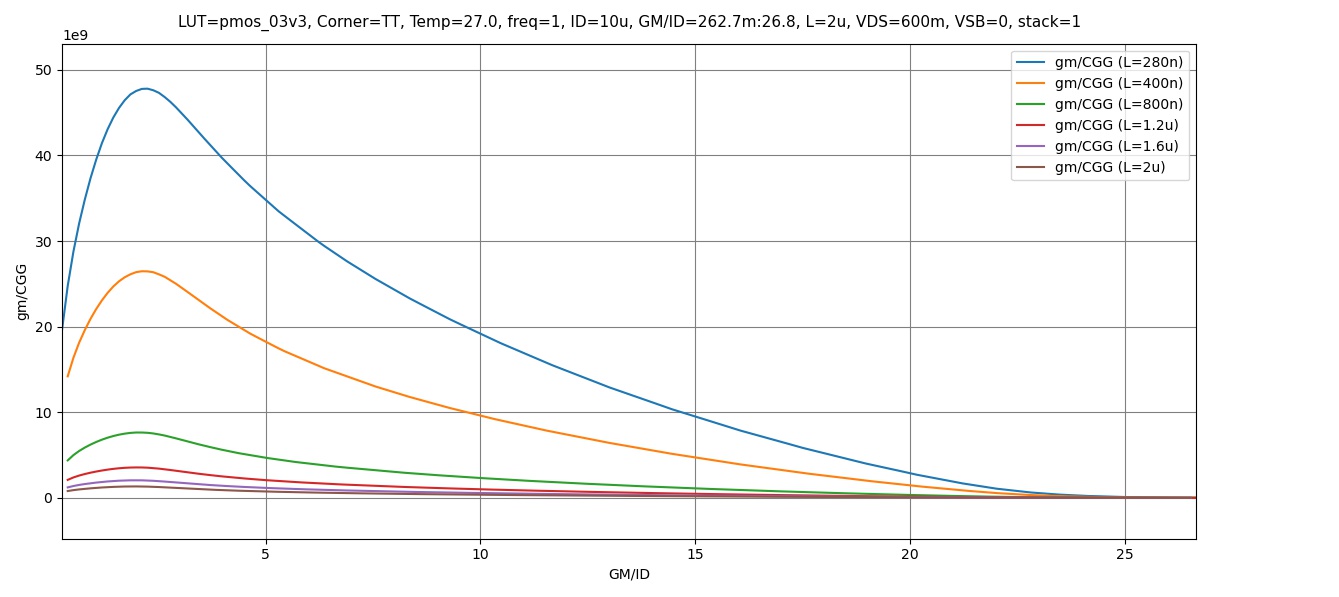


Figure gm/Cgg vs gm/ID

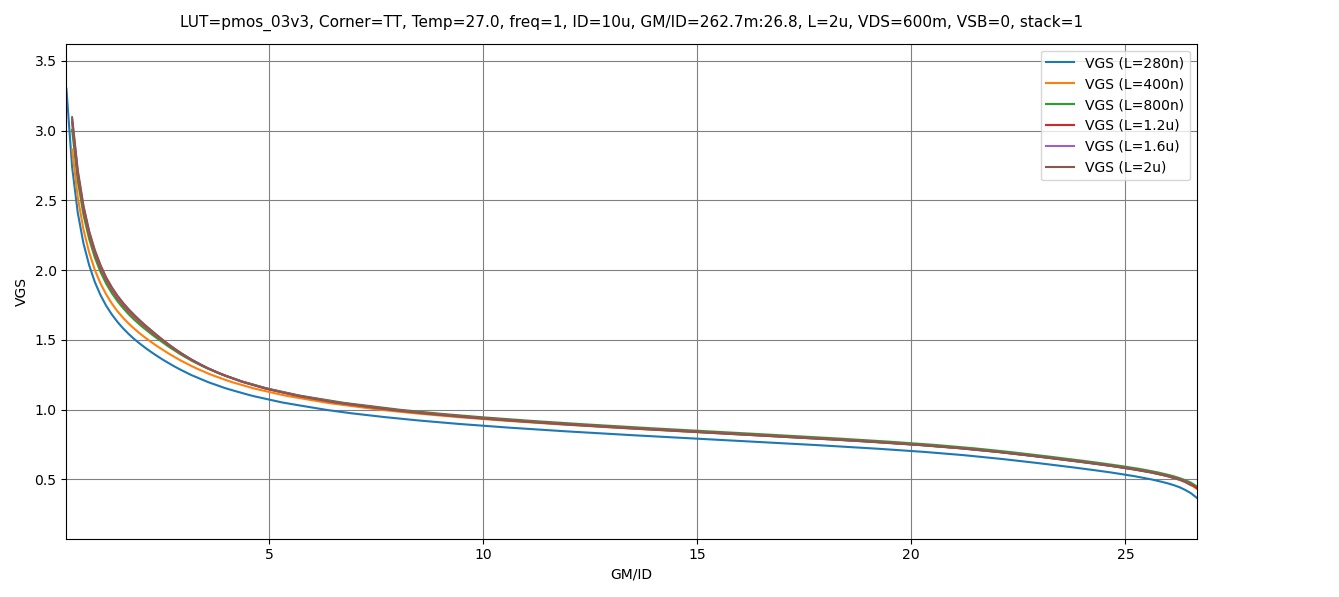


Figure VGS vs gm/ID

Part 2: OTA Design

Required Specifications:

|  |  |
| --- | --- |
| Technology | 0.18um CMOS |
| Supply voltage | 1.8V |
| Load | 5pF |
| Open loop DC voltage gain | >= 34dB |
| CMRR @ DC1 | >= 74dB |
| Phase margin | >= 70o |
| CM input range – low | <= 1V |
| CM input range – high | >= 1.5V |
| GBW | >= 10MHz |

Design Observations:

* The Gain required isn’t too large and easily achievable using a single stage OTA
* The CMIR required is close to the Supply Rail, Thus an NMOS input stage is preferred.
* The specification can be met using a 5T-OTA topology

We have to size 3 pairs of MOSFETS.

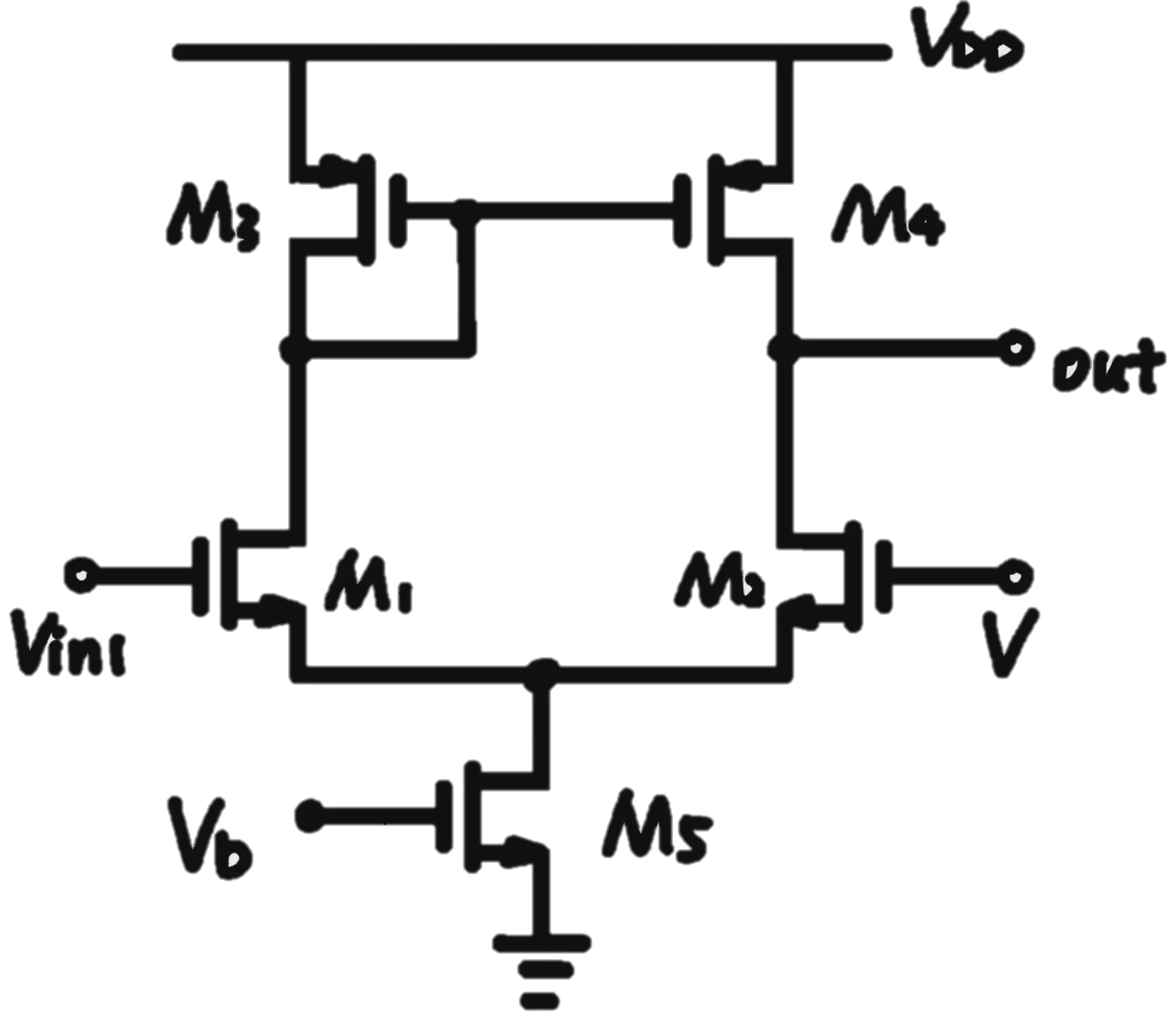


Figure 5T OTA Topology

Input Transistors:

**Assuming the Voltage Drop is divided equally across all 3 transistors in branch, VDS of each transistor = 0.6V**

**M1,2 Experience Body Effect, thus VSB = 0.6**

**We may assume a lesser voltage drop at the bottom transistor to 0.3 thus Vds = 0.9V**

Using these three parameters we can get the width and length of the input pair quickly using ADT:

A screenshot of a computer

AI-generated content may be incorrect.

Figure Intial Values for the input pair from SA

These are acceptable values for the Input Pair and decent for initial design!

PMOS Current Mirror Load:

Using CMIR-Max:

Using assumptions from the previous part:

Plugging in these Values in ADT SA we get:

A screenshot of a computer

AI-generated content may be incorrect.

Figure Initial Values for the PMOS Current Mirror Load Pair from SA

These are acceptable values for the Input Pair and decent for initial design!

Tail Current Mirror Sizing:

For the purposes of this design, I will use a simple current mirror at the tail.

Using the spec for CMRR:

Using the Spec for CMIR-Low:

Plugging in these Values into ADT SA:

A screenshot of a computer

AI-generated content may be incorrect.

Figure Initial Values for the Tail Current Mirror Load Pair from SA

The Value for the width is extremely high especially considering I need to multiply it by 4 for the mirroring ratio.

Thus I will assume an initial Value of W of 40um and slightly increase the Width of M1,2 then iterate the design till I reach acceptable Values for the transistor that satisfy the specifications.

Initial Design Point:

|  |  |  |  |
| --- | --- | --- | --- |
|  | M1,2 | M3,4 | M5,6 |
| W | 16.72um | 320nm | 40um |
| L | 430nm | 2.57um | 2.43um |
| ID | 20uA | 20uA | 40uA |
| gm/ID | 16 | 20 | 9.2 |
| VDsat | 101.4mV | 62.6mV | 169.5mV |
| Vov | 25.91mV | -22.39mV | 170.8mV |
| Vstar | 125mV | 100mV | 217.4mV |

Simulation and Design Iteration:

A computer screen shot of a diagram

AI-generated content may be incorrect.

Figure 5T OTA Schematic After Iterations

After very Few iterations these are the values, I reached for all transistors that satisfy all specs.