**Lab 7**

OTA Design

Part 1: gm/ID Design Charts

NMOS Charts:

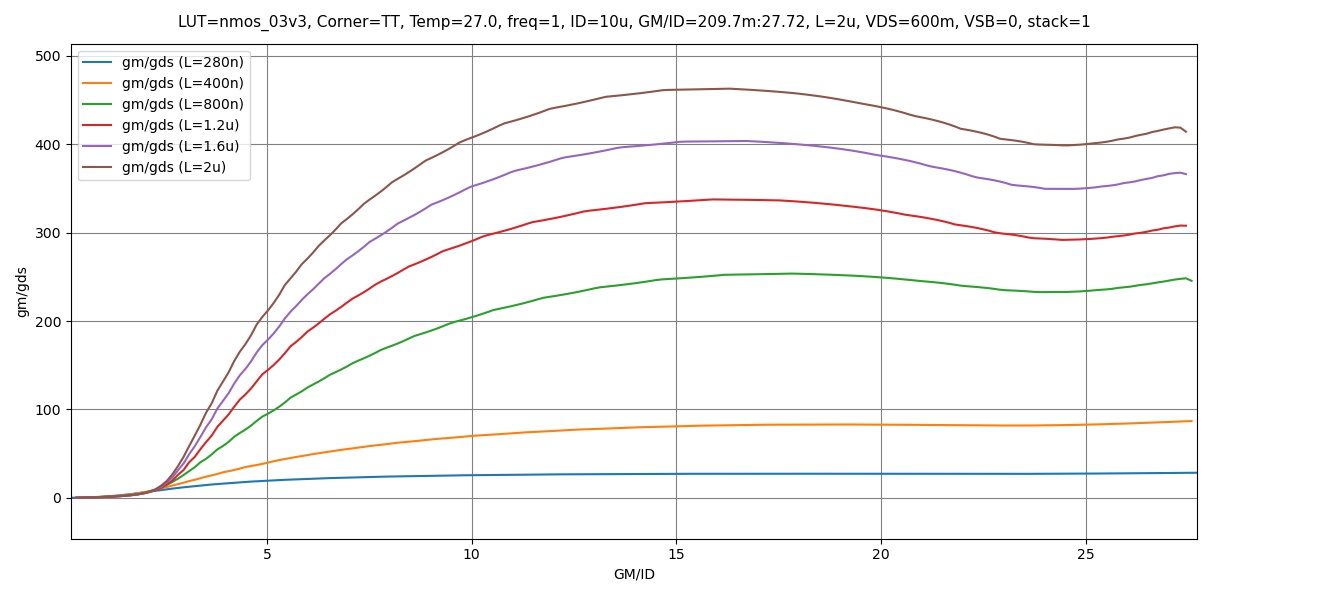


Figure 1 gm/gds vs gm/id

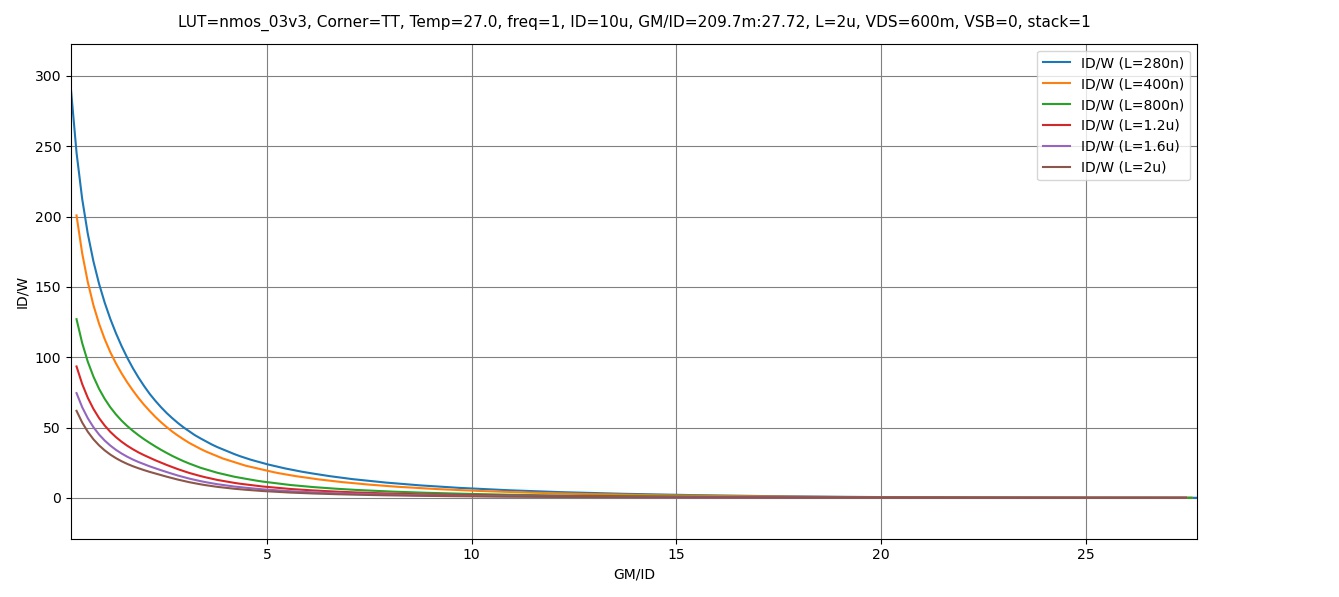


Figure 2 ID/W vs gm/ID

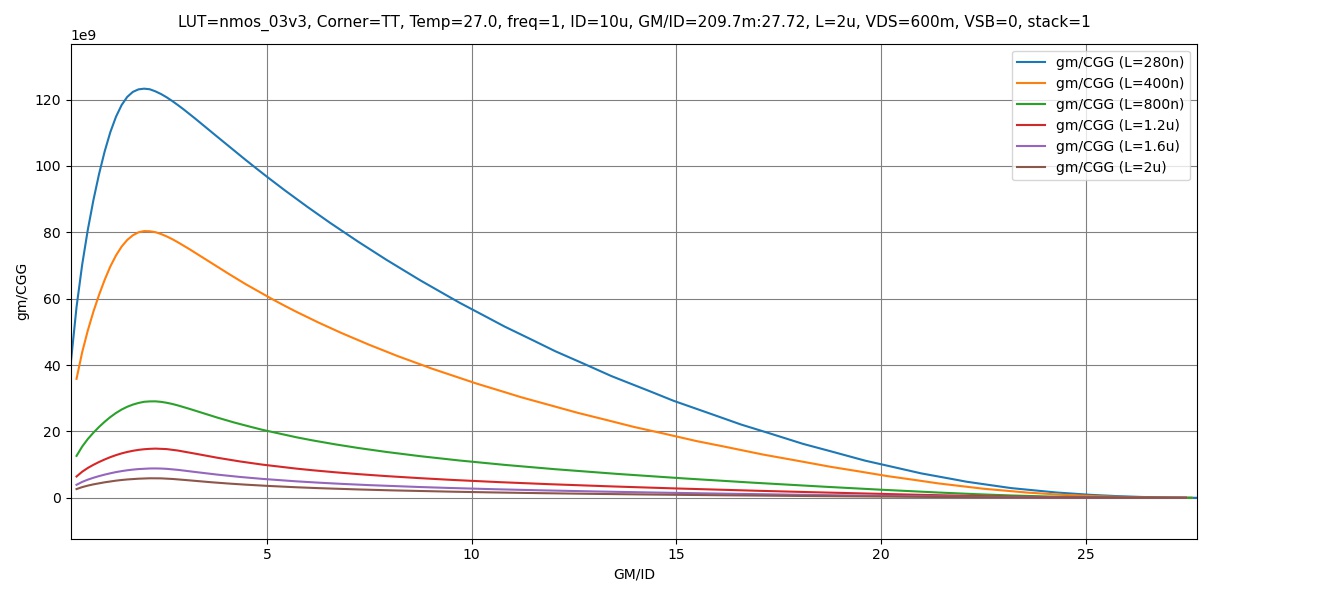


Figure 3 gm/Cgg vs gm/ID

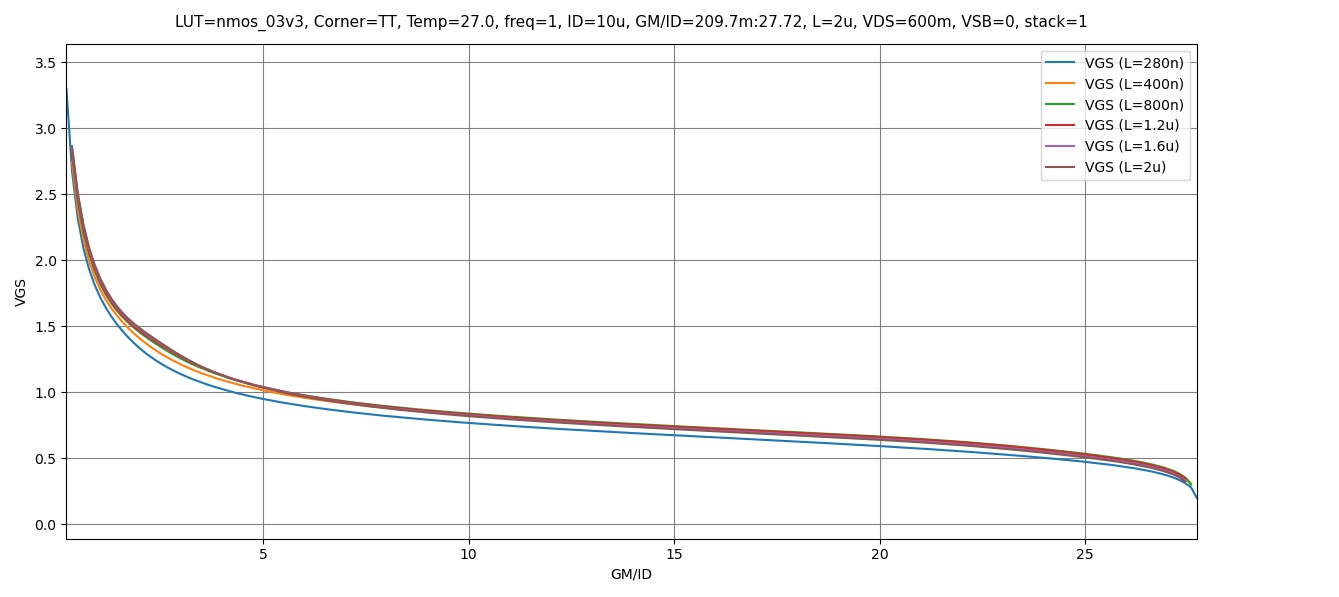


Figure 4 VGS vs gm/ID

PMOS Charts:

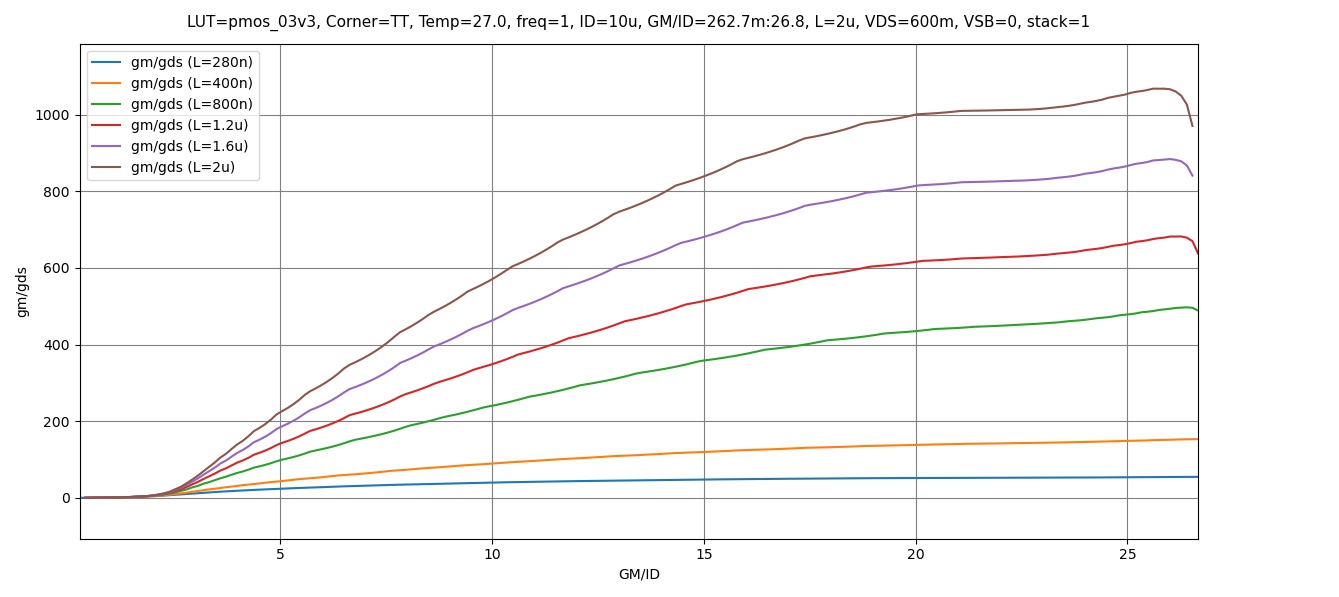


Figure 5 gm/gds vs gm/ID

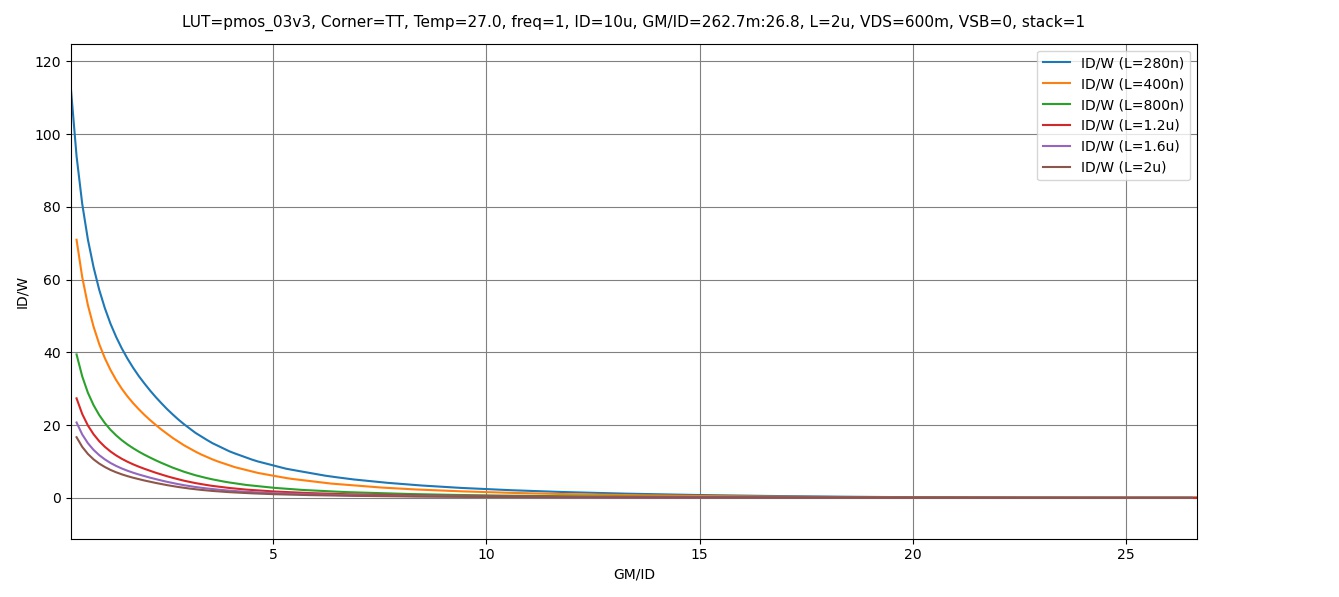


Figure 6 ID/W vs gm/ID

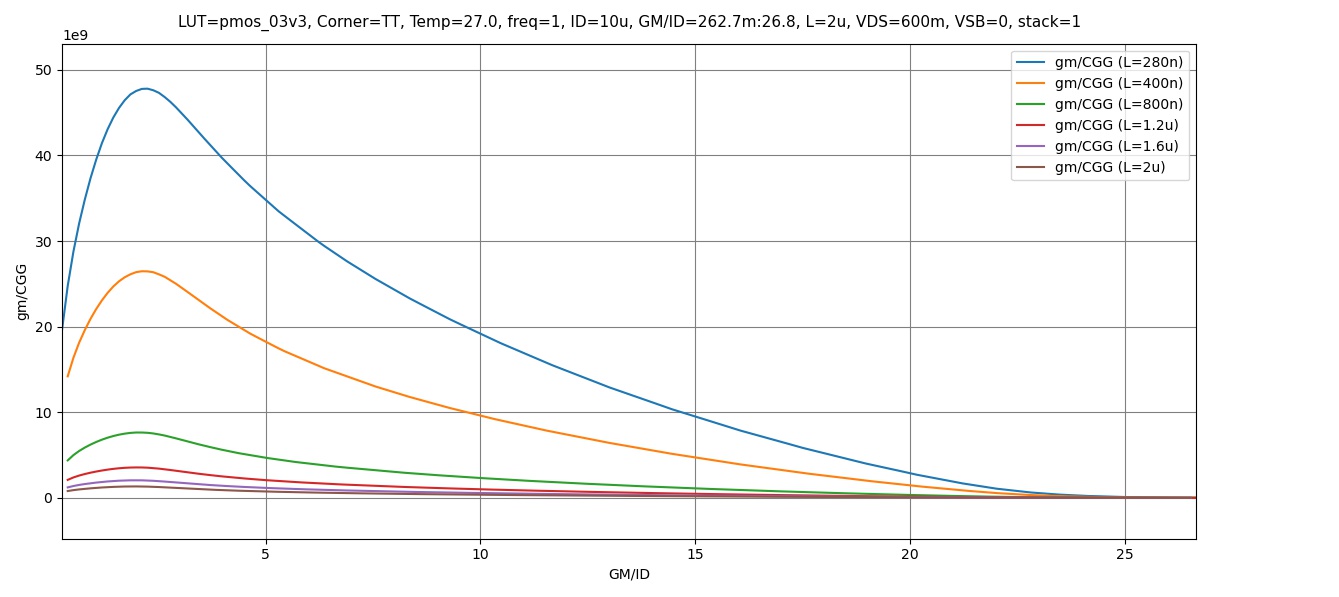


Figure 7 gm/Cgg vs gm/ID

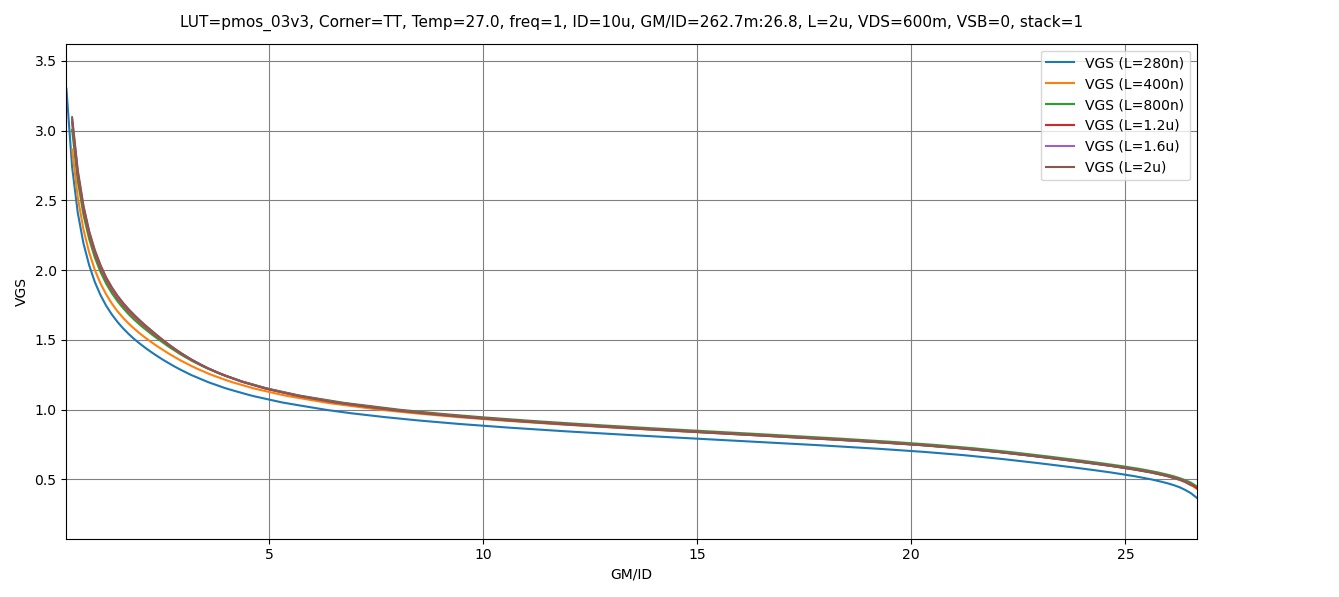


Figure 8 VGS vs gm/ID

Part 2: OTA Design

Required Specifications:

|  |  |
| --- | --- |
| Technology | 0.18um CMOS |
| Supply voltage | 1.8V |
| Load | 5pF |
| Open loop DC voltage gain | >= 34dB |
| CMRR @ DC1 | >= 74dB |
| Phase margin | >= 70o |
| CM input range – low | <= 1V |
| CM input range – high | >= 1.5V |
| GBW | >= 10MHz |

Design Observations:

* The Gain required isn’t too large and easily achievable using a single stage OTA
* The CMIR required is close to the Supply Rail, Thus an NMOS input stage is preferred.
* The specification can be met using a 5T-OTA topology

We have to size 3 pairs of MOSFETS.

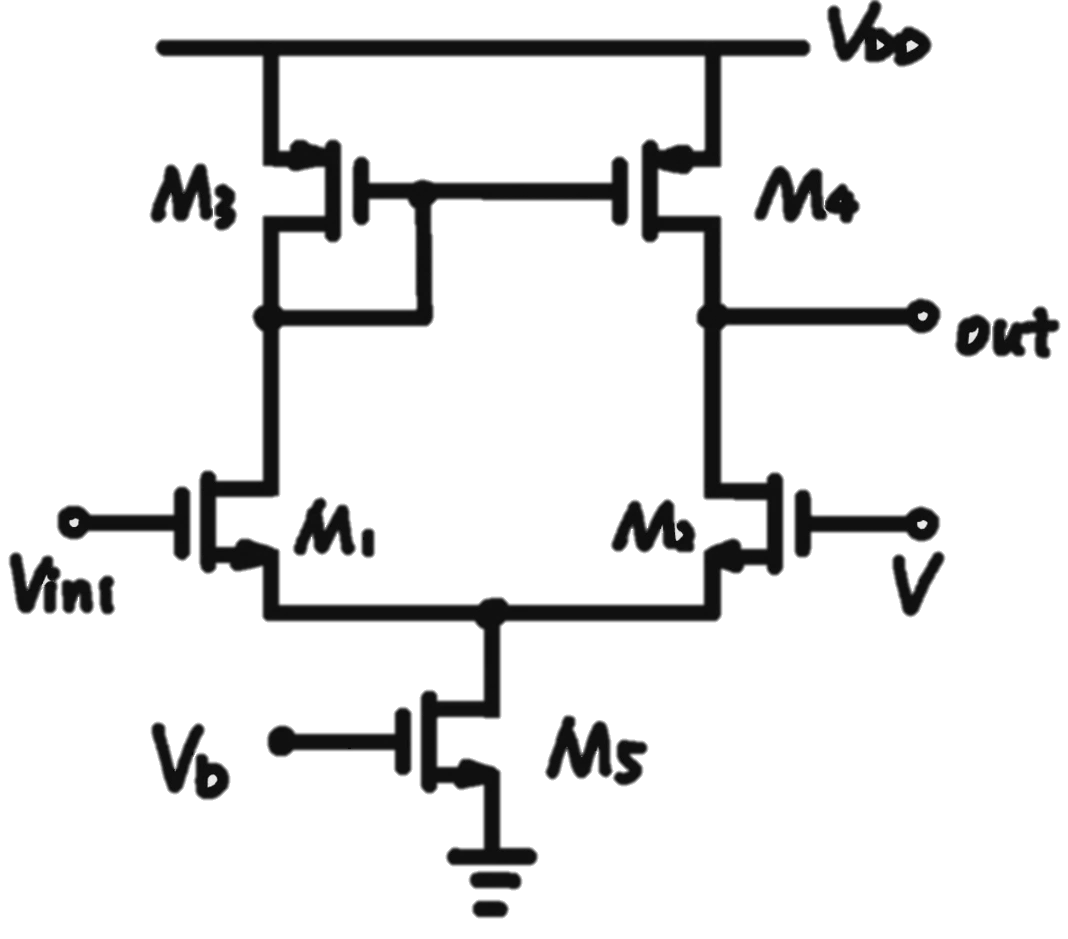


Figure 9 5T OTA Topology

Input Transistors:

Assuming the Voltage Drop is divided equally across all 3 transistors in branch, VDS of each transistor = 0.6V

M1,2 Experience Body Effect, thus VSB = 0.6

We may assume a lesser voltage drop at the bottom transistor to 0.3 thus Vds = 0.9V

Using these three parameters we can get the width and length of the input pair quickly using ADT:

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Figure 10 Intial Values for the input pair from SA

These are acceptable values for the Input Pair and decent for initial design!

PMOS Current Mirror Load:

Using CMIR-Max:

Using assumptions from the previous part:

Plugging in these Values in ADT SA we get:

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Figure 11 Initial Values for the PMOS Current Mirror Load Pair from SA

These are acceptable values for the Input Pair and decent for initial design!

Tail Current Mirror Sizing:

For the purposes of this design, I will use a simple current mirror at the tail.

Using the spec for CMRR:

Using the Spec for CMIR-Low:

Plugging in these Values into ADT SA:

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Figure 12 Initial Values for the Tail Current Mirror Load Pair from SA

The Value for the width is extremely high especially considering I need to multiply it by 4 for the mirroring ratio.

Thus I will assume an initial Value of W of 40um and slightly increase the Width of M1,2 then iterate the design till I reach acceptable Values for the transistor that satisfy the specifications.

Initial Design Point:

|  |  |  |  |
| --- | --- | --- | --- |
|  | M1,2 | M3,4 | M5,6 |
| W | 16.72um | 320nm | 40um |
| L | 430nm | 2.57um | 2.43um |
| ID | 20uA | 20uA | 40uA |
| gm/ID | 16 | 20 | 9.2 |
| VDsat | 101.4mV | 62.6mV | 169.5mV |
| Vov | 25.91mV | -22.39mV | 170.8mV |
| Vstar | 125mV | 100mV | 217.4mV |

Simulation and Design Iteration:

A computer screen shot of a diagram

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Figure 13 5T OTA Schematic After Iterations

After very Few iterations these are the values, I reached for all transistors that satisfy all specs.

Final Design Point:

|  |  |  |  |
| --- | --- | --- | --- |
|  | M1,2 | M3,4 | M5,6 |
| W | 20um | 3.5um | 40um |
| L | 450nm | 330nm | 2.2um |
| ID | 20uA | 20uA | 40uA |
| gm/ID | 11 | 5 | 5 |
| VDsat | 156.1mV | 303.9mV | 300mV |
| Vov | 131.5mV | 307.3mV | 389.2mV |
| Vstar | 181.8mV | 389.5mV | 422mV |

These values were calculated at different VDS and VSB values matching the assumptions we did during the design stage but they differ greatly when doing the simulation as we’ll see in the following results.

Simulation and Results:

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Figure 14 Testbench Schematic for first part

OP Analysis:

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|  |  |  |  |
| --- | --- | --- | --- |
|  | M1,2 | M3,4 | M5,6 |
| gm/ID | 16.364 | 5.965 | 9.796 |
| Vov | 16.2mV | 287.51mV | 155.018mV |
| Vstar | 122.22mV | 335.3mV | 204.16mV |

Figure 15 OP Analysis Results for all transistors

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Figure 16 DC Voltages Annotated in Testbench

A computer screen shot of a diagram

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Figure 17 Voltages Annotated on 5T OTA Schematic

• Is the current (and gm) in the input pair exactly equal?

Yes, the current is exactly equal in both transistors of the input pair.

• What is DC voltage at VOUT? Why?

There’s a virtual short-circuit between the drain and gate of M3 cause both Vout and V1 to have the same voltage.

Differential Small Signal:

A graph with lines and numbers

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Figure 18 Diff Gain (dB )vs Frequency

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Figure 19 Diff Gain Values

**Hand Analysis:**

Using Values from OP Analysis:

|  |  |  |
| --- | --- | --- |
|  | Simulation | Hand Analysis |
| Gain | 53.415 | 54.46 |
| Gain (dB) | 34.55 | 34.7213 |

Hand analysis and simulation results agree with each other and satisfy the required spec.

CM Small Signal:

A graph with green lines

AI-generated content may be incorrect.

Figure 20 CM Gain (dB) vs Frequency



Figure 21 CM Gain Values

**Hand Analysis:**

Using Values from OP Analysis:

|  |  |  |
| --- | --- | --- |
|  | Simulation | Hand Analysis |
| Gain | 4.095e-3 | 5.0578e-3 |
| Gain (dB) | -47.75 | -45.92 |

Hand analysis and simulation results agree with each other.

CMRR:

A graph with green lines

AI-generated content may be incorrect.

Figure 22 CMRR vs Freq from simulation

**Hand Analysis:**

Using Diff and CM gain values from last 2 parts:

|  |  |  |
| --- | --- | --- |
|  | Simulation | Hand Analysis |
| Gain (dB) | 82.31 | 80.6413 |

Hand analysis and simulation results agree with each other and satisfy the required spec.

Diff Large Signal:

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Figure 23 VOUT vs Vid

What is the value of Vout at VID = 0? Why?

**,**  Same Value as Vout calculated During OP Analysis, This is the Quiescent point of the amplifier

A graph with green lines

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Figure 24 Derivates of Vout vs Vid



Figure 25 Value at the Peak

The Value of the derivative of Vout vs Vid is the DC Gain, the value at the peak=**58.87** is observed to be slightly higher than Avd=**53.415** but still comparable to it

CM Large Signal:

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Figure 26 CMIR From Simulation

The result meets the required spec

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Figure 27 GBW vs VCIM wiht VCIM Annotated

The result for GBW meets the required specifications inside the input range!

**If you are using NMOS input pair, body effect may cause CMIR to extend till VDD (why?).**

As Increasing the VSB of M1,2 Transistors can increase the Maximum to be higher than VDD also increasing the width of M3,4 decreases their VGS thus increasing the VICM-Max as well

Part 4: Closed Loop OTA Simulation:

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Figure 28 Closed Loop Testbench

A screenshot of a computer screen

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Figure 29 OP Point in Feedback Configuration

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | M1 | M2 | M3 | M4 | M5 |
| gm/ID | 16.457 | 16.528 | 5.997 | 5.981 | 8.9147 |
| Vov | 12.88mV | 10.8mV | 285.753mV | 286.719mV | 857mV |
| Vstar | 121.52mV | 121mV | 333.48mV | 334.37mV | 224.34mV |

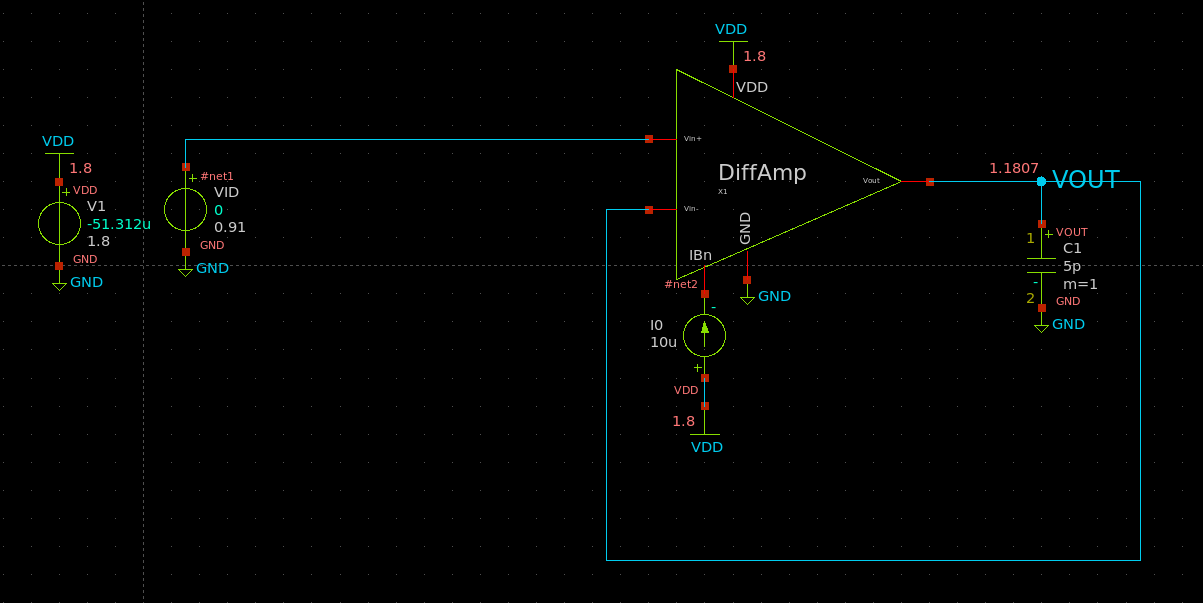


Figure 30 DC Voltages Annotated in TB Schematic

A computer screen shot of a circuit

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Figure 31 Dc Voltages Annotated in OTA

• **Is the current (and gm) in the input pair exactly equal? Why?**

No, there is a slight mismatch between them. As the output node voltage deviates from its CM value to match the input value resulting in a non-zero differential input causing a mismatch

• **Calculate the mismatch in 𝐼𝐷 and gm.**

Loop Gain:

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Figure 32 STB Simulation Testbench

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Figure 33 STB Simulation Results

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Figure 34 Loop Gain (dB) vs Frequency

A graph with green line

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Figure 35 Loop Gain Phase vs Frequency

Compare DC gain and GBW with those obtained from open-loop simulation

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Figure 36 Closed Loop Gain in dB vs Frequency

The Amplifier works as a buffer in this configuration thus the gain is approximately equal to 0dB (Unity Gain).

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Figure 37 Closed Loop Bandwidth

Compared to open loop simulation the closed loop gain here is unity but we can see the GBW is approximately the same, this is because the BW from the open loop simulation was increased by a factor of which is approximately equal to multiplied by the unity gain of this configuration gives us equivalent GBW for both Open Loop and Closed Loop.

Hand Analysis:

|  |  |  |
| --- | --- | --- |
|  | Simulation | Hand Analysis |
| Beta | 1 | 1 |
| Loop Gain | 53.395 | 58.479 |
| Loop Gain (dB) | 34.55 | 35.34 |
| Closed Loop Gain | 0.9827 | 0.9816 |
| Closed Loop Gain (dB) | -0.1516 | -0.1611 |

The Open Loop gain in this configuration is slightly higher than the open loop gain from the simulation in the previous part this is due to the slight mismatch (verr) changing the q-point and increasing the gain a little bit close to the Maximum.

Other than that, Analytic Results agree with Hand Analysis for the most part.

Conclusion:

Comparing Achieved Spec with Required:

|  |  |  |
| --- | --- | --- |
| Specification | Required | Achieved |
| Supply voltage | 1.8V | 1.8V |
| Load | 5pF | 5pF |
| Open loop DC voltage gain | >= 34dB | 34.55 |
| CMRR @ DC | >= 74dB | 82.31 |
| Phase margin | >= 70o | 89.7o |
| CM input range – low | <= 1V | 0.86V |
| CM input range – high | >= 1.5V | 1.516 |
| GBW | >= 10MHz | 10.413MHz |

Using the gm/Id Methodology and a little bit of fine tuning via iterations I was able to achieve the required specification with relatively small area.