# Register Description

### SYSCON\_RST\_SW\_SET

Offset Address: 0x40000000

block software reset set register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SET\_FC0\_RST | rw | 0 | 1'b0 | Write 1 to set FLEXCOMM0 reset |
| SET\_FC1\_RST | rw | 1 | 1'b0 | Write 1 to set FLEXCOMM1 reset |
| SET\_FC2\_RST | rw | 2 | 1'b0 | Write 1 to set FLEXCOMM2 reset |
| SET\_FC3\_RST | rw | 3 | 1'b0 | Write 1 to set FLEXCOMM3 reset |
| SET\_TIM0\_RST | rw | 4 | 1'b0 | Write 1 to set CTIMER0 reset |
| SET\_TIM1\_RST | rw | 5 | 1'b0 | Write 1 to set CTIMER1 reset |
| SET\_TIM2\_RST | rw | 6 | 1'b0 | Write 1 to set CTIMER2 reset |
| SET\_TIM3\_RST | rw | 7 | 1'b0 | Write 1 to set CTIMER3 reset |
| SET\_SCT\_RST | rw | 8 | 1'b0 | Write 1 to set SCT reset |
| SET\_WDT\_RST | rw | 9 | 1'b0 | Write 1 to set Watch Dog reset |
| SET\_USB\_RST | rw | 10 | 1'b0 | Write 1 to set USB reset |
| SET\_GPIO\_RST | rw | 11 | 1'b0 | Write 1 to set GPIO reset |
| SET\_RTC\_RST | rw | 12 | 1'b0 | Write 1 to set RTC reset |
| SET\_ADC\_RST | rw | 13 | 1'b0 | Write 1 to set ADC interface reset |
| SET\_DAC\_RST | rw | 14 | 1'b0 | Write 1 to set DAC interface reset |
| SET\_CS\_RST | rw | 15 | 1'b0 | Write 1 to set Cap sensor interface reset |
| SET\_FSP\_RST | rw | 16 | 1'b0 | Write 1 to set FSP reset |
| SET\_DMA\_RST | rw | 17 | 1'b0 | Write 1 to set DMA reset |
| Reserved | rw | 18 | 1'b0 | Reserved |
| SET\_QDEC0\_RST | rw | 19 | 1'b0 | Write 1 to set QDEC 0 reset |
| SET\_QDEC1\_RST | rw | 20 | 1'b0 | Write 1 to set QDEC 1 reset |
| Reserved | rw | 21 | 1'b0 | Reserved |
| SET\_SPIFI\_RST | rw | 22 | 1'b0 | Write 1 to set SPIFI reset |
| Reserved | rw | 25:23 | 3'b0 | Reserved |
| SET\_CPU\_RST | rw | 26 | 1'b0 | Write 1 to set CPU reset |
| SET\_BLE\_RST | rw | 27 | 1'b0 | Write 1 to set BLE reset |
| SET\_FLASH\_RST | rw | 28 | 1'b0 | Write 1 to set flash controller reset |
| SET\_DP\_RST | rw | 29 | 1'b0 | Write 1 to set DataPath reset |
| SET\_REG\_RST | rw | 30 | 1'b0 | Write 1 to reset retention register |
| SET\_REBOOT | rw | 31 | 1'b0 | Write 1 to Reboot entire system |

### SYSCON\_RST\_SW\_CLR

Offset Address: 0x40000004

block software reset clear register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CLR\_FC0\_RST | rw | 0 | 1'b0 | Write 1 to clear FLEXCOMM0 reset |
| CLR\_FC1\_RST | rw | 1 | 1'b0 | Write 1 to clear FLEXCOMM1 reset |
| CLR\_FC2\_RST | rw | 2 | 1'b0 | Write 1 to clear FLEXCOMM2 reset |
| CLR\_FC3\_RST | rw | 3 | 1'b0 | Write 1 to clear FLEXCOMM3 reset |
| CLR\_TIM0\_RST | rw | 4 | 1'b0 | Write 1 to clear CTIMER0 reset |
| CLR\_TIM1\_RST | rw | 5 | 1'b0 | Write 1 to clear CTIMER1 reset |
| CLR\_TIM2\_RST | rw | 6 | 1'b0 | Write 1 to clear CTIMER2 reset |
| CLR\_TIM3\_RST | rw | 7 | 1'b0 | Write 1 to clear CTIMER3 reset |
| CLR\_SCT\_RST | rw | 8 | 1'b0 | Write 1 to clear SCT reset |
| CLR\_WDT\_RST | rw | 9 | 1'b0 | Write 1 to clear Watch Dog reset |
| CLR\_USB\_RST | rw | 10 | 1'b0 | Write 1 to clear USB reset |
| CLR\_GPIO\_RST | rw | 11 | 1'b0 | Write 1 to clear GPIO reset |
| CLR\_RTC\_RST | rw | 12 | 1'b0 | Write 1 to clear RTC reset |
| CLR\_ADC\_RST | rw | 13 | 1'b0 | Write 1 to clear ADC interface reset |
| CLR\_DAC\_RST | rw | 14 | 1'b0 | Write 1 to clear DAC interface reset |
| CLR\_CS\_RST | rw | 15 | 1'b0 | Write 1 to clear cap sensor interface reset |
| CLR\_FSP\_RST | rw | 16 | 1'b0 | Write 1 to clear FSP reset |
| CLR\_DMA\_RST | rw | 17 | 1'b0 | Write 1 to clear DMA reset |
| Reserved | rw | 18 | 1'b0 | Reserved |
| CLR\_QDEC0\_RST | rw | 19 | 1'b0 | Write 1 to clear QDEC 0 reset |
| CLR\_QDEC1\_RST | rw | 20 | 1'b0 | Write 1 to clear QDEC 1 reset |
| Reserved | rw | 21 | 1'b0 | Reserved |
| CLR\_SPIFI\_RST | rw | 22 | 1'b0 | Write 1 to clear SPIFI reset |
| Reserved | rw | 25:23 | 3'b0 | Reserved |
| CLR\_CPU\_RST | rw | 26 | 1'b0 | Write 1 to clear CPU reset |
| CLR\_BLE\_RST | rw | 27 | 1'b0 | Write 1 to clear BLE reset |
| CLR\_FLASH\_RST | rw | 28 | 1'b0 | Write 1 to clear flash controller reset |
| CLR\_DP\_RST | rw | 29 | 1'b0 | Write 1 to clear DataPath reset |
| CLR\_REG\_RST | rw | 30 | 1'b0 | Write 1 to clear retention register reset |
| Reserved | rw | 31 | 1'b0 | Reserved |

### SYSCON\_CLK\_DIS

Offset Address: 0x40000008

clock disable register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CLK\_FC0\_DIS | rw | 0 | 1'b0 | Write 1 to disable FLEXCOMM0 clock |
| CLK\_FC1\_DIS | rw | 1 | 1'b0 | Write 1 to disable FLEXCOMM1 clock |
| CLK\_FC2\_DIS | rw | 2 | 1'b0 | Write 1 to disable FLEXCOMM2 clock |
| CLK\_FC3\_DIS | rw | 3 | 1'b0 | Write 1 to disable FLEXCOMM3 clock |
| CLK\_TIM0\_DIS | rw | 4 | 1'b0 | Write 1 to disable CTIMER0 clock |
| CLK\_TIM1\_DIS | rw | 5 | 1'b0 | Write 1 to disable CTIMER1 clock |
| CLK\_TIM2\_DIS | rw | 6 | 1'b0 | Write 1 to disable CTIMER2 clock |
| CLK\_TIM3\_DIS | rw | 7 | 1'b0 | Write 1 to disable CTIMER3 clock |
| CLK\_SCT\_DIS | rw | 8 | 1'b0 | Write 1 to disable SCT clock |
| CLK\_WDT\_DIS | rw | 9 | 1'b0 | Write 1 to disable Watch Dog clock |
| CLK\_USB\_DIS | rw | 10 | 1'b0 | Write 1 to disable USB clock; |
| CLK\_GPIO\_DIS | rw | 11 | 1'b0 | Write 1 to disable GPIO clock |
| CLK\_BIV\_DIS | rw | 12 | 1'b0 | Write 1 to disable BIV APB clock include RTC BiV register. |
| CLK\_ADC\_DIS | rw | 13 | 1'b0 | Write 1 to disable ADC clock; |
| CLK\_DAC\_DIS | rw | 14 | 1'b0 | Write 1 to disable DAC clock; |
| CLK\_CS\_DIS | rw | 15 | 1'b0 | Write 1 to disable Cap sensor clock; |
| CLK\_FSP\_DIS | rw | 16 | 1'b0 | Write 1 to disable FSP clock; |
| CLK\_DMA\_DIS | rw | 17 | 1'b0 | Write 1 to disable DMA clock |
| Reserved | rw | 18 | 1'b0 | Reserved |
| CLK\_QDEC0\_DIS | rw | 19 | 1'b0 | Write 1 to disable QDEC0 clock; |
| CLK\_QDEC1\_DIS | rw | 20 | 1'b0 | Write 1 to disable QDEC1 clock; |
| CLK\_DP\_DIS | rw | 21 | 1'b0 | Write 1 to disable Data Path 16/8MHz clock; |
| CLK\_SPIFI\_DIS | rw | 22 | 1'b0 | Write 1 to disable SPIFI clock; |
| Reserved | rw | 24:23 | 2'b0 | Reserved |
| CLK\_CAL\_DIS | rw | 25 | 1'b0 | Write 1 to disable Calibration clock; |
| Reserved | rw | 26 | 1'b0 | Reserved |
| CLK\_BLE\_DIS | rw | 27 | 1'b0 | Write 1 to disable BLE clock |
| Reserved | rw | 29:28 | 2'b0 | Reserved |
| PCLK\_DIS | rw | 30 | 1'b0 | Write 1 to disable PCLK of some logic; |
| FCLK\_DIS | rw | 31 | 1'b0 | Write 1 to disable CPU FCLK; |

### SYSCON\_CLK\_EN

Offset Address: 0x4000000c

clock enable register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CLK\_FC0\_EN | rw | 0 | 1'b0 | Write 1 to enable FLEXCOMM0 clock |
| CLK\_FC1\_EN | rw | 1 | 1'b0 | Write 1 to enable FLEXCOMM1 clock |
| CLK\_FC2\_EN | rw | 2 | 1'b0 | Write 1 to enable FLEXCOMM2 clock |
| CLK\_FC3\_EN | rw | 3 | 1'b0 | Write 1 to enable FLEXCOMM3 clock |
| CLK\_TIM0\_EN | rw | 4 | 1'b0 | Write 1 to enable CTIMER0 clock |
| CLK\_TIM1\_EN | rw | 5 | 1'b0 | Write 1 to enable CTIMER1 clock |
| CLK\_TIM2\_EN | rw | 6 | 1'b0 | Write 1 to enable CTIMER2 clock |
| CLK\_TIM3\_EN | rw | 7 | 1'b0 | Write 1 to enable CTIMER3 clock |
| CLK\_SCT\_EN | rw | 8 | 1'b0 | Write 1 to enable SCT clock |
| CLK\_WDT\_EN | rw | 9 | 1'b0 | Write 1 to enable Watch Dog clock |
| CLK\_USB\_EN | rw | 10 | 1'b0 | Write 1 to enable USB clock; |
| CLK\_GPIO\_EN | rw | 11 | 1'b0 | Write 1 to enable GPIO clock |
| CLK\_BIV\_EN | rw | 12 | 1'b0 | Write 1 to enable BIV APB clock include RTC BiV register. |
| CLK\_ADC\_EN | rw | 13 | 1'b0 | Write 1 to enable ADC clock; |
| CLK\_DAC\_EN | rw | 14 | 1'b0 | Write 1 to enable DAC clock; |
| CLK\_CS\_EN | rw | 15 | 1'b0 | Write 1 to enable Cap sensor clock; |
| CLK\_FSP\_EN | rw | 16 | 1'b0 | Write 1 to enable FSP clock; |
| CLK\_DMA\_EN | rw | 17 | 1'b0 | Write 1 to enable DMA clock |
| Reserved | rw | 18 | 1'b0 | Reserved |
| CLK\_QDEC0\_EN | rw | 19 | 1'b0 | Write 1 to enable QDEC0 clock; |
| CLK\_QDEC1\_EN | rw | 20 | 1'b0 | Write 1 to enable QDEC1 clock; |
| CLK\_DP\_EN | rw | 21 | 1'b0 | Write 1 to enable Data Path 16/8MHz clock; |
| CLK\_SPIFI\_EN | rw | 22 | 1'b0 | Write 1 to enable SPIFI clock; |
| Reserved | rw | 24:23 | 2'b0 | Reserved |
| CLK\_CAL\_EN | rw | 25 | 1'b0 | Write 1 to enable Calibration clock; |
| Reserved | rw | 26 | 1'b0 | Reserved |
| CLK\_BLE\_EN | rw | 27 | 1'b0 | Write 1 to enable BLE clock |
| Reserved | rw | 31:28 | 4'b0 | Reserved |

### SYSCON\_CLK\_CTRL

Offset Address: 0x40000010

system clock source and divider register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| APB\_DIV | rw | 3:0 | 4'b0 | APB\_CLK = AHB\_CLK/(APB\_DIV+1) |
| AHB\_DIV | rw | 16:4 | 13'b0 | AHB\_CLK = SYS\_CLK / (AHB\_DIV+1);Note Before enable BLE clock (CLK\_BLE\_EN =1) It is mandatory to set AHB\_CLK = 32 or 16 or 8 MHz. |
| CLK\_BLE\_SEL | rw | 17 | 1'b0 | BLE frequency indicator |
| CLK\_WDT\_SEL | rw | 18 | 1'b0 | Select Watch Dog clock |
| CLK\_XTAL\_SEL | rw | 19 | 1'b0 | Crytal clock selection |
| CLK\_OSC32M\_DIV | rw | 20 | 1'b0 | digital OSC clock input selection |
| CLK\_32K\_SEL | rw | 21 | 1'b0 | 32K clock source selection |
| CLK\_XTAL\_OE | rw | 22 | 1'b0 | system clock output enable |
| CLK\_32K\_OE | rw | 23 | 1'b0 | 32K clock output enable |
| XTAL\_OUT\_DIV | rw | 27:24 | 4'b0 | high frequency xtal clock output divider |
| CGBYPASS | rw | 28 | 1'b0 | If it is 0, it can save CPU power in active mode |
| Reserved | rw | 29 | 1'b0 | Reserved |
| SYS\_CLK\_SEL | rw | 31:30 | 2'b0 | Select SYS\_CLK source |

### SYSCON\_SYS\_MODE\_CTRL

Offset Address: 0x40000014

system mode and address remap register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| REMAP | rw | 1:0 | 2'b0 | software remap system address |
| LOCKUP\_EN | rw | 2 | 1'b0 | lock up enable |
| Reserved | rw | 24:3 | 22'b0 | Reserved |
| XTAL\_RDY | rw | 25 | 1'b0 | 16/32 MHz xtal ready readout |
| XTAL32K\_RDY | rw | 26 | 1'b0 | 32KHz xtal ready readout |
| PLL48M\_RDY | rw | 27 | 1'b0 | 48MHz PLL ready readout |
| OSC32M\_RDY | rw | 28 | 1'b0 | 32MHz oscillator ready readout |
| BG\_RDY | rw | 29 | 1'b0 | BG ready readout |
| Reserved | rw | 30 | 1'b0 | Reserved |
| BOOT\_MODE | rw | 31 | 1'b0 | boot mode pin status |

### SYSCON\_SYS\_STAT

Offset Address: 0x40000080

system status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FREQ\_WORD | rw | 7:0 | 8'b0 | BLE Frequency word; |
| BLE\_FREQ\_HOP | rw | 8 | 1'b0 | BLE frequency word change flag; |
| EVENT\_IN\_PROCESS | rw | 9 | 1'b0 | BLE event indicator |
| RX\_EN | rw | 10 | 1'b0 | when 1, system is in RX state |
| TX\_EN | rw | 11 | 1'b0 | when 1, system is in TX state |
| OSC\_EN | rw | 12 | 1'b0 | BLE osc\_en output; |
| RADIO\_EN | rw | 13 | 1'b0 | BLE radio\_en output; |
| CLK\_STATUS | rw | 14 | 1'b0 | BLE status |
| Reserved | rw | 31:15 | 17'b0 | Reserved |

### SYSCON\_SYS\_TICK

Offset Address: 0x40000100

systick timer control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TENMS | rw | 23:0 | 24'b0 | system tick timer calibration value |
| SKEW | rw | 24 | 1'b0 | whether THE TENMS value will generate a precise 10 millisencod time or an approximation |
| NOREF | rw | 25 | 1'b0 | whether an external reference clock is available |
| Reserved | rw | 30:26 | 5'b0 | Reserved |
| EN\_STCLKEN | rw | 31 | 1'b0 | 1 is enable STCLKEN; |

### SYSCON\_SRAM\_CTRL

Offset Address: 0x40000104

Exchange memory base address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| EM\_BASE\_ADDR | rw | 14:0 | 15'b0 | Exchange memory base address in system memory. Default value is 9K word. |
| Reserved | rw | 31:15 | 17'b0 | Reserved |

### SYSCON\_CHIP\_ID

Offset Address: 0x40000108

chip id register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CID0 | rw | 2:0 | 3'b0 | CHIP ID for manufacture fab |
| CID1 | rw | 5:3 | 3'b0 | CHIP ID for product family |
| CID2 | rw | 7:6 | 2'b0 | CHIP ID for minor revision |
| CID3 | rw | 13:8 | 6'b0 | CHIP ID for product ID |
| CID4 | rw | 15:14 | 2'b0 | CHIP ID for major revision |
| Reserved | rw | 25:16 | 10'b0 | Reserved |
| MEM\_OPTION | rw | 26 | 1'b0 | memory bond indicator |
| ADC\_OPTION | rw | 27 | 1'b0 | adc bond indicator |
| FLASH\_OPTION | rw | 28 | 1'b0 | flash bond indicator |
| FPU\_OPTION | rw | 29 | 1'b0 | fpu bond indicator |
| USB\_OPTION | rw | 30 | 1'b0 | usb bond indicator |
| FSP\_OPTION | rw | 31 | 1'b0 | fsp bond indicator |

### SYSCON\_ANA\_CTRL0

Offset Address: 0x40000110

crystal and PA register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PA\_POWER | rw | 7:0 | 8'b0 | PA power control (all of below is minus data) |
| Reserved | rw | 19:8 | 12'b0 | Reserved |
| XTAL\_AMP | rw | 21:20 | 2'b0 | crystal amplitude set register |
| XTAL\_LOAD\_CAP | rw | 27:22 | 6'b0 | Register controlled load cap of the XTAL in normal modeLOAD\_CAP=5pF+0.35pF\*CSEL+5pF\*XADD\_C |
| XTAL\_EXTRA\_CAP | rw | 28 | 1'b0 | Add extra 16/32 MHz xtal load cap |
| Reserved | rw | 29 | 1'b0 | Reserved |
| XTAL\_MODE | rw | 31:30 | 2'b0 | Injection mode of the XTAL |

### SYSCON\_XTAL\_CTRL

Offset Address: 0x40000180

crystal control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 4:0 | 5'b0 | Reserved |
| XTAL\_XCUR\_BOOST\_REG | rw | 5 | 1'b0 | 1 to increase 16/32 MHz xtal current |
| XTAL\_BPXDLY | rw | 6 | 1'b0 | Bypass the power up delay in the XTAL core. |
| XTAL\_BP\_HYSRES\_REG | rw | 7 | 1'b0 | 1 to bypass the degeneration resistor in order to reduce the hysteresis voltage |
| XTAL\_XSMT\_EN\_REG | rw | 8 | 1'b0 | 1 to use hysteresis buffer |
| XTAL\_XRDY\_REG | rw | 9 | 1'b0 | 1 to set xtal ready signal by register |
| XTAL\_XOUT\_DIS\_REG | rw | 10 | 1'b0 | 1 not to send 16/32 MHz xtal clk out |
| DIV\_DIFF\_CLK\_DIG\_DIS | rw | 11 | 1'b0 | disable differential clock of digital |
| Reserved | rw | 15:12 | 4'b0 | Reserved |
| XTAL\_SU\_CB\_REG | rw | 21:16 | 6'b0 | Register controlled load cap of the XTAL\_B in speed up modeCB=2pF+0.35pF\*SU\_CB+5pF\*XADD\_C |
| Reserved | rw | 23:22 | 2'b0 | Reserved |
| XTAL\_SU\_CA\_REG | rw | 29:24 | 6'b0 | Register controlled load cap of the XTAL\_A in speed up modeCA=2pF+0.35pF\*SU\_CA+5pF\*XADD\_C |
| XTAL\_INV | rw | 30 | 1'b0 | Inverse crystal clock |
| XTAL\_DIV | rw | 31 | 1'b0 | Divide crystal clock when external crystal is 32M this bit should be configured into 1 otherwise 0. |

### SYSCON\_BUCK

Offset Address: 0x40000184

buck control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| BUCK\_DRIVER\_PART\_EN | rw | 0 | 1'b0 | 1 to short external inductor |
| BUCK\_IND\_USE\_EN | rw | 1 | 1'b0 | 1 to turn on buck output stage gradually |
| Reserved | rw | 7:2 | 6'b0 | Reserved |
| BUCK\_ISEL | rw | 9:8 | 2'b0 | buck current bias control |
| BUCK\_VREF\_SEL | rw | 11:10 | 2'b0 | buck current setting |
| BUCK\_VBG\_SEL | rw | 13:12 | 2'b0 | buck reference setting |
| Reserved | rw | 15:14 | 2'b0 | Reserved |
| BUCK\_TMOS | rw | 20:16 | 5'b0 | buck constant on time control |
| BUCK\_IC | rw | 21 | 1'b0 | frequency compensation versus BVDD variation |
| Reserved | rw | 31:22 | 10'b0 | Reserved |

### SYSCON\_FC\_FRG

Offset Address: 0x40000200

flexcomm 0 and 1 clock divider register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FRG\_DIV0 | rw | 7:0 | 8'b0 | flexcomm0 clock generator, Denominator of the fractional divider. DIV is equal to the programmed value +1. Always set to 0xFF to use with the fractional baud rate generator. |
| FRG\_MULT0 | rw | 15:8 | 8'b0 | flexcomm0 clock generator, Numerator of the fractional divider. MULT is equal to the programmed value |
| FRG\_DIV1 | rw | 23:16 | 8'b0 | flexcomm1 clock generator, Denominator of the fractional divider. DIV is equal to the programmed value +1. Always set to 0xFF to use with the fractional baud rate generator. |
| FRG\_MULT1 | rw | 31:24 | 8'b0 | flexcomm1 clock generator, Numerator of the fractional divider. MULT is equal to the programmed value |

### SYSCON\_PIO\_PULL\_CFG0

Offset Address: 0x40000800

pad pull control register 0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PA00\_PULL | rw | 1:0 | 2'b0 | PA00 pull control register |
| PA01\_PULL | rw | 3:2 | 2'b0 | PA01 pull control register |
| PA02\_PULL | rw | 5:4 | 2'b0 | PA02 pull control register |
| PA03\_PULL | rw | 7:6 | 2'b0 | PA03 pull control register |
| PA04\_PULL | rw | 9:8 | 2'b0 | PA04 pull control register |
| PA05\_PULL | rw | 11:10 | 2'b0 | PA05 pull control register |
| PA06\_PULL | rw | 13:12 | 2'b0 | PA06 pull control register |
| PA07\_PULL | rw | 15:14 | 2'b0 | PA07 pull control register |
| PA08\_PULL | rw | 17:16 | 2'b0 | PA08 pull control register |
| PA09\_PULL | rw | 19:18 | 2'b0 | PA09 pull control register |
| PA10\_PULL | rw | 21:20 | 2'b0 | PA10 pull control register |
| PA11\_PULL | rw | 23:22 | 2'b0 | PA11 pull control register |
| PA12\_PULL | rw | 25:24 | 2'b0 | PA12 pull control register |
| PA13\_PULL | rw | 27:26 | 2'b0 | PA13 pull control register |
| PA14\_PULL | rw | 29:28 | 2'b0 | PA14 pull control register |
| PA15\_PULL | rw | 31:30 | 2'b0 | PA15 pull control register |

### SYSCON\_PIO\_PULL\_CFG1

Offset Address: 0x40000804

pad pull control register 1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PA16\_PULL | rw | 1:0 | 2'b0 | PA16 pull control register |
| PA17\_PULL | rw | 3:2 | 2'b0 | PA17 pull control register |
| PA18\_PULL | rw | 5:4 | 2'b0 | PA18 pull control register |
| PA19\_PULL | rw | 7:6 | 2'b0 | PA19 pull control register |
| PA20\_PULL | rw | 9:8 | 2'b0 | PA20 pull control register |
| PA21\_PULL | rw | 11:10 | 2'b0 | PA21 pull control register |
| PA22\_PULL | rw | 13:12 | 2'b0 | PA22 pull control register |
| PA23\_PULL | rw | 15:14 | 2'b0 | PA23 pull control register |
| PA24\_PULL | rw | 17:16 | 2'b0 | PA24 pull control register |
| PA25\_PULL | rw | 19:18 | 2'b0 | PA25 pull control register |
| PA26\_PULL | rw | 21:20 | 2'b0 | PA26 pull control register |
| PA27\_PULL | rw | 23:22 | 2'b0 | PA27 pull control register |
| PA28\_PULL | rw | 25:24 | 2'b0 | PA28 pull control register |
| PA29\_PULL | rw | 27:26 | 2'b0 | PA29 pull control register |
| PA30\_PULL | rw | 29:28 | 2'b0 | PA30 pull control register |
| PA31\_PULL | rw | 31:30 | 2'b0 | PA31 pull control register |

### SYSCON\_PIO\_PULL\_CFG2

Offset Address: 0x40000808

pad pull control register 2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PB00\_PULL | rw | 1:0 | 2'b0 | PB00 pull control register |
| PB01\_PULL | rw | 3:2 | 2'b0 | PB01 pull control register |
| PB02\_PULL | rw | 5:4 | 2'b0 | PB02 pull control register |
| Reserved | rw | 31:6 | 26'b0 | Reserved |

### SYSCON\_IO\_CAP

Offset Address: 0x4000080c

io status capture register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PIN\_RETENTION | rw | 0 | 1'b0 | Write 1 to capture pad output and output enable and the status will be saved in PIN\_SLP\_OEN0 PIN\_SLP\_OEN1 PIN\_SLP\_OUT0 and PIN\_SLP\_OUT1. |
| Reserved | rw | 31:1 | 31'b0 | Reserved |

### SYSCON\_PIO\_DRV\_CFG0

Offset Address: 0x40000810

pad drive strength register 0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PA00\_DRV | rw | 0 | 1'b0 | PA00 drive strength register |
| PA01\_DRV | rw | 1 | 1'b0 | PA01 drive strength register |
| PA02\_DRV | rw | 2 | 1'b0 | PA02 drive strength register |
| PA03\_DRV | rw | 3 | 1'b0 | PA03 drive strength register |
| PA04\_DRV | rw | 4 | 1'b0 | PA04 drive strength register |
| PA05\_DRV | rw | 5 | 1'b0 | PA05 drive strength register |
| PA06\_DRV | rw | 6 | 1'b0 | PA06 drive strength register |
| PA07\_DRV | rw | 7 | 1'b0 | PA07 drive strength register |
| PA08\_DRV | rw | 8 | 1'b0 | PA08 drive strength register |
| PA09\_DRV | rw | 9 | 1'b0 | PA09 drive strength register |
| PA10\_DRV | rw | 10 | 1'b0 | PA10 drive strength register |
| PA11\_DRV | rw | 11 | 1'b0 | PA11 drive strength register |
| PA12\_DRV | rw | 12 | 1'b0 | PA12 drive strength register |
| PA13\_DRV | rw | 13 | 1'b0 | PA13 drive strength register |
| PA14\_DRV | rw | 14 | 1'b0 | PA14 drive strength register |
| PA15\_DRV | rw | 15 | 1'b0 | PA15 drive strength register |
| PA16\_DRV | rw | 16 | 1'b0 | PA16 drive strength register |
| PA17\_DRV | rw | 17 | 1'b0 | PA17 drive strength register |
| PA18\_DRV | rw | 18 | 1'b0 | PA18 drive strength register |
| PA19\_DRV | rw | 19 | 1'b0 | PA19 drive strength register |
| PA20\_DRV | rw | 20 | 1'b0 | PA20 drive strength register |
| PA21\_DRV | rw | 21 | 1'b0 | PA21 drive strength register |
| PA22\_DRV | rw | 22 | 1'b0 | PA22 drive strength register |
| PA23\_DRV | rw | 23 | 1'b0 | PA23 drive strength register |
| PA24\_DRV | rw | 24 | 1'b0 | PA24 drive strength register |
| PA25\_DRV | rw | 25 | 1'b0 | PA25 drive strength register |
| PA26\_DRV | rw | 26 | 1'b0 | PA26 drive strength register |
| PA27\_DRV | rw | 27 | 1'b0 | PA27 drive strength register |
| PA28\_DRV | rw | 28 | 1'b0 | PA28 drive strength register |
| PA29\_DRV | rw | 29 | 1'b0 | PA29 drive strength register |
| PA30\_DRV | rw | 30 | 1'b0 | PA30 drive strength register |
| PA31\_DRV | rw | 31 | 1'b0 | PA31 drive strength register |

### SYSCON\_PIO\_DRV\_CFG1

Offset Address: 0x40000814

pad drive strength register 1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PB00\_DRV | rw | 0 | 1'b0 | PB00 drive strengh register |
| PB01\_DRV | rw | 1 | 1'b0 | PB01 drive strengh register |
| PB02\_DRV | rw | 2 | 1'b0 | PB02 drive strengh register |
| Reserved | rw | 31:3 | 29'b0 | Reserved |

### SYSCON\_PIO\_DRV\_CFG2

Offset Address: 0x40000818

pad drive extra register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 5:0 | 6'b0 | Reserved |
| PA06\_DRV\_EXTRA | rw | 6 | 1'b0 | Write 1 to enable extra driven on PA06 |
| Reserved | rw | 10:7 | 4'b0 | Reserved |
| PA11\_DRV\_EXTRA | rw | 11 | 1'b0 | Write 1 to enable extra driven on PA11 |
| Reserved | rw | 18:12 | 7'b0 | Reserved |
| PA19\_DRV\_EXTRA | rw | 19 | 1'b0 | Write 1 to enable extra driven on PA19 |
| Reserved | rw | 25:20 | 6'b0 | Reserved |
| PA26\_DRV\_EXTRA | rw | 26 | 1'b0 | Write 1 to enable extra driven on PA26 |
| PA27\_DRV\_EXTRA | rw | 27 | 1'b0 | Write 1 to enable extra driven on PA27 |
| Reserved | rw | 31:28 | 4'b0 | Reserved |

### SYSCON\_PIO\_CFG\_MISC

Offset Address: 0x4000081c

pin misc control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PB00\_AE | rw | 0 | 1'b0 | Enable PB00 analog function |
| PB01\_AE | rw | 1 | 1'b0 | Enable PB01 analog function |
| Reserved | rw | 14:2 | 13'b0 | Reserved |
| PSYNC | rw | 15 | 1'b0 | when 1, bypass first stage of synchronization of DMA pin trigger |
| PB02\_MODE | rw | 16 | 1'b0 | chip mode pin function select |
| Reserved | rw | 17 | 1'b0 | Reserved |
| TRX\_EN\_INV | rw | 18 | 1'b0 | inverse TX\_EN &amp; RX\_EN pin mux output polarity |
| RFE\_INV | rw | 19 | 1'b0 | Inverse RFE polarity |
| Reserved | rw | 31:20 | 12'b0 | Reserved |

### SYSCON\_PIO\_WAKEUP\_LVL0

Offset Address: 0x40000820

pin wakeup polarity register 0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PA00\_WAKEUP\_LVL | rw | 0 | 1'b0 | Control the wake up polarity of PA00 in sleep mode. 0: high level wakeup, 1: low level wakeup |
| PA01\_WAKEUP\_LVL | rw | 1 | 1'b0 | Control the wake up polarity of PA01 in sleep mode. |
| PA02\_WAKEUP\_LVL | rw | 2 | 1'b0 | Control the wake up polarity of PA02 in sleep mode. |
| PA03\_WAKEUP\_LVL | rw | 3 | 1'b0 | Control the wake up polarity of PA03 in sleep mode. |
| PA04\_WAKEUP\_LVL | rw | 4 | 1'b0 | Control the wake up polarity of PA04 in sleep mode. |
| PA05\_WAKEUP\_LVL | rw | 5 | 1'b0 | Control the wake up polarity of PA05 in sleep mode. |
| PA06\_WAKEUP\_LVL | rw | 6 | 1'b0 | Control the wake up polarity of PA06 in sleep mode. |
| PA07\_WAKEUP\_LVL | rw | 7 | 1'b0 | Control the wake up polarity of PA07 in sleep mode. |
| PA08\_WAKEUP\_LVL | rw | 8 | 1'b0 | Control the wake up polarity of PA08 in sleep mode. |
| PA09\_WAKEUP\_LVL | rw | 9 | 1'b0 | Control the wake up polarity of PA09 in sleep mode. |
| PA10\_WAKEUP\_LVL | rw | 10 | 1'b0 | Control the wake up polarity of PA10 in sleep mode. |
| PA11\_WAKEUP\_LVL | rw | 11 | 1'b0 | Control the wake up polarity of PA11 in sleep mode. |
| PA12\_WAKEUP\_LVL | rw | 12 | 1'b0 | Control the wake up polarity of PA12 in sleep mode. |
| PA13\_WAKEUP\_LVL | rw | 13 | 1'b0 | Control the wake up polarity of PA13 in sleep mode. |
| PA14\_WAKEUP\_LVL | rw | 14 | 1'b0 | Control the wake up polarity of PA14 in sleep mode. |
| PA15\_WAKEUP\_LVL | rw | 15 | 1'b0 | Control the wake up polarity of PA15 in sleep mode. |
| PA16\_WAKEUP\_LVL | rw | 16 | 1'b0 | Control the wake up polarity of PA16 in sleep mode. |
| PA17\_WAKEUP\_LVL | rw | 17 | 1'b0 | Control the wake up polarity of PA17 in sleep mode. |
| PA18\_WAKEUP\_LVL | rw | 18 | 1'b0 | Control the wake up polarity of PA18 in sleep mode. |
| PA19\_WAKEUP\_LVL | rw | 19 | 1'b0 | Control the wake up polarity of PA19 in sleep mode. |
| PA20\_WAKEUP\_LVL | rw | 20 | 1'b0 | Control the wake up polarity of PA20 in sleep mode. |
| PA21\_WAKEUP\_LVL | rw | 21 | 1'b0 | Control the wake up polarity of PA21 in sleep mode. |
| PA22\_WAKEUP\_LVL | rw | 22 | 1'b0 | Control the wake up polarity of PA22 in sleep mode. |
| PA23\_WAKEUP\_LVL | rw | 23 | 1'b0 | Control the wake up polarity of PA23 in sleep mode. |
| PA24\_WAKEUP\_LVL | rw | 24 | 1'b0 | Control the wake up polarity of PA24 in sleep mode. |
| PA25\_WAKEUP\_LVL | rw | 25 | 1'b0 | Control the wake up polarity of PA25 in sleep mode. |
| PA26\_WAKEUP\_LVL | rw | 26 | 1'b0 | Control the wake up polarity of PA26 in sleep mode. |
| PA27\_WAKEUP\_LVL | rw | 27 | 1'b0 | Control the wake up polarity of PA27 in sleep mode. |
| PA28\_WAKEUP\_LVL | rw | 28 | 1'b0 | Control the wake up polarity of PA28 in sleep mode. |
| PA29\_WAKEUP\_LVL | rw | 29 | 1'b0 | Control the wake up polarity of PA29 in sleep mode. |
| PA30\_WAKEUP\_LVL | rw | 30 | 1'b0 | Control the wake up polarity of PA30 in sleep mode. |
| PA31\_WAKEUP\_LVL | rw | 31 | 1'b0 | Control the wake up polarity of PA31 in sleep mode. |

### SYSCON\_PIO\_WAKEUP\_LVL1

Offset Address: 0x40000824

pin wakeup polarity register 1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PB00\_WAKEUP\_LVL | rw | 0 | 1'b0 | Control the wake up polarity of PB01 in sleep mode. |
| PB01\_WAKEUP\_LVL | rw | 1 | 1'b0 | Control the wake up polarity of PB02 in sleep mode. |
| PB02\_WAKEUP\_LVL | rw | 2 | 1'b0 | Control the wake up polarity of PB03 in sleep mode. |
| Reserved | rw | 31:3 | 29'b0 | Reserved |

### SYSCON\_PIO\_IE\_CFG0

Offset Address: 0x40000828

pad input enable register 0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PA00\_IE | rw | 0 | 1'b0 | PA00 digital input enable |
| PA01\_IE | rw | 1 | 1'b0 | PA01 digital input enable |
| PA02\_IE | rw | 2 | 1'b0 | PA02 digital input enable |
| PA03\_IE | rw | 3 | 1'b0 | PA03 digital input enable |
| PA04\_IE | rw | 4 | 1'b0 | PA04 digital input enable |
| PA05\_IE | rw | 5 | 1'b0 | PA05 digital input enable |
| PA06\_IE | rw | 6 | 1'b0 | PA06 digital input enable |
| PA07\_IE | rw | 7 | 1'b0 | PA07 digital input enable |
| PA08\_IE | rw | 8 | 1'b0 | PA08 digital input enable |
| PA09\_IE | rw | 9 | 1'b0 | PA09 digital input enable |
| PA10\_IE | rw | 10 | 1'b0 | PA10 digital input enable |
| PA11\_IE | rw | 11 | 1'b0 | PA11 digital input enable |
| PA12\_IE | rw | 12 | 1'b0 | PA12 digital input enable |
| PA13\_IE | rw | 13 | 1'b0 | PA13 digital input enable |
| PA14\_IE | rw | 14 | 1'b0 | PA14 digital input enable |
| PA15\_IE | rw | 15 | 1'b0 | PA15 digital input enable |
| PA16\_IE | rw | 16 | 1'b0 | PA16 digital input enable |
| PA17\_IE | rw | 17 | 1'b0 | PA17 digital input enable |
| PA18\_IE | rw | 18 | 1'b0 | PA18 digital input enable |
| PA19\_IE | rw | 19 | 1'b0 | PA19 digital input enable |
| PA20\_IE | rw | 20 | 1'b0 | PA20 digital input enable |
| PA21\_IE | rw | 21 | 1'b0 | PA21 digital input enable |
| PA22\_IE | rw | 22 | 1'b0 | PA22 digital input enable |
| PA23\_IE | rw | 23 | 1'b0 | PA23 digital input enable |
| PA24\_IE | rw | 24 | 1'b0 | PA24 digital input enable |
| PA25\_IE | rw | 25 | 1'b0 | PA25 digital input enable |
| PA26\_IE | rw | 26 | 1'b0 | PA26 digital input enable |
| PA27\_IE | rw | 27 | 1'b0 | PA27 digital input enable |
| PA28\_IE | rw | 28 | 1'b0 | PA28 digital input enable |
| PA29\_IE | rw | 29 | 1'b0 | PA29 digital input enable |
| PA30\_IE | rw | 30 | 1'b0 | PA30 digital input enable |
| PA31\_IE | rw | 31 | 1'b0 | PA31 digital input enable |

### SYSCON\_PIO\_IE\_CFG1

Offset Address: 0x4000082c

pad input enable register 1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PB00\_IE | rw | 0 | 1'b0 | PB00 digital input enable |
| PB01\_IE | rw | 1 | 1'b0 | PB01 digital input enable |
| BOOT\_MODE\_IE | rw | 2 | 1'b0 | PB02 input enable |
| Reserved | rw | 31:3 | 29'b0 | Reserved |

### SYSCON\_PIO\_FUNC\_CFG0

Offset Address: 0x40000830

pin mux control register 0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PA00\_FUNC | rw | 2:0 | 3'b0 | PA00 function control register |
| Reserved | rw | 3 | 1'b0 | Reserved |
| PA01\_FUNC | rw | 6:4 | 3'b0 | PA01 function control register |
| Reserved | rw | 7 | 1'b0 | Reserved |
| PA02\_FUNC | rw | 10:8 | 3'b0 | PA02 function control register |
| Reserved | rw | 11 | 1'b0 | Reserved |
| PA03\_FUNC | rw | 14:12 | 3'b0 | PA03 function control register |
| Reserved | rw | 15 | 1'b0 | Reserved |
| PA04\_FUNC | rw | 18:16 | 3'b0 | PA04 function control register |
| Reserved | rw | 19 | 1'b0 | Reserved |
| PA05\_FUNC | rw | 22:20 | 3'b0 | PA05 function control register |
| Reserved | rw | 23 | 1'b0 | Reserved |
| PA06\_FUNC | rw | 26:24 | 3'b0 | PA06 function control register |
| Reserved | rw | 27 | 1'b0 | Reserved |
| PA07\_FUNC | rw | 30:28 | 3'b0 | PA07 function control register |
| Reserved | rw | 31 | 1'b0 | Reserved |

### SYSCON\_PIO\_FUNC\_CFG1

Offset Address: 0x40000834

pin mux control register 1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PA08\_FUNC | rw | 2:0 | 3'b0 | PA08 function control register |
| Reserved | rw | 3 | 1'b0 | Reserved |
| PA09\_FUNC | rw | 6:4 | 3'b0 | PA09 function control register |
| Reserved | rw | 7 | 1'b0 | Reserved |
| PA10\_FUNC | rw | 10:8 | 3'b0 | PA10 function control register |
| Reserved | rw | 11 | 1'b0 | Reserved |
| PA11\_FUNC | rw | 14:12 | 3'b0 | PA11 function control register |
| Reserved | rw | 15 | 1'b0 | Reserved |
| PA12\_FUNC | rw | 18:16 | 3'b0 | PA12 function control register |
| Reserved | rw | 19 | 1'b0 | Reserved |
| PA13\_FUNC | rw | 22:20 | 3'b0 | PA13 function control register |
| Reserved | rw | 23 | 1'b0 | Reserved |
| PA14\_FUNC | rw | 26:24 | 3'b0 | PA14 function control register |
| Reserved | rw | 27 | 1'b0 | Reserved |
| PA15\_FUNC | rw | 30:28 | 3'b0 | PA15 function control register |
| Reserved | rw | 31 | 1'b0 | Reserved |

### SYSCON\_PIO\_FUNC\_CFG2

Offset Address: 0x40000838

pin mux control register 2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PA16\_FUNC | rw | 2:0 | 3'b0 | PA16 function control register |
| Reserved | rw | 3 | 1'b0 | Reserved |
| PA17\_FUNC | rw | 6:4 | 3'b0 | PA17 function control register |
| Reserved | rw | 7 | 1'b0 | Reserved |
| PA18\_FUNC | rw | 10:8 | 3'b0 | PA18 function control register |
| Reserved | rw | 11 | 1'b0 | Reserved |
| PA19\_FUNC | rw | 14:12 | 3'b0 | PA19 function control register |
| Reserved | rw | 15 | 1'b0 | Reserved |
| PA20\_FUNC | rw | 18:16 | 3'b0 | PA20 function control register |
| Reserved | rw | 19 | 1'b0 | Reserved |
| PA21\_FUNC | rw | 22:20 | 3'b0 | PA21 function control register |
| Reserved | rw | 23 | 1'b0 | Reserved |
| PA22\_FUNC | rw | 26:24 | 3'b0 | PA22 function control register |
| Reserved | rw | 27 | 1'b0 | Reserved |
| PA23\_FUNC | rw | 30:28 | 3'b0 | PA23 function control register |
| Reserved | rw | 31 | 1'b0 | Reserved |

### SYSCON\_PIO\_FUNC\_CFG3

Offset Address: 0x4000083c

pin mux control register 3

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PA24\_FUNC | rw | 2:0 | 3'b0 | PA24 function control register |
| Reserved | rw | 3 | 1'b0 | Reserved |
| PA25\_FUNC | rw | 6:4 | 3'b0 | PA25 function control register |
| Reserved | rw | 7 | 1'b0 | Reserved |
| PA26\_FUNC | rw | 10:8 | 3'b0 | PA26 function control register |
| Reserved | rw | 11 | 1'b0 | Reserved |
| PA27\_FUNC | rw | 14:12 | 3'b0 | PA27 function control register |
| Reserved | rw | 15 | 1'b0 | Reserved |
| PA28\_FUNC | rw | 18:16 | 3'b0 | PA28 function control register |
| Reserved | rw | 19 | 1'b0 | Reserved |
| PA29\_FUNC | rw | 22:20 | 3'b0 | PA29 function control register |
| Reserved | rw | 23 | 1'b0 | Reserved |
| PA30\_FUNC | rw | 26:24 | 3'b0 | PA30 function control register |
| Reserved | rw | 27 | 1'b0 | Reserved |
| PA31\_FUNC | rw | 30:28 | 3'b0 | PA31 function control register |
| Reserved | rw | 31 | 1'b0 | Reserved |

### SYSCON\_PIO\_WAKEUP\_EN0

Offset Address: 0x40000840

pin function selection in power down mode register 0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PA00\_WAKEUP\_EN | rw | 0 | 1'b0 | Control GPIOA[31-0] as Wakeup source. |
| PA01\_WAKEUP\_EN | rw | 1 | 1'b0 | no description available |
| PA02\_WAKEUP\_EN | rw | 2 | 1'b0 | no description available |
| PA03\_WAKEUP\_EN | rw | 3 | 1'b0 | no description available |
| PA04\_WAKEUP\_EN | rw | 4 | 1'b0 | no description available |
| PA05\_WAKEUP\_EN | rw | 5 | 1'b0 | no description available |
| PA06\_WAKEUP\_EN | rw | 6 | 1'b0 | no description available |
| PA07\_WAKEUP\_EN | rw | 7 | 1'b0 | no description available |
| PA08\_WAKEUP\_EN | rw | 8 | 1'b0 | no description available |
| PA09\_WAKEUP\_EN | rw | 9 | 1'b0 | no description available |
| PA10\_WAKEUP\_EN | rw | 10 | 1'b0 | no description available |
| PA11\_WAKEUP\_EN | rw | 11 | 1'b0 | no description available |
| PA12\_WAKEUP\_EN | rw | 12 | 1'b0 | no description available |
| PA13\_WAKEUP\_EN | rw | 13 | 1'b0 | no description available |
| PA14\_WAKEUP\_EN | rw | 14 | 1'b0 | no description available |
| PA15\_WAKEUP\_EN | rw | 15 | 1'b0 | no description available |
| PA16\_WAKEUP\_EN | rw | 16 | 1'b0 | no description available |
| PA17\_WAKEUP\_EN | rw | 17 | 1'b0 | no description available |
| PA18\_WAKEUP\_EN | rw | 18 | 1'b0 | no description available |
| PA19\_WAKEUP\_EN | rw | 19 | 1'b0 | no description available |
| PA20\_WAKEUP\_EN | rw | 20 | 1'b0 | no description available |
| PA21\_WAKEUP\_EN | rw | 21 | 1'b0 | no description available |
| PA22\_WAKEUP\_EN | rw | 22 | 1'b0 | no description available |
| PA23\_WAKEUP\_EN | rw | 23 | 1'b0 | no description available |
| PA24\_WAKEUP\_EN | rw | 24 | 1'b0 | no description available |
| PA25\_WAKEUP\_EN | rw | 25 | 1'b0 | no description available |
| PA26\_WAKEUP\_EN | rw | 26 | 1'b0 | no description available |
| PA27\_WAKEUP\_EN | rw | 27 | 1'b0 | no description available |
| PA28\_WAKEUP\_EN | rw | 28 | 1'b0 | no description available |
| PA29\_WAKEUP\_EN | rw | 29 | 1'b0 | no description available |
| PA30\_WAKEUP\_EN | rw | 30 | 1'b0 | no description available |
| PA31\_WAKEUP\_EN | rw | 31 | 1'b0 | no description available |

### SYSCON\_PIO\_WAKEUP\_EN1

Offset Address: 0x40000844

pin function selection in power down mode register 1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PB00\_WAKEUP\_EN | rw | 0 | 1'b0 | Control GPIOB as Wakeup source. |
| PB01\_WAKEUP\_EN | rw | 1 | 1'b0 | no description available |
| PB02\_WAKEUP\_EN | rw | 2 | 1'b0 | no description available |
| Reserved | rw | 3 | 1'b0 | Reserved |
| PA04\_32K\_OE | rw | 4 | 1'b0 | 32K clock output enable. When this bit is set to 1 PA04 will output 32k clock. At this time PIN\_CTRL register is not effective to control this IO's function. |
| PA05\_XTAL\_OE | rw | 5 | 1'b0 | XTAL clock output enable. When this bit is set to 1 PA05 will output XTAL clock. At this time PIN\_CTRL register is not effective to control this IO's function. |
| Reserved | rw | 9:6 | 4'b0 | Reserved |
| PA10\_32K\_OE | rw | 10 | 1'b0 | 32K clock output enable. When this bit is set to 1 PA10 (GPIO10) will output 32k clock. At this time PIN\_CTRL register is not effective to control this IO's function. |
| PA11\_XTAL\_OE | rw | 11 | 1'b0 | XTAL clock output enable. When this bit is set to 1 PA11 will output XTAL clock. At this time PIN\_CTRL register is not effective to control this IO's function. |
| Reserved | rw | 17:12 | 6'b0 | Reserved |
| PA18\_32K\_OE | rw | 18 | 1'b0 | 32K clock output enable. When this bit is set to 1 PA18 will output 32k clock. At this time PIN\_CTRL register is not effective to control this IO's function. |
| PA19\_XTAL\_OE | rw | 19 | 1'b0 | XTAL clock output enable. When this bit is set to 1 PA19 will output XTAL clock. At this time PIN\_CTRL register is not effective to control this IO's function. |
| Reserved | rw | 23:20 | 4'b0 | Reserved |
| PA24\_32K\_OE | rw | 24 | 1'b0 | 32K clock output enable. When this bit is set to 1 PA24 will output 32k clock. At this time PIN\_CTRL register is not effective to control this IO's function. |
| PA25\_XTAL\_OE | rw | 25 | 1'b0 | XTAL clock output enable. When this bit is set to 1 PA25 will output XTAL clock. At this time PIN\_CTRL register is not effective to control this IO's function. |
| Reserved | rw | 30:26 | 5'b0 | Reserved |
| PDM\_IO\_SEL | rw | 31 | 1'b0 | pin status selection in power down mode |

### SYSCON\_PIO\_CAP\_OE0

Offset Address: 0x40000848

pin output enable status register 0 while captured by writing 1 to IO\_CAP

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PA00\_CAP\_OE | rw | 0 | 1'b0 | PA00 output enable status captured by writing 1 to IO\_CAP |
| PA01\_CAP\_OE | rw | 1 | 1'b0 | PA01 output enable status captured by writing 1 to IO\_CAP |
| PA02\_CAP\_OE | rw | 2 | 1'b0 | PA02 output enable status captured by writing 1 to IO\_CAP |
| PA03\_CAP\_OE | rw | 3 | 1'b0 | PA03 output enable status captured by writing 1 to IO\_CAP |
| PA04\_CAP\_OE | rw | 4 | 1'b0 | PA04 output enable status captured by writing 1 to IO\_CAP |
| PA05\_CAP\_OE | rw | 5 | 1'b0 | PA05 output enable status captured by writing 1 to IO\_CAP |
| PA06\_CAP\_OE | rw | 6 | 1'b0 | PA06 output enable status captured by writing 1 to IO\_CAP |
| PA07\_CAP\_OE | rw | 7 | 1'b0 | PA07 output enable status captured by writing 1 to IO\_CAP |
| PA08\_CAP\_OE | rw | 8 | 1'b0 | PA08 output enable status captured by writing 1 to IO\_CAP |
| PA09\_CAP\_OE | rw | 9 | 1'b0 | PA09 output enable status captured by writing 1 to IO\_CAP |
| PA10\_CAP\_OE | rw | 10 | 1'b0 | PA10 output enable status captured by writing 1 to IO\_CAP |
| PA11\_CAP\_OE | rw | 11 | 1'b0 | PA11 output enable status captured by writing 1 to IO\_CAP |
| PA12\_CAP\_OE | rw | 12 | 1'b0 | PA12 output enable status captured by writing 1 to IO\_CAP |
| PA13\_CAP\_OE | rw | 13 | 1'b0 | PA13 output enable status captured by writing 1 to IO\_CAP |
| PA14\_CAP\_OE | rw | 14 | 1'b0 | PA14 output enable status captured by writing 1 to IO\_CAP |
| PA15\_CAP\_OE | rw | 15 | 1'b0 | PA15 output enable status captured by writing 1 to IO\_CAP |
| PA16\_CAP\_OE | rw | 16 | 1'b0 | PA16 output enable status captured by writing 1 to IO\_CAP |
| PA17\_CAP\_OE | rw | 17 | 1'b0 | PA17 output enable status captured by writing 1 to IO\_CAP |
| PA18\_CAP\_OE | rw | 18 | 1'b0 | PA18 output enable status captured by writing 1 to IO\_CAP |
| PA19\_CAP\_OE | rw | 19 | 1'b0 | PA19 output enable status captured by writing 1 to IO\_CAP |
| PA20\_CAP\_OE | rw | 20 | 1'b0 | PA20 output enable status captured by writing 1 to IO\_CAP |
| PA21\_CAP\_OE | rw | 21 | 1'b0 | PA21 output enable status captured by writing 1 to IO\_CAP |
| PA22\_CAP\_OE | rw | 22 | 1'b0 | PA22 output enable status captured by writing 1 to IO\_CAP |
| PA23\_CAP\_OE | rw | 23 | 1'b0 | PA23 output enable status captured by writing 1 to IO\_CAP |
| PA24\_CAP\_OE | rw | 24 | 1'b0 | PA24 output enable status captured by writing 1 to IO\_CAP |
| PA25\_CAP\_OE | rw | 25 | 1'b0 | PA25 output enable status captured by writing 1 to IO\_CAP |
| PA26\_CAP\_OE | rw | 26 | 1'b0 | PA26 output enable status captured by writing 1 to IO\_CAP |
| PA27\_CAP\_OE | rw | 27 | 1'b0 | PA27 output enable status captured by writing 1 to IO\_CAP |
| PA28\_CAP\_OE | rw | 28 | 1'b0 | PA28 output enable status captured by writing 1 to IO\_CAP |
| PA29\_CAP\_OE | rw | 29 | 1'b0 | PA29 output enable status captured by writing 1 to IO\_CAP |
| PA30\_CAP\_OE | rw | 30 | 1'b0 | PA30 output enable status captured by writing 1 to IO\_CAP |
| PA31\_CAP\_OE | rw | 31 | 1'b0 | PA31 output enable status captured by writing 1 to IO\_CAP |

### SYSCON\_PIO\_CAP\_OE1

Offset Address: 0x4000084c

pin output enable status register 1 while captured by writing 1 to IO\_CAP

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PB00\_CAP\_OE | rw | 0 | 1'b0 | PB00 output enable status captured by writing 1 to IO\_CAP |
| PB01\_CAP\_OE | rw | 1 | 1'b0 | PB01 output enable status captured by writing 1 to IO\_CAP |
| PB02\_CAP\_OE | rw | 2 | 1'b0 | PB02 output enable status captured by writing 1 to IO\_CAP |
| Reserved | rw | 31:3 | 29'b0 | Reserved |

### SYSCON\_PIO\_CAP\_OUT0

Offset Address: 0x40000850

pin output status register 0 while captured by writing 1 to IO\_CAP

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PA00\_CAP\_OUT | rw | 0 | 1'b0 | PA00 output status captured by writing 1 to IO\_CAP |
| PA01\_CAP\_OUT | rw | 1 | 1'b0 | PA01 output status captured by writing 1 to IO\_CAP |
| PA02\_CAP\_OUT | rw | 2 | 1'b0 | PA02 output status captured by writing 1 to IO\_CAP |
| PA03\_CAP\_OUT | rw | 3 | 1'b0 | PA03 output status captured by writing 1 to IO\_CAP |
| PA04\_CAP\_OUT | rw | 4 | 1'b0 | PA04 output status captured by writing 1 to IO\_CAP |
| PA05\_CAP\_OUT | rw | 5 | 1'b0 | PA05 output status captured by writing 1 to IO\_CAP |
| PA06\_CAP\_OUT | rw | 6 | 1'b0 | PA06 output status captured by writing 1 to IO\_CAP |
| PA07\_CAP\_OUT | rw | 7 | 1'b0 | PA07 output status captured by writing 1 to IO\_CAP |
| PA08\_CAP\_OUT | rw | 8 | 1'b0 | PA08 output status captured by writing 1 to IO\_CAP |
| PA09\_CAP\_OUT | rw | 9 | 1'b0 | PA09 output status captured by writing 1 to IO\_CAP |
| PA10\_CAP\_OUT | rw | 10 | 1'b0 | PA10 output status captured by writing 1 to IO\_CAP |
| PA11\_CAP\_OUT | rw | 11 | 1'b0 | PA11 output status captured by writing 1 to IO\_CAP |
| PA12\_CAP\_OUT | rw | 12 | 1'b0 | PA12 output status captured by writing 1 to IO\_CAP |
| PA13\_CAP\_OUT | rw | 13 | 1'b0 | PA13 output status captured by writing 1 to IO\_CAP |
| PA14\_CAP\_OUT | rw | 14 | 1'b0 | PA14 output status captured by writing 1 to IO\_CAP |
| PA15\_CAP\_OUT | rw | 15 | 1'b0 | PA15 output status captured by writing 1 to IO\_CAP |
| PA16\_CAP\_OUT | rw | 16 | 1'b0 | PA16 output status captured by writing 1 to IO\_CAP |
| PA17\_CAP\_OUT | rw | 17 | 1'b0 | PA17 output status captured by writing 1 to IO\_CAP |
| PA18\_CAP\_OUT | rw | 18 | 1'b0 | PA18 output status captured by writing 1 to IO\_CAP |
| PA19\_CAP\_OUT | rw | 19 | 1'b0 | PA19 output status captured by writing 1 to IO\_CAP |
| PA20\_CAP\_OUT | rw | 20 | 1'b0 | PA20 output status captured by writing 1 to IO\_CAP |
| PA21\_CAP\_OUT | rw | 21 | 1'b0 | PA21 output status captured by writing 1 to IO\_CAP |
| PA22\_CAP\_OUT | rw | 22 | 1'b0 | PA22 output status captured by writing 1 to IO\_CAP |
| PA23\_CAP\_OUT | rw | 23 | 1'b0 | PA23 output status captured by writing 1 to IO\_CAP |
| PA24\_CAP\_OUT | rw | 24 | 1'b0 | PA24 output status captured by writing 1 to IO\_CAP |
| PA25\_CAP\_OUT | rw | 25 | 1'b0 | PA25 output status captured by writing 1 to IO\_CAP |
| PA26\_CAP\_OUT | rw | 26 | 1'b0 | PA26 output status captured by writing 1 to IO\_CAP |
| PA27\_CAP\_OUT | rw | 27 | 1'b0 | PA27 output status captured by writing 1 to IO\_CAP |
| PA28\_CAP\_OUT | rw | 28 | 1'b0 | PA28 output status captured by writing 1 to IO\_CAP |
| PA29\_CAP\_OUT | rw | 29 | 1'b0 | PA29 output status captured by writing 1 to IO\_CAP |
| PA30\_CAP\_OUT | rw | 30 | 1'b0 | PA30 output status captured by writing 1 to IO\_CAP |
| PA31\_CAP\_OUT | rw | 31 | 1'b0 | PA31 output status captured by writing 1 to IO\_CAP |

### SYSCON\_PIO\_CAP\_OUT1

Offset Address: 0x40000854

pin output status register 0 while captured by writing 1 to IO\_CAP

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PB00\_CAP\_OUT | rw | 0 | 1'b0 | PB00 output status while captured by writing 1 to IO\_CAP |
| PB01\_CAP\_OUT | rw | 1 | 1'b0 | PB01 output status while captured by writing 1 to IO\_CAP |
| PB02\_CAP\_OUT | rw | 2 | 1'b0 | PB02 output status while captured by writing 1 to IO\_CAP |
| Reserved | rw | 31:3 | 29'b0 | Reserved |

### SYSCON\_RST\_CAUSE\_SRC

Offset Address: 0x40000858

reset source status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| RESET\_CAUSE | rw | 8:0 | 9'b0 | reset source indicator. xxxxxxxx1b = Power-on Reset; xxxxxxx1xb = Brown-Down Reset; xxxxxx1xxb = External pin Reset; xxxxx1xxxb = Watch Dog Reset; xxxx1xxxxb = Lock Up Reset; xxx1xxxxxb = Reboot Reset; xx1000000b = CPU system Reset requirement; x10000000b = Wake Up reset 10000000b = CPU software Reset; |
| Reserved | rw | 30:9 | 22'b0 | Reserved |
| RST\_CAUSE\_CLR | rw | 31 | 1'b0 | Write '1' clear RESET\_CAUSE bits; |

### SYSCON\_PMU\_CTRL0

Offset Address: 0x4000085c

power management uinit control register 0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MEM0\_DIS | rw | 0 | 1'b0 | power down sram memory block 0 |
| MEM1\_DIS | rw | 1 | 1'b0 | power down sram memory block 1 |
| MEM2\_DIS | rw | 2 | 1'b0 | power down sram memory block 2 |
| MEM3\_DIS | rw | 3 | 1'b0 | power down sram memory block 3 |
| MEM4\_DIS | rw | 4 | 1'b0 | power down sram memory block 4 |
| MEM5\_DIS | rw | 5 | 1'b0 | power down sram memory block 5 |
| MEM6\_DIS | rw | 6 | 1'b0 | power down sram memory block 6 |
| MEM7\_DIS | rw | 7 | 1'b0 | power down sram memory block 7 |
| MEM8\_DIS | rw | 8 | 1'b0 | power down sram memory block 8 |
| MEM9\_DIS | rw | 9 | 1'b0 | power down sram memory block 9 |
| Reserved | rw | 15:10 | 6'b0 | Reserved |
| BLE\_DIS | rw | 16 | 1'b0 | power down BLE |
| FIR\_DIS | rw | 17 | 1'b0 | power down FIR buffer |
| FSP\_DIS | rw | 18 | 1'b0 | power down FSP |
| Reserved | rw | 19 | 1'b0 | Reserved |
| MCU\_MODE | rw | 20 | 1'b0 | power control of BG, V2I, VREG\_A, VREG\_D |
| Reserved | rw | 25:21 | 5'b0 | Reserved |
| OSC\_INT\_EN | rw | 26 | 1'b0 | 1 to enable OSC\_EN as interrupt and wakeup source |
| RTC\_SEC\_WAKEUP\_EN | rw | 27 | 1'b0 | 1 to enable RTC interrupt as wakeup source |
| WAKEUP\_EN | rw | 28 | 1'b0 | 1 to enable sleep wake up source |
| PMU\_EN | rw | 29 | 1'b0 | 1 to enable chip power down mode |
| RETENTION\_EN | rw | 30 | 1'b0 | 1 to enable all CPU registers to be retentioned in sleep mode |
| BOND\_EN | rw | 31 | 1'b0 | 1 to enable FSP\_BOND\_EN bond option |

### SYSCON\_PMU\_CTRL1

Offset Address: 0x40000860

power management uinit control register 1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| RCO32K\_DIS | rw | 0 | 1'b0 | 1 to switch off 32K RCO power |
| XTAL32K\_DIS | rw | 1 | 1'b0 | 1 to switch off 32K XTAL power |
| XTAL\_DIS | rw | 2 | 1'b0 | 1 to switch off XTAL of digital power |
| OSC32M\_DIS | rw | 3 | 1'b0 | 1 to switch off 32M OSC power |
| USBPLL\_DIS | rw | 4 | 1'b0 | 1 to switch off USB 48M PLL power |
| ADC\_BUF\_DIS | rw | 5 | 1'b0 | 1 to switch off buffer in SD ADC |
| ADC\_BG\_DIS | rw | 6 | 1'b0 | 1 to switch off bandgap in SD ADC |
| ADC\_DIS | rw | 7 | 1'b0 | 1 to switch off SD ADC |
| ADC\_VCM\_DIS | rw | 8 | 1'b0 | 1 to switch off VCM DRV in SD ADC |
| ADC\_VREF\_DIS | rw | 9 | 1'b0 | 1 to switch off VREF DRV in SD ADC |
| DAC\_DIS | rw | 10 | 1'b0 | 1 to switch off DAC |
| CAP\_SEN\_DIS | rw | 11 | 1'b0 | 1 to switch off CAP\_SEN |
| Reserved | rw | 15:12 | 4'b0 | Reserved |
| BUCK\_CTRL | rw | 19:16 | 4'b0 | BUCK power control, 0x00 to power on, and 0x0F to power down |
| Reserved | rw | 29:20 | 10'b0 | Reserved |
| RCO32K\_PDM\_DIS | rw | 30 | 1'b0 | In sleep mode this bit ORs with DIS\_RCO\_32K to control the RCO 32K power |
| XTAL32K\_PDM\_DIS | rw | 31 | 1'b0 | In sleep mode this bit ORs with DIS\_XTAL32K to control the XTAL32 power |

### SYSCON\_ANA\_EN

Offset Address: 0x40000864

analog setting register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| BOD\_AMP\_EN | rw | 0 | 1'b0 | Enable the AMP of browned out detector |
| BOD\_EN | rw | 1 | 1'b0 | Enable browned out detector |
| BAT\_MON\_EN | rw | 2 | 1'b0 | Enable battery monitor |
| ACMP0\_EN | rw | 3 | 1'b0 | Enable comparator 0 |
| ACMP1\_EN | rw | 4 | 1'b0 | Enable comparator 1 |
| BOR\_AMP\_EN | rw | 5 | 1'b0 | Enable the AMP of browned reset detector |
| BOR\_EN | rw | 6 | 1'b0 | Enable browned reset detector |
| Reserved | rw | 7 | 1'b0 | Reserved |
| ACMP0\_REF | rw | 11:8 | 4'b0 | acmp0 reference voltage selection, vref0=Acmp\_vref\*ACMP0\_REF/16 |
| ACMP1\_REF | rw | 15:12 | 4'b0 | acmp1 reference voltage selection, vref1=Acmp\_vref\*ACMP1\_REF/16 |
| ACMP0\_HYST\_EN | rw | 16 | 1'b0 | Hysteresis enable of ACMP0 when 1 |
| ACMP1\_HYST\_EN | rw | 17 | 1'b0 | Hysteresis enable of ACMP1 when 1 |
| ACMP\_VREF\_SEL | rw | 18 | 1'b0 | Acmp\_vref selection |
| BOD\_THR | rw | 20:19 | 2'b0 | Browned-out detector threshold voltages, when VDD is lower than this voltage, BOD\_OUT interrupt happens. And the detector has a hysteresis. |
| BOR\_THR | rw | 22:21 | 2'b0 | Browned-out reset threshold voltages |
| Reserved | rw | 23 | 1'b0 | Reserved |
| ACMP0\_OUT | rw | 24 | 1'b0 | Comparator 0 output. |
| ACMP1\_OUT | rw | 25 | 1'b0 | Comparator 1 output. |
| ACMP0\_EDGE\_SEL | rw | 27:26 | 2'b0 | ACMP0 interrupt edge selection |
| ACMP1\_EDGE\_SEL | rw | 29:28 | 2'b0 | ACMP1 interrupt edge selection |
| ACMP0\_INTEN | rw | 30 | 1'b0 | 1 to enable ACMP0 interrupt |
| ACMP1\_INTEN | rw | 31 | 1'b0 | 1 to enable ACMP1 interrupt |

### SYSCON\_XTAL32K\_CTRL

Offset Address: 0x40000868

crystal 32K control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| XTAL32K\_ICTRL | rw | 5:0 | 6'b0 | Xtal 32 gm cell current bias Y |
| XTAL32K\_INJ | rw | 7:6 | 2'b0 | Xtal 32KHz clk injection mode1xb = external sine wave clock |
| XTAL32K\_LOAD\_CAP | rw | 13:8 | 6'b0 | load cap selection of xtal32 |
| XTAL32K\_EXTRA\_CAP | rw | 14 | 1'b0 | add extra xtal32 load cap |
| Reserved | rw | 31:15 | 17'b0 | Reserved |

### SYSCON\_USB\_CFG

Offset Address: 0x4000086c

USB configuration register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DPPUEN\_B\_PHY\_POL | rw | 0 | 1'b0 | drive high to inverse the polarity of the connection |
| DPPUEN\_B\_PHY\_SEL | rw | 1 | 1'b0 | The control source selection for pull-up resistor |
| Reserved | rw | 2 | 1'b0 | Reserved |
| USB\_VBUS | rw | 3 | 1'b0 | USB connection voltage selection |
| USB\_PHYSTDBY | rw | 4 | 1'b0 | 1 to enable USB\_PHY in standby mode |
| USB\_PHYSTDBY\_WEN | rw | 5 | 1'b0 | 1 to enable USB\_PHYSTDBY control by register |
| Reserved | rw | 31:6 | 26'b0 | Reserved |

### SYSCON\_PMU\_CTRL2

Offset Address: 0x40000880

power management uinit control register 2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| BG\_PDM\_DIS | rw | 0 | 1'b0 | 1 to power down bandcap in power down mode |
| MV2I\_PDM\_DIS | rw | 1 | 1'b0 | 1 to power down V2I in power down mode |
| VREG\_A\_PDM\_DIS | rw | 2 | 1'b0 | 1 to power down VREG\_A in power down mode |
| VREG\_D\_PDM\_DIS | rw | 3 | 1'b0 | 1 to power down VREG\_D in power down mode |
| XTAL\_PDM\_DIS | rw | 4 | 1'b0 | 1 to power down XTAL in power down mode |
| OSC32M\_PDM\_DIS | rw | 5 | 1'b0 | 1 to power down OSC32M in power down mode |
| RFAGC\_ON | rw | 6 | 1'b0 | 1 to enable RFAGC |
| RX\_EN\_SEL | rw | 7 | 1'b0 | RX\_EN width selection |
| BG\_DIS | rw | 8 | 1'b0 | 1 to switch off bandcap power |
| MV2I\_DIS | rw | 9 | 1'b0 | 1 to switch off V2I power |
| VREG\_A\_DIS | rw | 10 | 1'b0 | 1 to switch off VREG\_A power |
| VREG\_D\_DIS | rw | 11 | 1'b0 | 1 to switch off VREG\_D power |
| LO\_DIS | rw | 12 | 1'b0 | 1 to switch off LO power |
| VCO\_DIS | rw | 13 | 1'b0 | 1 to switch off VCO power |
| PA\_PK\_DIS | rw | 14 | 1'b0 | 1 to switch off PA peek detector power |
| PA\_DIS | rw | 15 | 1'b0 | 1 to switch off PA power |
| LNA\_DIS | rw | 16 | 1'b0 | 1 to switch off LNA power |
| MIXER\_DIS | rw | 17 | 1'b0 | 1 to switch off MIXER power |
| PKDET\_DIS | rw | 18 | 1'b0 | 1 to switch off RRF and PPF peek detector power |
| PPF\_DIS | rw | 19 | 1'b0 | 1 to switch off PPF power |
| SAR\_DIS | rw | 20 | 1'b0 | 1 to switch off SAR ADC power |
| RC\_CAL\_DIS | rw | 21 | 1'b0 | 1 to switch off RCCAL power |
| Reserved | rw | 28:22 | 7'b0 | Reserved |
| FLSH\_DIS | rw | 29 | 1'b0 | 1 to switch off flash power |
| FLSH\_PDM\_DIS | rw | 30 | 1'b0 | 1 to power down flash VDD25 in power down mode |
| SEL\_PD | rw | 31 | 1'b0 | power control selection |

### SYSCON\_ANA\_CTRL1

Offset Address: 0x40000884

IVREF and DVREG setting register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| VDD\_PMU\_SET\_PDM | rw | 1:0 | 2'b0 | Vdd\_pmu while in power down |
| VDD\_PMU\_SET | rw | 3:2 | 2'b0 | Vdd\_pmu while wakeup |
| VDD\_MEM\_SET\_PDM | rw | 5:4 | 2'b0 | Vdd\_mem while in power down mode |
| VDD\_MEM\_SET | rw | 7:6 | 2'b0 | Vdd\_mem while wakeup |
| VDD\_PMU\_SET\_EXTRA | rw | 8 | 1'b0 | extra high setting for vdd\_pmu |
| VDD\_MEM\_SET\_EXTRA | rw | 9 | 1'b0 | extra high setting for vdd\_mem |
| VDD\_PMU\_SET\_ULTRA\_LOW | rw | 10 | 1'b0 | ultra low setting for vdd\_pmu |
| VDD\_PMU\_MEM\_SW | rw | 11 | 1'b0 | 1 to close the switch betwwen vdd\_omu and vdd\_mem |
| IV\_BG\_SEL | rw | 15:12 | 4'b0 | VBG voltage select- |
| PDM\_DIS\_BUCK | rw | 16 | 1'b0 | 1 to power off buck in power down mode |
| BUCK\_PD\_CCM | rw | 17 | 1'b0 | 0 buck in CCM mode |
| BUCK\_PD\_DCM | rw | 18 | 1'b0 | 0 buck in DCM mode |
| IV\_IREF\_SEL | rw | 20:19 | 2'b0 | Reference current select |
| IV\_VREG11\_SET | rw | 23:21 | 3'b0 | VREG11 setting |
| XTAL32K\_FORCE\_RDY | rw | 24 | 1'b0 | Xtal32k ready from register |
| MX32\_SMT\_EN | rw | 25 | 1'b0 | 1 to enable schmidt trigger in xtal32 |
| BM\_X32BUF | rw | 27:26 | 2'b0 | Xtal 32 buffer current bias |
| DVREG11\_SET\_DIG | rw | 30:28 | 3'b0 | Vregd set |
| BUCK\_DPD | rw | 31 | 1'b0 | ZC control select |

### SYSCON\_MISC

Offset Address: 0x40000890

MISC register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| RCO\_PWR\_MODE | rw | 1:0 | 2'b0 | RCO VDD selection |
| Reserved | rw | 15:2 | 14'b0 | Reserved |
| EN\_SWD | rw | 16 | 1'b0 | enable swd register when SWD is selected in PIO\_FUNC\_CTRL |
| DIS\_FLSH\_POWER | rw | 17 | 1'b0 | flash power disable |
| DIS\_USB\_PULLUP | rw | 18 | 1'b0 | USB pull resister connection |
| Reserved | rw | 23:19 | 5'b0 | Reserved |
| DPPU\_OPT\_SEL | rw | 24 | 1'b0 | pull up strength source. 0: from DPPU\_OPT\_POL, 1: from usb device |
| DPPU\_OPT\_POL | rw | 25 | 1'b0 | swap pull up strength value |
| Reserved | rw | 31:26 | 6'b0 | Reserved |

### WDT\_LOAD

Offset Address: 0x40001000

watch dog counter start value register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| LOAD | rw | 31:0 | 32'b0 | Contain the value from which the counter is to decrement. When this register is written to the count is immediately restarted from the new value. The minimum valid value is 1. |

### WDT\_VALUE

Offset Address: 0x40001004

watch dog counter value register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| VALUE | rw | 31:0 | 32'b0 | The current value of the decrementing counter. |

### WDT\_CTRL

Offset Address: 0x40001008

watch dog control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| INTEN | rw | 0 | 1'b0 | Enable the interrupt event WDOGINT. Set HIGH to enable the counter and the interrupt and set LOW to disable the counter and interrupt. Reloads the counter from the value in WDOGLOAD when the interrupt is enabled, and was previously disabled. |
| RESEN | rw | 1 | 1'b0 | Enable watchdog reset output WDOGRES. Acts as a mask for the reset output. Set HIGH to enablethe reset and LOW to disable the reset. |
| Reserved | rw | 31:2 | 30'b0 | Reserved |

### WDT\_INT\_CLR

Offset Address: 0x4000100c

interrupt clear register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| INTCLR | rw | 0 | 1'b0 | A write of any value to the Register clears the watchdog interrupt and reloads the counter from the value in WDOGLOAD. |
| Reserved | rw | 31:1 | 31'b0 | Reserved |

### WDT\_INT\_RAW

Offset Address: 0x40001010

raw interrupt status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| RAWINTSTAT | rw | 0 | 1'b0 | Raw interrupt status from the counter |
| Reserved | rw | 31:1 | 31'b0 | Reserved |

### WDT\_MIS

Offset Address: 0x40001014

interrupt mask register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MASKINTSTAT | rw | 0 | 1'b0 | Enabled interrupt status from the counter |
| Reserved | rw | 31:1 | 31'b0 | Reserved |

### WDT\_LOCK

Offset Address: 0x40001020

watch dog lock register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| LOCK\_31\_0 | rw | 31:0 | 32'b0 | Writing 0x1ACCE551to this register enables write access to all other registers. |

### CTIMER0\_IR

Offset Address: 0x40002000

Interrupt Register. The IR can be written to clear interrupts. The IR can be read to identify which of eight possible interrupt sources are pending.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MR0INT | rw | 0 | 1'b0 | Interrupt flag for match channel 0. |
| MR1INT | rw | 1 | 1'b0 | Interrupt flag for match channel 1. |
| MR2INT | rw | 2 | 1'b0 | Interrupt flag for match channel 2. |
| MR3INT | rw | 3 | 1'b0 | Interrupt flag for match channel 3. |
| CR0INT | rw | 4 | 1'b0 | Interrupt flag for capture channel 0 event. |
| CR1INT | rw | 5 | 1'b0 | Interrupt flag for capture channel 1 event. |
| CR2INT | rw | 6 | 1'b0 | Interrupt flag for capture channel 2 event. |
| Reserved | rw | 31:7 | 25'b0 | Reserved |

### CTIMER0\_TCR

Offset Address: 0x40002004

Timer Control Register. The TCR is used to control the Timer Counter functions. The Timer Counter can be disabled or reset through the TCR.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CEN | rw | 0 | 1'b0 | Counter enable. |
| CRST | rw | 1 | 1'b0 | Counter reset. |
| Reserved | rw | 31:2 | 30'b0 | Reserved |

### CTIMER0\_TC

Offset Address: 0x40002008

Timer Counter. The 32 bit TC is incremented every PR+1 cycles of the APB bus clock. The TC is controlled through the TCR.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TCVAL | rw | 31:0 | 32'b0 | Timer counter value. |

### CTIMER0\_PR

Offset Address: 0x4000200c

Prescale Register. When the Prescale Counter (PC) is equal to this value, the next clock increments the TC and clears the PC.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PRVAL | rw | 31:0 | 32'b0 | Prescale counter value. |

### CTIMER0\_PC

Offset Address: 0x40002010

Prescale Counter. The 32 bit PC is a counter which is incremented to the value stored in PR. When the value in PR is reached, the TC is incremented and the PC is cleared. The PC is observable and controllable through the bus interface.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PCVAL | rw | 31:0 | 32'b0 | Prescale counter value. |

### CTIMER0\_MCR

Offset Address: 0x40002014

Match Control Register. The MCR is used to control if an interrupt is generated and if the TC is reset when a Match occurs.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MR0I | rw | 0 | 1'b0 | Interrupt on MR0: an interrupt is generated when MR0 matches the value in the TC. 0 = disabled. 1 = enabled. |
| MR0R | rw | 1 | 1'b0 | Reset on MR0: the TC will be reset if MR0 matches it. 0 = disabled. 1 = enabled. |
| MR0S | rw | 2 | 1'b0 | Stop on MR0: the TC and PC will be stopped and TCR[0] will be set to 0 if MR0 matches the TC. 0 = disabled. 1 = enabled. |
| MR1I | rw | 3 | 1'b0 | Interrupt on MR1: an interrupt is generated when MR1 matches the value in the TC. 0 = disabled. 1 = enabled. 0 = disabled. 1 = enabled. |
| MR1R | rw | 4 | 1'b0 | Reset on MR1: the TC will be reset if MR1 matches it. 0 = disabled. 1 = enabled. |
| MR1S | rw | 5 | 1'b0 | Stop on MR1: the TC and PC will be stopped and TCR[0] will be set to 0 if MR1 matches the TC. 0 = disabled. 1 = enabled. |
| MR2I | rw | 6 | 1'b0 | Interrupt on MR2: an interrupt is generated when MR2 matches the value in the TC. 0 = disabled. 1 = enabled. |
| MR2R | rw | 7 | 1'b0 | Reset on MR2: the TC will be reset if MR2 matches it. 0 = disabled. 1 = enabled. |
| MR2S | rw | 8 | 1'b0 | Stop on MR2: the TC and PC will be stopped and TCR[0] will be set to 0 if MR2 matches the TC. 0 = disabled. 1 = enabled. |
| MR3I | rw | 9 | 1'b0 | Interrupt on MR3: an interrupt is generated when MR3 matches the value in the TC. 0 = disabled. 1 = enabled. |
| MR3R | rw | 10 | 1'b0 | Reset on MR3: the TC will be reset if MR3 matches it. 0 = disabled. 1 = enabled. |
| MR3S | rw | 11 | 1'b0 | Stop on MR3: the TC and PC will be stopped and TCR[0] will be set to 0 if MR3 matches the TC. 0 = disabled. 1 = enabled. |
| Reserved | rw | 31:12 | 20'b0 | Reserved |

### CTIMER0\_MRs

Offset Address: 0x40002018

Match Register . MR can be enabled through the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt every time MR matches the TC.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MATCH | rw | 31:0 | 32'b0 | Timer counter match value. |

### CTIMER0\_CCR

Offset Address: 0x40002028

Capture Control Register. The CCR controls which edges of the capture inputs are used to load the Capture Registers and whether or not an interrupt is generated when a capture takes place.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CAP0RE | rw | 0 | 1'b0 | Rising edge of capture channel 0: a sequence of 0 then 1 causes CR0 to be loaded with the contents of TC. 0 = disabled. 1 = enabled. |
| CAP0FE | rw | 1 | 1'b0 | Falling edge of capture channel 0: a sequence of 1 then 0 causes CR0 to be loaded with the contents of TC. 0 = disabled. 1 = enabled. |
| CAP0I | rw | 2 | 1'b0 | Generate interrupt on channel 0 capture event: a CR0 load generates an interrupt. |
| CAP1RE | rw | 3 | 1'b0 | Rising edge of capture channel 1: a sequence of 0 then 1 causes CR1 to be loaded with the contents of TC. 0 = disabled. 1 = enabled. |
| CAP1FE | rw | 4 | 1'b0 | Falling edge of capture channel 1: a sequence of 1 then 0 causes CR1 to be loaded with the contents of TC. 0 = disabled. 1 = enabled. |
| CAP1I | rw | 5 | 1'b0 | Generate interrupt on channel 1 capture event: a CR1 load generates an interrupt. |
| CAP2RE | rw | 6 | 1'b0 | Rising edge of capture channel 2: a sequence of 0 then 1 causes CR2 to be loaded with the contents of TC. 0 = disabled. 1 = enabled. |
| CAP2FE | rw | 7 | 1'b0 | Falling edge of capture channel 2: a sequence of 1 then 0 causes CR2 to be loaded with the contents of TC. 0 = disabled. 1 = enabled. |
| CAP2I | rw | 8 | 1'b0 | Generate interrupt on channel 2 capture event: a CR2 load generates an interrupt. |
| Reserved | rw | 31:9 | 23'b0 | Reserved |

### CTIMER0\_CRs

Offset Address: 0x4000202c

Capture Register . CR is loaded with the value of TC when there is an event on the CAPn. input.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CAP | rw | 31:0 | 32'b0 | Timer counter capture value. |

### CTIMER0\_EMR

Offset Address: 0x4000203c

External Match Register. The EMR controls the match function and the external match pins.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| EM0 | rw | 0 | 1'b0 | External Match 0. This bit reflects the state of output MAT0, whether or not this output is connected to a pin. When a match occurs between the TC and MR0, this bit can either toggle, go LOW, go HIGH, or do nothing, as selected by EMR[5:4]. This bit is driven to the MAT pins if the match function is selected via IOCON. 0 = LOW. 1 = HIGH. |
| EM1 | rw | 1 | 1'b0 | External Match 1. This bit reflects the state of output MAT1, whether or not this output is connected to a pin. When a match occurs between the TC and MR1, this bit can either toggle, go LOW, go HIGH, or do nothing, as selected by EMR[7:6]. This bit is driven to the MAT pins if the match function is selected via IOCON. 0 = LOW. 1 = HIGH. |
| EM2 | rw | 2 | 1'b0 | External Match 2. This bit reflects the state of output MAT2, whether or not this output is connected to a pin. When a match occurs between the TC and MR2, this bit can either toggle, go LOW, go HIGH, or do nothing, as selected by EMR[9:8]. This bit is driven to the MAT pins if the match function is selected via IOCON. 0 = LOW. 1 = HIGH. |
| EM3 | rw | 3 | 1'b0 | External Match 3. This bit reflects the state of output MAT3, whether or not this output is connected to a pin. When a match occurs between the TC and MR3, this bit can either toggle, go LOW, go HIGH, or do nothing, as selected by MR[11:10]. This bit is driven to the MAT pins if the match function is selected via IOCON. 0 = LOW. 1 = HIGH. |
| EMC0 | rw | 5:4 | 2'b0 | External Match Control 0. Determines the functionality of External Match 0. |
| EMC1 | rw | 7:6 | 2'b0 | External Match Control 1. Determines the functionality of External Match 1. |
| EMC2 | rw | 9:8 | 2'b0 | External Match Control 2. Determines the functionality of External Match 2. |
| EMC3 | rw | 11:10 | 2'b0 | External Match Control 3. Determines the functionality of External Match 3. |
| Reserved | rw | 31:12 | 20'b0 | Reserved |

### CTIMER0\_CTCR

Offset Address: 0x40002070

Count Control Register. The CTCR selects between Timer and Counter mode, and in Counter mode selects the signal and edge(s) for counting.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CTMODE | rw | 1:0 | 2'b0 | Counter/Timer Mode This field selects which rising APB bus clock edges can increment Timer'-s Prescale Counter (PC), or clear PC and increment Timer Counter (TC). Timer Mode: the TC is incremented when the Prescale Counter matches the Prescale Register. |
| CINSEL | rw | 3:2 | 2'b0 | Count Input Select When bits 1:0 in this register are not 00, these bits select which CAP pin is sampled for clocking. Note: If Counter mode is selected for a particular CAPn input in the CTCR, the 3 bits for that input in the Capture Control Register (CCR) must be programmed as 000. However, capture and/or interrupt can be selected for the other 3 CAPn inputs in the same timer. |
| ENCC | rw | 4 | 1'b0 | Setting this bit to 1 enables clearing of the timer and the prescaler when the capture-edge event specified in bits 7:5 occurs. |
| SELCC | rw | 7:5 | 3'b0 | Edge select. When bit 4 is 1, these bits select which capture input edge will cause the timer and prescaler to be cleared. These bits have no effect when bit 4 is low. Values 0x2 to 0x3 and 0x6 to 0x7 are reserved. |
| Reserved | rw | 31:8 | 24'b0 | Reserved |

### CTIMER0\_PWMC

Offset Address: 0x40002074

PWM Control Register. The PWMCON enables PWM mode for the external match pins.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PWMEN0 | rw | 0 | 1'b0 | PWM mode enable for channel0. |
| PWMEN1 | rw | 1 | 1'b0 | PWM mode enable for channel1. |
| PWMEN2 | rw | 2 | 1'b0 | PWM mode enable for channel2. |
| PWMEN3 | rw | 3 | 1'b0 | PWM mode enable for channel3. Note: It is recommended to use match channel 3 to set the PWM cycle. |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### PINT\_ISEL

Offset Address: 0x40006000

Pin Interrupt Mode register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PMODE | rw | 3:0 | 4'b0 | Selects the interrupt mode for each pin interrupt. Bit n configures the pin interrupt selected in PINTSELn. 0 = Edge sensitive 1 = Level sensitive |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### PINT\_IENR

Offset Address: 0x40006004

Pin interrupt level or rising edge interrupt enable register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ENRL | rw | 3:0 | 4'b0 | Enables the rising edge or level interrupt for each pin interrupt. Bit n configures the pin interrupt selected in PINTSELn. 0 = Disable rising edge or level interrupt. 1 = Enable rising edge or level interrupt. |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### PINT\_SIENR

Offset Address: 0x40006008

Pin interrupt level or rising edge interrupt set register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SETENRL | rw | 3:0 | 4'b0 | Ones written to this address set bits in the IENR, thus enabling interrupts. Bit n sets bit n in the IENR register. 0 = No operation. 1 = Enable rising edge or level interrupt. |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### PINT\_CIENR

Offset Address: 0x4000600c

Pin interrupt level (rising edge interrupt) clear register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CENRL | rw | 3:0 | 4'b0 | Ones written to this address clear bits in the IENR, thus disabling the interrupts. Bit n clears bit n in the IENR register. 0 = No operation. 1 = Disable rising edge or level interrupt. |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### PINT\_IENF

Offset Address: 0x40006010

Pin interrupt active level or falling edge interrupt enable register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ENAF | rw | 3:0 | 4'b0 | Enables the falling edge or configures the active level interrupt for each pin interrupt. Bit n configures the pin interrupt selected in PINTSELn. 0 = Disable falling edge interrupt or set active interrupt level LOW. 1 = Enable falling edge interrupt enabled or set active interrupt level HIGH. |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### PINT\_SIENF

Offset Address: 0x40006014

Pin interrupt active level or falling edge interrupt set register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SETENAF | rw | 3:0 | 4'b0 | Ones written to this address set bits in the IENF, thus enabling interrupts. Bit n sets bit n in the IENF register. 0 = No operation. 1 = Select HIGH-active interrupt or enable falling edge interrupt. |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### PINT\_CIENF

Offset Address: 0x40006018

Pin interrupt active level or falling edge interrupt clear register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CENAF | rw | 3:0 | 4'b0 | Ones written to this address clears bits in the IENF, thus disabling interrupts. Bit n clears bit n in the IENF register. 0 = No operation. 1 = LOW-active interrupt selected or falling edge interrupt disabled. |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### PINT\_RISE

Offset Address: 0x4000601c

Pin interrupt rising edge register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| RDET | rw | 3:0 | 4'b0 | Rising edge detect. Bit n detects the rising edge of the pin selected in PINTSELn. Read 0: No rising edge has been detected on this pin since Reset or the last time a one was written to this bit. Write 0: no operation. Read 1: a rising edge has been detected since Reset or the last time a one was written to this bit. Write 1: clear rising edge detection for this pin. |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### PINT\_FALL

Offset Address: 0x40006020

Pin interrupt falling edge register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FDET | rw | 3:0 | 4'b0 | Falling edge detect. Bit n detects the falling edge of the pin selected in PINTSELn. Read 0: No falling edge has been detected on this pin since Reset or the last time a one was written to this bit. Write 0: no operation. Read 1: a falling edge has been detected since Reset or the last time a one was written to this bit. Write 1: clear falling edge detection for this pin. |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### PINT\_IST

Offset Address: 0x40006024

Pin interrupt status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PSTAT | rw | 3:0 | 4'b0 | Pin interrupt status. Bit n returns the status, clears the edge interrupt, or inverts the active level of the pin selected in PINTSELn. Read 0: interrupt is not being requested for this interrupt pin. Write 0: no operation. Read 1: interrupt is being requested for this interrupt pin. Write 1 (edge-sensitive): clear rising- and falling-edge detection for this pin. Write 1 (level-sensitive): switch the active level for this pin (in the IENF register). |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### PINT\_PMCTRL

Offset Address: 0x40006028

Pattern match interrupt control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SEL\_PMATCH | rw | 0 | 1'b0 | Specifies whether the 8 pin interrupts are controlled by the pin interrupt function or by the pattern match function. |
| ENA\_RXEV | rw | 1 | 1'b0 | Enables the RXEV output to the CPU and/or to a GPIO output when the specified boolean expression evaluates to true. |
| Reserved | rw | 23:2 | 22'b0 | Reserved |
| PMAT | rw | 31:24 | 8'b0 | This field displays the current state of pattern matches. A 1 in any bit of this field indicates that the corresponding product term is matched by the current state of the appropriate inputs. |

### PINT\_PMSRC

Offset Address: 0x4000602c

Pattern match interrupt bit-slice source register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 7:0 | 8'b0 | Reserved |
| SRC0 | rw | 10:8 | 3'b0 | Selects the input source for bit slice 0 |
| SRC1 | rw | 13:11 | 3'b0 | Selects the input source for bit slice 1 |
| SRC2 | rw | 16:14 | 3'b0 | Selects the input source for bit slice 2 |
| SRC3 | rw | 19:17 | 3'b0 | Selects the input source for bit slice 3 |
| SRC4 | rw | 22:20 | 3'b0 | Selects the input source for bit slice 4 |
| SRC5 | rw | 25:23 | 3'b0 | Selects the input source for bit slice 5 |
| SRC6 | rw | 28:26 | 3'b0 | Selects the input source for bit slice 6 |
| SRC7 | rw | 31:29 | 3'b0 | Selects the input source for bit slice 7 |

### PINT\_PMCFG

Offset Address: 0x40006030

Pattern match interrupt bit slice configuration register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PROD\_ENDPTS0 | rw | 0 | 1'b0 | Determines whether slice 0 is an endpoint. |
| PROD\_ENDPTS1 | rw | 1 | 1'b0 | Determines whether slice 1 is an endpoint. |
| PROD\_ENDPTS2 | rw | 2 | 1'b0 | Determines whether slice 2 is an endpoint. |
| PROD\_ENDPTS3 | rw | 3 | 1'b0 | Determines whether slice 3 is an endpoint. |
| PROD\_ENDPTS4 | rw | 4 | 1'b0 | Determines whether slice 4 is an endpoint. |
| PROD\_ENDPTS5 | rw | 5 | 1'b0 | Determines whether slice 5 is an endpoint. |
| PROD\_ENDPTS6 | rw | 6 | 1'b0 | Determines whether slice 6 is an endpoint. |
| Reserved | rw | 7 | 1'b0 | Reserved |
| CFG0 | rw | 10:8 | 3'b0 | Specifies the match contribution condition for bit slice 0. |
| CFG1 | rw | 13:11 | 3'b0 | Specifies the match contribution condition for bit slice 1. |
| CFG2 | rw | 16:14 | 3'b0 | Specifies the match contribution condition for bit slice 2. |
| CFG3 | rw | 19:17 | 3'b0 | Specifies the match contribution condition for bit slice 3. |
| CFG4 | rw | 22:20 | 3'b0 | Specifies the match contribution condition for bit slice 4. |
| CFG5 | rw | 25:23 | 3'b0 | Specifies the match contribution condition for bit slice 5. |
| CFG6 | rw | 28:26 | 3'b0 | Specifies the match contribution condition for bit slice 6. |
| CFG7 | rw | 31:29 | 3'b0 | Specifies the match contribution condition for bit slice 7. |

### INPUTMUX\_PINTSELs

Offset Address: 0x40006200

Pin interrupt select register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| INTPIN | rw | 4:0 | 5'b0 | Pin number select for pin interrupt or pattern match engine input. (PIO0\_0 to PIO1\_31 correspond to numbers 0 to 63). |
| Reserved | rw | 31:5 | 27'b0 | Reserved |

### INPUTMUX\_DMA\_ITRIG\_INMUXs

Offset Address: 0x40006400

Trigger select register for DMA channel

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| INP | rw | 4:0 | 5'b0 | Trigger input number (decimal value) for DMA channel n (n = 0 to 21). 0 = ADC0 Sequence A interrupt 1 = ADC0 Sequence B interrupt 2 = SCT0 DMA request 0 3 = SCT0 DMA request 1 4 = Timer CT32B0 Match 0 5 = Timer CT32B0 Match 1 6 = Timer CT32B1 Match 0 7 = Timer CT32B2 Match 0 8 = Timer CT32B2 Match 1 9 = Timer CT32B3 Match 0 10 = Timer CT32B4 Match 0 11 = Timer CT32B4 Match 1 12 = Pin interrupt 0 13 = Pin interrupt 1 14 = Pin interrupt 2 15 = Pin interrupt 3 16 = DMA output trigger mux 0 17 = DMA output trigger mux 1 18 = DMA output trigger mux 2 19 = DMA output trigger mux 3 |
| Reserved | rw | 31:5 | 27'b0 | Reserved |

### INPUTMUX\_DMA\_OTRIG\_INMUXs

Offset Address: 0x40006a00

DMA output trigger selection to become DMA trigger

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| INP | rw | 4:0 | 5'b0 | DMA trigger output number (decimal value) for DMA channel n (n = 0 to 19). |
| Reserved | rw | 31:5 | 27'b0 | Reserved |

### ADC\_CTRL

Offset Address: 0x40007000

ADC control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ENABLE | rw | 0 | 1'b0 | ADC enable. Write 1 to Writing 1 before starting conversion and 0 to end conversion. |
| CONV\_MODE | rw | 1 | 1'b0 | ADC conversion mode |
| SCAN\_EN | rw | 2 | 1'b0 | 1 to enable scan mode |
| WCMP\_EN | rw | 3 | 1'b0 | 1 to enable window compare |
| Reserved | rw | 6:4 | 3'b0 | Reserved |
| SW\_START | rw | 7 | 1'b0 | Software start ADC conversion write1 to trigger one time ADC conversion, no need clear. |
| CLKSEL | rw | 12:8 | 5'b0 | Sigma-Delta ADC clock select |
| SIG\_INV\_EN | rw | 13 | 1'b0 | 1 to invert Signma-Delta input signal |
| VREF\_SEL | rw | 15:14 | 2'b0 | Sigma-Delta ADC Reference source selection. |
| Reserved | rw | 17:16 | 2'b0 | Reserved |
| CH\_IDX\_EN | rw | 18 | 1'b0 | 1 to append channel index in data result to be used in scan mode |
| DATA\_FORMAT | rw | 19 | 1'b0 | Data output format. When DATA\_FORMAT ==0, When CH\_IDX\_EN ==0, the ADC\_DATA[31:0] is adc data, signed data, 31 bit frac. When CH\_IDX\_EN ==1, the ADC\_DATA[4:0] is channel output, {ADC\_DATA[31:5],5'h0} is adc data, signed data, 31 bit frac. When DATA\_FORMAT ==1, When CH\_IDX\_EN ==0, the ADC\_DATA[22:0] is adc data, signed data, 22 bit frac. When CH\_IDX\_EN ==1, the ADC\_DATA[31:27] is channel output, ADC\_DATA[22:0] is adc data, signed data, 22 bit frac. |
| VREFO\_EN | rw | 20 | 1'b0 | 1 to enable bandgap out-chip capacitor |
| SRST\_DIS | rw | 21 | 1'b0 | 1 to disable adc reset. |
| Reserved | rw | 22 | 1'b0 | Reserved |
| TRIGGER | rw | 28:23 | 6'b0 | Adc start trigger. 0 to 31 PA00 to PA31; 32 to 34 GPIOB0 to GPIOB2; 35, software trigger; 36, rng trigger; 56 to 59, timer 0 to timer 3; 60 to 63 pwm 0 to pwm 3 |
| Reserved | rw | 31:29 | 3'b0 | Reserved |

### ADC\_CH\_SEL

Offset Address: 0x40007004

ADC channel selection register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CH\_SEL | rw | 31:0 | 32'b0 | In scan conversion mode, the channels with 1 set will be scanned, from LSB to MSB. In none scan conversion mode, only the first channel from LSB with 1 set will be converted. If all bits are set to 0, no ADC conversion will be started. |

### ADC\_CH\_CFG

Offset Address: 0x40007008

ADC channel configuration register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CH\_CFG | rw | 31:0 | 32'b0 | whenCH\_CONFIG[N] is 0, the N channelwill select the configure 0 option(seeregister SD\_CONFIG0). whenCH\_CONFIG[N] is 1, the N channelwill select the configure 1 option(seeregister SD\_CONFIG1). |

### ADC\_WCMP\_THR

Offset Address: 0x4000700c

Window compare threshold register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| WCMP\_THR\_LOW | rw | 15:0 | 16'b0 | &lt;s 0 15&gt; Windows compare low threshold. |
| WCMP\_THR\_HIGH | rw | 31:16 | 16'b0 | &lt;s 0 15&gt; Windows compare high threshold If ADC decimation result is out of the window one compare interrupt will be triggered. |

### ADC\_INTEN

Offset Address: 0x40007010

ADC interrupt enable register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DAT\_RDY\_INTEN | rw | 0 | 1'b0 | 1 to enable Data ready interrupt |
| WCMP\_INTEN | rw | 1 | 1'b0 | 1 to enable Window compare interrupt. |
| FIFO\_OF\_INTEN | rw | 2 | 1'b0 | 1 to enalble FIFO overflow interrupt. |
| Reserved | rw | 30:3 | 28'b0 | Reserved |
| ADC\_INTEN | rw | 31 | 1'b0 | 1 to enable ADC interrupt |

### ADC\_INT

Offset Address: 0x40007014

ADC interrupt status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DAT\_RDY\_INT | rw | 0 | 1'b0 | Data ready interrupt will be cleared after fifo data is read can not be cleared by write 1. |
| WCMP\_INT | rw | 1 | 1'b0 | Window compare interrupt. |
| FIFO\_OF\_INT | rw | 2 | 1'b0 | FIFO overflow interrupt. |
| Reserved | rw | 30:3 | 28'b0 | Reserved |
| ADC\_INT | rw | 31 | 1'b0 | ADC interrupt. |

### ADC\_DATA

Offset Address: 0x40007018

ADC converted data output

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DATA | rw | 31:0 | 32'b0 | ADC data read from FIFO. |

### ADC\_CFGs

Offset Address: 0x40007020

ADC configuration register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PGA\_GAIN | rw | 2:0 | 3'b0 | SD ADC input PGA gain=2^value the range is 1-16. |
| PGA\_BP | rw | 3 | 1'b0 | 1 to bypass SD ADC input PGA |
| PGA\_VINN | rw | 5:4 | 2'b0 | SD ADC PGA VIN input offset selection |
| ADC\_GAIN | rw | 7:6 | 2'b0 | SD ADC gain selection. |
| VREF\_GAIN | rw | 8 | 1'b0 | SD ADC Reference Gain seletion |
| ADC\_VCM | rw | 11:9 | 3'b0 | SD ADC input common voltage selection. |
| PGA\_VCM\_EN | rw | 12 | 1'b0 | SD ADC PGA output common voltage control enable signal. |
| PGA\_VCM\_DIR | rw | 13 | 1'b0 | SD ADC PGA output common voltage control direction signal. |
| PGA\_VCM | rw | 19:14 | 6'b0 | SD ADC PGA output common voltage, adjustment = (PGA\_VCM0[5]+1)\*(PGA\_VCM0[3:0]+1)\*40mv |
| DOWN\_SAMPLE\_RATE | rw | 22:20 | 3'b0 | Down sample rate |
| DS\_DATA\_STABLE | rw | 28:23 | 6'b0 | Down sample date stable number. you can keep the bit 1:0 to 2'b11. DS\_DATA\_STABLE0[5:2]+1 |
| SCAN\_INTV | rw | 31:29 | 3'b0 | Interval when switching ADC source; 2/4/8/16/32/64/128/256 clock cycle. |

### ADC\_BG\_BF

Offset Address: 0x40007028

ADC bandcap and buffer setting register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PGA\_BM | rw | 2:0 | 3'b0 | SD ADC buffer bias current selection. |
| Reserved | rw | 3 | 1'b0 | Reserved |
| BG\_SEL | rw | 7:4 | 4'b0 | Bandgap voltage selection to compensate PVT variations8 steps with 5mV each upward. VBG=1205+5\*BGSEL(mV) |
| Reserved | rw | 11:8 | 4'b0 | Reserved |
| TEMP\_EN | rw | 12 | 1'b0 | 1 to enable temperature sensor |
| PGA\_CHOP\_EN | rw | 13 | 1'b0 | 1 to enable chopper in PGA |
| PGA\_BM\_DIV2 | rw | 14 | 1'b0 | 1 to half PGA bias current |
| Reserved | rw | 31:15 | 17'b0 | Reserved |

### ADC\_ANA\_CTRL

Offset Address: 0x4000702c

ADC core and reference setting regsiter

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ADC\_BM | rw | 2:0 | 3'b0 | ADC bias current selection. |
| Reserved | rw | 3 | 1'b0 | Reserved |
| ADC\_ORDER | rw | 4 | 1'b0 | 1 to enable SD ADC 2 order mode selection |
| DITHER\_EN | rw | 5 | 1'b0 | 1 to enable SD ADC PN Sequence in chopper mode |
| CHOP\_EN | rw | 6 | 1'b0 | 1 to enable SD ADC chopper |
| INV\_CLK | rw | 7 | 1'b0 | 1 to invert SD ADC Output Clock |
| VREF\_BM | rw | 10:8 | 3'b0 | SD ADC Reference Driver bias current selection. |
| VREF\_BM\_X3 | rw | 11 | 1'b0 | SD ADC Reference Driver bias current triple. |
| VINN\_IN\_BM | rw | 14:12 | 3'b0 | PGA VlNN Input Driver bias current selection. |
| Reserved | rw | 15 | 1'b0 | Reserved |
| VINN\_OUT\_BM | rw | 18:16 | 3'b0 | PGA VlNN Output Driver bias current selection. |
| VINN\_OUT\_BM\_X3 | rw | 19 | 1'b0 | PGA VlNN Output Driver bias current triple. |
| ADC\_BM\_DIV2 | rw | 20 | 1'b0 | SD ADC bias current half. |
| Reserved | rw | 31:21 | 11'b0 | Reserved |

### DAC\_ANA\_CFG

Offset Address: 0x40007400

reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FILTER\_BM | rw | 2:0 | 3'b0 | Set the filter bias current |
| Reserved | rw | 3 | 1'b0 | Reserved |
| DAC\_AMP | rw | 6:4 | 3'b0 | Set the current bias of the DAC |
| Reserved | rw | 7 | 1'b0 | Reserved |
| FILTER\_BW | rw | 9:8 | 2'b0 | Set the Miller compensation capacitance of the OPAMP. This compensation capacitance is determined by the off-chip load resistance |
| Reserved | rw | 11:10 | 2'b0 | Reserved |
| FILTER\_150K\_EN | rw | 12 | 1'b0 | Set the filter type and bandwidth |
| Reserved | rw | 15:13 | 3'b0 | Reserved |
| VCM | rw | 19:16 | 4'b0 | Set the common mode I of the driver. |
| Reserved | rw | 31:20 | 12'b0 | Reserved |

### DAC\_CTRL

Offset Address: 0x40007404

DAC clock invert

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ENABLE | rw | 0 | 1'b0 | DAC module enable |
| SIN\_EN | rw | 1 | 1'b0 | Sin wave enable |
| MOD\_EN | rw | 2 | 1'b0 | Modulator enable |
| MOD\_WD | rw | 3 | 1'b0 | Modulator output width |
| SMPL\_RATE | rw | 6:4 | 3'b0 | sigma delta modulator down sample rate |
| SGN\_INV | rw | 7 | 1'b0 | Sign bit inverse |
| BUF\_IN\_ALGN | rw | 8 | 1'b0 | FIFO input data align |
| BUF\_OUT\_ALGN | rw | 9 | 1'b0 | FIFO output data and Sine wave generator output align mode when no modulation mode |
| TRG\_MODE | rw | 10 | 1'b0 | Trigger mode |
| TRG\_EDGE | rw | 12:11 | 2'b0 | Trigger edge select |
| Reserved | rw | 15:13 | 3'b0 | Reserved |
| TRG\_SEL | rw | 21:16 | 6'b0 | Trigger select |
| Reserved | rw | 23:22 | 2'b0 | Reserved |
| CLK\_DIV | rw | 30:24 | 7'b0 | DAC clock divider |
| CLK\_INV | rw | 31 | 1'b0 | DAC clock invert |

### DAC\_SIN\_CFG0

Offset Address: 0x40007408

sin amplitude

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SIN\_FREQ | rw | 15:0 | 16'b0 | sin frequency |
| SIN\_AMP | rw | 31:16 | 16'b0 | sin amplitude |

### DAC\_SIN\_CFG1

Offset Address: 0x4000740c

reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SIN\_DC | rw | 19:0 | 20'b0 | DC value of sin wave |
| Reserved | rw | 31:20 | 12'b0 | Reserved |

### DAC\_GAIN\_CTRL

Offset Address: 0x40007410

reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| GAIN\_CTRL | rw | 7:0 | 8'b0 | digital FIFO output multiply with GAIN\_CTRL to scale to certain range. Where GAIN\_CTRL is a &amp;lt;u 4 4&amp;gt; value. |
| Reserved | rw | 31:8 | 24'b0 | Reserved |

### DAC\_CLR\_TRG

Offset Address: 0x40007414

Reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| BUF\_CLR | rw | 0 | 1'b0 | clear buffer signal write 1 to clear. |
| SW\_TRG | rw | 1 | 1'b0 | Software trigger |
| Reserved | rw | 31:2 | 30'b0 | Reserved |

### DAC\_DIN

Offset Address: 0x40007418

DAC data input

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DIN | rw | 31:0 | 32'b0 | DAC data input |

### DAC\_INT

Offset Address: 0x4000741c

Reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| BUF\_NFUL\_INT | rw | 0 | 1'b0 | Buffer not full interrupt |
| BUF\_FUL\_INT | rw | 1 | 1'b0 | Buffer full interrupt |
| BUF\_EMT\_INT | rw | 2 | 1'b0 | Buffer empty interrupt |
| BUF\_HEMT\_INT | rw | 3 | 1'b0 | buffer half empty interrupt |
| BUF\_OV\_INT | rw | 4 | 1'b0 | Buffer overflow interrupt write 1 to clear |
| BUF\_UD\_INT | rw | 5 | 1'b0 | Buffer underflow interrupt write 1 to clear |
| BUF\_HFUL\_INT | rw | 6 | 1'b0 | Buffer half full interrupt |
| Reserved | rw | 31:7 | 25'b0 | Reserved |

### DAC\_INTEN

Offset Address: 0x40007420

Reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| BUF\_NFUL\_INTEN | rw | 0 | 1'b0 | buffer not full interrupt enable |
| BUF\_FUL\_INTEN | rw | 1 | 1'b0 | buffer full interrupt enable |
| BUF\_EMT\_INTEN | rw | 2 | 1'b0 | buffer empty interrupt enable |
| BUF\_HEMT\_INTEN | rw | 3 | 1'b0 | buffer half empty interrupt enable |
| BUF\_OV\_INTEN | rw | 4 | 1'b0 | buffer over flow interrupt enable |
| BUF\_UD\_INTEN | rw | 5 | 1'b0 | Buffer under flow interrupt enable |
| BUF\_HFUL\_INTEN | rw | 6 | 1'b0 | buffer half full interrupt enable |
| Reserved | rw | 31:7 | 25'b0 | Reserved |

### DAC\_INT\_STAT

Offset Address: 0x40007424

Reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| BUF\_NFUL\_INT\_STAT | rw | 0 | 1'b0 | buffer not full interrupt status |
| BUF\_FUL\_INT\_STAT | rw | 1 | 1'b0 | buffer full interrupt status |
| BUF\_EMT\_INT\_STAT | rw | 2 | 1'b0 | buffer empty interrupt status |
| BUF\_HEMT\_INT\_STAT | rw | 3 | 1'b0 | buffer half empty interrupt status |
| BUF\_OV\_INT\_STAT | rw | 4 | 1'b0 | buffer over flow interrupt status |
| BUF\_UD\_INT\_STAT | rw | 5 | 1'b0 | Buffer under flow interrupt status |
| BUF\_HFUL\_INT\_STAT | rw | 6 | 1'b0 | buffer half full interrupt status |
| Reserved | rw | 15:7 | 9'b0 | Reserved |
| DAC\_INT\_STAT | rw | 16 | 1'b0 | DAC all interrupt status |
| Reserved | rw | 31:17 | 15'b0 | Reserved |

### DAC\_STATUS

Offset Address: 0x40007428

Reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| BUSY | rw | 0 | 1'b0 | busy |
| Reserved | rw | 15:1 | 15'b0 | Reserved |
| BUF\_WR\_PTR | rw | 18:16 | 3'b0 | Buffer write pointer |
| Reserved | rw | 19 | 1'b0 | Reserved |
| BUF\_RD\_PTR | rw | 22:20 | 3'b0 | Buffer read pointer |
| Reserved | rw | 31:23 | 9'b0 | Reserved |

### CS\_CTRL0

Offset Address: 0x40007800

CapSense control register 0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ENABLE | rw | 0 | 1'b0 | CapSense enable. Write 1 to start work, 0 to stop. |
| SRST | rw | 1 | 1'b0 | Soft reset. Set 1 to reset, and 0 to de-assert. |
| OSC\_FREQ | rw | 7:2 | 6'b0 | Oscillation frequency control. The driving current will change accordingly. |
| Reserved | rw | 15:8 | 8'b0 | Reserved |
| CLK\_DIV | rw | 24:16 | 9'b0 | Clock divider from CLK\_APB : CLK\_CS\_DIV = CLK\_APB/(CLK\_DIV + 1) |
| Reserved | rw | 31:25 | 7'b0 | Reserved |

### CS\_CTRL1

Offset Address: 0x40007804

CapSense control register 1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PERIOD | rw | 15:0 | 16'b0 | The scan period for one channel, which is PERIOD/(CLK\_DIV+1) clock cycles of CLK\_APB. |
| CH | rw | 23:16 | 8'b0 | Channel enable, each bit represent one channel, with CH[0] for CS0, CH[1] for CS1 |
| Reserved | rw | 31:24 | 8'b0 | Reserved |

### CS\_INT

Offset Address: 0x40007808

Interrupt status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIFO\_NOTEMPTY\_INT | rw | 0 | 1'b0 | FIFO not empty status indicator. Will clear automatically if no data available. |
| FIFO\_HFULL\_INT | rw | 1 | 1'b0 | FIFO half full status indicator. Will clear automatically once less than half. |
| FIFO\_FULL\_INT | rw | 2 | 1'b0 | FIFO full status indicator. Will clear automatically once not full. |
| SCAN\_INT | rw | 3 | 1'b0 | Scan done status flag for all enabled channels. Write 1 to clear. |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### CS\_INTEN

Offset Address: 0x4000780c

Interrupt mask register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIFO\_NOTEMPTY\_INTEN | rw | 0 | 1'b0 | Interrupt mask of FIFO\_NOTEMPTY\_INT. Set 1 to enable the interrupt. |
| FIFO\_HFULL\_INTEN | rw | 1 | 1'b0 | Interrupt mask of FIFO\_HFULL\_INT. Set 1 to enable the interrupt. |
| FIFO\_FULL\_INTEN | rw | 2 | 1'b0 | Interrupt mask of FIFO\_FULL\_INT. Set 1 to enable the interrupt. |
| SCAN\_INTEN | rw | 3 | 1'b0 | Interrupt mask of SCAN\_INT. Set 1 to enable the interrupt. |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### CS\_DATA

Offset Address: 0x40007810

Output data register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DATA | rw | 18:0 | 19'b0 | Output data to MCU: DATA[18:16]: channel index, DATA[15:0]: counter output for that channel. |
| Reserved | rw | 31:19 | 13'b0 | Reserved |

### CS\_LP\_CTRL

Offset Address: 0x40007814

Control register for low power mode

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DEBONCE\_NUM | rw | 3:0 | 4'b0 | (DEBONCE\_NUM+1) consecutive samples to judge one touch action. |
| LP\_EN | rw | 4 | 1'b0 | Enable for low power mode. |
| LP\_CH | rw | 7:5 | 3'b0 | The index of the channel to monitor in low power mode, representing 0~7. |
| Reserved | rw | 15:8 | 8'b0 | Reserved |
| THR | rw | 31:16 | 16'b0 | Threshold to decide the touch action. |

### CS\_LP\_INT

Offset Address: 0x40007818

Low power interrupt register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| LP\_INT | rw | 0 | 1'b0 | Interrupt in low power mode when counter output is less than THR. |
| Reserved | rw | 31:1 | 31'b0 | Reserved |

### CS\_LP\_INTEN

Offset Address: 0x4000781c

low power interrupt enable register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| LP\_INTEN | rw | 0 | 1'b0 | Interrupt enable of LP\_INT. Set 1 to enable. |
| Reserved | rw | 31:1 | 31'b0 | Reserved |

### CS\_IDLE\_PERIOD

Offset Address: 0x40007820

Idle preiod number register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| IDLE\_PERIOD | rw | 15:0 | 16'b0 | Number of idle period. Zero represents no idle time between consecutive scan. |
| Reserved | rw | 31:16 | 16'b0 | Reserved |

### RNG\_CTRL

Offset Address: 0x40007c00

control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ENABLE | rw | 0 | 1'b0 | write 1 to enable randome number generator |
| START | rw | 1 | 1'b0 | write 1 to start random number generation, auto clear |
| Reserved | rw | 3:2 | 2'b0 | Reserved |
| NUM | rw | 5:4 | 2'b0 | total bits |
| Reserved | rw | 31:6 | 26'b0 | Reserved |

### RNG\_STAT

Offset Address: 0x40007c04

status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| BUSY | rw | 0 | 1'b0 | module in processing |
| Reserved | rw | 31:1 | 31'b0 | Reserved |

### RNG\_DATA

Offset Address: 0x40007c08

random data output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DATA | rw | 31:0 | 32'b0 | final random data read by SW |

### RNG\_INT

Offset Address: 0x40007c0c

interrupt register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DONE | rw | 0 | 1'b0 | random data generate done |
| Reserved | rw | 31:1 | 31'b0 | Reserved |

### RNG\_INTEN

Offset Address: 0x40007c10

interrupt mask register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DONE\_INTEN | rw | 0 | 1'b0 | random data generate done mask |
| Reserved | rw | 31:1 | 31'b0 | Reserved |

### QDEC0\_CTRL

Offset Address: 0x40009000

control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| QDEC\_EN | rw | 0 | 1'b0 | no description available |
| START | rw | 1 | 1'b0 | no description available |
| STOP | rw | 2 | 1'b0 | no description available |
| SOFT\_CLR | rw | 3 | 1'b0 | no description available |
| AUTO\_CLR\_EN | rw | 4 | 1'b0 | no description available |
| SINGLE\_SAMPLE\_SRST\_EN | rw | 5 | 1'b0 | no description available |
| DB\_FILTER\_EN | rw | 6 | 1'b0 | no description available |
| Reserved | rw | 31:7 | 25'b0 | Reserved |

### QDEC0\_SAMP\_CTRL

Offset Address: 0x40009004

QDEC sample settting register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DIVIDE | rw | 4:0 | 5'b0 | divide number to APB clk 0~20 total 21modes |
| Reserved | rw | 7:5 | 3'b0 | Reserved |
| PTS | rw | 11:8 | 4'b0 | total sample points 0~11 total 12modes cf. 8.2 |
| Reserved | rw | 15:12 | 4'b0 | Reserved |
| DB\_SAMP\_DIV | rw | 19:16 | 4'b0 | Debounce filter sample clk devide cf. 8.3 |
| Reserved | rw | 31:20 | 12'b0 | Reserved |

### QDEC0\_SAMPLE

Offset Address: 0x40009008

QDEC sample result register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SAMPLE | rw | 1:0 | 2'b0 | Sample value each time (2's complement) |
| Reserved | rw | 31:2 | 30'b0 | Reserved |

### QDEC0\_ACC

Offset Address: 0x4000900c

QDEC accumulate register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ACC | rw | 10:0 | 11'b0 | shift counter (-1 &amp; +1 ) normal case |
| Reserved | rw | 31:11 | 21'b0 | Reserved |

### QDEC0\_ACC\_R

Offset Address: 0x40009010

QDEC accumulate snapshot register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ACC\_R | rw | 10:0 | 11'b0 | ACC RO snapshot when END event is valid |
| Reserved | rw | 31:11 | 21'b0 | Reserved |

### QDEC0\_DB

Offset Address: 0x40009014

double sample register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DB | rw | 3:0 | 4'b0 | 2 trans counter ERROR case max value 15. |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### QDEC0\_DB\_R

Offset Address: 0x40009018

DB snapshot register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DB\_R | rw | 3:0 | 4'b0 | DB\_R RO snapshot when END event is valid |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### QDEC0\_INT

Offset Address: 0x4000901c

interrupt register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SINGLE\_SAMPLE | rw | 0 | 1'b0 | Each time when normal sample is done |
| SAMPLE\_END | rw | 1 | 1'b0 | END event triggered |
| ACC\_OF | rw | 2 | 1'b0 | Normal sample (+1/-1) number is overflow |
| DB\_OF | rw | 3 | 1'b0 | Double sample (2 trans )number is overflow |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### QDEC0\_INTEN

Offset Address: 0x40009020

interrupt mask register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SINGLE\_SAMPLE\_INTEN | rw | 0 | 1'b0 | single sample done interrupt enable |
| SAMPLE\_END\_INTEN | rw | 1 | 1'b0 | sample end interrupt enable |
| ACC\_OF\_INTEN | rw | 2 | 1'b0 | normal sample overflow interrupt enable |
| DB\_OF\_INTEN | rw | 3 | 1'b0 | double sample overflow interrupt enable |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### QDEC0\_STAT

Offset Address: 0x40009024

QDEC is running

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| BUSY | rw | 0 | 1'b0 | QDEC is running |
| Reserved | rw | 31:1 | 31'b0 | Reserved |

### RTC\_CTRL

Offset Address: 0x4000b000

RTC control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SEC\_INT\_EN | rw | 0 | 1'b0 | RTC second interrupt enable |
| Reserved | rw | 1 | 1'b0 | Reserved |
| CFG | rw | 2 | 1'b0 | RTC second configuration control. This bit is self-cleared after synchronization |
| Reserved | rw | 7:3 | 5'b0 | Reserved |
| CAL\_EN | rw | 8 | 1'b0 | Calibration enable |
| Reserved | rw | 31:9 | 23'b0 | Reserved |

### RTC\_STATUS

Offset Address: 0x4000b004

RTC status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SEC\_INT | rw | 0 | 1'b0 | Second interrupt flag |
| Reserved | rw | 7:1 | 7'b0 | Reserved |
| CTRL\_SYNC | rw | 8 | 1'b0 | Control Register synchronization busy indicator |
| STATUS\_SYNC | rw | 9 | 1'b0 | Status Register synchronization busy indicator |
| SEC\_SYNC | rw | 10 | 1'b0 | Second configuration Register synchronization busy indicator |
| Reserved | rw | 11 | 1'b0 | Reserved |
| CALIB\_SYNC | rw | 12 | 1'b0 | Calibration Register synchronization busy indicator |
| Reserved | rw | 15:13 | 3'b0 | Reserved |
| FREE\_SYNC | rw | 16 | 1'b0 | Free running counter control Register synchronization busy indicator |
| THR\_INT\_SYNC | rw | 17 | 1'b0 | Free running counter interrupt Threshold Register synchronization busy indicator |
| THR\_RST\_SYNC | rw | 18 | 1'b0 | Free running counter Reset Threshold Register synchronization busy indicator |
| Reserved | rw | 30:19 | 12'b0 | Reserved |
| FREE\_RUNNING\_INT | rw | 31 | 1'b0 | Free running interrupt status. |

### RTC\_SEC

Offset Address: 0x4000b008

RTC second register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SEC | rw | 31:0 | 32'b0 | Second configuration register. |

### RTC\_CAL

Offset Address: 0x4000b010

RTC calibration register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PPM | rw | 15:0 | 16'b0 | RTC calibration ppm value the precision is 1 ppm. |
| DIR | rw | 16 | 1'b0 | RTC calibration direction indicator |
| Reserved | rw | 31:17 | 15'b0 | Reserved |

### RTC\_CNT\_VAL

Offset Address: 0x4000b014

RTC count value register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CNT | rw | 14:0 | 15'b0 | RTC counter current value read only. |
| Reserved | rw | 31:15 | 17'b0 | Reserved |

### RTC\_CNT2\_CTRL

Offset Address: 0x4000b020

Free running control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CNT2\_EN | rw | 0 | 1'b0 | 1 to enable free running counter |
| CNT2\_INT\_EN | rw | 1 | 1'b0 | 1 to enable free running interrupt |
| CNT2\_WAKEUP | rw | 2 | 1'b0 | 1 to enable free running wakeup |
| CNT2\_RST | rw | 3 | 1'b0 | 1 to enable free running reset |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### RTC\_THR\_INT

Offset Address: 0x4000b024

interrupt threshold of free running counter register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| THR\_INT | rw | 31:0 | 32'b0 | The Threshold of free running counter is to generate free running interrupt. |

### RTC\_THR\_RST

Offset Address: 0x4000b028

reset threshold of free running counter register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| THR\_RST | rw | 31:0 | 32'b0 | The Threshold of free running counter is to generate free running reset. |

### RTC\_CNT2

Offset Address: 0x4000b02c

free running count value

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CNT2 | rw | 31:0 | 32'b0 | The current value of free running counter |

### AGC\_CTRL0

Offset Address: 0x4000c000

AGC control register 0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PPF\_INTRPT\_MOD | rw | 1:0 | 2'b0 | Control whether fsm can interrupt |
| FREZ\_MOD | rw | 3:2 | 2'b0 | Control whether fsm can restore last value when correalation trigh happens |
| RRF\_GAIN\_SEL | rw | 6:4 | 3'b0 | LNA gain controlGAIN=26-12\*LNA\_GAIN\_SEL |
| RRF\_WEN | rw | 7 | 1'b0 | Lna gain write enable |
| PPF\_GAIN | rw | 11:8 | 4'b0 | PPF gain controlGain=36-3\*PPF\_GAIN |
| PPF\_WEN | rw | 12 | 1'b0 | Ppf gain write enable |
| PKWT\_TH\_DIG\_1 | rw | 17:13 | 5'b0 | PKWT\_TH\_DIG + PKWT\_TH\_DIG\_ADD in ccode |
| PD\_CLR\_EN | rw | 18 | 1'b0 | Force clear analog PD |
| PD\_RST\_LEN | rw | 21:19 | 3'b0 | Pd disable time when reset0h0us 1h8us 2h16us 7h56us |
| RFAGC\_FSYNC\_DET\_DIS | rw | 22 | 1'b0 | Use to control rfagc gain adjust0brfagc stops when sync 1brfagc always on |
| RFAGC\_DIRECTION\_FREEZE | rw | 23 | 1'b0 | Use to disable rfagc gain adjust when switching antenna at direction found mode0b rfagc enable 1brfagc disable |
| DOWN\_24\_EN | rw | 24 | 1'b0 | Lna decrease 24dbm0bdisable 1benable |
| SWITCH\_PD\_RST\_LEN | rw | 26:25 | 2'b0 | Pd disable time when direction found rfagc reset00b2us 01b4us 10b8us 11b16us |
| GLNA\_MAX\_REDU | rw | 27 | 1'b0 | Lna max gain reduce 12dbm0bdisable 1benable |
| Reserved | rw | 31:28 | 4'b0 | Reserved |

### AGC\_CTRL1

Offset Address: 0x4000c004

AGC control register 1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PD3\_TH\_REG | rw | 2:0 | 3'b0 | Pd3 threshold |
| PD3\_TH\_HYST\_REG | rw | 6:3 | 4'b0 | Desired upper boundary |
| PKWT\_TH\_ANA\_1 | rw | 12:7 | 6'b0 | PKWT\_TH\_ANA + PKWT\_TH\_ANA\_ADD |
| PKWT\_TH\_ANA\_0 | rw | 17:13 | 5'b0 | PKWT\_TH\_ANA in ccode |
| PKWT\_TH\_DIG\_0 | rw | 22:18 | 5'b0 | PKWT\_TH\_DIG in ccode |
| SETL\_TH\_PPF\_2 | rw | 27:23 | 5'b0 | SETL\_TH\_PPF\_2 + DLY\_DIG 1 in ccode |
| Reserved | rw | 31:28 | 4'b0 | Reserved |

### AGC\_CTRL2

Offset Address: 0x4000c008

AGC control register 2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 7:0 | 8'b0 | Reserved |
| PPF\_PDVTH\_LOW | rw | 8 | 1'b0 | PPF peak detect threshold select |
| RRF\_MG\_PK | rw | 11:9 | 3'b0 | LNA medium gain peak detect threshold selectAMP=(400-25\* LNA\_MG\_PK)mv |
| RRF\_HG\_PK | rw | 14:12 | 3'b0 | LNA high gain peak detect threshold selectAMP=(100-8\* LNA\_HG\_PK)mv |
| Reserved | rw | 31:15 | 17'b0 | Reserved |

### AGC\_CTRL3

Offset Address: 0x4000c00c

AGC control register 3

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| GF2\_PAR00 | rw | 3:0 | 4'b0 | no description available |
| GF2\_PAR01 | rw | 7:4 | 4'b0 | no description available |
| GF2\_PAR10 | rw | 11:8 | 4'b0 | no description available |
| SETL\_TH\_OVSHT\_DIG | rw | 14:12 | 3'b0 | no description available |
| SETL\_TH\_OVSHT\_INTRPT | rw | 17:15 | 3'b0 | no description available |
| SETL\_TH\_OVSHT | rw | 20:18 | 3'b0 | no description available |
| Reserved | rw | 31:21 | 11'b0 | Reserved |

### AGC\_CTRL4

Offset Address: 0x4000c010

AGC control register 4

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SETL\_TH\_PD1 | rw | 3:0 | 4'b0 | no description available |
| SETL\_TH\_PD2 | rw | 7:4 | 4'b0 | no description available |
| SETL\_TH\_PD3\_1 | rw | 13:8 | 6'b0 | no description available |
| SETL\_TH\_PD3\_2 | rw | 19:14 | 6'b0 | no description available |
| GF2\_STAT24\_TH | rw | 23:20 | 4'b0 | no description available |
| Reserved | rw | 31:24 | 8'b0 | Reserved |

### AGC\_CTRL5

Offset Address: 0x4000c014

AGC control register 5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TEST\_CTRL | rw | 3:0 | 4'b0 | no description available |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### AGC\_STAT

Offset Address: 0x4000c018

AGC status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| GLNA\_CODE\_OUT | rw | 2:0 | 3'b0 | no description available |
| GF2\_CODE\_OUT | rw | 6:3 | 4'b0 | no description available |
| RFAGC\_TRIGGER\_O | rw | 7 | 1'b0 | no description available |
| RF\_GAIN | rw | 14:8 | 7'b0 | no description available |
| NUM\_GAIN\_ADJ | rw | 19:15 | 5'b0 | no description available |
| CUR\_STAT | rw | 22:20 | 3'b0 | no description available |
| Reserved | rw | 31:23 | 9'b0 | Reserved |

### PROP\_TX\_BUF

Offset Address: 0x4000d000

transmit data buffer input port register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TX\_BUF | rw | 7:0 | 8'b0 | TX BUF |
| Reserved | rw | 31:8 | 24'b0 | Reserved |

### PROP\_RX\_BUF

Offset Address: 0x4000d004

received data buffer output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| RX\_BUF | rw | 7:0 | 8'b0 | RX BUF |
| Reserved | rw | 31:8 | 24'b0 | Reserved |

### PROP\_STAT

Offset Address: 0x4000d008

status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| BIT\_ORDER | rw | 0 | 1'b0 | no description available |
| TX\_INTEN | rw | 1 | 1'b0 | TX interrupt enable |
| RX\_INTEN | rw | 2 | 1'b0 | RX interrupt enable |
| RX\_INT | rw | 3 | 1'b0 | RX interrupt |
| TX\_INT | rw | 4 | 1'b0 | TX interrupt |
| RX\_BUSY | rw | 5 | 1'b0 | RX is busy |
| TX\_BUSY | rw | 6 | 1'b0 | TX is busy |
| CLR | rw | 7 | 1'b0 | Clear intf control register. |
| Reserved | rw | 31:8 | 24'b0 | Reserved |

### BLEDP\_DP\_TOP\_SYSTEM\_CTRL

Offset Address: 0x4000e000

datapath system control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| RX\_PDU\_LEN\_IN | rw | 13:0 | 14'b0 | pdu length user programmed header+payload unit is bit. |
| AA\_SEL | rw | 14 | 1'b0 | access address selection |
| PDU\_LEN\_SEL | rw | 15 | 1'b0 | pdu length selection |
| H\_IDX | rw | 23:16 | 8'b0 | h index from 0.25 to 0.75 default is 0.5. |
| RX\_EN\_SEL | rw | 24 | 1'b0 | rx enable select signal |
| TX\_EN\_SEL | rw | 25 | 1'b0 | tx enable select signal |
| RX\_REQ | rw | 26 | 1'b0 | rx request. |
| TX\_REQ | rw | 27 | 1'b0 | tx request. |
| RX\_MODE | rw | 29:28 | 2'b0 | rx mode |
| ANT\_DATA\_START | rw | 30 | 1'b0 | ant mode data start signal need write 0 first then to 1. |
| DET\_MODE | rw | 31 | 1'b0 | detection mode 0low ppwer mode 1high performance mode. |

### BLEDP\_PROP\_MODE\_CTRL

Offset Address: 0x4000e004

properity mode control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PROP\_AA\_ADDR\_IN | rw | 7:0 | 8'b0 | prop mode when access address is 5 byte the access address is {prop\_aa\_addr\_in aa\_addr\_in} otherwise is aa\_addr\_in |
| PROP\_CRC\_NUM | rw | 9:8 | 2'b0 | prop mode crc number |
| Reserved | rw | 11:10 | 2'b0 | Reserved |
| PROP\_AA\_NUM | rw | 13:12 | 2'b0 | prop mode network address number |
| Reserved | rw | 15:14 | 2'b0 | Reserved |
| PROP\_PRE\_NUM | rw | 18:16 | 3'b0 | prop mode preamble number |
| Reserved | rw | 19 | 1'b0 | Reserved |
| PROP\_DATA\_RATE | rw | 21:20 | 2'b0 | prop mode data rate |
| PROP\_DIRECTION\_RATE | rw | 23:22 | 2'b0 | prop direction find mode sample rate |
| PROP\_DIRECTION\_MODE | rw | 24 | 1'b0 | prop direction find mode just work at prop mode. |
| RX\_ALWAYS\_ON | rw | 25 | 1'b0 | rx always on |
| TX\_ALWAYS\_ON | rw | 26 | 1'b0 | tx always on |
| TX\_POWER\_DONE\_TIME | rw | 31:27 | 5'b0 | tx power down time in ant mode and prop mode unit is us. |

### BLEDP\_ACCESS\_ADDRESS

Offset Address: 0x4000e008

access address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| AA\_ADDR\_IN | rw | 31:0 | 32'b0 | access address user programmed. |

### BLEDP\_ANT\_PDU\_DATA0

Offset Address: 0x4000e00c

pdu data 0 to 1 byte, and preamble register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PDU\_DATA0 | rw | 15:0 | 16'b0 | pdu data 0 to 1 byte |
| PATTERN\_SEL | rw | 19:16 | 4'b0 | pattern selection |
| TEST\_PATTERN\_EN | rw | 20 | 1'b0 | enable test pattern. |
| Reserved | rw | 22:21 | 2'b0 | Reserved |
| PROP\_PREAMBLE\_WEN | rw | 23 | 1'b0 | when high enable manual prop mode preamble. |
| PROP\_PREAMBLE | rw | 31:24 | 8'b0 | prop mode preamble. |

### BLEDP\_ANT\_PDU\_DATA1

Offset Address: 0x4000e010

pdu data 2 to 5 byte

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PDU\_DATA1 | rw | 31:0 | 32'b0 | pdu data 2 to 5 byte |

### BLEDP\_ANT\_PDU\_DATA2

Offset Address: 0x4000e014

pdu data 6 to 9 byte

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PDU\_DATA2 | rw | 31:0 | 32'b0 | pdu data 6 to 9 byte |

### BLEDP\_ANT\_PDU\_DATA3

Offset Address: 0x4000e018

pdu data 10 to 13 byte

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PDU\_DATA3 | rw | 31:0 | 32'b0 | pdu data 10 to 13 byte |

### BLEDP\_ANT\_PDU\_DATA4

Offset Address: 0x4000e01c

pdu data 14 to 17 byte

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PDU\_DATA4 | rw | 31:0 | 32'b0 | pdu data 14 to 17 byte |

### BLEDP\_ANT\_PDU\_DATA5

Offset Address: 0x4000e020

pdu data 18 to 21 byte

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PDU\_DATA5 | rw | 31:0 | 32'b0 | pdu data 18 to 21 byte |

### BLEDP\_ANT\_PDU\_DATA6

Offset Address: 0x4000e024

pdu data 22 to 25 byte

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PDU\_DATA6 | rw | 31:0 | 32'b0 | pdu data 22 to 25 byte |

### BLEDP\_ANT\_PDU\_DATA7

Offset Address: 0x4000e028

pdu data 26 to 29 byte

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PDU\_DATA7 | rw | 31:0 | 32'b0 | pdu data 26 to 29 byte |

### BLEDP\_CRCSEED

Offset Address: 0x4000e02c

crc seed

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CRC\_SEED\_IN | rw | 23:0 | 24'b0 | user programmed crc seed. |
| CRC\_SEED\_WEN | rw | 24 | 1'b0 | when high enable manual program crc seed. |
| Reserved | rw | 31:25 | 7'b0 | Reserved |

### BLEDP\_DP\_FUNCTION\_CTRL

Offset Address: 0x4000e030

datapath function control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DP\_STATISTICS\_SEL | rw | 2:0 | 3'b0 | datapath statistics selection. |
| CHF\_COEF\_WEN | rw | 3 | 1'b0 | manual select channel filter coefficent. |
| CHF\_COEF\_IDX | rw | 5:4 | 2'b0 | no description available |
| LP\_SNR\_LEN\_AUTO | rw | 6 | 1'b0 | when enable auto adjust lp mode snr acc length otherwise the legnth fixed. |
| DOUT\_ADJ\_DIS | rw | 7 | 1'b0 | data delay adjust disable. |
| LP\_ADJ\_MODE | rw | 8 | 1'b0 | lp mode delay adjust mode |
| FR\_OFFSET\_EN | rw | 9 | 1'b0 | pdu frequency offset track enable. |
| DC\_AVE\_EN | rw | 10 | 1'b0 | when high enable cfo estimation average. |
| FIX\_DELAY\_EN | rw | 11 | 1'b0 | no description available |
| TRACK\_LEN | rw | 13:12 | 2'b0 | track length |
| TRACK\_LEN\_WEN | rw | 14 | 1'b0 | when high manual track length. |
| Reserved | rw | 15 | 1'b0 | Reserved |
| XCORR\_FILT\_EN | rw | 16 | 1'b0 | when high enable xcorr filter. |
| XCORR\_FULLWIN\_EN | rw | 17 | 1'b0 | when xcorr\_win\_auto\_en low full sync enable. |
| XCORR\_AA\_LEN | rw | 18 | 1'b0 | select access address bit number |
| XCORR\_AA\_LEN\_WEN | rw | 19 | 1'b0 | enable manual correlation aa length. |
| XCORR\_WIN\_AUTO\_EN | rw | 20 | 1'b0 | correlation window size auto selection enable. |
| RESAMPLER\_TAP | rw | 21 | 1'b0 | resampler tap number |
| RESAMPLER\_TAP\_WEN | rw | 22 | 1'b0 | when high enable manual resampler tap number otherwise auto selection. |
| RESAMPLER\_BP | rw | 23 | 1'b0 | resampler enable or bypass |
| FAGC\_WIN\_LEN | rw | 24 | 1'b0 | select estimation length |
| FAGC\_WEN | rw | 25 | 1'b0 | when high enable manual fine agc gain. |
| HP\_CFO\_EN | rw | 26 | 1'b0 | when hp mode cfo estimation enable |
| CFO\_TRACK\_EN | rw | 27 | 1'b0 | tracking cfo enable. |
| CFO\_INI\_EN | rw | 28 | 1'b0 | initial cfo enable. |
| ADC\_IN\_FLIP | rw | 29 | 1'b0 | when 1 exchange i and q signals. |
| TX\_EN\_MODE | rw | 30 | 1'b0 | transmit mode |
| RX\_EN\_MODE | rw | 31 | 1'b0 | receiver mode |

### BLEDP\_DP\_TEST\_CTRL

Offset Address: 0x4000e034

datapath test iinterface register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TIF\_SEL | rw | 7:0 | 8'b0 | test interface selection. |
| TIF\_CLK\_SEL | rw | 9:8 | 2'b0 | test interface clock selection |
| Reserved | rw | 10 | 1'b0 | Reserved |
| CORDIC\_DAC\_OUT | rw | 11 | 1'b0 | when high cordic to dac |
| TIF\_EN | rw | 12 | 1'b0 | test interface enable |
| IMR\_INV | rw | 13 | 1'b0 | datapath mixer nco if selection |
| CLK\_TX\_GATE\_DIS | rw | 14 | 1'b0 | clock tx gate disable |
| BUF\_FULL\_OFFRF\_DIS | rw | 15 | 1'b0 | (new standard)\_\_\_\_\_\_when high rf always on in rx\_en other wise when buffer full rf will be off. |
| CLK\_BUST\_GATE\_DIS | rw | 16 | 1'b0 | clock burst gate disable |
| CLK\_RX\_GATE\_DIS | rw | 17 | 1'b0 | clock rx gate disable |
| CLK\_LPDET\_GATE\_DIS | rw | 18 | 1'b0 | clock lp mode detector gate disable |
| CLK\_HPDET\_GATE\_DIS | rw | 19 | 1'b0 | clock hp mode detector gate disable |
| CLK\_RFE\_GATE\_DIS | rw | 20 | 1'b0 | clock rfe gate disable |
| IQSWAP\_XOR | rw | 21 | 1'b0 | iq swap xor. |
| Reserved | rw | 22 | 1'b0 | Reserved |
| DAC\_TEST\_EN | rw | 23 | 1'b0 | dac test enable dac input comes from register |
| DAC\_TEST | rw | 31:24 | 8'b0 | dac input data value |

### BLEDP\_BLE\_DP\_STATUS1

Offset Address: 0x4000e038

datapath status register 1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SNR\_EST | rw | 7:0 | 8'b0 | snr estimation |
| CNR\_EST | rw | 13:8 | 6'b0 | cnr estimation |
| Reserved | rw | 15:14 | 2'b0 | Reserved |
| AGC\_RSSI | rw | 23:16 | 8'b0 | signal rssi db value. |
| AGC\_RSSI\_READY | rw | 24 | 1'b0 | signal rssi valid. |
| SNR\_VLD | rw | 25 | 1'b0 | snr estimation valid. |
| CNR\_VLD | rw | 26 | 1'b0 | cnr estimation valid. |
| TX\_BUSY | rw | 27 | 1'b0 | tx busy signal. |
| Reserved | rw | 31:28 | 4'b0 | Reserved |

### BLEDP\_BLE\_DP\_STATUS2

Offset Address: 0x4000e03c

datapath status register 2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| VALID\_PCK\_NUM | rw | 15:0 | 16'b0 | received valid packet number. |
| AA\_ERR\_NUM | rw | 21:16 | 6'b0 | access address error number. |
| Reserved | rw | 28:22 | 7'b0 | Reserved |
| CRC\_ERROR | rw | 29 | 1'b0 | indicator of packet crc error. |
| BURST\_DET | rw | 30 | 1'b0 | indicator of burst detection |
| DP\_STATUS\_VLD\_0 | rw | 31 | 1'b0 | data path status valid after access address valid. |

### BLEDP\_BLE\_DP\_STATUS3

Offset Address: 0x4000e040

datapath status register 3

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FD\_CFO\_TRACK | rw | 10:0 | 11'b0 | normalized cfo tracking estimation. |
| Reserved | rw | 15:11 | 5'b0 | Reserved |
| CFO\_EST\_FD | rw | 26:16 | 11'b0 | normalized lp cfo initial estimation. |
| Reserved | rw | 31:27 | 5'b0 | Reserved |

### BLEDP\_BLE\_DP\_STATUS4

Offset Address: 0x4000e044

datapath status register 4

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| RESAMPLER\_PH | rw | 9:0 | 10'b0 | resampler phase. |
| Reserved | rw | 15:10 | 6'b0 | Reserved |
| HP\_CFO | rw | 27:16 | 12'b0 | normalized hp cfo estimation. |
| Reserved | rw | 30:28 | 3'b0 | Reserved |
| HP\_CFO\_VLD | rw | 31 | 1'b0 | hp mode cfo estimation result valid |

### BLEDP\_RX\_FRONT\_END\_CTRL1

Offset Address: 0x4000e048

rx front end control register 1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CFO\_COMP | rw | 14:0 | 15'b0 | \_\_\_\_\_\_cfo user programmed. |
| Reserved | rw | 15 | 1'b0 | Reserved |
| DCNOTCH\_GIN | rw | 17:16 | 2'b0 | dc notch coefficient |
| Reserved | rw | 31:18 | 14'b0 | Reserved |

### BLEDP\_RX\_FRONT\_END\_CTRL2

Offset Address: 0x4000e04c

rx front end control register 2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FAGC\_GAIN | rw | 10:0 | 11'b0 | fine agc gain. |
| FAGC\_INI\_VAL | rw | 11 | 1'b0 | fagc gain initial value |
| CNR\_IDX\_DELTA | rw | 15:12 | 4'b0 | cnr index delta. |
| FAGC\_REF | rw | 23:16 | 8'b0 | fine agc signal reference. |
| CORDIC\_MIN\_VIN\_TH | rw | 27:24 | 4'b0 | cordic input signal min threshold |
| FREQ\_TRADE\_EN | rw | 28 | 1'b0 | enable frequency trade when cordic input signal small than cordic\_min\_vin\_th |
| CHN\_SHIFT | rw | 31:29 | 3'b0 | channel filter shift |

### BLEDP\_FREQ\_DOMAIN\_CTRL1

Offset Address: 0x4000e050

frequency domain control register 1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SYNC\_WORD\_IN0 | rw | 7:0 | 8'b0 | manul sync word [3932] |
| SYNC\_WORD\_WEN | rw | 8 | 1'b0 | when high enable manul sync word |
| Reserved | rw | 14:9 | 6'b0 | Reserved |
| SYNC\_P\_SEL | rw | 15 | 1'b0 | no description available |
| RD\_EXBIT\_EN | rw | 16 | 1'b0 | read extra 8 samples after sync |
| RFAGC\_TRACK\_DLY | rw | 19:17 | 3'b0 | buffer settle threshold from 1us to 127us step is 1us |
| Reserved | rw | 23:20 | 4'b0 | Reserved |
| PROP\_DF\_16US | rw | 31:24 | 8'b0 | prop mode direct found waiting 16 us. |

### BLEDP\_FREQ\_DOMAIN\_CTRL2

Offset Address: 0x4000e054

frequency domain control register 2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SYNC\_WORD\_IN1 | rw | 31:0 | 32'b0 | manul sync word [310] |

### BLEDP\_FREQ\_DOMAIN\_CTRL3

Offset Address: 0x4000e058

frequency domain control register 3

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| XCORR\_PAR\_TH3 | rw | 5:0 | 6'b0 | xcorr trigger par threshold3 |
| Reserved | rw | 7:6 | 2'b0 | Reserved |
| XCORR\_PAR\_TH2 | rw | 13:8 | 6'b0 | xcorr trigger par threshold2 |
| Reserved | rw | 15:14 | 2'b0 | Reserved |
| XCORR\_PAR\_TH1 | rw | 21:16 | 6'b0 | xcorr trigger par threshold1 |
| Reserved | rw | 23:22 | 2'b0 | Reserved |
| XCORR\_PAR\_TH0 | rw | 29:24 | 6'b0 | xcorr trigger par threshold0 |
| Reserved | rw | 31:30 | 2'b0 | Reserved |

### BLEDP\_FREQ\_DOMAIN\_CTRL4

Offset Address: 0x4000e05c

frequency domain control register 4

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| XCORR\_POW\_TH3 | rw | 5:0 | 6'b0 | xcorr power threshold3 |
| Reserved | rw | 7:6 | 2'b0 | Reserved |
| XCORR\_POW\_TH2 | rw | 13:8 | 6'b0 | xcorr power threshold2 |
| Reserved | rw | 15:14 | 2'b0 | Reserved |
| XCORR\_POW\_TH1 | rw | 21:16 | 6'b0 | xcorr power threshold1 |
| Reserved | rw | 23:22 | 2'b0 | Reserved |
| XCORR\_POW\_TH0 | rw | 29:24 | 6'b0 | xcorr power threshold0 |
| Reserved | rw | 31:30 | 2'b0 | Reserved |

### BLEDP\_FREQ\_DOMAIN\_CTRL5

Offset Address: 0x4000e060

frequency domain control register 5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| GAIN\_TED | rw | 1:0 | 2'b0 | ted gain |
| Reserved | rw | 3:2 | 2'b0 | Reserved |
| SYNC\_DIN\_SAT\_VALUE | rw | 6:4 | 3'b0 | &lt;u 1 2&gt;sync din amplitude limit value 0 to 1.75 correspond to 2 to 3.75 |
| SYNC\_DIN\_SAT\_EN | rw | 7 | 1'b0 | sync din amplitude limit enable |
| CNT\_SETTLE\_IDX | rw | 10:8 | 3'b0 | buffer settle threshold from 32 to 256 step is 32 |
| Reserved | rw | 11 | 1'b0 | Reserved |
| TRIG\_XCORR\_CNT | rw | 15:12 | 4'b0 | correlation search window size. |
| XCORR\_RSSI\_TH3 | rw | 19:16 | 4'b0 | xcorr triger rssi threshold0 |
| XCORR\_RSSI\_TH2 | rw | 23:20 | 4'b0 | xcorr triger rssi threshold0 |
| XCORR\_RSSI\_TH1 | rw | 27:24 | 4'b0 | xcorr triger rssi threshold0 |
| XCORR\_RSSI\_TH0 | rw | 31:28 | 4'b0 | xcorr triger rssi threshold0 |

### BLEDP\_FREQ\_DOMAIN\_CTRL6

Offset Address: 0x4000e064

frequency domain control register 5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| HP\_TRAIN\_SIZ | rw | 4:0 | 5'b0 | hp mode training size. |
| Reserved | rw | 7:5 | 3'b0 | Reserved |
| HP\_HIDX\_GAIN | rw | 15:8 | 8'b0 | h index reference gain when hp mode default is 1.0 |
| H\_REF\_GAIN | rw | 21:16 | 6'b0 | h index reference gain when frequency offset track default is 1.0 |
| Reserved | rw | 23:22 | 2'b0 | Reserved |
| DET\_FR\_IDX | rw | 25:24 | 2'b0 | pdu cfo tracking loop gain |
| Reserved | rw | 27:26 | 2'b0 | Reserved |
| CFO\_FR\_IDX | rw | 29:28 | 2'b0 | aa cfo tracking loop gain |
| Reserved | rw | 31:30 | 2'b0 | Reserved |

### BLEDP\_HP\_MODE\_CTRL1

Offset Address: 0x4000e068

when high hp mode training size same as cfo tracking.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| HP\_BMC\_P\_TRACK | rw | 5:0 | 6'b0 | p paramter in search period of frequency offset iir of bmc |
| Reserved | rw | 7:6 | 2'b0 | Reserved |
| HP\_BMC\_P\_TRAIN | rw | 13:8 | 6'b0 | p paramter in training period of frequency offset iir of bmc |
| Reserved | rw | 15:14 | 2'b0 | Reserved |
| HP\_BMC\_CZ1 | rw | 21:16 | 6'b0 | cz1 parameter. |
| Reserved | rw | 23:22 | 2'b0 | Reserved |
| BUF\_IDX\_DELTA | rw | 27:24 | 4'b0 | buffer index delta |
| WMF2\_DSAMP\_IDX | rw | 30:28 | 3'b0 | wmf2 down sampling position -4 to 3 |
| HP\_TRAIN\_SIZ\_FIX | rw | 31 | 1'b0 | when high hp mode training size same as cfo tracking. |

### BLEDP\_HP\_MODE\_CTRL2

Offset Address: 0x4000e06c

q paramter in training period of phase offset iir of bmc

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SNR\_EST\_REF | rw | 7:0 | 8'b0 | signal amplitude used in snr estimation whose unit is db |
| SNR\_EST\_LEN | rw | 9:8 | 2'b0 | symbol number used in snr estimation when pdu length is less than 4 8 32 will be used otherwise the value configured from register will be used |
| Reserved | rw | 11:10 | 2'b0 | Reserved |
| SNR\_EST\_EN | rw | 12 | 1'b0 | snr estimation in time domain enable |
| Reserved | rw | 15:13 | 3'b0 | Reserved |
| HP\_BMC\_Q\_TRACK | rw | 23:16 | 8'b0 | q paramter in search period of phase offset iir of bmc |
| HP\_BMC\_Q\_TRAIN | rw | 31:24 | 8'b0 | q paramter in training period of phase offset iir of bmc |

### BLEDP\_FREQ\_DOMAIN\_STATUS1

Offset Address: 0x4000e070

frequency domain status register 1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MAX\_XCORR | rw | 9:0 | 10'b0 | xcorr\_org value at the max par position |
| Reserved | rw | 15:10 | 6'b0 | Reserved |
| PKT\_OFFSET\_COM | rw | 24:16 | 9'b0 | time from access addres last bit to trigger finish. |
| Reserved | rw | 27:25 | 3'b0 | Reserved |
| NIDX | rw | 31:28 | 4'b0 | noise db buffer index |

### BLEDP\_FREQ\_DOMAIN\_STATUS2

Offset Address: 0x4000e074

frequency domain status register 2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MAX\_PAR\_SPWR | rw | 9:0 | 10'b0 | spwr value at the max par position |
| Reserved | rw | 15:10 | 6'b0 | Reserved |
| MAX\_PAR\_XCORR | rw | 25:16 | 10'b0 | xcorr\*xcorr value at the max par position |
| Reserved | rw | 31:26 | 6'b0 | Reserved |

### BLEDP\_DP\_AA\_ERROR\_CTRL

Offset Address: 0x4000e084

AA error control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| IQSWAP\_SEL | rw | 0 | 1'b0 | when high adc data iq swap with analog iqswap. datapath mixer nco if selection changed with analog iqswap. |
| AA\_ERROR\_EN | rw | 1 | 1'b0 | when high it will reset datapath when aa error. |
| AA\_ERROR\_CNR\_EN | rw | 2 | 1'b0 | when high the aa error reset condition is cnr &gt; threshold and aa error. when low it don care cnr. |
| AA\_ERROR\_CNR\_SEL | rw | 3 | 1'b0 | when high the cnr threshold is 24. when low the cnr threshold is 32. |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### BLEDP\_DP\_INT

Offset Address: 0x4000e088

data path interrupt register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DP\_INTERRUPT0 | rw | 0 | 1'b0 | datapath interrupt0 |
| DP\_INTERRUPT1 | rw | 1 | 1'b0 | datapath interrupt1 |
| DP\_INTERRUPT2 | rw | 2 | 1'b0 | datapath interrupt2 |
| DP\_INTERRUPT | rw | 3 | 1'b0 | datapath interrupt |
| Reserved | rw | 15:4 | 12'b0 | Reserved |
| DP\_INTERRUPT0\_SEL | rw | 19:16 | 4'b0 | datapath interrupt0 selection |
| DP\_INTERRUPT1\_SEL | rw | 23:20 | 4'b0 | datapath interrupt1 selection |
| DP\_INTERRUPT2\_SEL | rw | 27:24 | 4'b0 | datapath interrupt2 selection |
| DP\_INTERRUPT0\_MSK | rw | 28 | 1'b0 | datapath interrupt0 msk |
| DP\_INTERRUPT1\_MSK | rw | 29 | 1'b0 | datapath interrupt1 msk |
| DP\_INTERRUPT2\_MSK | rw | 30 | 1'b0 | datapath interrupt2 msk |
| DP\_INTERRUPT\_MSK | rw | 31 | 1'b0 | datapath interrupt msk |

### BLEDP\_DP\_AA\_ERROR\_TH

Offset Address: 0x4000e08c

AA error threshold register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| HP\_TRAIN\_POSITION | rw | 0 | 1'b0 | when high use the bits just ahead of pdu for rsve training. when low the training bit starts at the track bits. |
| CORDIC\_IN\_SCALE | rw | 1 | 1'b0 | when high cordic input will be auto scaled(shift) according to the magnitude of real/imag data. |
| PAR\_AUTO\_HIGHER\_SEL | rw | 2 | 1'b0 | when high par auto higher 1/4 when low par auto higher 1/8 it will work together with par\_auto\_higher\_en and rssi\_good\_dbm. |
| PAR\_AUTO\_HIGHER\_EN | rw | 3 | 1'b0 | when high when signal is good ( rssi large than rssi\_good\_dbm) it will auto higher the par threshold. |
| SNR\_GOOD\_TH | rw | 6:4 | 3'b0 | threshold for snr(fd mode calculated use aa) to reset datapath cooperate with cnr snr and aa error. |
| Reserved | rw | 7 | 1'b0 | Reserved |
| CNR\_GOOD\_TH | rw | 13:8 | 6'b0 | threshold for cnr to reset datapath cooperate with cnr snr and aa error. |
| Reserved | rw | 15:14 | 2'b0 | Reserved |
| RSSI\_GOOD\_TH | rw | 23:16 | 8'b0 | threshold for rssi to reset datapath cooperate with cnr snr and aa error. |
| RSSI\_GOOD\_DBM | rw | 31:24 | 8'b0 | when rssi dbm large than the -rssi\_good\_dbm the signal is good enough to higher the par threshold if the function enable. |

### BLEDP\_DF\_ANTENNA\_CTRL

Offset Address: 0x4000e090

antenna register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SWITCH\_MAP\_SEL\_8F | rw | 1:0 | 2'b0 | switch antenna map selection 8 to f |
| SWITCH\_MAP\_SEL\_07 | rw | 3:2 | 2'b0 | switch antenna map selection 0 to 7 |
| EXT\_ANTENNA\_NUM | rw | 7:4 | 4'b0 | user programmed switch antenna number |
| EXT\_ANTENNA\_NUM\_WEN | rw | 8 | 1'b0 | user programmed switch antenna enable |
| Reserved | rw | 15:9 | 7'b0 | Reserved |
| BUFFER\_BP | rw | 16 | 1'b0 | when high, bypass buffer, and not write/read buffer for datapath power test |
| TEST\_TD\_POWER | rw | 17 | 1'b0 | when high, test rfe,td detector power, other module don't work, the cordic work or not decided by resampler\_bp |
| TEST\_FD\_POWER | rw | 18 | 1'b0 | when high, test rfe, cordic and fd detector power, other module don't work |
| TEST\_SYNC\_POWER | rw | 19 | 1'b0 | when high, test rfe. Cordic and sync power. Other module don't work |
| TEST\_RFE\_CORDIC\_POWER | rw | 20 | 1'b0 | when high, test rfe and cordic power, other module don't work |
| TEST\_RFE\_POWER | rw | 21 | 1'b0 | when high, test rfe power, other module don't work |
| ADC01\_SAMPLE\_TIME | rw | 22 | 1'b0 | when high, will exchange the adc0/adc1 sample time, to avoid the error sample time for adc0/adc1 |
| PHY\_RATE\_MUX | rw | 23 | 1'b0 | ble data rate used in datapath, 0: 1mbps 1: 2mbps |
| PHY\_RATE\_REG | rw | 24 | 1'b0 | user programmed phy data rate |
| PHY\_RATE\_WEN | rw | 25 | 1'b0 | 0: phy rate comes from ble ip 1:phy rate comes from regsiter phy\_rate\_reg |
| PDU\_RSSI\_WAIT\_TIME | rw | 26 | 1'b0 | 0:wait 0us 1: wait 4us |
| PDU\_RSSI\_WIN\_LEN | rw | 27 | 1'b0 | select estimation length for pdu rssi calculate |
| CAL\_PDU\_RSSI\_EN | rw | 28 | 1'b0 | calculate rssi use pdu data enbale. |
| PROP\_CRC\_AA\_DIS | rw | 29 | 1'b0 | prop mode crc check disable check access address. |
| PROP\_AA\_LSB\_FIRST | rw | 30 | 1'b0 | prop mode access address lsb first for cbt test. |
| PRE\_NUM\_WEN | rw | 31 | 1'b0 | preamble number write enable |

### BLEDP\_ANTENNA\_MAP01

Offset Address: 0x4000e094

antenna switch map register 0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SWITCH\_MAP\_1 | rw | 13:0 | 14'b0 | switch antenna map 1 |
| Reserved | rw | 15:14 | 2'b0 | Reserved |
| SWITCH\_MAP\_0 | rw | 29:16 | 14'b0 | switch antenna map 0 |
| Reserved | rw | 31:30 | 2'b0 | Reserved |

### BLEDP\_ANTENNA\_MAP23

Offset Address: 0x4000e098

antenna switch map register 1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SWITCH\_MAP\_3 | rw | 13:0 | 14'b0 | switch antenna map 3 |
| Reserved | rw | 15:14 | 2'b0 | Reserved |
| SWITCH\_MAP\_2 | rw | 29:16 | 14'b0 | switch antenna map 2 |
| Reserved | rw | 31:30 | 2'b0 | Reserved |

### BLEDP\_ANTENNA\_MAP45

Offset Address: 0x4000e09c

antenna switch map register 2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SWITCH\_MAP\_5 | rw | 13:0 | 14'b0 | switch antenna map 5 |
| Reserved | rw | 15:14 | 2'b0 | Reserved |
| SWITCH\_MAP\_4 | rw | 29:16 | 14'b0 | switch antenna map 4 |
| Reserved | rw | 31:30 | 2'b0 | Reserved |

### BLEDP\_ANTENNA\_MAP67

Offset Address: 0x4000e0a0

antenna switch map register 3

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SWITCH\_MAP\_7 | rw | 13:0 | 14'b0 | switch antenna map 7 |
| Reserved | rw | 15:14 | 2'b0 | Reserved |
| SWITCH\_MAP\_6 | rw | 29:16 | 14'b0 | switch antenna map 6 |
| Reserved | rw | 31:30 | 2'b0 | Reserved |

### CALIB\_START

Offset Address: 0x4000f000

calibration start register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PO\_CLB\_START | rw | 0 | 1'b0 | Power on calibration start |
| HOP\_CLB\_START | rw | 1 | 1'b0 | Frequency hop calibration start |
| OSC\_CLB\_START | rw | 2 | 1'b0 | OSC calibration start |
| REF\_CLB\_START | rw | 3 | 1'b0 | REF PLL calibration start |
| RCO\_CLB\_START | rw | 4 | 1'b0 | RCO calibration start |
| XTL\_CLB\_START | rw | 5 | 1'b0 | XTAL calibration start |
| Reserved | rw | 31:6 | 26'b0 | Reserved |

### CALIB\_STATUS

Offset Address: 0x4000f004

calibration FSM status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TOP\_FSM | rw | 4:0 | 5'b0 | TOP FSM |
| DC\_FSM | rw | 8:5 | 4'b0 | DC FSM |
| VCOA\_FSM | rw | 11:9 | 3'b0 | VCOA FSM |
| VCOF\_FSM | rw | 16:12 | 5'b0 | VCOF FSM |
| KVCO\_FSM | rw | 20:17 | 4'b0 | KVCO FSM |
| RCO\_FSM | rw | 23:21 | 3'b0 | RCO FSM |
| OSC\_FSM | rw | 26:24 | 3'b0 | OSC FSM |
| REF\_FSM | rw | 29:27 | 3'b0 | REF FSM |
| Reserved | rw | 31:30 | 2'b0 | Reserved |

### CALIB\_DC\_CODE

Offset Address: 0x4000f008

DC code status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PPF\_DCCAL2\_I | rw | 3:0 | 4'b0 | Power on DC calibration i code |
| PPF\_DCCAL2\_Q | rw | 7:4 | 4'b0 | Power on DC calibration q code |
| Reserved | rw | 15:8 | 8'b0 | Reserved |
| PPF\_DCCAL\_I | rw | 21:16 | 6'b0 | DC re-calibration i code |
| Reserved | rw | 23:22 | 2'b0 | Reserved |
| PPF\_DCCAL\_Q | rw | 29:24 | 6'b0 | DC re-calibration q code |
| Reserved | rw | 31:30 | 2'b0 | Reserved |

### CALIB\_DC\_CFG

Offset Address: 0x4000f00c

DC code configured code register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PPF\_DCCAL2\_CFG\_I | rw | 3:0 | 4'b0 | Power on DC calibration i code configured |
| PPF\_DCCAL2\_CFG\_Q | rw | 7:4 | 4'b0 | Power on DC calibration q code configured |
| DC\_2NDCAL\_DIS | rw | 8 | 1'b0 | DC calibration disable |
| DC\_2NDCAL\_REQ | rw | 9 | 1'b0 | DC calibration request |
| Reserved | rw | 15:10 | 6'b0 | Reserved |
| PPF\_DCCAL\_CFG\_I | rw | 21:16 | 6'b0 | DC re-calibration i code configured |
| DC\_HOP\_CAL\_BP | rw | 22 | 1'b0 | DC hop calibration bypass |
| Reserved | rw | 23 | 1'b0 | Reserved |
| PPF\_DCCAL\_CFG\_Q | rw | 29:24 | 6'b0 | DC re-calibration q code configured |
| DC\_1STCAL\_DIS | rw | 30 | 1'b0 | DC hop calibration disable |
| DC\_1STCAL\_REQ | rw | 31 | 1'b0 | DC hop calibration request |

### CALIB\_RCO\_RC\_REF\_OSC\_CODE

Offset Address: 0x4000f010

RCO RC PLL48M OSC code status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CAU\_RCO\_CAP | rw | 3:0 | 4'b0 | RCO calibration output code |
| Reserved | rw | 7:4 | 4'b0 | Reserved |
| CAU\_OSC\_CUR | rw | 12:8 | 5'b0 | OSC calibration output code |
| Reserved | rw | 15:13 | 3'b0 | Reserved |
| CAU\_RC\_CAL\_OUT2REG | rw | 19:16 | 4'b0 | RC calibration output code |
| Reserved | rw | 23:20 | 4'b0 | Reserved |
| PLL48\_ENREF | rw | 27:24 | 4'b0 | REF calibration output code |
| Reserved | rw | 31:28 | 4'b0 | Reserved |

### CALIB\_RCO\_RC\_REF\_OSC\_CFG

Offset Address: 0x4000f014

RCO RC PLL48M OSC configured code register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CAU\_RCO\_CAP\_CFG | rw | 3:0 | 4'b0 | RCO calibration code configured |
| RCO\_CAL\_DIS | rw | 4 | 1'b0 | RCO calibration disable |
| RCO\_CAL\_REQ | rw | 5 | 1'b0 | RCO calibration request |
| Reserved | rw | 7:6 | 2'b0 | Reserved |
| CAU\_OSC\_CUR\_CFG | rw | 12:8 | 5'b0 | OSC calibration output code configured |
| OSC\_CAL\_DIS | rw | 13 | 1'b0 | OSC calibration disable |
| OSC\_CAL\_REQ | rw | 14 | 1'b0 | OSC calibration request |
| Reserved | rw | 15 | 1'b0 | Reserved |
| CAU\_RC\_CAL\_REG\_IN | rw | 19:16 | 4'b0 | RC calibration code to analog |
| CAU\_RC\_CAL\_DIS | rw | 20 | 1'b0 | RC calibration disable |
| RC\_CAL\_REQ | rw | 21 | 1'b0 | RC calibration request |
| Reserved | rw | 23:22 | 2'b0 | Reserved |
| PLL48\_ENREF\_CFG | rw | 27:24 | 4'b0 | REF calibration output code configured |
| REF\_CAL\_DIS | rw | 28 | 1'b0 | REF PLL calibration disable |
| REF\_CAL\_REQ | rw | 29 | 1'b0 | REF PLL calibration request |
| Reserved | rw | 31:30 | 2'b0 | Reserved |

### CALIB\_VCOA\_KVCO2M\_CODE

Offset Address: 0x4000f018

reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| KCALF2M\_PO | rw | 10:0 | 11'b0 | KVCO 2M mode calibration power on code |
| Reserved | rw | 15:11 | 5'b0 | Reserved |
| TX\_VCO\_AMP | rw | 20:16 | 5'b0 | VCO TX amplitude calibration output code |
| Reserved | rw | 23:21 | 3'b0 | Reserved |
| RX\_VCO\_AMP | rw | 28:24 | 5'b0 | VCO RX amplitude calibration output code |
| Reserved | rw | 31:29 | 3'b0 | Reserved |

### CALIB\_VCOA\_KVCO2M\_CFG

Offset Address: 0x4000f01c

reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| KCALF2M\_CFG | rw | 10:0 | 11'b0 | KVCO 2M mode calibration code configure |
| KCALF2M\_BP | rw | 11 | 1'b0 | bypass KVCO 2M mode power on calibration |
| KVCO\_CAL\_E | rw | 14:12 | 3'b0 | no description available |
| Reserved | rw | 15 | 1'b0 | Reserved |
| TX\_VCO\_AMP\_CFG | rw | 20:16 | 5'b0 | TX VCO amplitude calibration output code configured |
| VCOA\_CAL\_DIS | rw | 21 | 1'b0 | VCO amplitude calibration disable |
| VCOA\_CAL\_REQ | rw | 22 | 1'b0 | VCO amplitude calibration request |
| Reserved | rw | 23 | 1'b0 | Reserved |
| RX\_VCO\_AMP\_CFG | rw | 28:24 | 5'b0 | RX VCO amplitude calibration output code configured |
| Reserved | rw | 31:29 | 3'b0 | Reserved |

### CALIB\_VCOF\_KVCO\_PO\_CODE

Offset Address: 0x4000f020

reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| KCALF\_PO | rw | 10:0 | 11'b0 | KVCO power up calibration result |
| Reserved | rw | 15:11 | 5'b0 | Reserved |
| TX\_VCO\_CBANK\_PO | rw | 21:16 | 6'b0 | TX VCO frequency power on calibration output code |
| Reserved | rw | 23:22 | 2'b0 | Reserved |
| RX\_VCO\_CBANK\_PO | rw | 29:24 | 6'b0 | RX VCO frequency power on calibration output code |
| Reserved | rw | 31:30 | 2'b0 | Reserved |

### CALIB\_VCOF\_KVCO\_CFG

Offset Address: 0x4000f024

VCOF hop calibration bypass

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| KCALF\_CFG | rw | 10:0 | 11'b0 | KVCO calibration code configure |
| KVCO\_REQ | rw | 11 | 1'b0 | KVCO calibration request |
| KVCO\_DIS | rw | 12 | 1'b0 | KVCO calibration disable |
| KVCO\_SKIP | rw | 13 | 1'b0 | KVCO hop calibration calculation skip |
| Reserved | rw | 15:14 | 2'b0 | Reserved |
| TX\_VCO\_CBANK\_CFG | rw | 21:16 | 6'b0 | TX VCO frequency calibration output code configured |
| VCOF\_CAL\_DIS | rw | 22 | 1'b0 | VCO frequency calibration disable |
| VCOF\_CAL\_REQ | rw | 23 | 1'b0 | VCO frequency calibration request |
| RX\_VCO\_CBANK\_CFG | rw | 29:24 | 6'b0 | RX VCO frequency calibration output code configured |
| VCOF\_SKIP | rw | 30 | 1'b0 | VCOF hop calibration calculation skip |
| VCOF\_HOP\_BP | rw | 31 | 1'b0 | VCOF hop calibration bypass |

### CALIB\_VCOF\_KVCO\_CODE

Offset Address: 0x4000f028

reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| KCALF | rw | 10:0 | 11'b0 | KVCO calibration output at carrier frequency |
| Reserved | rw | 15:11 | 5'b0 | Reserved |
| TX\_VCO\_CBANK | rw | 21:16 | 6'b0 | TX VCO frequency calibration output code |
| Reserved | rw | 23:22 | 2'b0 | Reserved |
| RX\_VCO\_CBANK | rw | 29:24 | 6'b0 | RX VCO frequency calibration output code |
| Reserved | rw | 31:30 | 2'b0 | Reserved |

### CALIB\_KVCO\_HOP\_CODE

Offset Address: 0x4000f02c

reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| KCALF1M | rw | 10:0 | 11'b0 | KVCO hop calibration output at carrier frequency in 1M mode |
| Reserved | rw | 15:11 | 5'b0 | Reserved |
| KCALF2M | rw | 26:16 | 11'b0 | KVCO hop calibration output at carrier frequency in 2M mode |
| Reserved | rw | 31:27 | 5'b0 | Reserved |

### CALIB\_VCOF\_CNT\_SLOPE

Offset Address: 0x4000f030

reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TX\_VCOF\_CNT | rw | 7:0 | 8'b0 | TX VCO frequency power up calibration 8us count value |
| TX\_SLOPE | rw | 13:8 | 6'b0 | TX frequency curve slope |
| Reserved | rw | 15:14 | 2'b0 | Reserved |
| RX\_VCOF\_CNT | rw | 23:16 | 8'b0 | RX VCO frequency power up calibration 8us count value |
| RX\_SLOPE | rw | 29:24 | 6'b0 | RX frequency curve slope |
| Reserved | rw | 31:30 | 2'b0 | Reserved |

### CALIB\_XTL\_CODE

Offset Address: 0x4000f034

Reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| XTL\_XICTRL\_CODE | rw | 5:0 | 6'b0 | crystal calibration code |
| Reserved | rw | 7:6 | 2'b0 | Reserved |
| XTL\_AMP\_DET\_OUT | rw | 8 | 1'b0 | crystal comparator output result |
| Reserved | rw | 31:9 | 23'b0 | Reserved |

### CALIB\_XTL\_CFG

Offset Address: 0x4000f038

Reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| XTL\_XICTRL\_CFG | rw | 5:0 | 6'b0 | crystal calibration CFG |
| XTL\_CAL\_DIS | rw | 6 | 1'b0 | crystal code disable |
| XTL\_CAL\_REQ | rw | 7 | 1'b0 | crystal calibration request |
| Reserved | rw | 31:8 | 24'b0 | Reserved |

### CALIB\_CAL\_DLY

Offset Address: 0x4000f03c

hop calibration delay bypass

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| HOP\_DLY | rw | 5:0 | 6'b0 | hop calibration delay time |
| Reserved | rw | 6 | 1'b0 | Reserved |
| HOP\_DLY\_BP | rw | 7 | 1'b0 | hop calibration delay bypass |
| TX\_DLY\_DIG1M | rw | 9:8 | 2'b0 | no description available |
| TX\_DLY\_DIG2M | rw | 11:10 | 2'b0 | no description available |
| TX\_DLY\_DAC\_1M | rw | 13:12 | 2'b0 | no description available |
| TX\_DLY\_DAC\_2M | rw | 15:14 | 2'b0 | no description available |
| RX\_PWRUP\_CNT\_TH1M | rw | 23:16 | 8'b0 | no description available |
| RX\_PWRUP\_CNT\_TH2M | rw | 31:24 | 8'b0 | no description available |

### CALIB\_DONE

Offset Address: 0x4000f040

Reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 1:0 | 2'b0 | Reserved |
| OSC\_CAL\_DONE | rw | 2 | 1'b0 | OSC calibration done |
| REF\_CAL\_DONE | rw | 3 | 1'b0 | REF PLL calibration done |
| RCO\_CAL\_DONE | rw | 4 | 1'b0 | RCO calibration done |
| RC\_CAL\_DONE | rw | 5 | 1'b0 | RC calibration done |
| VCOF\_CAL\_DONE | rw | 6 | 1'b0 | VCO frequency calibration done |
| VCOA\_CAL\_DONE | rw | 7 | 1'b0 | VCO amplitude calibration done |
| DC2ND\_CAL\_DONE | rw | 8 | 1'b0 | DC 2nd stage calibration done |
| DC1ST\_CAL\_DONE | rw | 9 | 1'b0 | DC 1st stage calibration done |
| XTL\_CAL\_DONE | rw | 10 | 1'b0 | XTL calibration done |
| KVCO\_CAL\_DONE | rw | 11 | 1'b0 | KVCO calibration done |
| KVCO\_HOP\_DONE | rw | 12 | 1'b0 | KVCO calibration done |
| Reserved | rw | 31:13 | 19'b0 | Reserved |

### CALIB\_RRF1

Offset Address: 0x4000f400

Amplitude of LO buffer for active mixer

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| RRF\_INCAP2 | rw | 2:0 | 3'b0 | LNA input LC cap bank |
| RRF\_LOAD\_CAP | rw | 6:3 | 4'b0 | LNA load LC cap bank |
| RRF\_TX\_INCAP1 | rw | 9:7 | 3'b0 | LNA&amp;PA matching cap bank |
| RRF\_RX\_INCAP1 | rw | 12:10 | 3'b0 | LNA&amp;PA matching cap bank |
| RRF\_VGATE11\_LNA | rw | 15:13 | 3'b0 | LNA vrega voltage |
| RRF\_BM\_GM | rw | 17:16 | 2'b0 | Constant gm current control |
| RRF\_BM\_LNA | rw | 19:18 | 2'b0 | LNA bias current control- |
| RRF\_BM\_MIXER | rw | 21:20 | 2'b0 | Mixer current bias |
| PPF\_DCCAL\_RES | rw | 23:22 | 2'b0 | Input res selection of ppf for dccal |
| RRF\_CAL\_MIX\_EN | rw | 24 | 1'b0 | no description available |
| RRF\_CAL\_MIX1\_EN | rw | 25 | 1'b0 | no description available |
| RRF\_LO\_SEL\_P | rw | 27:26 | 2'b0 | Dc voltage bias control for the pmos switch of active mixer |
| RRF\_LO\_SEL\_N | rw | 29:28 | 2'b0 | Dc voltage bias control for the nmos switch of active mixer |
| RRF\_LO\_AMP | rw | 31:30 | 2'b0 | Amplitude of LO buffer for active mixer |

### CALIB\_PLL48\_PPF

Offset Address: 0x4000f404

reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PPF\_BM | rw | 1:0 | 2'b0 | Ppf current control- |
| PPF\_IQSW | rw | 2 | 1'b0 | no description available |
| PLL48\_DIFF\_CLK\_48M\_DIS | rw | 3 | 1'b0 | no description available |
| PLL48\_TST\_CPREF | rw | 7:4 | 4'b0 | CP current selecting |
| Reserved | rw | 31:8 | 24'b0 | Reserved |

### CALIB\_LO0

Offset Address: 0x4000f408

reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| VCO\_DAC\_IPTAT | rw | 3:0 | 4'b0 | Set the temperature characteristic of TX DAC in order to compensate the modulation gain error of the VCO |
| VCO\_TST\_CP | rw | 7:4 | 4'b0 | LO CP current control- |
| VCO\_VTUN\_SET | rw | 12:8 | 5'b0 | Set VTUNE voltage change in order to properly compensate the VUNE error introduced by charge injection when the PLL loop is broken;VTUNE change introduced by this register is around 50uV\*(VTUNE\_SET-16) |
| VCO\_ACAL\_SET | rw | 15:13 | 3'b0 | Set the threshold (differential peak) in VCO amplitude calibration-VTH=0.2+0.05\*ACAL\_SET |
| VCO\_BM\_TXFIL | rw | 17:16 | 2'b0 | Set the bias current of the TX filter |
| VCO\_BM\_TXDAC | rw | 19:18 | 2'b0 | Set the bias current of the TX DAC |
| Reserved | rw | 22:20 | 3'b0 | Reserved |
| VCO\_SAMP\_EN | rw | 23 | 1'b0 | no description available |
| VCO\_CAP\_HALF\_EN | rw | 24 | 1'b0 | no description available |
| VCO\_SET\_VCO\_VDD\_LOW | rw | 25 | 1'b0 | no description available |
| VCO\_8OR16M\_INV\_EN | rw | 26 | 1'b0 | no description available |
| VCO\_DIV\_PD\_EN | rw | 27 | 1'b0 | no description available |
| VCO\_TXDLY1M | rw | 28 | 1'b0 | no description available |
| VCO\_TXDLY2M | rw | 29 | 1'b0 | no description available |
| VCO\_RX\_CK\_TST | rw | 30 | 1'b0 | no description available |
| VCO\_DSM\_INT\_EN | rw | 31 | 1'b0 | no description available |

### CALIB\_LO1

Offset Address: 0x4000f40c

Reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SPEED\_UP\_TIME | rw | 4:0 | 5'b0 | LO speed up time |
| SW\_LO\_SPEED\_UP | rw | 5 | 1'b0 | software LO speed up |
| RX\_PLLPFD\_EN | rw | 6 | 1'b0 | PLL pfd enable in RX mode |
| TX\_PLLPFD\_EN | rw | 7 | 1'b0 | PLL pfd enable in TX mode |
| LO\_SET\_TIME | rw | 13:8 | 6'b0 | LO settle time |
| MOD\_TEST | rw | 14 | 1'b0 | LO open loop or close loop select |
| DIV\_DIFF\_CLK\_LO\_DIS | rw | 15 | 1'b0 | no description available |
| TX\_VCO\_FTC\_SET | rw | 17:16 | 2'b0 | no description available |
| RX\_VCO\_FTC\_SET | rw | 19:18 | 2'b0 | no description available |
| Reserved | rw | 31:20 | 12'b0 | Reserved |

### CALIB\_PA\_CTRL

Offset Address: 0x4000f410

Reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PA\_ON\_DLY | rw | 5:0 | 6'b0 | PA turn on delay time |
| Reserved | rw | 7:6 | 2'b0 | Reserved |
| PA\_OFF\_DLY | rw | 11:8 | 4'b0 | PA turn off delay time |
| Reserved | rw | 15:12 | 4'b0 | Reserved |
| PA\_INCREASE\_SEL | rw | 18:16 | 3'b0 | PA output power increasing control |
| PA\_SEL\_BIAS | rw | 19 | 1'b0 | PA duty cycle voltage bias |
| PA\_BM\_CUR | rw | 21:20 | 2'b0 | Pa bias current control |
| PA\_VDUTY\_CYCLE\_SEL | rw | 23:22 | 2'b0 | PA duty cycle control voltage select |
| PA\_VCDCG | rw | 24 | 1'b0 | PA duty cycle control |
| Reserved | rw | 31:25 | 7'b0 | Reserved |

### CALIB\_CTRL

Offset Address: 0x4000f800

Reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| RC\_TIM | rw | 1:0 | 2'b0 | RC calibration reset time |
| Reserved | rw | 3:2 | 2'b0 | Reserved |
| VCO\_TEST\_INT | rw | 4 | 1'b0 | no description available |
| Reserved | rw | 7:5 | 3'b0 | Reserved |
| HOP\_CLB\_SEL | rw | 8 | 1'b0 | Frequency hop calibration start select |
| Reserved | rw | 15:9 | 7'b0 | Reserved |
| XTL\_PO\_TIM | rw | 17:16 | 2'b0 | crystal calibration power on wait time |
| XTL\_CAL\_TIM | rw | 19:18 | 2'b0 | crystal calibration code wait time |
| XTL\_AMP\_DET\_PWR\_SEL | rw | 21:20 | 2'b0 | crystal amplitude detector power select |
| XTL\_SWCAL\_EN | rw | 22 | 1'b0 | crystal software calibration enable |
| Reserved | rw | 31:23 | 9'b0 | Reserved |

### CALIB\_INT\_RAW

Offset Address: 0x4000f804

Reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PO\_CAL\_DONE\_INT | rw | 0 | 1'b0 | power on calibration done interrupt |
| HOP\_CAL\_DONE\_INT | rw | 1 | 1'b0 | hop calibration done interrupt |
| OSC\_CAL\_DONE\_INT | rw | 2 | 1'b0 | OSC calibration done interrupt |
| REF\_CAL\_DONE\_INT | rw | 3 | 1'b0 | REF PLL calibration done interrupt |
| RCO\_CAL\_DONE\_INT | rw | 4 | 1'b0 | RCO calibration done interrupt |
| XTL\_CAL\_DONE\_INT | rw | 5 | 1'b0 | XTL calibration done interrupt |
| Reserved | rw | 7:6 | 2'b0 | Reserved |
| PO\_ALL\_DONE\_INT | rw | 8 | 1'b0 | RCO &amp; REF &amp; OSC &amp; Power on calibration all done interrupt. And signal of above interrupt |
| Reserved | rw | 15:9 | 7'b0 | Reserved |
| CAL\_INT | rw | 16 | 1'b0 | or signal of all calibration interrupt |
| Reserved | rw | 31:17 | 15'b0 | Reserved |

### CALIB\_INTEN

Offset Address: 0x4000f808

Reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PO\_CAL\_DONE\_INTEN | rw | 0 | 1'b0 | power on calibration done interrupt enable |
| HOP\_CAL\_DONE\_INTEN | rw | 1 | 1'b0 | hop calibration done interrupt enable |
| OSC\_CAL\_DONE\_INTEN | rw | 2 | 1'b0 | OSC calibration done interrupt enable |
| REF\_CAL\_DONE\_INTEN | rw | 3 | 1'b0 | REF PLL calibration done interrupt enable |
| RCO\_CAL\_DONE\_INTEN | rw | 4 | 1'b0 | RCO calibration done interrupt enable |
| XTL\_CAL\_DONE\_INTEN | rw | 5 | 1'b0 | XTL calibration done interrupt enable |
| Reserved | rw | 7:6 | 2'b0 | Reserved |
| PO\_ALL\_DONE\_INTEN | rw | 8 | 1'b0 | PO\_ALL\_DONE\_INT enable |
| Reserved | rw | 31:9 | 23'b0 | Reserved |

### CALIB\_INT\_STAT

Offset Address: 0x4000f80c

Reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PO\_CAL\_DONE\_INT\_STAT | rw | 0 | 1'b0 | power on calibration done interrupt status |
| HOP\_CAL\_DONE\_INT\_STAT | rw | 1 | 1'b0 | hop calibration done interrupt status |
| OSC\_CAL\_DONE\_INT\_STAT | rw | 2 | 1'b0 | OSC calibration done interrupt status |
| REF\_CAL\_DONE\_INT\_STAT | rw | 3 | 1'b0 | REF PLL calibration done interrupt status |
| RCO\_CAL\_DONE\_INT\_STAT | rw | 4 | 1'b0 | RCO calibration done interrupt status |
| XTL\_CAL\_DONE\_INT\_STAT | rw | 5 | 1'b0 | XTL calibration done interrupt status |
| Reserved | rw | 7:6 | 2'b0 | Reserved |
| PO\_ALL\_DONE\_INT\_STAT | rw | 8 | 1'b0 | PO\_ALL\_DONE\_INT status |
| Reserved | rw | 15:9 | 7'b0 | Reserved |
| CAL\_INT\_STAT | rw | 16 | 1'b0 | calibration all interrupt status |
| Reserved | rw | 31:17 | 15'b0 | Reserved |

### CALIB\_TIF

Offset Address: 0x4000f810

reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TEST\_CTRL | rw | 3:0 | 4'b0 | Test interface selection |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### CALIB\_KVCO\_MEAN

Offset Address: 0x4000f814

reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| KVCO\_CNT\_MEAN | rw | 20:0 | 21'b0 | KVCO counter 1 and counter 2 mean |
| Reserved | rw | 31:21 | 11'b0 | Reserved |

### CALIB\_KVCO\_DLT

Offset Address: 0x4000f818

reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| KVCO\_CNT\_DLT | rw | 8:0 | 9'b0 | KVCO counter 1 and counter 2 delta |
| Reserved | rw | 31:9 | 23'b0 | Reserved |

### CALIB\_LO\_CFG

Offset Address: 0x4000f81c

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| LO\_INT\_CFG | rw | 5:0 | 6'b0 | no description available |
| LO\_FRAC\_CFG | rw | 27:6 | 22'b0 | no description available |
| Reserved | rw | 29:28 | 2'b0 | Reserved |
| LO\_SEL | rw | 30 | 1'b0 | no description available |
| LO\_CHANGE | rw | 31 | 1'b0 | no description available |

### CALIB\_LO\_TABLE

Offset Address: 0x4000f820

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| LO\_INT\_TABLE | rw | 5:0 | 6'b0 | no description available |
| LO\_FRAC\_TABLE | rw | 25:6 | 20'b0 | no description available |
| Reserved | rw | 31:26 | 6'b0 | Reserved |

### CALIB\_LO\_RATIO

Offset Address: 0x4000f824

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| LO\_INT | rw | 5:0 | 6'b0 | no description available |
| LO\_FRAC | rw | 27:6 | 22'b0 | no description available |
| Reserved | rw | 31:28 | 4'b0 | Reserved |

### CALIB\_VCO\_MOD\_CFG

Offset Address: 0x4000f828

TRX 2M mode selection signal

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| VCO\_MOD\_TX\_CFG | rw | 0 | 1'b0 | VCO\_MOD\_TX register configured value. See section 6.10.5 for detail. |
| VCO\_MOD\_TX\_SEL | rw | 1 | 1'b0 | VCO\_MOD\_TX selection |
| TRX2M\_MODE\_CFG | rw | 2 | 1'b0 | TRX 2M mode software configured value |
| TRX2M\_MODE\_SEL | rw | 3 | 1'b0 | TRX 2M mode selection signal |
| IMR | rw | 4 | 1'b0 | no description available |
| Reserved | rw | 31:5 | 27'b0 | Reserved |

### CALIB\_VCO\_MOD\_STAT

Offset Address: 0x4000f82c

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| VCO\_MOD\_TX | rw | 0 | 1'b0 | no description available |
| Reserved | rw | 1 | 1'b0 | Reserved |
| TRX2M\_MODE | rw | 2 | 1'b0 | no description available |
| Reserved | rw | 31:3 | 29'b0 | Reserved |

### CALIB\_CH\_IDX

Offset Address: 0x4000f830

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CH\_IDX | rw | 7:0 | 8'b0 | no description available |
| Reserved | rw | 31:8 | 24'b0 | Reserved |

### CALIB\_VCOF\_CNT\_UP

Offset Address: 0x4000f834

reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TX\_VCOF\_CNT\_UP | rw | 7:0 | 8'b0 | TX VCO frequency power up calibration 8us count value |
| Reserved | rw | 15:8 | 8'b0 | Reserved |
| RX\_VCOF\_CNT\_UP | rw | 23:16 | 8'b0 | RX VCO frequency power up calibration 8us count value |
| Reserved | rw | 31:24 | 8'b0 | Reserved |

### CALIB\_VCOF\_CNT\_DN

Offset Address: 0x4000f838

reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TX\_VCOF\_CNT\_DN | rw | 7:0 | 8'b0 | TX VCO frequency power up calibration 8us count value |
| Reserved | rw | 15:8 | 8'b0 | Reserved |
| RX\_VCOF\_CNT\_DN | rw | 23:16 | 8'b0 | RX VCO frequency power up calibration 8us count value |
| Reserved | rw | 31:24 | 8'b0 | Reserved |

### SPIFI0\_CTRL

Offset Address: 0x40080000

SPIFI control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TIMEOUT | rw | 15:0 | 16'b0 | This field contains the number of serial clock periods without the processor reading data in memory mode, which will cause the SPIFI hardware to terminate the command by driving the CS pin high and negating the CMD bit in the Status register. (This allows the flash memory to enter a lower-power state.) If the processor reads data from the flash region after a time-out, the command in the Memory Command Register is issued again. |
| CSHIGH | rw | 19:16 | 4'b0 | This field controls the minimum CS high time, expressed as a number of serial clock periods minus one. |
| Reserved | rw | 20 | 1'b0 | Reserved |
| D\_PRFTCH\_DIS | rw | 21 | 1'b0 | This bit allows conditioning of memory mode prefetches based on the AHB HPROT (instruction/data) access information. A 1 in this register means that the SPIFI will not attempt a speculative prefetch when it encounters data accesses. |
| INTEN | rw | 22 | 1'b0 | If this bit is 1 when a command ends, the SPIFI will assert its interrupt request output. See INTRQ in the status register for further details. |
| MODE3 | rw | 23 | 1'b0 | SPI Mode 3 select. |
| Reserved | rw | 26:24 | 3'b0 | Reserved |
| PRFTCH\_DIS | rw | 27 | 1'b0 | Cache prefetching enable. The SPIFI includes an internal cache. A 1 in this bit disables prefetching of cache lines. |
| DUAL | rw | 28 | 1'b0 | Select dual protocol. |
| RFCLK | rw | 29 | 1'b0 | Select active clock edge for input data. |
| FBCLK | rw | 30 | 1'b0 | Feedback clock select. |
| DMAEN | rw | 31 | 1'b0 | A 1 in this bit enables the DMA Request output from the SPIFI. Set this bit only when a DMA channel is used to transfer data in peripheral mode. Do not set this bit when a DMA channel is used for memory-to-memory transfers from the SPIFI memory area. DMAEN should only be used in Command mode. |

### SPIFI0\_CMD

Offset Address: 0x40080004

SPIFI command register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DATALEN | rw | 13:0 | 14'b0 | Except when the POLL bit in this register is 1, this field controls how many data bytes are in the command. 0 indicates that the command does not contain a data field. |
| POLL | rw | 14 | 1'b0 | This bit should be written as 1 only with an opcode that a) contains an input data field, and b) causes the serial flash device to return byte status repetitively (e.g., a Read Status command). When this bit is 1, the SPIFI hardware continues to read bytes until the test specified by the DATALEN field is met. The hardware tests the bit in each status byte selected by DATALEN bits 2:0, until a bit is found that is equal to DATALEN bit 3. When the test succeeds, the SPIFI captures the byte that meets this test so that it can be read from the Data Register, and terminates the command by raising CS. The end-of-command interrupt can be enabled to inform software when this occurs |
| DOUT | rw | 15 | 1'b0 | If the DATALEN field is not zero, this bit controls the direction of the data: |
| INTLEN | rw | 18:16 | 3'b0 | This field controls how many intermediate bytes precede the data. (Each such byte may require 8 or 2 SCK cycles, depending on whether the intermediate field is in serial, 2-bit, or 4-bit format.) Intermediate bytes are output by the SPIFI, and include post-address control information, dummy and delay bytes. See the description of the Intermediate Data register for the contents of such bytes. |
| FIELDFORM | rw | 20:19 | 2'b0 | This field controls how the fields of the command are sent. |
| FRAMEFORM | rw | 23:21 | 3'b0 | This field controls the opcode and address fields. |
| OPCODE | rw | 31:24 | 8'b0 | The opcode of the command (not used for some FRAMEFORM values). |

### SPIFI0\_ADDR

Offset Address: 0x40080008

SPIFI address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ADDRESS | rw | 31:0 | 32'b0 | Address. |

### SPIFI0\_IDATA

Offset Address: 0x4008000c

SPIFI intermediate data register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| IDATA | rw | 31:0 | 32'b0 | Value of intermediate bytes. |

### SPIFI0\_CLIMIT

Offset Address: 0x40080010

SPIFI limit register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CLIMIT | rw | 31:0 | 32'b0 | Zero-based upper limit of cacheable memory |

### SPIFI0\_DATA

Offset Address: 0x40080014

SPIFI data register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DATA | rw | 31:0 | 32'b0 | Input or output data |

### SPIFI0\_MCMD

Offset Address: 0x40080018

SPIFI memory command register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 13:0 | 14'b0 | Reserved |
| POLL | rw | 14 | 1'b0 | This bit should be written as 0. |
| DOUT | rw | 15 | 1'b0 | This bit should be written as 0. |
| INTLEN | rw | 18:16 | 3'b0 | This field controls how many intermediate bytes precede the data. (Each such byte may require 8 or 2 SCK cycles, depending on whether the intermediate field is in serial, 2-bit, or 4-bit format.) Intermediate bytes are output by the SPIFI, and include post-address control information, dummy and delay bytes. See the description of the Intermediate Data register for the contents of such bytes. |
| FIELDFORM | rw | 20:19 | 2'b0 | This field controls how the fields of the command are sent. |
| FRAMEFORM | rw | 23:21 | 3'b0 | This field controls the opcode and address fields. |
| OPCODE | rw | 31:24 | 8'b0 | The opcode of the command (not used for some FRAMEFORM values). |

### SPIFI0\_STAT

Offset Address: 0x4008001c

SPIFI status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MCINIT | rw | 0 | 1'b0 | This bit is set when software successfully writes the Memory Command register, and is cleared by Reset or by writing a 1 to the RESET bit in this register. |
| CMD | rw | 1 | 1'b0 | This bit is 1 when the Command register is written. It is cleared by a hardware reset, a write to the RESET bit in this register, or the deassertion of CS which indicates that the command has completed communication with the SPI Flash. |
| Reserved | rw | 3:2 | 2'b0 | Reserved |
| RESET | rw | 4 | 1'b0 | Write a 1 to this bit to abort a current command or memory mode. This bit is cleared when the hardware is ready for a new command to be written to the Command register. |
| INTRQ | rw | 5 | 1'b0 | This bit reflects the SPIFI interrupt request. Write a 1 to this bit to clear it. This bit is set when a CMD was previously 1 and has been cleared due to the deassertion of CS. |
| Reserved | rw | 23:6 | 18'b0 | Reserved |
| VERSION | rw | 31:24 | 8'b0 | - |

### FLASH\_INI\_RD\_EN

Offset Address: 0x40081000

flash initial read register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| INI\_RD\_EN | rw | 0 | 1'b0 | enable contoller to automatically read GDR repaired information and lock bit |
| Reserved | rw | 31:1 | 31'b0 | Reserved |

### FLASH\_ERASE\_CTRL

Offset Address: 0x40081004

flash erase control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PAGE\_IDXL | rw | 6:0 | 7'b0 | Low 256KB page erase index |
| Reserved | rw | 7 | 1'b0 | Reserved |
| PAGE\_IDXH | rw | 14:8 | 7'b0 | High 256KB page erase index |
| Reserved | rw | 27:15 | 13'b0 | Reserved |
| HALF\_ERASEL\_EN | rw | 28 | 1'b0 | Write '1' to Enable Mass Erase Low 256KB Flash; Write '0' is inactive. This bit is set by software and reset at the end of low 256KB flash mass erase operation by hardware. |
| HALF\_ERASEH\_EN | rw | 29 | 1'b0 | Write '1' to Enable Mass Erase High 256KB Flash; Write '0' is inactive. This bit is set by software and reset at the end of high 256KB flash mass erase operation by hardware. |
| PAGE\_ERASEL\_EN | rw | 30 | 1'b0 | Low 256KB block page erase enable. This bit initiates a page erase operation when set. This bit is set by software and reset at the end of page erase operation by hardware. |
| PAGE\_ERASEH\_EN | rw | 31 | 1'b0 | High 256KB block page erase enable. This bit initiates a page erase operation when set. This bit is set by software and reset at the end of page erase operation by hardware. |

### FLASH\_ERASE\_TIME

Offset Address: 0x40081008

flash erase time setting register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ERASE\_TIME\_BASE | rw | 19:0 | 20'b0 | Erase time, which is used to control Terase, Tme and Tsme. An 8MHz clock is to count the erase time. The maximum time of erase is 100ms. Default value is 640000 cycles in 8 MHz, that's 80 ms. User should set a pessimistic value to avoid possible error in erase operation. |
| Reserved | rw | 31:20 | 12'b0 | Reserved |

### FLASH\_TIME\_CTRL

Offset Address: 0x4008100c

flash operation time setting register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PRGM\_CYCLE | rw | 11:0 | 12'b0 | Time base of some flash timing parameters, which represents 2 us. Default value is 64 cycles in 32 MHz (ahb clock). It is used in write and erase operations. |
| TIME\_BASE | rw | 19:12 | 8'b0 | Max write operation times in one program, which are used to control Terase and Tme. User should set a pessimistic value to avoid possible error in erase/page erase operation. When user do write operation: It is used to limit allowed write numbers. (Max 21 ms-Tnvs-Tpgs-Tpgh-Tnvh)/18us = 1167 This register is only used when common write. |
| Reserved | rw | 31:20 | 12'b0 | Reserved |

### FLASH\_SMART\_CTRL

Offset Address: 0x40081010

smart erase control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PRGML\_EN | rw | 0 | 1'b0 | It enable Low 256KB Flash write operation; |
| PRGMH\_EN | rw | 1 | 1'b0 | It enable High 256KB Flash write operation; |
| SMART\_WRITEL\_EN | rw | 2 | 1'b0 | It enable Low 256KB Flash Smart program flow. When smart write is done, hardware automatically clear it |
| SMART\_WRITEH\_EN | rw | 3 | 1'b0 | It enable High 256KB Flash Smart program flow. When smart write is done, hardware automatically clear it |
| SMART\_ERASEL\_EN | rw | 4 | 1'b0 | It enable Low 256KB Flash Smart erase flow; When smart erase is done, hardware automatically clear it |
| SMART\_ERASEH\_EN | rw | 5 | 1'b0 | It enable High 256KB Flash Smart erase flow; When smart erase is done, hardware automatically clear it |
| Reserved | rw | 7:6 | 2'b0 | Reserved |
| MAX\_WRITE | rw | 11:8 | 4'b0 | When smart program is used, this is the maximum retry number for one write operation. |
| MAX\_ERASE | rw | 17:12 | 6'b0 | When smart erase is used, this is the maximum retry number for one erase operation. |
| Reserved | rw | 31:18 | 14'b0 | Reserved |

### FLASH\_INTEN

Offset Address: 0x40081014

interrupt enable register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| AHBL\_INTEN | rw | 0 | 1'b0 | low 256K flash AHB error interrupt enable |
| LOCKL\_INTEN | rw | 1 | 1'b0 | low 256K flash lock error interrupt enable |
| ERASEL\_INTEN | rw | 2 | 1'b0 | low 256K flash erase status interrupt enable |
| WRITEL\_INTEN | rw | 3 | 1'b0 | low 256K flash write status interrupt enable |
| WRBUFL\_INTEN | rw | 4 | 1'b0 | low 256K flash write buffer status interrupt enable |
| Reserved | rw | 7:5 | 3'b0 | Reserved |
| AHBH\_INTEN | rw | 8 | 1'b0 | high 256K flash AHB error interrupt enable |
| LOCKH\_INTEN | rw | 9 | 1'b0 | high 256K flash lock error interrupt enable |
| ERASEH\_INTEN | rw | 10 | 1'b0 | high 256K flash erase status interrupt enable |
| WRITEH\_INTEN | rw | 11 | 1'b0 | high 256K flash write status interrupt enable |
| WRBUFH\_INTEN | rw | 12 | 1'b0 | high 256K flash write buffer status interrupt enable |
| Reserved | rw | 30:13 | 18'b0 | Reserved |
| FLASH\_INTEN | rw | 31 | 1'b0 | flash total interrupt enable |

### FLASH\_INT\_STAT

Offset Address: 0x40081018

interrupt status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| AHBL\_INT | rw | 0 | 1'b0 | It is low 256KB Flash AHB error interrupt stat. 1 indicates AHB operation error AHB error include: Write/read unmapped space; AHB align rules violation; Byte/half-word Flash write operation; |
| LOCKL\_INT | rw | 1 | 1'b0 | It is low 256KB Flash Lock page be accessed interrupt status |
| ERASEL\_INT | rw | 2 | 1'b0 | It is low 256KB Erase operation done interrupt status If erase is used, it indicates one erase is done. |
| WRITEL\_INT | rw | 3 | 1'b0 | It is low 256KB write operation done interrupt status If write is used, it indicates one program is done. |
| WRBUFL\_INT | rw | 4 | 1'b0 | It is low 256KB Write Buffer empty interrupt status 0 = write buffer is not empty 1 = write buffer is empty It is auto cleared when write buffer is written. It is enabled only when PRGML\_EN is enabled and write buffer is empty |
| WRITE\_FAIL\_L\_INT | rw | 5 | 1'b0 | When smart write of low 256KB Flash is enable, 0 = Smart write is successful, 1 = Smart write is fail. |
| ERASE\_FAIL\_L\_INT | rw | 6 | 1'b0 | When smart erase of low 256KB Flash is enable, 0 = Smart erase is successful, 1 = Smart erase is fail. |
| Reserved | rw | 7 | 1'b0 | Reserved |
| AHBH\_INT | rw | 8 | 1'b0 | it is high 256KB Flash AHB error interrupt stat 1 indicates AHB operation error AHB error include: Write/read unmapped space; AHB align rules violation; Byte/half-word Flash write operation; |
| LOCKH\_INT | rw | 9 | 1'b0 | it is high 256KB Flash Lock page be accessed interrupt status |
| ERASEH\_INT | rw | 10 | 1'b0 | it is high 256KB Flash Erase operation done interrupt status If erase is used, it indicates one erase is done. |
| WRITEH\_INT | rw | 11 | 1'b0 | it is high 256KB Flash write operation done interrupt status If write is used, it indicates one program is done. |
| WRBUFH\_INT | rw | 12 | 1'b0 | it is high 256KB Flash Write Buffer empty interrupt status 0 = write buffer is not empty 1 = write buffer is empty It is auto cleared when write buffer is written. It is enabled only when PRGMH\_EN is enabled and write buffer is empty |
| WRITE\_FAIL\_H\_INT | rw | 13 | 1'b0 | When smart write of high 256KB Flash is enable, 0 = Smart write is successful, 1 = Smart write is fail. |
| ERASE\_FAIL\_H\_INT | rw | 14 | 1'b0 | When smart erase of high 256KB Flash is enable, 0 = Smart erase is successful, 1 = Smart erase is fail. |
| Reserved | rw | 31:15 | 17'b0 | Reserved |

### FLASH\_INTCLR

Offset Address: 0x4008101c

interrupt clear register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| AHBL\_INTCLR | rw | 0 | 1'b0 | low 256K flash AHB error interrupt clear |
| LOCKL\_INTCLR | rw | 1 | 1'b0 | low 256K flash lock error interrupt clear |
| ERASEL\_INTCLR | rw | 2 | 1'b0 | low 256K flash erase status interrupt clear |
| WRITEL\_INTCLR | rw | 3 | 1'b0 | low 256K flash write status interrupt clear |
| Reserved | rw | 7:4 | 4'b0 | Reserved |
| AHBH\_INTCLR | rw | 8 | 1'b0 | high 256K flash AHB error interrupt clear |
| LOCKH\_INTCLR | rw | 9 | 1'b0 | high 256K flash lock error interrupt clear |
| ERASEH\_INTCLR | rw | 10 | 1'b0 | high 256K flash erase status interrupt clear |
| WRITEH\_INTCLR | rw | 11 | 1'b0 | high 256K flash write status interrupt clear |
| Reserved | rw | 31:12 | 20'b0 | Reserved |

### FLASH\_LOCK\_STAT0

Offset Address: 0x40081020

lock control register 0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PAGE\_LOCK0 | rw | 31:0 | 32'b0 | Low 256K flash main memory page 0-31 write and erase lock status |

### FLASH\_LOCK\_STAT1

Offset Address: 0x40081024

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PAGE\_LOCK1 | rw | 31:0 | 32'b0 | Low 256K flash main memory page 32-63 write and erase lock status |

### FLASH\_LOCK\_STAT2

Offset Address: 0x40081028

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PAGE\_LOCK2 | rw | 31:0 | 32'b0 | Low 256K flash main memory page 64-95 write and erase lock status |

### FLASH\_LOCK\_STAT3

Offset Address: 0x4008102c

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PAGE\_LOCK3 | rw | 31:0 | 32'b0 | Low 256K flash main memory page 96-127 write and erase lock status |

### FLASH\_LOCK\_STAT4

Offset Address: 0x40081030

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PAGE\_LOCK4 | rw | 31:0 | 32'b0 | high 256K flash main memory page 0-31 write and erase lock status |

### FLASH\_LOCK\_STAT5

Offset Address: 0x40081034

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PAGE\_LOCK5 | rw | 31:0 | 32'b0 | high 256K flash main memory page 32-63 write and erase lock status |

### FLASH\_LOCK\_STAT6

Offset Address: 0x40081038

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PAGE\_LOCK6 | rw | 31:0 | 32'b0 | high 256K flash main memory page 64-95 write and erase lock status |

### FLASH\_LOCK\_STAT7

Offset Address: 0x4008103c

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PAGE\_LOCK7 | rw | 31:0 | 32'b0 | high 256K flash main memory page 96-127 write and erase lock status |

### FLASH\_LOCK\_STAT8

Offset Address: 0x40081040

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MASS\_ERASE\_LOCK | rw | 0 | 1'b0 | Mass erase operation lock status 0 : Mass erase operation is locked 1 : Mass erase operation is unlocked |
| FSH\_PROTECT | rw | 1 | 1'b0 | SWD flash protection status 0 : flash is unprotected 1 : flash is protected |
| MEM\_PROTECT | rw | 2 | 1'b0 | SWD memory protection status 0 : Memory is unprotected 1 : Memory is protected |
| Reserved | rw | 31:3 | 29'b0 | Reserved |

### FLASH\_STATUS1

Offset Address: 0x40081048

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 8:0 | 9'b0 | Reserved |
| FSH\_ERA\_BUSY\_L | rw | 9 | 1'b0 | flash block 0 erase operation status 0 : no flash block 0 erase operation in progress. 1 : flash block 0 erase operation is in progress. |
| FSH\_WR\_BUSY\_L | rw | 10 | 1'b0 | flash block 0 write operation status: 0 : no flash block 0 write operation in progress. 1 : flash block 0 write operation is in progress. |
| DBG\_ERA\_DONE\_L | rw | 11 | 1'b0 | A flash block 0 debug initiated smart mass erase status. 0 : no debug port initiated flash block 0 smart mass erase operation in progress. 1 : debug port initiated flash block 0 smart mass erase operation in progress. |
| FSH\_ERA\_BUSY\_H | rw | 12 | 1'b0 | flash block 1 erase operation status 0 : no flash block 1 erase operation in progress. 1 : flash block 1 erase operation is in progress. |
| FSH\_WR\_BUSY\_H | rw | 13 | 1'b0 | flash block 1 write operation status: 0 : no flash block 1 write operation in progress. 1 : flash block 1 write operation is in progress. |
| DBG\_ERA\_DONE\_H | rw | 14 | 1'b0 | A flash block 1 debug initiated smart mass erase status. 0 : no debug port initiated flash block 1 smart mass erase operation in progress. 1 : debug port initiated flash block 1 smart mass erase operation in progress. |
| INI\_RD\_DONE | rw | 15 | 1'b0 | flash initial read done. |
| Reserved | rw | 25:16 | 10'b0 | Reserved |
| FSH\_STA | rw | 26 | 1'b0 | when 0 means data information is 0x55AA. |
| RESERVED | rw | 31:27 | 5'b0 | reserved |

### FLASH\_ERR\_INFOL1

Offset Address: 0x4008105c

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| WR\_FAILEDL\_ADDR | rw | 17:0 | 18'b0 | When a flash block 0 smart write fails, the address is stored in this bit filed |
| SMART\_FAILL\_CTR | rw | 23:18 | 6'b0 | The amount of fails during a smart write or smart erase is stored in this bit field |
| Reserved | rw | 31:24 | 8'b0 | Reserved |

### FLASH\_ERR\_INFOL2

Offset Address: 0x40081060

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| WR\_FAILEDL\_DATA | rw | 31:0 | 32'b0 | When a flash block 0 smart write fails, the data is stored in this bit field |

### FLASH\_ERR\_INFOL3

Offset Address: 0x40081064

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ERA\_FAILEDL\_INFO | rw | 17:0 | 18'b0 | When a smart erase on flash block 0 fails, the address is stored in this bit field |
| Reserved | rw | 31:18 | 14'b0 | Reserved |

### FLASH\_ERR\_INFOH1

Offset Address: 0x40081068

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| WR\_FAILEDH\_ADDR | rw | 17:0 | 18'b0 | When a flash block 1 smart write fails, the address is stored in this bit field |
| SMART\_FAILH\_CTR | rw | 23:18 | 6'b0 | The amount of fails during a msart write or smart erase is stored int his bit field |
| Reserved | rw | 31:24 | 8'b0 | Reserved |

### FLASH\_ERR\_INFOH2

Offset Address: 0x4008106c

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| WR\_FAILEDH\_DATA | rw | 31:0 | 32'b0 | When a flash block 1 smart write fails, the data is stored in this bit field |

### FLASH\_ERR\_INFOH3

Offset Address: 0x40081070

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ERA\_FAILEDH\_INFO | rw | 17:0 | 18'b0 | when a smart erase on flash block 1 fails, the address is stored in this bit field |
| Reserved | rw | 31:18 | 14'b0 | Reserved |

### FLASH\_DEBUG\_PASSWORD

Offset Address: 0x400810a8

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DEBUG\_PASSWORD | rw | 31:0 | 32'b0 | An SWD initiated smart mass erase operation will only be issued if this register is programmed with the value 0xCA1E093F. |

### FLASH\_ERASE\_PASSWORD

Offset Address: 0x400810ac

no description available

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ERASE\_PASSWORD | rw | 31:0 | 32'b0 | When this register is programmed with the value 0xCA1E093F, a FW initiated mass erase or page erase operation will bypass the current lock and protection scheme. |

### DMA0\_CTRL

Offset Address: 0x40082000

DMA control.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ENABLE | rw | 0 | 1'b0 | DMA controller master enable. |
| Reserved | rw | 31:1 | 31'b0 | Reserved |

### DMA0\_INTSTAT

Offset Address: 0x40082004

Interrupt status.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 0 | 1'b0 | Reserved |
| ACTIVEINT | rw | 1 | 1'b0 | Summarizes whether any enabled interrupts (other than error interrupts) are pending. |
| ACTIVEERRINT | rw | 2 | 1'b0 | Summarizes whether any error interrupts are pending. |
| Reserved | rw | 31:3 | 29'b0 | Reserved |

### DMA0\_SRAMBASE

Offset Address: 0x40082008

SRAM address of the channel configuration table.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 8:0 | 9'b0 | Reserved |
| OFFSET | rw | 31:9 | 23'b0 | Address bits 31:9 of the beginning of the DMA descriptor table. For 18 channels, the table must begin on a 512 byte boundary. |

### DMA0\_ENABLESET0

Offset Address: 0x40082020

Channel Enable read and Set for all DMA channels.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ENA | rw | 31:0 | 32'b0 | Enable for DMA channels. Bit n enables or disables DMA channel n. The number of bits = number of DMA channels in this device. Other bits are reserved. 0 = disabled. 1 = enabled. |

### DMA0\_ENABLECLR0

Offset Address: 0x40082028

Channel Enable Clear for all DMA channels.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CLR | rw | 31:0 | 32'b0 | Writing ones to this register clears the corresponding bits in ENABLESET0. Bit n clears the channel enable bit n. The number of bits = number of DMA channels in this device. Other bits are reserved. |

### DMA0\_ACTIVE0

Offset Address: 0x40082030

Channel Active status for all DMA channels.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ACT | rw | 31:0 | 32'b0 | Active flag for DMA channel n. Bit n corresponds to DMA channel n. The number of bits = number of DMA channels in this device. Other bits are reserved. 0 = not active. 1 = active. |

### DMA0\_BUSY0

Offset Address: 0x40082038

Channel Busy status for all DMA channels.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| BSY | rw | 31:0 | 32'b0 | Busy flag for DMA channel n. Bit n corresponds to DMA channel n. The number of bits = number of DMA channels in this device. Other bits are reserved. 0 = not busy. 1 = busy. |

### DMA0\_ERRINT0

Offset Address: 0x40082040

Error Interrupt status for all DMA channels.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ERR | rw | 31:0 | 32'b0 | Error Interrupt flag for DMA channel n. Bit n corresponds to DMA channel n. The number of bits = number of DMA channels in this device. Other bits are reserved. 0 = error interrupt is not active. 1 = error interrupt is active. |

### DMA0\_INTENSET0

Offset Address: 0x40082048

Interrupt Enable read and Set for all DMA channels.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| INTEN | rw | 31:0 | 32'b0 | Interrupt Enable read and set for DMA channel n. Bit n corresponds to DMA channel n. The number of bits = number of DMA channels in this device. Other bits are reserved. 0 = interrupt for DMA channel is disabled. 1 = interrupt for DMA channel is enabled. |

### DMA0\_INTENCLR0

Offset Address: 0x40082050

Interrupt Enable Clear for all DMA channels.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CLR | rw | 31:0 | 32'b0 | Writing ones to this register clears corresponding bits in the INTENSET0. Bit n corresponds to DMA channel n. The number of bits = number of DMA channels in this device. Other bits are reserved. |

### DMA0\_INTA0

Offset Address: 0x40082058

Interrupt A status for all DMA channels.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| IA | rw | 31:0 | 32'b0 | Interrupt A status for DMA channel n. Bit n corresponds to DMA channel n. The number of bits = number of DMA channels in this device. Other bits are reserved. 0 = the DMA channel interrupt A is not active. 1 = the DMA channel interrupt A is active. |

### DMA0\_INTB0

Offset Address: 0x40082060

Interrupt B status for all DMA channels.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| IB | rw | 31:0 | 32'b0 | Interrupt B status for DMA channel n. Bit n corresponds to DMA channel n. The number of bits = number of DMA channels in this device. Other bits are reserved. 0 = the DMA channel interrupt B is not active. 1 = the DMA channel interrupt B is active. |

### DMA0\_SETVALID0

Offset Address: 0x40082068

Set ValidPending control bits for all DMA channels.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SV | rw | 31:0 | 32'b0 | SETVALID control for DMA channel n. Bit n corresponds to DMA channel n. The number of bits = number of DMA channels in this device. Other bits are reserved. 0 = no effect. 1 = sets the VALIDPENDING control bit for DMA channel n |

### DMA0\_SETTRIG0

Offset Address: 0x40082070

Set Trigger control bits for all DMA channels.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TRIG | rw | 31:0 | 32'b0 | Set Trigger control bit for DMA channel 0. Bit n corresponds to DMA channel n. The number of bits = number of DMA channels in this device. Other bits are reserved. 0 = no effect. 1 = sets the TRIG bit for DMA channel n. |

### DMA0\_ABORT0

Offset Address: 0x40082078

Channel Abort control for all DMA channels.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ABORTCTRL | rw | 31:0 | 32'b0 | Abort control for DMA channel 0. Bit n corresponds to DMA channel n. 0 = no effect. 1 = aborts DMA operations on channel n. |

### FLEXCOMM0\_IOMODE

Offset Address: 0x40083f00

io mode register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DIO\_MODE | rw | 0 | 1'b0 | IO mode register, SPI share MISO/MOSI at MOSI, USART share TXD/RXD at RXD |
| DIO\_OEN | rw | 1 | 1'b0 | shared pin direction register |
| Reserved | rw | 31:2 | 30'b0 | Reserved |

### FLEXCOMM0\_PSELID

Offset Address: 0x40083ff8

Peripheral Select and Flexcomm ID register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PERSEL | rw | 2:0 | 3'b0 | Peripheral Select. This field is writable by software. |
| LOCK | rw | 3 | 1'b0 | Lock the peripheral select. This field is writable by software. |
| USARTPRESENT | rw | 4 | 1'b0 | USART present indicator. This field is Read-only. |
| SPIPRESENT | rw | 5 | 1'b0 | SPI present indicator. This field is Read-only. |
| MI2CPRESENT | rw | 6 | 1'b0 | I2C present indicator. This field is Read-only. |
| MI2SPRESENT | rw | 7 | 1'b0 | I 2S present indicator. This field is Read-only. |
| SC3W | rw | 8 | 1'b0 | Smart card/SPI 3 wire mode feature indicator. This field is Read-only |
| Reserved | rw | 11:9 | 3'b0 | Reserved |
| ID | rw | 31:12 | 20'b0 | Flexcomm ID. |

### FLEXCOMM0\_PID

Offset Address: 0x40083ffc

Peripheral identification register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 7:0 | 8'b0 | Reserved |
| Minor\_Rev | rw | 11:8 | 4'b0 | Minor revision of module implementation. |
| Major\_Rev | rw | 15:12 | 4'b0 | Major revision of module implementation. |
| ID | rw | 31:16 | 16'b0 | Module identifier for the selected function. |

### USART0\_CFG

Offset Address: 0x40083000

USART Configuration register. Basic USART configuration settings that typically are not changed during operation.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ENABLE | rw | 0 | 1'b0 | USART Enable. |
| Reserved | rw | 1 | 1'b0 | Reserved |
| DATALEN | rw | 3:2 | 2'b0 | Selects the data size for the USART. |
| PARITYSEL | rw | 5:4 | 2'b0 | Selects what type of parity is used by the USART. |
| STOPLEN | rw | 6 | 1'b0 | Number of stop bits appended to transmitted data. Only a single stop bit is required for received data. |
| MODE32K | rw | 7 | 1'b0 | Selects standard or 32 kHz clocking mode. |
| LINMODE | rw | 8 | 1'b0 | LIN break mode enable. |
| CTSEN | rw | 9 | 1'b0 | CTS Enable. Determines whether CTS is used for flow control. CTS can be from the input pin, or from the USART'-s own RTS if loopback mode is enabled. |
| Reserved | rw | 10 | 1'b0 | Reserved |
| SYNCEN | rw | 11 | 1'b0 | Selects synchronous or asynchronous operation. |
| CLKPOL | rw | 12 | 1'b0 | Selects the clock polarity and sampling edge of received data in synchronous mode. |
| Reserved | rw | 13 | 1'b0 | Reserved |
| SYNCMST | rw | 14 | 1'b0 | Synchronous mode Master select. |
| LOOP | rw | 15 | 1'b0 | Selects data loopback mode. |
| Reserved | rw | 17:16 | 2'b0 | Reserved |
| OETA | rw | 18 | 1'b0 | Output Enable Turnaround time enable for RS-485 operation. |
| AUTOADDR | rw | 19 | 1'b0 | Automatic Address matching enable. |
| OESEL | rw | 20 | 1'b0 | Output Enable Select. |
| OEPOL | rw | 21 | 1'b0 | Output Enable Polarity. |
| RXPOL | rw | 22 | 1'b0 | Receive data polarity. |
| TXPOL | rw | 23 | 1'b0 | Transmit data polarity. |
| Reserved | rw | 31:24 | 8'b0 | Reserved |

### USART0\_CTL

Offset Address: 0x40083004

USART Control register. USART control settings that are more likely to change during operation.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 0 | 1'b0 | Reserved |
| TXBRKEN | rw | 1 | 1'b0 | Break Enable. |
| ADDRDET | rw | 2 | 1'b0 | Enable address detect mode. |
| Reserved | rw | 5:3 | 3'b0 | Reserved |
| TXDIS | rw | 6 | 1'b0 | Transmit Disable. |
| Reserved | rw | 7 | 1'b0 | Reserved |
| CC | rw | 8 | 1'b0 | Continuous Clock generation. By default, SCLK is only output while data is being transmitted in synchronous mode. |
| CLRCCONRX | rw | 9 | 1'b0 | Clear Continuous Clock. |
| Reserved | rw | 15:10 | 6'b0 | Reserved |
| AUTOBAUD | rw | 16 | 1'b0 | Autobaud enable. |
| Reserved | rw | 31:17 | 15'b0 | Reserved |

### USART0\_STAT

Offset Address: 0x40083008

USART Status register. The complete status value can be read here. Writing ones clears some bits in the register. Some bits can be cleared by writing a 1 to them.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 0 | 1'b0 | Reserved |
| RXIDLE | rw | 1 | 1'b0 | Receiver Idle. When 0, indicates that the receiver is currently in the process of receiving data. When 1, indicates that the receiver is not currently in the process of receiving data. |
| Reserved | rw | 2 | 1'b0 | Reserved |
| TXIDLE | rw | 3 | 1'b0 | Transmitter Idle. When 0, indicates that the transmitter is currently in the process of sending data.When 1, indicate that the transmitter is not currently in the process of sending data. |
| CTS | rw | 4 | 1'b0 | This bit reflects the current state of the CTS signal, regardless of the setting of the CTSEN bit in the CFG register. This will be the value of the CTS input pin unless loopback mode is enabled. |
| DELTACTS | rw | 5 | 1'b0 | This bit is set when a change in the state is detected for the CTS flag above. This bit is cleared by software. |
| TXDISSTAT | rw | 6 | 1'b0 | Transmitter Disabled Status flag. When 1, this bit indicates that the USART transmitter is fully idle after being disabled via the TXDIS bit in the CFG register (TXDIS = 1). |
| Reserved | rw | 9:7 | 3'b0 | Reserved |
| RXBRK | rw | 10 | 1'b0 | Received Break. This bit reflects the current state of the receiver break detection logic. It is set when the Un\_RXD pin remains low for 16 bit times. Note that FRAMERRINT will also be set when this condition occurs because the stop bit(s) for the character would be missing. RXBRK is cleared when the Un\_RXD pin goes high. |
| DELTARXBRK | rw | 11 | 1'b0 | This bit is set when a change in the state of receiver break detection occurs. Cleared by software. |
| START | rw | 12 | 1'b0 | This bit is set when a start is detected on the receiver input. Its purpose is primarily to allow wake-up from Deep-sleep or Power-down mode immediately when a start is detected. Cleared by software. |
| FRAMERRINT | rw | 13 | 1'b0 | Framing Error interrupt flag. This flag is set when a character is received with a missing stop bit at the expected location. This could be an indication of a baud rate or configuration mismatch with the transmitting source. |
| PARITYERRINT | rw | 14 | 1'b0 | Parity Error interrupt flag. This flag is set when a parity error is detected in a received character. |
| RXNOISEINT | rw | 15 | 1'b0 | Received Noise interrupt flag. Three samples of received data are taken in order to determine the value of each received data bit, except in synchronous mode. This acts as a noise filter if one sample disagrees. This flag is set when a received data bit contains one disagreeing sample. This could indicate line noise, a baud rate or character format mismatch, or loss of synchronization during data reception. |
| ABERR | rw | 16 | 1'b0 | Auto baud Error. An auto baud error can occur if the BRG counts to its limit before the end of the start bit that is being measured, essentially an auto baud time-out. |
| Reserved | rw | 31:17 | 15'b0 | Reserved |

### USART0\_INTENSET

Offset Address: 0x4008300c

Interrupt Enable read and Set register for USART (not FIFO) status. Contains individual interrupt enable bits for each potential USART interrupt. A complete value may be read from this register. Writing a 1 to any implemented bit position causes that bit to be set.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 2:0 | 3'b0 | Reserved |
| TXIDLEEN | rw | 3 | 1'b0 | When 1, enables an interrupt when the transmitter becomes idle (TXIDLE = 1). |
| Reserved | rw | 4 | 1'b0 | Reserved |
| DELTACTSEN | rw | 5 | 1'b0 | When 1, enables an interrupt when there is a change in the state of the CTS input. |
| TXDISEN | rw | 6 | 1'b0 | When 1, enables an interrupt when the transmitter is fully disabled as indicated by the TXDISINT flag in STAT. See description of the TXDISINT bit for details. |
| Reserved | rw | 10:7 | 4'b0 | Reserved |
| DELTARXBRKEN | rw | 11 | 1'b0 | When 1, enables an interrupt when a change of state has occurred in the detection of a received break condition (break condition asserted or deasserted). |
| STARTEN | rw | 12 | 1'b0 | When 1, enables an interrupt when a received start bit has been detected. |
| FRAMERREN | rw | 13 | 1'b0 | When 1, enables an interrupt when a framing error has been detected. |
| PARITYERREN | rw | 14 | 1'b0 | When 1, enables an interrupt when a parity error has been detected. |
| RXNOISEEN | rw | 15 | 1'b0 | When 1, enables an interrupt when noise is detected. See description of the RXNOISEINT bit in Table 354. |
| ABERREN | rw | 16 | 1'b0 | When 1, enables an interrupt when an auto baud error occurs. |
| Reserved | rw | 31:17 | 15'b0 | Reserved |

### USART0\_INTENCLR

Offset Address: 0x40083010

Interrupt Enable Clear register. Allows clearing any combination of bits in the INTENSET register. Writing a 1 to any implemented bit position causes the corresponding bit to be cleared.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 2:0 | 3'b0 | Reserved |
| TXIDLECLR | rw | 3 | 1'b0 | Writing 1 clears the corresponding bit in the INTENSET register. |
| Reserved | rw | 4 | 1'b0 | Reserved |
| DELTACTSCLR | rw | 5 | 1'b0 | Writing 1 clears the corresponding bit in the INTENSET register. |
| TXDISCLR | rw | 6 | 1'b0 | Writing 1 clears the corresponding bit in the INTENSET register. |
| Reserved | rw | 10:7 | 4'b0 | Reserved |
| DELTARXBRKCLR | rw | 11 | 1'b0 | Writing 1 clears the corresponding bit in the INTENSET register. |
| STARTCLR | rw | 12 | 1'b0 | Writing 1 clears the corresponding bit in the INTENSET register. |
| FRAMERRCLR | rw | 13 | 1'b0 | Writing 1 clears the corresponding bit in the INTENSET register. |
| PARITYERRCLR | rw | 14 | 1'b0 | Writing 1 clears the corresponding bit in the INTENSET register. |
| RXNOISECLR | rw | 15 | 1'b0 | Writing 1 clears the corresponding bit in the INTENSET register. |
| ABERRCLR | rw | 16 | 1'b0 | Writing 1 clears the corresponding bit in the INTENSET register. |
| Reserved | rw | 31:17 | 15'b0 | Reserved |

### USART0\_BRG

Offset Address: 0x40083020

Baud Rate Generator register. 16-bit integer baud rate divisor value.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| BRGVAL | rw | 15:0 | 16'b0 | This value is used to divide the USART input clock to determine the baud rate, based on the input clock from the FRG. 0 = FCLK is used directly by the USART function. 1 = FCLK is divided by 2 before use by the USART function. 2 = FCLK is divided by 3 before use by the USART function. 0xFFFF = FCLK is divided by 65,536 before use by the USART function. |
| Reserved | rw | 31:16 | 16'b0 | Reserved |

### USART0\_INTSTAT

Offset Address: 0x40083024

Interrupt status register. Reflects interrupts that are currently enabled.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 2:0 | 3'b0 | Reserved |
| TXIDLE | rw | 3 | 1'b0 | Transmitter Idle status. |
| Reserved | rw | 4 | 1'b0 | Reserved |
| DELTACTS | rw | 5 | 1'b0 | This bit is set when a change in the state of the CTS input is detected. |
| TXDISINT | rw | 6 | 1'b0 | Transmitter Disabled Interrupt flag. |
| Reserved | rw | 10:7 | 4'b0 | Reserved |
| DELTARXBRK | rw | 11 | 1'b0 | This bit is set when a change in the state of receiver break detection occurs. |
| START | rw | 12 | 1'b0 | This bit is set when a start is detected on the receiver input. |
| FRAMERRINT | rw | 13 | 1'b0 | Framing Error interrupt flag. |
| PARITYERRINT | rw | 14 | 1'b0 | Parity Error interrupt flag. |
| RXNOISEINT | rw | 15 | 1'b0 | Received Noise interrupt flag. |
| ABERRINT | rw | 16 | 1'b0 | Auto baud Error Interrupt flag. |
| Reserved | rw | 31:17 | 15'b0 | Reserved |

### USART0\_OSR

Offset Address: 0x40083028

Oversample selection register for asynchronous communication.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| OSRVAL | rw | 3:0 | 4'b0 | Oversample Selection Value. 0 to 3 = not supported 0x4 = 5 function clocks are used to transmit and receive each data bit. 0x5 = 6 function clocks are used to transmit and receive each data bit. 0xF= 16 function clocks are used to transmit and receive each data bit. |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### USART0\_ADDR

Offset Address: 0x4008302c

Address register for automatic address matching.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ADDRESS | rw | 7:0 | 8'b0 | 8-bit address used with automatic address matching. Used when address detection is enabled (ADDRDET in CTL = 1) and automatic address matching is enabled (AUTOADDR in CFG = 1). |
| Reserved | rw | 31:8 | 24'b0 | Reserved |

### USART0\_FIFOCFG

Offset Address: 0x40083e00

FIFO configuration and enable register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ENABLETX | rw | 0 | 1'b0 | Enable the transmit FIFO. |
| ENABLERX | rw | 1 | 1'b0 | Enable the receive FIFO. |
| Reserved | rw | 3:2 | 2'b0 | Reserved |
| SIZE | rw | 5:4 | 2'b0 | FIFO size configuration. This is a read-only field. 0x0 = FIFO is configured as 16 entries of 8 bits. 0x1, 0x2, 0x3 = not applicable to USART. |
| Reserved | rw | 11:6 | 6'b0 | Reserved |
| DMATX | rw | 12 | 1'b0 | DMA configuration for transmit. |
| DMARX | rw | 13 | 1'b0 | DMA configuration for receive. |
| Reserved | rw | 15:14 | 2'b0 | Reserved |
| EMPTYTX | rw | 16 | 1'b0 | Empty command for the transmit FIFO. When a 1 is written to this bit, the TX FIFO is emptied. |
| EMPTYRX | rw | 17 | 1'b0 | Empty command for the receive FIFO. When a 1 is written to this bit, the RX FIFO is emptied. |
| Reserved | rw | 31:18 | 14'b0 | Reserved |

### USART0\_FIFOSTAT

Offset Address: 0x40083e04

FIFO status register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TXERR | rw | 0 | 1'b0 | TX FIFO error. Will be set if a transmit FIFO error occurs. This could be an overflow caused by pushing data into a full FIFO, or by an underflow if the FIFO is empty when data is needed. Cleared by writing a 1 to this bit. |
| RXERR | rw | 1 | 1'b0 | RX FIFO error. Will be set if a receive FIFO overflow occurs, caused by software or DMA not emptying the FIFO fast enough. Cleared by writing a 1 to this bit. |
| Reserved | rw | 2 | 1'b0 | Reserved |
| PERINT | rw | 3 | 1'b0 | Peripheral interrupt. When 1, this indicates that the peripheral function has asserted an interrupt. The details can be found by reading the peripheral'-s STAT register. |
| TXEMPTY | rw | 4 | 1'b0 | Transmit FIFO empty. When 1, the transmit FIFO is empty. The peripheral may still be processing the last piece of data. |
| TXNOTFULL | rw | 5 | 1'b0 | Transmit FIFO not full. When 1, the transmit FIFO is not full, so more data can be written. When 0, the transmit FIFO is full and another write would cause it to overflow. |
| RXNOTEMPTY | rw | 6 | 1'b0 | Receive FIFO not empty. When 1, the receive FIFO is not empty, so data can be read. When 0, the receive FIFO is empty. |
| RXFULL | rw | 7 | 1'b0 | Receive FIFO full. When 1, the receive FIFO is full. Data needs to be read out to prevent the peripheral from causing an overflow. |
| TXLVL | rw | 12:8 | 5'b0 | Transmit FIFO current level. A 0 means the TX FIFO is currently empty, and the TXEMPTY and TXNOTFULL flags will be 1. Other values tell how much data is actually in the TX FIFO at the point where the read occurs. If the TX FIFO is full, the TXEMPTY and TXNOTFULL flags will be 0. |
| Reserved | rw | 15:13 | 3'b0 | Reserved |
| RXLVL | rw | 20:16 | 5'b0 | Receive FIFO current level. A 0 means the RX FIFO is currently empty, and the RXFULL and RXNOTEMPTY flags will be 0. Other values tell how much data is actually in the RX FIFO at the point where the read occurs. If the RX FIFO is full, the RXFULL and RXNOTEMPTY flags will be 1. |
| Reserved | rw | 31:21 | 11'b0 | Reserved |

### USART0\_FIFOTRIG

Offset Address: 0x40083e08

FIFO trigger settings for interrupt and DMA request.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TXLVLENA | rw | 0 | 1'b0 | Transmit FIFO level trigger enable. This trigger will become an interrupt if enabled in FIFOINTENSET, or a DMA trigger if DMATX in FIFOCFG is set. |
| RXLVLENA | rw | 1 | 1'b0 | Receive FIFO level trigger enable. This trigger will become an interrupt if enabled in FIFOINTENSET, or a DMA trigger if DMARX in FIFOCFG is set. |
| Reserved | rw | 7:2 | 6'b0 | Reserved |
| TXLVL | rw | 11:8 | 4'b0 | Transmit FIFO level trigger point. This field is used only when TXLVLENA = 1. If enabled to do so, the FIFO level can wake up the device just enough to perform DMA, then return to the reduced power mode. See Hardware Wake-up control register. 0 = trigger when the TX FIFO becomes empty. 1 = trigger when the TX FIFO level decreases to one entry. 15 = trigger when the TX FIFO level decreases to 15 entries (is no longer full). |
| Reserved | rw | 15:12 | 4'b0 | Reserved |
| RXLVL | rw | 19:16 | 4'b0 | Receive FIFO level trigger point. The RX FIFO level is checked when a new piece of data is received. This field is used only when RXLVLENA = 1. If enabled to do so, the FIFO level can wake up the device just enough to perform DMA, then return to the reduced power mode. See Hardware Wake-up control register. 0 = trigger when the RX FIFO has received one entry (is no longer empty). 1 = trigger when the RX FIFO has received two entries. 15 = trigger when the RX FIFO has received 16 entries (has become full). |
| Reserved | rw | 31:20 | 12'b0 | Reserved |

### USART0\_FIFOINTENSET

Offset Address: 0x40083e10

FIFO interrupt enable set (enable) and read register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TXERR | rw | 0 | 1'b0 | Determines whether an interrupt occurs when a transmit error occurs, based on the TXERR flag in the FIFOSTAT register. |
| RXERR | rw | 1 | 1'b0 | Determines whether an interrupt occurs when a receive error occurs, based on the RXERR flag in the FIFOSTAT register. |
| TXLVL | rw | 2 | 1'b0 | Determines whether an interrupt occurs when a the transmit FIFO reaches the level specified by the TXLVL field in the FIFOTRIG register. |
| RXLVL | rw | 3 | 1'b0 | Determines whether an interrupt occurs when a the receive FIFO reaches the level specified by the TXLVL field in the FIFOTRIG register. |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### USART0\_FIFOINTENCLR

Offset Address: 0x40083e14

FIFO interrupt enable clear (disable) and read register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TXERR | rw | 0 | 1'b0 | Writing one clears the corresponding bits in the FIFOINTENSET register. |
| RXERR | rw | 1 | 1'b0 | Writing one clears the corresponding bits in the FIFOINTENSET register. |
| TXLVL | rw | 2 | 1'b0 | Writing one clears the corresponding bits in the FIFOINTENSET register. |
| RXLVL | rw | 3 | 1'b0 | Writing one clears the corresponding bits in the FIFOINTENSET register. |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### USART0\_FIFOINTSTAT

Offset Address: 0x40083e18

FIFO interrupt status register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TXERR | rw | 0 | 1'b0 | TX FIFO error. |
| RXERR | rw | 1 | 1'b0 | RX FIFO error. |
| TXLVL | rw | 2 | 1'b0 | Transmit FIFO level interrupt. |
| RXLVL | rw | 3 | 1'b0 | Receive FIFO level interrupt. |
| PERINT | rw | 4 | 1'b0 | Peripheral interrupt. |
| Reserved | rw | 31:5 | 27'b0 | Reserved |

### USART0\_FIFOWR

Offset Address: 0x40083e20

FIFO write data.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TXDATA | rw | 8:0 | 9'b0 | Transmit data to the FIFO. |
| Reserved | rw | 31:9 | 23'b0 | Reserved |

### USART0\_FIFORD

Offset Address: 0x40083e30

FIFO read data.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| RXDATA | rw | 8:0 | 9'b0 | Received data from the FIFO. The number of bits used depends on the DATALEN and PARITYSEL settings. |
| Reserved | rw | 12:9 | 4'b0 | Reserved |
| FRAMERR | rw | 13 | 1'b0 | Framing Error status flag. This bit reflects the status for the data it is read along with from the FIFO, and indicates that the character was received with a missing stop bit at the expected location. This could be an indication of a baud rate or configuration mismatch with the transmitting source. |
| PARITYERR | rw | 14 | 1'b0 | Parity Error status flag. This bit reflects the status for the data it is read along with from the FIFO. This bit will be set when a parity error is detected in a received character. |
| RXNOISE | rw | 15 | 1'b0 | Received Noise flag. See description of the RxNoiseInt bit in Table 354. |
| Reserved | rw | 31:16 | 16'b0 | Reserved |

### USART0\_FIFORDNOPOP

Offset Address: 0x40083e40

FIFO data read with no FIFO pop.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| RXDATA | rw | 8:0 | 9'b0 | Received data from the FIFO. The number of bits used depends on the DATALEN and PARITYSEL settings. |
| Reserved | rw | 12:9 | 4'b0 | Reserved |
| FRAMERR | rw | 13 | 1'b0 | Framing Error status flag. This bit reflects the status for the data it is read along with from the FIFO, and indicates that the character was received with a missing stop bit at the expected location. This could be an indication of a baud rate or configuration mismatch with the transmitting source. |
| PARITYERR | rw | 14 | 1'b0 | Parity Error status flag. This bit reflects the status for the data it is read along with from the FIFO. This bit will be set when a parity error is detected in a received character. |
| RXNOISE | rw | 15 | 1'b0 | Received Noise flag. See description of the RxNoiseInt bit in Table 354. |
| Reserved | rw | 31:16 | 16'b0 | Reserved |

### USART0\_ID

Offset Address: 0x40083ffc

USART module Identification. This value appears in the shared Flexcomm peripheral ID register when USART is selected.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| APERTURE | rw | 7:0 | 8'b0 | Aperture: encoded as (aperture size/4K) -1, so 0x00 means a 4K aperture. |
| MINOR\_REV | rw | 11:8 | 4'b0 | Minor revision of module implementation, starting at 0. Minor revision of module implementation, starting at 0. Software compatibility is expected between minor revisions. |
| MAJOR\_REV | rw | 15:12 | 4'b0 | Major revision of module implementation, starting at 0. There may not be software compatibility between major revisions. |
| ID | rw | 31:16 | 16'b0 | Unique module identifier for this IP block. |

### USB0\_DEVCMDSTAT

Offset Address: 0x40084000

USB Device Command/Status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DEV\_ADDR | rw | 6:0 | 7'b0 | USB device address. After bus reset, the address is reset to 0x00. If the enable bit is set, the device will respond on packets for function address DEV\_ADDR. When receiving a SetAddress Control Request from the USB host, software must program the new address before completing the status phase of the SetAddress Control Request. |
| DEV\_EN | rw | 7 | 1'b0 | USB device enable. If this bit is set, the HW will start responding on packets for function address DEV\_ADDR. |
| SETUP | rw | 8 | 1'b0 | SETUP token received. If a SETUP token is received and acknowledged by the device, this bit is set. As long as this bit is set all received IN and OUT tokens will be NAKed by HW. SW must clear this bit by writing a one. If this bit is zero, HW will handle the tokens to the CTRL EP0 as indicated by the CTRL EP0 IN and OUT data information programmed by SW. |
| FORCE\_NEEDCLK | rw | 9 | 1'b0 | Forces the NEEDCLK output to always be on: |
| Reserved | rw | 10 | 1'b0 | Reserved |
| LPM\_SUP | rw | 11 | 1'b0 | LPM Supported: |
| INTONNAK\_AO | rw | 12 | 1'b0 | Interrupt on NAK for interrupt and bulk OUT EP |
| INTONNAK\_AI | rw | 13 | 1'b0 | Interrupt on NAK for interrupt and bulk IN EP |
| INTONNAK\_CO | rw | 14 | 1'b0 | Interrupt on NAK for control OUT EP |
| INTONNAK\_CI | rw | 15 | 1'b0 | Interrupt on NAK for control IN EP |
| DCON | rw | 16 | 1'b0 | Device status - connect. The connect bit must be set by SW to indicate that the device must signal a connect. The pull-up resistor on USB\_DP will be enabled when this bit is set and the VBUSDEBOUNCED bit is one. |
| DSUS | rw | 17 | 1'b0 | Device status - suspend. The suspend bit indicates the current suspend state. It is set to 1 when the device hasn'-t seen any activity on its upstream port for more than 3 milliseconds. It is reset to 0 on any activity. When the device is suspended (Suspend bit DSUS = 1) and the software writes a 0 to it, the device will generate a remote wake-up. This will only happen when the device is connected (Connect bit = 1). When the device is not connected or not suspended, a writing a 0 has no effect. Writing a 1 never has an effect. |
| Reserved | rw | 18 | 1'b0 | Reserved |
| LPM\_SUS | rw | 19 | 1'b0 | Device status - LPM Suspend. This bit represents the current LPM suspend state. It is set to 1 by HW when the device has acknowledged the LPM request from the USB host and the Token Retry Time of 10 ms has elapsed. When the device is in the LPM suspended state (LPM suspend bit = 1) and the software writes a zero to this bit, the device will generate a remote walk-up. Software can only write a zero to this bit when the LPM\_REWP bit is set to 1. HW resets this bit when it receives a host initiated resume. HW only updates the LPM\_SUS bit when the LPM\_SUPP bit is equal to one. |
| LPM\_REWP | rw | 20 | 1'b0 | LPM Remote Wake-up Enabled by USB host. HW sets this bit to one when the bRemoteWake bit in the LPM extended token is set to 1. HW will reset this bit to 0 when it receives the host initiated LPM resume, when a remote wake-up is sent by the device or when a USB bus reset is received. Software can use this bit to check if the remote wake-up feature is enabled by the host for the LPM transaction. |
| Reserved | rw | 23:21 | 3'b0 | Reserved |
| DCON\_C | rw | 24 | 1'b0 | Device status - connect change. The Connect Change bit is set when the device'-s pull-up resistor is disconnected because VBus disappeared. The bit is reset by writing a one to it. |
| DSUS\_C | rw | 25 | 1'b0 | Device status - suspend change. The suspend change bit is set to 1 when the suspend bit toggles. The suspend bit can toggle because: - The device goes in the suspended state - The device is disconnected - The device receives resume signaling on its upstream port. The bit is reset by writing a one to it. |
| DRES\_C | rw | 26 | 1'b0 | Device status - reset change. This bit is set when the device received a bus reset. On a bus reset the device will automatically go to the default state (unconfigured and responding to address 0). The bit is reset by writing a one to it. |
| Reserved | rw | 27 | 1'b0 | Reserved |
| VBUSDEBOUNCED | rw | 28 | 1'b0 | This bit indicates if Vbus is detected or not. The bit raises immediately when Vbus becomes high. It drops to zero if Vbus is low for at least 3 ms. If this bit is high and the DCon bit is set, the HW will enable the pull-up resistor to signal a connect. |
| Reserved | rw | 31:29 | 3'b0 | Reserved |

### USB0\_INFO

Offset Address: 0x40084004

USB Info register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FRAME\_NR | rw | 10:0 | 11'b0 | Frame number. This contains the frame number of the last successfully received SOF. In case no SOF was received by the device at the beginning of a frame, the frame number returned is that of the last successfully received SOF. In case the SOF frame number contained a CRC error, the frame number returned will be the corrupted frame number as received by the device. |
| ERR\_CODE | rw | 14:11 | 4'b0 | The error code which last occurred: |
| Reserved | rw | 31:15 | 17'b0 | Reserved |

### USB0\_EPLISTSTART

Offset Address: 0x40084008

USB EP Command/Status List start address

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 7:0 | 8'b0 | Reserved |
| EP\_LIST | rw | 31:8 | 24'b0 | Start address of the USB EP Command/Status List. |

### USB0\_DATABUFSTART

Offset Address: 0x4008400c

USB Data buffer start address

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 21:0 | 22'b0 | Reserved |
| DA\_BUF | rw | 31:22 | 10'b0 | Start address of the buffer pointer page where all endpoint data buffers are located. |

### USB0\_LPM

Offset Address: 0x40084010

USB Link Power Management register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| HIRD\_HW | rw | 3:0 | 4'b0 | Host Initiated Resume Duration - HW. This is the HIRD value from the last received LPM token |
| HIRD\_SW | rw | 7:4 | 4'b0 | Host Initiated Resume Duration - SW. This is the time duration required by the USB device system to come out of LPM initiated suspend after receiving the host initiated LPM resume. |
| DATA\_PENDING | rw | 8 | 1'b0 | As long as this bit is set to one and LPM supported bit is set to one, HW will return a NYET handshake on every LPM token it receives. If LPM supported bit is set to one and this bit is zero, HW will return an ACK handshake on every LPM token it receives. If SW has still data pending and LPM is supported, it must set this bit to 1. |
| Reserved | rw | 31:9 | 23'b0 | Reserved |

### USB0\_EPSKIP

Offset Address: 0x40084014

USB Endpoint skip

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SKIP | rw | 29:0 | 30'b0 | Endpoint skip: Writing 1 to one of these bits, will indicate to HW that it must deactivate the buffer assigned to this endpoint and return control back to software. When HW has deactivated the endpoint, it will clear this bit, but it will not modify the EPINUSE bit. An interrupt will be generated when the Active bit goes from 1 to 0. Note: In case of double-buffering, HW will only clear the Active bit of the buffer indicated by the EPINUSE bit. |
| Reserved | rw | 31:30 | 2'b0 | Reserved |

### USB0\_EPINUSE

Offset Address: 0x40084018

USB Endpoint Buffer in use

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 1:0 | 2'b0 | Reserved |
| BUF | rw | 9:2 | 8'b0 | Buffer in use: This register has one bit per physical endpoint. 0: HW is accessing buffer 0. 1: HW is accessing buffer 1. |
| Reserved | rw | 31:10 | 22'b0 | Reserved |

### USB0\_EPBUFCFG

Offset Address: 0x4008401c

USB Endpoint Buffer Configuration register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 1:0 | 2'b0 | Reserved |
| BUF\_SB | rw | 9:2 | 8'b0 | Buffer usage: This register has one bit per physical endpoint. 0: Single-buffer. 1: Double-buffer. If the bit is set to single-buffer (0), it will not toggle the corresponding EPINUSE bit when it clears the active bit. If the bit is set to double-buffer (1), HW will toggle the EPINUSE bit when it clears the Active bit for the buffer. |
| Reserved | rw | 31:10 | 22'b0 | Reserved |

### USB0\_INTSTAT

Offset Address: 0x40084020

USB interrupt status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| EP0OUT | rw | 0 | 1'b0 | Interrupt status register bit for the Control EP0 OUT direction. This bit will be set if NBytes transitions to zero or the skip bit is set by software or a SETUP packet is successfully received for the control EP0. If the IntOnNAK\_CO is set, this bit will also be set when a NAK is transmitted for the Control EP0 OUT direction. Software can clear this bit by writing a one to it. |
| EP0IN | rw | 1 | 1'b0 | Interrupt status register bit for the Control EP0 IN direction. This bit will be set if NBytes transitions to zero or the skip bit is set by software. If the IntOnNAK\_CI is set, this bit will also be set when a NAK is transmitted for the Control EP0 IN direction. Software can clear this bit by writing a one to it. |
| EP1OUT | rw | 2 | 1'b0 | Interrupt status register bit for the EP1 OUT direction. This bit will be set if the corresponding Active bit is cleared by HW. This is done in case the programmed NBytes transitions to zero or the skip bit is set by software. If the IntOnNAK\_AO is set, this bit will also be set when a NAK is transmitted for the EP1 OUT direction. Software can clear this bit by writing a one to it. |
| EP1IN | rw | 3 | 1'b0 | Interrupt status register bit for the EP1 IN direction. This bit will be set if the corresponding Active bit is cleared by HW. This is done in case the programmed NBytes transitions to zero or the skip bit is set by software. If the IntOnNAK\_AI is set, this bit will also be set when a NAK is transmitted for the EP1 IN direction. Software can clear this bit by writing a one to it. |
| EP2OUT | rw | 4 | 1'b0 | Interrupt status register bit for the EP2 OUT direction. This bit will be set if the corresponding Active bit is cleared by HW. This is done in case the programmed NBytes transitions to zero or the skip bit is set by software. If the IntOnNAK\_AO is set, this bit will also be set when a NAK is transmitted for the EP2 OUT direction. Software can clear this bit by writing a one to it. |
| EP2IN | rw | 5 | 1'b0 | Interrupt status register bit for the EP2 IN direction. This bit will be set if the corresponding Active bit is cleared by HW. This is done in case the programmed NBytes transitions to zero or the skip bit is set by software. If the IntOnNAK\_AI is set, this bit will also be set when a NAK is transmitted for the EP2 IN direction. Software can clear this bit by writing a one to it. |
| EP3OUT | rw | 6 | 1'b0 | Interrupt status register bit for the EP3 OUT direction. This bit will be set if the corresponding Active bit is cleared by HW. This is done in case the programmed NBytes transitions to zero or the skip bit is set by software. If the IntOnNAK\_AO is set, this bit will also be set when a NAK is transmitted for the EP3 OUT direction. Software can clear this bit by writing a one to it. |
| EP3IN | rw | 7 | 1'b0 | Interrupt status register bit for the EP3 IN direction. This bit will be set if the corresponding Active bit is cleared by HW. This is done in case the programmed NBytes transitions to zero or the skip bit is set by software. If the IntOnNAK\_AI is set, this bit will also be set when a NAK is transmitted for the EP3 IN direction. Software can clear this bit by writing a one to it. |
| EP4OUT | rw | 8 | 1'b0 | Interrupt status register bit for the EP4 OUT direction. This bit will be set if the corresponding Active bit is cleared by HW. This is done in case the programmed NBytes transitions to zero or the skip bit is set by software. If the IntOnNAK\_AO is set, this bit will also be set when a NAK is transmitted for the EP4 OUT direction. Software can clear this bit by writing a one to it. |
| EP4IN | rw | 9 | 1'b0 | Interrupt status register bit for the EP4 IN direction. This bit will be set if the corresponding Active bit is cleared by HW. This is done in case the programmed NBytes transitions to zero or the skip bit is set by software. If the IntOnNAK\_AI is set, this bit will also be set when a NAK is transmitted for the EP4 IN direction. Software can clear this bit by writing a one to it. |
| EP5OUT | rw | 10 | 1'b0 | Interrupt status register bit for the EP5 OUT direction. This bit will be set if the corresponding Active bit is cleared by HW. This is done in case the programmed NBytes transitions to zero or the skip bit is set by software. If the IntOnNAK\_AO is set, this bit will also be set when a NAK is transmitted for the EP5 OUT direction. Software can clear this bit by writing a one to it. |
| EP5IN | rw | 11 | 1'b0 | Interrupt status register bit for the EP5 IN direction. This bit will be set if the corresponding Active bit is cleared by HW. This is done in case the programmed NBytes transitions to zero or the skip bit is set by software. If the IntOnNAK\_AI is set, this bit will also be set when a NAK is transmitted for the EP5 IN direction. Software can clear this bit by writing a one to it. |
| EP6OUT | rw | 12 | 1'b0 | Interrupt status register bit for the EP6 OUT direction. This bit will be set if the corresponding Active bit is cleared by HW. This is done in case the programmed NBytes transitions to zero or the skip bit is set by software. If the IntOnNAK\_AO is set, this bit will also be set when a NAK is transmitted for the EP6 OUT direction. Software can clear this bit by writing a one to it. |
| EP6IN | rw | 13 | 1'b0 | Interrupt status register bit for the EP6 IN direction. This bit will be set if the corresponding Active bit is cleared by HW. This is done in case the programmed NBytes transitions to zero or the skip bit is set by software. If the IntOnNAK\_AI is set, this bit will also be set when a NAK is transmitted for the EP6 IN direction. Software can clear this bit by writing a one to it. |
| EP7OUT | rw | 14 | 1'b0 | Interrupt status register bit for the EP7 OUT direction. This bit will be set if the corresponding Active bit is cleared by HW. This is done in case the programmed NBytes transitions to zero or the skip bit is set by software. If the IntOnNAK\_AO is set, this bit will also be set when a NAK is transmitted for the EP7 OUT direction. Software can clear this bit by writing a one to it. |
| EP7IN | rw | 15 | 1'b0 | Interrupt status register bit for the EP7 IN direction. This bit will be set if the corresponding Active bit is cleared by HW. This is done in case the programmed NBytes transitions to zero or the skip bit is set by software. If the IntOnNAK\_AI is set, this bit will also be set when a NAK is transmitted for the EP7 IN direction. Software can clear this bit by writing a one to it. |
| Reserved | rw | 29:16 | 14'b0 | Reserved |
| FRAME\_INT | rw | 30 | 1'b0 | Frame interrupt. This bit is set to one every millisecond when the VbusDebounced bit and the DCON bit are set. This bit can be used by software when handling isochronous endpoints. Software can clear this bit by writing a one to it. |
| DEV\_INT | rw | 31 | 1'b0 | Device status interrupt. This bit is set by HW when one of the bits in the Device Status Change register are set. Software can clear this bit by writing a one to it. |

### USB0\_INTEN

Offset Address: 0x40084024

USB interrupt enable register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| EP\_INT\_EN | rw | 15:0 | 16'b0 | If this bit is set and the corresponding USB interrupt status bit is set, a HW interrupt is generated on the interrupt line indicated by the corresponding USB interrupt routing bit. |
| Reserved | rw | 29:16 | 14'b0 | Reserved |
| FRAME\_INT\_EN | rw | 30 | 1'b0 | If this bit is set and the corresponding USB interrupt status bit is set, a HW interrupt is generated on the interrupt line indicated by the corresponding USB interrupt routing bit. |
| DEV\_INT\_EN | rw | 31 | 1'b0 | If this bit is set and the corresponding USB interrupt status bit is set, a HW interrupt is generated on the interrupt line indicated by the corresponding USB interrupt routing bit. |

### USB0\_INTSETSTAT

Offset Address: 0x40084028

USB set interrupt status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| EP\_SET\_INT | rw | 15:0 | 16'b0 | If software writes a one to one of these bits, the corresponding USB interrupt status bit is set. When this register is read, the same value as the USB interrupt status register is returned. |
| Reserved | rw | 29:16 | 14'b0 | Reserved |
| FRAME\_SET\_INT | rw | 30 | 1'b0 | If software writes a one to one of these bits, the corresponding USB interrupt status bit is set. When this register is read, the same value as the USB interrupt status register is returned. |
| DEV\_SET\_INT | rw | 31 | 1'b0 | If software writes a one to one of these bits, the corresponding USB interrupt status bit is set. When this register is read, the same value as the USB interrupt status register is returned. |

### USB0\_EPTOGGLE

Offset Address: 0x40084034

USB Endpoint toggle register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TOGGLE | rw | 15:0 | 16'b0 | Endpoint data toggle: This field indicates the current value of the data toggle for the corresponding endpoint. |
| Reserved | rw | 31:16 | 16'b0 | Reserved |

### SCT0\_CONFIG

Offset Address: 0x40085000

SCT configuration register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| UNIFY | rw | 0 | 1'b0 | SCT operation |
| CLKMODE | rw | 2:1 | 2'b0 | SCT clock mode |
| CKSEL | rw | 6:3 | 4'b0 | SCT clock select. The specific functionality of the designated input/edge is dependent on the CLKMODE bit selection in this register. |
| NORELAOD\_L | rw | 7 | 1'b0 | A 1 in this bit prevents the lower match registers from being reloaded from their respective reload registers. Setting this bit eliminates the need to write to the reload registers MATCHREL if the match values are fixed. Software can write to set or clear this bit at any time. This bit applies to both the higher and lower registers when the UNIFY bit is set. |
| NORELOAD\_H | rw | 8 | 1'b0 | A 1 in this bit prevents the higher match registers from being reloaded from their respective reload registers. Setting this bit eliminates the need to write to the reload registers MATCHREL if the match values are fixed. Software can write to set or clear this bit at any time. This bit is not used when the UNIFY bit is set. |
| INSYNC | rw | 12:9 | 4'b0 | Synchronization for input N (bit 9 = input 0, bit 10 = input 1,, bit 12 = input 3); all other bits are reserved. A 1 in one of these bits subjects the corresponding input to synchronization to the SCT clock, before it is used to create an event. If an input is known to already be synchronous to the SCT clock, this bit may be set to 0 for faster input response. (Note: The SCT clock is the system clock for CKMODEs 0-2. It is the selected, asynchronous SCT input clock for CKMODE3). Note that the INSYNC field only affects inputs used for event generation. It does not apply to the clock input specified in the CKSEL field. |
| Reserved | rw | 16:13 | 4'b0 | Reserved |
| AUTOLIMIT\_L | rw | 17 | 1'b0 | A one in this bit causes a match on match register 0 to be treated as a de-facto LIMIT condition without the need to define an associated event. As with any LIMIT event, this automatic limit causes the counter to be cleared to zero in unidirectional mode or to change the direction of count in bi-directional mode. Software can write to set or clear this bit at any time. This bit applies to both the higher and lower registers when the UNIFY bit is set. |
| AUTOLIMIT\_H | rw | 18 | 1'b0 | A one in this bit will cause a match on match register 0 to be treated as a de-facto LIMIT condition without the need to define an associated event. As with any LIMIT event, this automatic limit causes the counter to be cleared to zero in unidirectional mode or to change the direction of count in bi-directional mode. Software can write to set or clear this bit at any time. This bit is not used when the UNIFY bit is set. |
| Reserved | rw | 31:19 | 13'b0 | Reserved |

### SCT0\_CTRL

Offset Address: 0x40085004

SCT control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DOWN\_L | rw | 0 | 1'b0 | This bit is 1 when the L or unified counter is counting down. Hardware sets this bit when the counter is counting up, counter limit occurs, and BIDIR = 1.Hardware clears this bit when the counter is counting down and a limit condition occurs or when the counter reaches 0. |
| STOP\_L | rw | 1 | 1'b0 | When this bit is 1 and HALT is 0, the L or unified counter does not run, but I/O events related to the counter can occur. If a designated start event occurs, this bit is cleared and counting resumes. |
| HALT\_L | rw | 2 | 1'b0 | When this bit is 1, the L or unified counter does not run and no events can occur. A reset sets this bit. When the HALT\_L bit is one, the STOP\_L bit is cleared. It is possible to remove the halt condition while keeping the SCT in the stop condition (not running) with a single write to this register to simultaneously clear the HALT bit and set the STOP bit. Once set, only software can clear this bit to restore counter operation. This bit is set on reset. |
| CLRCTR\_L | rw | 3 | 1'b0 | Writing a 1 to this bit clears the L or unified counter. This bit always reads as 0. |
| BIDIR\_L | rw | 4 | 1'b0 | L or unified counter direction select |
| PRE\_L | rw | 12:5 | 8'b0 | Specifies the factor by which the SCT clock is prescaled to produce the L or unified counter clock. The counter clock is clocked at the rate of the SCT clock divided by PRE\_L+1. Clear the counter (by writing a 1 to the CLRCTR bit) whenever changing the PRE value. |
| Reserved | rw | 15:13 | 3'b0 | Reserved |
| DOWN\_H | rw | 16 | 1'b0 | This bit is 1 when the H counter is counting down. Hardware sets this bit when the counter is counting, a counter limit condition occurs, and BIDIR is 1. Hardware clears this bit when the counter is counting down and a limit condition occurs or when the counter reaches 0. |
| STOP\_H | rw | 17 | 1'b0 | When this bit is 1 and HALT is 0, the H counter does not, run but I/O events related to the counter can occur. If such an event matches the mask in the Start register, this bit is cleared and counting resumes. |
| HALT\_H | rw | 18 | 1'b0 | When this bit is 1, the H counter does not run and no events can occur. A reset sets this bit. When the HALT\_H bit is one, the STOP\_H bit is cleared. It is possible to remove the halt condition while keeping the SCT in the stop condition (not running) with a single write to this register to simultaneously clear the HALT bit and set the STOP bit. Once set, this bit can only be cleared by software to restore counter operation. This bit is set on reset. |
| CLRCTR\_H | rw | 19 | 1'b0 | Writing a 1 to this bit clears the H counter. This bit always reads as 0. |
| BIDIR\_H | rw | 20 | 1'b0 | Direction select |
| PRE\_H | rw | 28:21 | 8'b0 | Specifies the factor by which the SCT clock is prescaled to produce the H counter clock. The counter clock is clocked at the rate of the SCT clock divided by PRELH+1. Clear the counter (by writing a 1 to the CLRCTR bit) whenever changing the PRE value. |
| Reserved | rw | 31:29 | 3'b0 | Reserved |

### SCT0\_LIMIT

Offset Address: 0x40085008

SCT limit event select register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| LIMMSK\_L | rw | 15:0 | 16'b0 | If bit n is one, event n is used as a counter limit for the L or unified counter (event 0 = bit 0, event 1 = bit 1, etc.). The number of bits = number of events in this SCT. |
| LIMMSK\_H | rw | 31:16 | 16'b0 | If bit n is one, event n is used as a counter limit for the H counter (event 0 = bit 16, event 1 = bit 17, etc.). The number of bits = number of events in this SCT. |

### SCT0\_HALT

Offset Address: 0x4008500c

SCT halt event select register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| HALTMSK\_L | rw | 15:0 | 16'b0 | If bit n is one, event n sets the HALT\_L bit in the CTRL register (event 0 = bit 0, event 1 = bit 1, etc.). The number of bits = number of events in this SCT. |
| HALTMSK\_H | rw | 31:16 | 16'b0 | If bit n is one, event n sets the HALT\_H bit in the CTRL register (event 0 = bit 16, event 1 = bit 17, etc.). The number of bits = number of events in this SCT. |

### SCT0\_STOP

Offset Address: 0x40085010

SCT stop event select register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| STOPMSK\_L | rw | 15:0 | 16'b0 | If bit n is one, event n sets the STOP\_L bit in the CTRL register (event 0 = bit 0, event 1 = bit 1, etc.). The number of bits = number of events in this SCT. |
| STOPMSK\_H | rw | 31:16 | 16'b0 | If bit n is one, event n sets the STOP\_H bit in the CTRL register (event 0 = bit 16, event 1 = bit 17, etc.). The number of bits = number of events in this SCT. |

### SCT0\_START

Offset Address: 0x40085014

SCT start event select register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| STARTMSK\_L | rw | 15:0 | 16'b0 | If bit n is one, event n clears the STOP\_L bit in the CTRL register (event 0 = bit 0, event 1 = bit 1, etc.). The number of bits = number of events in this SCT. |
| STARTMSK\_H | rw | 31:16 | 16'b0 | If bit n is one, event n clears the STOP\_H bit in the CTRL register (event 0 = bit 16, event 1 = bit 17, etc.). The number of bits = number of events in this SCT. |

### SCT0\_COUNT

Offset Address: 0x40085040

SCT counter register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CTR\_L | rw | 15:0 | 16'b0 | When UNIFY = 0, read or write the 16-bit L counter value. When UNIFY = 1, read or write the lower 16 bits of the 32-bit unified counter. |
| CTR\_H | rw | 31:16 | 16'b0 | When UNIFY = 0, read or write the 16-bit H counter value. When UNIFY = 1, read or write the upper 16 bits of the 32-bit unified counter. |

### SCT0\_STATE

Offset Address: 0x40085044

SCT state register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| STATE\_L | rw | 4:0 | 5'b0 | State variable. |
| Reserved | rw | 15:5 | 11'b0 | Reserved |
| STATE\_H | rw | 20:16 | 5'b0 | State variable. |
| Reserved | rw | 31:21 | 11'b0 | Reserved |

### SCT0\_INPUT

Offset Address: 0x40085048

SCT input register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| AIN0 | rw | 0 | 1'b0 | Input 0 state. Input 0 state on the last SCT clock edge. |
| AIN1 | rw | 1 | 1'b0 | Input 1 state. Input 1 state on the last SCT clock edge. |
| AIN2 | rw | 2 | 1'b0 | Input 2 state. Input 2 state on the last SCT clock edge. |
| AIN3 | rw | 3 | 1'b0 | Input 3 state. Input 3 state on the last SCT clock edge. |
| AIN4 | rw | 4 | 1'b0 | Input 4 state. Input 4 state on the last SCT clock edge. |
| AIN5 | rw | 5 | 1'b0 | Input 5 state. Input 5 state on the last SCT clock edge. |
| AIN6 | rw | 6 | 1'b0 | Input 6 state. Input 6 state on the last SCT clock edge. |
| AIN7 | rw | 7 | 1'b0 | Input 7 state. Input 7 state on the last SCT clock edge. |
| AIN8 | rw | 8 | 1'b0 | Input 8 state. Input 8 state on the last SCT clock edge. |
| AIN9 | rw | 9 | 1'b0 | Input 9 state. Input 9 state on the last SCT clock edge. |
| AIN10 | rw | 10 | 1'b0 | Input 10 state. Input 10 state on the last SCT clock edge. |
| AIN11 | rw | 11 | 1'b0 | Input 11 state. Input 11 state on the last SCT clock edge. |
| AIN12 | rw | 12 | 1'b0 | Input 12 state. Input 12 state on the last SCT clock edge. |
| AIN13 | rw | 13 | 1'b0 | Input 13 state. Input 13 state on the last SCT clock edge. |
| AIN14 | rw | 14 | 1'b0 | Input 14 state. Input 14 state on the last SCT clock edge. |
| AIN15 | rw | 15 | 1'b0 | Input 15 state. Input 15 state on the last SCT clock edge. |
| SIN0 | rw | 16 | 1'b0 | Input 0 state. Input 0 state following the synchronization specified by INSYNC. |
| SIN1 | rw | 17 | 1'b0 | Input 1 state. Input 1 state following the synchronization specified by INSYNC. |
| SIN2 | rw | 18 | 1'b0 | Input 2 state. Input 2 state following the synchronization specified by INSYNC. |
| SIN3 | rw | 19 | 1'b0 | Input 3 state. Input 3 state following the synchronization specified by INSYNC. |
| SIN4 | rw | 20 | 1'b0 | Input 4 state. Input 4 state following the synchronization specified by INSYNC. |
| SIN5 | rw | 21 | 1'b0 | Input 5 state. Input 5 state following the synchronization specified by INSYNC. |
| SIN6 | rw | 22 | 1'b0 | Input 6 state. Input 6 state following the synchronization specified by INSYNC. |
| SIN7 | rw | 23 | 1'b0 | Input 7 state. Input 7 state following the synchronization specified by INSYNC. |
| SIN8 | rw | 24 | 1'b0 | Input 8 state. Input 8 state following the synchronization specified by INSYNC. |
| SIN9 | rw | 25 | 1'b0 | Input 9 state. Input 9 state following the synchronization specified by INSYNC. |
| SIN10 | rw | 26 | 1'b0 | Input 10 state. Input 10 state following the synchronization specified by INSYNC. |
| SIN11 | rw | 27 | 1'b0 | Input 11 state. Input 11 state following the synchronization specified by INSYNC. |
| SIN12 | rw | 28 | 1'b0 | Input 12 state. Input 12 state following the synchronization specified by INSYNC. |
| SIN13 | rw | 29 | 1'b0 | Input 13 state. Input 13 state following the synchronization specified by INSYNC. |
| SIN14 | rw | 30 | 1'b0 | Input 14 state. Input 14 state following the synchronization specified by INSYNC. |
| SIN15 | rw | 31 | 1'b0 | Input 15 state. Input 15 state following the synchronization specified by INSYNC. |

### SCT0\_REGMODE

Offset Address: 0x4008504c

SCT match/capture mode register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| REGMOD\_L | rw | 15:0 | 16'b0 | Each bit controls one match/capture register (register 0 = bit 0, register 1 = bit 1, etc.). The number of bits = number of match/captures in this SCT. 0 = register operates as match register. 1 = register operates as capture register. |
| REGMOD\_H | rw | 31:16 | 16'b0 | Each bit controls one match/capture register (register 0 = bit 16, register 1 = bit 17, etc.). The number of bits = number of match/captures in this SCT. 0 = register operates as match registers. 1 = register operates as capture registers. |

### SCT0\_OUTPUT

Offset Address: 0x40085050

SCT output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| OUT | rw | 15:0 | 16'b0 | Writing a 1 to bit n forces the corresponding output HIGH. Writing a 0 forces the corresponding output LOW (output 0 = bit 0, output 1 = bit 1, etc.). The number of bits = number of outputs in this SCT. |
| Reserved | rw | 31:16 | 16'b0 | Reserved |

### SCT0\_OUTPUTDIRCTRL

Offset Address: 0x40085054

SCT output counter direction control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SETCLR0 | rw | 1:0 | 2'b0 | Set/clear operation on output 0. Value 0x3 is reserved. Do not program this value. |
| SETCLR1 | rw | 3:2 | 2'b0 | Set/clear operation on output 1. Value 0x3 is reserved. Do not program this value. |
| SETCLR2 | rw | 5:4 | 2'b0 | Set/clear operation on output 2. Value 0x3 is reserved. Do not program this value. |
| SETCLR3 | rw | 7:6 | 2'b0 | Set/clear operation on output 3. Value 0x3 is reserved. Do not program this value. |
| SETCLR4 | rw | 9:8 | 2'b0 | Set/clear operation on output 4. Value 0x3 is reserved. Do not program this value. |
| SETCLR5 | rw | 11:10 | 2'b0 | Set/clear operation on output 5. Value 0x3 is reserved. Do not program this value. |
| SETCLR6 | rw | 13:12 | 2'b0 | Set/clear operation on output 6. Value 0x3 is reserved. Do not program this value. |
| SETCLR7 | rw | 15:14 | 2'b0 | Set/clear operation on output 7. Value 0x3 is reserved. Do not program this value. |
| SETCLR8 | rw | 17:16 | 2'b0 | Set/clear operation on output 8. Value 0x3 is reserved. Do not program this value. |
| SETCLR9 | rw | 19:18 | 2'b0 | Set/clear operation on output 9. Value 0x3 is reserved. Do not program this value. |
| SETCLR10 | rw | 21:20 | 2'b0 | Set/clear operation on output 10. Value 0x3 is reserved. Do not program this value. |
| SETCLR11 | rw | 23:22 | 2'b0 | Set/clear operation on output 11. Value 0x3 is reserved. Do not program this value. |
| SETCLR12 | rw | 25:24 | 2'b0 | Set/clear operation on output 12. Value 0x3 is reserved. Do not program this value. |
| SETCLR13 | rw | 27:26 | 2'b0 | Set/clear operation on output 13. Value 0x3 is reserved. Do not program this value. |
| SETCLR14 | rw | 29:28 | 2'b0 | Set/clear operation on output 14. Value 0x3 is reserved. Do not program this value. |
| SETCLR15 | rw | 31:30 | 2'b0 | Set/clear operation on output 15. Value 0x3 is reserved. Do not program this value. |

### SCT0\_RES

Offset Address: 0x40085058

SCT conflict resolution register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MO0RES | rw | 1:0 | 2'b0 | Effect of simultaneous set and clear on output 0. |
| MO1RES | rw | 3:2 | 2'b0 | Effect of simultaneous set and clear on output 1. |
| MO2RES | rw | 5:4 | 2'b0 | Effect of simultaneous set and clear on output 2. |
| MO3RES | rw | 7:6 | 2'b0 | Effect of simultaneous set and clear on output 3. |
| MO4RES | rw | 9:8 | 2'b0 | Effect of simultaneous set and clear on output 4. |
| MO5RES | rw | 11:10 | 2'b0 | Effect of simultaneous set and clear on output 5. |
| MO6RES | rw | 13:12 | 2'b0 | Effect of simultaneous set and clear on output 6. |
| MO7RES | rw | 15:14 | 2'b0 | Effect of simultaneous set and clear on output 7. |
| MO8RES | rw | 17:16 | 2'b0 | Effect of simultaneous set and clear on output 8. |
| MO9RES | rw | 19:18 | 2'b0 | Effect of simultaneous set and clear on output 9. |
| MO10RES | rw | 21:20 | 2'b0 | Effect of simultaneous set and clear on output 10. |
| MO11RES | rw | 23:22 | 2'b0 | Effect of simultaneous set and clear on output 11. |
| MO12RES | rw | 25:24 | 2'b0 | Effect of simultaneous set and clear on output 12. |
| MO13RES | rw | 27:26 | 2'b0 | Effect of simultaneous set and clear on output 13. |
| MO14RES | rw | 29:28 | 2'b0 | Effect of simultaneous set and clear on output 14. |
| MO15RES | rw | 31:30 | 2'b0 | Effect of simultaneous set and clear on output 15. |

### SCT0\_DMA0REQUEST

Offset Address: 0x4008505c

SCT DMA request 0 register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DEV\_0 | rw | 15:0 | 16'b0 | If bit n is one, event n triggers DMA request 0 (event 0 = bit 0, event 1 = bit 1, etc.). The number of bits = number of events in this SCT. |
| Reserved | rw | 29:16 | 14'b0 | Reserved |
| DRL0 | rw | 30 | 1'b0 | A 1 in this bit triggers DMA request 0 when it loads the MATCH\_L/Unified registers from the RELOAD\_L/Unified registers. |
| DRQ0 | rw | 31 | 1'b0 | This read-only bit indicates the state of DMA Request 0. Note that if the related DMA channel is enabled and properly set up, it is unlikely that software will see this flag, it will be cleared rapidly by the DMA service. The flag remaining set could point to an issue with DMA setup. |

### SCT0\_DMA1REQUEST

Offset Address: 0x40085060

SCT DMA request 1 register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DEV\_1 | rw | 15:0 | 16'b0 | If bit n is one, event n triggers DMA request 1 (event 0 = bit 0, event 1 = bit 1, etc.). The number of bits = number of events in this SCT. |
| Reserved | rw | 29:16 | 14'b0 | Reserved |
| DRL1 | rw | 30 | 1'b0 | A 1 in this bit triggers DMA request 1 when it loads the Match L/Unified registers from the Reload L/Unified registers. |
| DRQ1 | rw | 31 | 1'b0 | This read-only bit indicates the state of DMA Request 1. Note that if the related DMA channel is enabled and properly set up, it is unlikely that software will see this flag, it will be cleared rapidly by the DMA service. The flag remaining set could point to an issue with DMA setup. |

### SCT0\_EVEN

Offset Address: 0x400850f0

SCT event interrupt enable register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| IEN | rw | 15:0 | 16'b0 | The SCT requests an interrupt when bit n of this register and the event flag register are both one (event 0 = bit 0, event 1 = bit 1, etc.). The number of bits = number of events in this SCT. |
| Reserved | rw | 31:16 | 16'b0 | Reserved |

### SCT0\_EVFLAG

Offset Address: 0x400850f4

SCT event flag register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FLAG | rw | 15:0 | 16'b0 | Bit n is one if event n has occurred since reset or a 1 was last written to this bit (event 0 = bit 0, event 1 = bit 1, etc.). The number of bits = number of events in this SCT. |
| Reserved | rw | 31:16 | 16'b0 | Reserved |

### SCT0\_CONEN

Offset Address: 0x400850f8

SCT conflict interrupt enable register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| NCEN | rw | 15:0 | 16'b0 | The SCT requests an interrupt when bit n of this register and the SCT conflict flag register are both one (output 0 = bit 0, output 1 = bit 1, etc.). The number of bits = number of outputs in this SCT. |
| Reserved | rw | 31:16 | 16'b0 | Reserved |

### SCT0\_CONFLAG

Offset Address: 0x400850fc

SCT conflict flag register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| NCFLAG | rw | 15:0 | 16'b0 | Bit n is one if a no-change conflict event occurred on output n since reset or a 1 was last written to this bit (output 0 = bit 0, output 1 = bit 1, etc.). The number of bits = number of outputs in this SCT. |
| Reserved | rw | 29:16 | 14'b0 | Reserved |
| BUSERRL | rw | 30 | 1'b0 | The most recent bus error from this SCT involved writing CTR L/Unified, STATE L/Unified, MATCH L/Unified, or the Output register when the L/U counter was not halted. A word write to certain L and H registers can be half successful and half unsuccessful. |
| BUSERRH | rw | 31 | 1'b0 | The most recent bus error from this SCT involved writing CTR H, STATE H, MATCH H, or the Output register when the H counter was not halted. |

### SCT0\_SCTCAPs

Offset Address: 0x40085100

SCT capture register of capture channel

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CAPn\_L | rw | 15:0 | 16'b0 | When UNIFY = 0, read the 16-bit counter value at which this register was last captured. When UNIFY = 1, read the lower 16 bits of the 32-bit value at which this register was last captured. |
| CAPn\_H | rw | 31:16 | 16'b0 | When UNIFY = 0, read the 16-bit counter value at which this register was last captured. When UNIFY = 1, read the upper 16 bits of the 32-bit value at which this register was last captured. |

### SCT0\_SCTMATCHs

Offset Address: 0x40085100

SCT match value register of match channels

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MATCHn\_L | rw | 15:0 | 16'b0 | When UNIFY = 0, read or write the 16-bit value to be compared to the L counter. When UNIFY = 1, read or write the lower 16 bits of the 32-bit value to be compared to the unified counter. |
| MATCHn\_H | rw | 31:16 | 16'b0 | When UNIFY = 0, read or write the 16-bit value to be compared to the H counter. When UNIFY = 1, read or write the upper 16 bits of the 32-bit value to be compared to the unified counter. |

### SCT0\_SCTCAPCTRLs

Offset Address: 0x40085200

SCT capture control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CAPCONn\_L | rw | 15:0 | 16'b0 | If bit m is one, event m causes the CAPn\_L (UNIFY = 0) or the CAPn (UNIFY = 1) register to be loaded (event 0 = bit 0, event 1 = bit 1, etc.). The number of bits = number of match/captures in this SCT. |
| CAPCONn\_H | rw | 31:16 | 16'b0 | If bit m is one, event m causes the CAPn\_H (UNIFY = 0) register to be loaded (event 0 = bit 16, event 1 = bit 17, etc.). The number of bits = number of match/captures in this SCT. |

### SCT0\_SCTMATCHRELs

Offset Address: 0x40085200

SCT match reload value register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| RELOADn\_L | rw | 15:0 | 16'b0 | When UNIFY = 0, specifies the 16-bit value to be loaded into the MATCHn\_L register. When UNIFY = 1, specifies the lower 16 bits of the 32-bit value to be loaded into the MATCHn register. |
| RELOADn\_H | rw | 31:16 | 16'b0 | When UNIFY = 0, specifies the 16-bit to be loaded into the MATCHn\_H register. When UNIFY = 1, specifies the upper 16 bits of the 32-bit value to be loaded into the MATCHn register. |

### SCT0\_MODULECONTENT

Offset Address: 0x400857fc

Reserved

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |

### MI2C0\_CFG

Offset Address: 0x40086800

Configuration for shared functions.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MSTEN | rw | 0 | 1'b0 | Master Enable. When disabled, configurations settings for the Master function are not changed, but the Master function is internally reset. |
| SLVEN | rw | 1 | 1'b0 | Slave Enable. When disabled, configurations settings for the Slave function are not changed, but the Slave function is internally reset. |
| MONEN | rw | 2 | 1'b0 | Monitor Enable. When disabled, configurations settings for the Monitor function are not changed, but the Monitor function is internally reset. |
| TIMEOUTEN | rw | 3 | 1'b0 | I2C bus Time-out Enable. When disabled, the time-out function is internally reset. |
| MONCLKSTR | rw | 4 | 1'b0 | Monitor function Clock Stretching. |
| Reserved | rw | 31:5 | 27'b0 | Reserved |

### MI2C0\_STAT

Offset Address: 0x40086804

Status register for Master, Slave, and Monitor functions.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MSTPENDING | rw | 0 | 1'b0 | Master Pending. Indicates that the Master is waiting to continue communication on the I2C-bus (pending) or is idle. When the master is pending, the MSTSTATE bits indicate what type of software service if any the master expects. This flag will cause an interrupt when set if, enabled via the INTENSET register. The MSTPENDING flag is not set when the DMA is handling an event (if the MSTDMA bit in the MSTCTL register is set). If the master is in the idle state, and no communication is needed, mask this interrupt. |
| MSTSTATE | rw | 3:1 | 3'b0 | Master State code. The master state code reflects the master state when the MSTPENDING bit is set, that is the master is pending or in the idle state. Each value of this field indicates a specific required service for the Master function. All other values are reserved. See Table 400 for details of state values and appropriate responses. |
| MSTARBLOSS | rw | 4 | 1'b0 | Master Arbitration Loss flag. This flag can be cleared by software writing a 1 to this bit. It is also cleared automatically a 1 is written to MSTCONTINUE. |
| Reserved | rw | 5 | 1'b0 | Reserved |
| MSTSTSTPERR | rw | 6 | 1'b0 | Master Start/Stop Error flag. This flag can be cleared by software writing a 1 to this bit. It is also cleared automatically a 1 is written to MSTCONTINUE. |
| Reserved | rw | 7 | 1'b0 | Reserved |
| SLVPENDING | rw | 8 | 1'b0 | Slave Pending. Indicates that the Slave function is waiting to continue communication on the I2C-bus and needs software service. This flag will cause an interrupt when set if enabled via INTENSET. The SLVPENDING flag is not set when the DMA is handling an event (if the SLVDMA bit in the SLVCTL register is set). The SLVPENDING flag is read-only and is automatically cleared when a 1 is written to the SLVCONTINUE bit in the SLVCTL register. The point in time when SlvPending is set depends on whether the I2C interface is in HSCAPABLE mode. See Section 25.7.2.2.2. When the I2C interface is configured to be HSCAPABLE, HS master codes are detected automatically. Due to the requirements of the HS I2C specification, slave addresses must also be detected automatically, since the address must be acknowledged before the clock can be stretched. |
| SLVSTATE | rw | 10:9 | 2'b0 | Slave State code. Each value of this field indicates a specific required service for the Slave function. All other values are reserved. See Table 401 for state values and actions. note that the occurrence of some states and how they are handled are affected by DMA mode and Automatic Operation modes. |
| SLVNOTSTR | rw | 11 | 1'b0 | Slave Not Stretching. Indicates when the slave function is stretching the I2C clock. This is needed in order to gracefully invoke Deep Sleep or Power-down modes during slave operation. This read-only flag reflects the slave function status in real time. |
| SLVIDX | rw | 13:12 | 2'b0 | Slave address match Index. This field is valid when the I2C slave function has been selected by receiving an address that matches one of the slave addresses defined by any enabled slave address registers, and provides an identification of the address that was matched. It is possible that more than one address could be matched, but only one match can be reported here. |
| SLVSEL | rw | 14 | 1'b0 | Slave selected flag. SLVSEL is set after an address match when software tells the Slave function to acknowledge the address, or when the address has been automatically acknowledged. It is cleared when another address cycle presents an address that does not match an enabled address on the Slave function, when slave software decides to NACK a matched address, when there is a Stop detected on the bus, when the master NACKs slave data, and in some combinations of Automatic Operation. SLVSEL is not cleared if software NACKs data. |
| SLVDESEL | rw | 15 | 1'b0 | Slave Deselected flag. This flag will cause an interrupt when set if enabled via INTENSET. This flag can be cleared by writing a 1 to this bit. |
| MONRDY | rw | 16 | 1'b0 | Monitor Ready. This flag is cleared when the MONRXDAT register is read. |
| MONOV | rw | 17 | 1'b0 | Monitor Overflow flag. |
| MONACTIVE | rw | 18 | 1'b0 | Monitor Active flag. Indicates when the Monitor function considers the I 2C bus to be active. Active is defined here as when some Master is on the bus: a bus Start has occurred more recently than a bus Stop. |
| MONIDLE | rw | 19 | 1'b0 | Monitor Idle flag. This flag is set when the Monitor function sees the I2C bus change from active to inactive. This can be used by software to decide when to process data accumulated by the Monitor function. This flag will cause an interrupt when set if enabled via the INTENSET register. The flag can be cleared by writing a 1 to this bit. |
| Reserved | rw | 23:20 | 4'b0 | Reserved |
| EVENTTIMEOUT | rw | 24 | 1'b0 | Event Time-out Interrupt flag. Indicates when the time between events has been longer than the time specified by the TIMEOUT register. Events include Start, Stop, and clock edges. The flag is cleared by writing a 1 to this bit. No time-out is created when the I2C-bus is idle. |
| SCLTIMEOUT | rw | 25 | 1'b0 | SCL Time-out Interrupt flag. Indicates when SCL has remained low longer than the time specific by the TIMEOUT register. The flag is cleared by writing a 1 to this bit. |
| Reserved | rw | 31:26 | 6'b0 | Reserved |

### MI2C0\_INTENSET

Offset Address: 0x40086808

Interrupt Enable Set and read register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MSTPENDINGEN | rw | 0 | 1'b0 | Master Pending interrupt Enable. |
| Reserved | rw | 3:1 | 3'b0 | Reserved |
| MSTARBLOSSEN | rw | 4 | 1'b0 | Master Arbitration Loss interrupt Enable. |
| Reserved | rw | 5 | 1'b0 | Reserved |
| MSTSTSTPERREN | rw | 6 | 1'b0 | Master Start/Stop Error interrupt Enable. |
| Reserved | rw | 7 | 1'b0 | Reserved |
| SLVPENDINGEN | rw | 8 | 1'b0 | Slave Pending interrupt Enable. |
| Reserved | rw | 10:9 | 2'b0 | Reserved |
| SLVNOTSTREN | rw | 11 | 1'b0 | Slave Not Stretching interrupt Enable. |
| Reserved | rw | 14:12 | 3'b0 | Reserved |
| SLVDESELEN | rw | 15 | 1'b0 | Slave Deselect interrupt Enable. |
| MONRDYEN | rw | 16 | 1'b0 | Monitor data Ready interrupt Enable. |
| MONOVEN | rw | 17 | 1'b0 | Monitor Overrun interrupt Enable. |
| Reserved | rw | 18 | 1'b0 | Reserved |
| MONIDLEEN | rw | 19 | 1'b0 | Monitor Idle interrupt Enable. |
| Reserved | rw | 23:20 | 4'b0 | Reserved |
| EVENTTIMEOUTEN | rw | 24 | 1'b0 | Event time-out interrupt Enable. |
| SCLTIMEOUTEN | rw | 25 | 1'b0 | SCL time-out interrupt Enable. |
| Reserved | rw | 31:26 | 6'b0 | Reserved |

### MI2C0\_INTENCLR

Offset Address: 0x4008680c

Interrupt Enable Clear register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MSTPENDINGCLR | rw | 0 | 1'b0 | Master Pending interrupt clear. Writing 1 to this bit clears the corresponding bit in the INTENSET register if implemented. |
| Reserved | rw | 3:1 | 3'b0 | Reserved |
| MSTARBLOSSCLR | rw | 4 | 1'b0 | Master Arbitration Loss interrupt clear. |
| Reserved | rw | 5 | 1'b0 | Reserved |
| MSTSTSTPERRCLR | rw | 6 | 1'b0 | Master Start/Stop Error interrupt clear. |
| Reserved | rw | 7 | 1'b0 | Reserved |
| SLVPENDINGCLR | rw | 8 | 1'b0 | Slave Pending interrupt clear. |
| Reserved | rw | 10:9 | 2'b0 | Reserved |
| SLVNOTSTRCLR | rw | 11 | 1'b0 | Slave Not Stretching interrupt clear. |
| Reserved | rw | 14:12 | 3'b0 | Reserved |
| SLVDESELCLR | rw | 15 | 1'b0 | Slave Deselect interrupt clear. |
| MONRDYCLR | rw | 16 | 1'b0 | Monitor data Ready interrupt clear. |
| MONOVCLR | rw | 17 | 1'b0 | Monitor Overrun interrupt clear. |
| Reserved | rw | 18 | 1'b0 | Reserved |
| MONIDLECLR | rw | 19 | 1'b0 | Monitor Idle interrupt clear. |
| Reserved | rw | 23:20 | 4'b0 | Reserved |
| EVENTTIMEOUTCLR | rw | 24 | 1'b0 | Event time-out interrupt clear. |
| SCLTIMEOUTCLR | rw | 25 | 1'b0 | SCL time-out interrupt clear. |
| Reserved | rw | 31:26 | 6'b0 | Reserved |

### MI2C0\_TIMEOUT

Offset Address: 0x40086810

Time-out value register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TOMIN | rw | 3:0 | 4'b0 | Time-out time value, bottom four bits. These are hard-wired to 0xF. This gives a minimum time-out of 16 I2C function clocks and also a time-out resolution of 16 I2C function clocks. |
| TO | rw | 15:4 | 12'b0 | Time-out time value. Specifies the time-out interval value in increments of 16 I 2C function clocks, as defined by the CLKDIV register. To change this value while I2C is in operation, disable all time-outs, write a new value to TIMEOUT, then re-enable time-outs. 0x000 = A time-out will occur after 16 counts of the I2C function clock. 0x001 = A time-out will occur after 32 counts of the I2C function clock. 0xFFF = A time-out will occur after 65,536 counts of the I2C function clock. |
| Reserved | rw | 31:16 | 16'b0 | Reserved |

### MI2C0\_CLKDIV

Offset Address: 0x40086814

Clock pre-divider for the entire I2C interface. This determines what time increments are used for the MSTTIME register, and controls some timing of the Slave function.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DIVVAL | rw | 15:0 | 16'b0 | This field controls how the Flexcomm clock (FCLK) is used by the I2C functions that need an internal clock in order to operate. 0x0000 = FCLK is used directly by the I2C. 0x0001 = FCLK is divided by 2 before use. 0x0002 = FCLK is divided by 3 before use. 0xFFFF = FCLK is divided by 65,536 before use. |
| Reserved | rw | 31:16 | 16'b0 | Reserved |

### MI2C0\_INTSTAT

Offset Address: 0x40086818

Interrupt Status register for Master, Slave, and Monitor functions.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MSTPENDING | rw | 0 | 1'b0 | Master Pending. |
| Reserved | rw | 3:1 | 3'b0 | Reserved |
| MSTARBLOSS | rw | 4 | 1'b0 | Master Arbitration Loss flag. |
| Reserved | rw | 5 | 1'b0 | Reserved |
| MSTSTSTPERR | rw | 6 | 1'b0 | Master Start/Stop Error flag. |
| Reserved | rw | 7 | 1'b0 | Reserved |
| SLVPENDING | rw | 8 | 1'b0 | Slave Pending. |
| Reserved | rw | 10:9 | 2'b0 | Reserved |
| SLVNOTSTR | rw | 11 | 1'b0 | Slave Not Stretching status. |
| Reserved | rw | 14:12 | 3'b0 | Reserved |
| SLVDESEL | rw | 15 | 1'b0 | Slave Deselected flag. |
| MONRDY | rw | 16 | 1'b0 | Monitor Ready. |
| MONOV | rw | 17 | 1'b0 | Monitor Overflow flag. |
| Reserved | rw | 18 | 1'b0 | Reserved |
| MONIDLE | rw | 19 | 1'b0 | Monitor Idle flag. |
| Reserved | rw | 23:20 | 4'b0 | Reserved |
| EVENTTIMEOUT | rw | 24 | 1'b0 | Event time-out Interrupt flag. |
| SCLTIMEOUT | rw | 25 | 1'b0 | SCL time-out Interrupt flag. |
| Reserved | rw | 31:26 | 6'b0 | Reserved |

### MI2C0\_MSTCTL

Offset Address: 0x40086820

Master control register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MSTCONTINUE | rw | 0 | 1'b0 | Master Continue. This bit is write-only. |
| MSTSTART | rw | 1 | 1'b0 | Master Start control. This bit is write-only. |
| MSTSTOP | rw | 2 | 1'b0 | Master Stop control. This bit is write-only. |
| MSTDMA | rw | 3 | 1'b0 | Master DMA enable. Data operations of the I2C can be performed with DMA. Protocol type operations such as Start, address, Stop, and address match must always be done with software, typically via an interrupt. Address acknowledgement must also be done by software except when the I2C is configured to be HSCAPABLE (and address acknowledgement is handled entirely by hardware) or when Automatic Operation is enabled. When a DMA data transfer is complete, MSTDMA must be cleared prior to beginning the next operation, typically a Start or Stop.This bit is read/write. |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### MI2C0\_MSTTIME

Offset Address: 0x40086824

Master timing configuration.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MSTSCLLOW | rw | 2:0 | 3'b0 | Master SCL Low time. Specifies the minimum low time that will be asserted by this master on SCL. Other devices on the bus (masters or slaves) could lengthen this time. This corresponds to the parameter t LOW in the I2C bus specification. I2C bus specification parameters tBUF and tSU;STA have the same values and are also controlled by MSTSCLLOW. |
| Reserved | rw | 3 | 1'b0 | Reserved |
| MSTSCLHIGH | rw | 6:4 | 3'b0 | Master SCL High time. Specifies the minimum high time that will be asserted by this master on SCL. Other masters in a multi-master system could shorten this time. This corresponds to the parameter tHIGH in the I2C bus specification. I2C bus specification parameters tSU;STO and tHD;STA have the same values and are also controlled by MSTSCLHIGH. |
| Reserved | rw | 31:7 | 25'b0 | Reserved |

### MI2C0\_MSTDAT

Offset Address: 0x40086828

Combined Master receiver and transmitter data register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DATA | rw | 7:0 | 8'b0 | Master function data register. Read: read the most recently received data for the Master function. Write: transmit data using the Master function. |
| Reserved | rw | 31:8 | 24'b0 | Reserved |

### MI2C0\_SLVCTL

Offset Address: 0x40086840

Slave control register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SLVCONTINUE | rw | 0 | 1'b0 | Slave Continue. |
| SLVNACK | rw | 1 | 1'b0 | Slave NACK. |
| Reserved | rw | 2 | 1'b0 | Reserved |
| SLVDMA | rw | 3 | 1'b0 | Slave DMA enable. |
| Reserved | rw | 7:4 | 4'b0 | Reserved |
| AUTOACK | rw | 8 | 1'b0 | Automatic Acknowledge.When this bit is set, it will cause an I2C header which matches SLVADR0 and the direction set by AUTOMATCHREAD to be ACKed immediately; this is used with DMA to allow processing of the data without intervention. If this bit is clear and a header matches SLVADR0, the behavior is controlled by AUTONACK in the SLVADR0 register: allowing NACK or interrupt. |
| AUTOMATCHREAD | rw | 9 | 1'b0 | When AUTOACK is set, this bit controls whether it matches a read or write request on the next header with an address matching SLVADR0. Since DMA needs to be configured to match the transfer direction, the direction needs to be specified. This bit allows a direction to be chosen for the next operation. |
| Reserved | rw | 31:10 | 22'b0 | Reserved |

### MI2C0\_SLVDAT

Offset Address: 0x40086844

Combined Slave receiver and transmitter data register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DATA | rw | 7:0 | 8'b0 | Slave function data register. Read: read the most recently received data for the Slave function. Write: transmit data using the Slave function. |
| Reserved | rw | 31:8 | 24'b0 | Reserved |

### MI2C0\_SLVADRs

Offset Address: 0x40086848

Slave address register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SADISABLE | rw | 0 | 1'b0 | Slave Address n Disable. |
| SLVADR | rw | 7:1 | 7'b0 | Slave Address. Seven bit slave address that is compared to received addresses if enabled. |
| Reserved | rw | 14:8 | 7'b0 | Reserved |
| AUTONACK | rw | 15 | 1'b0 | Automatic NACK operation. Used in conjunction with AUTOACK and AUTOMATCHREAD, allows software to ignore I2C traffic while handling previous I2C data or other operations. |
| Reserved | rw | 31:16 | 16'b0 | Reserved |

### MI2C0\_SLVQUAL0

Offset Address: 0x40086858

Slave Qualification for address 0.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| QUALMODE0 | rw | 0 | 1'b0 | Qualify mode for slave address 0. |
| SLVQUAL0 | rw | 7:1 | 7'b0 | Slave address Qualifier for address 0. A value of 0 causes the address in SLVADR0 to be used as-is, assuming that it is enabled. If QUALMODE0 = 0, any bit in this field which is set to 1 will cause an automatic match of the corresponding bit of the received address when it is compared to the SLVADR0 register. If QUALMODE0 = 1, an address range is matched for address 0. This range extends from the value defined by SLVADR0 to the address defined by SLVQUAL0 (address matches when SLVADR0[7:1] &amp;lt;= received address &amp;lt;= SLVQUAL0[7:1]). |
| Reserved | rw | 31:8 | 24'b0 | Reserved |

### MI2C0\_MONRXDAT

Offset Address: 0x40086880

Monitor receiver data register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MONRXDAT | rw | 7:0 | 8'b0 | Monitor function Receiver Data. This reflects every data byte that passes on the I2C pins. |
| MONSTART | rw | 8 | 1'b0 | Monitor Received Start. |
| MONRESTART | rw | 9 | 1'b0 | Monitor Received Repeated Start. |
| MONNACK | rw | 10 | 1'b0 | Monitor Received NACK. |
| Reserved | rw | 31:11 | 21'b0 | Reserved |

### MI2C0\_ID

Offset Address: 0x40086ffc

I2C module Identification. This value appears in the shared Flexcomm peripheral ID register when I2C is selected.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| APERTURE | rw | 7:0 | 8'b0 | Aperture: encoded as (aperture size/4K) -1, so 0x00 means a 4K aperture. |
| MINOR\_REV | rw | 11:8 | 4'b0 | Minor revision of module implementation, starting at 0. Minor revision of module implementation, starting at 0. Software compatibility is expected between minor revisions. |
| MAJOR\_REV | rw | 15:12 | 4'b0 | Major revision of module implementation, starting at 0. There may not be software compatibility between major revisions. |
| ID | rw | 31:16 | 16'b0 | Unique module identifier for this IP block. |

### SPI0\_CFG

Offset Address: 0x40087400

SPI Configuration register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ENABLE | rw | 0 | 1'b0 | SPI enable. |
| Reserved | rw | 1 | 1'b0 | Reserved |
| MASTER | rw | 2 | 1'b0 | Master mode select. |
| LSBF | rw | 3 | 1'b0 | LSB First mode enable. |
| CPHA | rw | 4 | 1'b0 | Clock Phase select. |
| CPOL | rw | 5 | 1'b0 | Clock Polarity select. |
| Reserved | rw | 6 | 1'b0 | Reserved |
| LOOP | rw | 7 | 1'b0 | Loopback mode enable. Loopback mode applies only to Master mode, and connects transmit and receive data connected together to allow simple software testing. |
| SPOL0 | rw | 8 | 1'b0 | SSEL0 Polarity select. |
| SPOL1 | rw | 9 | 1'b0 | SSEL1 Polarity select. |
| SPOL2 | rw | 10 | 1'b0 | SSEL2 Polarity select. |
| SPOL3 | rw | 11 | 1'b0 | SSEL3 Polarity select. |
| Reserved | rw | 31:12 | 20'b0 | Reserved |

### SPI0\_DLY

Offset Address: 0x40087404

SPI Delay register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| PRE\_DELAY | rw | 3:0 | 4'b0 | Controls the amount of time between SSEL assertion and the beginning of a data transfer. There is always one SPI clock time between SSEL assertion and the first clock edge. This is not considered part of the pre-delay. 0x0 = No additional time is inserted. 0x1 = 1 SPI clock time is inserted. 0x2 = 2 SPI clock times are inserted. 0xF = 15 SPI clock times are inserted. |
| POST\_DELAY | rw | 7:4 | 4'b0 | Controls the amount of time between the end of a data transfer and SSEL deassertion. 0x0 = No additional time is inserted. 0x1 = 1 SPI clock time is inserted. 0x2 = 2 SPI clock times are inserted. 0xF = 15 SPI clock times are inserted. |
| FRAME\_DELAY | rw | 11:8 | 4'b0 | If the EOF flag is set, controls the minimum amount of time between the current frame and the next frame (or SSEL deassertion if EOT). 0x0 = No additional time is inserted. 0x1 = 1 SPI clock time is inserted. 0x2 = 2 SPI clock times are inserted. 0xF = 15 SPI clock times are inserted. |
| TRANSFER\_DELAY | rw | 15:12 | 4'b0 | Controls the minimum amount of time that the SSEL is deasserted between transfers. 0x0 = The minimum time that SSEL is deasserted is 1 SPI clock time. (Zero added time.) 0x1 = The minimum time that SSEL is deasserted is 2 SPI clock times. 0x2 = The minimum time that SSEL is deasserted is 3 SPI clock times. 0xF = The minimum time that SSEL is deasserted is 16 SPI clock times. |
| Reserved | rw | 31:16 | 16'b0 | Reserved |

### SPI0\_STAT

Offset Address: 0x40087408

SPI Status. Some status flags can be cleared by writing a 1 to that bit position.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 3:0 | 4'b0 | Reserved |
| SSA | rw | 4 | 1'b0 | Slave Select Assert. This flag is set whenever any slave select transitions from deasserted to asserted, in both master and slave modes. This allows determining when the SPI transmit/receive functions become busy, and allows waking up the device from reduced power modes when a slave mode access begins. This flag is cleared by software. |
| SSD | rw | 5 | 1'b0 | Slave Select Deassert. This flag is set whenever any asserted slave selects transition to deasserted, in both master and slave modes. This allows determining when the SPI transmit/receive functions become idle. This flag is cleared by software. |
| STALLED | rw | 6 | 1'b0 | Stalled status flag. This indicates whether the SPI is currently in a stall condition. |
| ENDTRANSFER | rw | 7 | 1'b0 | End Transfer control bit. Software can set this bit to force an end to the current transfer when the transmitter finishes any activity already in progress, as if the EOT flag had been set prior to the last transmission. This capability is included to support cases where it is not known when transmit data is written that it will be the end of a transfer. The bit is cleared when the transmitter becomes idle as the transfer comes to an end. Forcing an end of transfer in this manner causes any specified FRAME\_DELAY and TRANSFER\_DELAY to be inserted. |
| MSTIDLE | rw | 8 | 1'b0 | Master idle status flag. This bit is 1 whenever the SPI master function is fully idle. This means that the transmit holding register is empty and the transmitter is not in the process of sending data. |
| Reserved | rw | 31:9 | 23'b0 | Reserved |

### SPI0\_INTENSET

Offset Address: 0x4008740c

SPI Interrupt Enable read and Set. A complete value may be read from this register. Writing a 1 to any implemented bit position causes that bit to be set.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 3:0 | 4'b0 | Reserved |
| SSAEN | rw | 4 | 1'b0 | Slave select assert interrupt enable. Determines whether an interrupt occurs when the Slave Select is asserted. |
| SSDEN | rw | 5 | 1'b0 | Slave select deassert interrupt enable. Determines whether an interrupt occurs when the Slave Select is deasserted. |
| Reserved | rw | 7:6 | 2'b0 | Reserved |
| MSTIDLEEN | rw | 8 | 1'b0 | Master idle interrupt enable. |
| Reserved | rw | 31:9 | 23'b0 | Reserved |

### SPI0\_INTENCLR

Offset Address: 0x40087410

SPI Interrupt Enable Clear. Writing a 1 to any implemented bit position causes the corresponding bit in INTENSET to be cleared.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 3:0 | 4'b0 | Reserved |
| SSAEN | rw | 4 | 1'b0 | Writing 1 clears the corresponding bit in the INTENSET register. |
| SSDEN | rw | 5 | 1'b0 | Writing 1 clears the corresponding bit in the INTENSET register. |
| Reserved | rw | 7:6 | 2'b0 | Reserved |
| MSTIDLE | rw | 8 | 1'b0 | Writing 1 clears the corresponding bit in the INTENSET register. |
| Reserved | rw | 31:9 | 23'b0 | Reserved |

### SPI0\_DIV

Offset Address: 0x40087424

SPI clock Divider

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DIVVAL | rw | 15:0 | 16'b0 | Rate divider value. Specifies how the Flexcomm clock (FCLK) is divided to produce the SPI clock rate in master mode. DIVVAL is -1 encoded such that the value 0 results in FCLK/1, the value 1 results in FCLK/2, up to the maximum possible divide value of 0xFFFF, which results in FCLK/65536. |
| Reserved | rw | 31:16 | 16'b0 | Reserved |

### SPI0\_INTSTAT

Offset Address: 0x40087428

SPI Interrupt Status

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 3:0 | 4'b0 | Reserved |
| SSA | rw | 4 | 1'b0 | Slave Select Assert. |
| SSD | rw | 5 | 1'b0 | Slave Select Deassert. |
| Reserved | rw | 7:6 | 2'b0 | Reserved |
| MSTIDLE | rw | 8 | 1'b0 | Master Idle status flag. |
| Reserved | rw | 31:9 | 23'b0 | Reserved |

### SPI0\_FIFOCFG

Offset Address: 0x40087e00

FIFO configuration and enable register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| ENABLETX | rw | 0 | 1'b0 | Enable the transmit FIFO. |
| ENABLERX | rw | 1 | 1'b0 | Enable the receive FIFO. |
| Reserved | rw | 3:2 | 2'b0 | Reserved |
| SIZE | rw | 5:4 | 2'b0 | FIFO size configuration. This is a read-only field. 0x1 = FIFO is configured as 8 entries of 16 bits. 0x0, 0x2, 0x3 = not applicable to SPI. |
| Reserved | rw | 11:6 | 6'b0 | Reserved |
| DMATX | rw | 12 | 1'b0 | DMA configuration for transmit. |
| DMARX | rw | 13 | 1'b0 | DMA configuration for receive. |
| Reserved | rw | 15:14 | 2'b0 | Reserved |
| EMPTYTX | rw | 16 | 1'b0 | Empty command for the transmit FIFO. When a 1 is written to this bit, the TX FIFO is emptied. |
| EMPTYRX | rw | 17 | 1'b0 | Empty command for the receive FIFO. When a 1 is written to this bit, the RX FIFO is emptied. |
| Reserved | rw | 31:18 | 14'b0 | Reserved |

### SPI0\_FIFOSTAT

Offset Address: 0x40087e04

FIFO status register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TXERR | rw | 0 | 1'b0 | TX FIFO error. Will be set if a transmit FIFO error occurs. This could be an overflow caused by pushing data into a full FIFO, or by an underflow if the FIFO is empty when data is needed. Cleared by writing a 1 to this bit. |
| RXERR | rw | 1 | 1'b0 | RX FIFO error. Will be set if a receive FIFO overflow occurs, caused by software or DMA not emptying the FIFO fast enough. Cleared by writing a 1 to this bit. |
| Reserved | rw | 2 | 1'b0 | Reserved |
| PERINT | rw | 3 | 1'b0 | Peripheral interrupt. When 1, this indicates that the peripheral function has asserted an interrupt. The details can be found by reading the peripheral' STAT register. |
| TXEMPTY | rw | 4 | 1'b0 | Transmit FIFO empty. When 1, the transmit FIFO is empty. The peripheral may still be processing the last piece of data. |
| TXNOTFULL | rw | 5 | 1'b0 | Transmit FIFO not full. When 1, the transmit FIFO is not full, so more data can be written. When 0, the transmit FIFO is full and another write would cause it to overflow. |
| RXNOTEMPTY | rw | 6 | 1'b0 | Receive FIFO not empty. When 1, the receive FIFO is not empty, so data can be read. When 0, the receive FIFO is empty. |
| RXFULL | rw | 7 | 1'b0 | Receive FIFO full. When 1, the receive FIFO is full. Data needs to be read out to prevent the peripheral from causing an overflow. |
| TXLVL | rw | 12:8 | 5'b0 | Transmit FIFO current level. A 0 means the TX FIFO is currently empty, and the TXEMPTY and TXNOTFULL flags will be 1. Other values tell how much data is actually in the TX FIFO at the point where the read occurs. If the TX FIFO is full, the TXEMPTY and TXNOTFULL flags will be 0. |
| Reserved | rw | 15:13 | 3'b0 | Reserved |
| RXLVL | rw | 20:16 | 5'b0 | Receive FIFO current level. A 0 means the RX FIFO is currently empty, and the RXFULL and RXNOTEMPTY flags will be 0. Other values tell how much data is actually in the RX FIFO at the point where the read occurs. If the RX FIFO is full, the RXFULL and RXNOTEMPTY flags will be 1. |
| Reserved | rw | 31:21 | 11'b0 | Reserved |

### SPI0\_FIFOTRIG

Offset Address: 0x40087e08

FIFO trigger settings for interrupt and DMA request.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TXLVLENA | rw | 0 | 1'b0 | Transmit FIFO level trigger enable. This trigger will become an interrupt if enabled in FIFOINTENSET, or a DMA trigger if DMATX in FIFOCFG is set. |
| RXLVLENA | rw | 1 | 1'b0 | Receive FIFO level trigger enable. This trigger will become an interrupt if enabled in FIFOINTENSET, or a DMA trigger if DMARX in FIFOCFG is set. |
| Reserved | rw | 7:2 | 6'b0 | Reserved |
| TXLVL | rw | 11:8 | 4'b0 | Transmit FIFO level trigger point. This field is used only when TXLVLENA = 1. If enabled to do so, the FIFO level can wake up the device just enough to perform DMA, then return to the reduced power mode See -Hardware Wake-up control register-. 0 = trigger when the TX FIFO becomes empty. 1 = trigger when the TX FIFO level decreases to one entry. 7 = 1 = trigger when the TX FIFO level decreases to 7 entries (is no longer full). |
| Reserved | rw | 15:12 | 4'b0 | Reserved |
| RXLVL | rw | 19:16 | 4'b0 | Receive FIFO level trigger point. The RX FIFO level is checked when a new piece of data is received. This field is used only when RXLVLENA = 1. If enabled to do so, the FIFO level can wake up the device just enough to perform DMA, then return to the reduced power mode See -Hardware Wake-up control register-. 0 = trigger when the RX FIFO has received one entry (is no longer empty). 1 = trigger when the RX FIFO has received two entries. 7 = trigger when the RX FIFO has received 8 entries (has become full). |
| Reserved | rw | 31:20 | 12'b0 | Reserved |

### SPI0\_FIFOINTENSET

Offset Address: 0x40087e10

FIFO interrupt enable set (enable) and read register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TXERR | rw | 0 | 1'b0 | Determines whether an interrupt occurs when a transmit error occurs, based on the TXERR flag in the FIFOSTAT register. |
| RXERR | rw | 1 | 1'b0 | Determines whether an interrupt occurs when a receive error occurs, based on the RXERR flag in the FIFOSTAT register. |
| TXLVL | rw | 2 | 1'b0 | Determines whether an interrupt occurs when a the transmit FIFO reaches the level specified by the TXLVL field in the FIFOTRIG register. |
| RXLVL | rw | 3 | 1'b0 | Determines whether an interrupt occurs when a the receive FIFO reaches the level specified by the TXLVL field in the FIFOTRIG register. |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### SPI0\_FIFOINTENCLR

Offset Address: 0x40087e14

FIFO interrupt enable clear (disable) and read register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TXERR | rw | 0 | 1'b0 | Writing one clears the corresponding bits in the FIFOINTENSET register. |
| RXERR | rw | 1 | 1'b0 | Writing one clears the corresponding bits in the FIFOINTENSET register. |
| TXLVL | rw | 2 | 1'b0 | Writing one clears the corresponding bits in the FIFOINTENSET register. |
| RXLVL | rw | 3 | 1'b0 | Writing one clears the corresponding bits in the FIFOINTENSET register. |
| Reserved | rw | 31:4 | 28'b0 | Reserved |

### SPI0\_FIFOINTSTAT

Offset Address: 0x40087e18

FIFO interrupt status register.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TXERR | rw | 0 | 1'b0 | TX FIFO error. |
| RXERR | rw | 1 | 1'b0 | RX FIFO error. |
| TXLVL | rw | 2 | 1'b0 | Transmit FIFO level interrupt. |
| RXLVL | rw | 3 | 1'b0 | Receive FIFO level interrupt. |
| PERINT | rw | 4 | 1'b0 | Peripheral interrupt. |
| Reserved | rw | 31:5 | 27'b0 | Reserved |

### SPI0\_FIFOWR

Offset Address: 0x40087e20

FIFO write data.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TXDATA | rw | 15:0 | 16'b0 | Transmit data to the FIFO. |
| TXSSEL0\_N | rw | 16 | 1'b0 | Transmit Slave Select. This field asserts SSEL0 in master mode. The output on the pin is active LOW by default. Remark: The active state of the SSEL0 pin is configured by bits in the CFG register. |
| TXSSEL1\_N | rw | 17 | 1'b0 | Transmit Slave Select. This field asserts SSEL1 in master mode. The output on the pin is active LOW by default. Remark: The active state of the SSEL1 pin is configured by bits in the CFG register. |
| TXSSEL2\_N | rw | 18 | 1'b0 | Transmit Slave Select. This field asserts SSEL2 in master mode. The output on the pin is active LOW by default. Remark: The active state of the SSEL2 pin is configured by bits in the CFG register. |
| TXSSEL3\_N | rw | 19 | 1'b0 | Transmit Slave Select. This field asserts SSEL3 in master mode. The output on the pin is active LOW by default. Remark: The active state of the SSEL3 pin is configured by bits in the CFG register. |
| EOT | rw | 20 | 1'b0 | End of Transfer. The asserted SSEL will be deasserted at the end of a transfer, and remain so for at least the time specified by the Transfer\_delay value in the DLY register. |
| EOF | rw | 21 | 1'b0 | End of Frame. Between frames, a delay may be inserted, as defined by the FRAME\_DELAY value in the DLY register. The end of a frame may not be particularly meaningful if the FRAME\_DELAY value = 0. This control can be used as part of the support for frame lengths greater than 16 bits. |
| RXIGNORE | rw | 22 | 1'b0 | Receive Ignore. This allows data to be transmitted using the SPI without the need to read unneeded data from the receiver.Setting this bit simplifies the transmit process and can be used with the DMA. |
| Reserved | rw | 23 | 1'b0 | Reserved |
| LEN | rw | 27:24 | 4'b0 | Data Length. Specifies the data length from 1 to 16 bits. Note that transfer lengths greater than 16 bits are supported by implementing multiple sequential transmits. 0x0 = Data transfer is 1 bit in length. Note: when LEN = 0, the underrun status is not meaningful. 0x1 = Data transfer is 2 bits in length. 0x2 = Data transfer is 3 bits in length. 0xF = Data transfer is 16 bits in length. |
| Reserved | rw | 31:28 | 4'b0 | Reserved |

### SPI0\_FIFORD

Offset Address: 0x40087e30

FIFO read data.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| RXDATA | rw | 15:0 | 16'b0 | Received data from the FIFO. |
| RXSSEL0\_N | rw | 16 | 1'b0 | Slave Select for receive. This field allows the state of the SSEL0 pin to be saved along with received data. The value will reflect the SSEL0 pin for both master and slave operation. A zero indicates that a slave select is active. The actual polarity of each slave select pin is configured by the related SPOL bit in CFG. |
| RXSSEL1\_N | rw | 17 | 1'b0 | Slave Select for receive. This field allows the state of the SSEL1 pin to be saved along with received data. The value will reflect the SSEL1 pin for both master and slave operation. A zero indicates that a slave select is active. The actual polarity of each slave select pin is configured by the related SPOL bit in CFG. |
| RXSSEL2\_N | rw | 18 | 1'b0 | Slave Select for receive. This field allows the state of the SSEL2 pin to be saved along with received data. The value will reflect the SSEL2 pin for both master and slave operation. A zero indicates that a slave select is active. The actual polarity of each slave select pin is configured by the related SPOL bit in CFG. |
| RXSSEL3\_N | rw | 19 | 1'b0 | Slave Select for receive. This field allows the state of the SSEL3 pin to be saved along with received data. The value will reflect the SSEL3 pin for both master and slave operation. A zero indicates that a slave select is active. The actual polarity of each slave select pin is configured by the related SPOL bit in CFG. |
| SOT | rw | 20 | 1'b0 | Start of Transfer flag. This flag will be 1 if this is the first data after the SSELs went from deasserted to asserted (i.e., any previous transfer has ended). This information can be used to identify the first piece of data in cases where the transfer length is greater than 16 bit. |
| Reserved | rw | 31:21 | 11'b0 | Reserved |

### SPI0\_FIFORDNOPOP

Offset Address: 0x40087e40

FIFO data read with no FIFO pop.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| RXDATA | rw | 15:0 | 16'b0 | Received data from the FIFO. |
| RXSSEL0\_N | rw | 16 | 1'b0 | Slave Select for receive. This field allows the state of the SSEL0 pin to be saved along with received data. The value will reflect the SSEL0 pin for both master and slave operation. A zero indicates that a slave select is active. The actual polarity of each slave select pin is configured by the related SPOL bit in CFG. |
| RXSSEL1\_N | rw | 17 | 1'b0 | Slave Select for receive. This field allows the state of the SSEL1 pin to be saved along with received data. The value will reflect the SSEL1 pin for both master and slave operation. A zero indicates that a slave select is active. The actual polarity of each slave select pin is configured by the related SPOL bit in CFG. |
| RXSSEL2\_N | rw | 18 | 1'b0 | Slave Select for receive. This field allows the state of the SSEL2 pin to be saved along with received data. The value will reflect the SSEL2 pin for both master and slave operation. A zero indicates that a slave select is active. The actual polarity of each slave select pin is configured by the related SPOL bit in CFG. |
| RXSSEL3\_N | rw | 19 | 1'b0 | Slave Select for receive. This field allows the state of the SSEL3 pin to be saved along with received data. The value will reflect the SSEL3 pin for both master and slave operation. A zero indicates that a slave select is active. The actual polarity of each slave select pin is configured by the related SPOL bit in CFG. |
| SOT | rw | 20 | 1'b0 | Start of Transfer flag. This flag will be 1 if this is the first data after the SSELs went from deasserted to asserted (i.e., any previous transfer has ended). This information can be used to identify the first piece of data in cases where the transfer length is greater than 16 bit. |
| Reserved | rw | 31:21 | 11'b0 | Reserved |

### SPI0\_ID

Offset Address: 0x40087ffc

SPI module Identification. This value appears in the shared Flexcomm peripheral ID register when SPI is selected.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| APERTURE | rw | 7:0 | 8'b0 | Aperture: encoded as (aperture size/4K) -1, so 0x00 means a 4K aperture. |
| MINOR\_REV | rw | 11:8 | 4'b0 | Minor revision of module implementation, starting at 0. Minor revision of module implementation, starting at 0. Software compatibility is expected between minor revisions. |
| MAJOR\_REV | rw | 15:12 | 4'b0 | Major revision of module implementation, starting at 0. There may not be software compatibility between major revisions. |
| ID | rw | 31:16 | 16'b0 | Unique module identifier for this IP block. |

### FSP\_SYS\_CTRL

Offset Address: 0x40088000

FSP system control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TE\_ABORT | rw | 0 | 1'b0 | Transform Engine abort write 1 to abort |
| MOU\_ABORT | rw | 1 | 1'b0 | Matrix Operation Unit abort write 1 to abort |
| SCF\_ABORT | rw | 2 | 1'b0 | SE COR FIR abort write 1 to abort |
| Reserved | rw | 31:3 | 29'b0 | Reserved |

### FSP\_STATUS

Offset Address: 0x40088004

FSP status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FPU0\_BUSY | rw | 0 | 1'b0 | SE COR FIR is in processing busy |
| FPU1\_BUSY | rw | 1 | 1'b0 | TE MOU is in processing busy |
| FIR\_READY | rw | 2 | 1'b0 | FIR output buffer is not empty which is valid for read |
| Reserved | rw | 31:3 | 29'b0 | Reserved |

### FSP\_INT

Offset Address: 0x40088008

FSP interrupt register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TE\_DONE\_INT | rw | 0 | 1'b0 | Transform engine done interrupt |
| MOU\_DONE\_INT | rw | 1 | 1'b0 | Matrix operation unit done interrupt |
| SE\_DONE\_INT | rw | 2 | 1'b0 | Statistic engine done interrupt |
| COR\_DONE\_INT | rw | 3 | 1'b0 | Correlation done interrupt |
| Reserved | rw | 7:4 | 4'b0 | Reserved |
| FPU0\_CALC\_IN\_ERR\_INT | rw | 8 | 1'b0 | SE COR FIR calculation input data error interrupt |
| FPU0\_CALC\_OUT\_ERR\_INT | rw | 9 | 1'b0 | SE COR FIR calculation output data error interrupt |
| FPU0\_DIN\_OV\_INT | rw | 10 | 1'b0 | SE COR FIR input data overflow interrupt (always 0) |
| FPU0\_DOUT\_OV\_INT | rw | 11 | 1'b0 | SE COR FIR output data overflow interrupt |
| SINGULAR\_INT | rw | 12 | 1'b0 | MOU singular interrupt |
| Reserved | rw | 15:13 | 3'b0 | Reserved |
| FPU1\_CALC\_IN\_ERR\_INT | rw | 16 | 1'b0 | MOU TE calculation input data error interrupt |
| FPU1\_CALC\_OUT\_ERR\_INT | rw | 17 | 1'b0 | MOU TE calculation output data error interrupt |
| FPU1\_DIN\_OV\_INT | rw | 18 | 1'b0 | MOU TE input data overflow interrupt |
| FPU1\_DOUT\_OV\_INT | rw | 19 | 1'b0 | MOU TE output data overflow interrupt |
| FINV\_DIN\_ERR\_INT | rw | 20 | 1'b0 | FINV input data is inf or nan |
| FINV\_DOUT\_OV\_INT | rw | 21 | 1'b0 | FINV output data overflow |
| FINV\_ZERO\_INT | rw | 22 | 1'b0 | FINV input data is zero |
| Reserved | rw | 23 | 1'b0 | Reserved |
| CORDIC\_DIN\_ERR | rw | 24 | 1'b0 | CORDIC input data error interrupt |
| CORDIC\_DOUT\_ERR\_INT | rw | 25 | 1'b0 | CORDIC output data error interrupt |
| CORDIC\_CALC\_ERR\_INT | rw | 26 | 1'b0 | CORDIC calculation error interrupt |
| Reserved | rw | 30:27 | 4'b0 | Reserved |
| FSP\_INT | rw | 31 | 1'b0 | Or signal of all FSP function interrupt in this register |

### FSP\_INTEN

Offset Address: 0x4008800c

FSP interrupt enable register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TE\_DONE\_INTEN | rw | 0 | 1'b0 | Transform engine done interrupt enable |
| MOU\_DONE\_INTEN | rw | 1 | 1'b0 | Matrix operation unit done interrupt enable |
| SE\_DONE\_INTEN | rw | 2 | 1'b0 | Statistic engine done interrupt enable |
| COR\_DONE\_INTEN | rw | 3 | 1'b0 | Correlation done interrupt enable |
| Reserved | rw | 7:4 | 4'b0 | Reserved |
| FPU0\_CALC\_IN\_ERR\_INTEN | rw | 8 | 1'b0 | SE COR FIR calculation input data error interrupt enable |
| FPU0\_CALC\_OUT\_ERR\_INTEN | rw | 9 | 1'b0 | SE COR FIR calculation output data error interrupt enable |
| FPU0\_DIN\_OV\_INTEN | rw | 10 | 1'b0 | SE COR FIR input data overflow interrupt enable |
| FPU0\_DOUT\_OV\_INTEN | rw | 11 | 1'b0 | SE COR FIR output data overflow interrupt enable |
| SINGULAR\_INTEN | rw | 12 | 1'b0 | MOU singular interrupt enable |
| Reserved | rw | 15:13 | 3'b0 | Reserved |
| FPU1\_CALC\_IN\_ERR\_INTEN | rw | 16 | 1'b0 | MOU TE calculation input data error interrupt enable |
| FPU1\_CALC\_OUT\_ERR\_INTEN | rw | 17 | 1'b0 | MOU TE calculation output data error interrupt enable |
| FPU1\_DIN\_OV\_INTEN | rw | 18 | 1'b0 | MOU TE input data overflow interrupt enable |
| FPU1\_DOUT\_OV\_INTEN | rw | 19 | 1'b0 | MOU TE output data overflow interrupt enable |
| FINV\_DIN\_ERR\_INTEN | rw | 20 | 1'b0 | FINV data input is inf or nan interrupt enable |
| FINV\_DOUT\_OV\_INTEN | rw | 21 | 1'b0 | FINV data output overflow interrupt enable |
| FINV\_ZERO\_INTEN | rw | 22 | 1'b0 | FINV input is zero interrupt enable |
| Reserved | rw | 23 | 1'b0 | Reserved |
| CORDIC\_DIN\_ERR\_INTEN | rw | 24 | 1'b0 | CORDIC input data error interrupt enable |
| CORDIC\_DOUT\_ERR\_INTEN | rw | 25 | 1'b0 | CORDIC output data error interrupt enable |
| CORDIC\_CALC\_ERR\_INTEN | rw | 26 | 1'b0 | CORDIC calculation error interrupt enable |
| Reserved | rw | 30:27 | 4'b0 | Reserved |
| FSP\_INTEN | rw | 31 | 1'b0 | Or signal of all FSP function interrupt in this register enable |

### FSP\_TE\_CTRL

Offset Address: 0x40088020

transmit engine control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TE\_MODE | rw | 1:0 | 2'b0 | TE compute mode |
| TE\_IO\_MODE | rw | 3:2 | 2'b0 | TE input &amp; output mode select |
| TE\_PTS | rw | 5:4 | 2'b0 | TE compute point |
| TE\_DIN\_FP\_SEL | rw | 6 | 1'b0 | TE input data format select |
| TE\_DOUT\_FP\_SEL | rw | 7 | 1'b0 | TE output data format select |
| TE\_SCALE | rw | 15:8 | 8'b0 | TE scale |
| Reserved | rw | 23:16 | 8'b0 | Reserved |
| TE\_PAUSE\_LVL | rw | 26:24 | 3'b0 | Transfer Engine stop level for debug use only. |
| Reserved | rw | 31:27 | 5'b0 | Reserved |

### FSP\_TE\_SRC\_BASE

Offset Address: 0x40088024

transfer engine source data memory base register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TE\_SRC\_BASE | rw | 16:0 | 17'b0 | TE source data memory base address |
| Reserved | rw | 31:17 | 15'b0 | Reserved |

### FSP\_TE\_DST\_BASE

Offset Address: 0x40088028

transfer engine destination data memory base register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| TE\_DST\_BASE | rw | 16:0 | 17'b0 | TE destination data memory base address |
| Reserved | rw | 31:17 | 15'b0 | Reserved |

### FSP\_MOU\_CTRL

Offset Address: 0x40088040

matrix operation unit control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| OP\_MODE | rw | 3:0 | 4'b0 | MOU operation mode |
| Reserved | rw | 7:4 | 4'b0 | Reserved |
| MOU\_DIN\_FP\_SEL | rw | 8 | 1'b0 | MOU data input format select |
| MOU\_DOUT\_FP\_SEL | rw | 9 | 1'b0 | MOU data output format select |
| Reserved | rw | 15:10 | 6'b0 | Reserved |
| MAT\_M | rw | 19:16 | 4'b0 | MOU Matrix column |
| MAT\_N | rw | 23:20 | 4'b0 | MOU Matrix row only valid when matrix's column is not equal to row |
| MAT\_K | rw | 27:24 | 4'b0 | MOU Matrix row only valid when matrix mult operation |
| DIV\_EPSILON | rw | 29:28 | 2'b0 | When the data exponent is small than DIV\_EPSILON the inverse operation will output a error signal. |
| LU\_STOP | rw | 30 | 1'b0 | Stop at LU |
| UINV\_STOP | rw | 31 | 1'b0 | stop at U-Matrix inverse |

### FSP\_MA\_SRC\_BASE

Offset Address: 0x40088044

matrix A source data memory base register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MA\_SRC\_BASE | rw | 16:0 | 17'b0 | Matrix A source data memory base address |
| Reserved | rw | 31:17 | 15'b0 | Reserved |

### FSP\_MB\_SRC\_BASE

Offset Address: 0x40088048

matrix B source data memory base register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MB\_SRC\_BASE | rw | 16:0 | 17'b0 | Matrix B source data memory base address |
| Reserved | rw | 31:17 | 15'b0 | Reserved |

### FSP\_MO\_DST\_BASE

Offset Address: 0x4008804c

matrix output data memory base register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MO\_DST\_BASE | rw | 16:0 | 17'b0 | Matrix Operation Unit output data destination memory base address |
| Reserved | rw | 31:17 | 15'b0 | Reserved |

### FSP\_MOU\_SCALEA

Offset Address: 0x40088050

scale coefficient A register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MOU\_SCALEA | rw | 31:0 | 32'b0 | MOU scale coefficient A |

### FSP\_MOU\_SCALEB

Offset Address: 0x40088054

scale coefficient B register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MOU\_SCALEB | rw | 31:0 | 32'b0 | MOU scale coefficient B |

### FSP\_SE\_CTRL

Offset Address: 0x40088060

stastic engine control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| MIN\_SEL | rw | 0 | 1'b0 | Minimum value selection |
| MAX\_SEL | rw | 1 | 1'b0 | Maximum value selection0 the first one1 the last one |
| MIN\_IDX\_EN | rw | 2 | 1'b0 | Minimum value index calculation enable |
| MAX\_IDX\_EN | rw | 3 | 1'b0 | Maximum value index calculation enable |
| SUM\_EN | rw | 4 | 1'b0 | Summary calculation enable |
| PWR\_EN | rw | 5 | 1'b0 | Power calculation enable |
| SE\_DIN\_FP\_SEL | rw | 6 | 1'b0 | SE data input format select |
| SE\_DOUT\_FP\_SEL | rw | 7 | 1'b0 | SE data output format select |
| Reserved | rw | 15:8 | 8'b0 | Reserved |
| SE\_LEN | rw | 23:16 | 8'b0 | Statistic engine length |
| Reserved | rw | 31:24 | 8'b0 | Reserved |

### FSP\_SE\_SRC\_BASE

Offset Address: 0x40088064

statistic engine source data base register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SE\_SRC\_BASE | rw | 16:0 | 17'b0 | Statistic engine source data base address |
| Reserved | rw | 31:17 | 15'b0 | Reserved |

### FSP\_SE\_IDX

Offset Address: 0x40088068

max or min data index register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SE\_MIN\_IDX | rw | 7:0 | 8'b0 | Minimum data index of an array |
| Reserved | rw | 15:8 | 8'b0 | Reserved |
| SE\_MAX\_IDX | rw | 23:16 | 8'b0 | Maximum data index of an array |
| Reserved | rw | 31:24 | 8'b0 | Reserved |

### FSP\_SE\_SUM

Offset Address: 0x4008806c

array summary result register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SE\_SUM | rw | 31:0 | 32'b0 | Summary of an array |

### FSP\_SE\_PWR

Offset Address: 0x40088070

array power result register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SE\_PWR | rw | 31:0 | 32'b0 | Power value of an array |

### FSP\_COR\_CTRL

Offset Address: 0x40088080

correlation control register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| Reserved | rw | 7:0 | 8'b0 | Reserved |
| COR\_DIN\_FP\_SEL | rw | 8 | 1'b0 | COR input data format select |
| COR\_DOUT\_FP\_SEL | rw | 9 | 1'b0 | COR output data format select |
| Reserved | rw | 15:10 | 6'b0 | Reserved |
| COR\_X\_LEN | rw | 23:16 | 8'b0 | The length of X sequence to be Correlator 0-255 |
| COR\_Y\_LEN | rw | 31:24 | 8'b0 | The length of Y sequence to be Correlator 0-255 |

### FSP\_CX\_SRC\_BASE

Offset Address: 0x40088084

correlation x sequence base register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| COR\_X\_ADDR | rw | 16:0 | 17'b0 | The base address of X sequence to be Correlator |
| Reserved | rw | 31:17 | 15'b0 | Reserved |

### FSP\_CY\_SRC\_BASE

Offset Address: 0x40088088

correlation y sequence base register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| COR\_Y\_ADDR | rw | 16:0 | 17'b0 | The base address of Y sequence to be Correlator |
| Reserved | rw | 31:17 | 15'b0 | Reserved |

### FSP\_CO\_DST\_BASE

Offset Address: 0x4008808c

correlation output sequence base register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| COR\_DST\_BASE | rw | 16:0 | 17'b0 | correlation output data destination address base |
| Reserved | rw | 31:17 | 15'b0 | Reserved |

### FSP\_COR\_OFFSET

Offset Address: 0x40088090

correlation offset register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| COR\_X\_OFFSET | rw | 7:0 | 8'b0 | COR input X SEQ offset 0-255 |
| COR\_Y\_OFFSET | rw | 15:8 | 8'b0 | COR input Y SEQ offset 0-255 |
| Reserved | rw | 31:16 | 16'b0 | Reserved |

### FSP\_FIR\_CFG\_CH0

Offset Address: 0x400880a0

FIR channel 0 configuration register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_CH0\_COEF\_BASE | rw | 15:0 | 16'b0 | FIR channel 0 coefficient base address |
| FIR\_CH0\_TAP\_LEN | rw | 19:16 | 4'b0 | FIR channel 0 tap length the register value equals to real tap length minus 1. |
| Reserved | rw | 29:20 | 10'b0 | Reserved |
| FIR\_BUF\_CLR\_ALL | rw | 30 | 1'b0 | clear all FIR buffer |
| FIR\_CH0\_BUF\_CLR | rw | 31 | 1'b0 | FIR channel 0 buffer clear |

### FSP\_FIR\_CFG\_CH1

Offset Address: 0x400880a4

FIR channel 1 configuration register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_CH1\_COEF\_BASE | rw | 15:0 | 16'b0 | FIR channel 1 coefficient base address |
| FIR\_CH1\_TAP\_LEN | rw | 19:16 | 4'b0 | FIR channel 1 tap length |
| Reserved | rw | 30:20 | 11'b0 | Reserved |
| FIR\_CH1\_BUF\_CLR | rw | 31 | 1'b0 | FIR channel 1 buffer clear |

### FSP\_FIR\_CFG\_CH2

Offset Address: 0x400880a8

FIR channel 2 configuration register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_CH2\_COEF\_BASE | rw | 15:0 | 16'b0 | FIR channel 2 coefficient base address |
| FIR\_CH2\_TAP\_LEN | rw | 19:16 | 4'b0 | FIR channel 2 tap length |
| Reserved | rw | 30:20 | 11'b0 | Reserved |
| FIR\_CH2\_BUF\_CLR | rw | 31 | 1'b0 | FIR channel 2 buffer clear |

### FSP\_FIR\_CFG\_CH3

Offset Address: 0x400880ac

FIR channel 3 configuration register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_CH3\_COEF\_BASE | rw | 15:0 | 16'b0 | FIR channel 3 coefficient base address |
| FIR\_CH3\_TAP\_LEN | rw | 19:16 | 4'b0 | FIR channel 3 tap length |
| Reserved | rw | 30:20 | 11'b0 | Reserved |
| FIR\_CH3\_BUF\_CLR | rw | 31 | 1'b0 | FIR channel 3 buffer clear |

### FSP\_FIR\_CFG\_CH4

Offset Address: 0x400880b0

FIR channel 4 configuration register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_CH4\_COEF\_BASE | rw | 15:0 | 16'b0 | FIR channel 4 coefficient base address |
| FIR\_CH4\_TAP\_LEN | rw | 19:16 | 4'b0 | FIR channel 4 tap length |
| Reserved | rw | 30:20 | 11'b0 | Reserved |
| FIR\_CH4\_BUF\_CLR | rw | 31 | 1'b0 | FIR channel 4 buffer clear |

### FSP\_FIR\_CFG\_CH5

Offset Address: 0x400880b4

FIR channel 5 configuration register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_CH5\_COEF\_BASE | rw | 15:0 | 16'b0 | FIR channel 5 coefficient base address |
| FIR\_CH5\_TAP\_LEN | rw | 19:16 | 4'b0 | FIR channel 5 tap length |
| Reserved | rw | 30:20 | 11'b0 | Reserved |
| FIR\_CH5\_BUF\_CLR | rw | 31 | 1'b0 | FIR channel 5 buffer clear |

### FSP\_FIR\_CFG\_CH6

Offset Address: 0x400880b8

FIR channel 6 configuration register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_CH6\_COEF\_BASE | rw | 15:0 | 16'b0 | FIR channel 6 coefficient base address |
| FIR\_CH6\_TAP\_LEN | rw | 19:16 | 4'b0 | FIR channel 6 tap length |
| Reserved | rw | 30:20 | 11'b0 | Reserved |
| FIR\_CH6\_BUF\_CLR | rw | 31 | 1'b0 | FIR channel 6 buffer clear |

### FSP\_FIR\_CFG\_CH7

Offset Address: 0x400880bc

FIR channel 7 configuration register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_CH7\_COEF\_BASE | rw | 15:0 | 16'b0 | FIR channel 7 coefficient base address |
| FIR\_CH7\_TAP\_LEN | rw | 19:16 | 4'b0 | FIR channel 7 tap length |
| Reserved | rw | 30:20 | 11'b0 | Reserved |
| FIR\_CH7\_BUF\_CLR | rw | 31 | 1'b0 | FIR channel 7 buffer clear |

### FSP\_FIR\_CFG\_CH8

Offset Address: 0x400880c0

FIR channel 8 configuration register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_CH8\_COEF\_BASE | rw | 15:0 | 16'b0 | FIR channel 8 coefficient base address |
| FIR\_CH8\_TAP\_LEN | rw | 19:16 | 4'b0 | FIR channel 8 tap length |
| Reserved | rw | 30:20 | 11'b0 | Reserved |
| FIR\_CH8\_BUF\_CLR | rw | 31 | 1'b0 | FIR channel 8 buffer clear |

### FSP\_FIR\_DAT0\_FX

Offset Address: 0x400880d0

FIR channel 0 fix point data input &amp; output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_DAT0\_FX | rw | 31:0 | 32'b0 | FIR channel 0 fix data |

### FSP\_FIR\_DAT1\_FX

Offset Address: 0x400880d4

FIR channel 1 fix point data input &amp; output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_DAT1\_FX | rw | 31:0 | 32'b0 | FIR channel1 fix data |

### FSP\_FIR\_DAT2\_FX

Offset Address: 0x400880d8

FIR channel 2 fix point data input &amp; output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_DAT2\_FX | rw | 31:0 | 32'b0 | FIR channel2 fix data |

### FSP\_FIR\_DAT3\_FX

Offset Address: 0x400880dc

FIR channel 3 fix point data input &amp; output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_DAT3\_FX | rw | 31:0 | 32'b0 | FIR channel3 fix data |

### FSP\_FIR\_DAT4\_FX

Offset Address: 0x400880e0

FIR channel 4 fix point data input &amp; output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_DAT4\_FX | rw | 31:0 | 32'b0 | FIR channel4 fix data |

### FSP\_FIR\_DAT5\_FX

Offset Address: 0x400880e4

FIR channel 5 fix point data input &amp; output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_DAT5\_FX | rw | 31:0 | 32'b0 | FIR channel5 fix data |

### FSP\_FIR\_DAT6\_FX

Offset Address: 0x400880e8

FIR channel 6 fix point data input &amp; output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_DAT6\_FX | rw | 31:0 | 32'b0 | FIR channel6 fix data |

### FSP\_FIR\_DAT7\_FX

Offset Address: 0x400880ec

FIR channel 7 fix point data input &amp; output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_DAT7\_FX | rw | 31:0 | 32'b0 | FIR channel7 fix data |

### FSP\_FIR\_DAT8\_FX

Offset Address: 0x400880f0

FIR channel 8 fix point data input &amp; output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_DAT8\_FX | rw | 31:0 | 32'b0 | FIR channel8 fix data |

### FSP\_FIR\_DAT0\_FL

Offset Address: 0x40088100

FIR channel 0 float point data input &amp; output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_DAT0\_FL | rw | 31:0 | 32'b0 | FIR channel 0 float data |

### FSP\_FIR\_DAT1\_FL

Offset Address: 0x40088104

FIR channel 1 float point data input &amp; output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_DAT1\_FL | rw | 31:0 | 32'b0 | FIR channel1 float data |

### FSP\_FIR\_DAT2\_FL

Offset Address: 0x40088108

FIR channel 2 float point data input &amp; output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_DAT2\_FL | rw | 31:0 | 32'b0 | FIR channel2 float data |

### FSP\_FIR\_DAT3\_FL

Offset Address: 0x4008810c

FIR channel 3 float point data input &amp; output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_DAT3\_FL | rw | 31:0 | 32'b0 | FIR channel3 float data |

### FSP\_FIR\_DAT4\_FL

Offset Address: 0x40088110

FIR channel 4 float point data input &amp; output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_DAT4\_FL | rw | 31:0 | 32'b0 | FIR channel4 float data |

### FSP\_FIR\_DAT5\_FL

Offset Address: 0x40088114

FIR channel 5 float point data input &amp; output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_DAT5\_FL | rw | 31:0 | 32'b0 | FIR channel5 float data |

### FSP\_FIR\_DAT6\_FL

Offset Address: 0x40088118

FIR channel 6 float point data input &amp; output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_DAT6\_FL | rw | 31:0 | 32'b0 | FIR channel6 float data |

### FSP\_FIR\_DAT7\_FL

Offset Address: 0x4008811c

FIR channel 7 float point data input &amp; output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_DAT7\_FL | rw | 31:0 | 32'b0 | FIR channel7 float data |

### FSP\_FIR\_DAT8\_FL

Offset Address: 0x40088120

FIR channel 8 float point data input &amp; output register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| FIR\_DAT8\_FL | rw | 31:0 | 32'b0 | FIR channel8 float data |

### FSP\_SIN\_COS\_IXOX

Offset Address: 0x40088140

sin &amp; cos input fix output fix mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SIN\_COS\_IXOX\_SRC | rw | 15:0 | 16'b0 | SIN\_COS input data source address. Input fix output fix |
| SIN\_COS\_IXOX\_DST | rw | 31:16 | 16'b0 | SIN\_COS output data destination address. Input fix output fix. |

### FSP\_SIN\_COS\_IXOL

Offset Address: 0x40088144

sin &amp; cos input fix output float mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SIN\_COS\_IXOL\_SRC | rw | 15:0 | 16'b0 | SIN\_COS input data source word address. Input fix output float |
| SIN\_COS\_IXOL\_DST | rw | 31:16 | 16'b0 | SIN\_COS output data destination word address. Input fix output float. |

### FSP\_SIN\_COS\_ILOX

Offset Address: 0x40088148

sin &amp; cos input float output fix mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SIN\_COS\_ILOX\_SRC | rw | 15:0 | 16'b0 | SIN\_COS input data source word address. Input float output fix |
| SIN\_COS\_ILOX\_DST | rw | 31:16 | 16'b0 | SIN\_COS output data destination word address. Input float output fix. |

### FSP\_SIN\_COS\_ILOL

Offset Address: 0x4008814c

sin &amp; cos input float output float mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| SIN\_COS\_ILOL\_SRC | rw | 15:0 | 16'b0 | SIN\_COS input data source word address. Input float output float |
| SIN\_COS\_ILOL\_DST | rw | 31:16 | 16'b0 | SIN\_COS output data destination word address. Input float output float |

### FSP\_LN\_SQRT\_IXOX

Offset Address: 0x40088150

LN &amp; sqrt input fix output fix mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| LN\_SQRT\_IXOX\_SRC | rw | 15:0 | 16'b0 | LN\_SQRT input data source word address. Input fix output fix |
| LN\_SQRT\_IXOX\_DST | rw | 31:16 | 16'b0 | LN\_SQRT output data destination word address. Input fix output fix. |

### FSP\_LN\_SQRT\_IXOL

Offset Address: 0x40088154

LN &amp; sqrt input fix output float mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| LN\_SQRT\_IXOL\_SRC | rw | 15:0 | 16'b0 | LN\_SQRT input data source word address. Input fix output float |
| LN\_SQRT\_IXOL\_DST | rw | 31:16 | 16'b0 | LN\_SQRT output data destination word address. Input fix output float. |

### FSP\_LN\_SQRT\_ILOX

Offset Address: 0x40088158

LN &amp; sqrt input float output fix mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| LN\_SQRT\_ILOX\_SRC | rw | 15:0 | 16'b0 | LN\_SQRT input data source word address. Input float output fix |
| LN\_SQRT\_ILOX\_DST | rw | 31:16 | 16'b0 | LN\_SQRT output data destination word address. Input float output fix. |

### FSP\_LN\_SQRT\_ILOL

Offset Address: 0x4008815c

LN &amp; sqrt input float output float mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| LN\_SQRT\_ILOL\_SRC | rw | 15:0 | 16'b0 | LN\_SQRT input data source word address. Input float output float |
| LN\_SQRT\_ILOL\_DST | rw | 31:16 | 16'b0 | LN\_SQRT output data destination word address. Input float output float |

### FSP\_CORDIC\_T0UP\_IXOX

Offset Address: 0x40088160

native cordic input fix output fix, t=0, u=1 mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CORDIC\_T0UP\_IXOX\_SRC | rw | 15:0 | 16'b0 | CORDIC\_T0UP\_IXOX input data source word address. Input fix output fix |
| CORDIC\_T0UP\_IXOX\_DST | rw | 31:16 | 16'b0 | CORDIC\_T0UP\_IXOX output data destination word address. X is saved at here Y is saved at word address CORDIC\_T0UP\_IXOX\_DST+1. Input fix output fix |

### FSP\_CORDIC\_T0UP\_IXOL

Offset Address: 0x40088164

native cordic input fix output float, t=0, u=1 mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CORDIC\_T0UP\_IXOL\_SRC | rw | 15:0 | 16'b0 | CORDIC\_T0UP\_IXOL input data source word address. Input fix output float |
| CORDIC\_T0UP\_IXOL\_DST | rw | 31:16 | 16'b0 | CORDIC\_T0UP\_IXOL output data destination word address. X is saved at here Y is saved at word address CORDIC\_T0UP\_IXOL\_DST+1. Input fix output float |

### FSP\_CORDIC\_T0UP\_ILOX

Offset Address: 0x40088168

native cordic input float output fix, t=0, u=1 mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CORDIC\_T0UP\_ILOX\_SRC | rw | 15:0 | 16'b0 | CORDIC\_T0UP\_ILOX input data source word address. Input float output fix |
| CORDIC\_T0UP\_ILOX\_DST | rw | 31:16 | 16'b0 | CORDIC\_T0UP\_ILOX output data destination word address. X is saved at here Y is saved at word address CORDIC\_T0UP\_ILOX\_DST+1. Input float output fix |

### FSP\_CORDIC\_T0UP\_ILOL

Offset Address: 0x4008816c

native cordic input float output float, t=0, u=1 mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CORDIC\_T0UP\_ILOL\_SRC | rw | 15:0 | 16'b0 | CORDIC\_T0UN\_ILOL input data source word address. Input float output float |
| CORDIC\_T0UP\_ILOL\_DST | rw | 31:16 | 16'b0 | CORDIC\_T0UN\_ILOL output data destination word address. X is saved at here Y is saved at word address CORDIC\_T0UN\_ILOL\_DST+1. Input float output float |

### FSP\_CORDIC\_T0UN\_IXOX

Offset Address: 0x40088170

native cordic input fix output fix, t=0, u=-1 mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CORDIC\_T0UN\_IXOX\_SRC | rw | 15:0 | 16'b0 | CORDIC\_T0UN\_IXOX input data source word address. Input fix output fix |
| CORDIC\_T0UN\_IXOX\_DST | rw | 31:16 | 16'b0 | CORDIC\_T0UN\_IXOX output data destination word address. X is saved at here Y is saved at word address CORDIC\_T0UN\_IXOX\_DST+1. Input fix output fix |

### FSP\_CORDIC\_T0UN\_IXOL

Offset Address: 0x40088174

native cordic input fix output float, t=0, u=-1 mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CORDIC\_T0UN\_IXOL\_SRC | rw | 15:0 | 16'b0 | CORDIC\_T0UN\_IXOL input data source word address. Input fix output float |
| CORDIC\_T0UN\_IXOL\_DST | rw | 31:16 | 16'b0 | CORDIC\_T0UN\_IXOL output data destination word address. X is saved at here Y is saved at word address CORDIC\_T0UN\_IXOL\_DST+1. Input fix output float |

### FSP\_CORDIC\_T0UN\_ILOX

Offset Address: 0x40088178

native cordic input float output fix, t=0, u=-1 mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CORDIC\_T0UN\_ILOX\_SRC | rw | 15:0 | 16'b0 | CORDIC\_T0UN\_ILOX input data source word address. Input float output fix |
| CORDIC\_T0UN\_ILOX\_DST | rw | 31:16 | 16'b0 | CORDIC\_T0UN\_ILOX output data destination word address. X is saved at here Y is saved at word address CORDIC\_T0UN\_ILOX\_DST+1. Input float output fix |

### FSP\_CORDIC\_T0UN\_ILOL

Offset Address: 0x4008817c

native cordic input float output float, t=0, u=-1 mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CORDIC\_T0UN\_ILOL\_SRC | rw | 15:0 | 16'b0 | CORDIC\_T0UN\_ILOL input data source word address. Input float output float |
| CORDIC\_T0UN\_ILOL\_DST | rw | 31:16 | 16'b0 | CORDIC\_T0UN\_ILOL output data destination word address. X is saved at here Y is saved at word address CORDIC\_T0UN\_ILOL\_DST+1. Input float output float |

### FSP\_CORDIC\_T1UP\_IXOX

Offset Address: 0x40088180

native cordic input fix output fix, t=1, u=1 mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CORDIC\_T1UP\_IXOX\_SRC | rw | 15:0 | 16'b0 | CORDIC\_T1UP\_IXOX input data source word address. Input fix output fix |
| CORDIC\_T1UP\_IXOX\_DST | rw | 31:16 | 16'b0 | CORDIC\_T1UP\_IXOX output data destination word address. X is saved at here Z is saved at word address CORDIC\_T1UP\_IXOX\_DST+1. Input fix output fix |

### FSP\_CORDIC\_T1UP\_IXOL

Offset Address: 0x40088184

native cordic input fix output float, t=1, u=1 mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CORDIC\_T1UP\_IXOL\_SRC | rw | 15:0 | 16'b0 | CORDIC\_T1UP\_IXOL input data source word address. Input fix output float |
| CORDIC\_T1UP\_IXOL\_DST | rw | 31:16 | 16'b0 | CORDIC\_T1UP\_IXOL output data destination word address. X is saved at here Z is saved at word address CORDIC\_T1UP\_IXOL\_DST+1. Input fix output float |

### FSP\_CORDIC\_T1UP\_ILOX

Offset Address: 0x40088188

native cordic input float output fix, t=1, u=1 mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CORDIC\_T1UP\_ILOX\_SRC | rw | 15:0 | 16'b0 | CORDIC\_T1UP\_ILOX input data source word address. Input float output fix |
| CORDIC\_T1UP\_ILOX\_DST | rw | 31:16 | 16'b0 | CORDIC\_T1UP\_ILOX output data destination word address. X is saved at here Z is saved at word address CORDIC\_T1UP\_ILOX\_DST+1. Input float output fix |

### FSP\_CORDIC\_T1UP\_ILOL

Offset Address: 0x4008818c

native cordic input float output float, t=1, u=1 mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CORDIC\_T1UP\_ILOL\_SRC | rw | 15:0 | 16'b0 | CORDIC\_T1UP\_ILOL input data source word address. Input float output float |
| CORDIC\_T1UP\_ILOL\_DST | rw | 31:16 | 16'b0 | CORDIC\_T1UP\_ILOL output data destination word address. X is saved at here Z is saved at word address CORDIC\_T1UP\_ILOL\_DST+1. Input float output float |

### FSP\_CORDIC\_T1UN\_IXOX

Offset Address: 0x40088190

native cordic input fix output fix, t=1, u=-1 mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CORDIC\_T1UN\_IXOX\_SRC | rw | 15:0 | 16'b0 | CORDIC\_T1UN\_IXOX input data source word address. Input fix output fix |
| CORDIC\_T1UN\_IXOX\_DST | rw | 31:16 | 16'b0 | CORDIC\_T1UN\_IXOX output data destination word address. X is saved at here Z is saved at word address CORDIC\_T1UN\_IXOX\_DST+1. Input fix output fix |

### FSP\_CORDIC\_T1UN\_IXOL

Offset Address: 0x40088194

native cordic input fix output float, t=1, u=-1 mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CORDIC\_T1UN\_IXOL\_SRC | rw | 15:0 | 16'b0 | CORDIC\_T1UN\_IXOL input data source word address. Input fix output float |
| CORDIC\_T1UN\_IXOL\_DST | rw | 31:16 | 16'b0 | CORDIC\_T1UN\_IXOL output data destination word address. X is saved at here Z is saved at word address CORDIC\_T1UN\_IXOL\_DST+1. Input fix output float |

### FSP\_CORDIC\_T1UN\_ILOX

Offset Address: 0x40088198

native cordic input float output fix, t=1, u=-1 mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CORDIC\_T1UN\_ILOX\_SRC | rw | 15:0 | 16'b0 | CORDIC\_T1UN\_ILOX input data source word address. Input float output fix |
| CORDIC\_T1UN\_ILOX\_DST | rw | 31:16 | 16'b0 | CORDIC\_T1UN\_ILOX output data destination word address. X is saved at here Z is saved at word address CORDIC\_T1UN\_ILOX\_DST+1. Input float output fix |

### FSP\_CORDIC\_T1UN\_ILOL

Offset Address: 0x4008819c

native cordic input float output float, t=1, u=-1 mode data address register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CORDIC\_T1UN\_ILOL\_SRC | rw | 15:0 | 16'b0 | CORDIC\_T1UN\_ILOL input data source word address. Input float output float |
| CORDIC\_T1UN\_ILOL\_DST | rw | 31:16 | 16'b0 | CORDIC\_T1UN\_ILOL output data destination word address. X is saved at here Z is saved at word address CORDIC\_T1UN\_ILOL\_DST+1. Input float output float |

### GPIOA\_DATA

Offset Address: 0x4008c000

GPIO value register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DATA | rw | 31:0 | 32'b0 | data value |

### GPIOA\_DATAOUT

Offset Address: 0x4008c004

GPIO output status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| DATAOUT | rw | 31:0 | 32'b0 | Data output register value |

### GPIOA\_OUTENSET

Offset Address: 0x4008c010

GPIO output enable set register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| OUTENSET | rw | 31:0 | 32'b0 | output enable clear |

### GPIOA\_OUTENCLR

Offset Address: 0x4008c014

GPIO output clear register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| OUTENCLR | rw | 31:0 | 32'b0 | output enable clear |

### GPIOA\_INTENSET

Offset Address: 0x4008c020

GPIO interrupt enable set register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| INTENSET | rw | 31:0 | 32'b0 | interrupt enable set |

### GPIOA\_INTENCLR

Offset Address: 0x4008c024

GPIO interrupt enable clear register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| INTENCLR | rw | 31:0 | 32'b0 | interrupt enable clear |

### GPIOA\_INTTYPESET

Offset Address: 0x4008c028

GPIO interrupt type set register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| INTTYPESET | rw | 31:0 | 32'b0 | interrupt type set |

### GPIOA\_INTTYPECLR

Offset Address: 0x4008c02c

GPIO interrupt type set register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| INTTYPECLR | rw | 31:0 | 32'b0 | interrupt type clear |

### GPIOA\_INTPOLSET

Offset Address: 0x4008c030

GPIO interrupt polarity set register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| INTPOLSET | rw | 31:0 | 32'b0 | interrupt polarity set |

### GPIOA\_INTPOLCLR

Offset Address: 0x4008c034

GPIO interrupt polarity clear register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| INTPOLCLR | rw | 31:0 | 32'b0 | interrupt polarity clear |

### GPIOA\_INTSTATUS

Offset Address: 0x4008c038

GPIO interrupt status register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| INTSTATUS | rw | 31:0 | 32'b0 | interrupt status |

### CRC\_ENGINE\_MODE

Offset Address: 0x4008e000

CRC mode register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CRC\_POLY | rw | 1:0 | 2'b0 | CRC polynomial: 1X = CRC-32 polynomial 01 = CRC-16 polynomial 00 = CRC-CCITT polynomial |
| BIT\_RVS\_WR | rw | 2 | 1'b0 | Data bit order: 1 = Bit order reverse for CRC\_WR\_DATA (per byte) 0 = No bit order reverse for CRC\_WR\_DATA (per byte) |
| CMPL\_WR | rw | 3 | 1'b0 | Data complement: 1 = 1'-s complement for CRC\_WR\_DATA 0 = No 1'-s complement for CRC\_WR\_DATA |
| BIT\_RVS\_SUM | rw | 4 | 1'b0 | CRC sum bit order: 1 = Bit order reverse for CRC\_SUM 0 = No bit order reverse for CRC\_SUM |
| CMPL\_SUM | rw | 5 | 1'b0 | CRC sum complement: 1 = 1'-s complement for CRC\_SUM 0 = No 1'-s complement for CRC\_SUM |
| Reserved | rw | 31:6 | 26'b0 | Reserved |

### CRC\_ENGINE\_SEED

Offset Address: 0x4008e004

CRC seed register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CRC\_SEED | rw | 31:0 | 32'b0 | A write access to this register will load CRC seed value to CRC\_SUM register with selected bit order and 1'-s complement pre-processes. A write access to this register will overrule the CRC calculation in progresses. |

### CRC\_ENGINE\_SUM

Offset Address: 0x4008e008

CRC checksum register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CRC\_SUM | rw | 31:0 | 32'b0 | The most recent CRC sum can be read through this register with selected bit order and 1'-s complement post-processes. |

### CRC\_ENGINE\_WR\_DATA

Offset Address: 0x4008e008

CRC data register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Field name | rwu | Bit # | Reset | Description |
| CRC\_WR\_DATA | rw | 31:0 | 32'b0 | Data written to this register will be taken to perform CRC calculation with selected bit order and 1'-s complement pre-process. Any write size 8, 16 or 32-bit are allowed and accept back-to-back transactions. |