Institut Teknologi Del
Jl. Sisingamangaraja
Sitoluama, Laguboti 22381
Toba Samosir – Sumatera Utara
http://www.del.ac.id/

PDS

Electronics Basic

6.2
Bipolar Junction Transistors

Figure 6-4 Emitter injects free electrons into base.

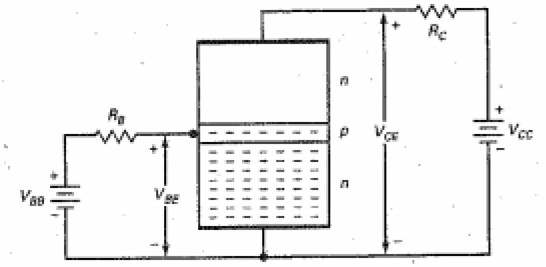
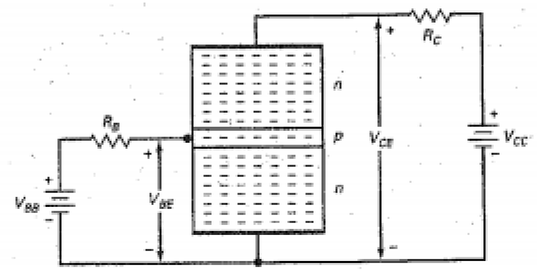


Figure 6-5 Free electrons from base flow into collector.



Example 6-3

A transistor has a collector current of 2 mA. If the current gain is 135, what is the base current?

SOLUTION Divide the collector current by the current gain to get:

$$I_B = \frac{2\ \text{mA}}{135} = 14.8\ \mu\text{A}$$

PRACTICE PROBLEM 6-3 If $I_C = 10$ mA in Example 6-3, find the transistor's base current.

Bipolar Junction Transistors

Topics Covered in Chapter 6

6-1: Transistor Construction

6-2: Proper Transistor Biasing

6-3: Operating Regions

6-4: Transistor Ratings

6-5: Checking a Transistor with an Ohmmeter

6-6: Transistor Biasing

6-1: Transistor Construction

- A transistor has three doped regions, as shown in Fig. 6-1 (next slide).
- Fig. 6-1 (a) shows an npn transistor, and a pnp is shown in (b).
- For both types, the base is a narrow region sandwiched between the larger collector and emitter regions.

6-1: Transistor Construction

- The <u>emitter</u> region is heavily doped and its job is to emit carriers into the base.
- The <u>base</u> region is very thin and lightly doped.
- Most of the current carriers injected into the base from emitter pass on to the collector.
- The <u>collector</u> region is moderately doped and is the largest of all three regions.

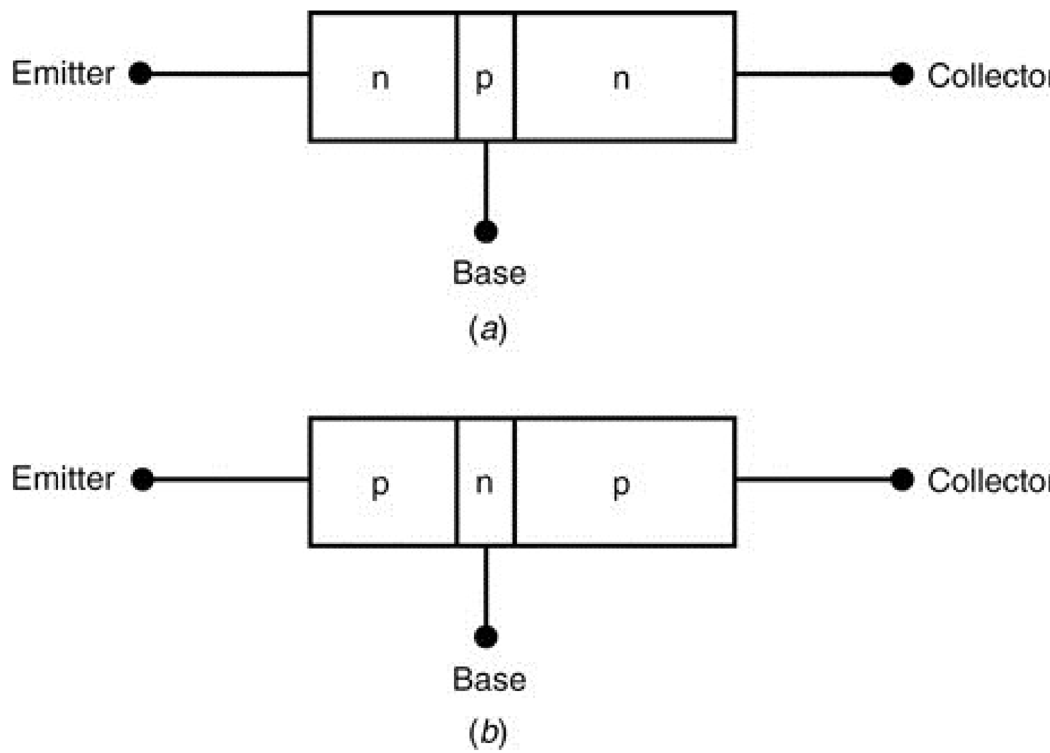
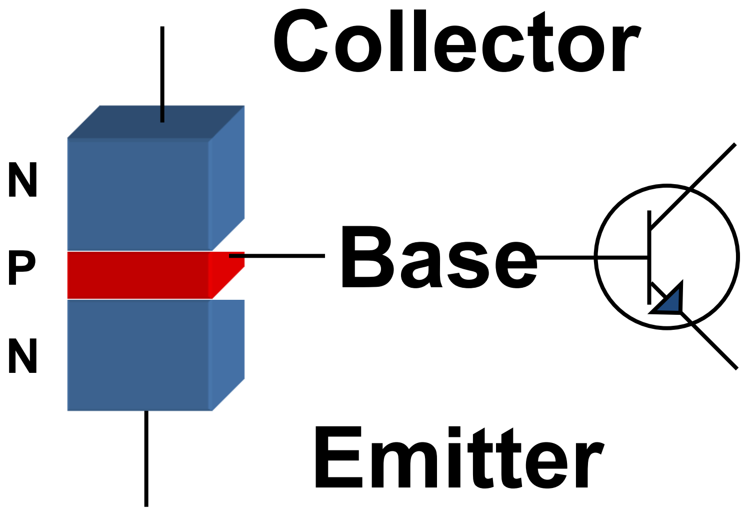
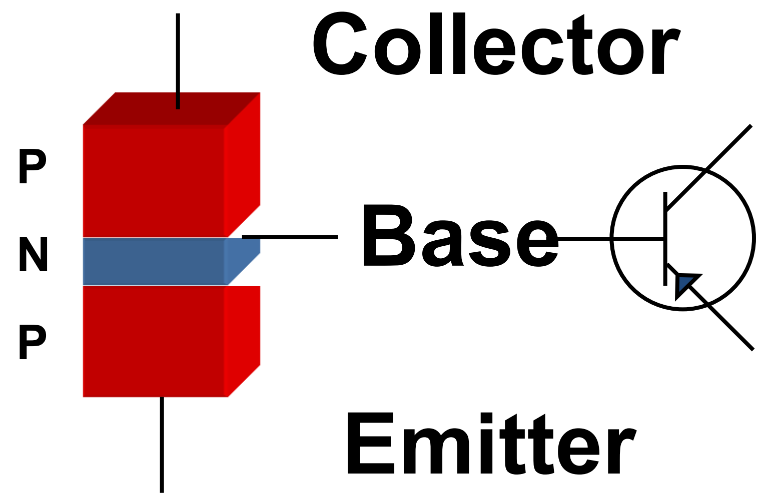
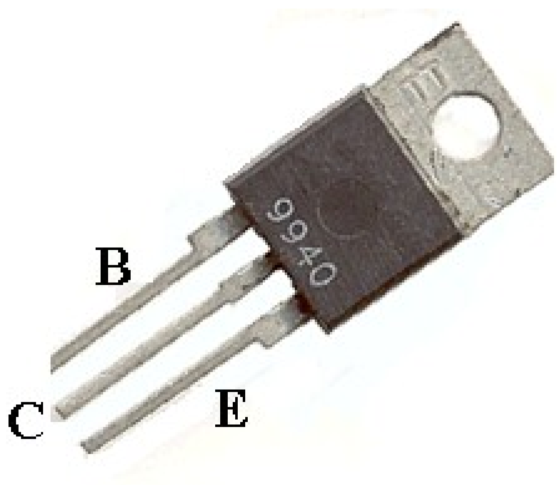


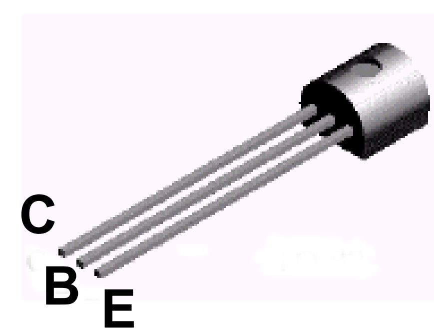
Fig. 6-1

Bipolar Transistors





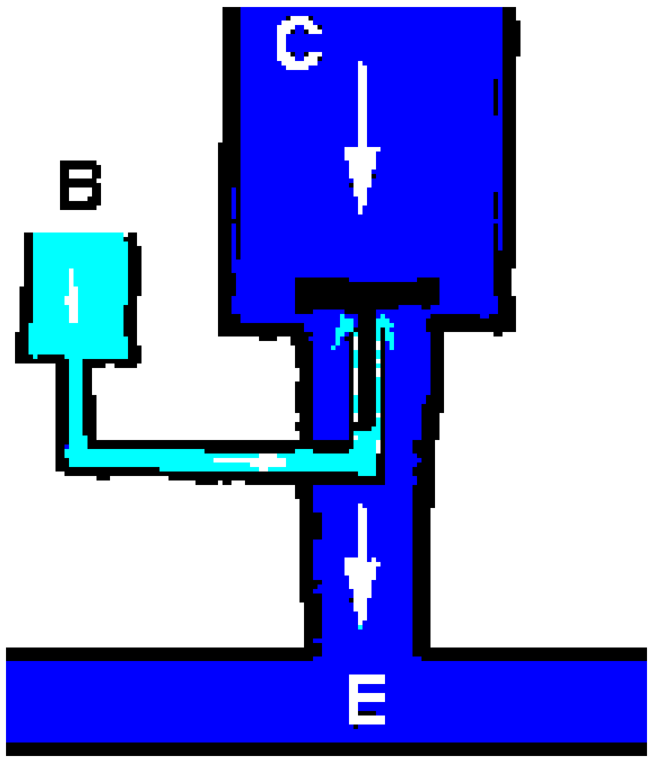


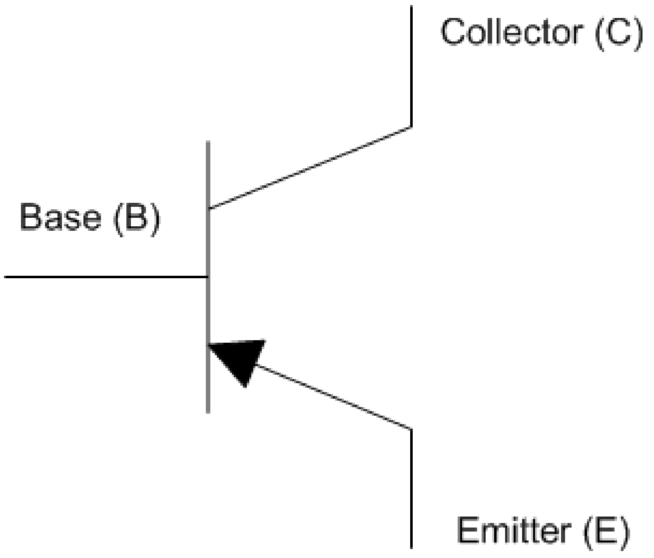


6-2: Proper Transistor Biasing

- For a transistor to function properly as an amplifier, the **emitter-base** junction must be forward-biased and the **collector-base** junction must be reverse-biased.
- The common connection for the voltage sources are at the base lead of the transistor.
- The emitter-base supply voltage is designated V_{EE} and the collector-base supply voltage is designated V_{CC}.
- For silicon, the barrier potential for both EB and CB junctions equals 0.7 V

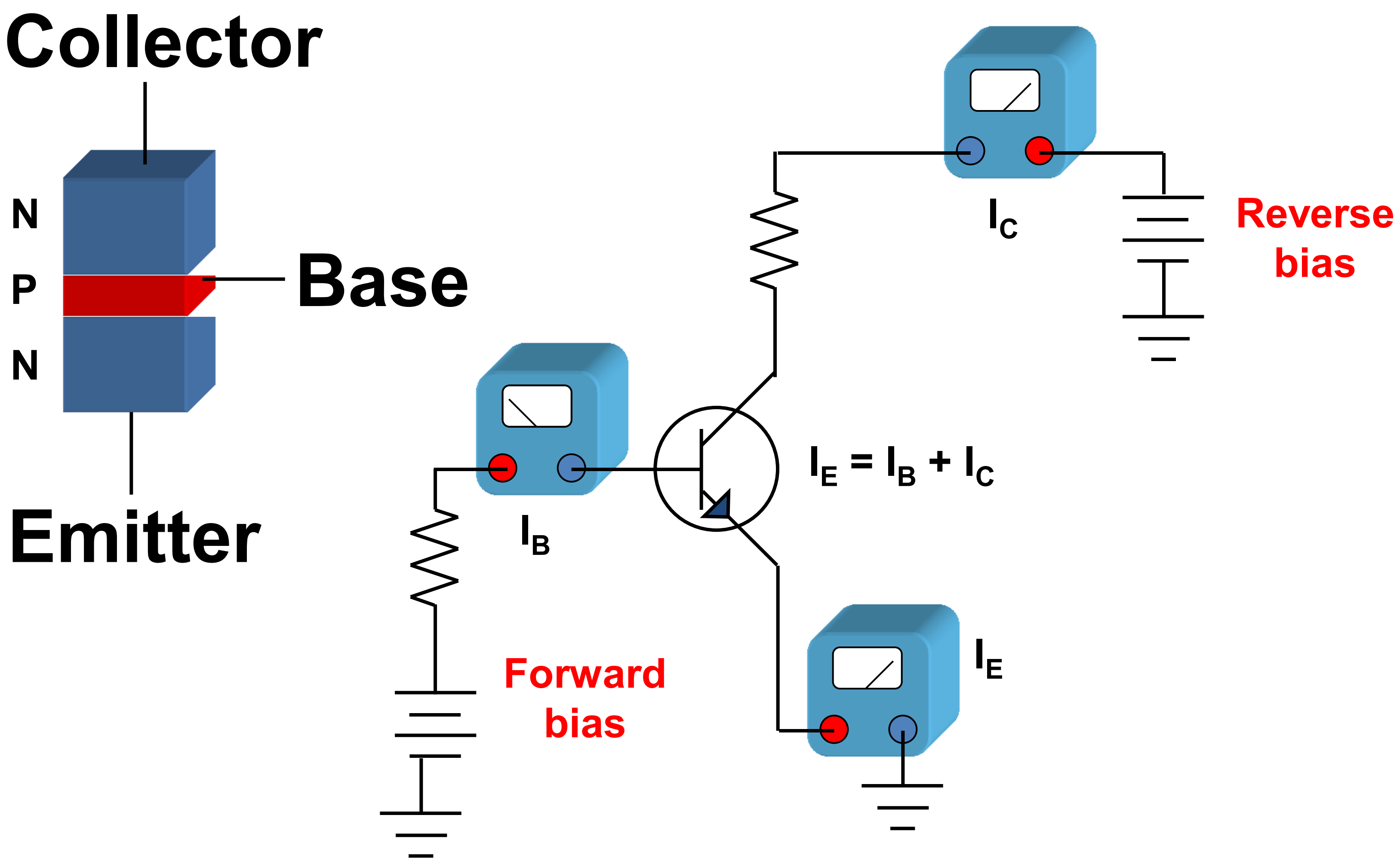
Schematic Symbol





PNP transistor

Transistor Biasing



6-2: Proper Transistor Biasing

- Fig. 6-4 shows transistor biasing for the *common-base* connection.
- Proper biasing for an npn transistor is shown in (a).
- The EB junction is forward-biased by the emitter supply voltage, V_{EE}.
- V_{CC} reverse-biases the CB junction.
- Fig. 6-4 (b) illustrates currents in a transistor.
- CE voltage of an npn transistor must be positive
- Ratio of I_C to I_E is called DC alpha α_{dc}

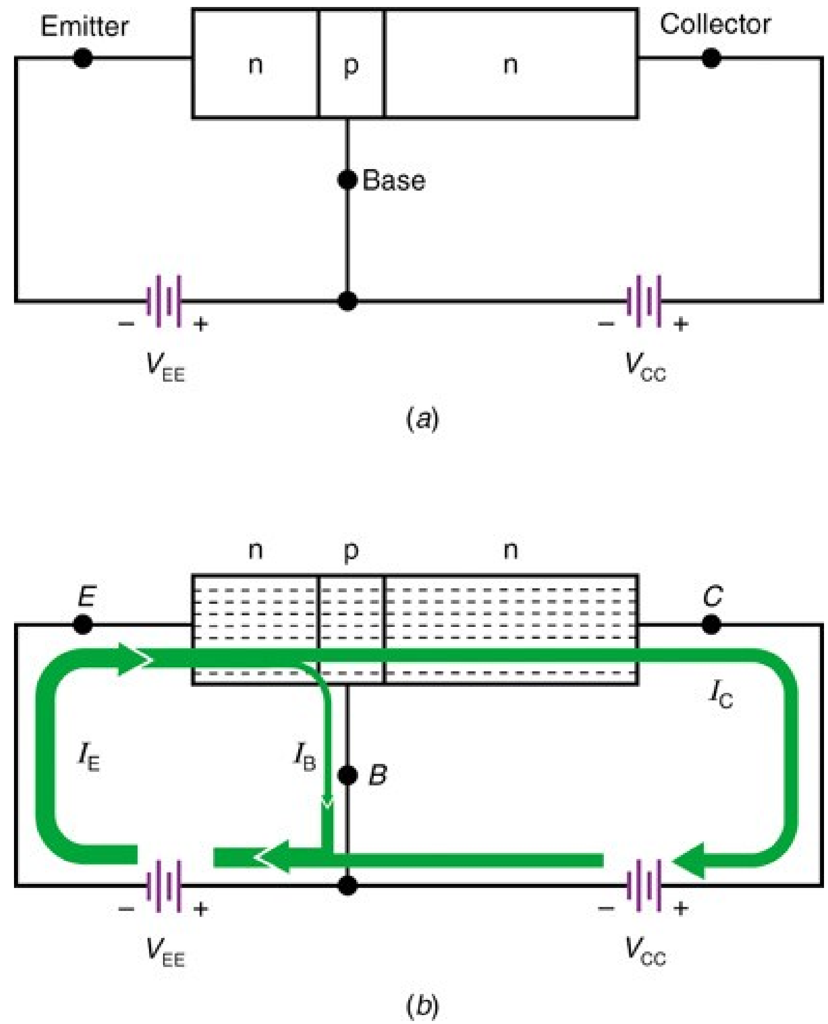
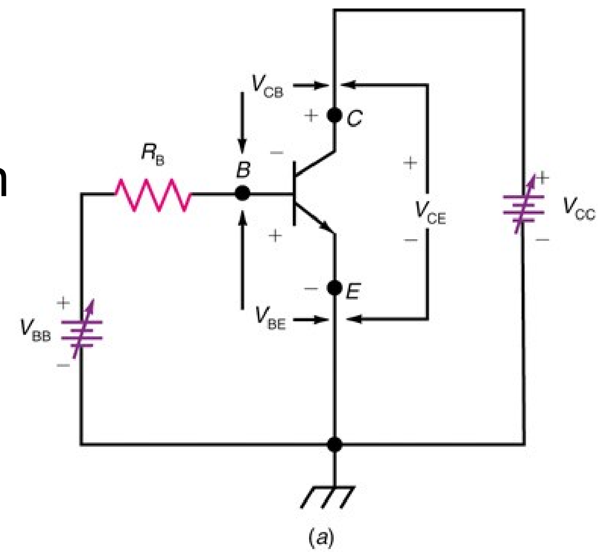


Fig. 6-4

6-3: Operating Regions

- Since emitter lead is common, this connection is called common-emitter connection
- Collector current I_C is <u>controlled</u> solely by the base current, I_B.
- By varying I_B, a transistor can be made to operate in any one of the following regions
    - Active
    - Saturation
    - Breakdown
    - Cutoff
- Ratio of I_C to I_B is called DC beta β_{dc}



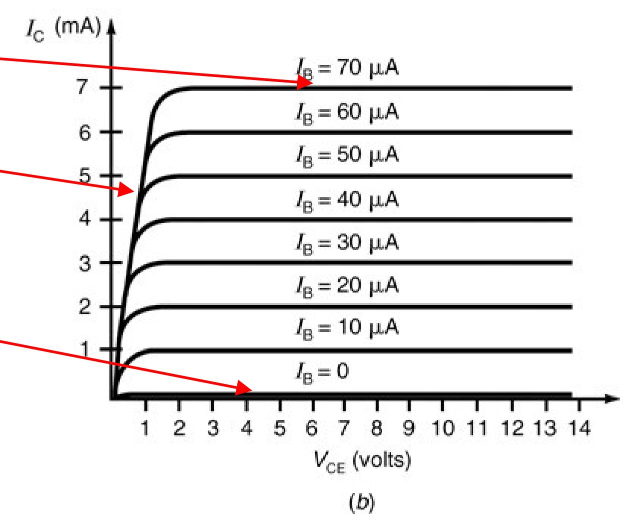


Fig. 6-6: Common-emitter connection (a) circuit. (b) Graph of I_C versus V_{CE} for different base current values.

6-3: Operating Regions

- Active Region
  - Collector curves are nearly horizontal
  - I_C is greater than I_B ($I_C = \beta_{dc} \times I_B$)
- Saturation
  - I_C is not controlled by I_B
  - Vertical portion of the curve near the origin
- Breakdown
  - Collector-base voltage is too large and collector-base diode breaks down
  - Undesired collector current
- Cutoff
  - $I_B = 0$
  - Small collector current flows $I_C \approx 0$

Transistor Currents

- $I_E = I_B + I_C$
- $I_C = I_E - I_B$
- $I_B = I_E - I_C$
- $\beta_{dc} = \dfrac{I_C}{I_B}$
- $\alpha_{dc} = \dfrac{I_C}{I_E}$
- $\alpha_{dc} = \dfrac{\beta_{dc}}{1 + \beta_{dc}}$

Example 6-4

- A transistor has the following currents:

  $I_E = 15$ mA

  $I_B = 60\ \mu$A

Calculate $\alpha_{dc,}$ and β_{dc}

- $I_C = I_E - I_B = 14.94$ mA
- $\alpha_{dc} = 0.996$
- $\beta_{dc} = 249$

6-4: Transistor Ratings

- A transistor, like any other device, has limitations on its operations.
- These limitations are specified in the manufacturer's data sheet.
- Maximum ratings are given for
  - Collector-base voltage
  - Collector-emitter voltage
  - Emitter-base voltage
  - Collector current
  - Power dissipation

6-5: Checking a Transistor with an Ohmmeter

- An analog <u>ohmmeter</u> can be used to check a transistor because the emitter-base and collector-base junctions are p-n junctions.
- This is illustrated in Fig. 6-8 where the npn transistor is replaced by its diode equivalent circuit.

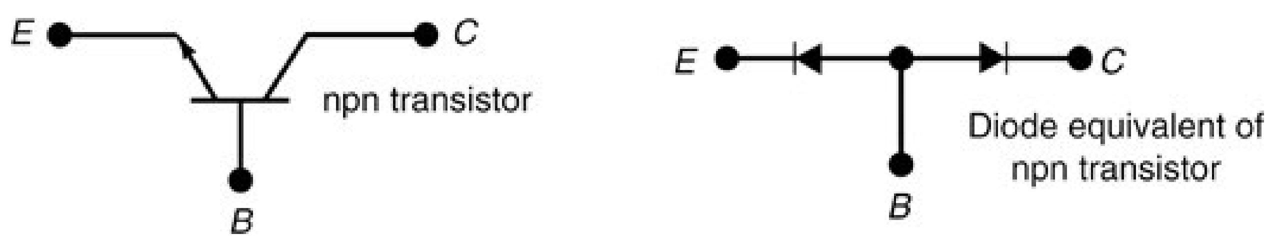


Fig. 6-8

Using a DMM to check a Diode

- Ohmmeter ranges in DMMs do not provide the proper forward bias to turn on the diode
- Set DMM to the special diode range
- In forward-bias, digital display indicates the forward voltage dropped across the diode
- In reverse-bias, digital display indicates an over range condition
- For silicon diode, using an analog meter, the ratio of reverse resistance, R_R, to forward resistance, R_F, should be very large such as 1000:1 or more

6-5: Checking a Transistor with an Ohmmeter

- To check the base-emitter junction of an npn transistor, first connect the ohmmeter as shown in Fig. 6-9 (a) and then reverse the ohmmeter leads as shown in (b).
- For a good p-n junction made of silicon, the ratio R_R/R_F should be equal to or greater than 1000:1.

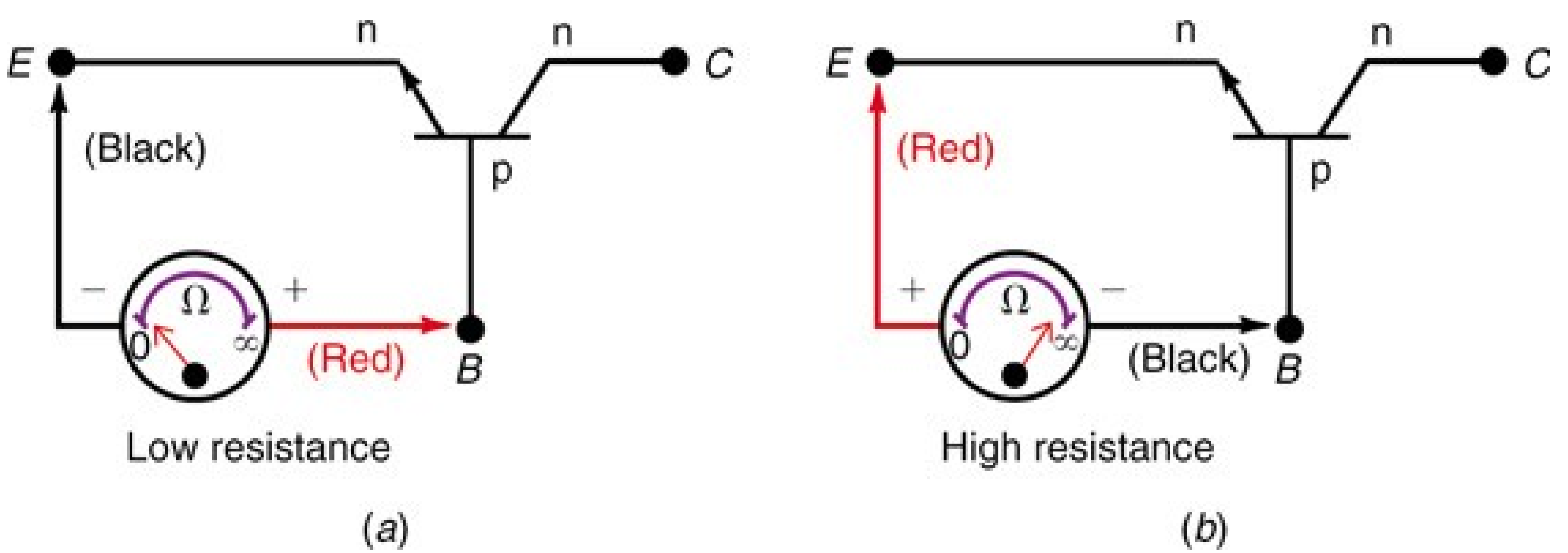


Fig. 6-9

6-5: Checking a Transistor with an Ohmmeter

- To check the <u>collector-base</u> junction, first connect the ohmmeter as shown in Fig. 6-10 (a) and then reverse the ohmmeter leads as shown in (b).
- For a good p-n junction made of silicon, the ratio R_R/R_F should be equal to or greater than 1000:1.
- Although not shown, the resistance measured between the collector and emitter should read high or infinite for <u>both</u> connections of the meter leads.

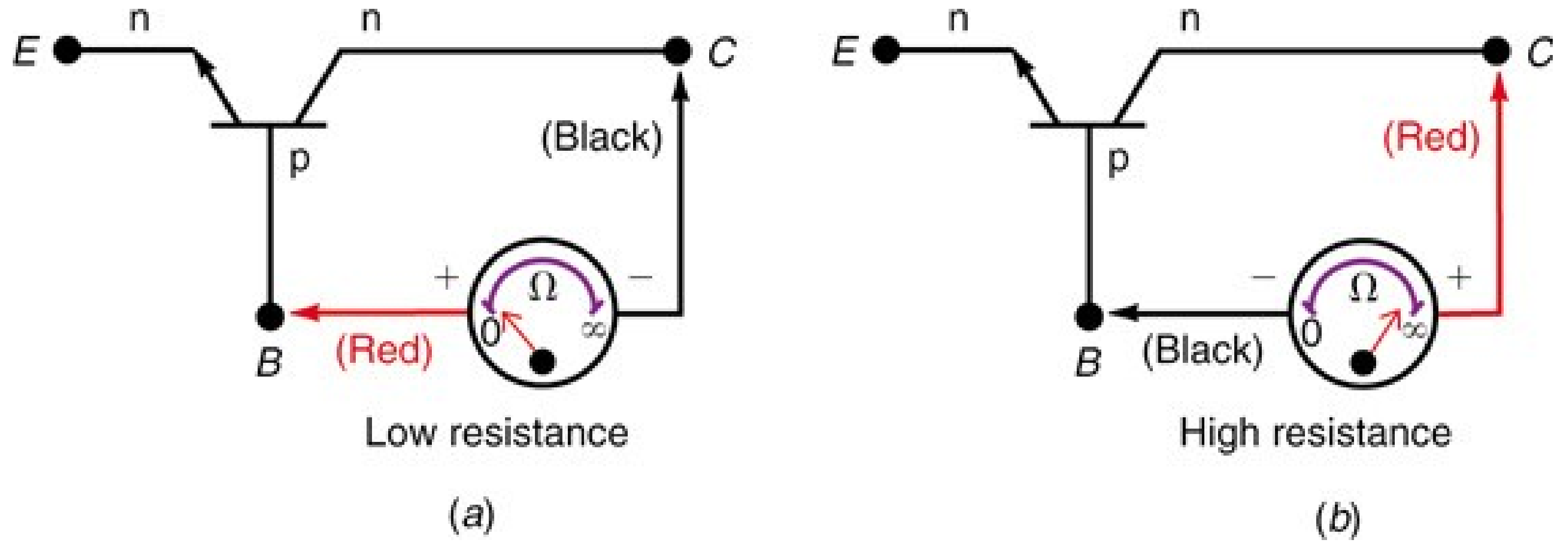


Fig. 6-10

Circuit with BJTs

Our approach: Operating point - dc operating point
Analysis of the signals - the signals to be amplified

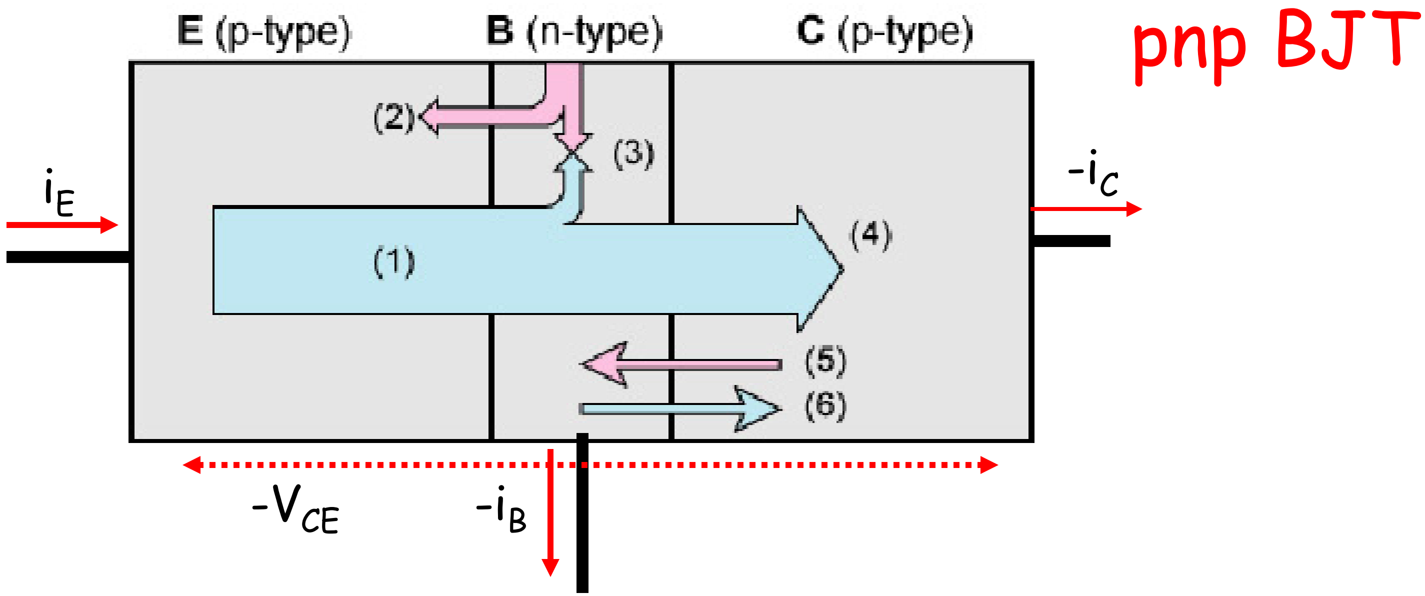
Circuit is divided into: model for large-signal dc analysis of BJT circuit
bias circuits for BJT amplifier
small-signal models used to analyze circuits for signals being amplified

Remember !

Table 2.3 The Four Regions of Operation of a Bipolar Junction Transistor

Region of Operation	Emitter-Base Junction	Collector-Base Junction
Forward active	forward biased	reverse biased
Reverse active	reverse biased	forward biased
Cutoff	reverse biased	reverse biased
Saturated	forward biased	forward biased

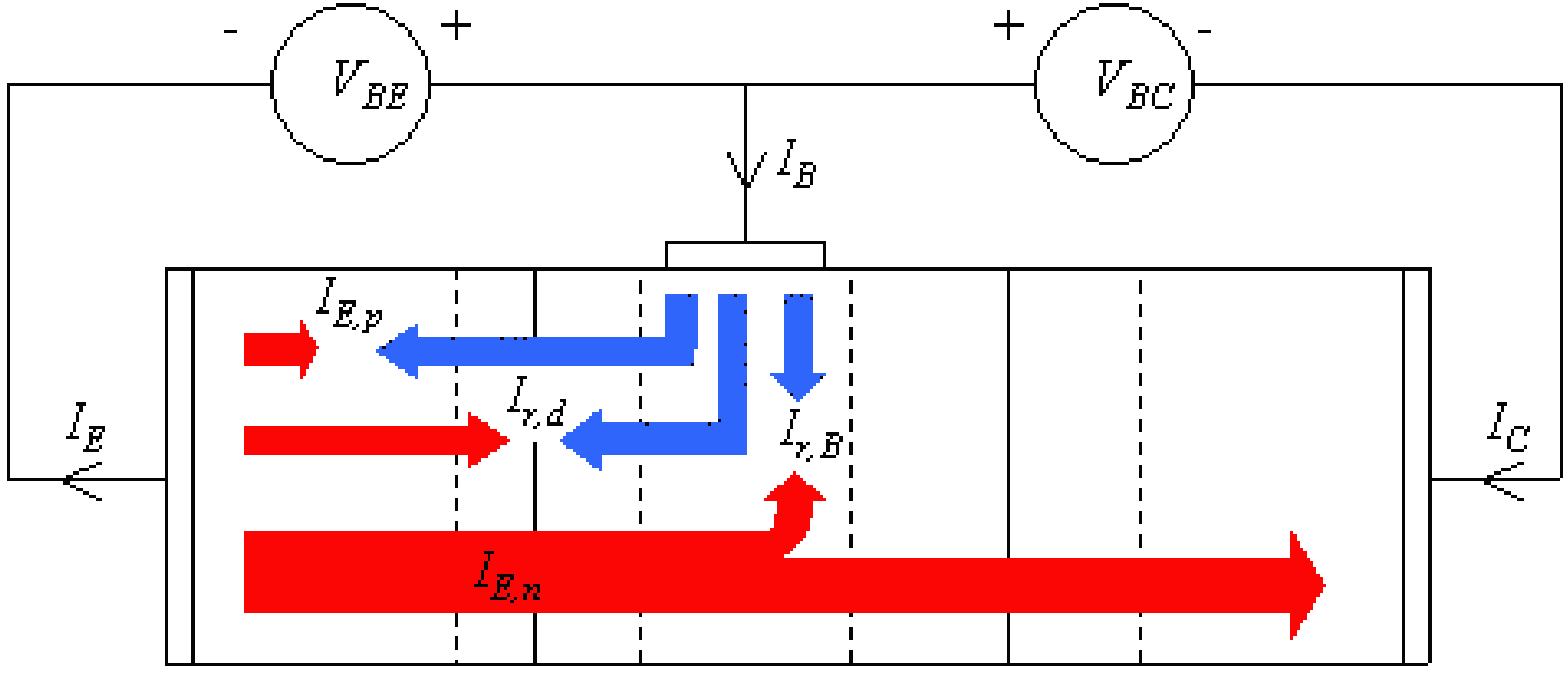
Current Flow in BJT



1. Injected h^+ current from E to B
2. e^- injected across the forward-biased EB junction (current from B to E)
3. e^- supplied by the B contact for recombination with h^+ (recombination current)
4. h^+ reaching the reverse-biased C junction

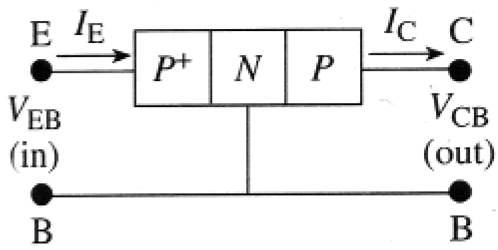
5,6. Thermally generated e^- & h^+ making up the reverse saturation current of the C junction

Now, you can try…



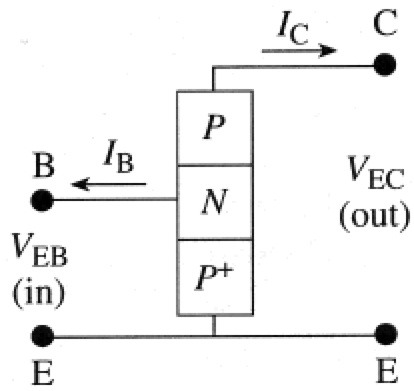
npn BJT

BJTs - Basic configurations



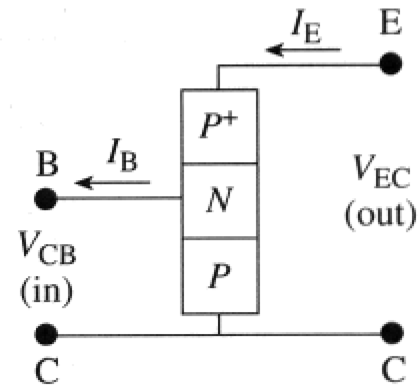
Common base

Both the input and output share the base "in common"



Common emitter

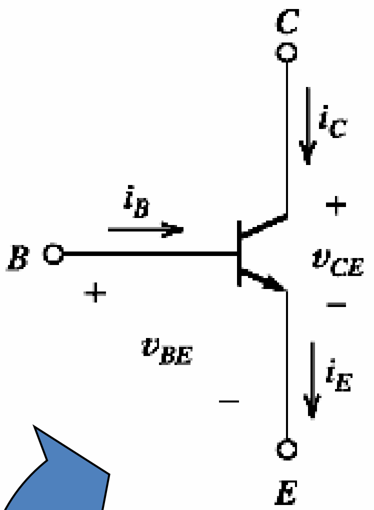
Both the input and output share the emitter "in common"



Common collector

Both the input and output share the Collector "in common"

npn BJTs – Operation Modes



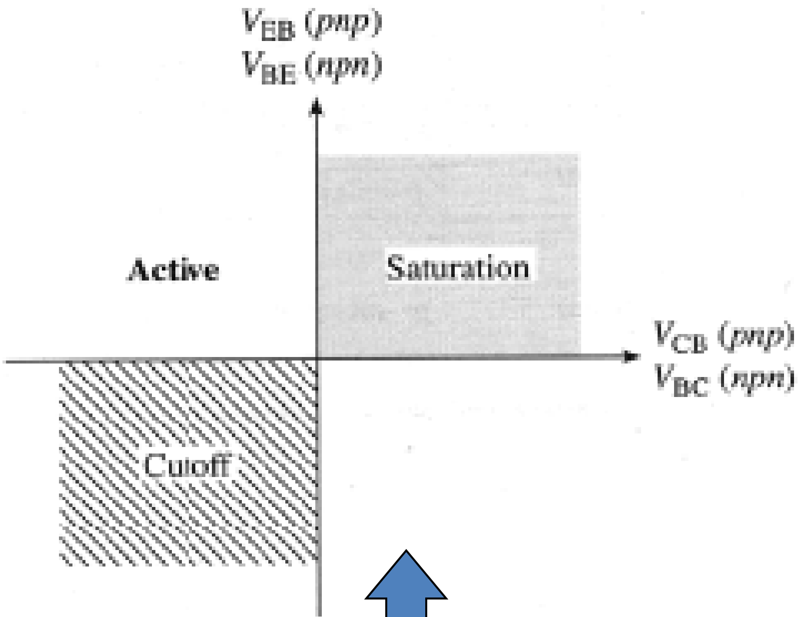
Forward & reverse polarized *pn* junctions

Different operation modes:

Table 2.3 The Four Regions of Operation of a Bipolar Junction Transistor

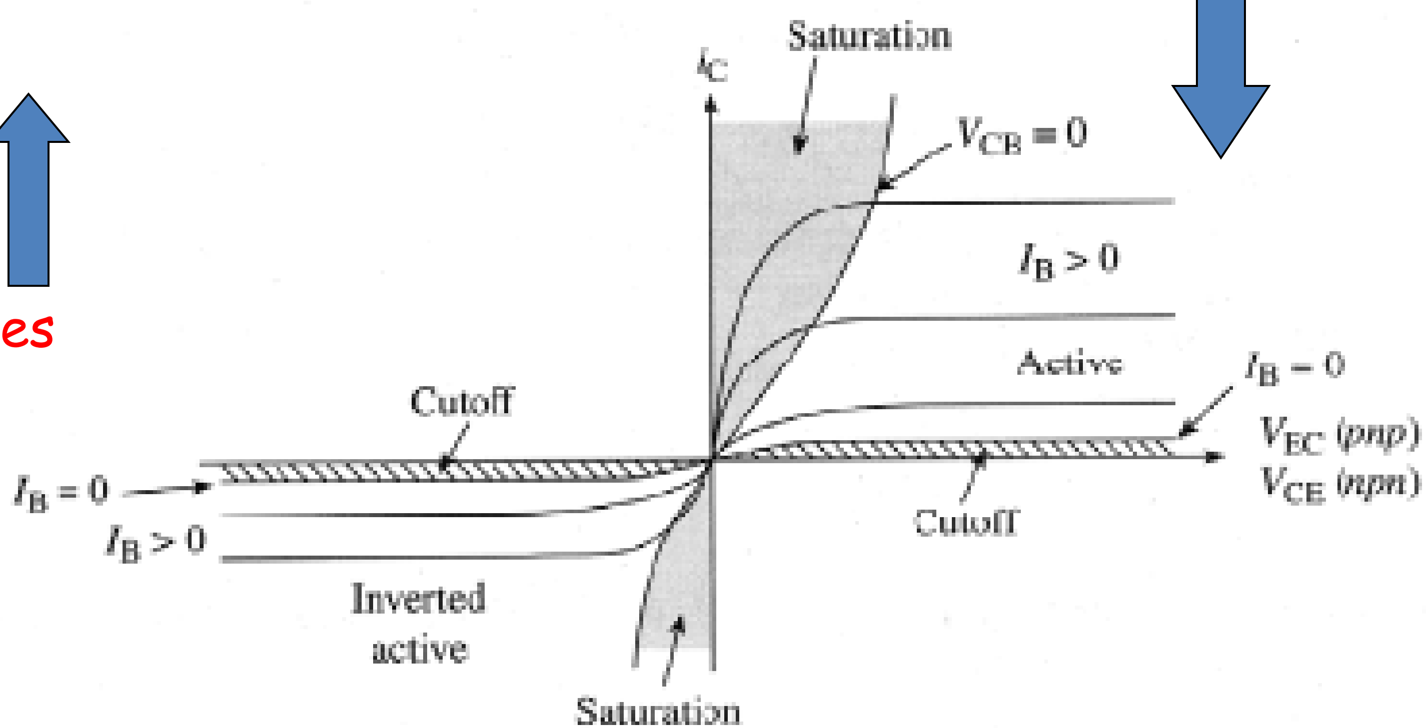
Region of Operation	Emitter-Base Junction	Collector-Base Junction
Forward active	forward biased	reverse biased
Reverse active	reverse biased	forward biased
Cutoff	reverse biased	reverse biased
Saturated	forward biased	forward biased

npn BJTs - Operation Modes

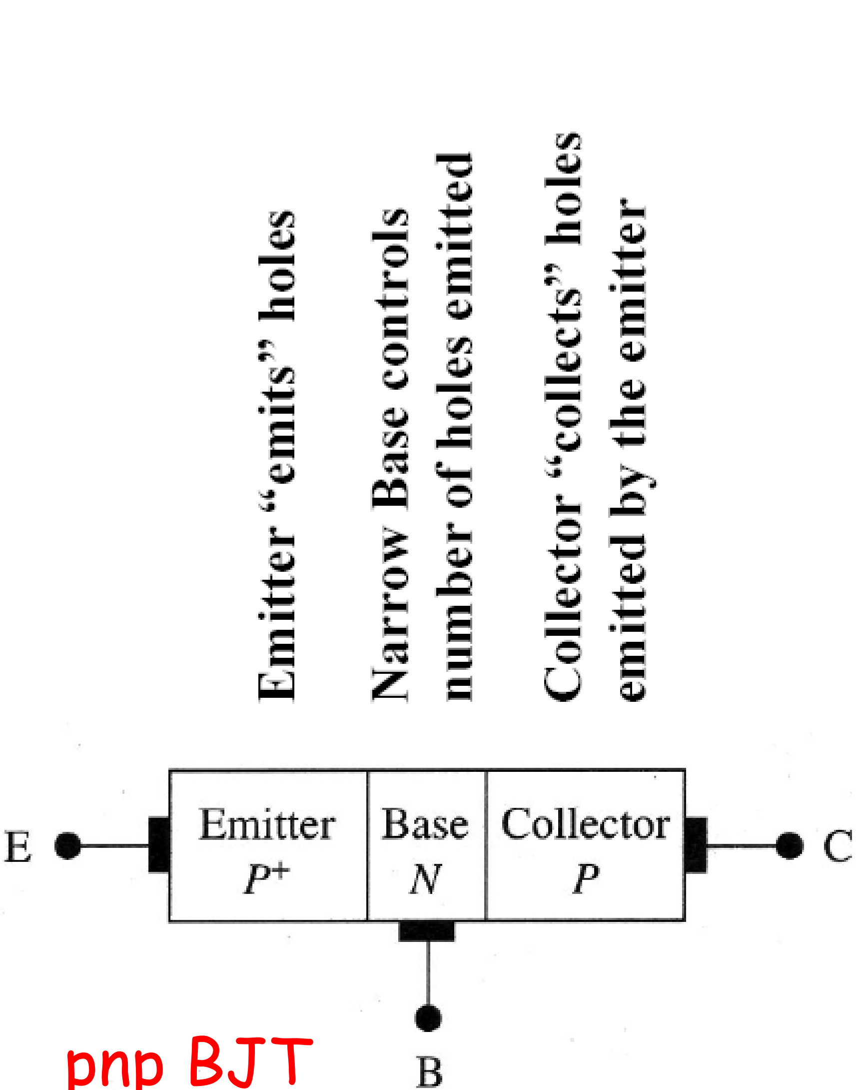


- When there is no I_B current almost no I_C flows
- When I_B current flows, I_C can flow
- The device is then a current controlled current device

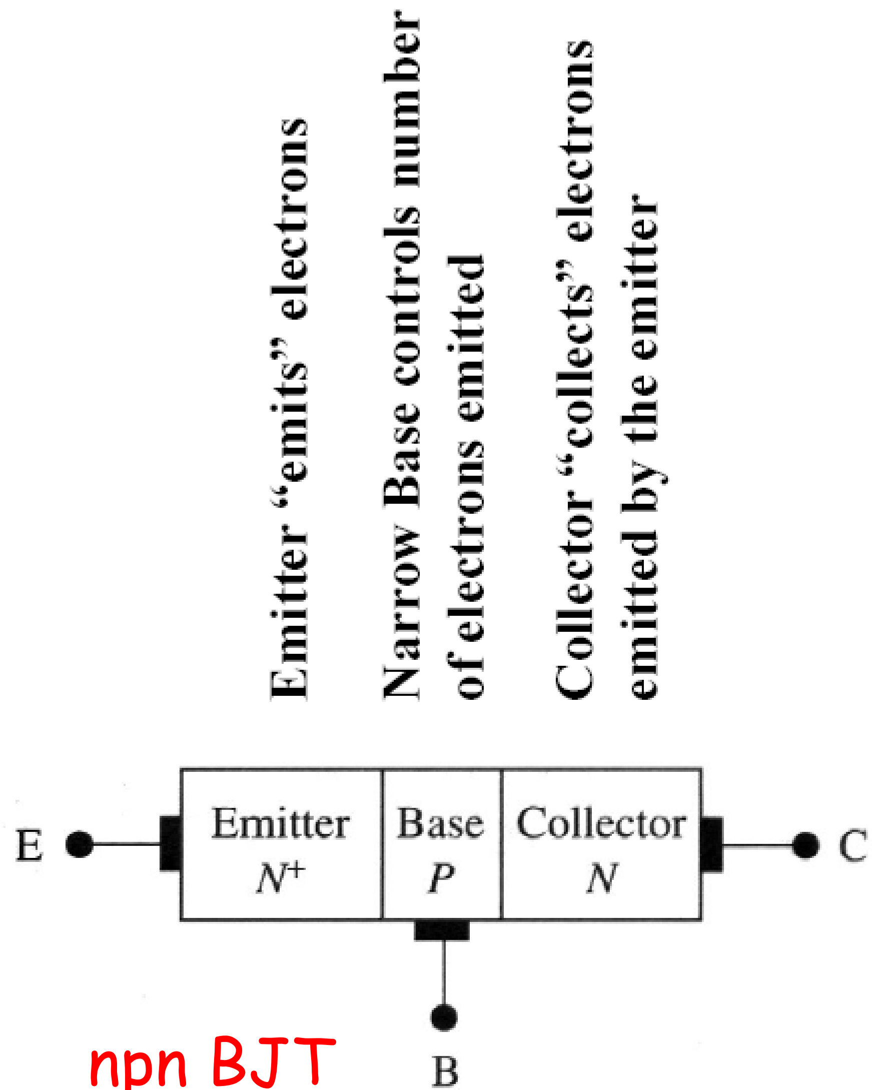
Operational modes can be defined based on V_{BE} and V_{BC}



BJT-Basic operation



pnp BJT



npn BJT

(n^+), (p^+) – heavy doped regions; Doping in E>B>C

BJTs - Current & Voltage Relationships

Operation mode: v_{BE} is forward & v_{BC} is reverse

Einstein relation

$$\frac{D}{\mu} = \frac{kT}{q}$$

The Shockley equation

$$i_E = I_{ES}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right]$$

I_{ES}-saturation I (10^{-12}-10^{-16}A); V_T=kT/q -thermal V (26meV)

D - diffusion coefficient [cm^2/s]

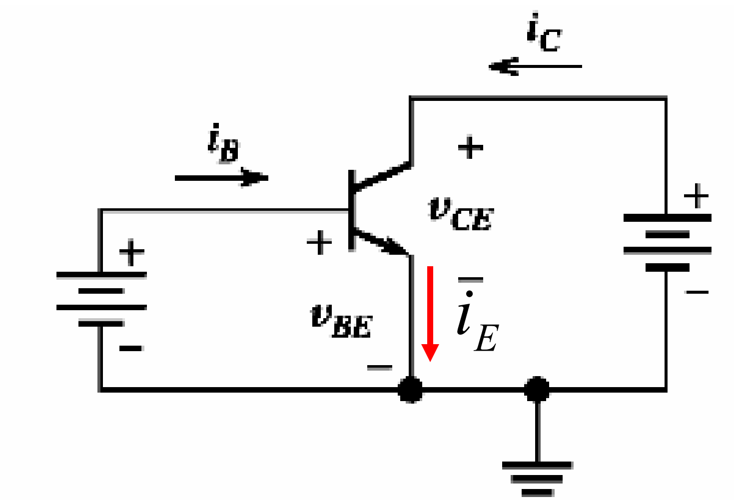
μ - carrier mobility [cm^2/Vs]

The Kirchhoff's laws

$$i_E = i_C + i_B$$

$$V_{BE} + V_{BC} + V_{CE} = 0$$

It is true regardless of the bias conditions of the junction



Useful parameter

$$\beta = \frac{i_C}{i_B}$$

the common-emitter current gain for ideal BJT β is infinite

BJTs - Current & Voltage Relationships

Useful parameter

$$\alpha = \frac{i_C}{i_E}$$

the common-base current gain
for typical BJT α is ~0.99

The Shockley equation once more

$$i_C = \alpha I_{ES}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right]$$

If we define the scale current

$$I_S = \alpha I_{ES}$$

$$i_C \cong I_S\left(\frac{v_{BE}}{V_T}\right)$$

A little bit of math... search for i_B

$$i_B = (1-\alpha)i_E \Rightarrow i_B = (1-\alpha)I_{ES}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right]$$

Finally...

$$\beta = \frac{i_C}{i_B} = \frac{\alpha}{1-\alpha}$$

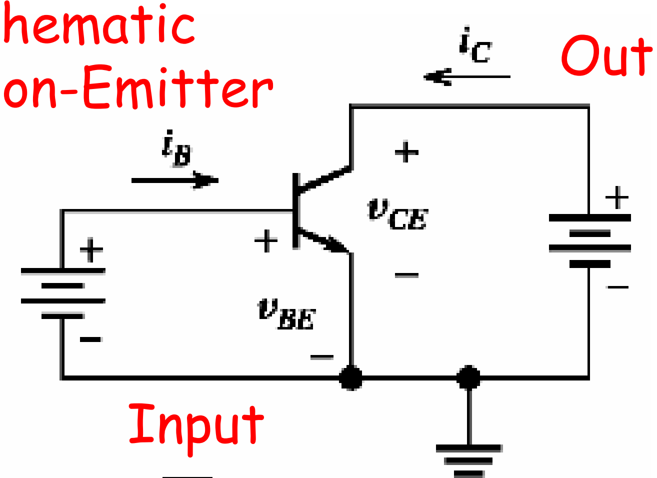
$$i_C = \beta i_B$$

BJTs - Characteristics

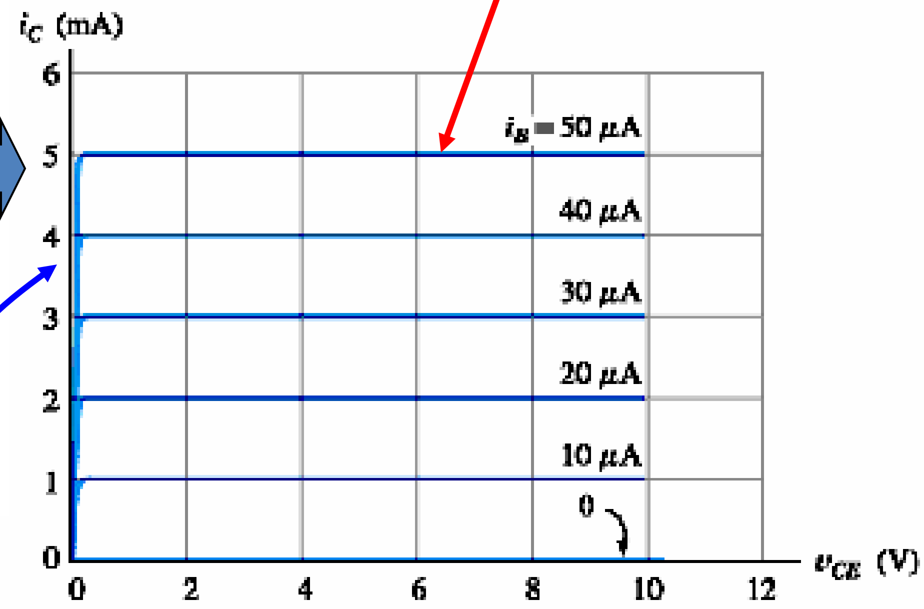
$$i_C = \beta i_B$$

Schematic
Common-Emitter

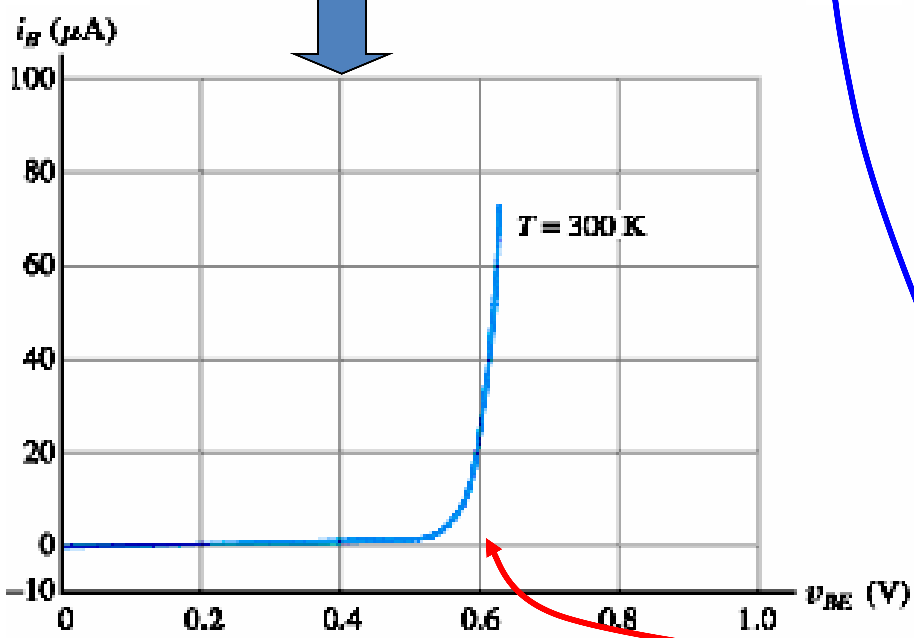
Output



Input



(b) Output characteristics



(a) Input characteristic

$V_{BC}<0$ or equivalently $V_{CE}>V_{BE}$

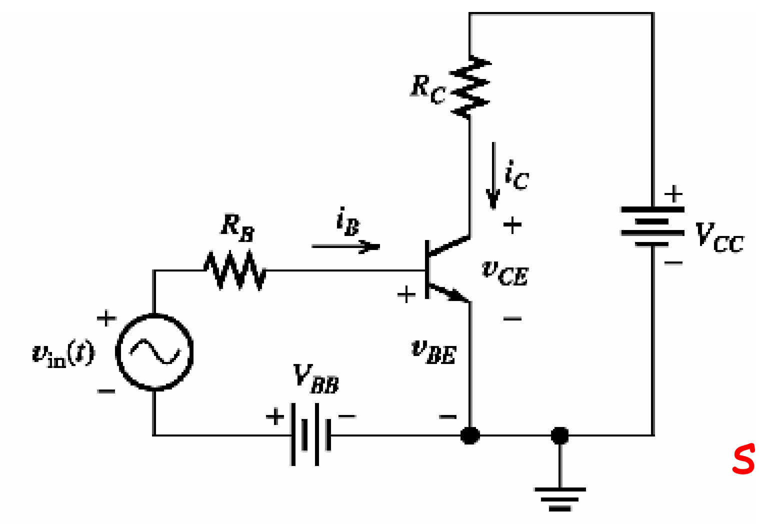
If $V_{CE}<V_{BE}$ the B-C junction is forward bias and I_C decreases

Remember V_{BE} has to be greater than 0.6-07 V

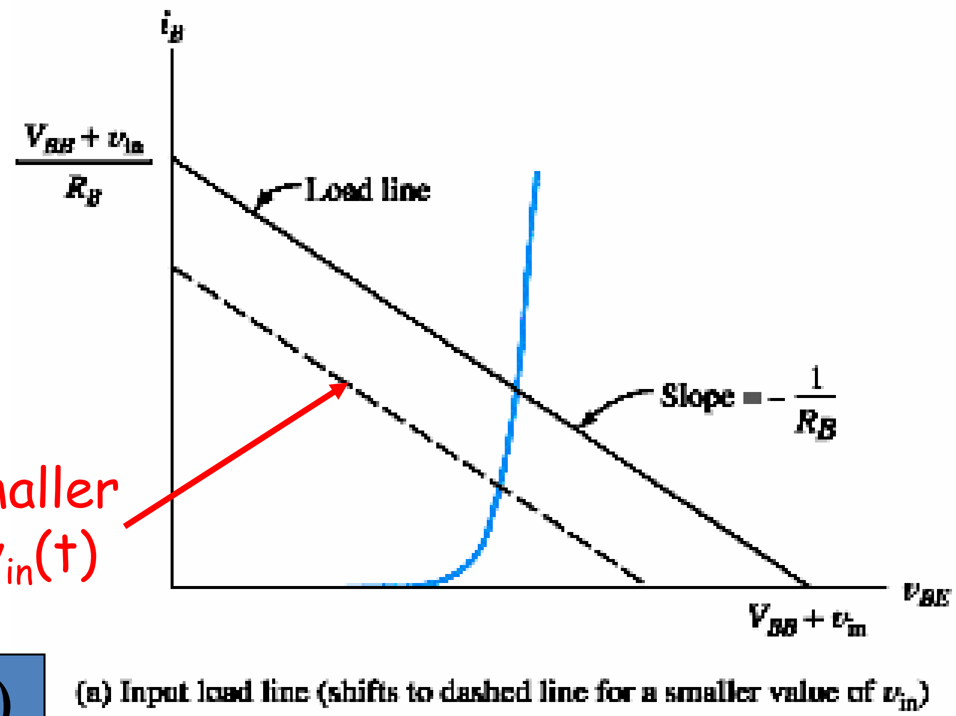
Example 13.1

BJTs - Load line analysis

Common-Emitter Amplifier



Input loop



smaller $v_{in}(t)$

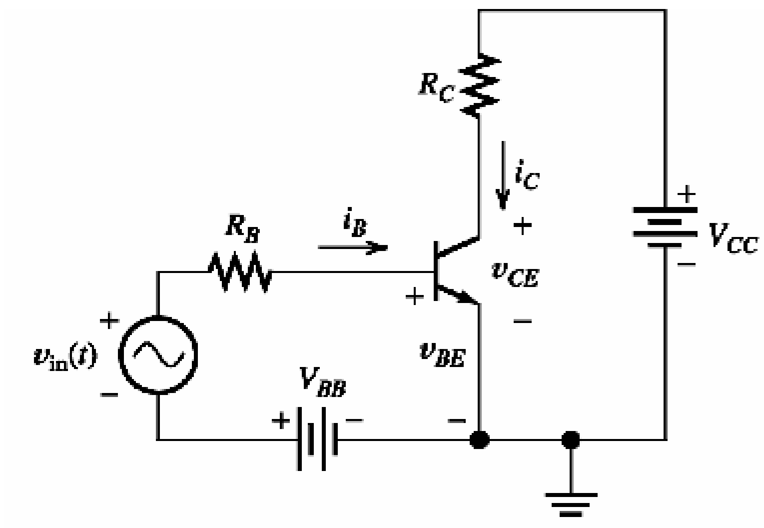
$$V_{BB}+v_{in}(t)=R_B i_B(t)+v_{BE}(t)$$

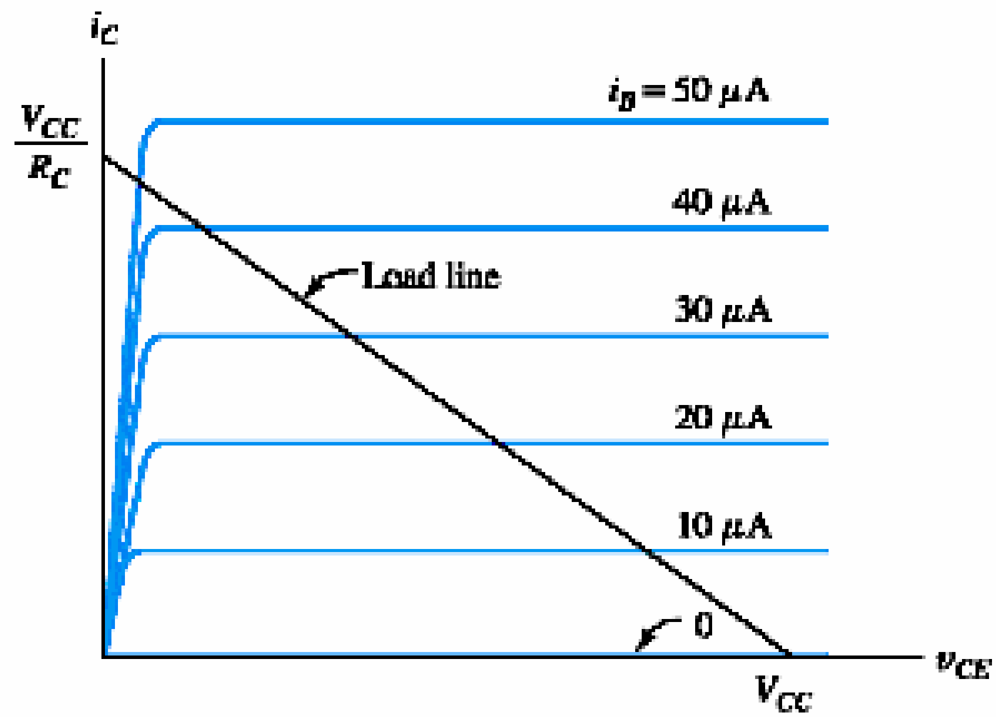
if $i_B=0$ $\quad v_{BE}=V_{BB}+v_{in}$

if $v_{BE}=0$ $\quad i_E=(V_{BB}+v_{in})/R_B$

BJTs - Load line analysis

Common-Emitter Amplifier





Output loop

$$V_{CC} = R_C i_C + v_{CE}$$

Example 13.2

Circuit with BJTs

Our approach: Operating point - dc operating point
Analysis of the signals - the signals to be amplified

Circuit is divided into: model for large-signal dc analysis of BJT circuit
bias circuits for BJT amplifier
small-signal models used to analyze circuits for signals being amplified

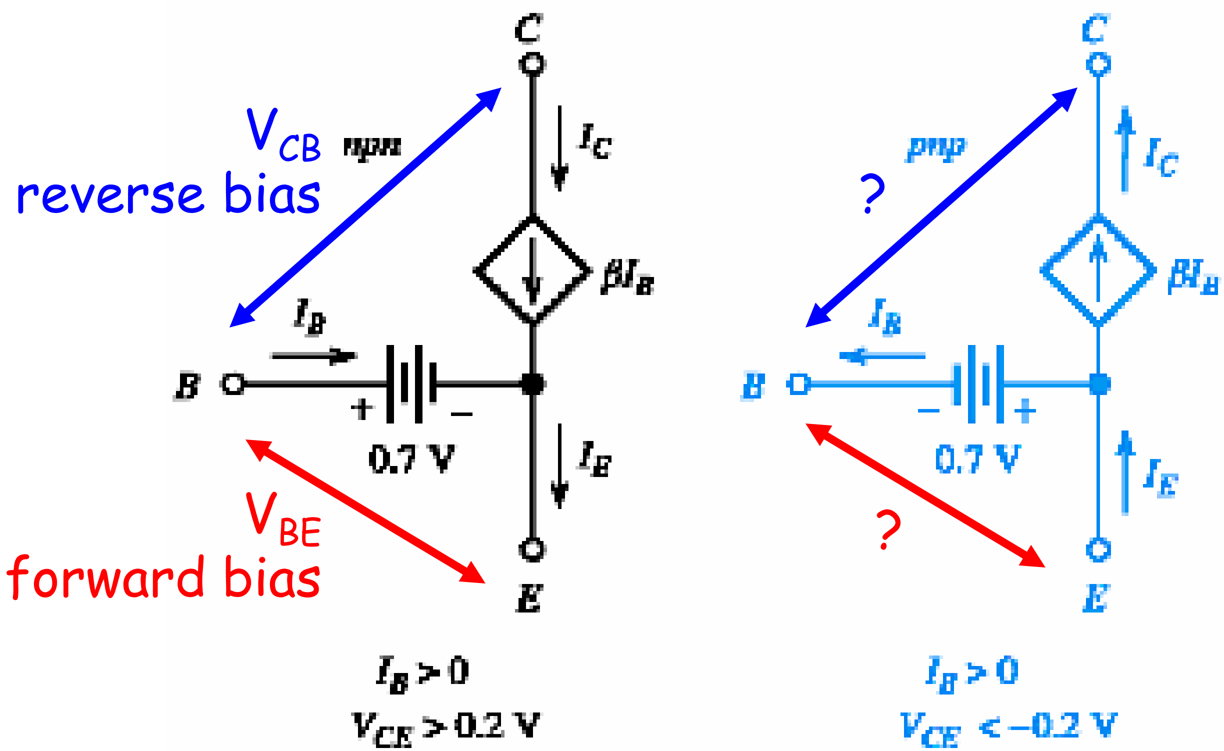
Remember !

Table 2.3 The Four Regions of Operation of a Bipolar Junction Transistor

Region of Operation	Emitter-Base Junction	Collector-Base Junction
Forward active	forward biased	reverse biased
Reverse active	reverse biased	forward biased
Cutoff	reverse biased	reverse biased
Saturated	forward biased	forward biased

Large-Signal dc Analysis: Active-Region Model

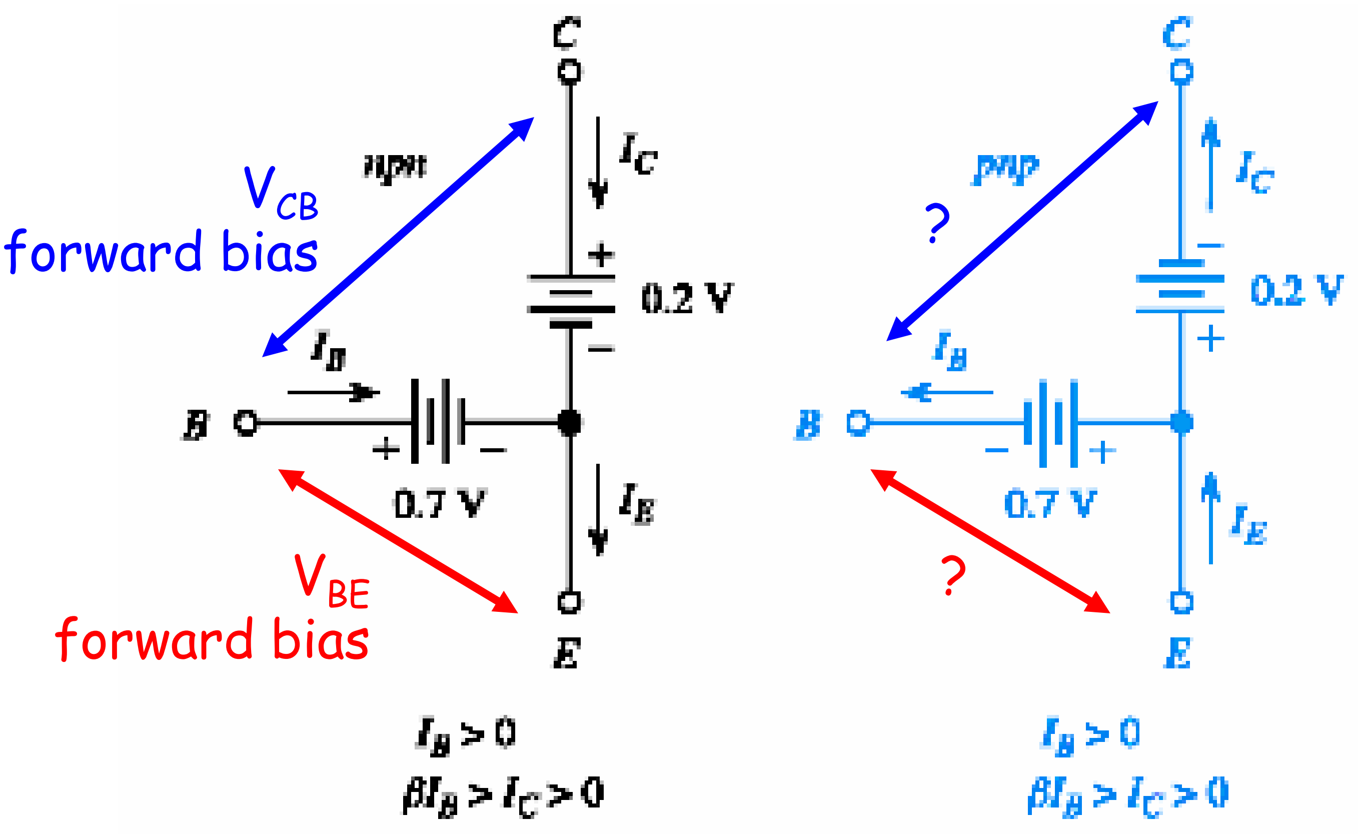
Important: a current-controlled current source models the dependence of the collector current on the base current



(a) Active region

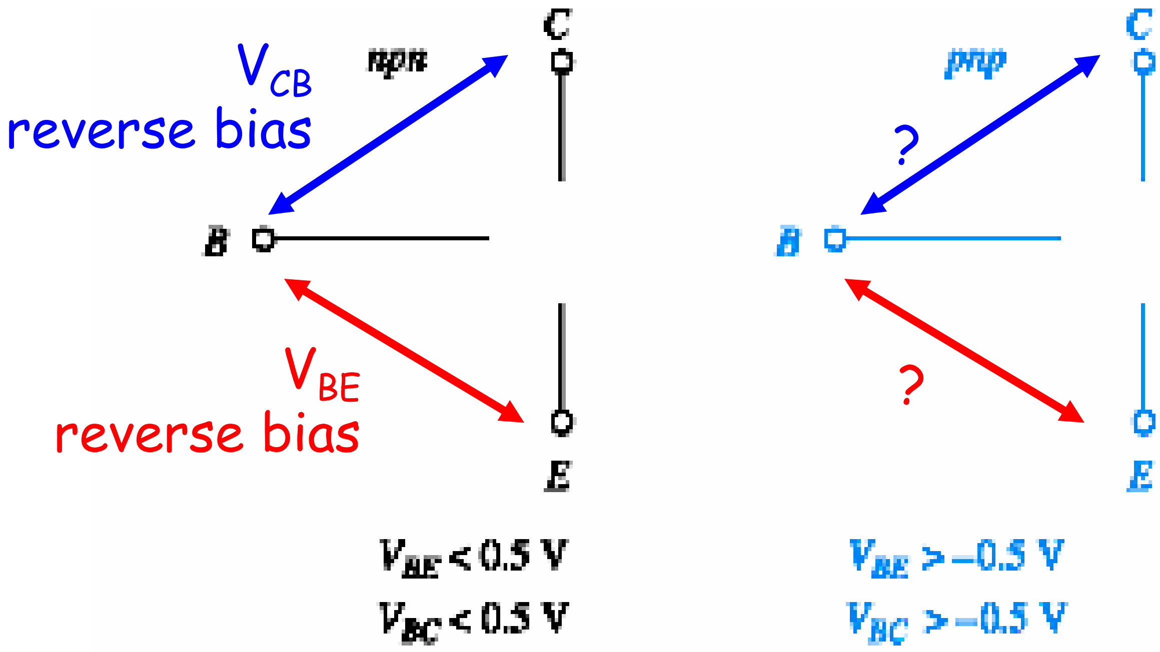
The constrains for I_B and V_{CE} must be satisfy to keep BJT in the active-mode

Large-Signal dc Analysis: Saturation-Region Model



(b) Saturation region

Large-Signal dc Analysis: Cutoff-Region Model



(c) Cutoff region

If small forward-bias voltage of up to about 0.5 V are applied, the currents are often negligible and we use the cutoff-region model.

Large-Signal dc Analysis: characteristics of an npn BJT

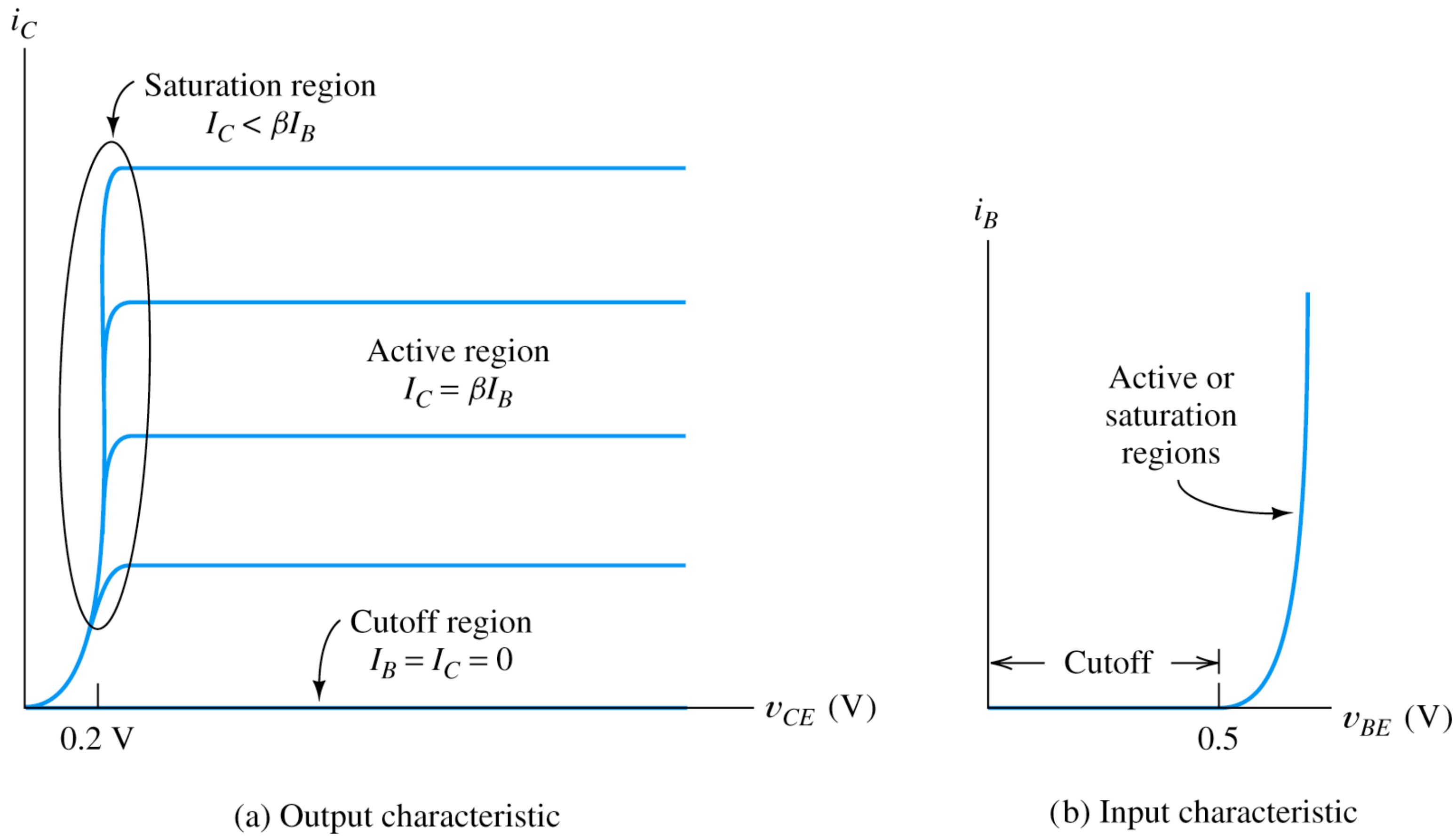


Figure 13.17 Regions of operation on the characteristics of an *npn* BJT.

Large-Signal dc Analysis

Procedure: (1) select the operation mode of the BJT
(2) use selected model for the device to solve the circuit and determine I_C, I_B, V_{BE}, and V_{CE}
(3) check to see if the solution satisfies the constrains for the region, if so the analysis is done
(4) if not, assume operation in a different region and repeat until a valid solution is found

This procedure is very important in the analysis and design of the bias circuit for BJT amplifier.

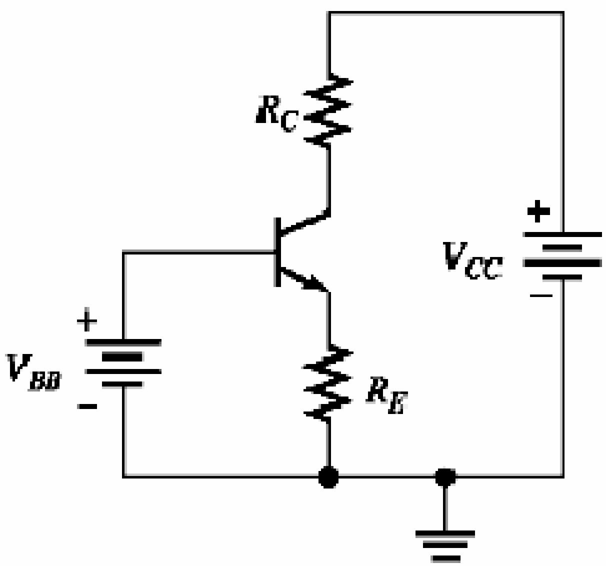
The objective of the bias circuit is to place the operating point in the active region.

Bias point – it is important to select I_C, I_B, V_{BE}, and V_{CE} independent of the β and operation temperature.

Example 6.4, 6.5, 6.6

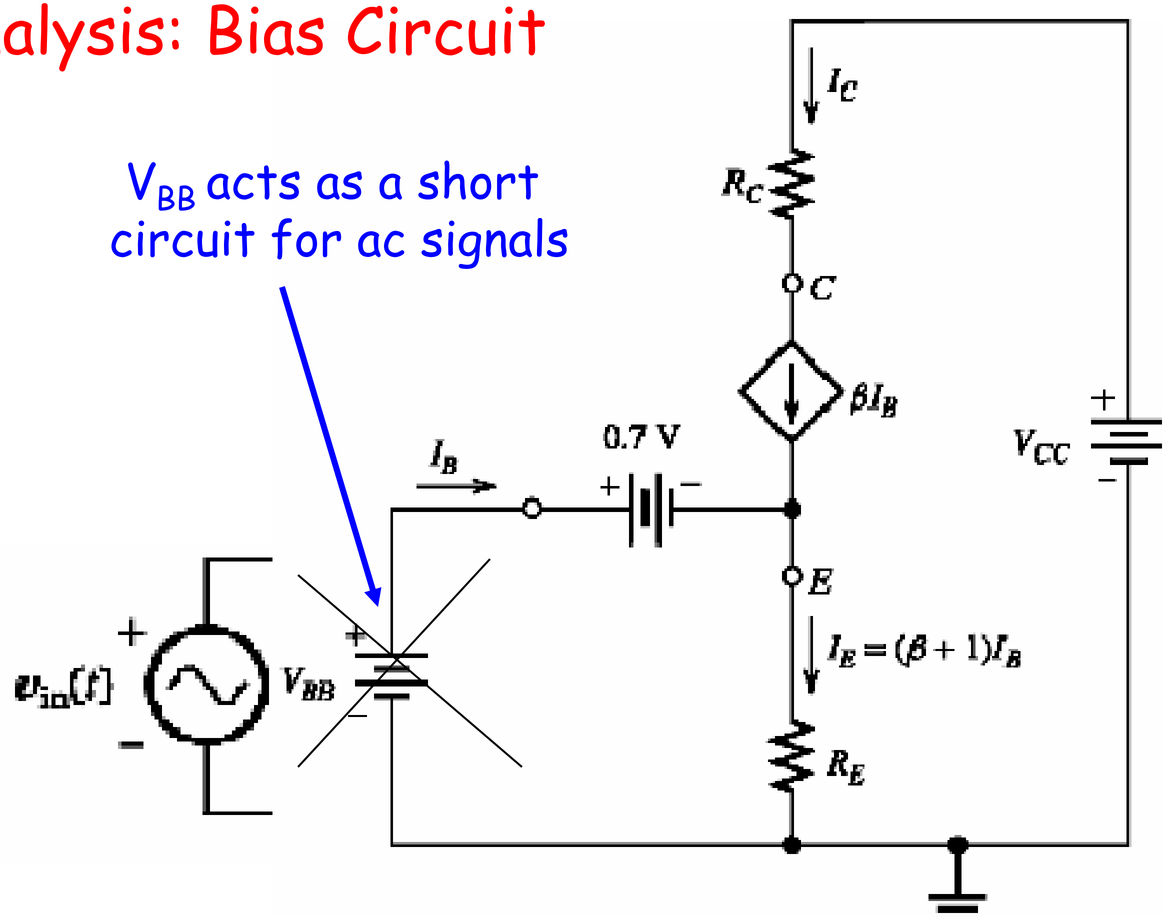
Large-Signal dc Analysis: Bias Circuit

From Example 6.6



(a) Original circuit

V_{BB} acts as a short circuit for ac signals



(b) Equivalent circuit assuming operation in the active region

Remember: that the Q point should be independent of the β (stability issue)

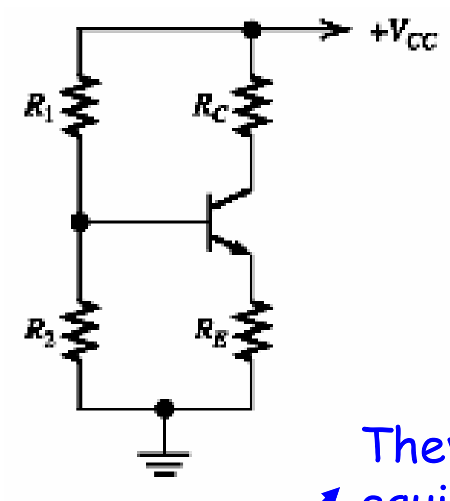
V_{BB} & V_{CC} provide this stability, however this impractical solution

Other approach is necessary to solve this problem-resistor network

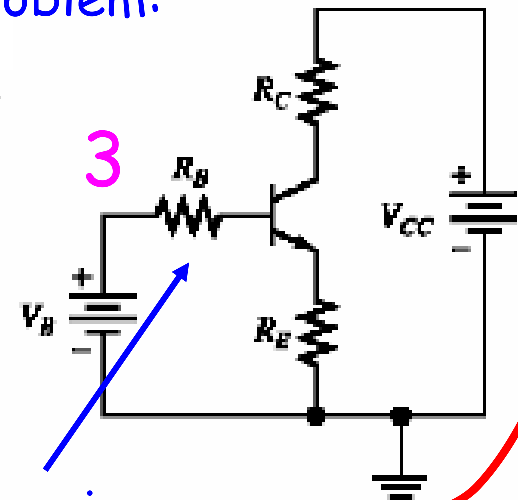
Large-Signal dc Analysis: Four-Resistor Bias Circuit

Solution of the bias problem:

1



3



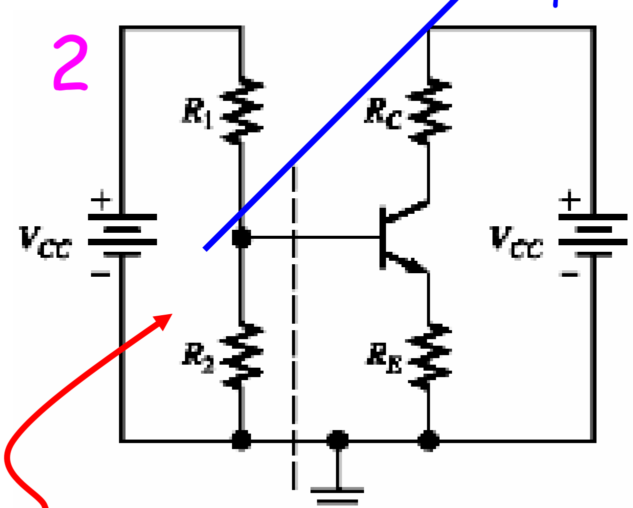
$$V_B = R_B I_B + V_{BE} + R_E I_E$$

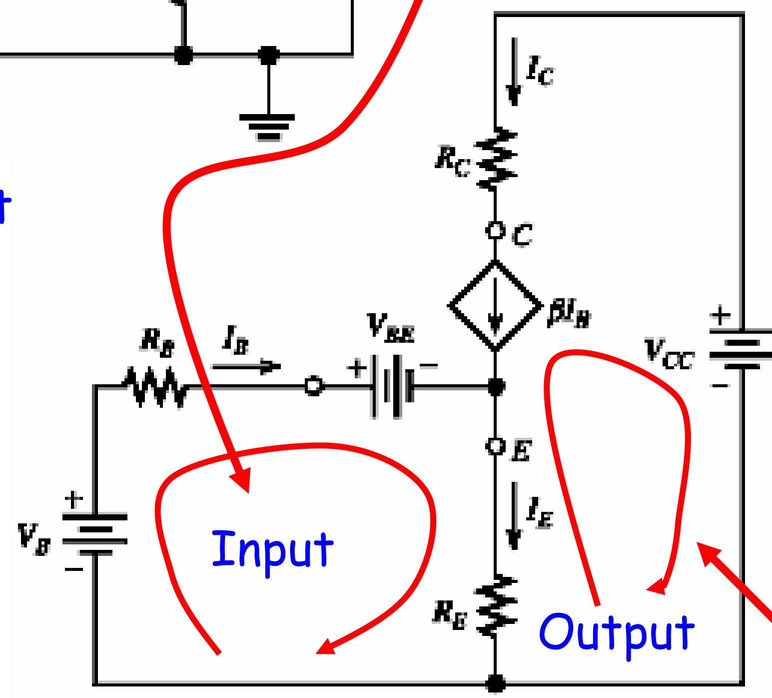
$$I_E = (\beta + 1) I_B \qquad V_{BE} \cong 0.7V$$

$$I_B = \frac{V_B - V_{BE}}{R_B + (\beta + 1) R_E}$$

Thevenin equivalent

2





4

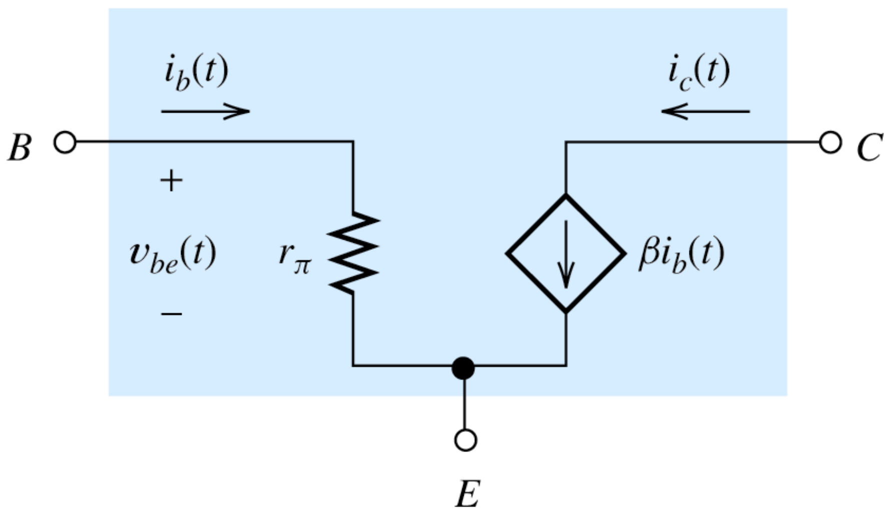
Equivalent circuit for active-region model

$$R_B = R_1 \| R_2 \qquad V_B = V_{CC}\left(R_2 / (R_1 + R_2)\right)$$

$$V_{CE} = V_{CC} - R_C I_C - R_E I_E$$

Small-Signal Equivalent Circuit

Small signal equivalent circuit for BJT:



$$i_B = I_{BQ} + i_b(t) =$$

$$= (1-\alpha) I_{ES} \left[\exp\left(\frac{v_{BEQ} + v_{be}(t)}{V_T} \right) \right]$$

$$= I_{BQ} \left[\exp\left(\frac{v_{be}(t)}{V_T} \right) \right]$$

$$\exp(x) = 1 + x,$$

$$I_{BQ} + i_b(t) = I_{BQ} \left(1 + \frac{v_{be}(t)}{V_T} \right)$$

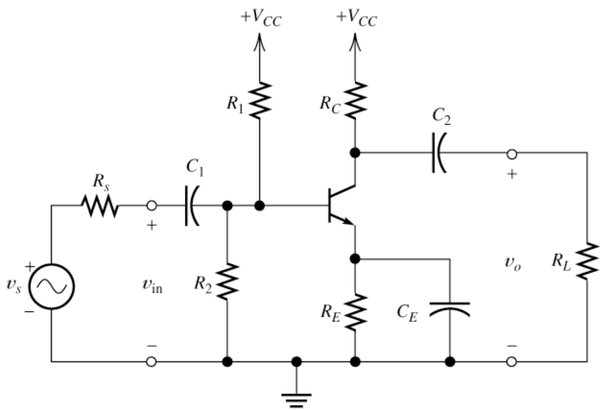
so

$$i_b(t) = I_{BQ} \frac{v_{be}(t)}{V_T} = \frac{v_{be}(t)}{r_\pi}$$

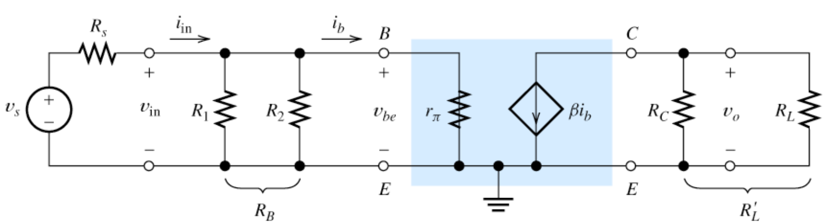
and

$$r_\pi = \frac{V_T}{I_{BQ}}$$

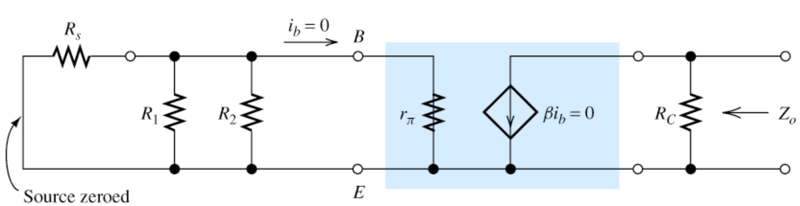
Common Emitter Amplifier



(a) Actual circuit



(b) Small-signal ac equivalent circuit



(c) Equivalent circuit used to find Z_o

First perform DC analysis to find small-signal equivalent parameters at the operating point.

Find voltage gain:

$$v_{in} = v_{be} = r_\pi i_b$$

$$v_o = -R'_L \beta i_b$$

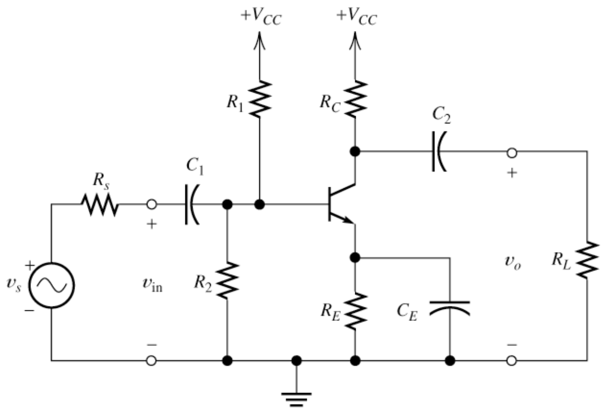
$$A_v = \frac{v_o}{v_{in}} = -\frac{R'_L \beta}{r_\pi}$$

$$A_{voc} = \frac{v_o}{v_{in}} = -\frac{R_C \beta}{r_\pi}$$

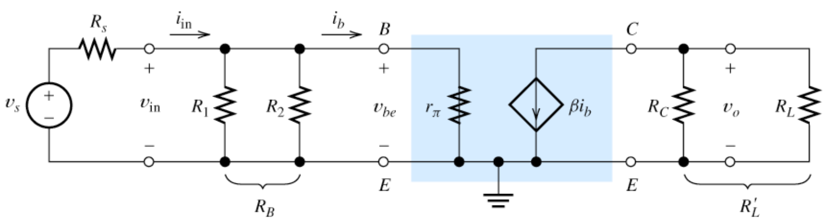
Find input impedance:

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{\frac{1}{R_B} + \frac{1}{r_\pi}}$$

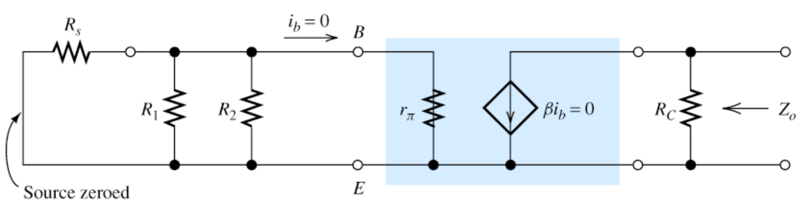
Common Emitter Amplifier



(a) Actual circuit



(b) Small-signal ac equivalent circuit



(c) Equivalent circuit used to find Z_o

Find current gain

$$A_i = \frac{i_o}{i_{in}} = \frac{A_v Z_{in}}{R_L}$$

Find power gain:

$$G = A_i A_v$$

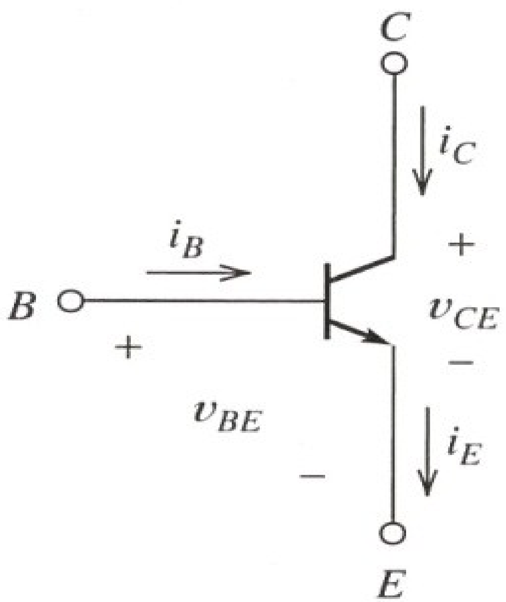
Find output impedance:

$$Z_o = R_C$$

Problem 6.6:

Suppose that a certain *npn* transistor has V_{BE} = 0.7V for I_E =10mA. Compute V_{BE} for I_E = 1mA.

Repeat for I_E = 1μA. Assume that V_T = 26mV.



$$I_E = I_{ES}\left(\exp\left(\frac{V_{BE}}{V_T}\right) - 1\right) \approx I_{ES}\exp\left(\frac{V_{BE}}{V_T}\right)$$

$$10\text{mA} = I_{ES}\exp\left(\frac{0.7}{0.026}\right) \quad \textit{and} \quad 1\text{mA} = I_{ES}\exp\left(\frac{V_{BE}}{0.026}\right)$$

$$\textit{divide both sides} \quad \Rightarrow \quad 10 = \exp\left(\frac{0.7 - V_{BE}}{0.026}\right)$$

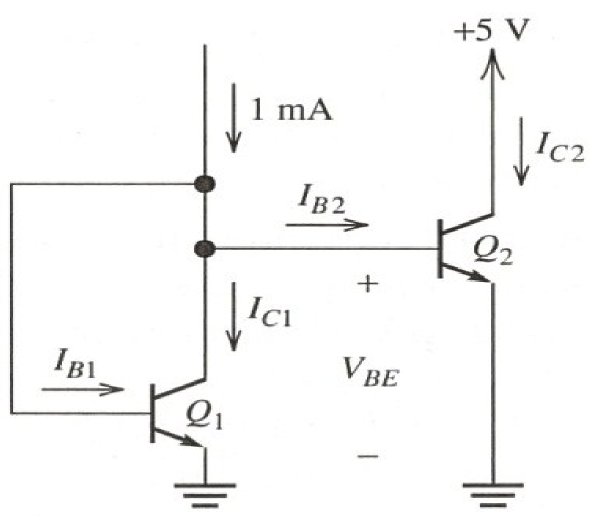
$$\Rightarrow \quad 0.026 * \ln 10 = 0.7 - V_{BE}$$

$$\therefore V_{BE} = 0.7 - 0.026 * \ln 10 = 0.64[V]$$

Problem 6.14:

Consider the circuit shown in Figure P6.14. Transistors Q_1 and Q_2 are identical, both having $I_{ES} = 10^{-14}$A and $\beta = 100$. Calculate V_{BE} and I_{C2}. Assume that V_T = 26mV for both transistors.

Hint: Both transistors are operating in the active region.
Because the transistors are identical and have identical values of V_{BE}, their collector currents are equal.



$$I_{B1} + I_{B2} + I_C = 1mA \quad \& \quad I_C = \beta I_B$$

$$\Rightarrow \quad I_C\left(\frac{2}{\beta}+1\right) = 1mA \quad \Rightarrow \quad I_C = \frac{1mA}{1.02} = 0.98mA$$

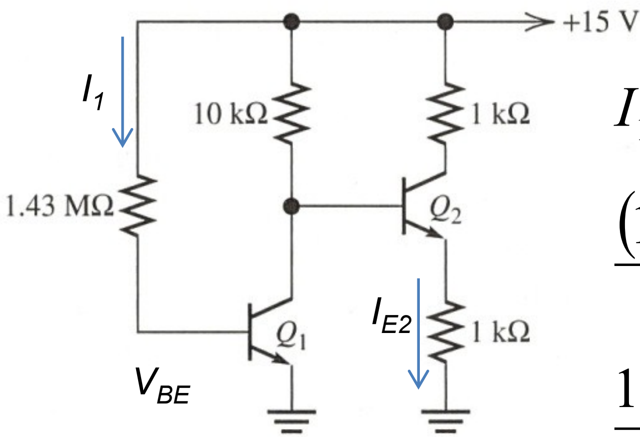
$$I_E = \left(1+\frac{1}{\beta}\right) I_C = 0.99mA$$

$$\sin ce \quad I_E \approx I_{ES}\exp\left(\frac{V_{BE}}{V_T}\right) \quad we\ have$$

$$\therefore V_{BE} = V_T \ln\frac{I_E}{I_{ES}} = 0.026 * \ln\left(0.99*10^{11}\right) = 0.658V$$

Problem 6.50:

The transistors shown in Figure P6.50 operate in active region and have $\beta = 100$, $V_{BE}=0.7V$. Determine I_C and V_{CE} for each transistor.



$$I_1 = \frac{14.3}{1.43M\Omega} = 10\mu A \qquad I_{C1} = \beta I_1 = 1mA$$

$$\frac{\left(15-\left(I_{E2}*1k+0.7\right)\right)}{10k} = I_{C1} + \frac{I_{E2}}{\beta+1}$$

$$\frac{14.3}{10k} - \frac{I_{E2}}{10} = 1mA + \frac{I_{E2}}{101}$$

$$0.43mA = I_{E2} * \left(\frac{1}{101} + \frac{1}{10}\right)$$

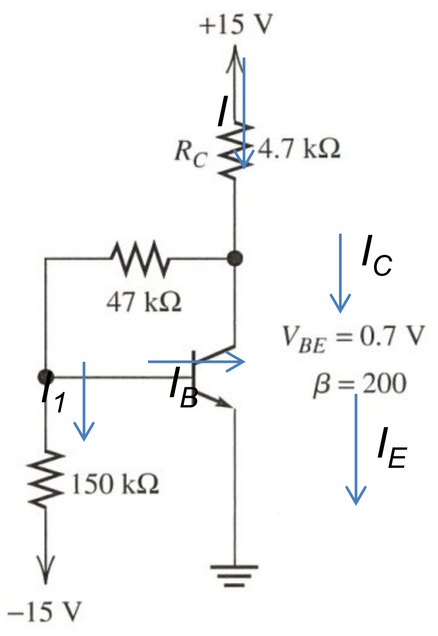
$$I_{E2} = 3.9126mA \quad => \quad I_{C2} = 0.99 I_{E2} = 3.8735mA$$

$$V_{CE2} = 15 - 1k*\left(I_{C2} + I_{E2}\right) = 15 - 1.99k * I_{E2} = 7.213V$$

$$V_{CE1} = 15 - 10k * \left(1mA + \frac{I_{C2}}{\beta}\right) = 4.6126V$$

Problem 6.52:

Analyze the circuit of Figure P6.52 to determine I_C and V_{CE}.



$$I = I_1 + I_E \qquad I_C = \beta I_B$$

$$I_1 = \frac{(0.7-(-15))V}{150K\Omega} = \frac{(0.7+15)V}{150K\Omega} = 0.1047mA \qquad I_E = (\beta+1)I_B$$

$$(I_1 + I_B) * 47k\Omega + 0.7 + I * 4.7k\Omega = 15V$$

$$I_1 * 47k + I_B * 47k + 0.7 + I_1 * 4.7k + (\beta+1) * I_B * 4.7k = 15V$$

$$I_1 * (47k + 4.7k) = 15 - 0.7 - I_B * (47k + 201 * 4.7k)$$

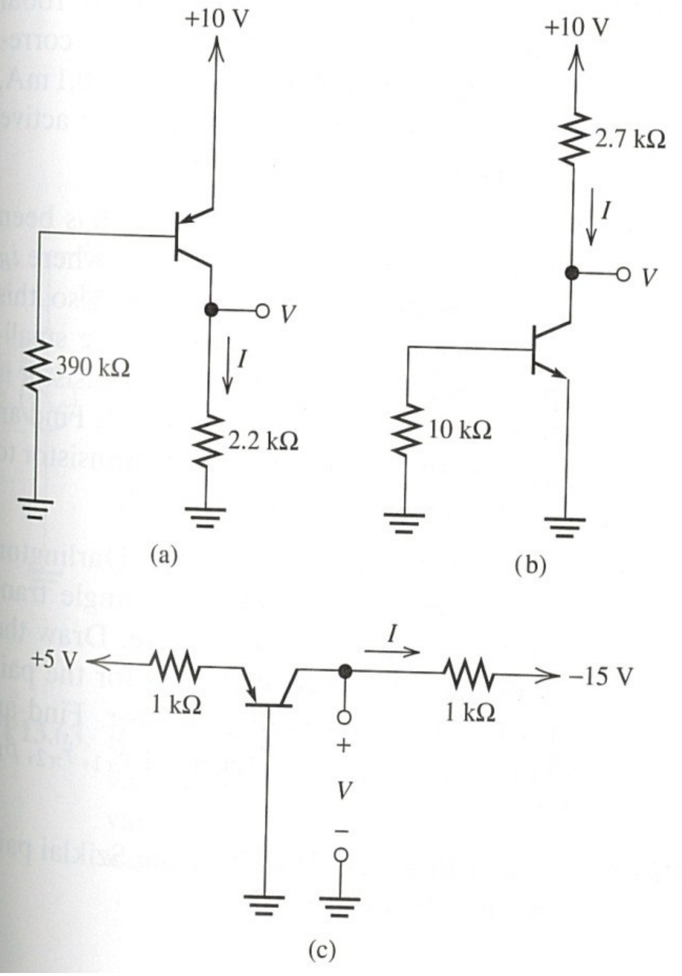
$$I_B = \frac{14.3 - 0.1047mA * 51.7k}{47k + 944.7k} = \frac{14.3 - 5.413}{991.7k} = 9.0\mu A$$

$$I_C = \beta I_B = 1.8mA$$

$$V_{CE} = V_{BE} + 47k * (I_1 + I_B) = 0.7 + 47k * 0.1137mA = 6.04V$$

Problem 6.45:

Analyze the circuits shown in Figure P6.45 to determine I and V. For all transistors, assume that $\beta = 100$ and $|V_{BE}| = 0.7V$ in both the active and saturation regions. Repeat for $\beta = 300$.



(a) for $\beta = 100$

$$|V_{BE}| = 0.7 \quad => \quad V_B = 9.3V$$

$$I_B = \frac{9.3}{390k} = 23.8\mu A$$

$$I_C = \beta I_B = 2.38mA \quad => \quad V = I_C * 2.2k = 5.236\,V$$

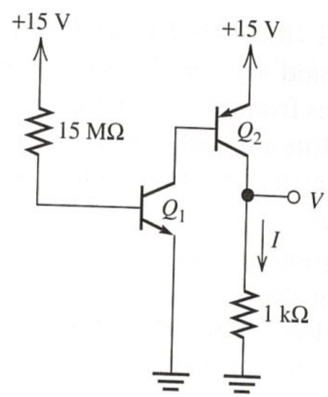
for $\beta = 300$

$$I_C = 7.15mA \quad => \quad V = I_C * 2.2k = 15.73V \quad (\text{Incorrect})$$

$$\text{Since } V_{\max} = 9.8V \quad => \quad I_{C\max} = \frac{9.8}{2.2k} = 4.43mA$$

$$=> \beta_{\max} = \frac{I_{\max}}{I_B} = \frac{4.42mA}{23.8\mu A} = 187.2$$

Problem 6.45: Contd.



(d) For $\beta = 100$

$$I_{B1} = \frac{14.3}{15M\Omega} = 0.9533\mu A \qquad I_{C1} = \beta I_{B1} = 95.33\mu A = I_{B2}$$

$$I = I_{C2} = I_{B2} * \beta = 9.533mA \quad => \quad V = I * 1k = 9.533\,V$$

For $\beta = 300$, $\mathrm{I_{B2}} = 286\mu A$ => $I_{C2} = I_{B2} * \beta = 85.8mA$

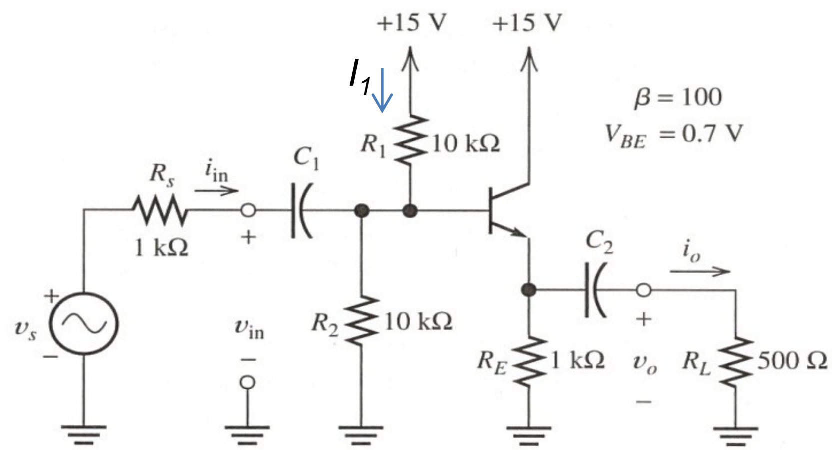
(would give $\mathrm{V} = 85.8V$, Incorrect)

$I_{C2} = \beta^2 I_{B1}$ and since $\mathrm{V_{max}} = 14.8V$ $\quad I_{\max} = 14.8mA = I_{C2\max}$

$$\beta_{\max} = \sqrt{\frac{I_{C2\max}}{I_{B1}}} = \sqrt{\frac{14.8mA}{0.953\mu A}} = 124.5$$

Problem 6.67:

Consider the emitter-follower amplifier of Figure P6.67 . Draw the dc circuit and find I_{CQ}. Next, determine the value of r_π. Then, calculate midband values for A_v, A_{voc}, Z_{in}, A_i, G and Z_0.



DC Analysis

$$I_1 * 10k + (I_1 - I_{BE}) * 10k = 15\,V \quad \Rightarrow \quad I_1 * 20k - I_B * 10k = 15\,V$$

$$15 - I_1 * 10k - 0.7 = (1+\beta) * I_B * 1k\Omega \quad \Rightarrow \quad I_1 * 10k + I_B * 101k = 14.3\,V$$

multiply 2nd equation by 2 and subtract the first one

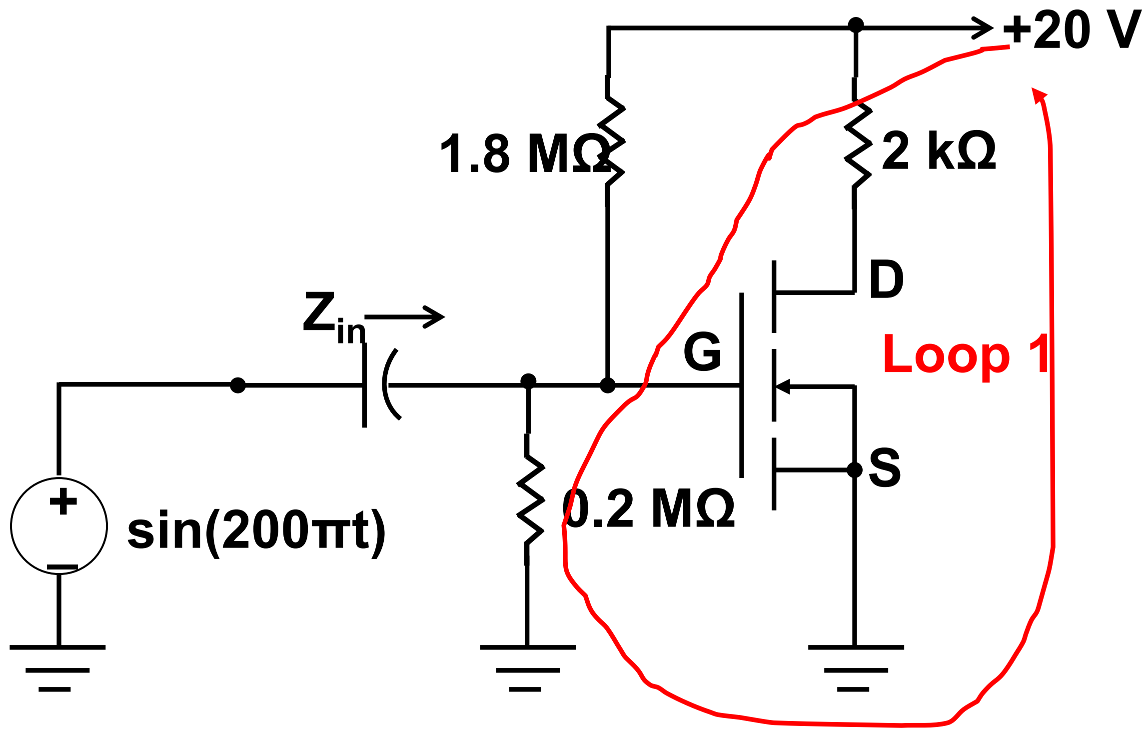
$$I_B * (202k + 10k) = 28.6 - 15 \qquad I_B = \frac{13.6}{212k} = 64.2\,\mu A$$

$$I_{CQ} = I_B * \beta = 6.42\,mA$$

Problem 8: Consider the amplifier shown below.
a) Find $v_{GS}(t)$. Assume that the coupling capacitor is a short circuit for the ac signal and an open circuit for the dc.

Soln (a): In loop 1 the 1.8 MΩ and 200 kΩ resistors act as voltage divider. The voltage drop across 200 kΩ resistor is the dc voltage V_{GSQ}

$V_{GSQ} = 20*0.2/2 = 2$ V



Treating the capacitor as short for ac signals, we have
$V_{GS} = 2 + \sin(200\pi t)$

b) If the FET has V_{t0} = 1V and K = 0.5 mA/V², sketch its drain characteristics to scale for V_{GS} = 1, 2, 3, and 4 V.
c) Draw the load line for the amplifier on the characteristics.
d) Find the values of V_{DSQ}, V_{DSmin}, and V_{DSmax}.

To obtain the drain characteristics apply the following equations

$$i_D = \begin{cases} 0 & when\ v_{GS} < V_{t0} \\ K[2(v_{GS} - V_{t0})v_{DS} - v_{DS}^2] & when\ (V_{GS} - V_{t0}) > 0 \\ K(v_{GS} - V_{t0})^2 & when\ v_{DS} > (v_{GS} - V_{t0}) > 0 \end{cases}$$

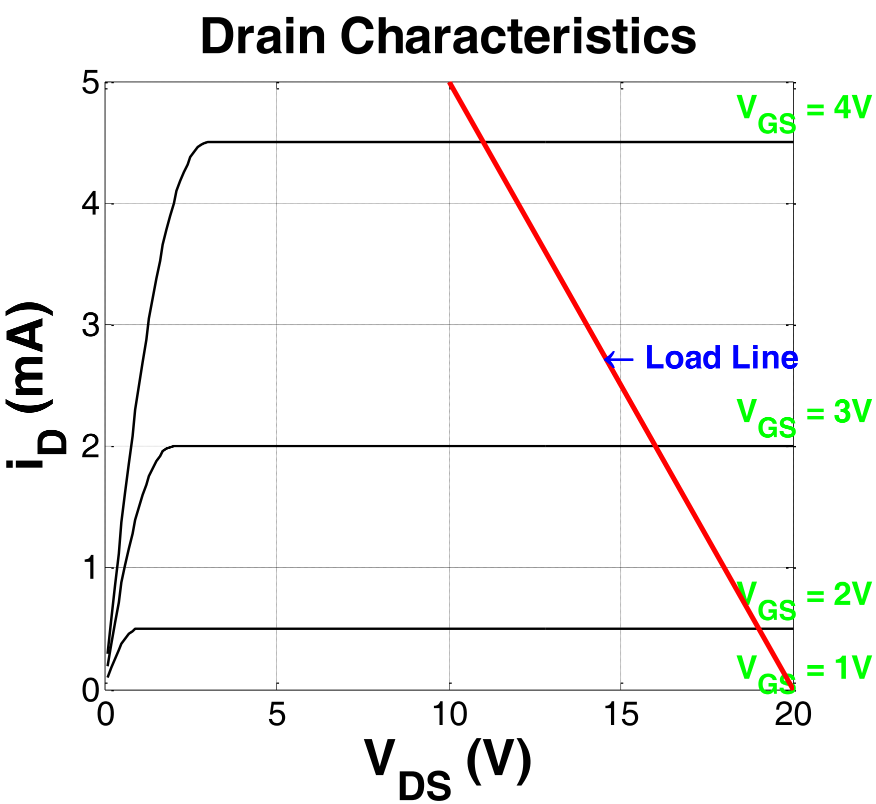
$$i_D = \begin{cases} 0 & when\ v_{GS} < V_{t0} \\ K[2(v_{GS} - V_{t0})v_{DS} - v_{DS}^2]\ when\ (V_{GS} - V_{t0}) > 0 \\ K(v_{GS} - V_{t0})^2 & when\ v_{DS} > (v_{GS} - V_{t0}) > 0 \end{cases}$$

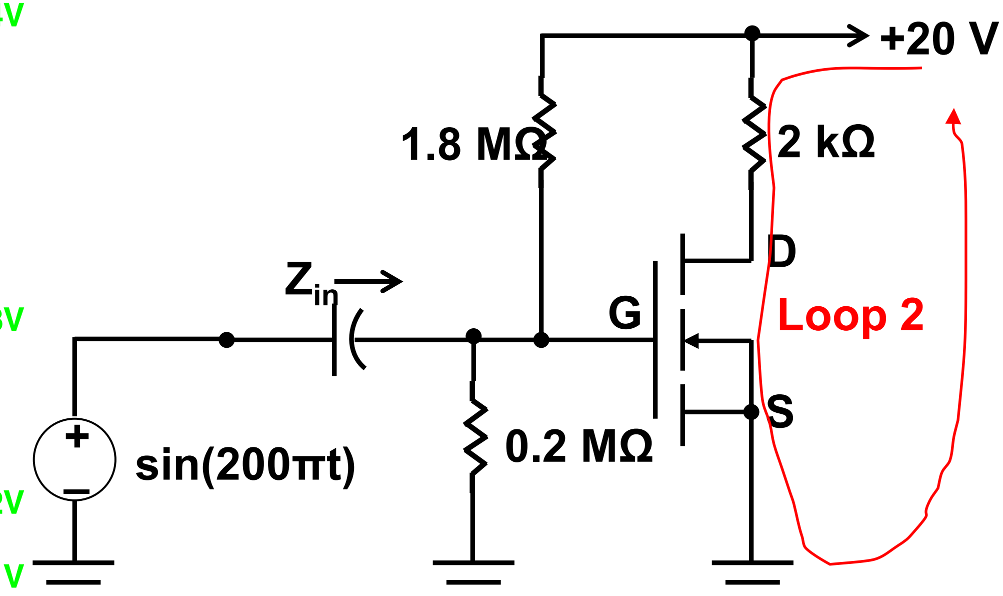
b) Plot shows the drain characteristics for V_{GS} = 1, 2, 3, and 4 V.

c) To get the load line apply KVL to loop 2:

$$20 - 2\ k\Omega * i_D(t) = V_{DS}(t)$$

The red line in the plot is the load line.

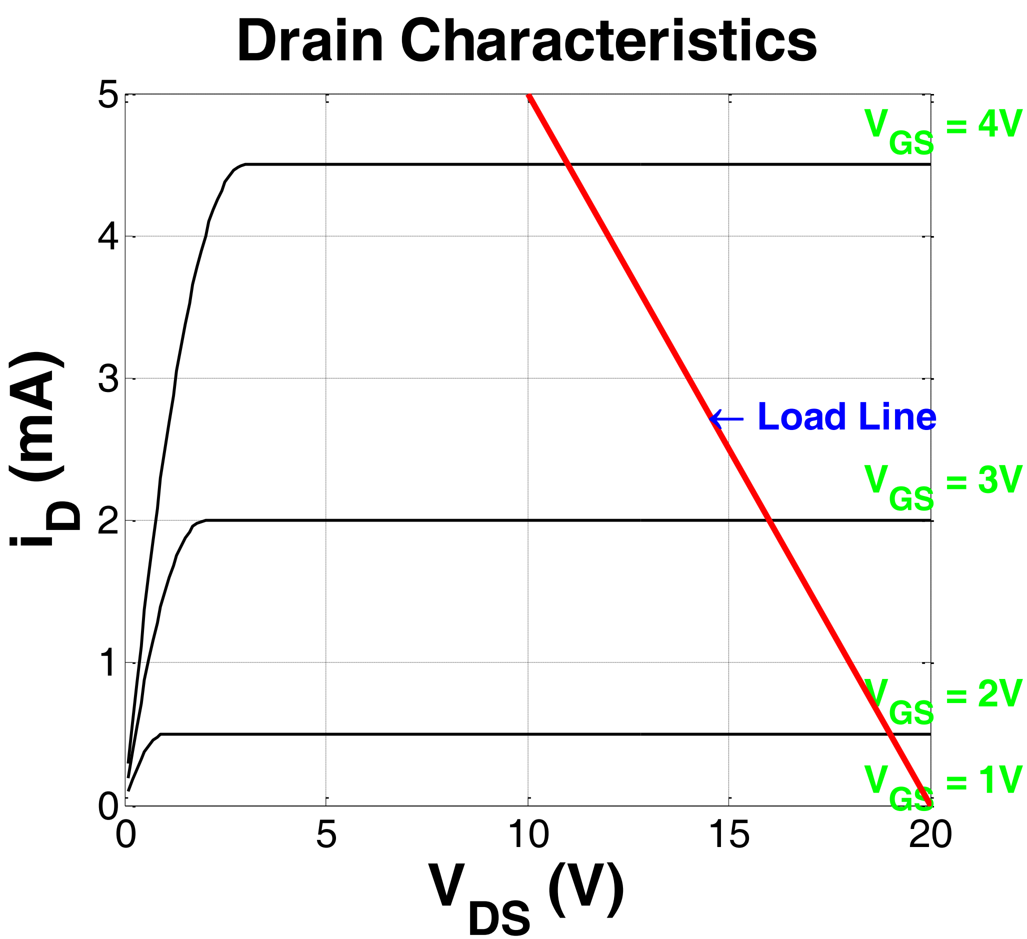




d) Find the values of V_{DSQ}, V_{DSmin}, and V_{DSmax}.

d) V_{DSQ}, V_{DSmin}, and V_{DSmax} are the points at which the load line intersects the drain characteristics for V_{GS} = 2 V, 3 V and 1 V respectively.

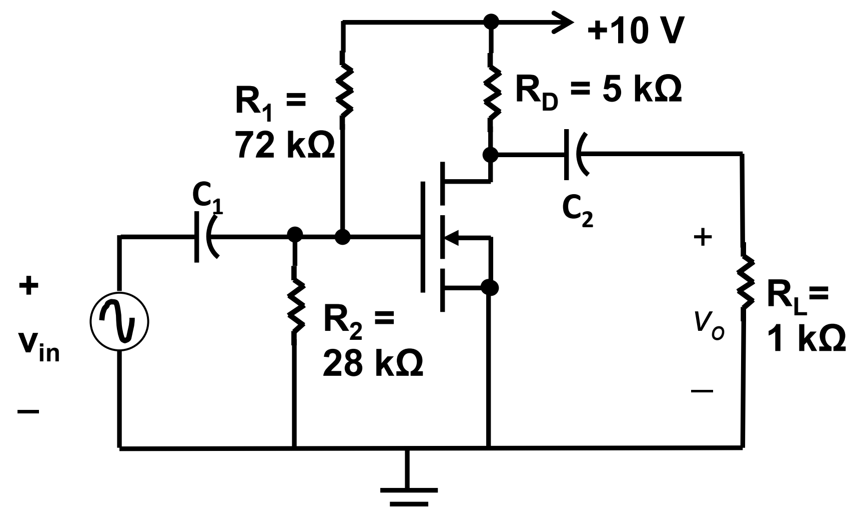
$$V_{DSQ} = 19\text{ V}$$
$$V_{DSmin} = 16\text{ V}$$
$$V_{DSmax} = 20\text{ V}$$



Problem 9: Consider the common source amplifier shown below. Assume NMOS transistor has the following parameters:
KP=60 $\mu A/V^2$, L=5 μm, W=100 μm, r_d=∞, and V_{to}=1.5 V.

a) Find the values of I_{DQ}, $V_{DSQ}$and g_m

The 72 kΩ and 28 kΩ resistors act as a voltage divider. The voltage drop across 28 kΩ resistor is the dc voltage V_{GSQ} is equal to



$$\mathrm{V}_{GSG} = V_{DD}\frac{R_2}{R_1+R_2} = 10\frac{28}{72+28} = 2.8V$$

$$\mathrm{K} = \frac{1}{2}KP\left(\frac{W}{L}\right) = 0.6mA/V^2$$

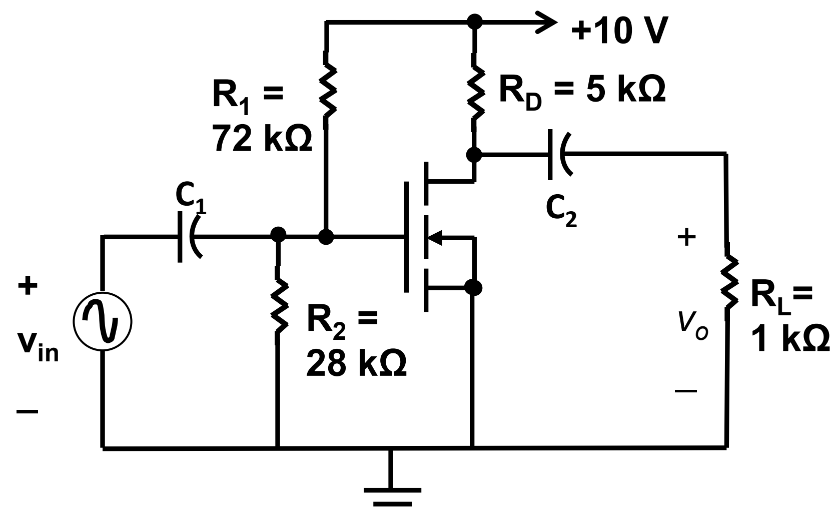
$$V_{DSQ} = \left(V_{DD} - R_D I_{DQ}\right) = 4.93V$$

$$I_{DQ} = K\left(V_{GSQ} - V_{to}\right)^2 = 1.014mA$$

$$g_m = 2\sqrt{KI_{DQ}} = 1.56mS$$

Problem 9 b): - Assuming that the coupling capacitors are short circuits for the ac signal, determine the following: voltage gain, input resistance and output resistance.

$$R_L' = \frac{1}{\frac{1}{R_D} + \frac{1}{R_L}} = 833.3\Omega$$

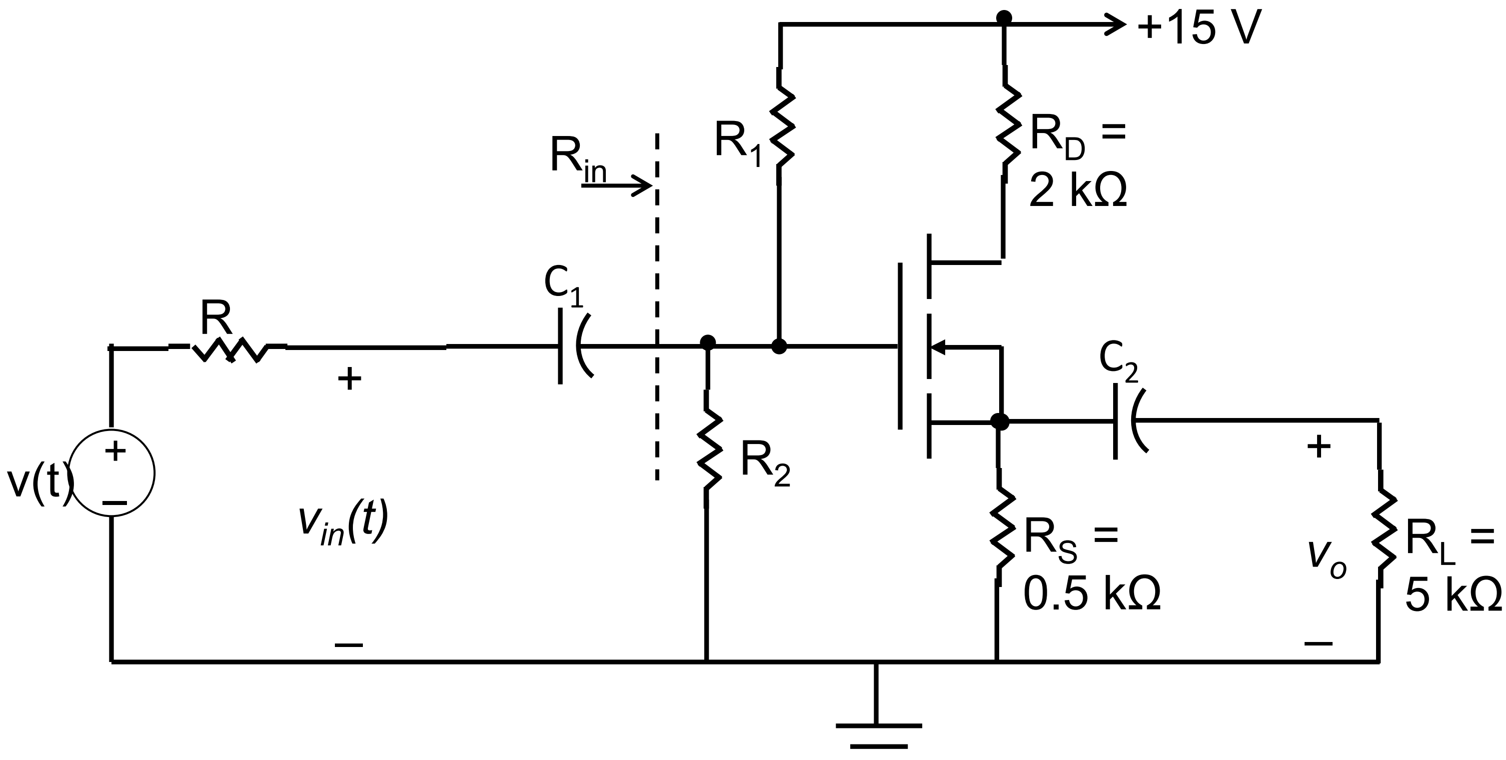


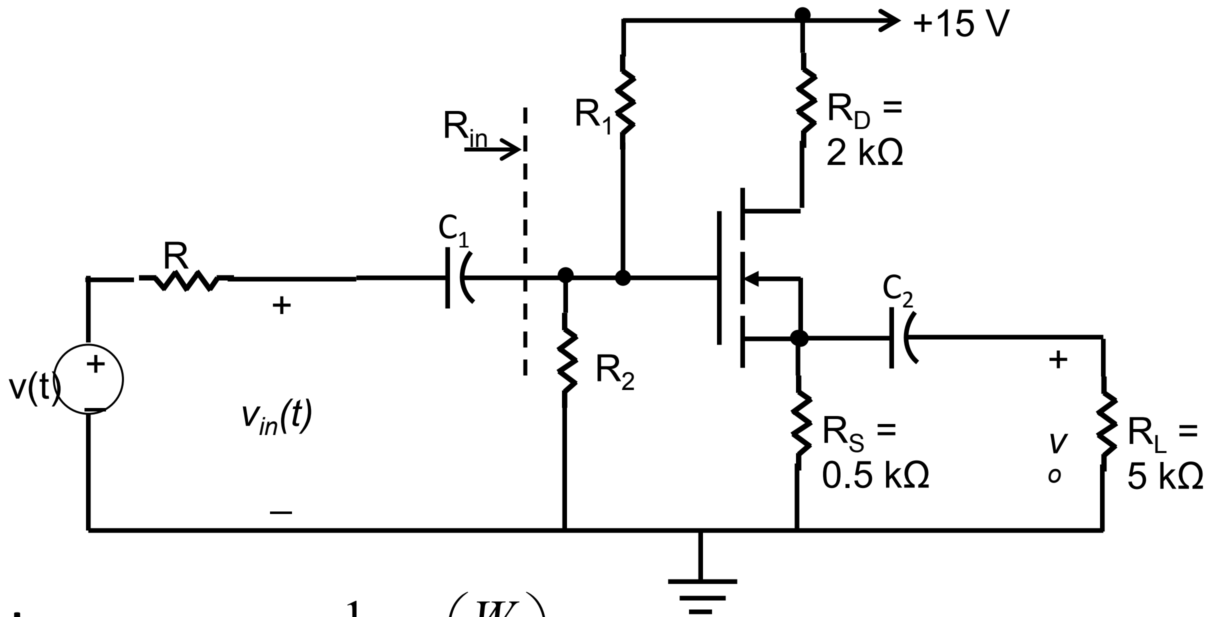
$$A_v = -g_m R_L' = -1.3$$

$$R_{in} = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2}} = 20.16k\Omega$$

$$R_o = R_D = 5k\Omega$$

Problem 10: - Consider the common source amplifier shown below. Assume NMOS transistor has the following parameters:
KP=75 $\mu A/V^2$, L=10 μm, W=400 μm, r_d=∞, and V_{to}=1 V.
a) If R_{in} = 250 kΩ, find the values for R_1 and R_2 to achieve I_{DQ}=2 mA.





- We have: $K = \frac{1}{2} KP\left(\frac{W}{L}\right) = 1.5mA/V^2$
- Given:

$$I_{DQ} = K\left(V_{GSQ} - V_{to}\right)^2 = 2mA \Rightarrow V_{GSQ} = V_{to} + \sqrt{I_{DQ}/K} = 2.155V$$

$$V_S = R_S I_{DQ} = 1V \qquad V_G = V_{GSQ} + V_S = 3.155V$$

$$V_G = V_{DD}\frac{R_2}{R_1 + R_2} = V_{DD}\frac{1}{R_1}R_{in}$$

- Solve for R_1: $R_1 = V_{DD}\frac{1}{V_G}R_{in} = 15 * \frac{1}{3.155} * 250 * 10^3 = 1.19M\Omega$

- We have R_{in} = 250 kΩ and R_1 = 1.19 M Ω

$$R_{in} = \left(R_1 \parallel R_2\right) = \frac{R_1 * R_2}{R_1 + R_2}$$

- Solve for R_2:

$$250k = \frac{1.19M * R_2}{1.19M + R_2} \Rightarrow R_2 = 316.5k\Omega$$

b) Determine the voltage gain

$$R_L^{'} = \frac{1}{{}^{1}\!/\!_{R_d} + {}^{1}\!/\!_{R_L} + {}^{1}\!/\!_{R_S}} = 454.54\Omega$$

$$g_m = 2\sqrt{KI_{DQ}} = 3.46mS$$

$$A_v = \frac{v_0}{v_{in}} = -g_m R_L^{'} = -1.572$$

Problem BJT P1: It has been found that in the circuit below V_E = 1V. If V_{BE} = -0.6V, determine: V_B, I_B, I_E, I_C, β, and α.

Soln (a): From KVL: $$5\text{V} = \text{I}_\text{E} * R_E + 1V$$

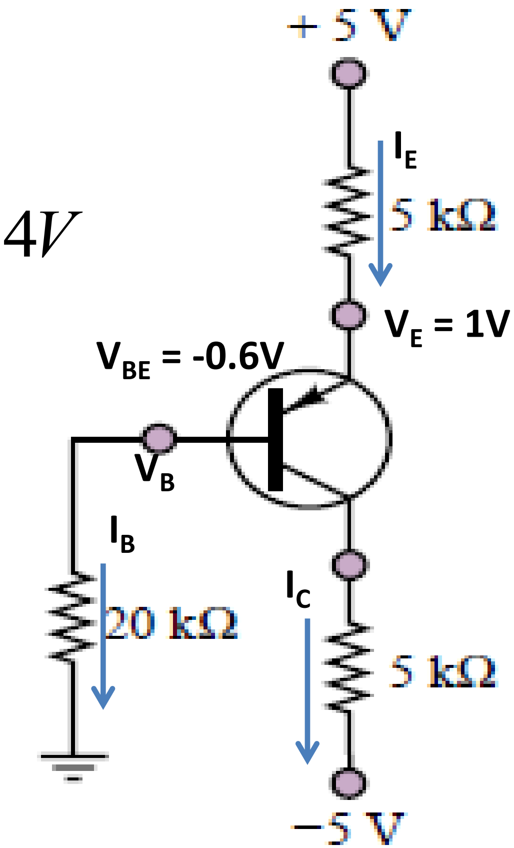
$$\Rightarrow \quad 4\text{V} = \text{I}_\text{E} * 5000 \quad \Rightarrow \quad \text{I}_\text{E} = 0.8mA$$

From KVL: $$V_B = V_E - V_{EB} = 1 - 0.6 = 0.4V$$

Ohm's law: $$V_B = I_B * R_B$$

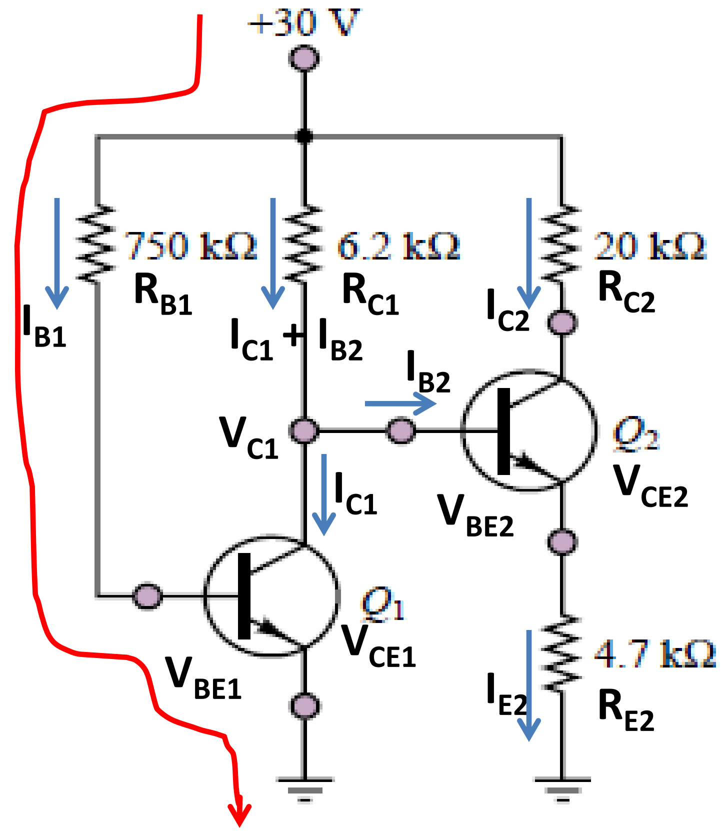
$$0.4\text{V} = I_B * 20k\Omega \quad \Rightarrow \quad I_B = 20\mu A$$

$$I_C = I_E - I_B = 0.78mA$$



$$\beta = \frac{I_C}{I_B} = 39 \qquad \alpha = \frac{I_C}{I_E} = 0.975$$

Problem BJT P2: - For the circuit below assume both transistors are silicon-based with β = 100. Determine: **a)** I_{C1}, V_{C1}, V_{CE1}. **b)** I_{C2}, V_{C2}, V_{CE2}.



- **Soln:**

  Assume $V_{BE} = V_{BE1} = V_{BE2} = 0.7V$

- **Part (a): -** Apply KVL along the path (red line).

$$-30 + I_{B1} * R_{B1} + V_{BE1} = 0$$

$$I_{B1} = \frac{30 - 0.7}{750 * 10^3} = 39.07 \mu A$$

$$I_{C1} = \beta * I_{B1} = 3.907 mA$$

- **Part (a) contd.:** - Apply KVL along the path (red line).

$$30-(I_{C1}+I_{B2})R_{C1}-V_{BE2}-I_{E2}R_{E2}=0$$

We know that $I_E=(\beta+1)I_B$

substituting we get

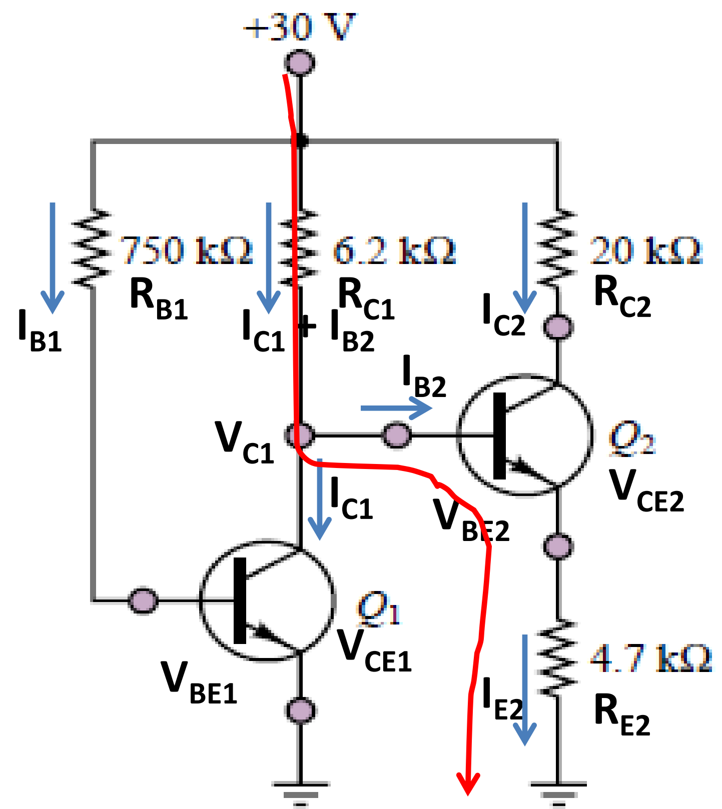
$$30-24.2234-I_{B2}R_{C1}-0.7-(\beta+1)I_{B2}R_{E2}=0$$

$$5.0766-I_{B2}(R_{C1}+101*R_{E2})=0 \Rightarrow I_{B2}=10.559\mu A$$

$$V_{C1}=30-(I_{C1}+I_{B2})*R_{C1}$$

$$V_{C1}=30-(3.907+0.010559)*6.2$$
$$=5.7111\,[V]$$

$$V_{CE1}=V_{C1}=5.7111V$$



- **Part (b): -** Apply KVL along the path (red line).

$$I_{E2} = (1+\beta)I_{B2} = 101*10.559\mu A = 1.0662mA$$

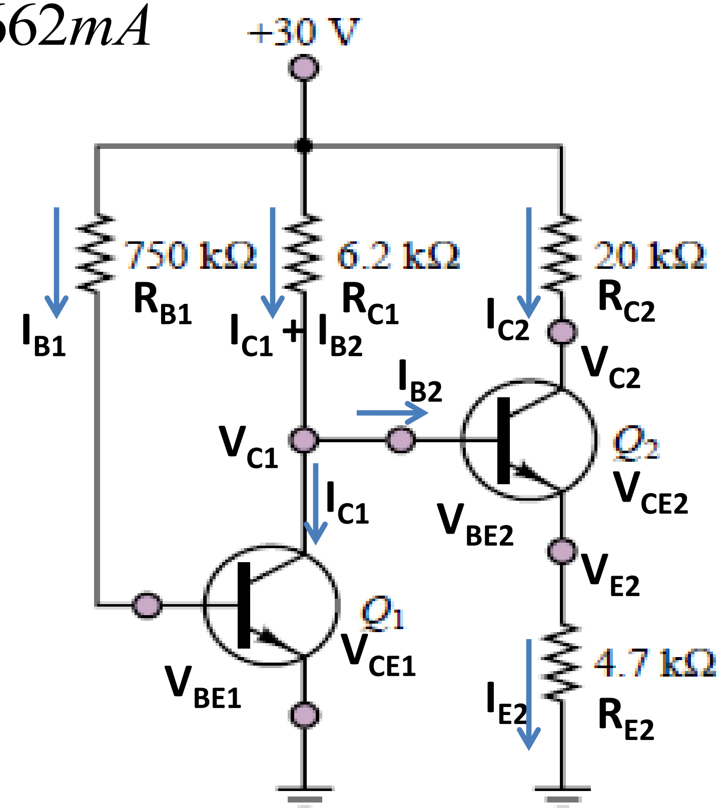
$$I_{C2} = I_{B2}\beta = 1.0556mA$$

$$V_{C2} = 30 - I_{C2}R_{C2}$$

$$V_{C2} = 30 - 1.0556*20 = 8.888V$$

$$V_{E2} = I_{E2}R_{E2} = 5.0111V$$

$$V_{CE2} = V_{C2} - V_{E2} = 3.8769V$$



Problem BJT P3: - Design the bias circuit (find R_C and R_B) to give a Q-point of I_C = 20µA and V_{CE} = 0.9V if the transistor current gain β_F = 50 and V_{BE} = 0.65V.
What is the Q-point if the current gain of the transistor is 125?

- **Soln:** Apply KVL along the path (red line).

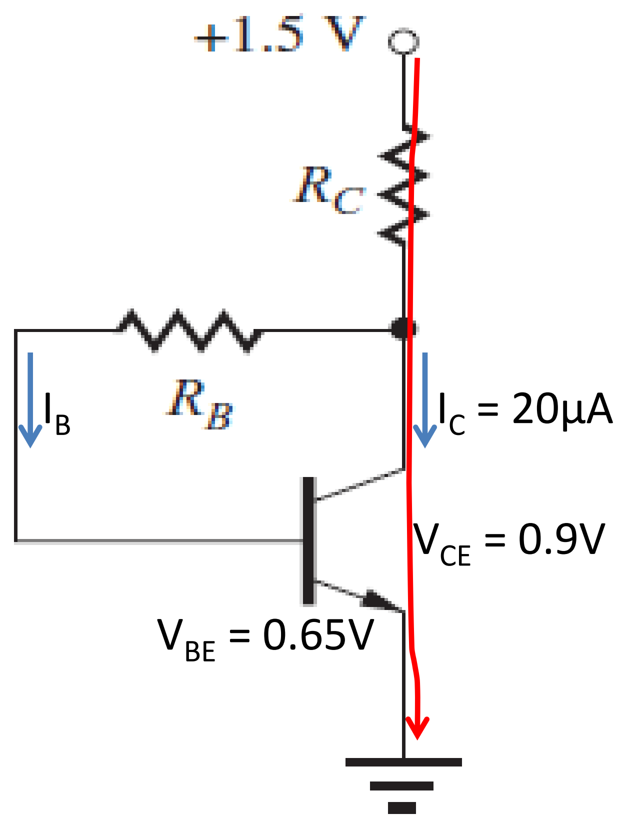
$$(I_C + I_B)R_C + V_{CE} = 1.5$$

$$\left(I_C + \frac{I_C}{\beta}\right)R_C + 0.9 = 1.5$$

$$I_C\left(1 + \frac{1}{\beta}\right)R_C = 0.6$$

$$20*10^{-6}\left(1 + \frac{1}{50}\right)R_C = 0.6$$

$$R_C = \frac{0.6}{20.4*10^{-6}} = 29.4117k\Omega$$



- **Soln contd.:** (find R_C and R_B) to give a Q-point of I_C = 20µA and V_{CE} = 0.9V.
- Apply KVL along the path (red line).

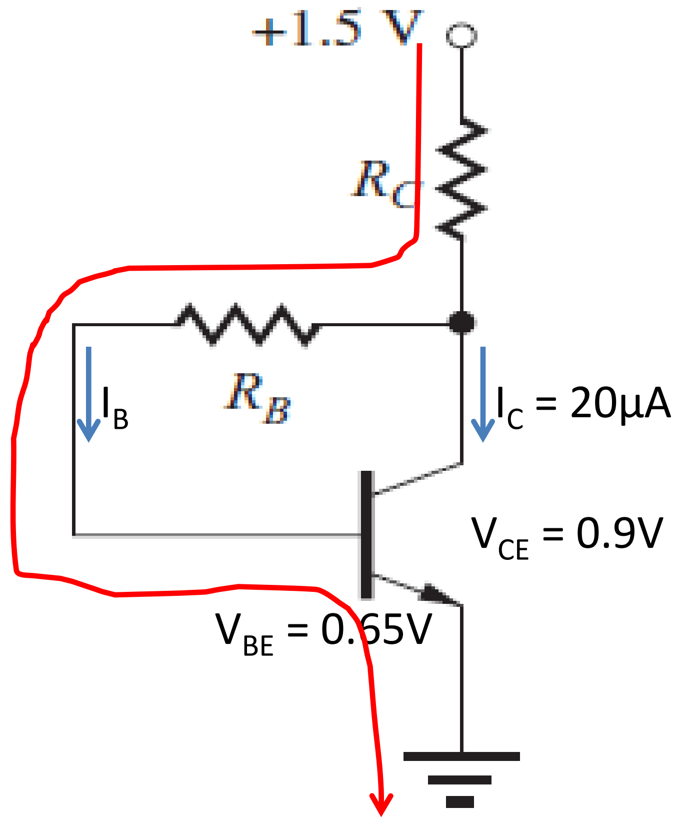
$$(I_C + I_B)R_C + I_B R_B + V_{BE} = 1.5$$

$$\left(I_C + \frac{I_C}{\beta}\right)R_C + \frac{I_C}{\beta}R_B + 0.65 = 1.5$$

$$0.6 + \left(\frac{20*10^{-6}}{50}\right)R_B + 0.65 = 1.5$$

$$0.4*10^{-6}*R_B = 0.25$$

$$R_B = \frac{0.25}{0.4*10^{-6}} = 625k\Omega$$



- **Soln contd.:** Find the Q-point if the current gain, β_F = 125. We have R_C=29.41kΩ, and R_B=625kΩ, from previous calculations.
- Apply KVL along the path (red line).

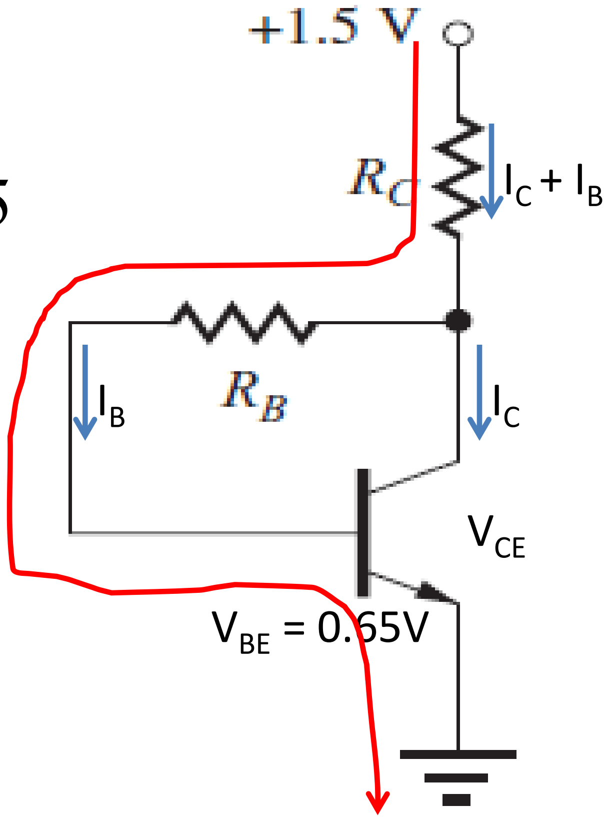
$$(I_C + I_B)R_C + I_B R_B + V_{BE} = 1.5$$

$$(\beta I_B + I_B)29.41k + I_B * 625k = 0.85$$

$$(126 * 29.41\,k + 625k)I_B = 0.85$$

$$I_B = \frac{0.85}{4.331 * 10^6} = 0.196\mu A$$

$$I_C = \beta I_B = 125 * 0.196 * 10^{-6} = 24.53\mu A$$

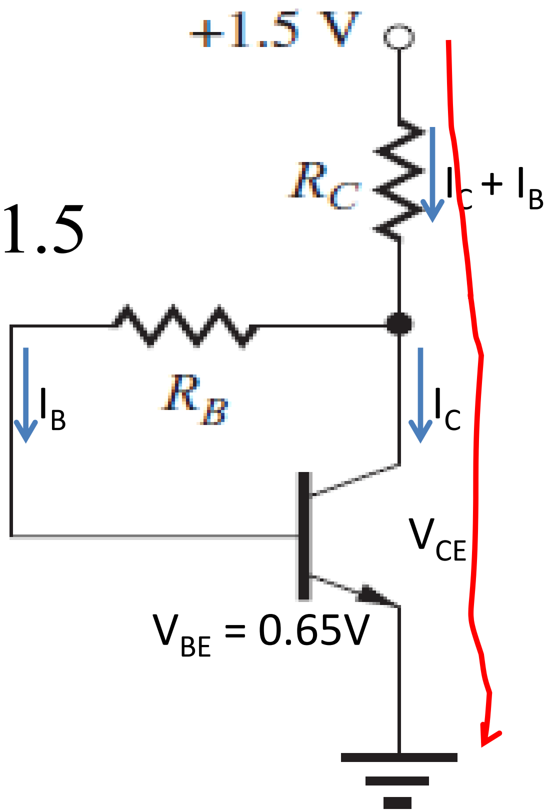


- **Soln contd.:** Apply KVL along the path (red line).

$$(I_C + I_B)R_C + V_{CE} = 1.5$$

$$(24.53 + 0.196) * 10^{-6} * 29.41\,k + V_{CE} = 1.5$$

$$V_{CE} = 1.5 - 0.727 = 0.773V$$

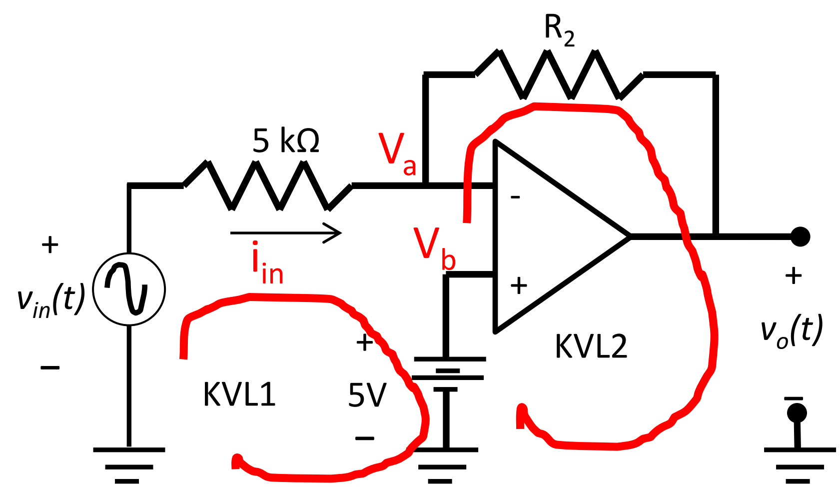


- The Q-Point is:

$$(I_C, V_{CE}) = (24.53\mu A, 0.773V)$$

Problem OP-AMP P1: - Consider the op-amp circuit shown below. If $v_{in}(t) = 6 + 9cos(500\pi t)$, calculate the value of R_2 required to generate a output, $v_o(t)$, with zero DC component. What is the resulting output voltage?

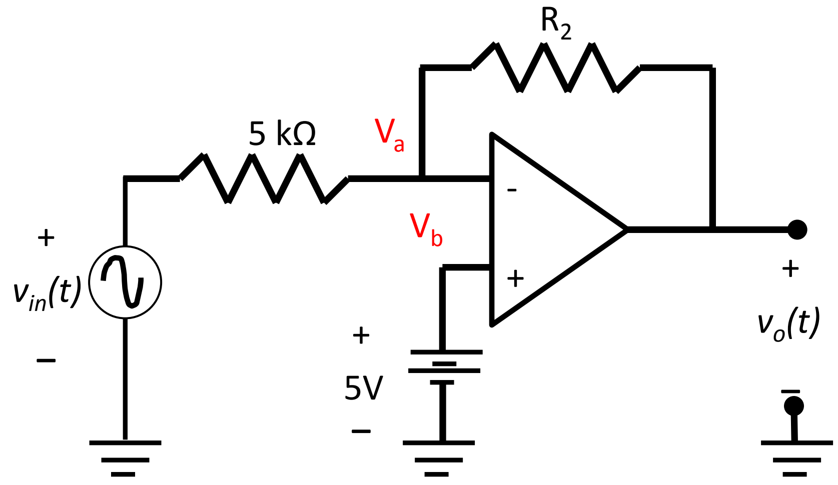
- **Soln:** The circuit shown is that of a differential amplifier. We can use superposition theorem to solve for the output voltage: connect inputs to ground (0 V), one at a time, and solve for output voltage.



- From summing point constraints: $V_a = V_b$
- From KVL2 $v_0 = 5 - i_{in}(t)R_2$
- From KVL1 and Ohms law $i_{in} = \dfrac{v_{in} - 5}{5k\Omega}$
- Therefore

$$v_o = 5 - \frac{(6 + 9\cos(500\pi t)) - 5}{5k\Omega} * R_2$$

$$v_o = 5 - \frac{\left(6 + 9\cos\left(500\pi t\right)\right) - 5}{5k\Omega} * R_2$$



- If DC component of v_o is zero,

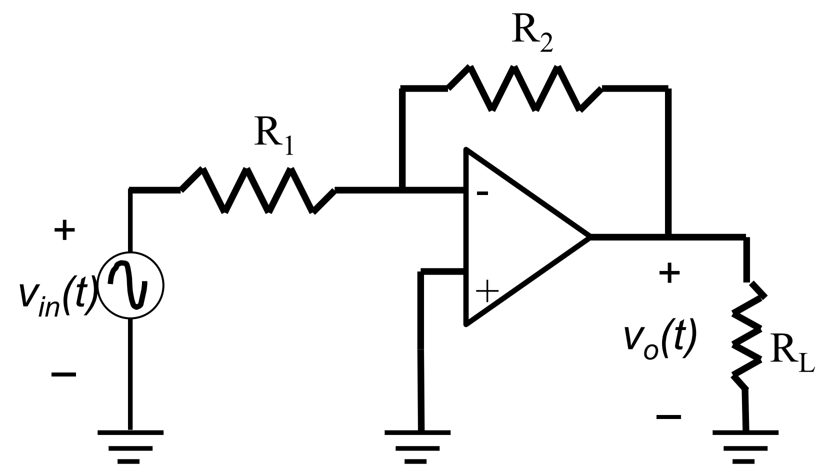
$$0 = 5 - \frac{6-5}{5k\Omega} * R_2$$

- Multiplying by $5k\Omega$ on both sides and solving for R_2,

  $R_2 = 25\ k\Omega$
- Then the output is $v_o = -45\cos(500\pi t)$,

Problem OP-AMP P2: - Consider the op-amp circuit shown below. Assume the maximum output voltage of the op-amp ranges from – 12 V to + 12 V; the maximum output current magnitude is 25 mA; and the slew-rate limit is 1.5 V/μs. If $v_{in}(t)$=$v_m sin(\omega t)$, R_1 = 5 kΩ, and R_2 = 25 kΩ.

a) Find the full-power bandwidth of the op-amp.



- **Soln:** The full-power bandwidth of the op-amp is given by

$$f_{FP} = \frac{SR}{2\pi V_{om}}$$

- Slew-rate, SR = 1.5 V/μs;

maximum output amplitude,V_{om} = 12 V.

$$f_{FP} = \frac{1.5*10^6}{2\pi(12)} \approx 19.9kHz$$

b) Find the peak output voltage possible without distortion for the following cases:

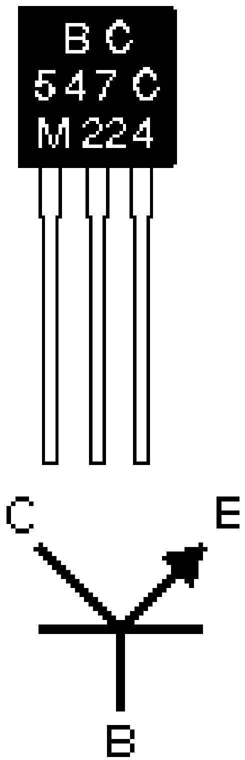
- **Case a:** Frequency of 5 kHz and R_L = 20 Ω
  - **Soln.:** The current limit of the op-amp limits the peak output voltage. Since R_L is very small compared to R_2 the current through R_2 can be neglected. Thus the peak output voltage is given by

$$V_{om} = 25mA * R_L = 0.5V$$

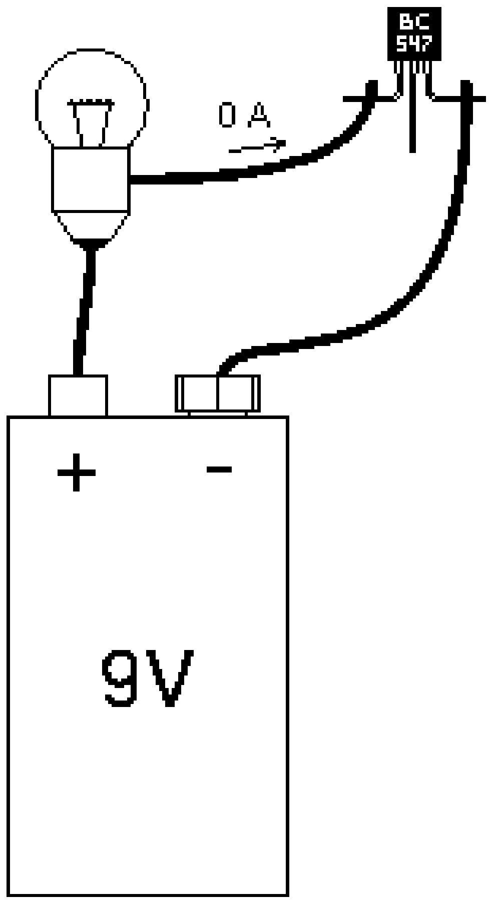
- **Case b:** Frequency of 5 kHz and R_L = 2.5 kΩ
  - **Soln.:** V_{om} = 12 V (The maximum voltage that the op-amp can achieve.)
- **Case c:** Frequency of 50 kHz and R_L = 2.5 kΩ
  - **Soln.:** The slew-rate limit of the op-amp limits the peak output voltage.

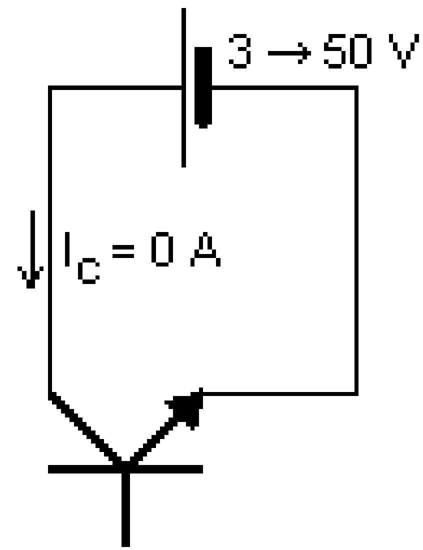
$$V_{om} = \frac{SR}{2\pi f} = \frac{1.5 * 10^6}{2\pi(50 * 10^3)} \approx 4.7V$$

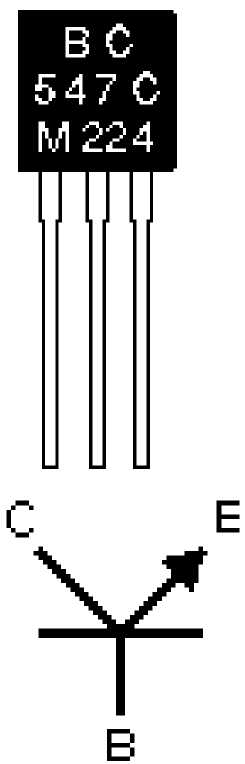
BJTs - Practical Aspects

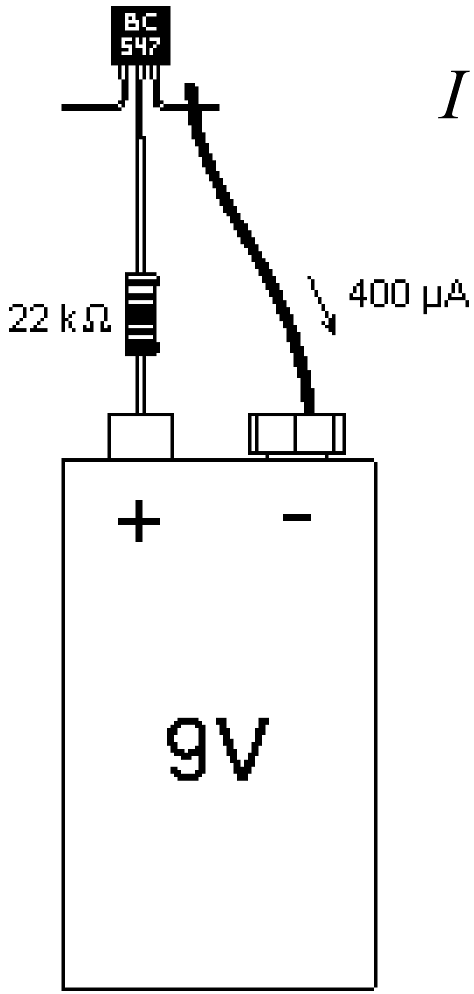


npn

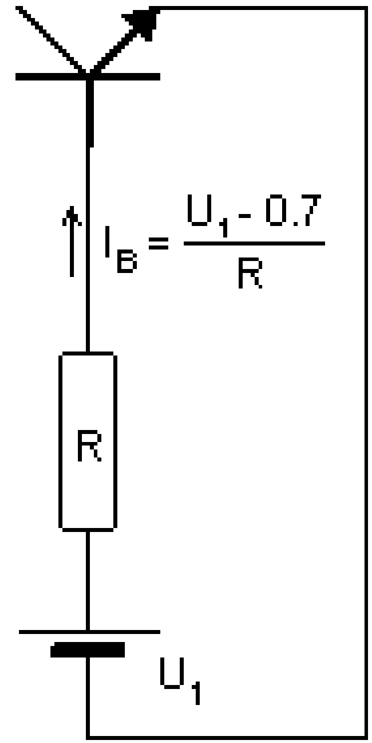


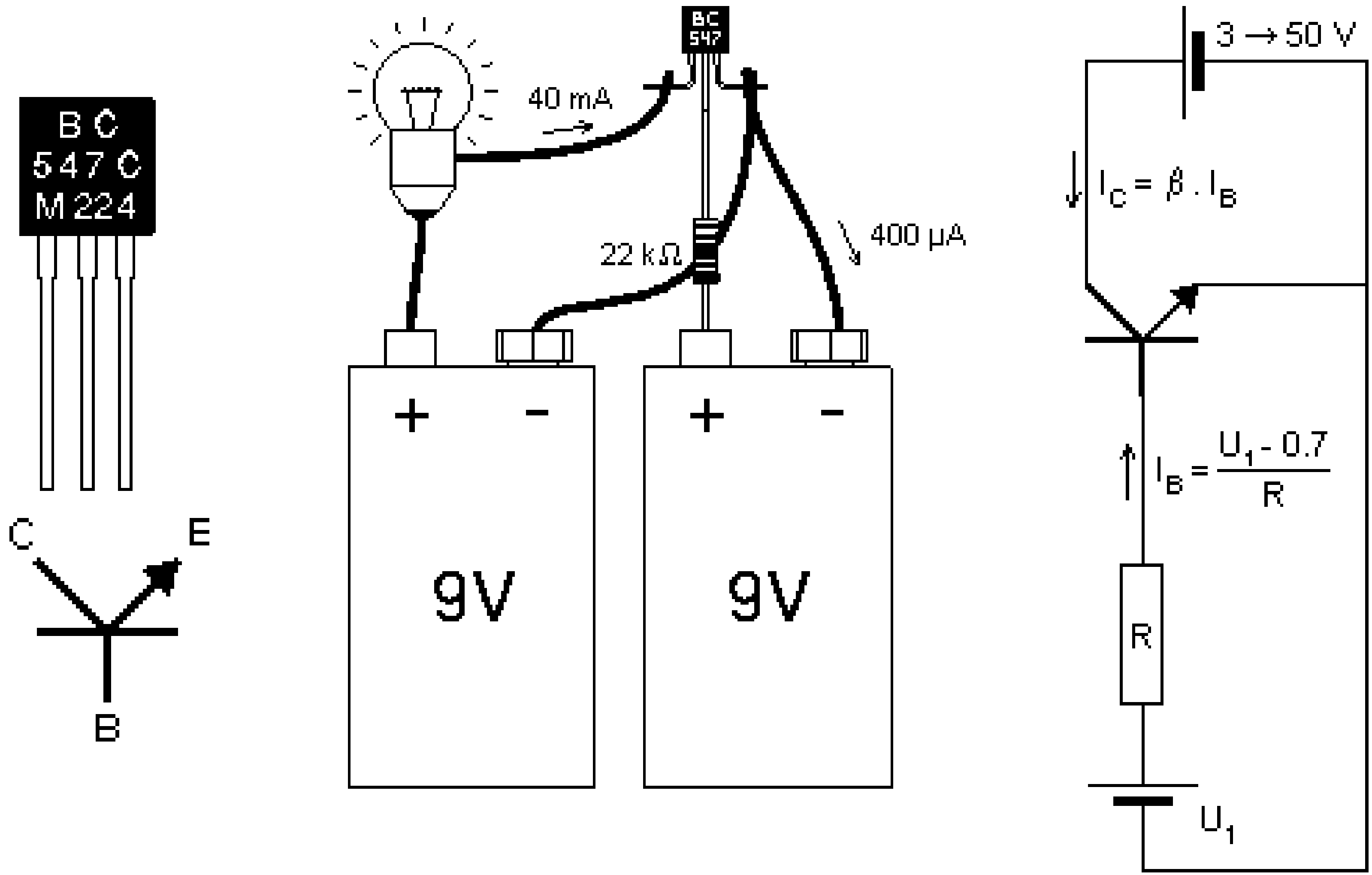




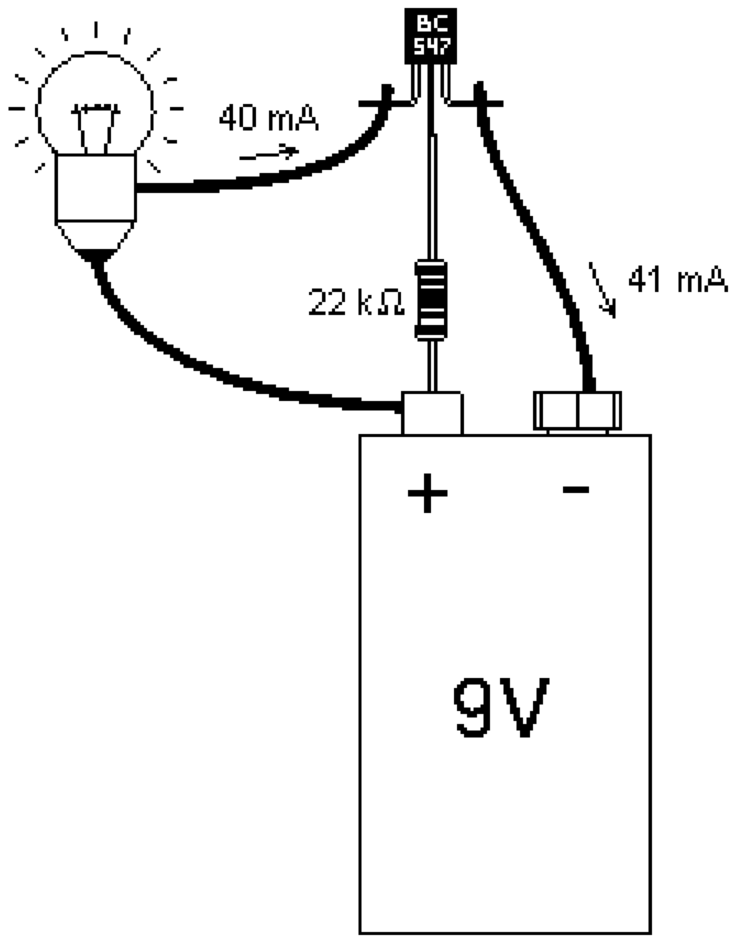


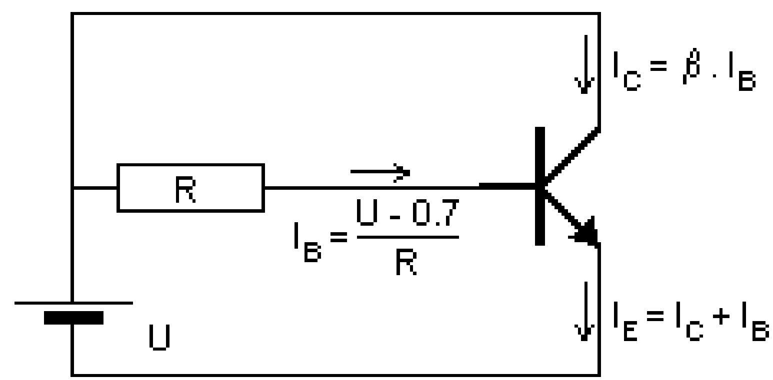
$$I = \frac{V}{R}$$





BC
547C
M224
C
E
B
BC
547
40 mA
22 kΩ
400 µA
+
-
9V
+
-
9V
3 → 50 V
$I_C = \beta \cdot I_B$
$I_B = \frac{U_1 - 0.7}{R}$
R
U_1

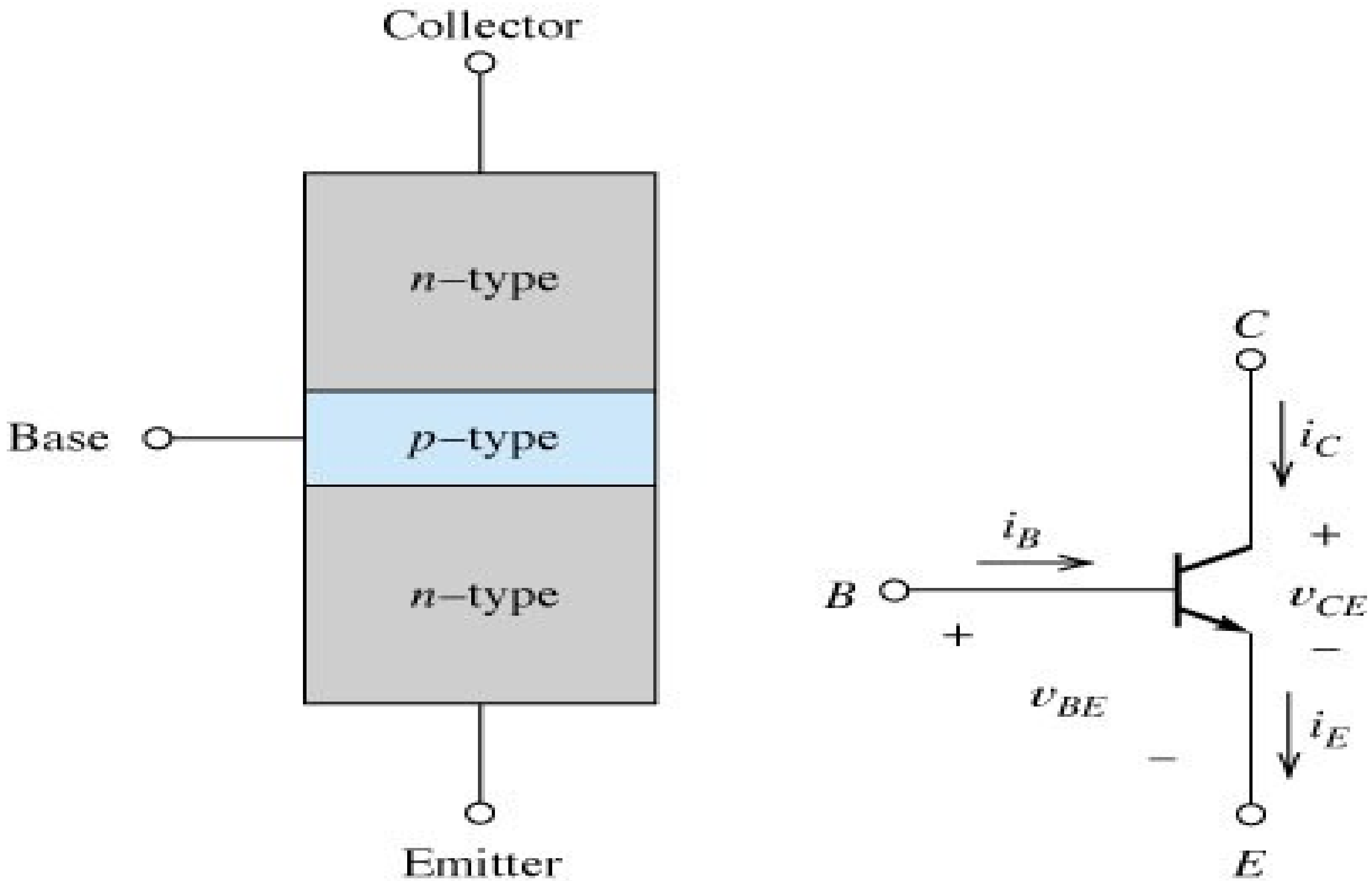

BC
547
40 mA
22 kΩ
41 mA
+
-
9V


R
$I_C = \beta \cdot I_B$
$I_B = \frac{U - 0.7}{R}$
$I_E = I_C + I_B$
U

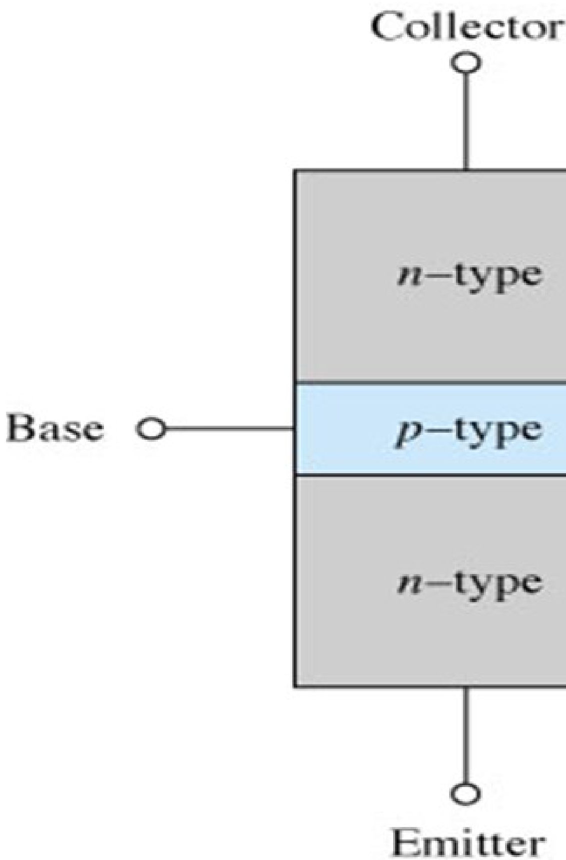

Please Compare a
bout That

Transistor

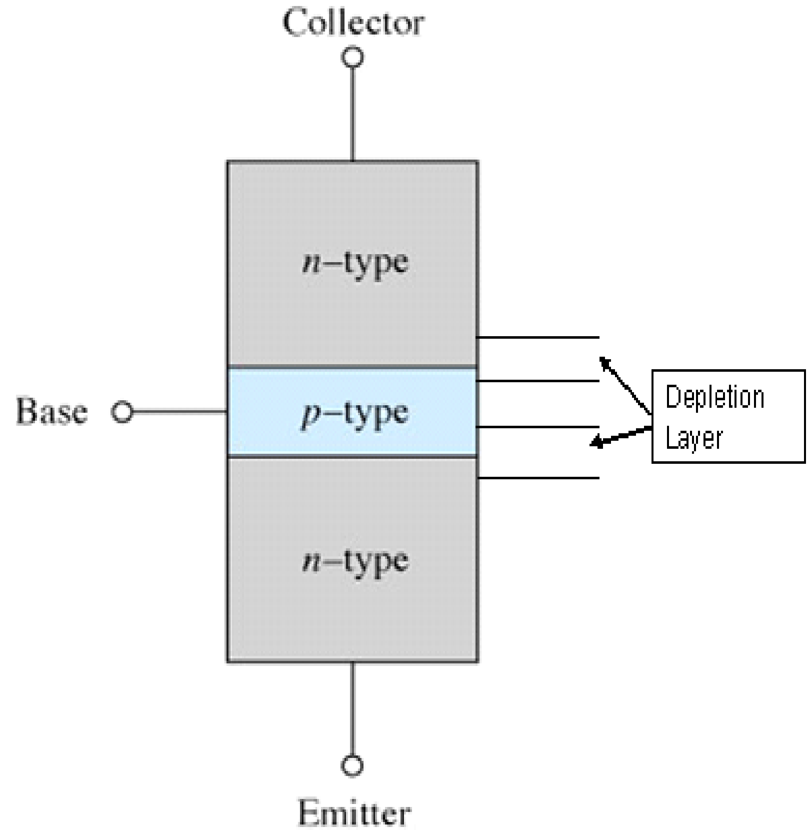
- Three doped regions
- Emitter, Base and Collector
- Base region is much thinner as compared to the collector and emitter
- ***npn*** and ***pnp***
- Emitter is heavily doped, Base is lightly and collector is intermediate
- Collector regions is physically largest



(a) Simplified physical structure (b) Circuit symbol



Before Diffusion



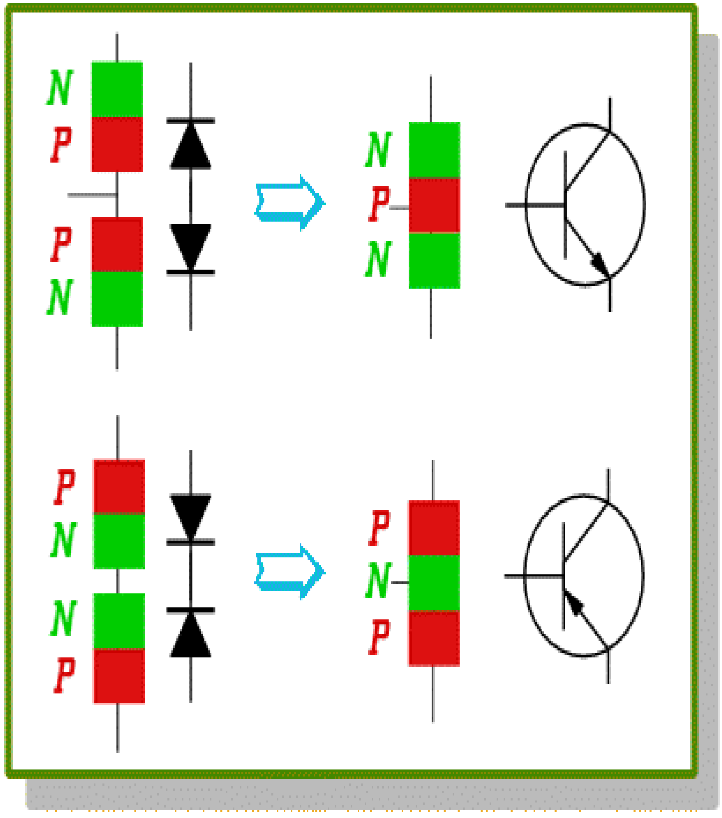
After Diffusion

Each of Dep. Layer barrier potential app. 0.7 V at 25^{o} C

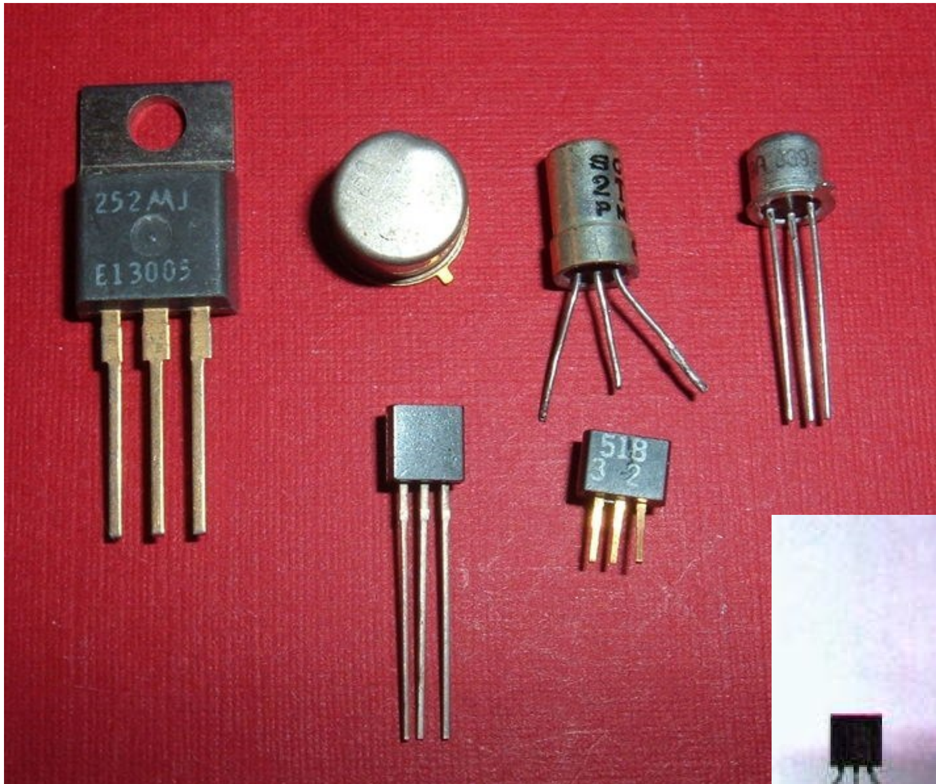
Unbiased transistor is like two back-to-back diodes

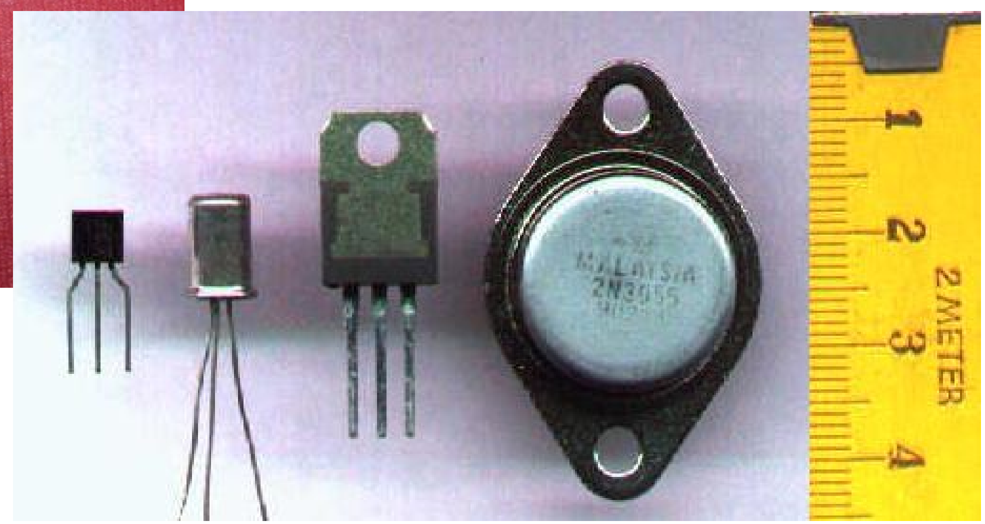
Bipolar Junction Transistors

- A bipolar transistor essentially consists of a pair of PN Junction diodes that are joined back-to-back.
- There are therefore two kinds of BJT, the **NPN** and **PNP** varieties.
- The three layers of the sandwich are conventionally called the **Collector**, **Base**, and **Emitter**.



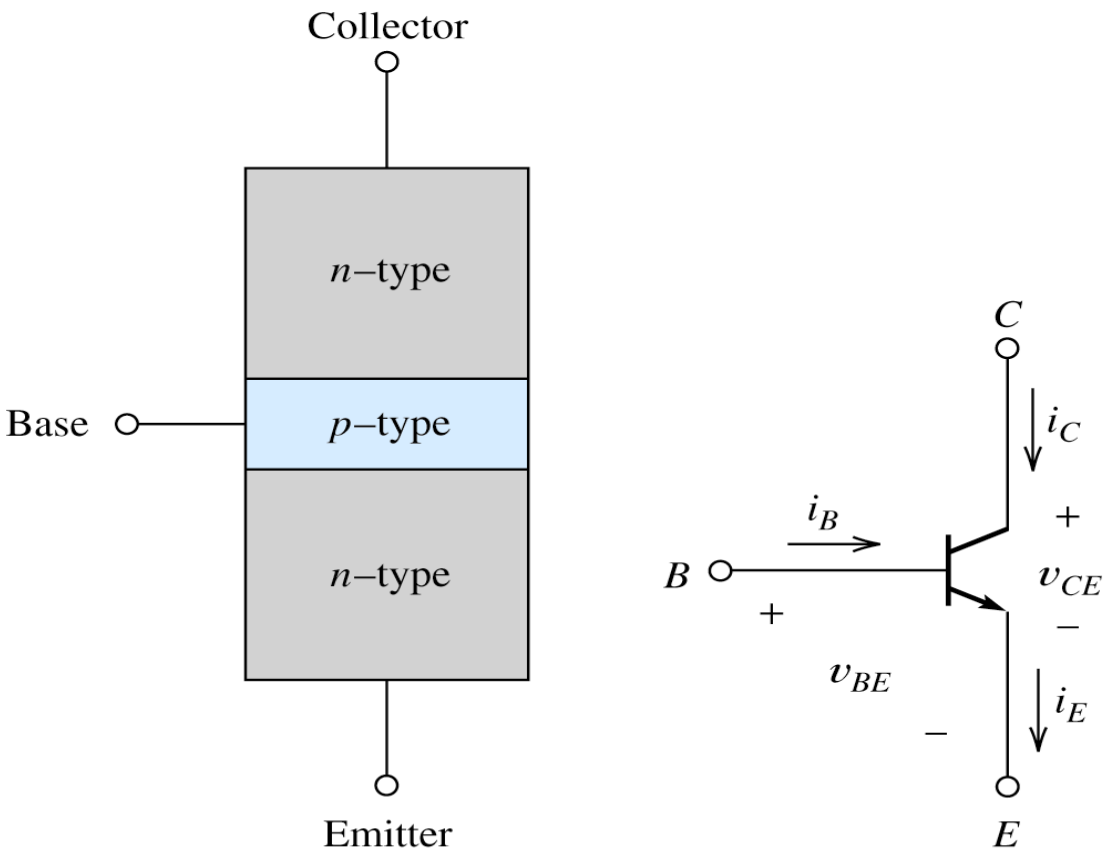
Modern Transistors





NPN Bipolar Junction Transistor

- One N-P (Base Collector) diode one P-N (Base Emitter) diode

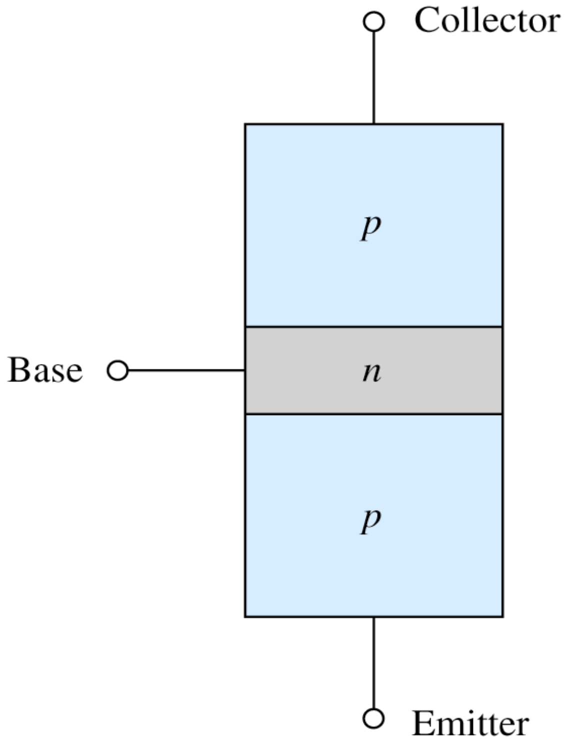


(a) Physical structure (b) Circuit symbol

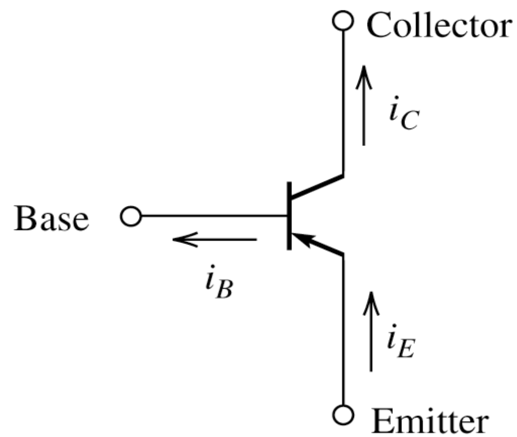
Figure 13.1 The *npn* BJT.

PNP Bipolar Junction Transistor

- One P-N (Base Collector) diode one N-P (Base Emitter) diode



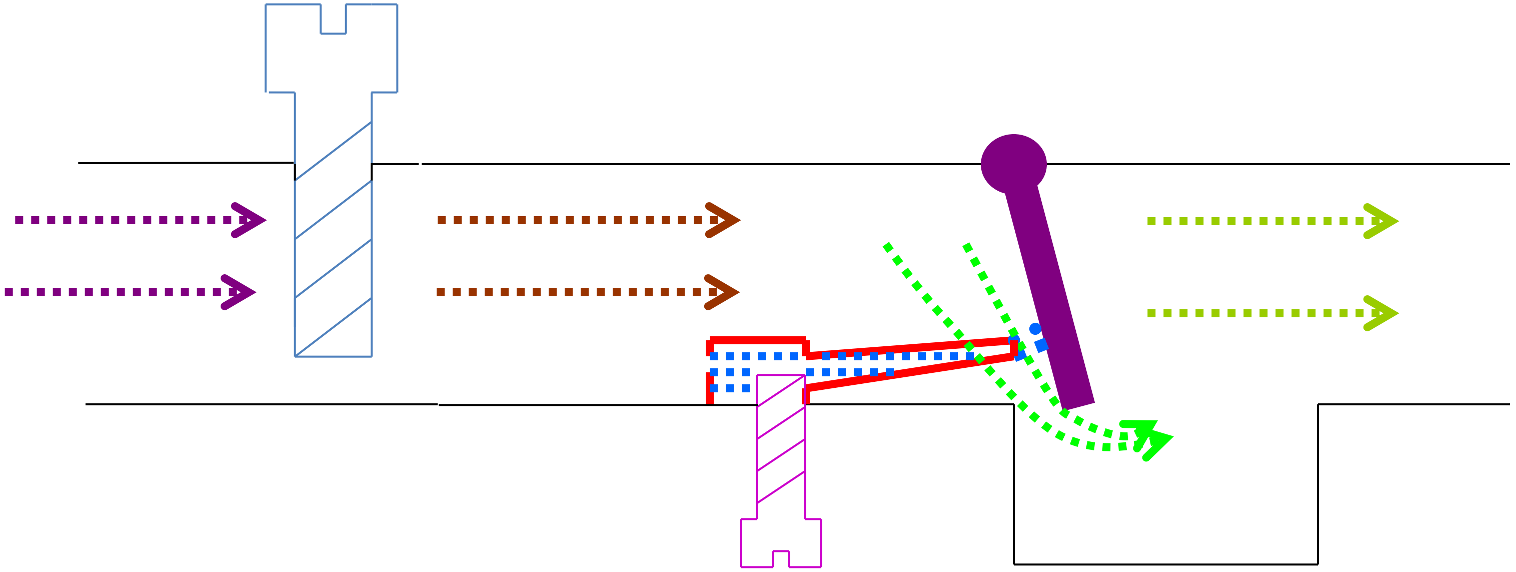
(a) Physical structure



(b) Circuit symbol with reference directions for currents

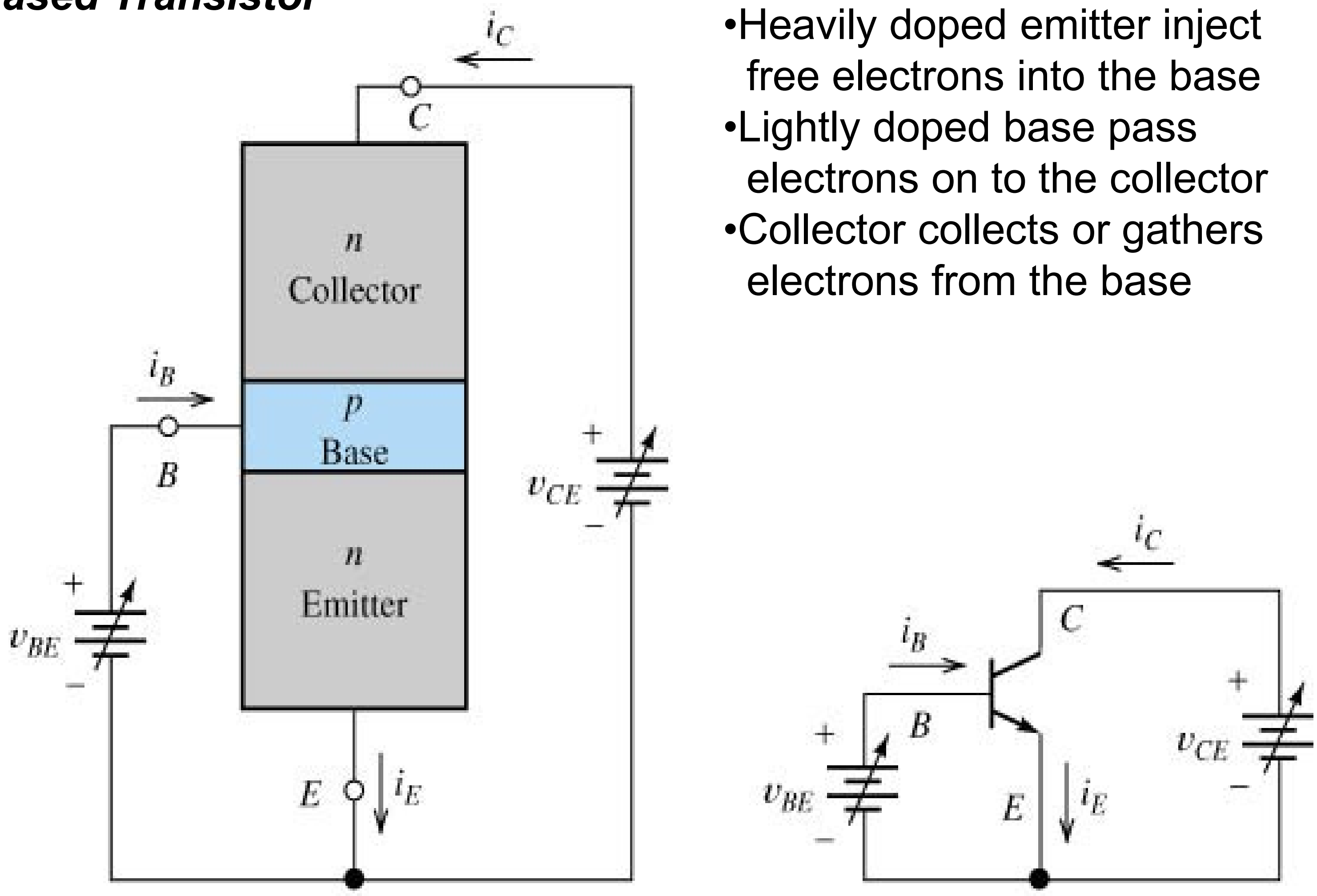
Figure 13.13 The *pnp* BJT.

Analogy with Transistor :Fluid-jet operated Valve



***The Biased Transistor**

- Heavily doped emitter inject free electrons into the base
- Lightly doped base pass electrons on to the collector
- Collector collects or gathers electrons from the base

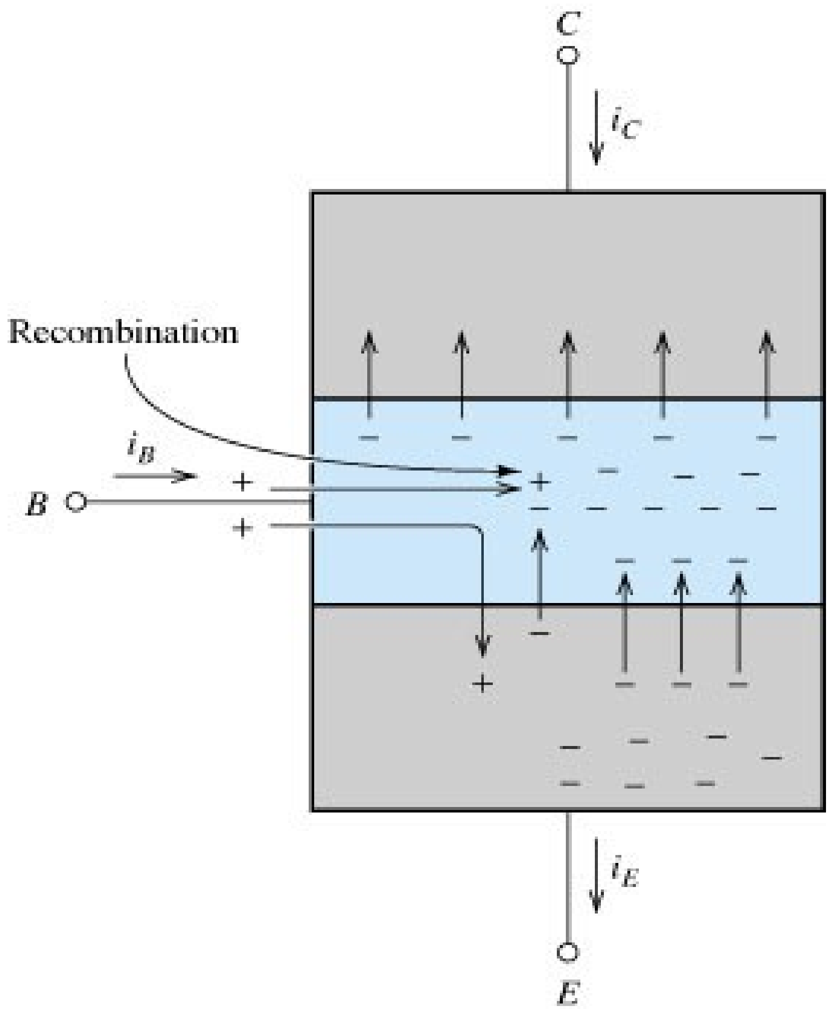


(a) (b)

Biasing method – Emitter junction FB

Collector junction RB

Summary



- Forward biased emitter diode, forcing the free electrons in the emitter to enter the base
- Thin and lightly doped base diffuse electrons into collector
- Collector, through R_C and into the positive terminal of V_{CC}

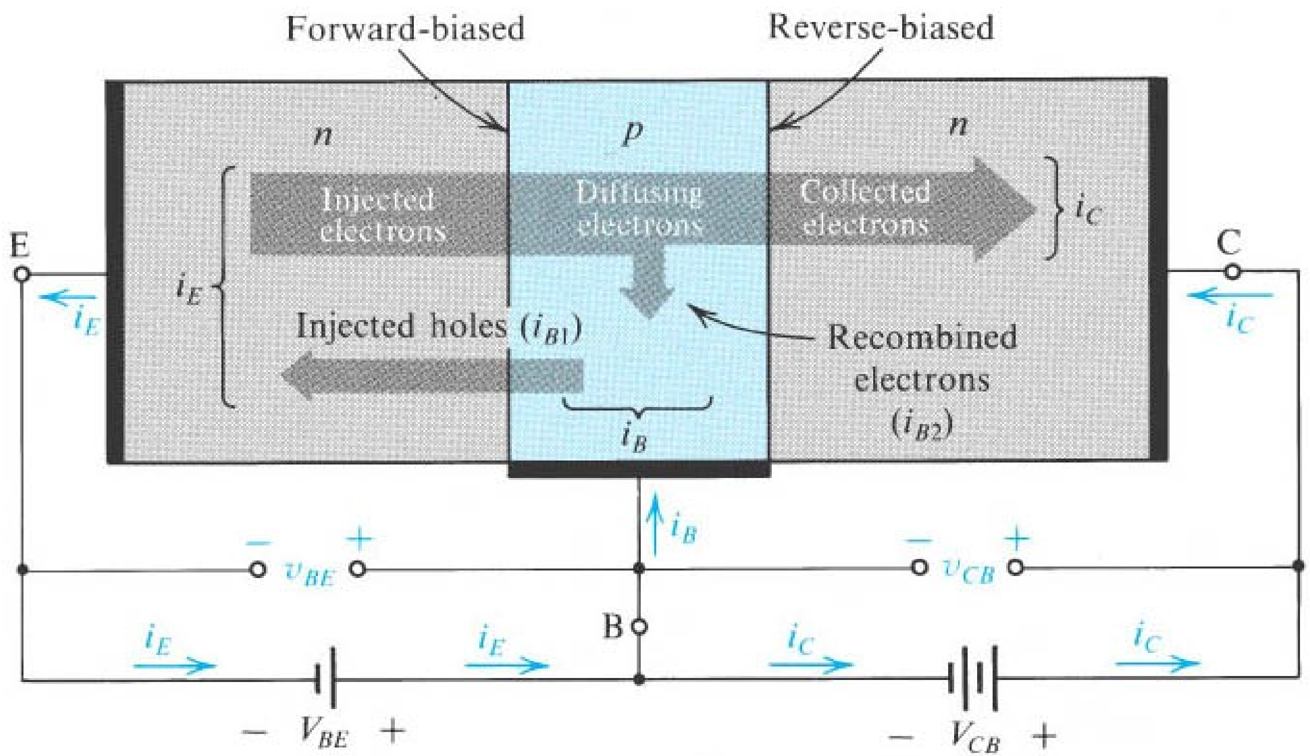
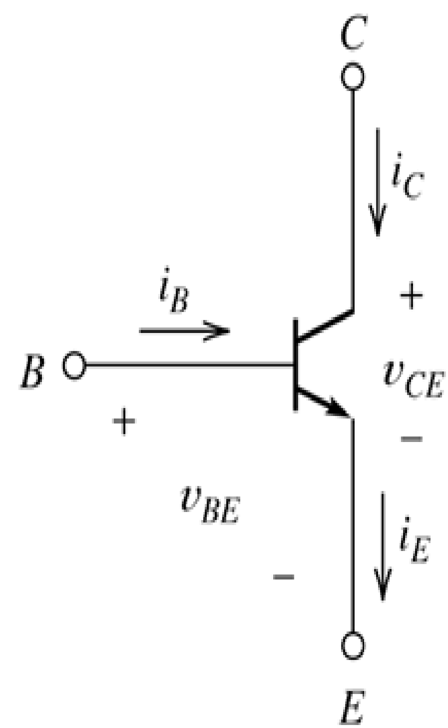


Figure 5.3 Current flow in an *npn* transistor biased to operate in the active mode. (Reverse current components due to drift of thermally generated minority carriers are not shown.)

Transistor Currents

- I_E – Largest emitter current
- Emitter electrons flow to the collector, $I_C \approx I_E$
- $I_B \leq 0.01\ I_C$
- KCL, $I_E = I_C + I_B$



Circuit symbol

BJT α and β

- From the previous figure $I_E = I_B + I_C$
- Define $\alpha_{dc} = I_C / I_E$
- DC alpha is slightly less than 1
- Low power transistor $\alpha_{dc} > 0.99$ and High power
  transistor $\alpha_{dc} > 0.95$
- Define $\beta_{dc} = I_C / I_B$ - known as a current gain

BJT α and β

- Then $\beta_{dc} = I_C / (I_E - I_C) = \alpha_{dc} /(1 - \alpha_{dc})$
- **Assignment – Derive $\alpha_{dc} = \beta_{dc} /(1 + \beta_{dc})$**
- Then $I_C = \alpha_{dc} I_E$ & $I_B = (1 - \alpha_{dc}) I_E$

Solved Example 6.1, 6.2, 6.3

NPN BJT Current flow

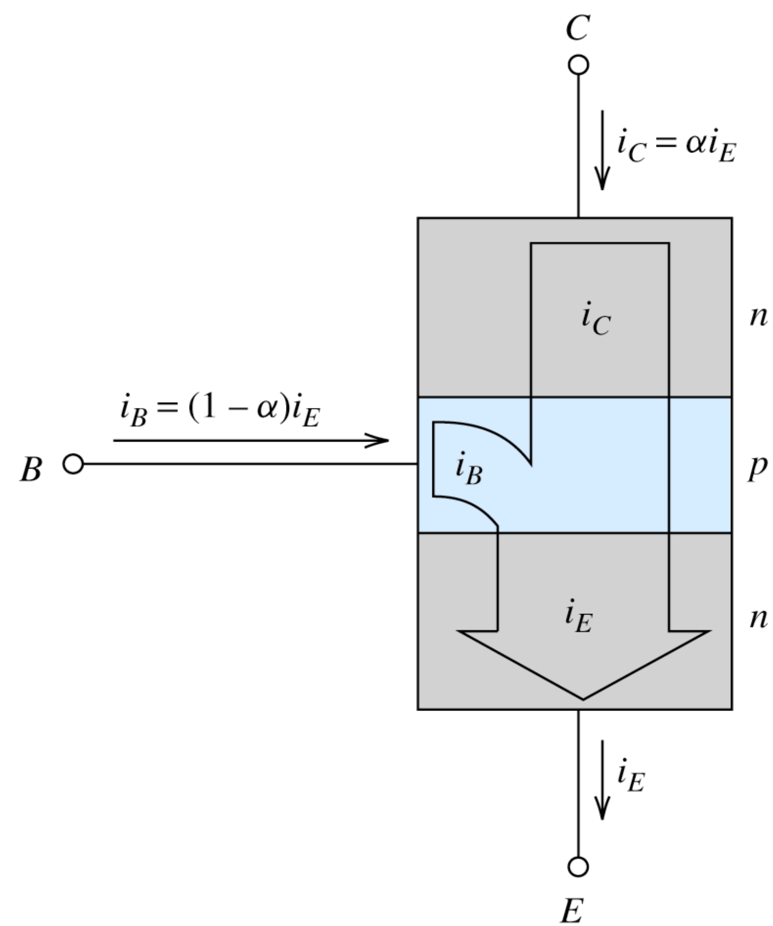
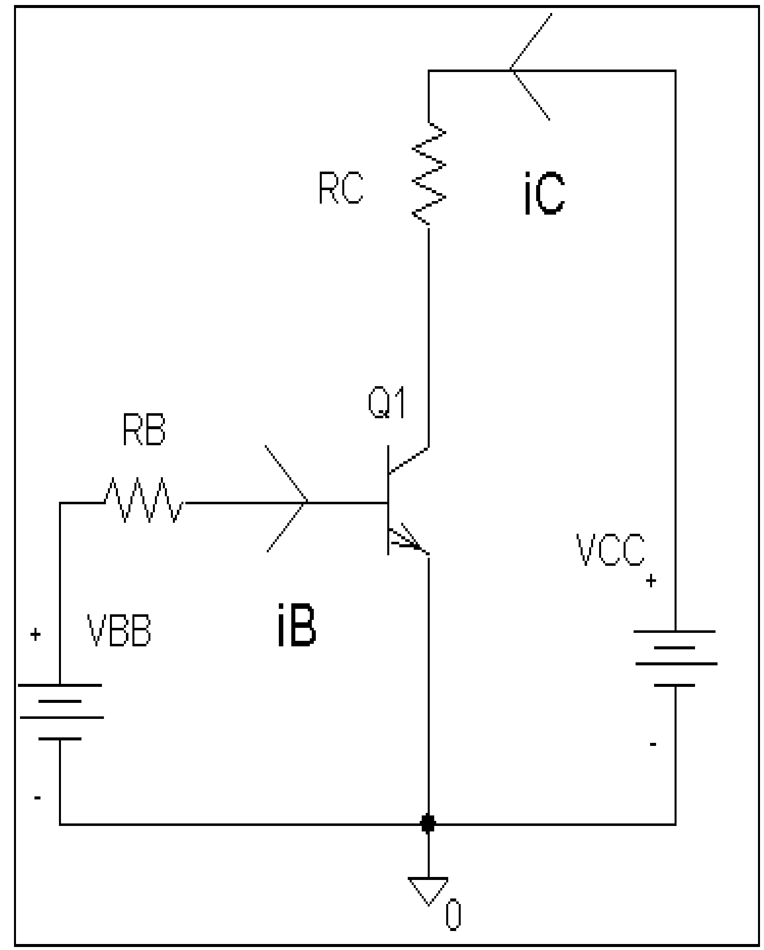


Figure 13.3 Only a small fraction of the emitter current flows into the base (provided that the collector–base junction is reverse biased and the base–emitter junction is forward biased).

The CE connection

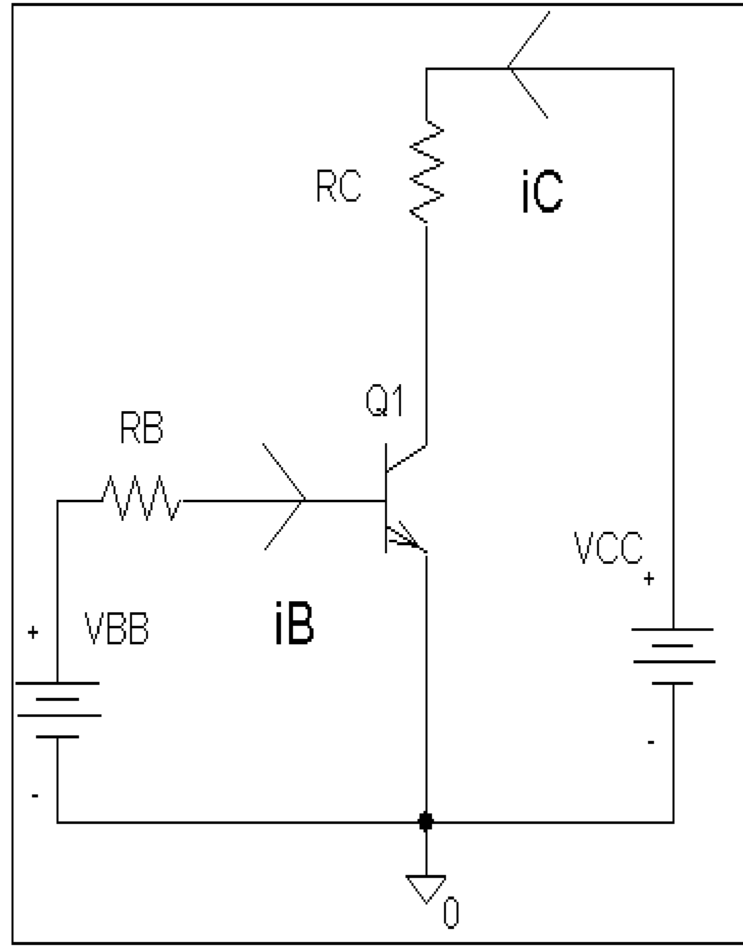
- **<u>CE</u>**, CC and CB
- CE because emitter is common to both V_{BB} and V_{CC}

- Left loop – Base loop
- Right loop – collector loop



The CE connection

- Base Loop, V_{BB} source and R_B – current limiting resistor
- Changing V_{BB} or R_B, change base current and I_B Change than I_C change
- **I_B controls I_C**



Notation

Double Subscripts

- Voltage source – VBB and VCC
- VBE – voltage between points B and E
- VCE – voltage between points C and E

Single Subscripts

- Used for Node voltages
- V_B – voltage between base and ground
- V_C and V_E
- $V_{CE} = V_C – V_E$
- V_{CB} and V_{BE}

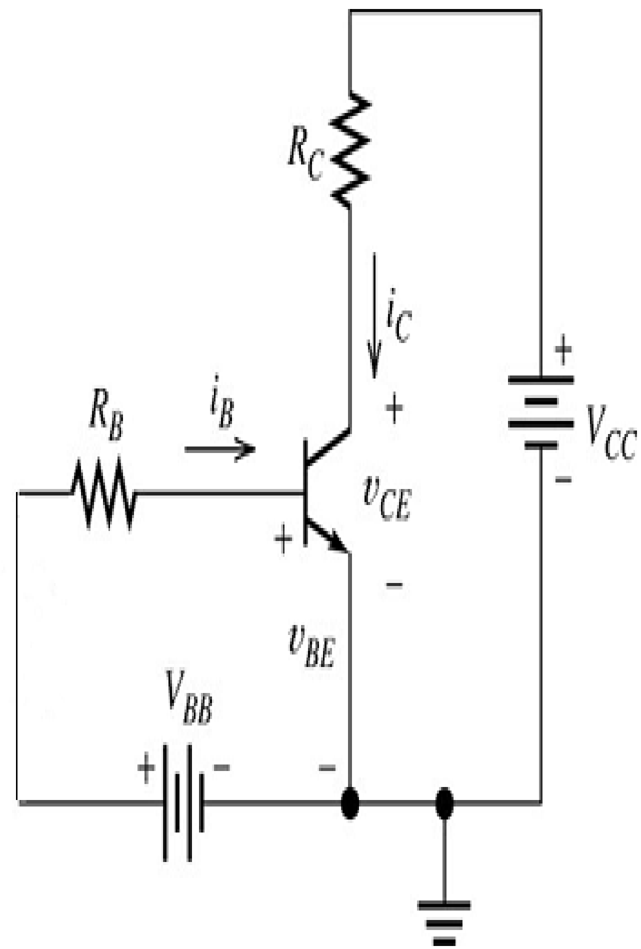
The Base Curve / Input Characteristics

- Graph I_B versus V_{BE}
- Like ordinary diode
- Ohm's low to Base loop

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

I

- Ideal diode V_{BE} = 0 and second app. V_{BE} = 0.7 V



Collector Curve / output Characteristics

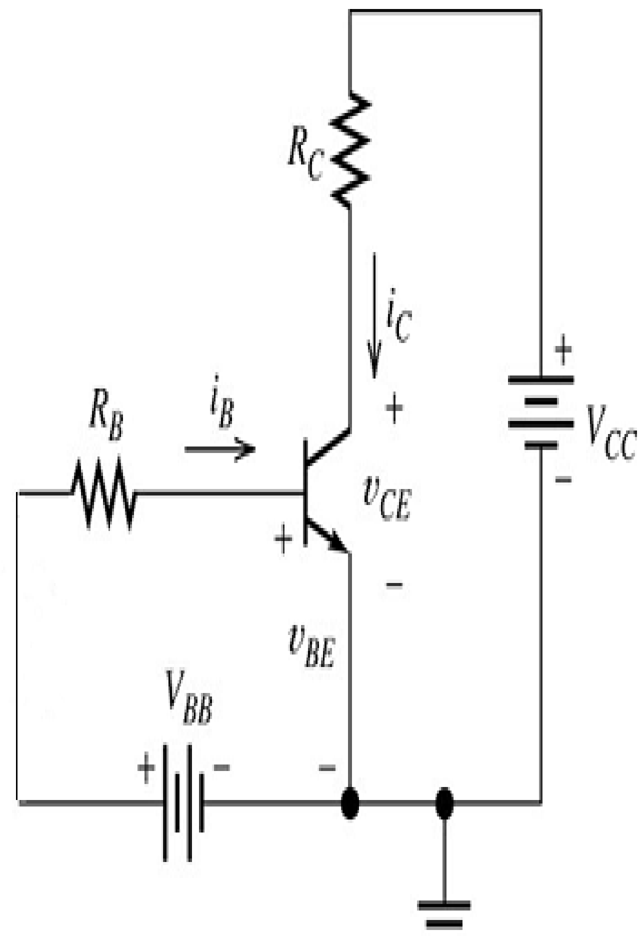
- Graph I_C versus V_{CE}

- Ohm's low to Collector loop

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

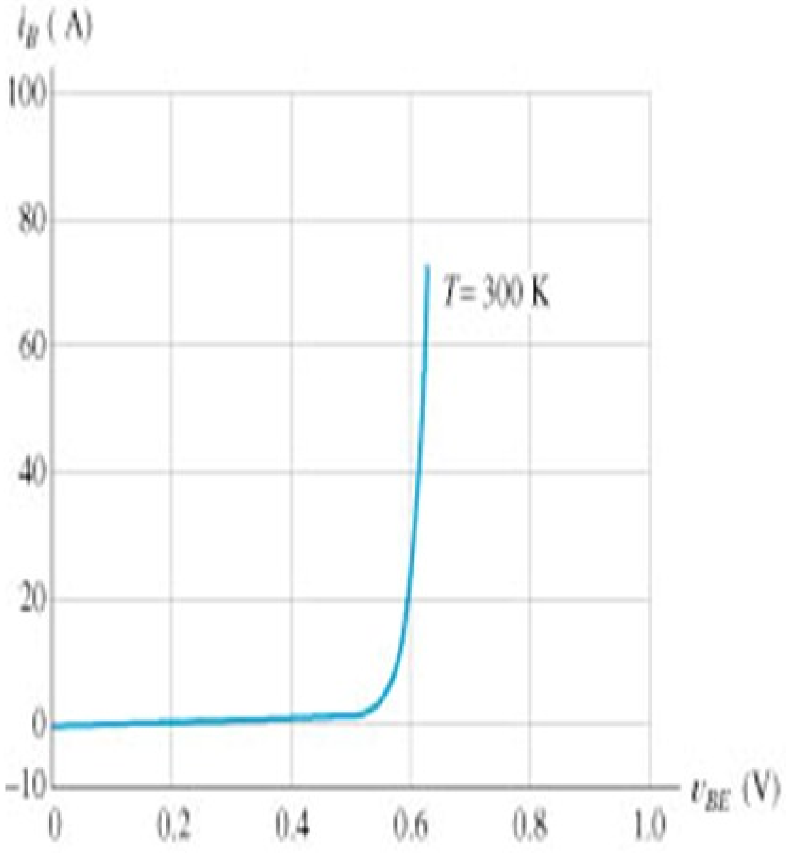
I

- Fixed value of based current, vary V_{CC} and measure I_C and V_{CE}

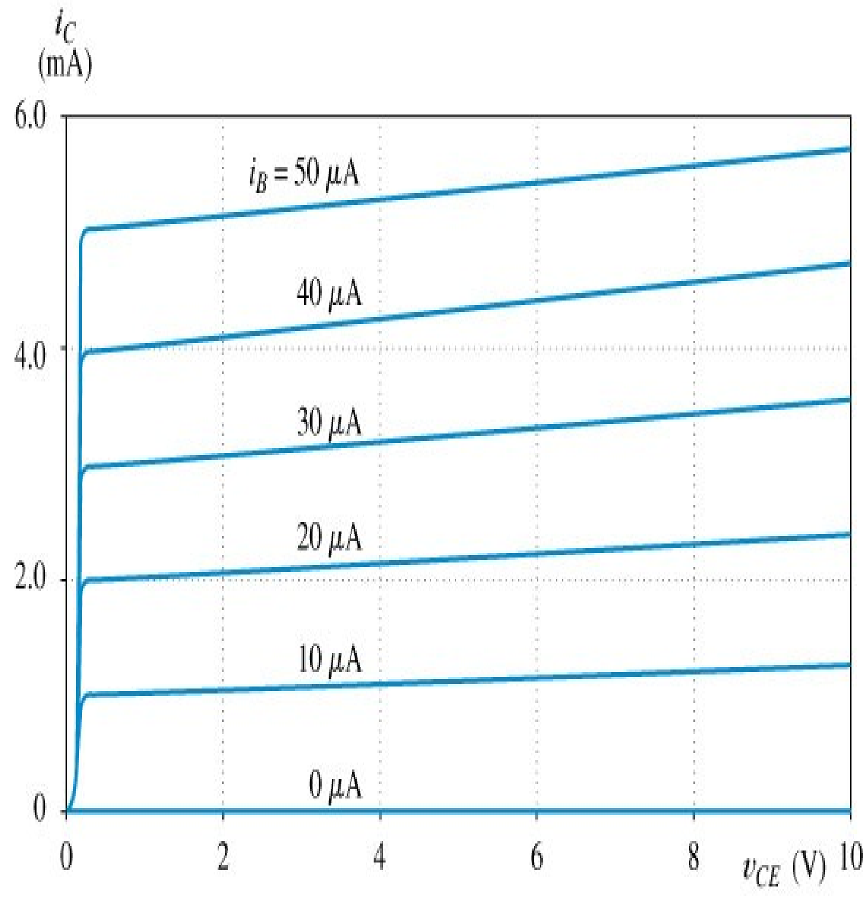


Transistor Characteristics

Input Characteristics



Output Characteristics



Active Region, Constant collector current

- After collector diode reverse biased, it collect all the electrons that reach its deplation layer
- Further increased V_{CE} cannot increased I_C
- Collector can collect only those free electrons that emitter injects

- $V_{CE} > V_{CE(max)}$, collector diode break down
- Power Dissipation $P_D = V_{CE}I_C$
- $P_D < P_{D(max)}$

Operating Region of Transistor

- **Active region**, middle region – normal operation of transistor

  Emitter diode – FB and Collector diode – RB
- **Breakdown region –** transistor will be destroyed
- **Saturation region** – rising part of curve, V_{CE} between zero and few tenth of volt

  Collector diode has insufficient positive voltage to collect all the free electrons injected into the base

Operating Region of Transistor

- **Cut off region** – $I_B = 0$ but still small collector current

  Because collector diode RB – Reverse minority carrier + Surface leakage current

BJT Operating Regions

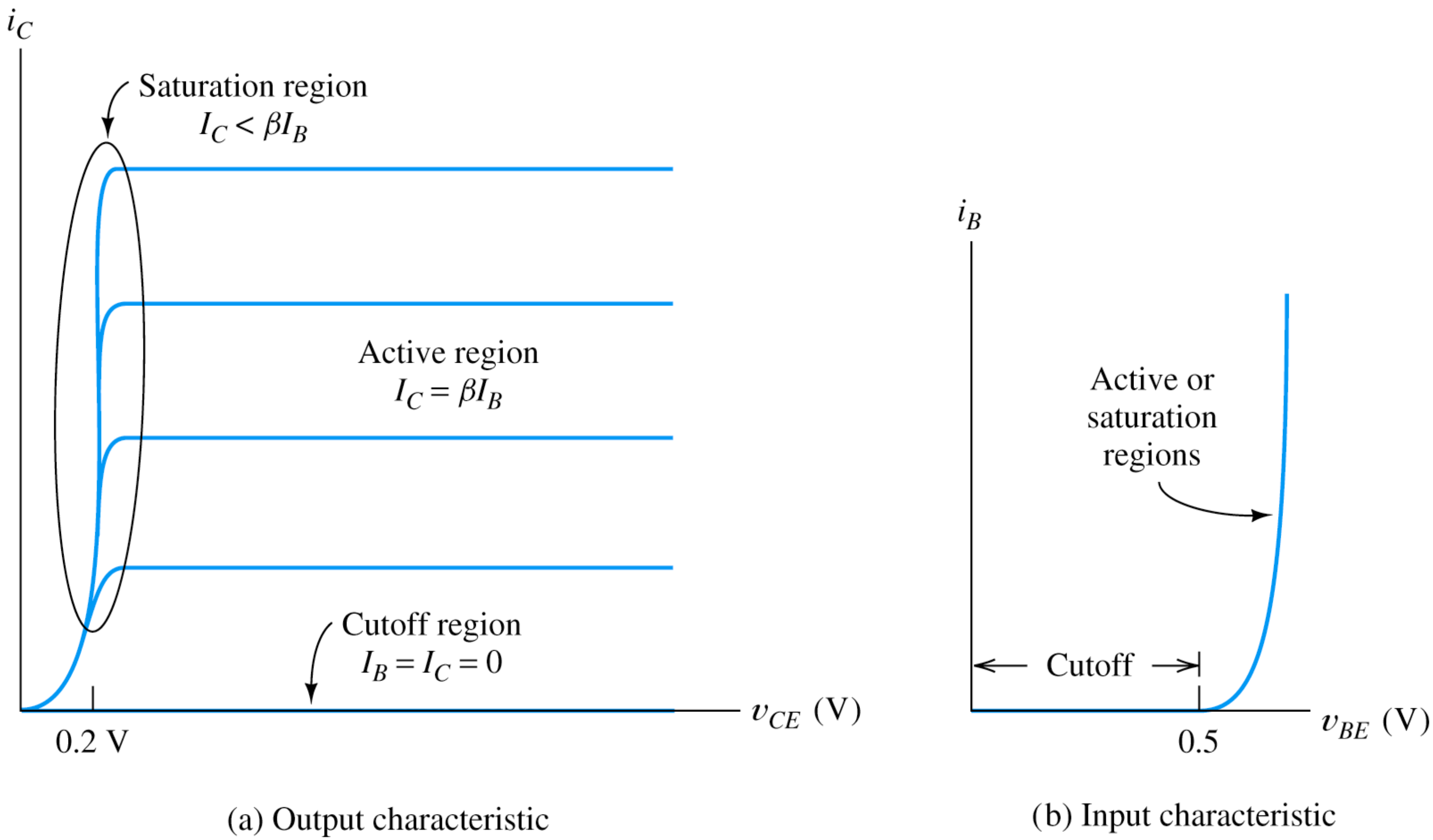
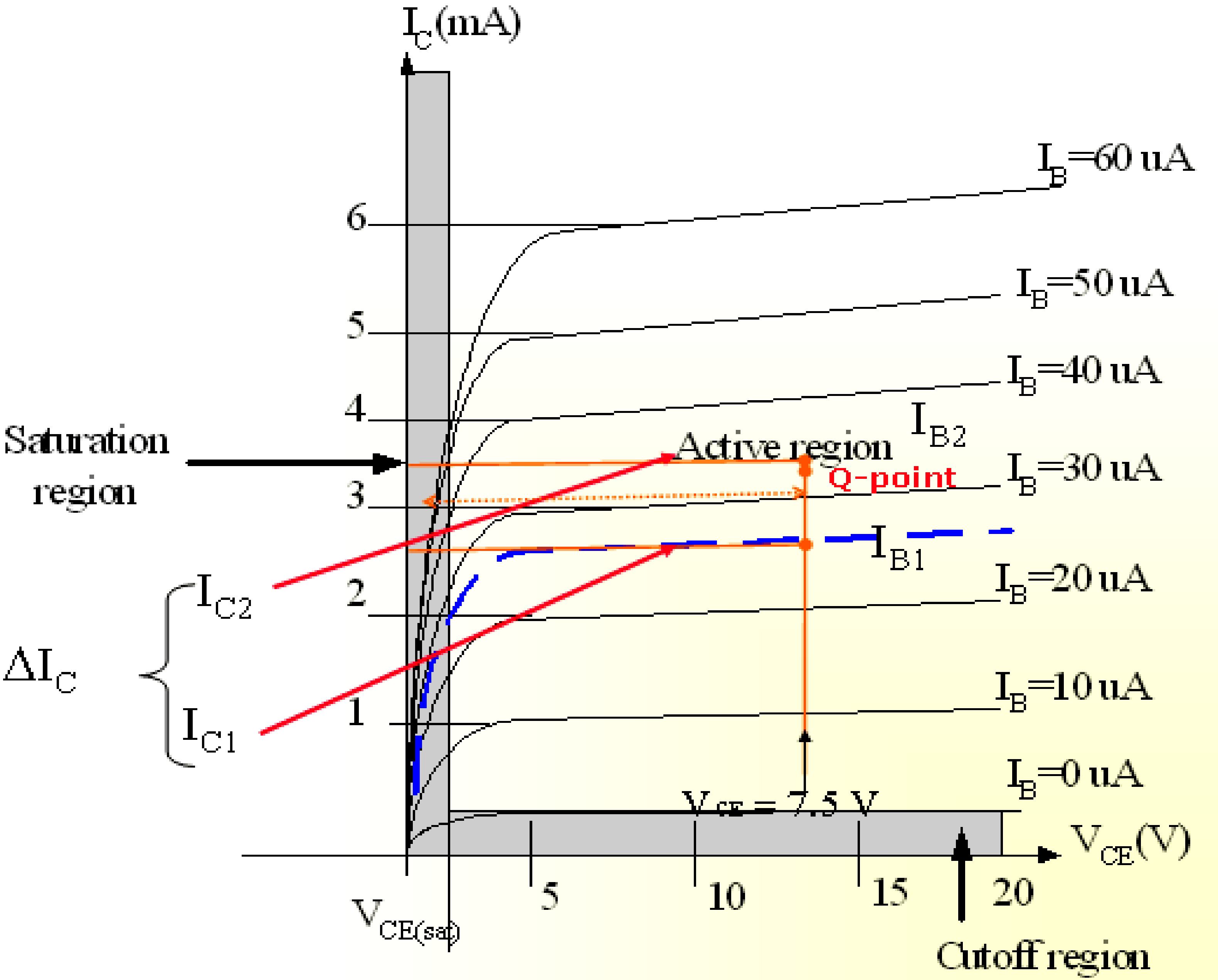
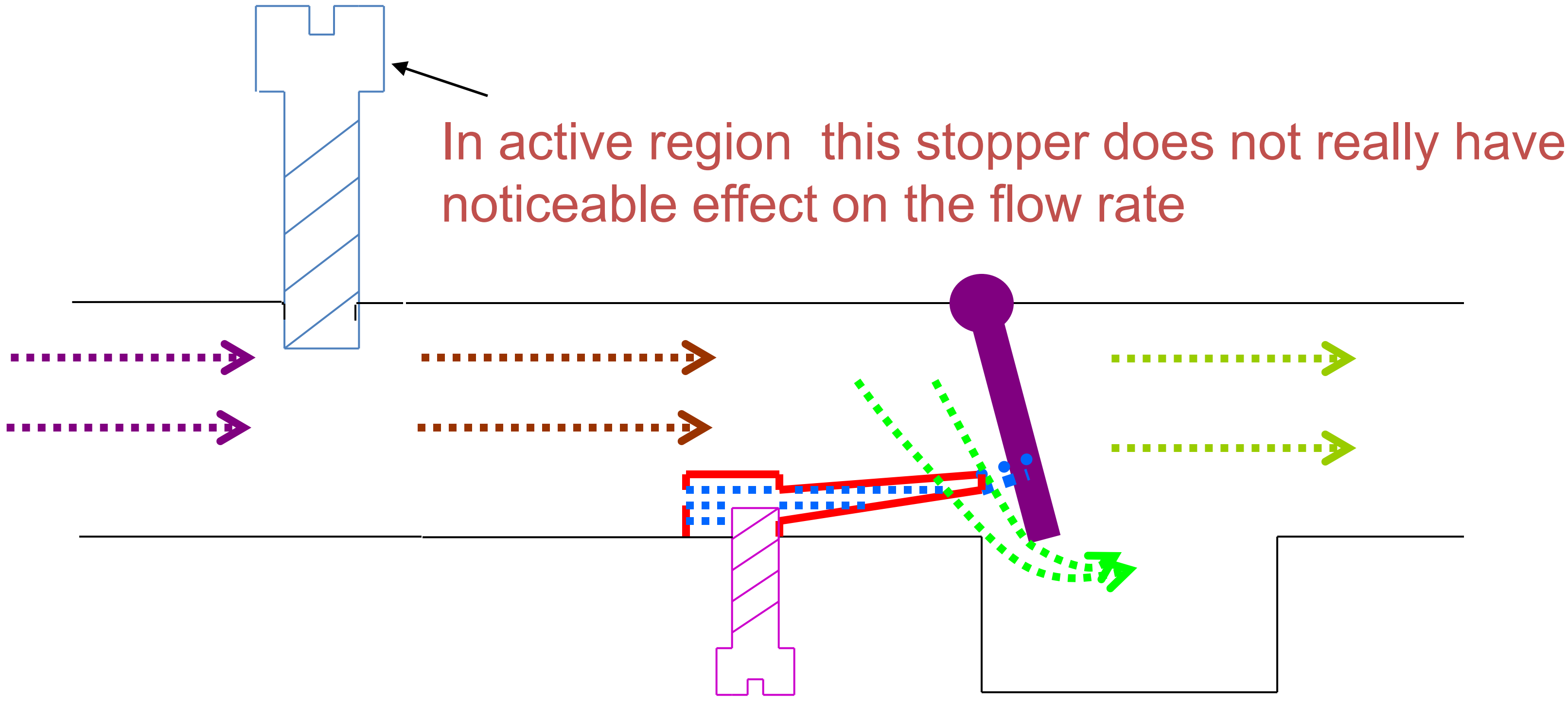


Figure 13.17 Regions of operation on the characteristics of an *npn* BJT.



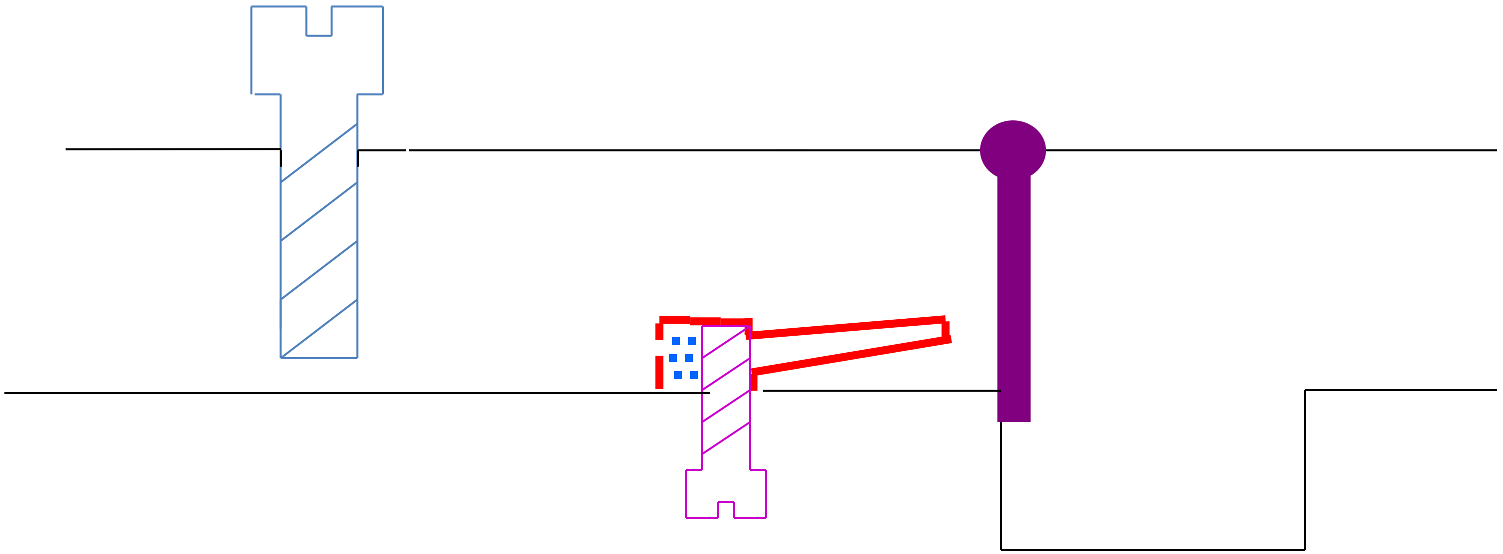
I_C (mA)
6
5
4
3
2
1
I_B=60 uA
I_B=50 uA
I_B=40 uA
I_B2
Active region
Q-point
I_B=30 uA
I_B1
I_B=20 uA
I_B=10 uA
I_B=0 uA
Saturation region
I_C2
ΔI_C
I_C1
V_CE = 7.5 V
V_CE(V)
5
10
15
20
V_CE(sat)
Cutoff region

Analogy with Transistor in Active Region: Fluid-jet operated Valve



Emitter Base Junction – FB
Collector Base Junction – RB

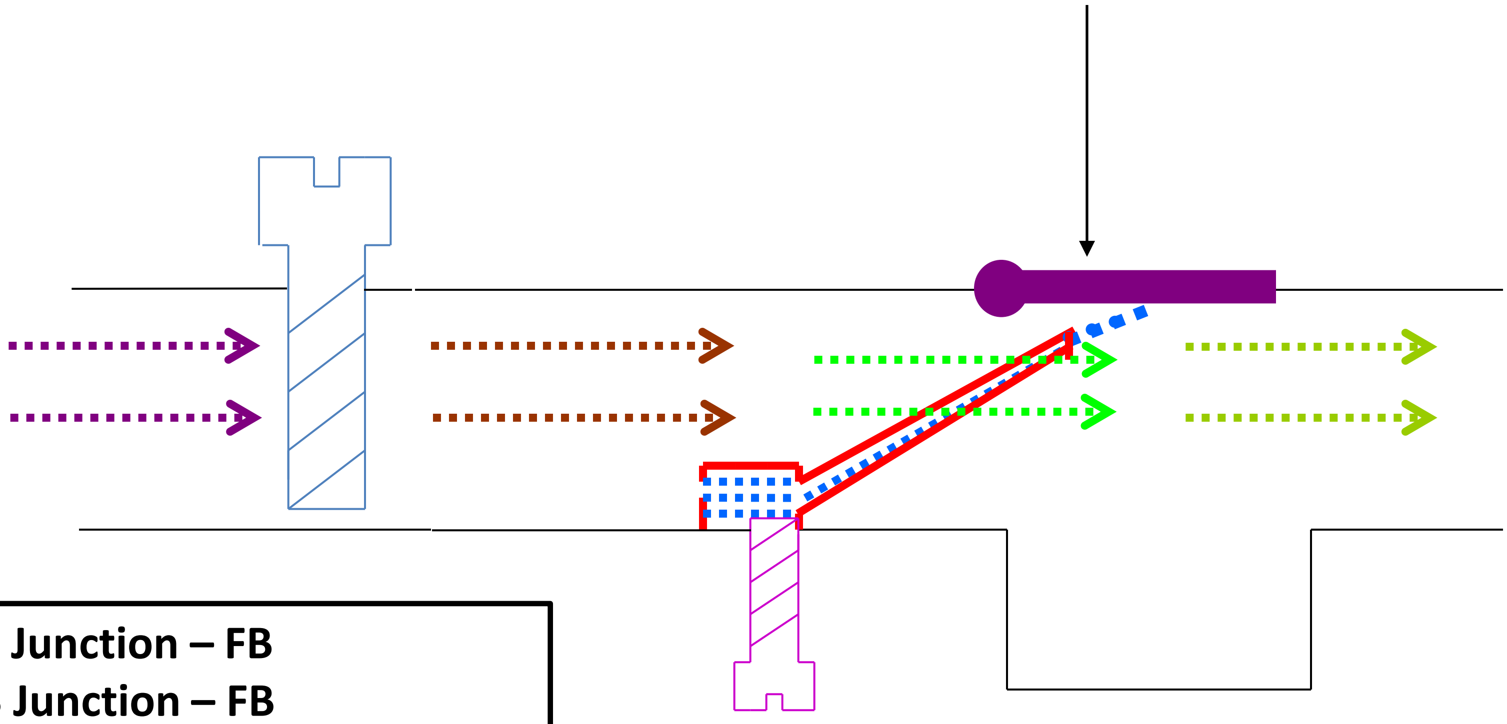
Analogy with Transistor Cutoff Fluid-jet operated Valve



Emitter Base Junction – RB
Collector Base Junction – RB

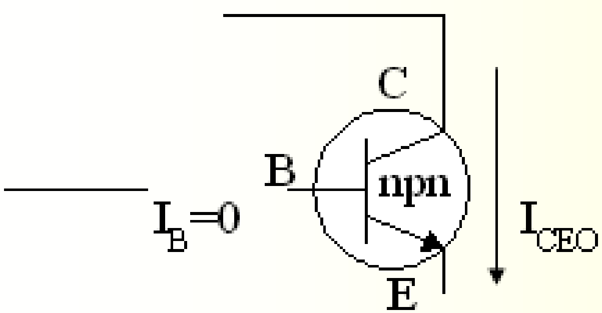
Analogy with Transistor Saturation Fluid-jet operated Valve

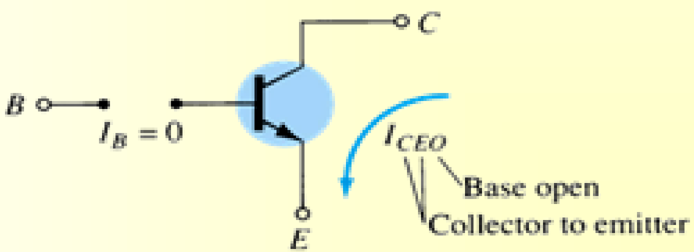
The valve is wide open; changing valve position a little bit does not have much influence on the flow rate.

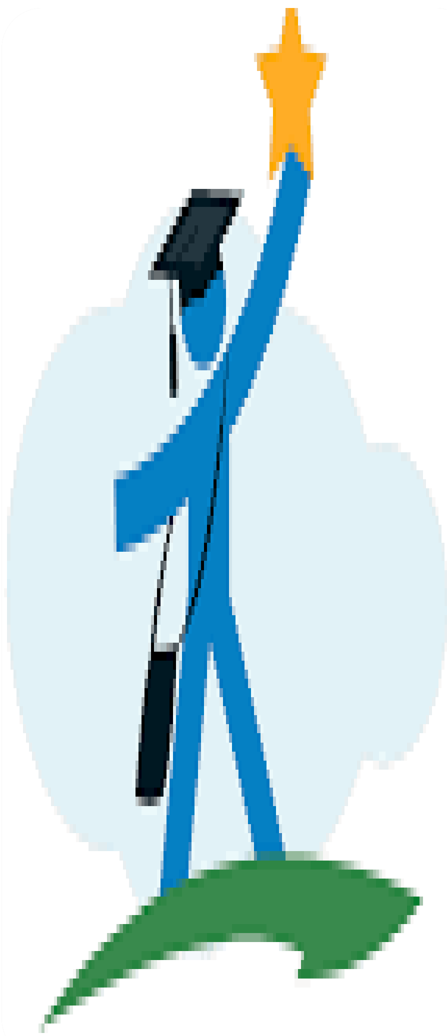


E-B Junction – FB
C-B Junction – FB

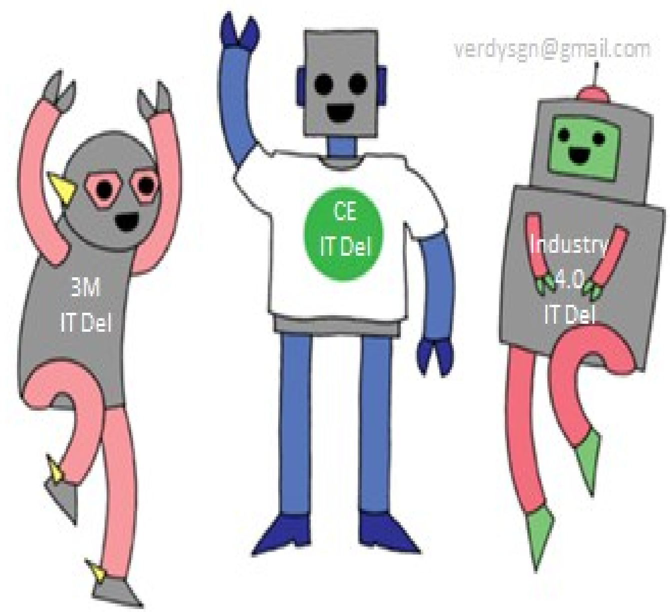
Active region	Saturation region	Cut-off region
• B-E junction is forward bias • C-B junction is reverse bias • can be employed for voltage, current and power amplification	• B-E and C-B junction is forward bias, thus the values of I_B and I_C is too big. • The value of V_{CE} is so small. • Suitable region when the transistor as a logic switch. • NOT and avoid this region when the transistor as an amplifier.	• region below $I_B = 0\mu A$ is to be avoided if an undistorted o/p signal is required • B-E junction and C-B junction is reverse bias • $I_B = 0$, I_C not zero, during this condition $I_C = I_{CEO}$ where is this current flow when B-E is reverse bias.








Thanks!


verdysgn@gmail.com
3M
IT Del
CE
IT Del
Industry
4.0
IT Del