vPIM: Efficient Virtual Address Translation for Scalable Processing-in-Memory Architectures

Amel Fatima, Sihang Liu, Korakit Seemakhupt, Rachata Ausavarungnirun, Samira Khan

Summary

- Multiple PIM stacks provide increase capacity for emerging data-intensive workloads

Problem: Address translation incurs significant overhead in accessing multiple PIM stacks

- ***Radix-based translation:*** Multiple sequential cross-stack page table walks
- ***Cuckoo hash-based translation:*** Multiple parallel accesses across memory stacks

Goal: *Design an efficient address translation scheme for multi-stack PIM systems*

Observations and Key Ideas:

- *Observation: High intra-stack parallelism with multiple vaults in each stack*
- Key Idea: Network-contention-aware hash
  - Change cuckoo hash layout to generate parallel accesses within one stack across multiple vaults
  - Send only one request towards the stack and generate parallel accesses within the stack
- *Observation: High parallelism enables minimal performance loss with fewer cores*
- Key Idea: Pre-translate addresses
  - Use a few cores to run ahead future iterations of the workload
  - Pre-translate cross-stack addresses and bring them inside the same stack for future use

Result: vPIM provide 4.4x and 1.7x speedup compared to radix and cuckoo hash

Outline

- Processing-in-Memory Introduction
- Address Translation in PIM Architecture
- Challenges and Key Ideas
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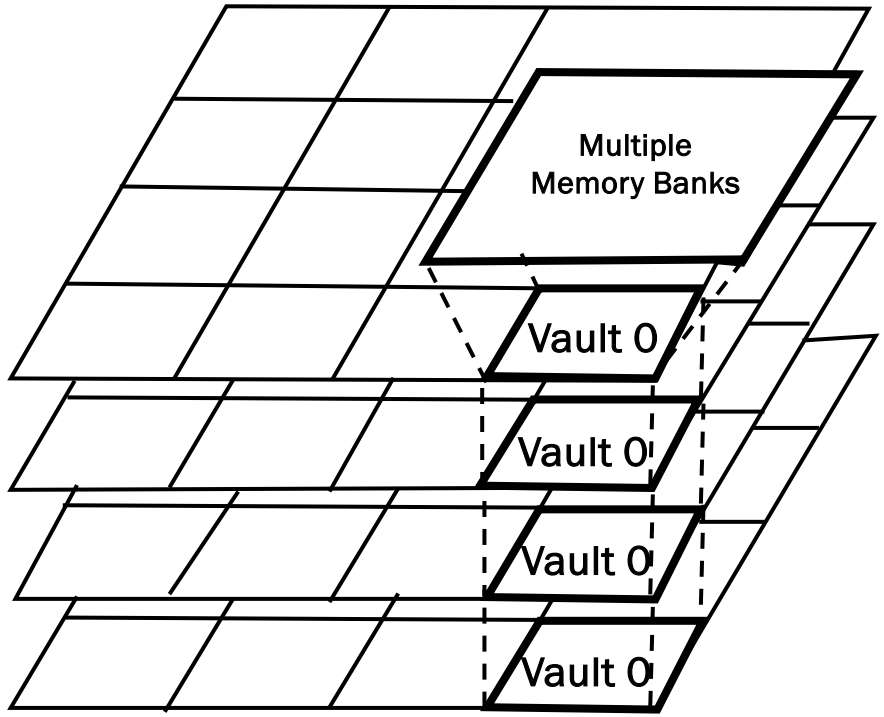

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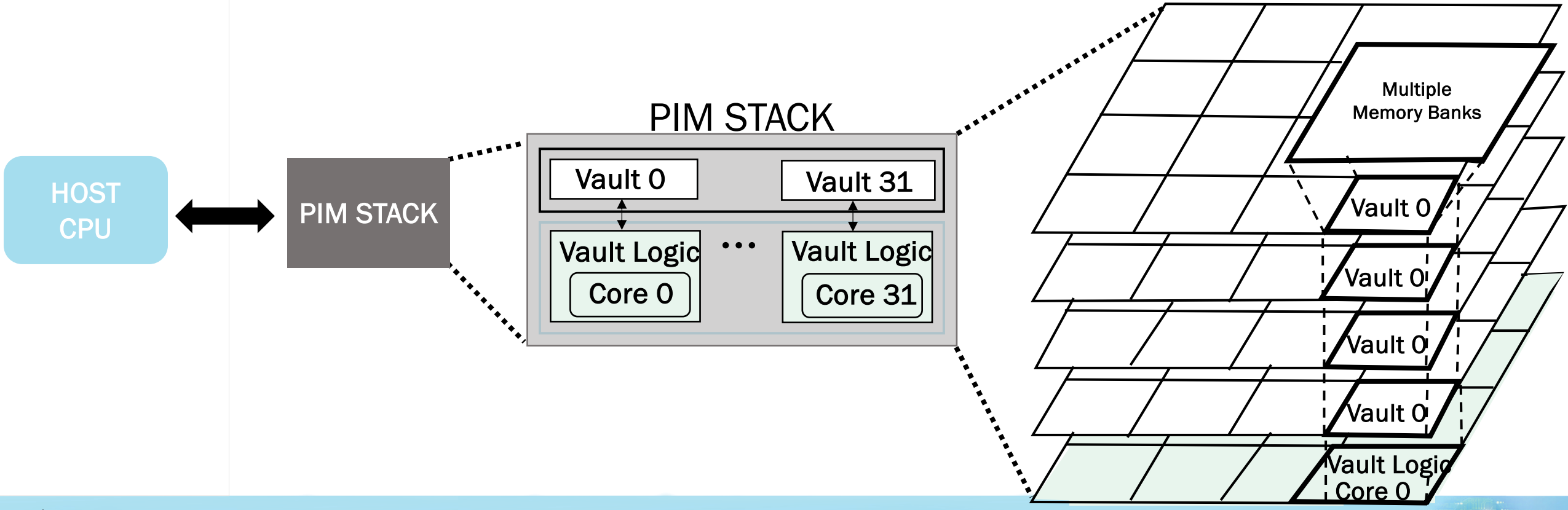

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- Prior works used PIM to reduce data movement between CPU and memory
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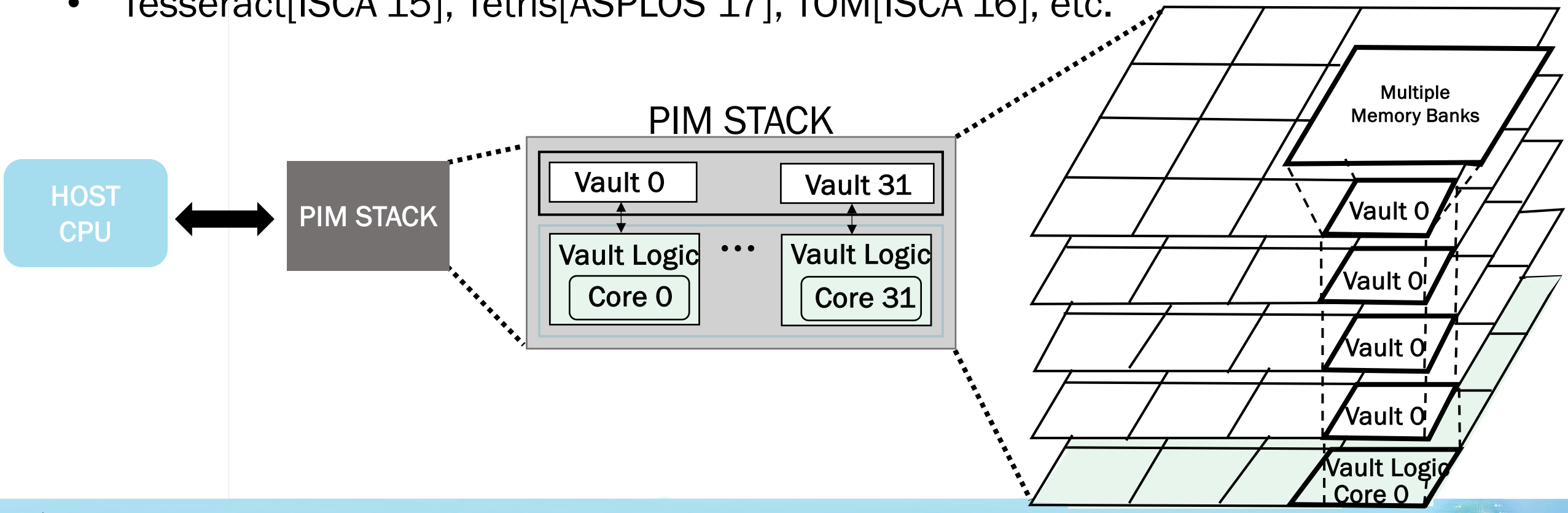

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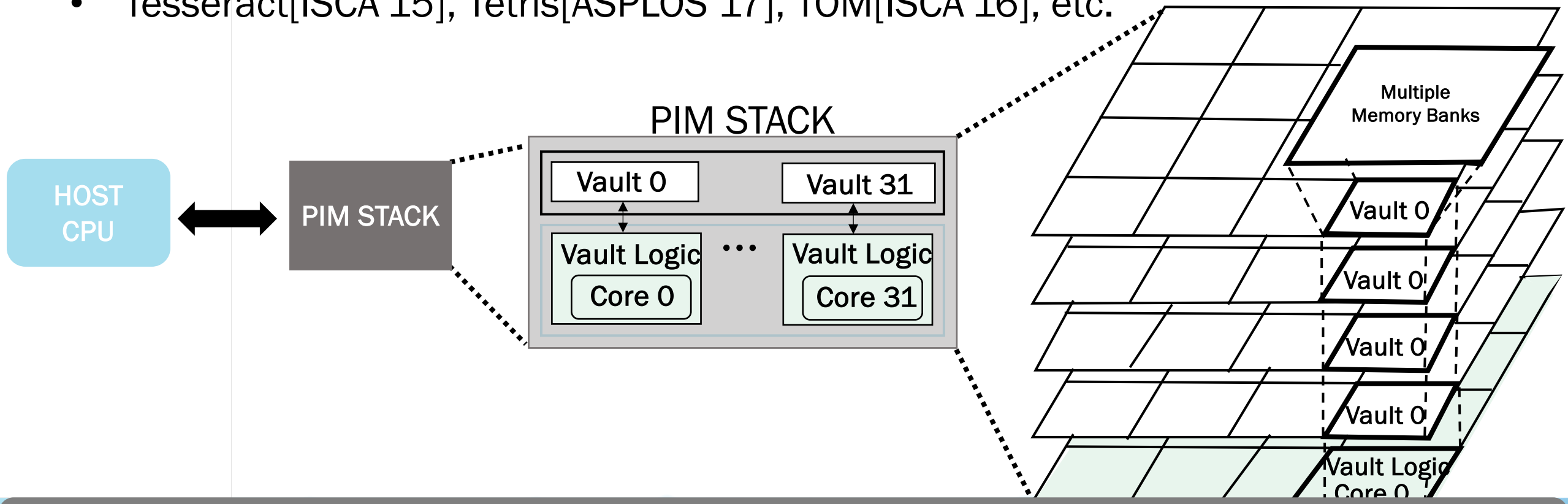
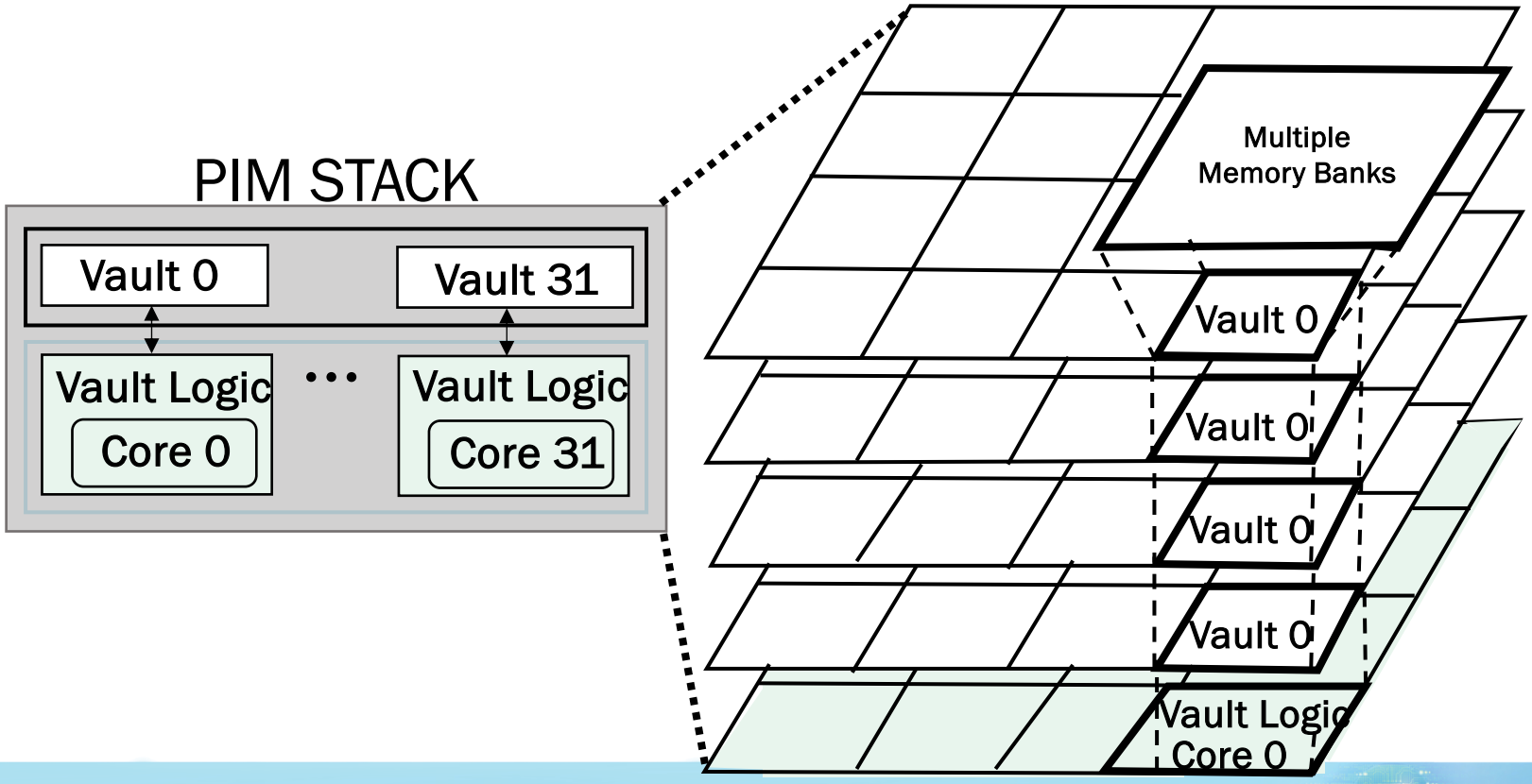


Placing computation closer to memory improves performance

Processing in Memory (PIM)

- Data-intensive applications demand more memory



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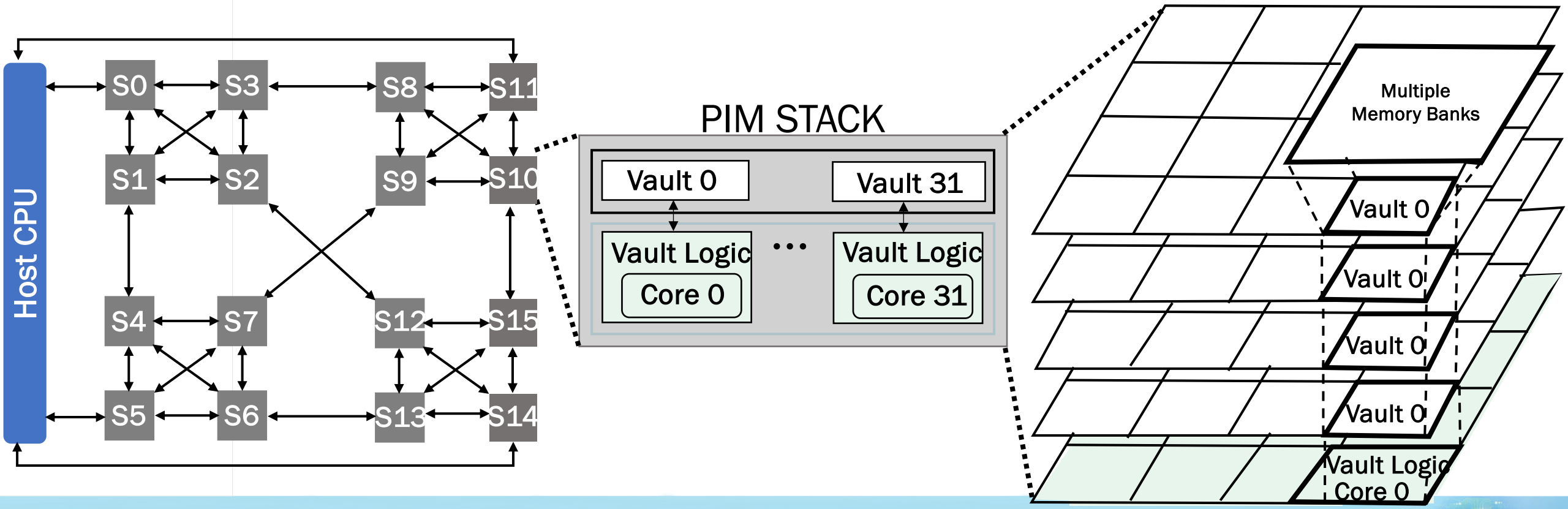
- Multiple stacks are connected over a memory network to scale up to higher capacity



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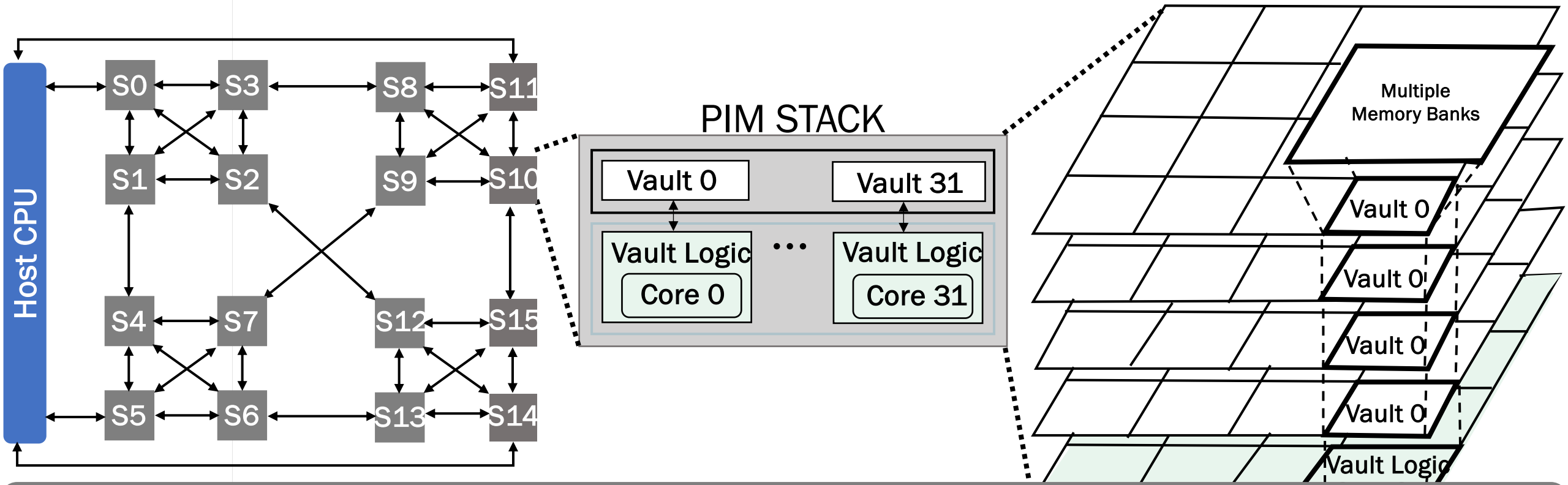

A multi-stacked PIM system provides increased capacity for emerging data-intensive applications

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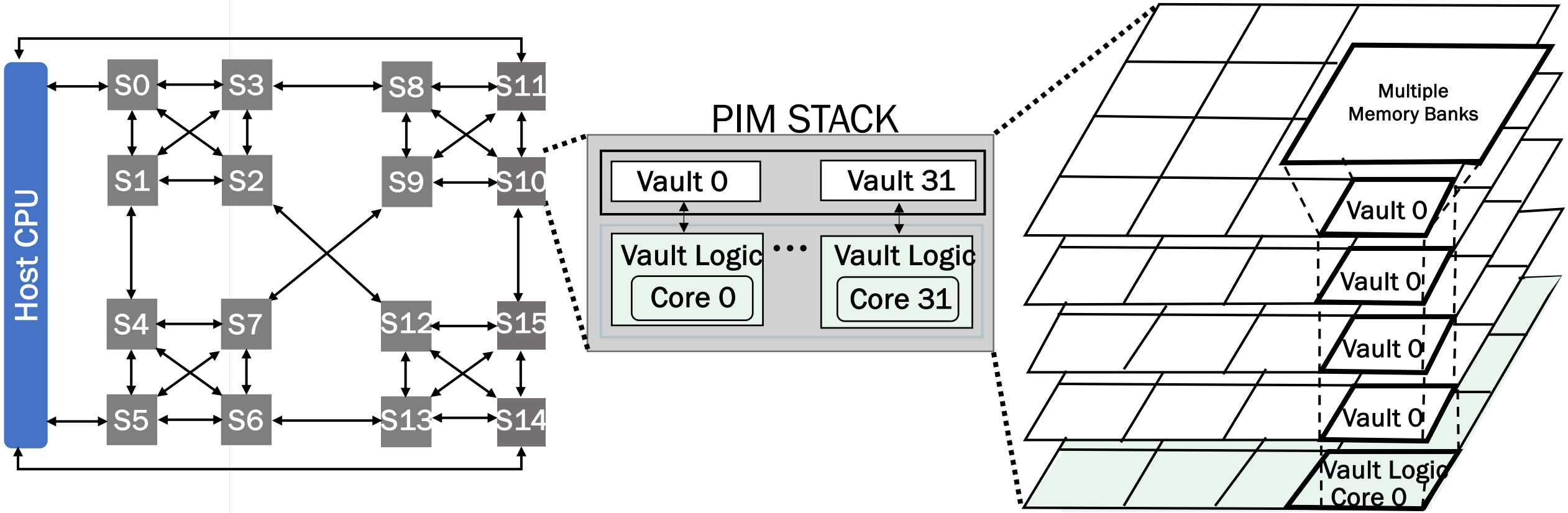

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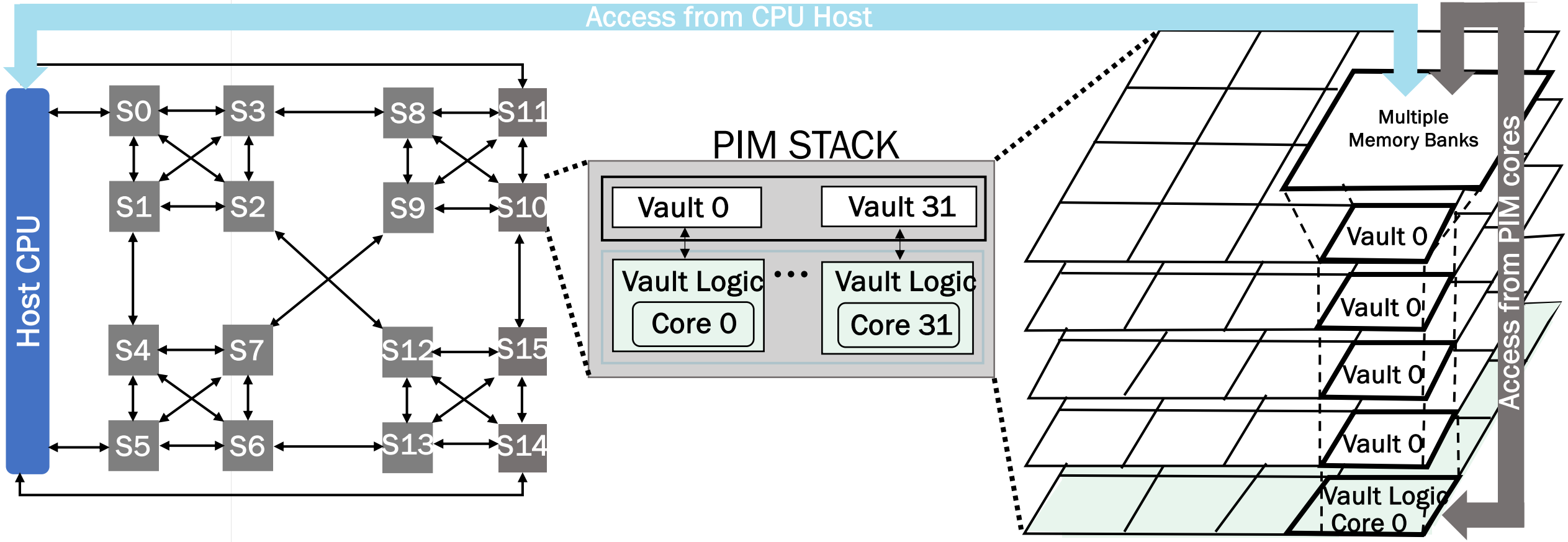

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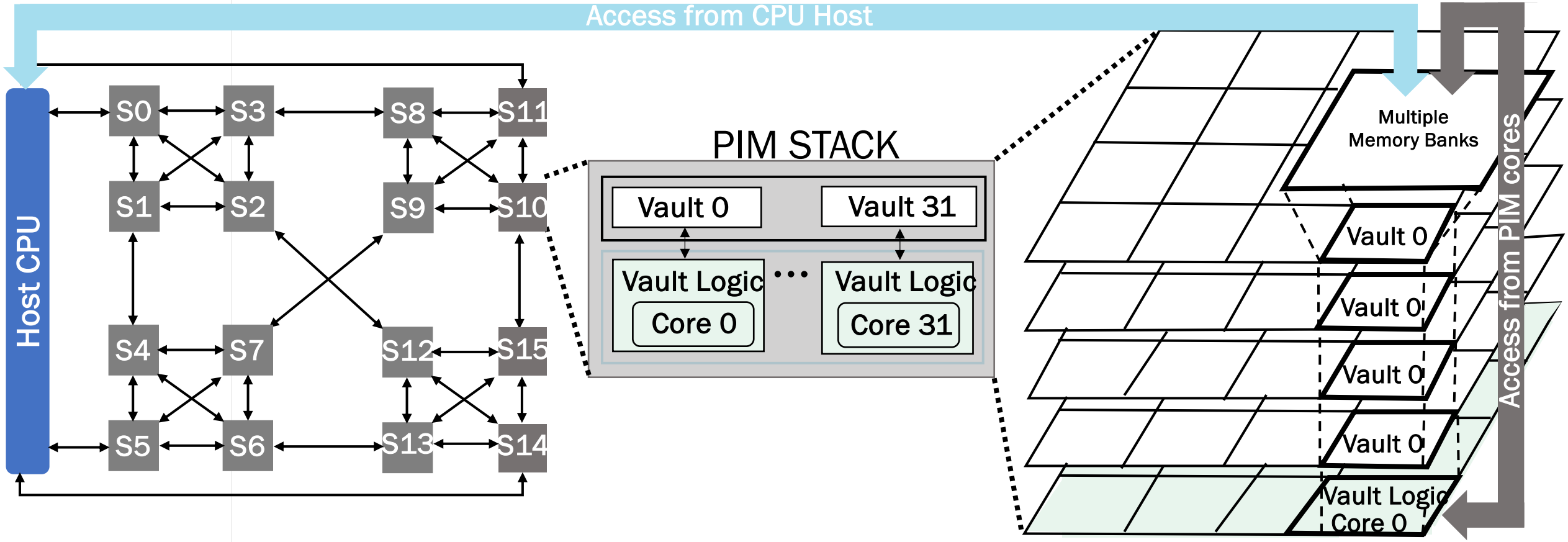

PIM provides an opportunity for a unified virtual address space

Address Translation

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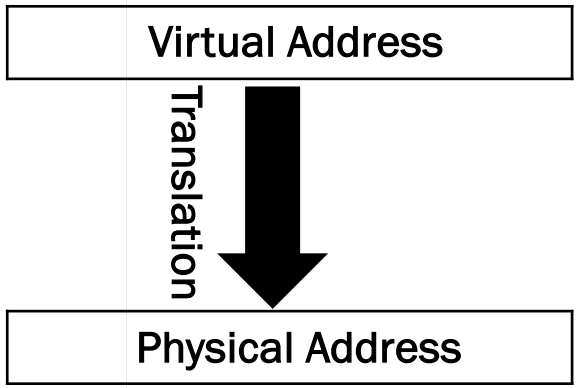

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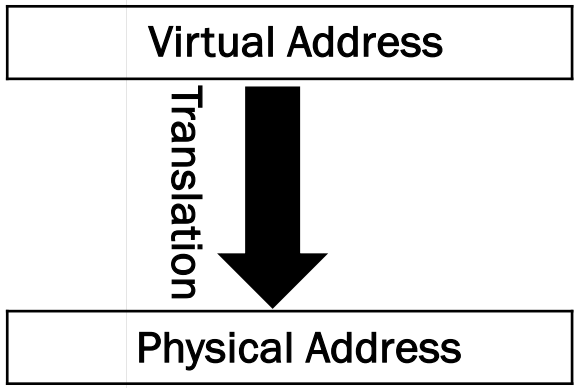

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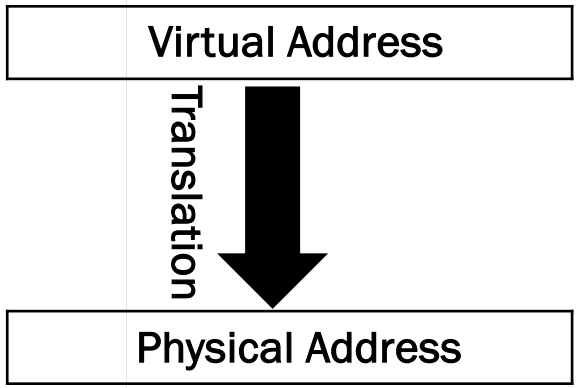

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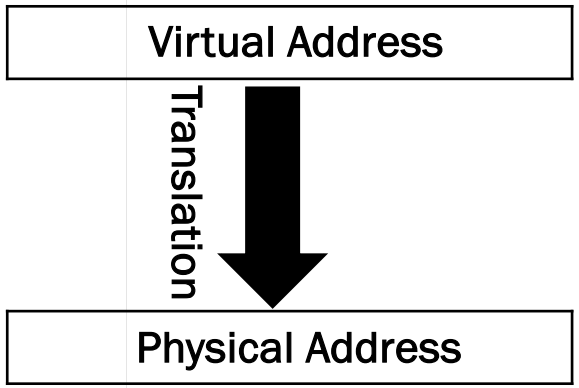

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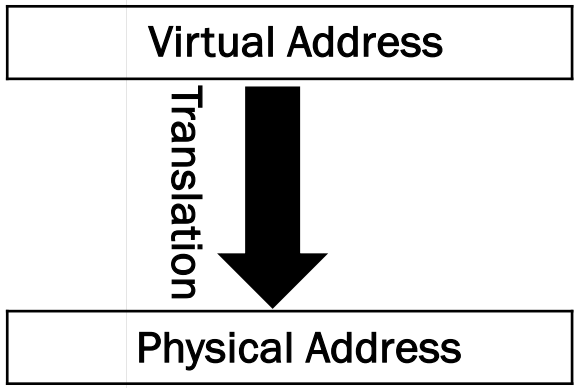

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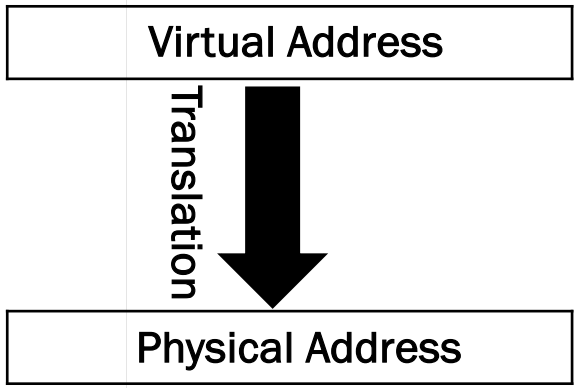

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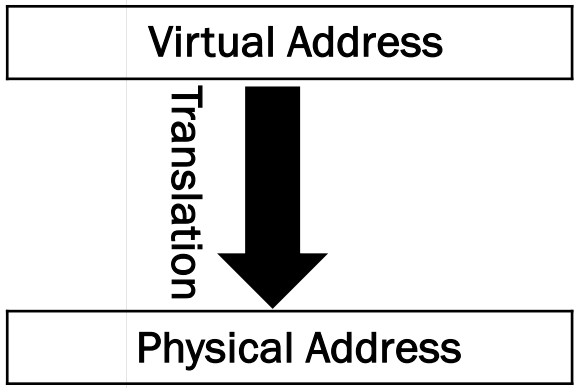

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Both radix and hash page table introduce significant overhead in multi-stacked PIM system

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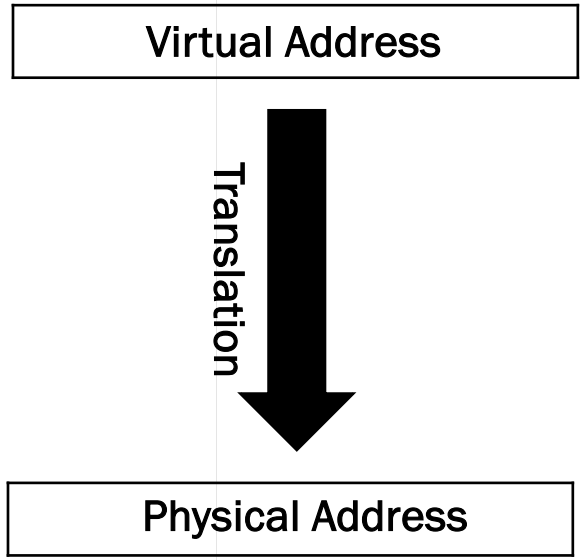

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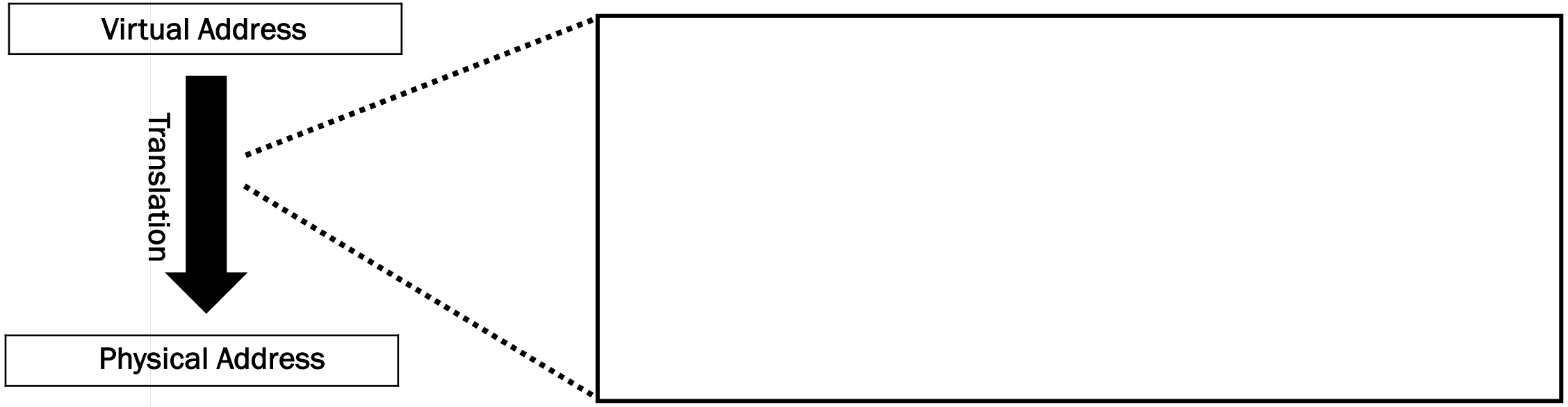

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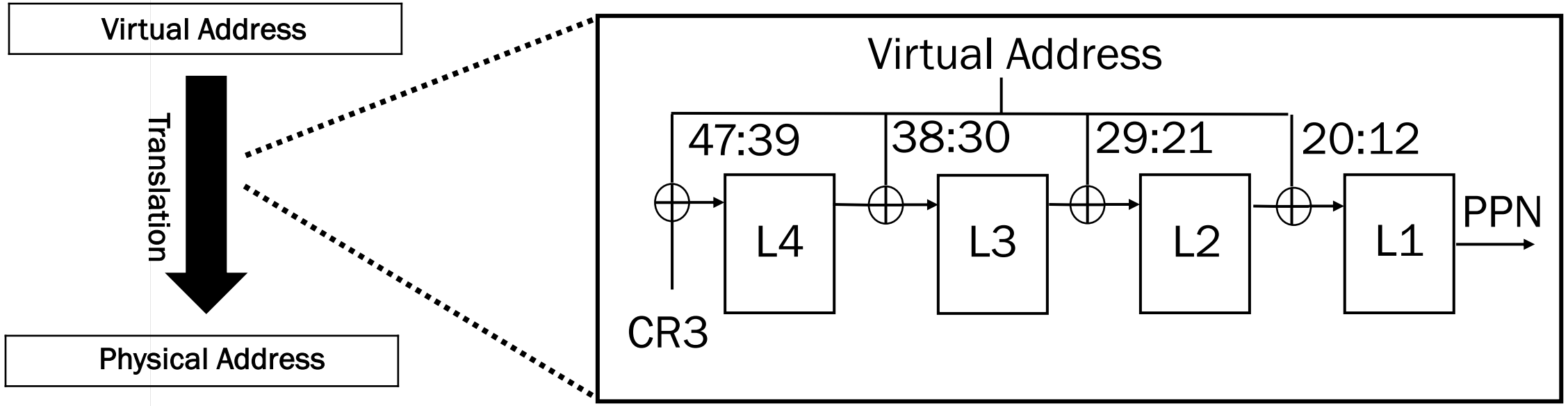

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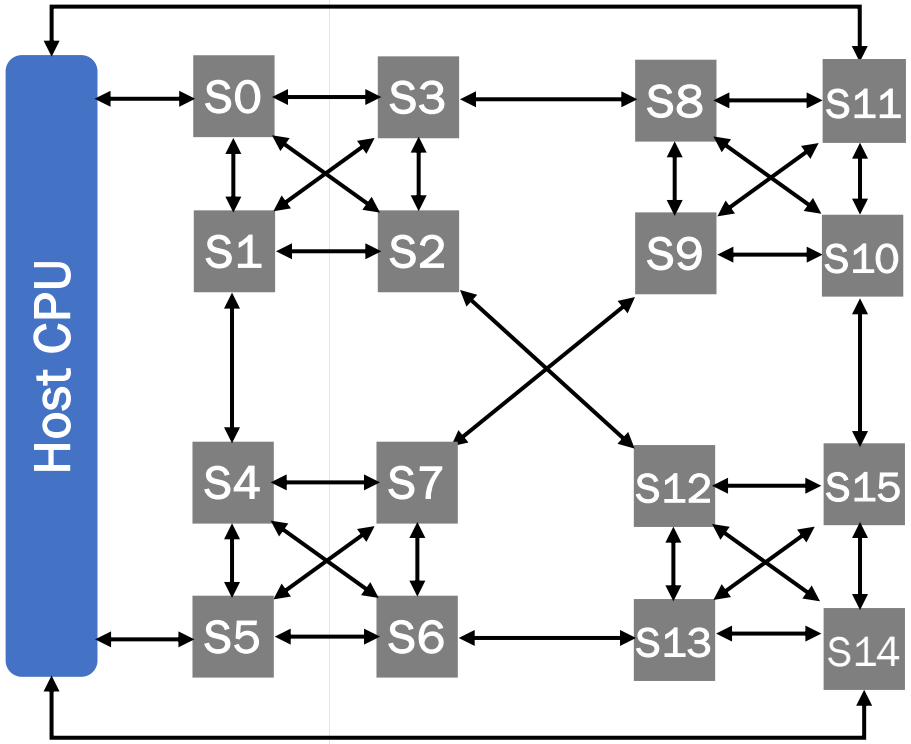

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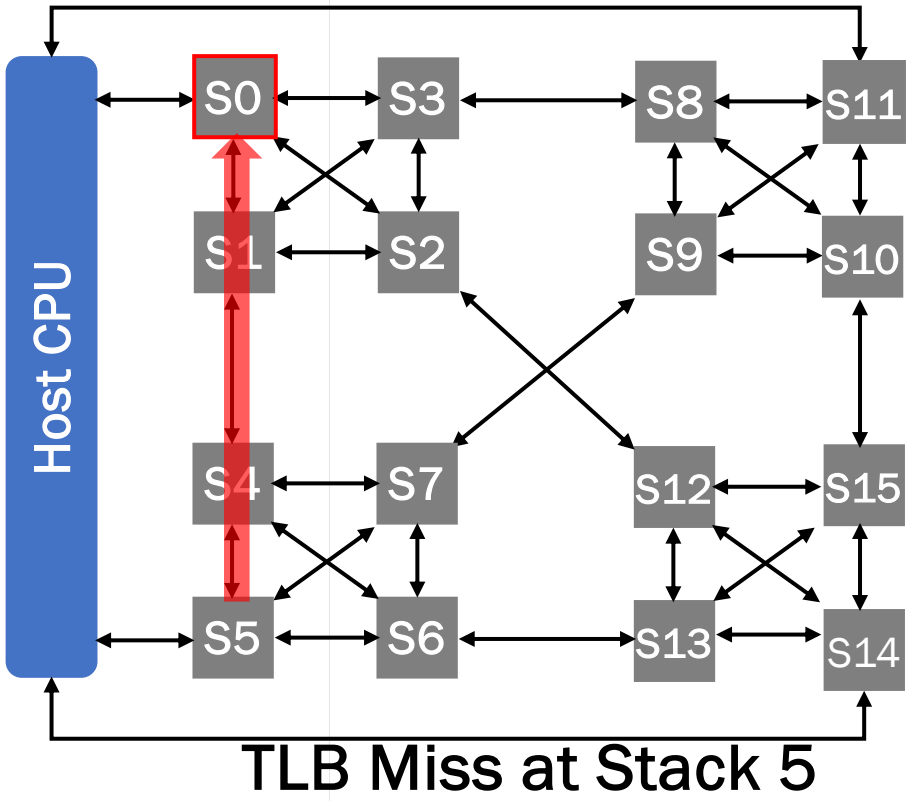

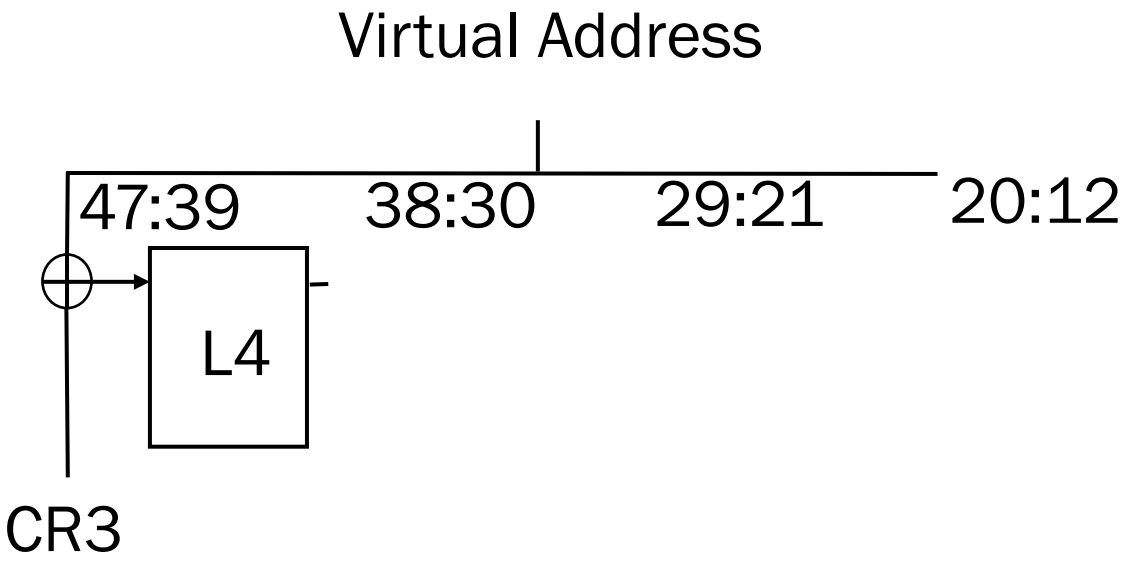

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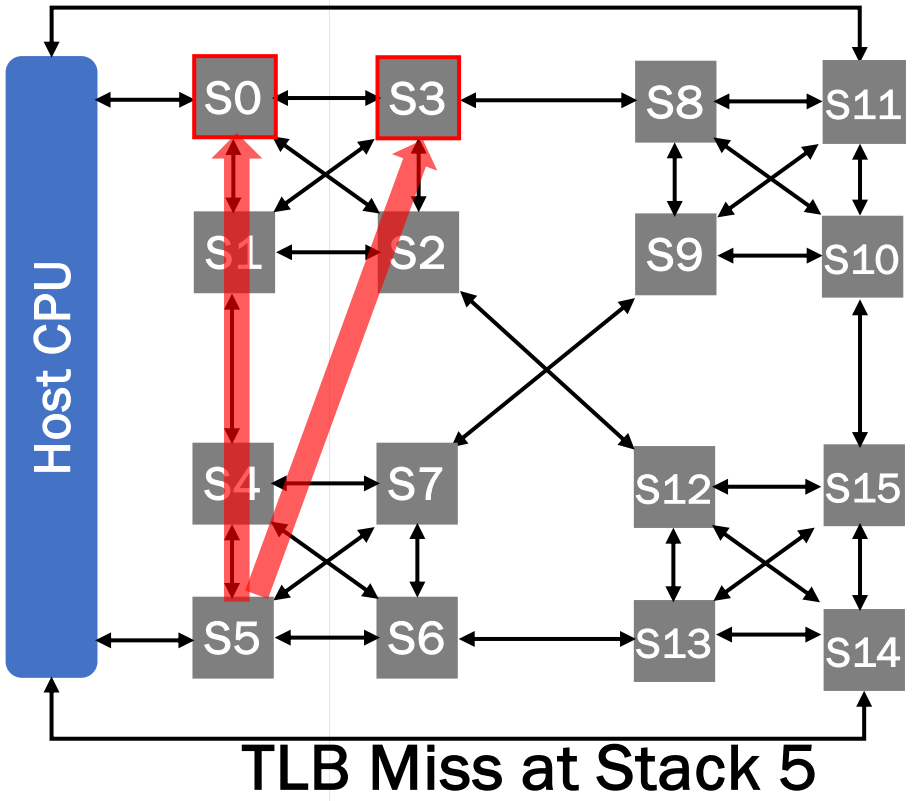

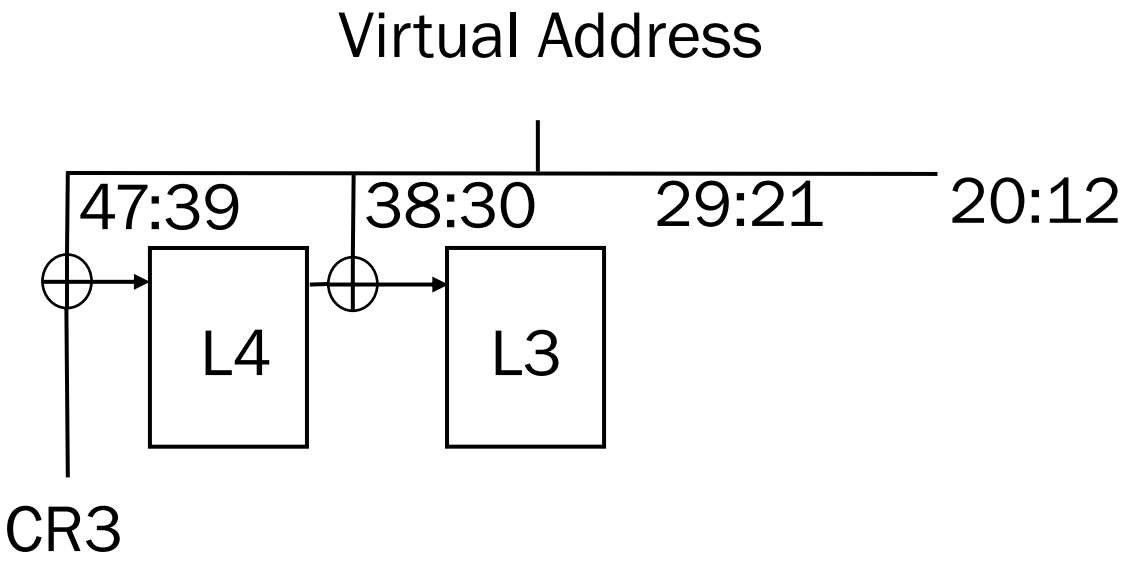

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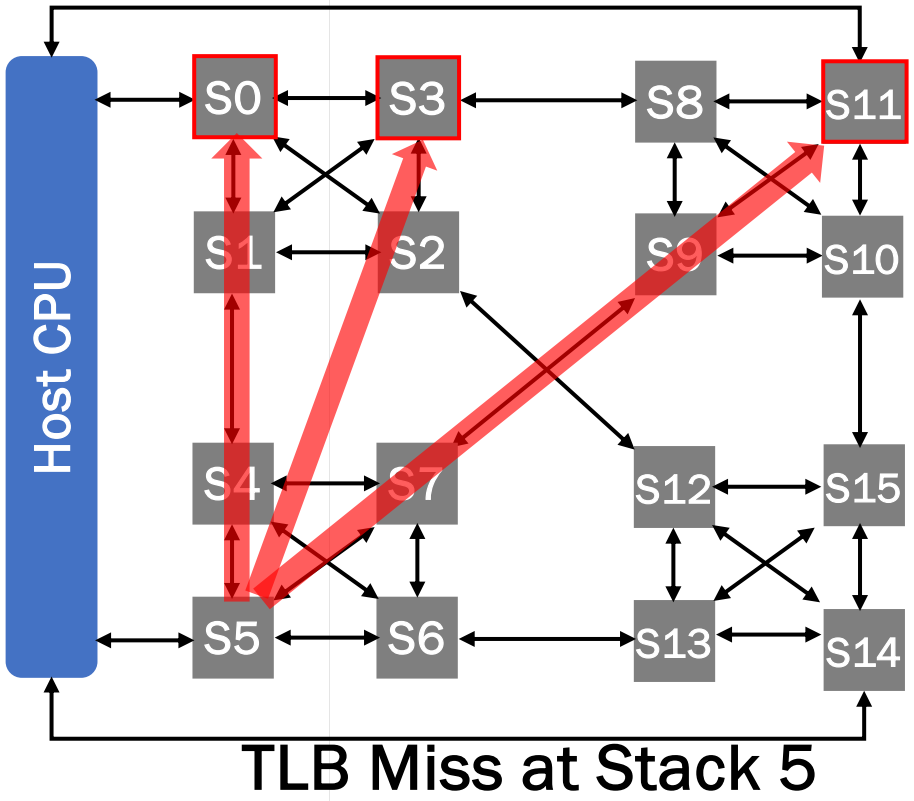

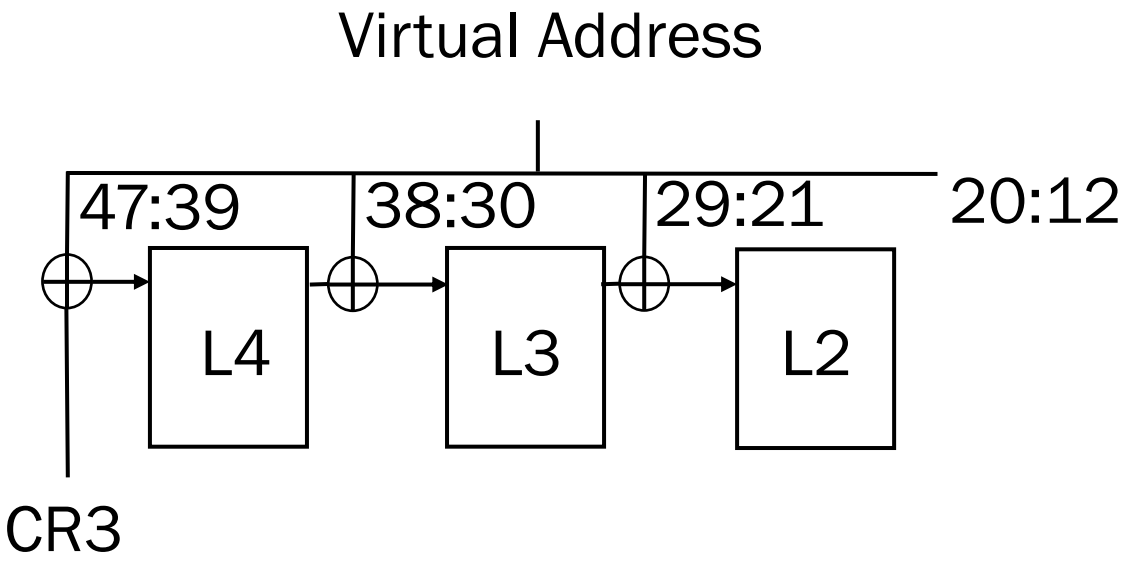

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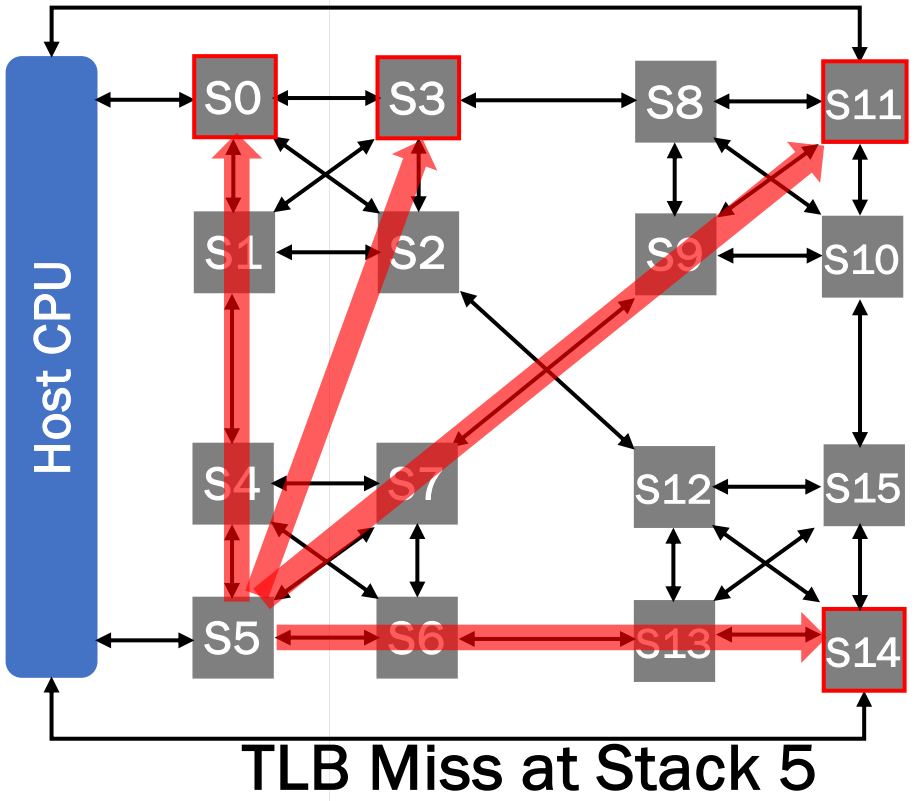

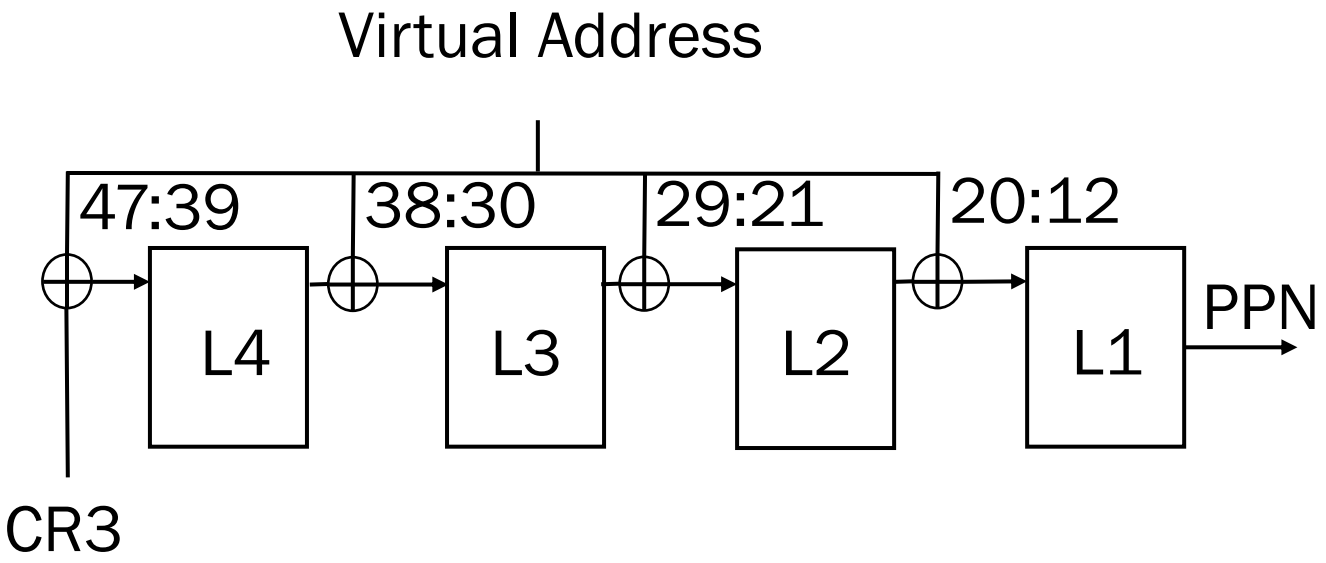

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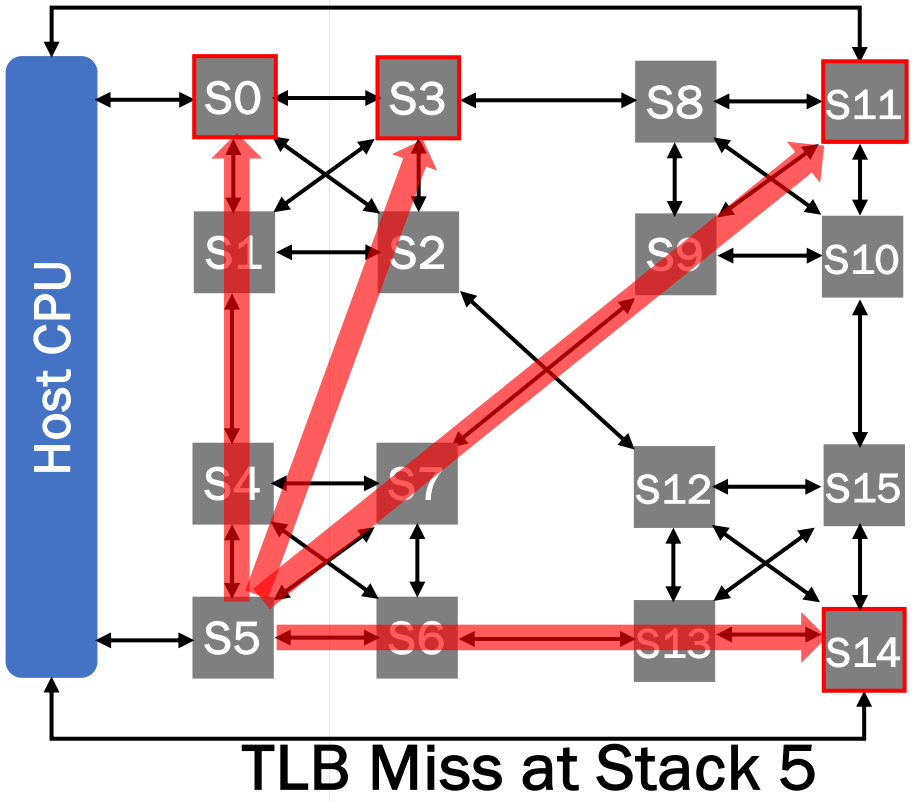
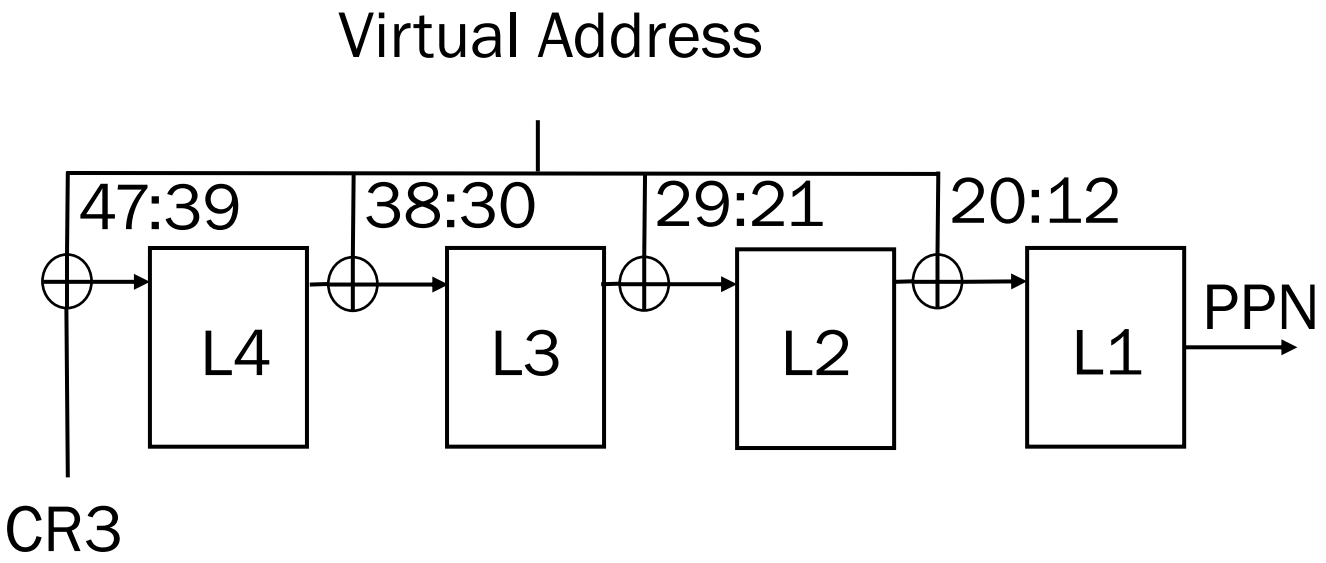
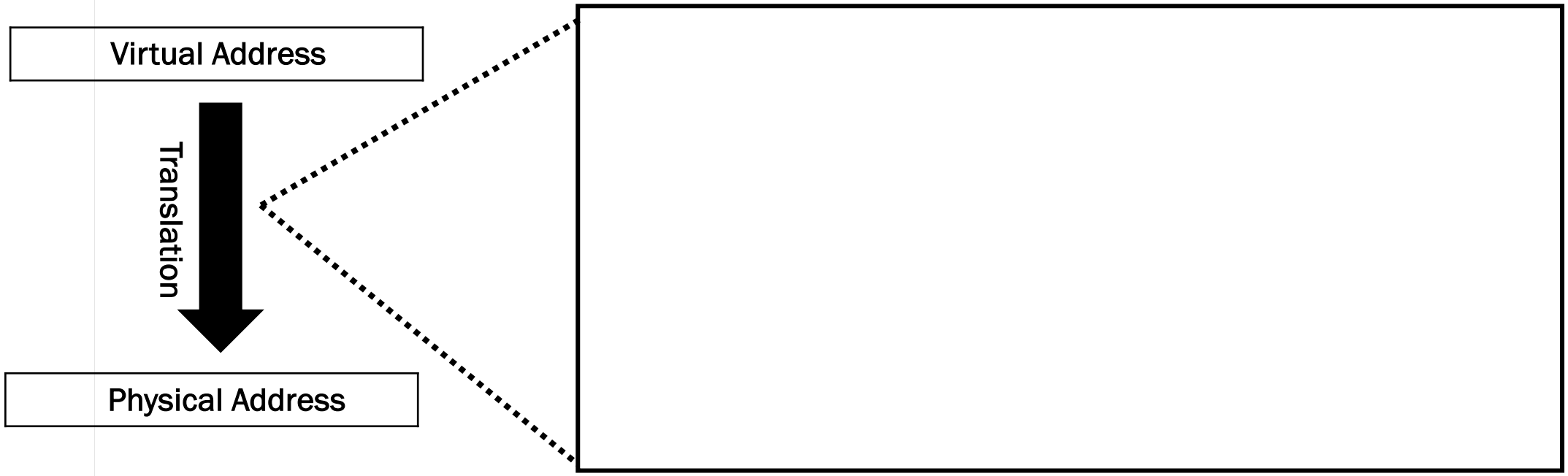




A single radix page walk can introduce sequential accesses to multiple memory stacks

Hash Based Address Translation

- Hash based translation use hash table to lookup a physical address



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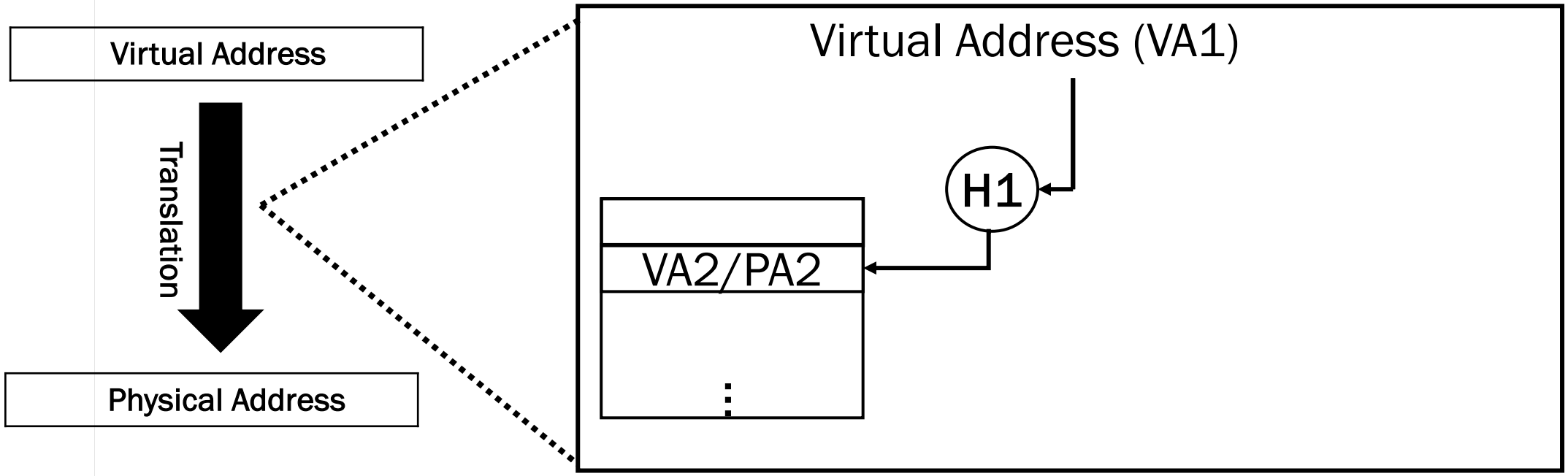

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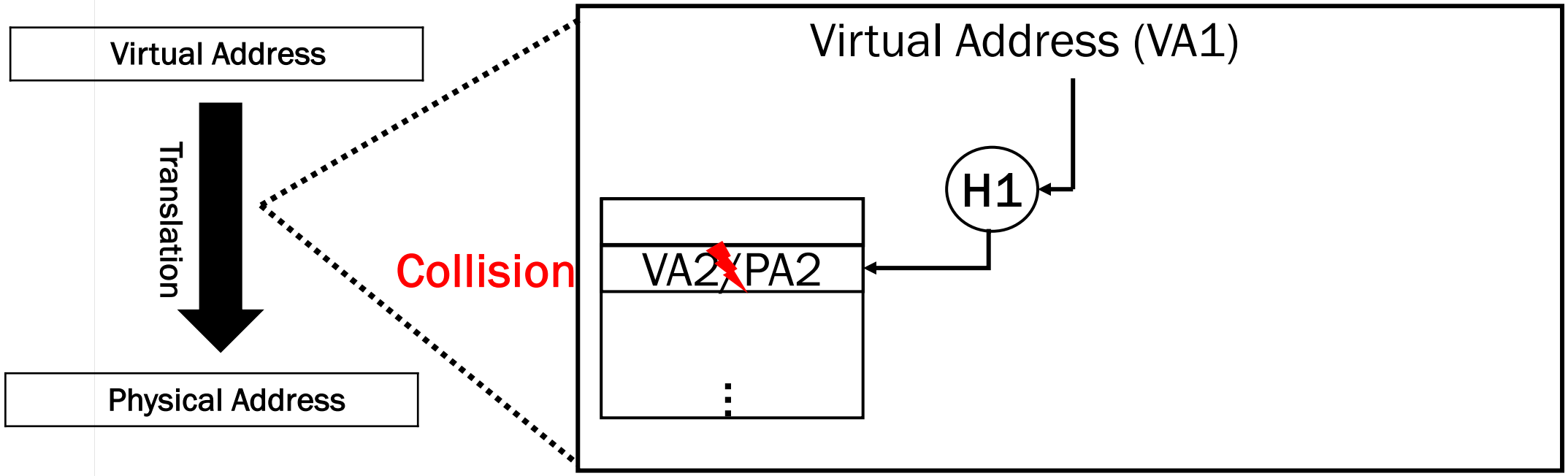

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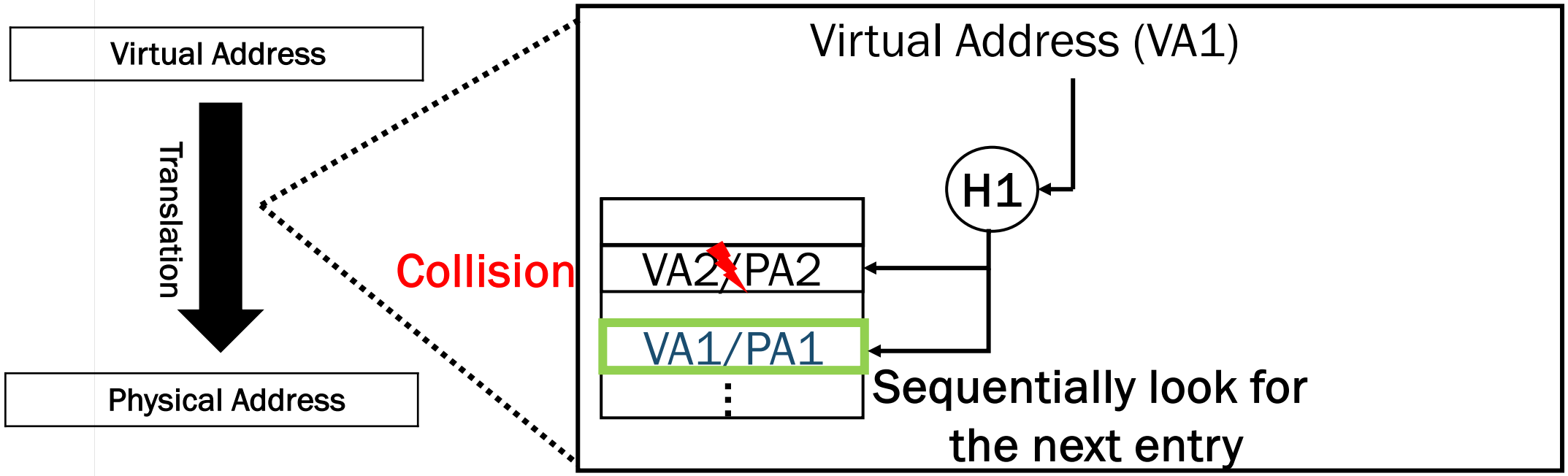

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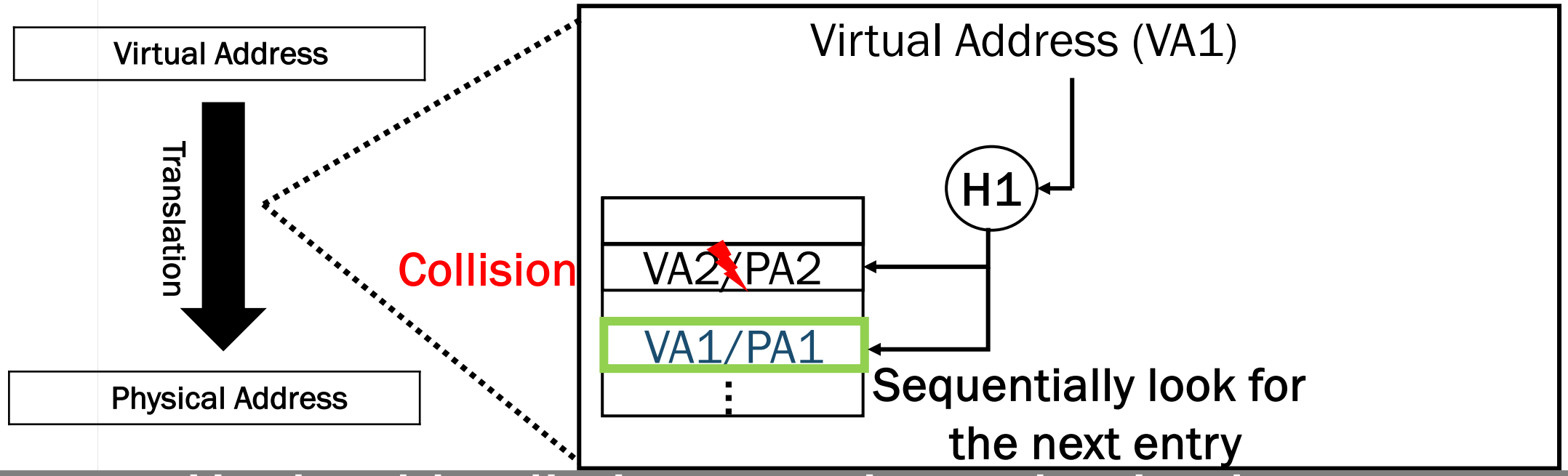

Hash table eliminates pointer chasing but introduces sequential accesses due to collisions.

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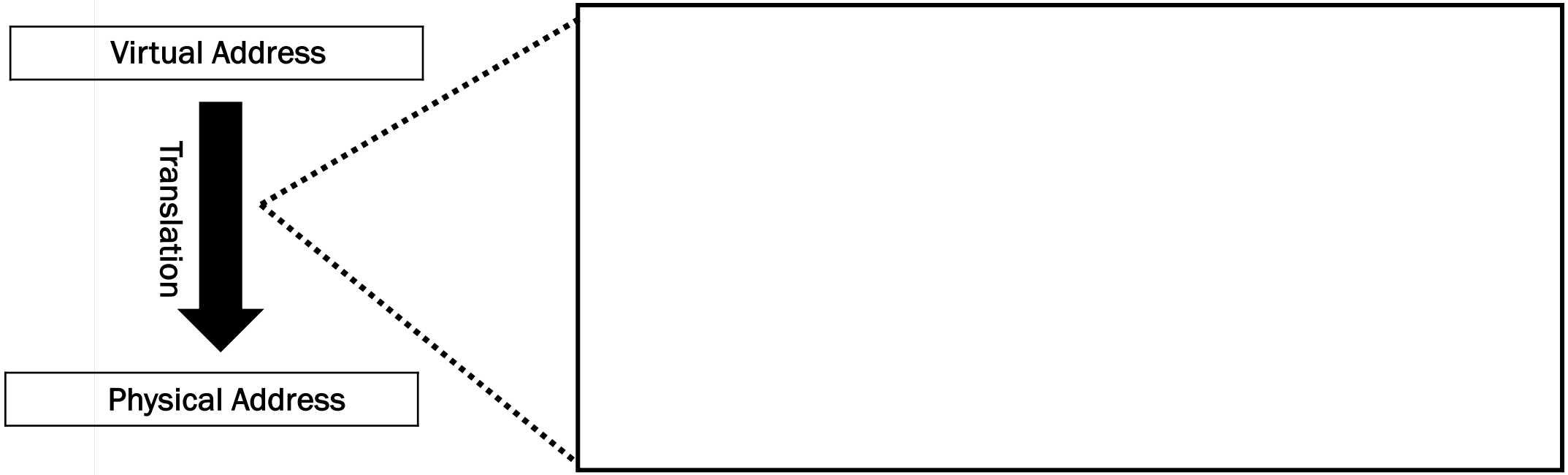
- Multiple parallel accesses are issued in hash table to mask the overhead of collisions



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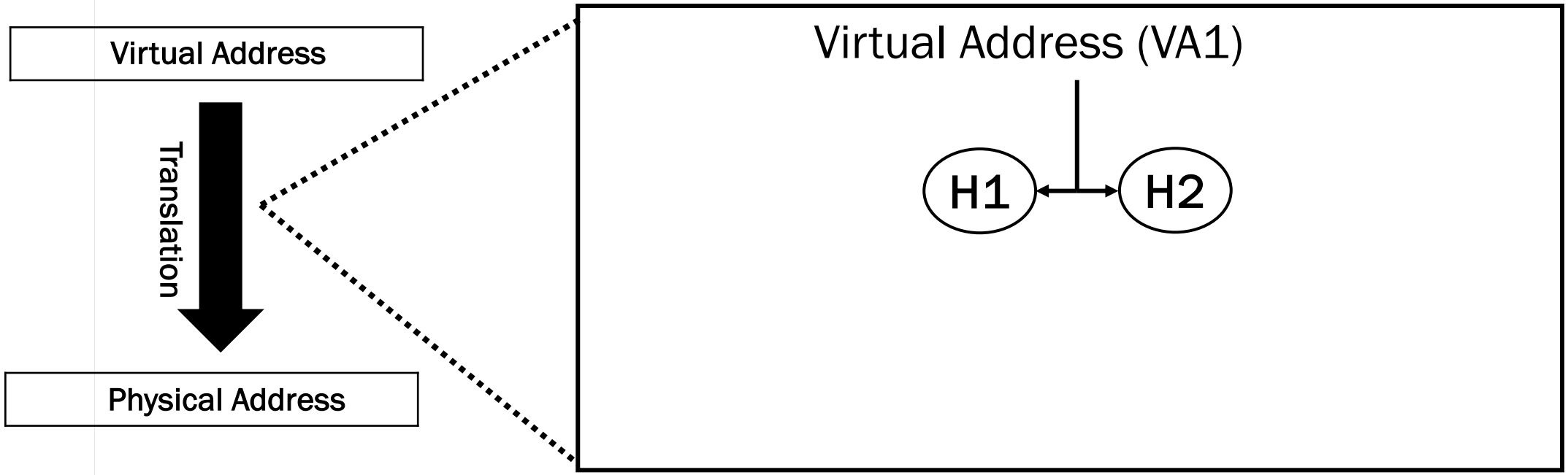

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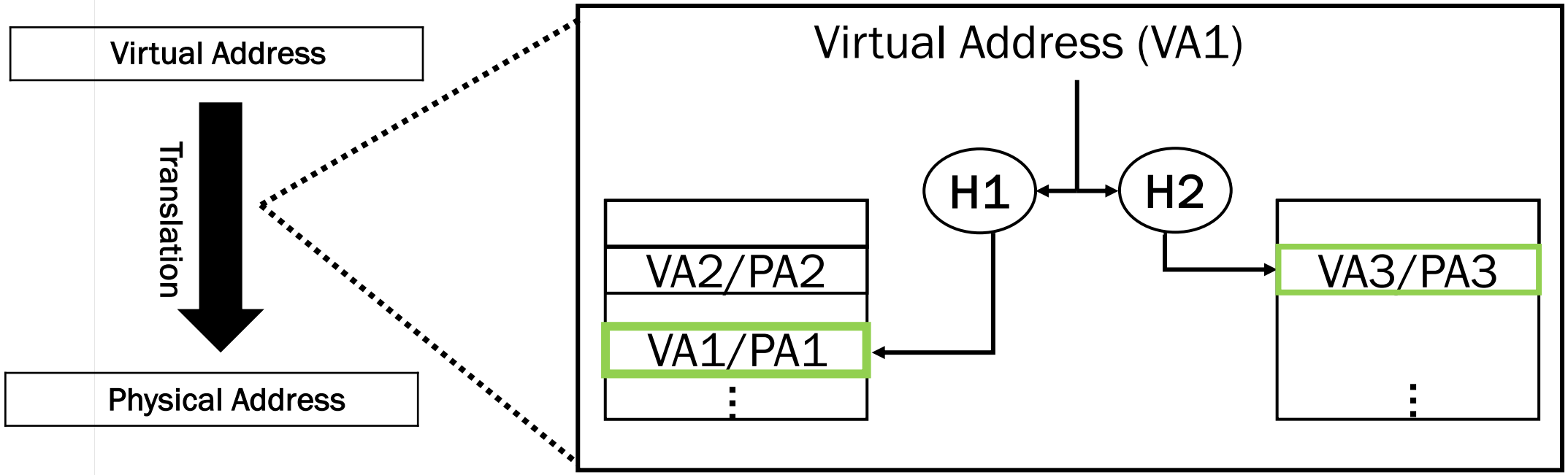

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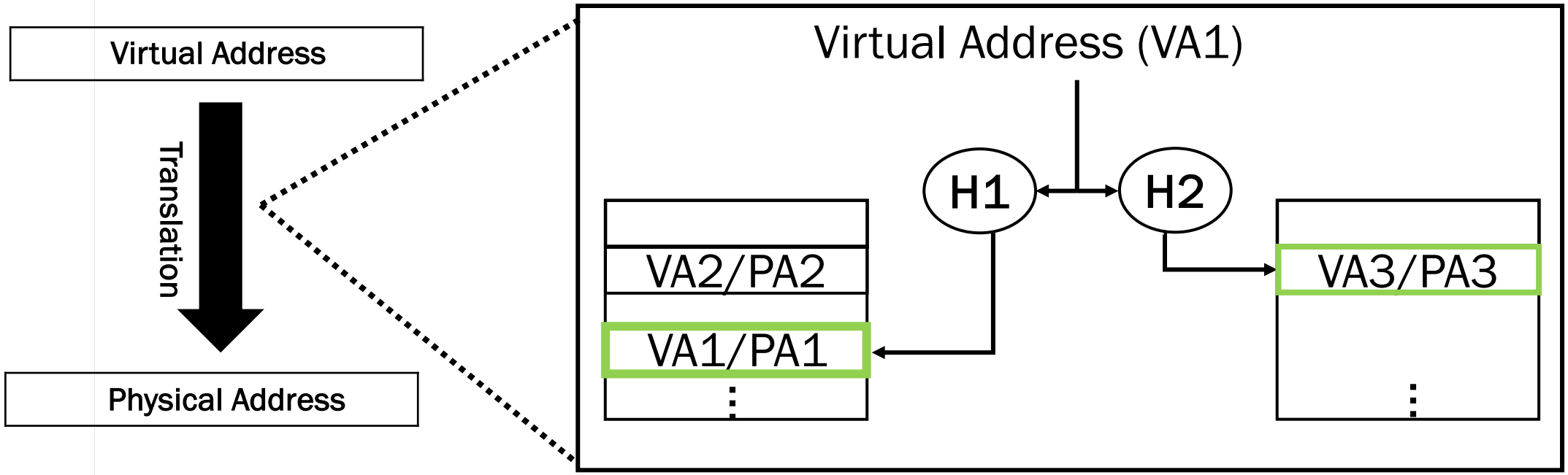
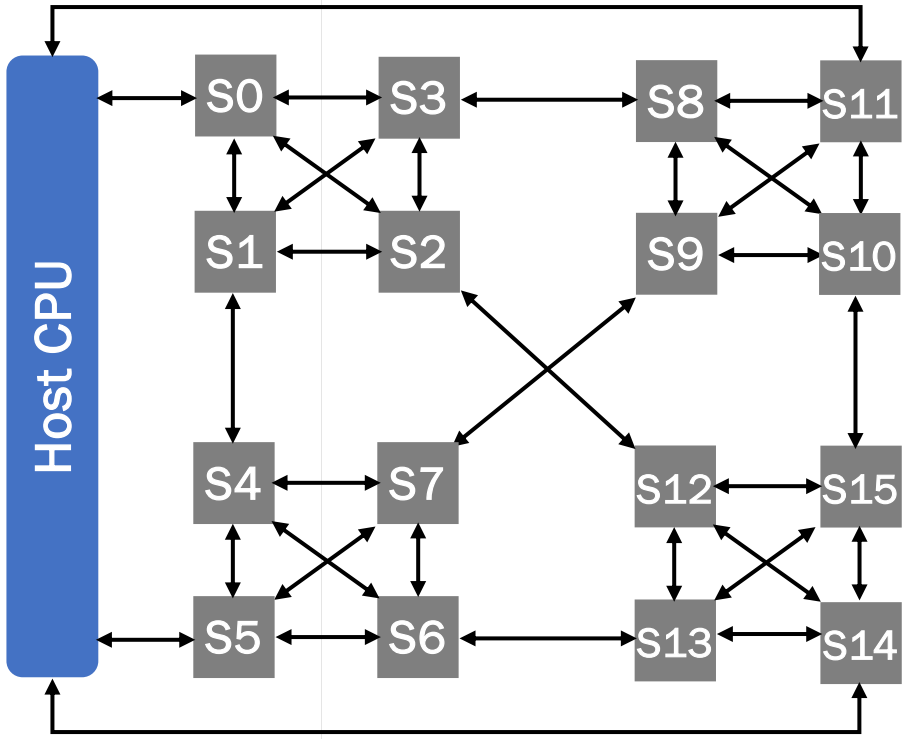


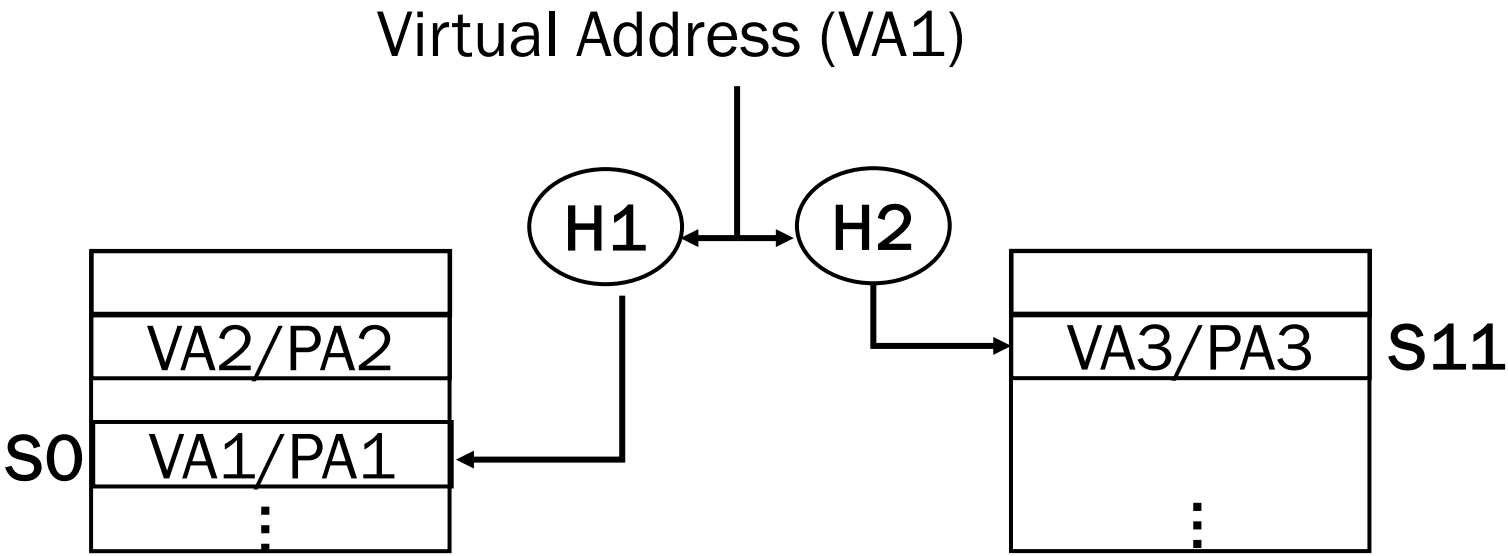
Cuckoo hash table enables parallel lookups upon collisions

Alternative: Cuckoo Hash Table in PIM

- Parallel accesses are issued across different stacks in PIM



TLB Miss at Stack 5



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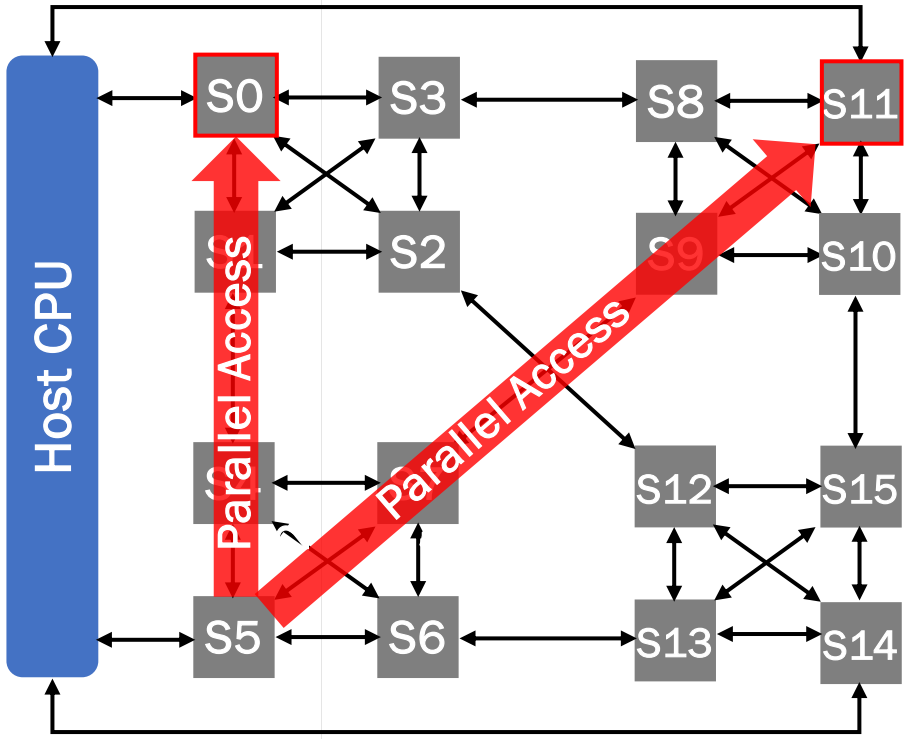

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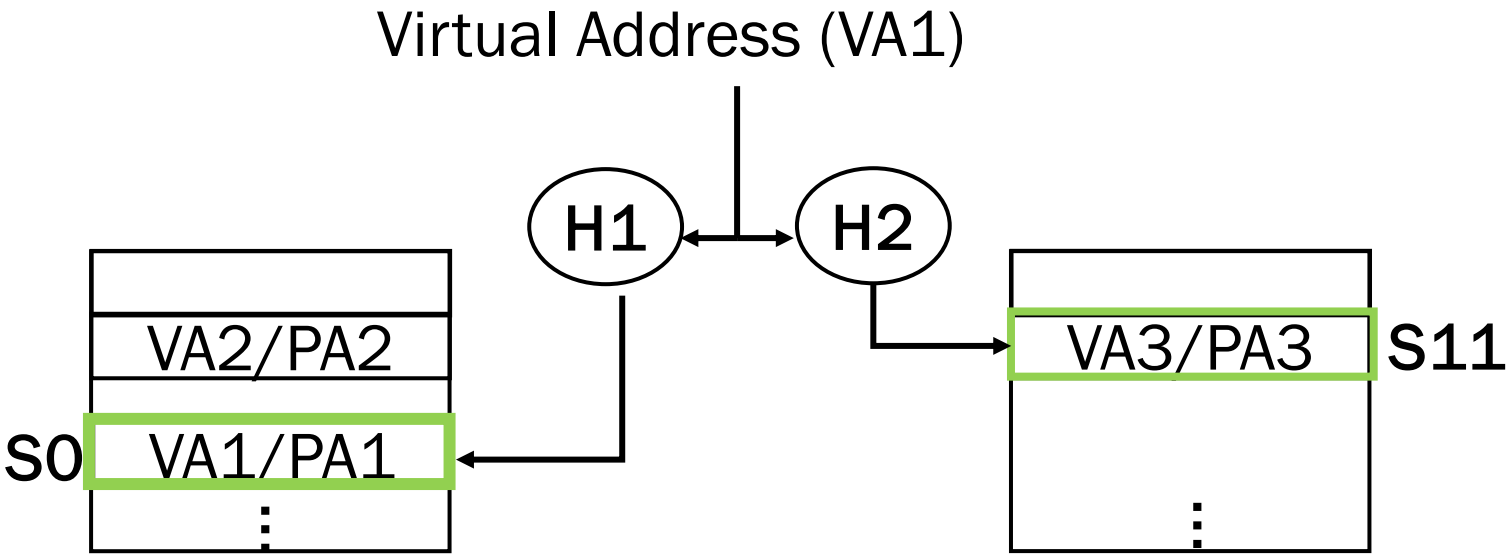

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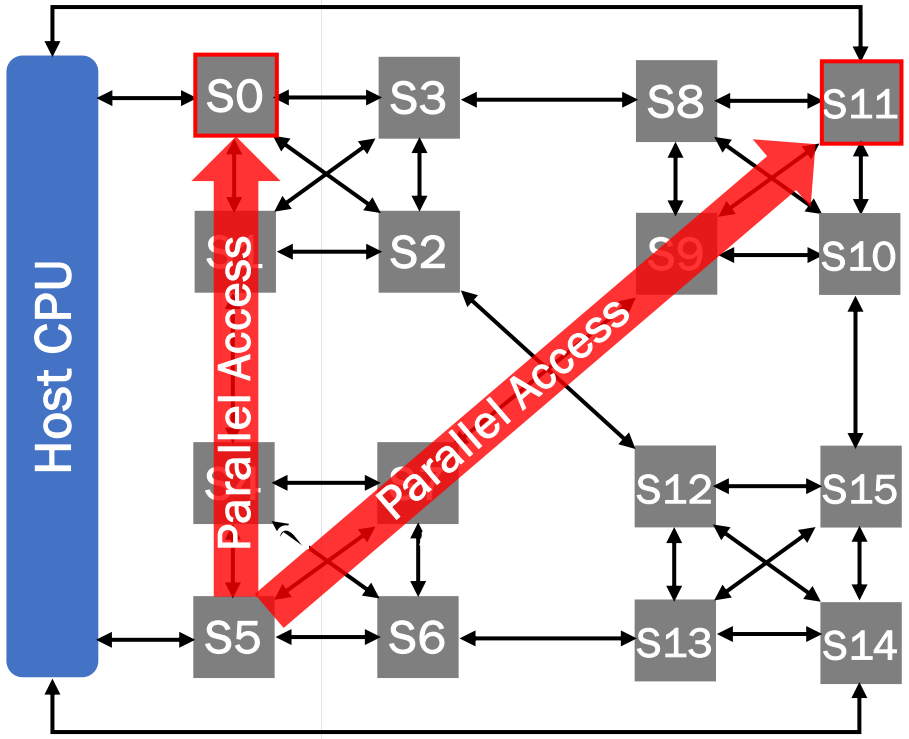

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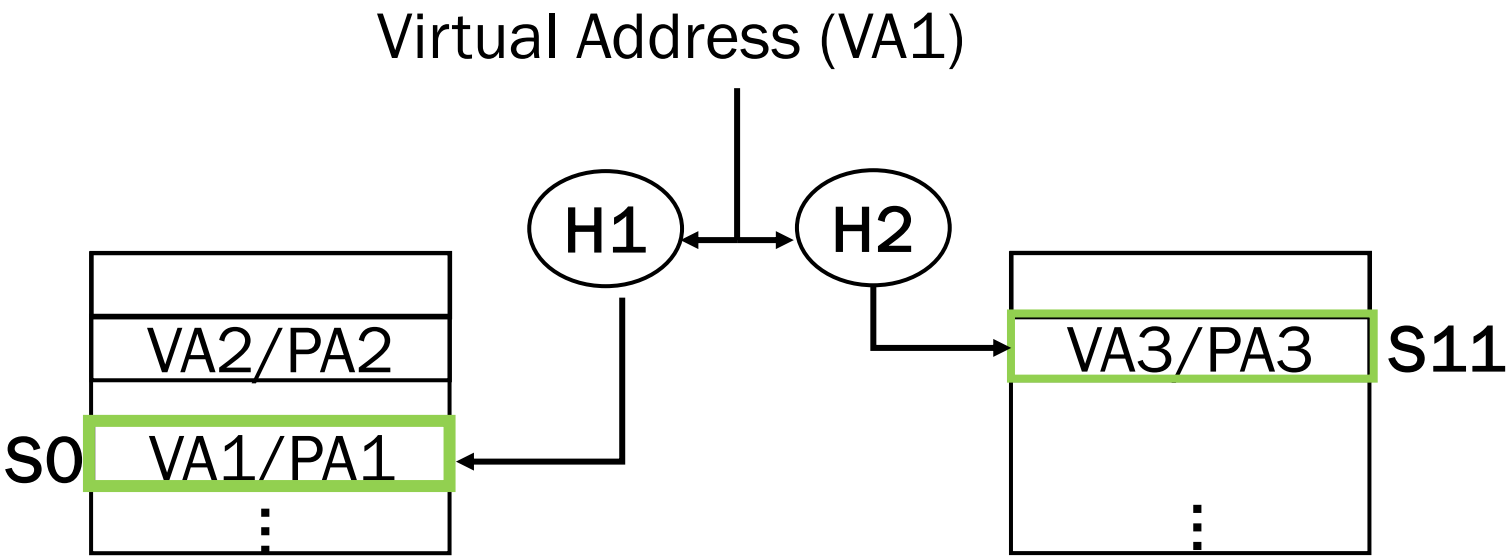

Parallel cross-stack accesses increase network contention and thus overall memory access time

Overhead of Hash and Radix Translation in PIM

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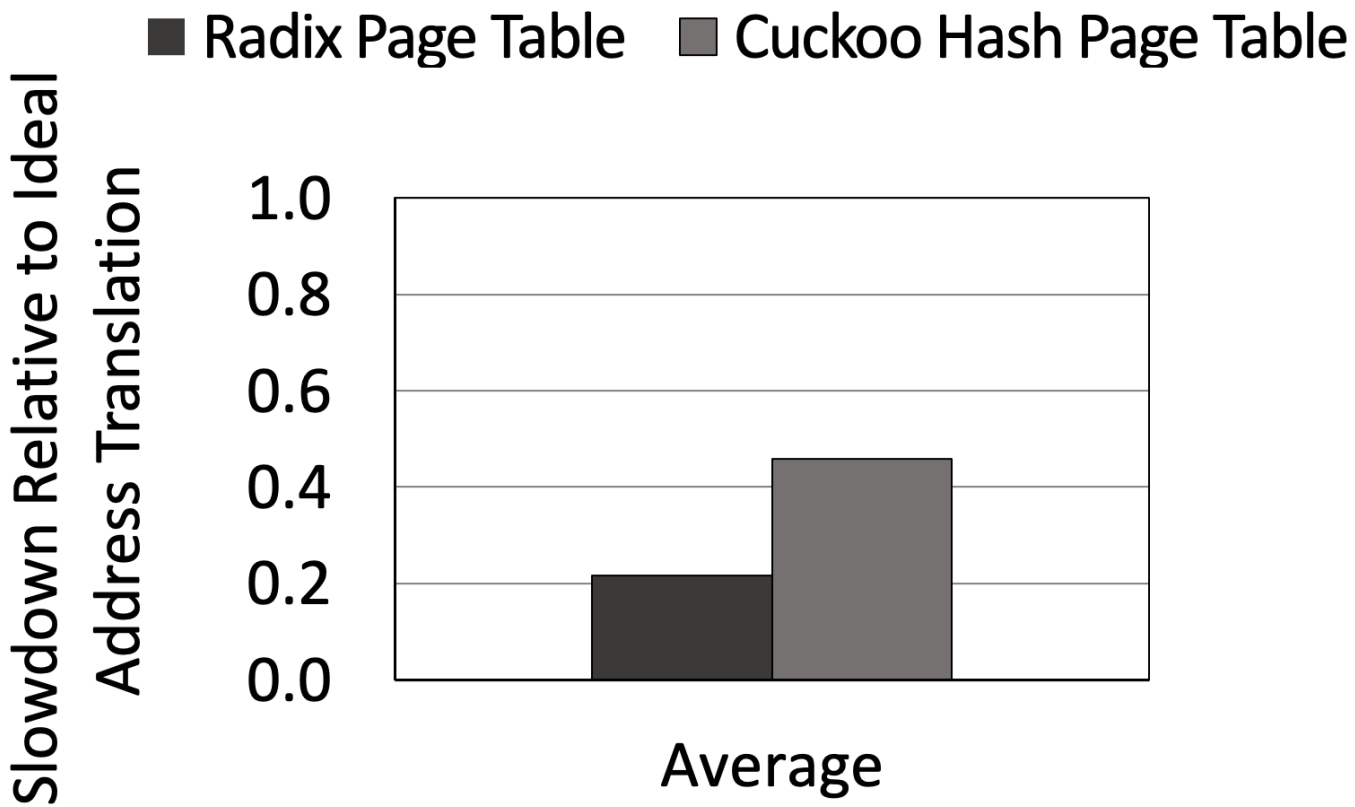

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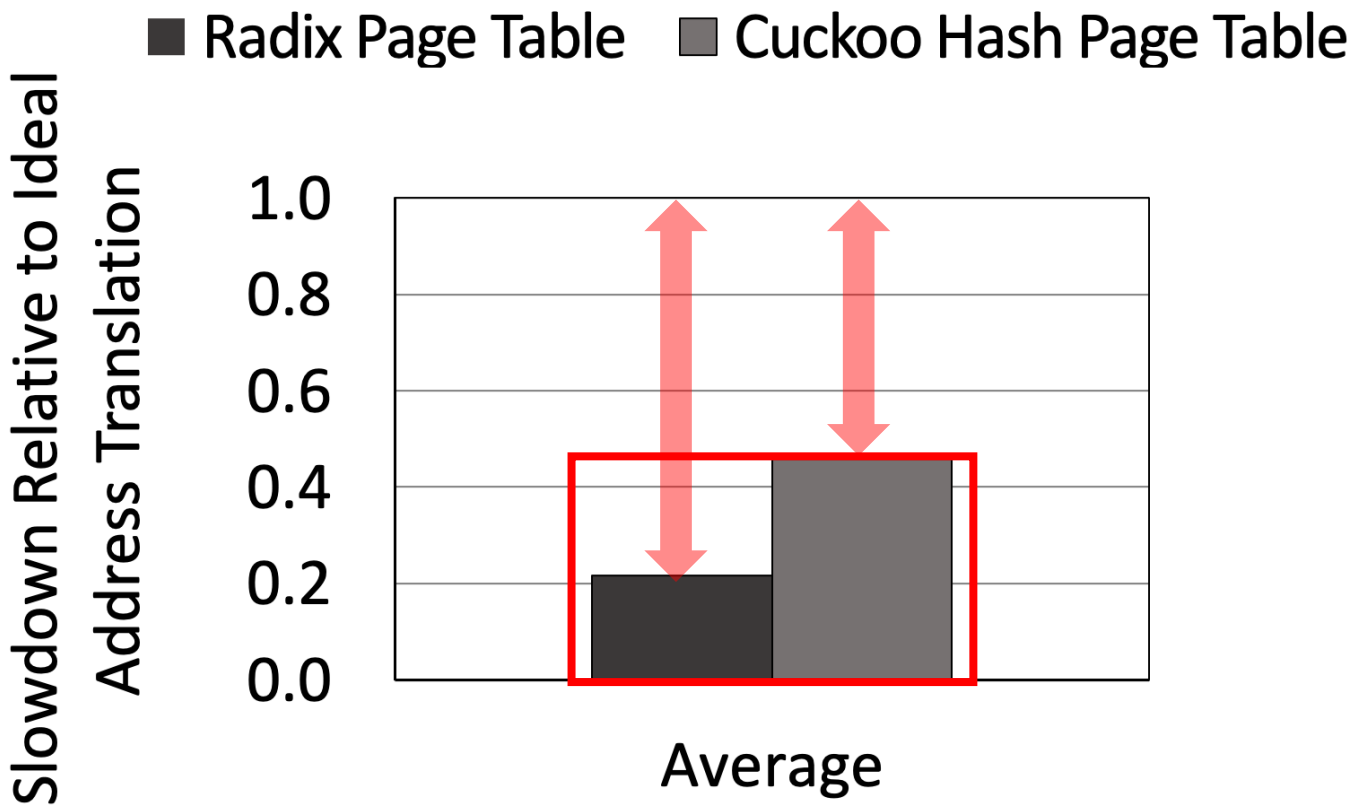


Naïve integration of radix and cuckoo hash page table cause significant slowdown in a PIM based system

Goal

Goal

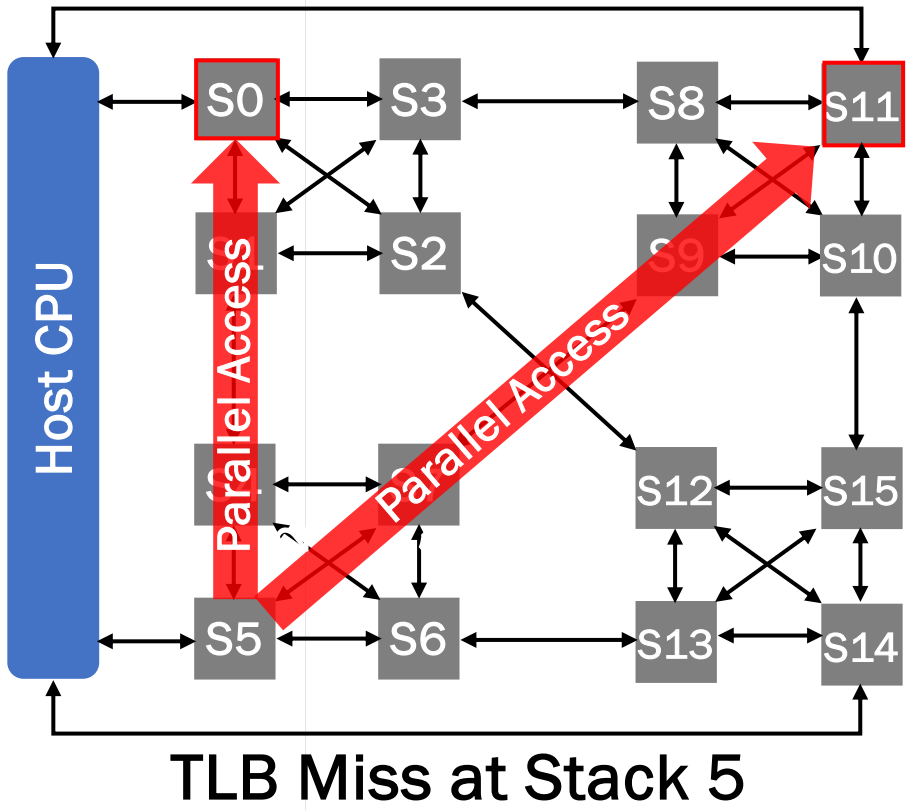
Design an efficient address translation scheme for multi-stack PIM systems

Outline

- Processing-in-Memory Introduction
- Address Translation in PIM Architecture
- Challenges and Key Ideas
- Evaluation
- Conclusion

Challenge: Parallel lookups increase contention

- Parallel lookups in cuckoo hash lead to increased memory network contention



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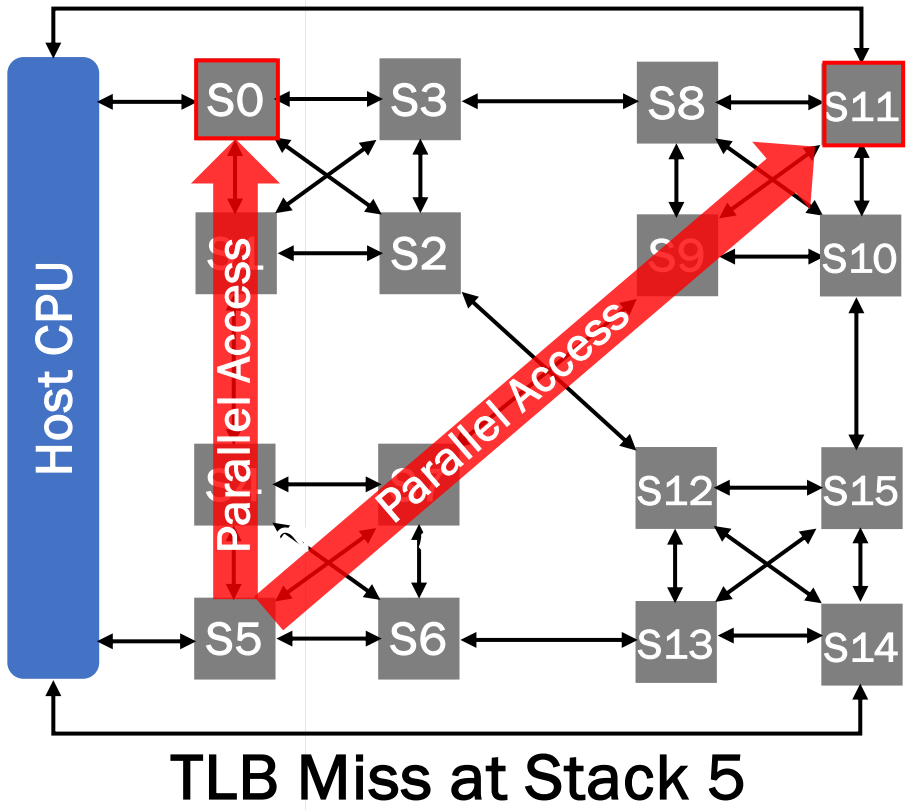

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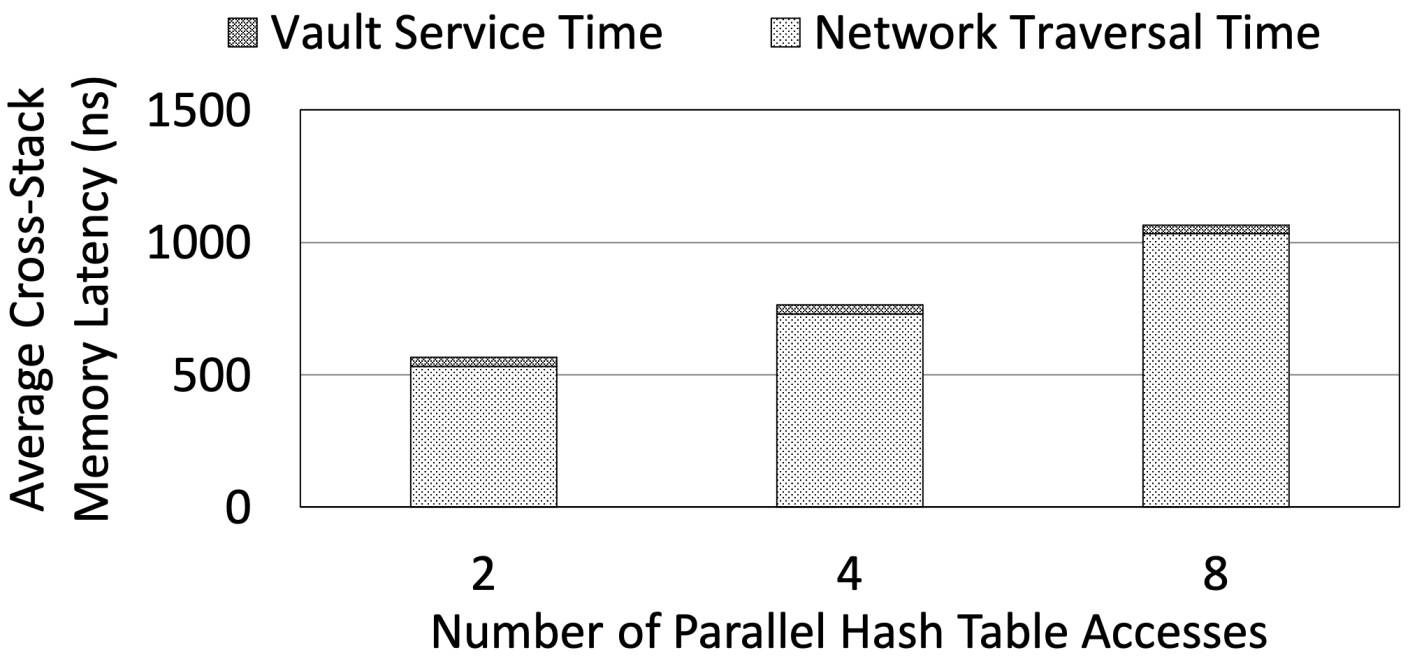

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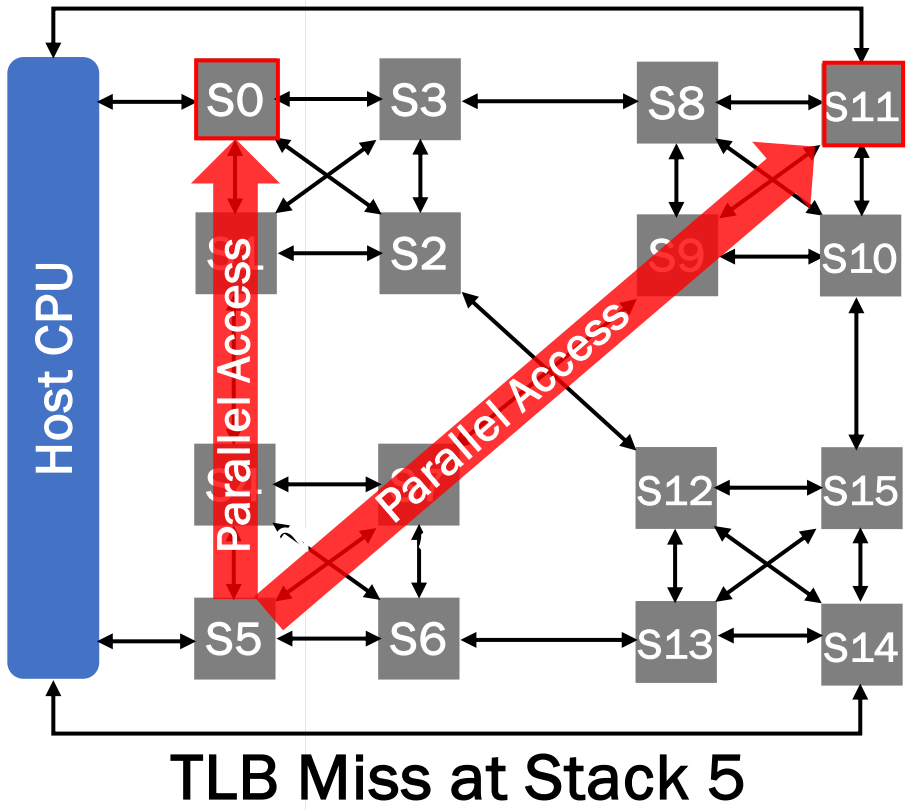

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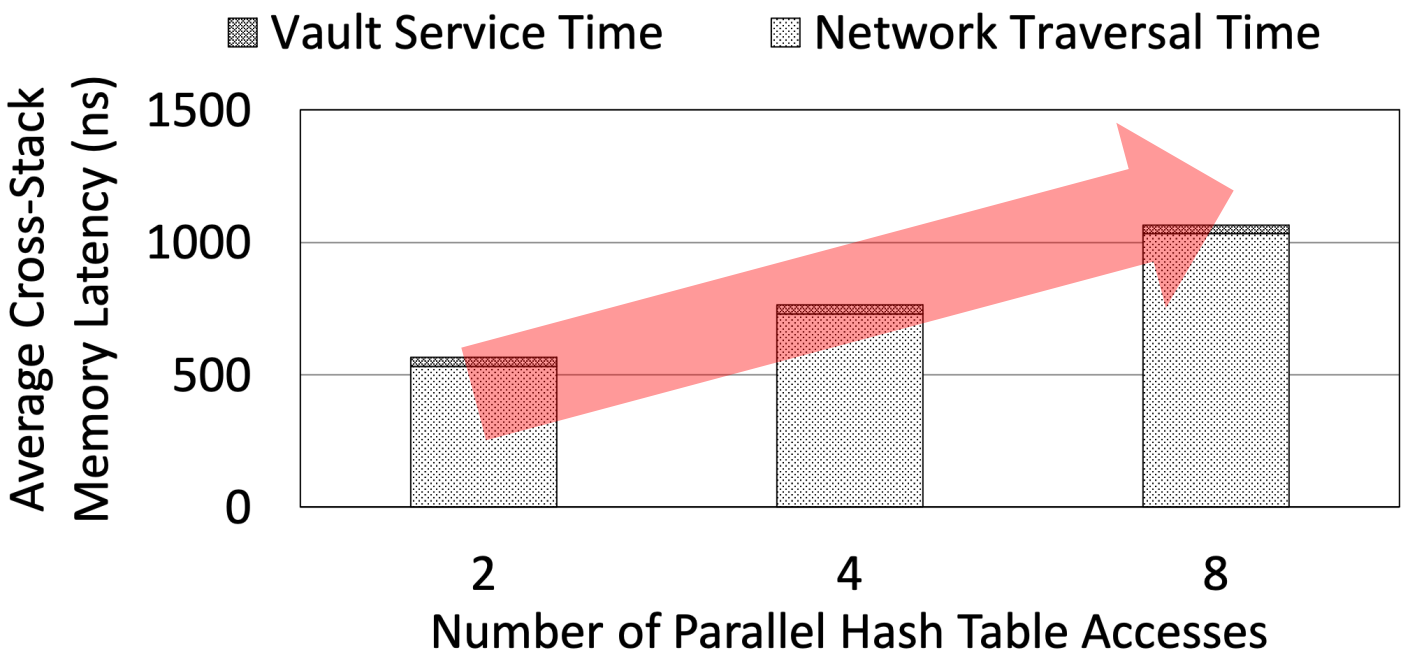

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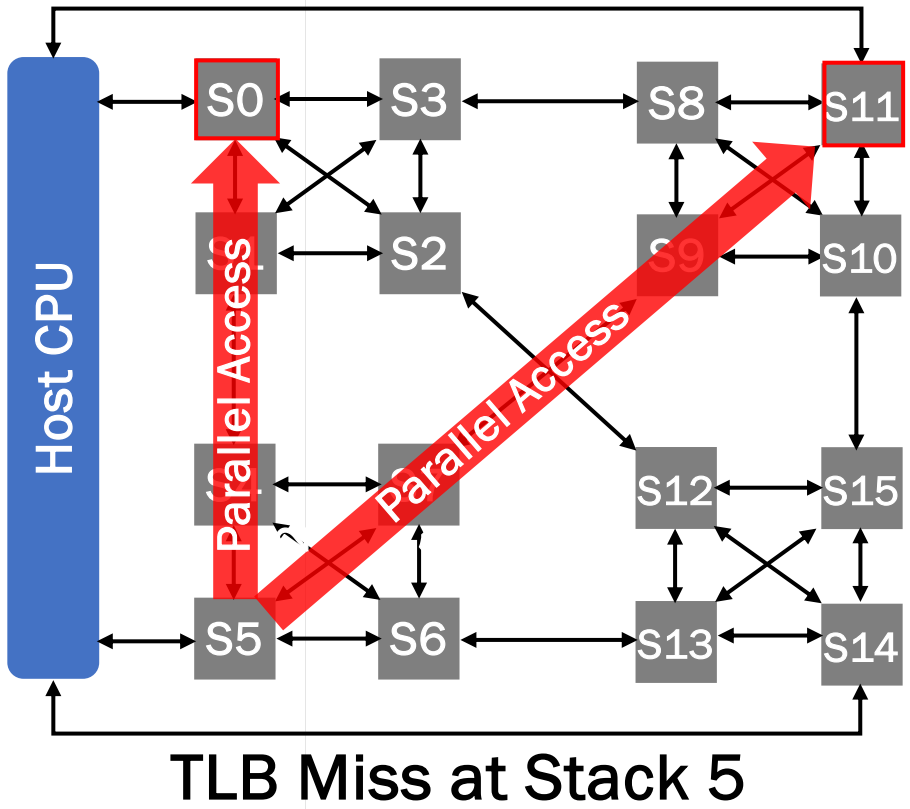

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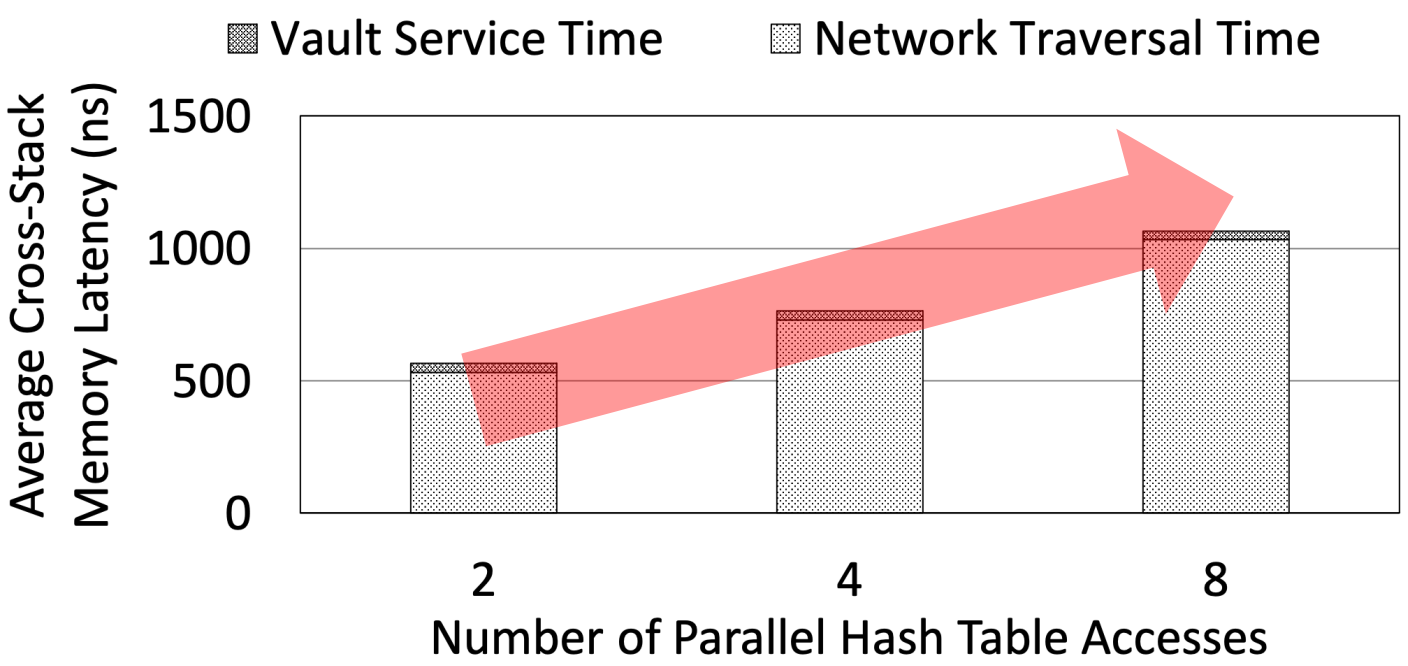
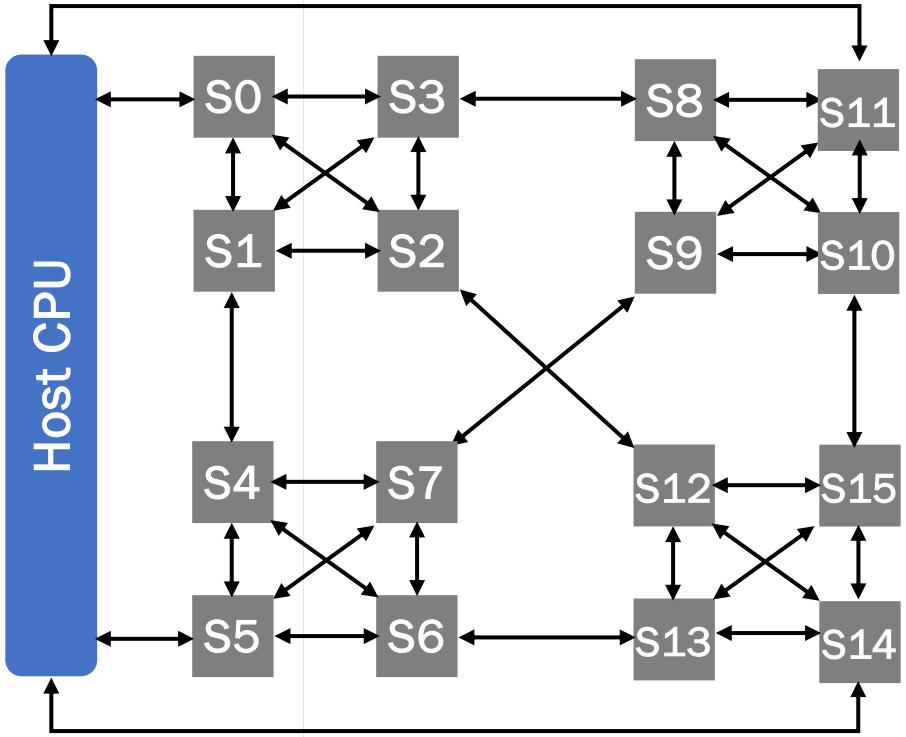


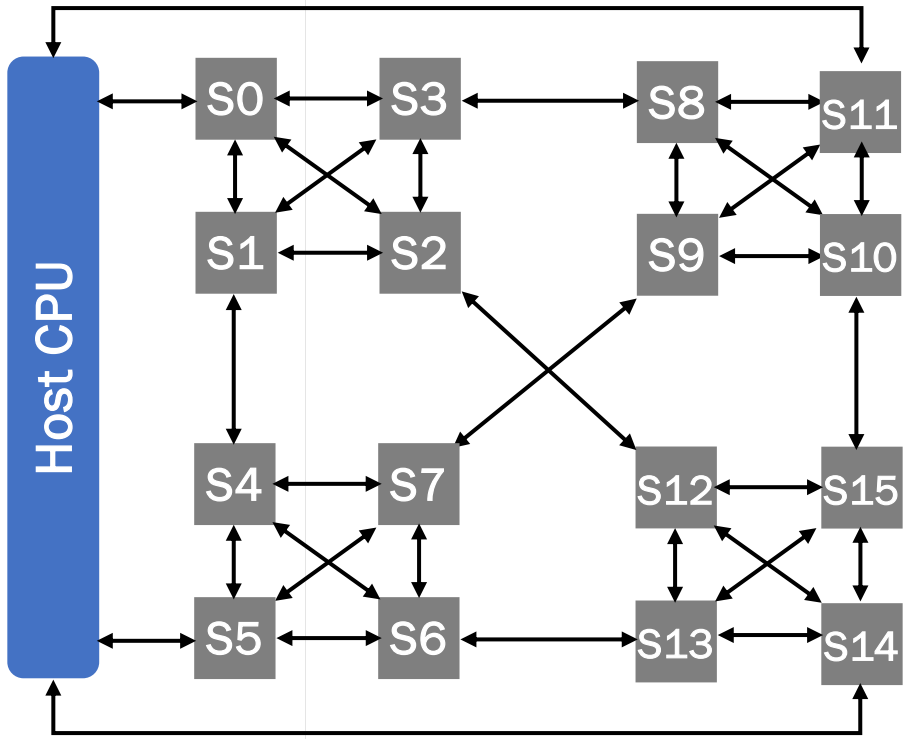
Cross-stack memory access latency increase with parallel accesses

Observation: Massive parallelism inside stack



Observation: Massive parallelism inside stack

- We observe immense intra-stack parallelism for parallel accesses



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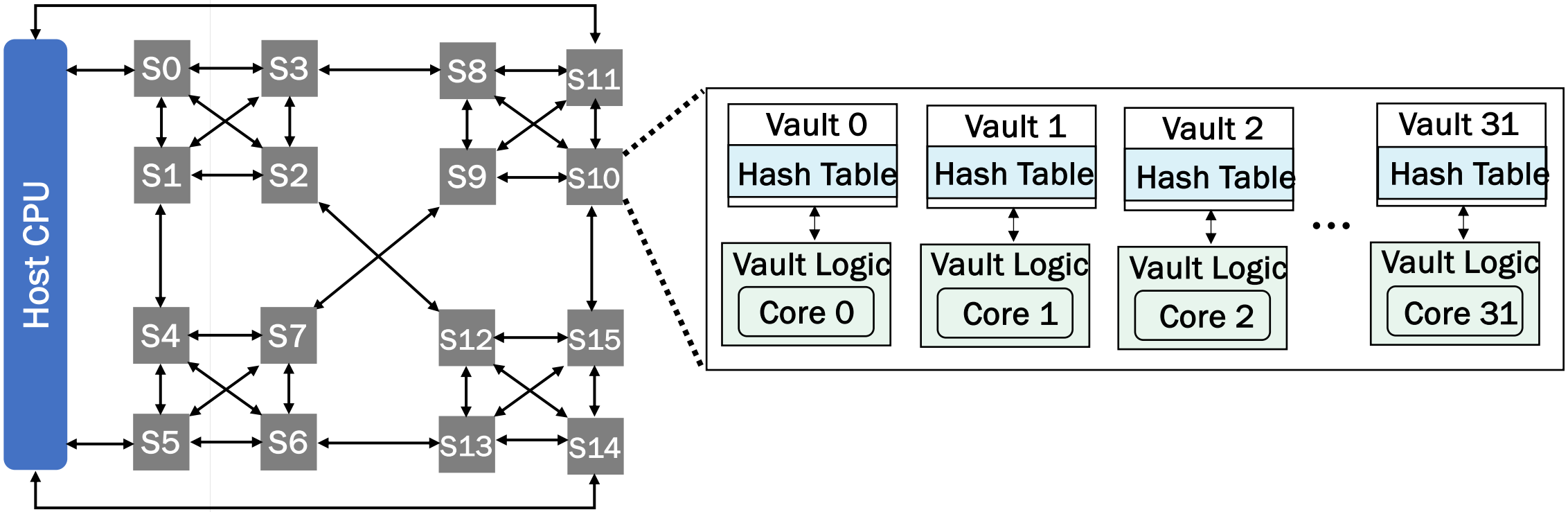

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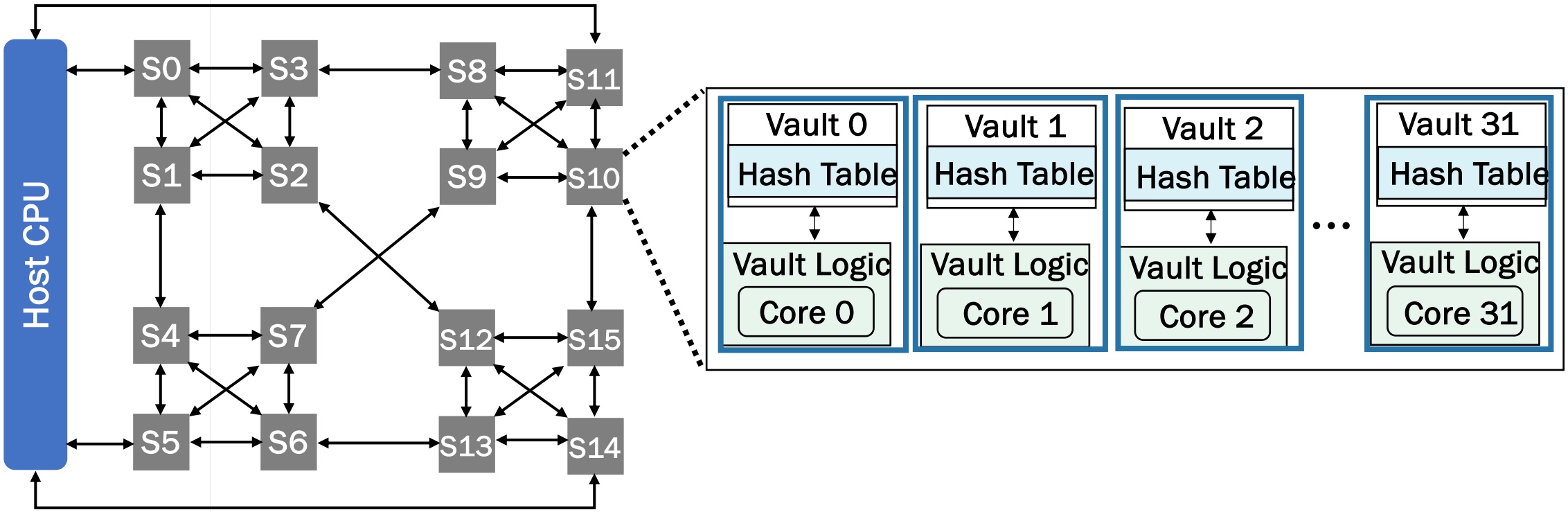

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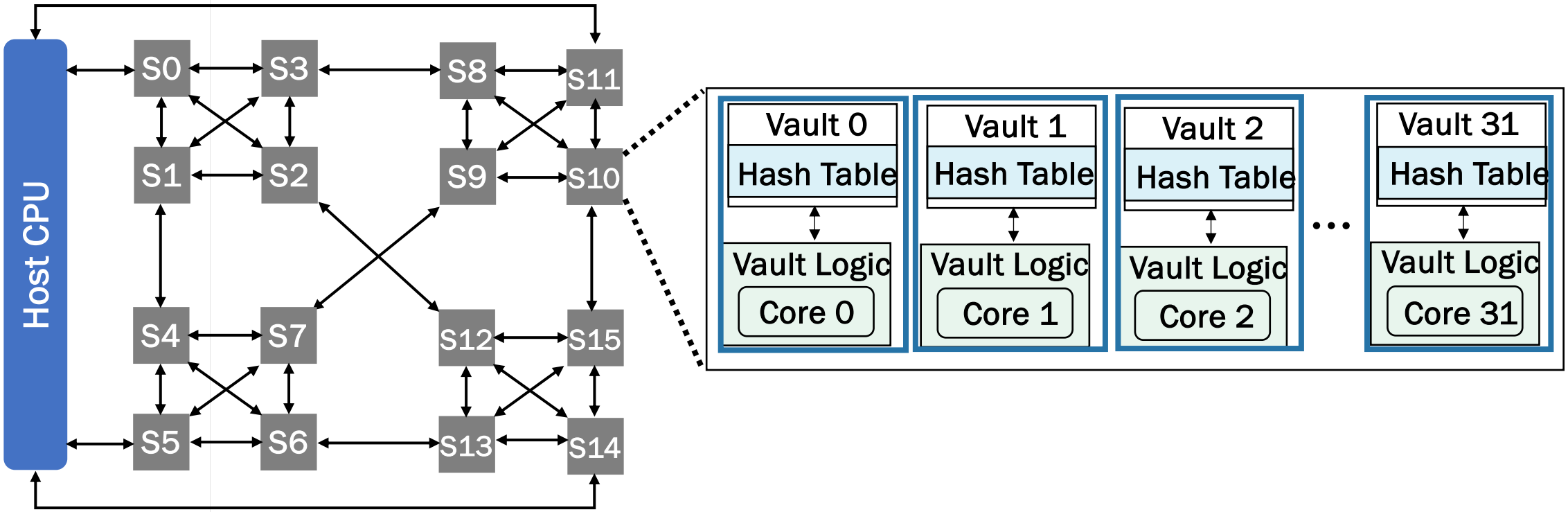

Network traversal can be avoided if parallel accesses are generated within the same stack and across different vaults

Key Idea: Network-contention-aware hash

- Parallel lookups generated within the stack avoid costly cross-stack page table walks

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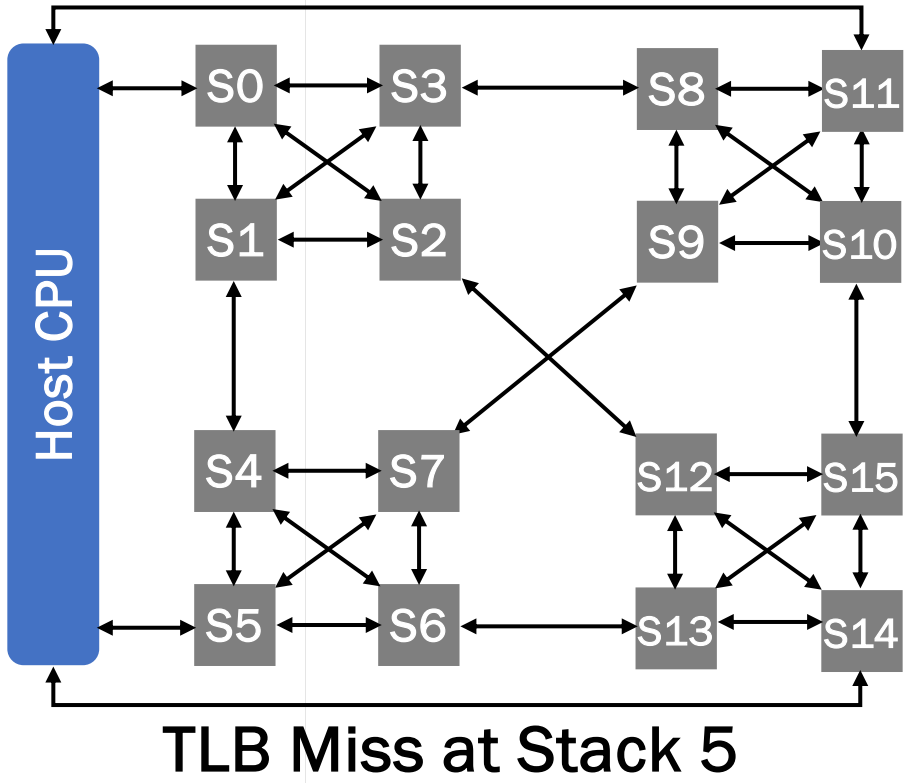

TLB Miss at Stack 5

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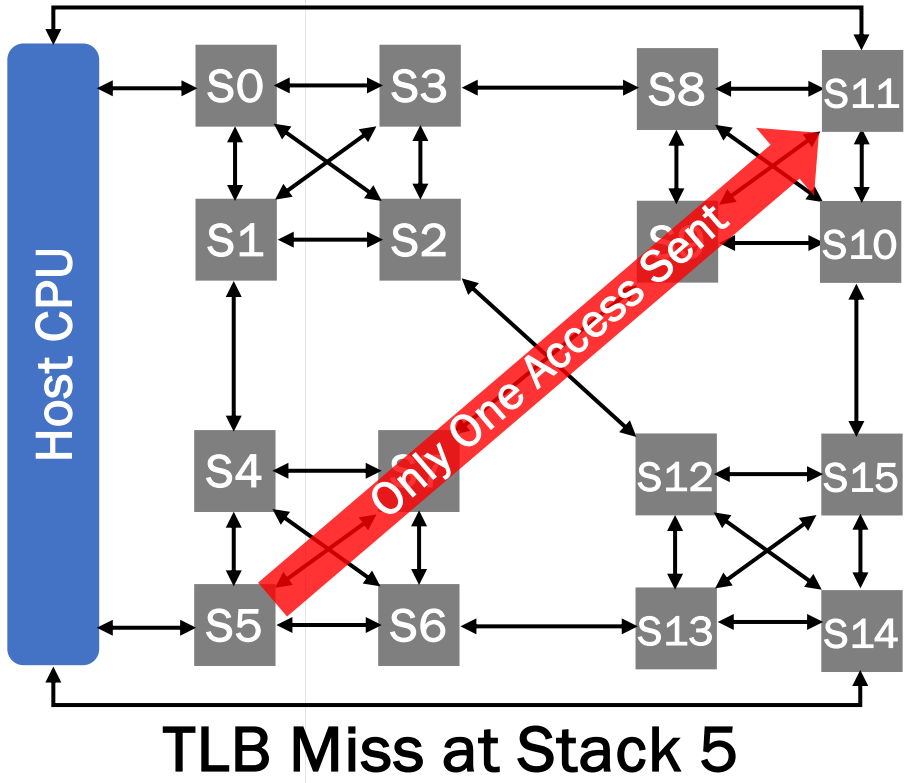

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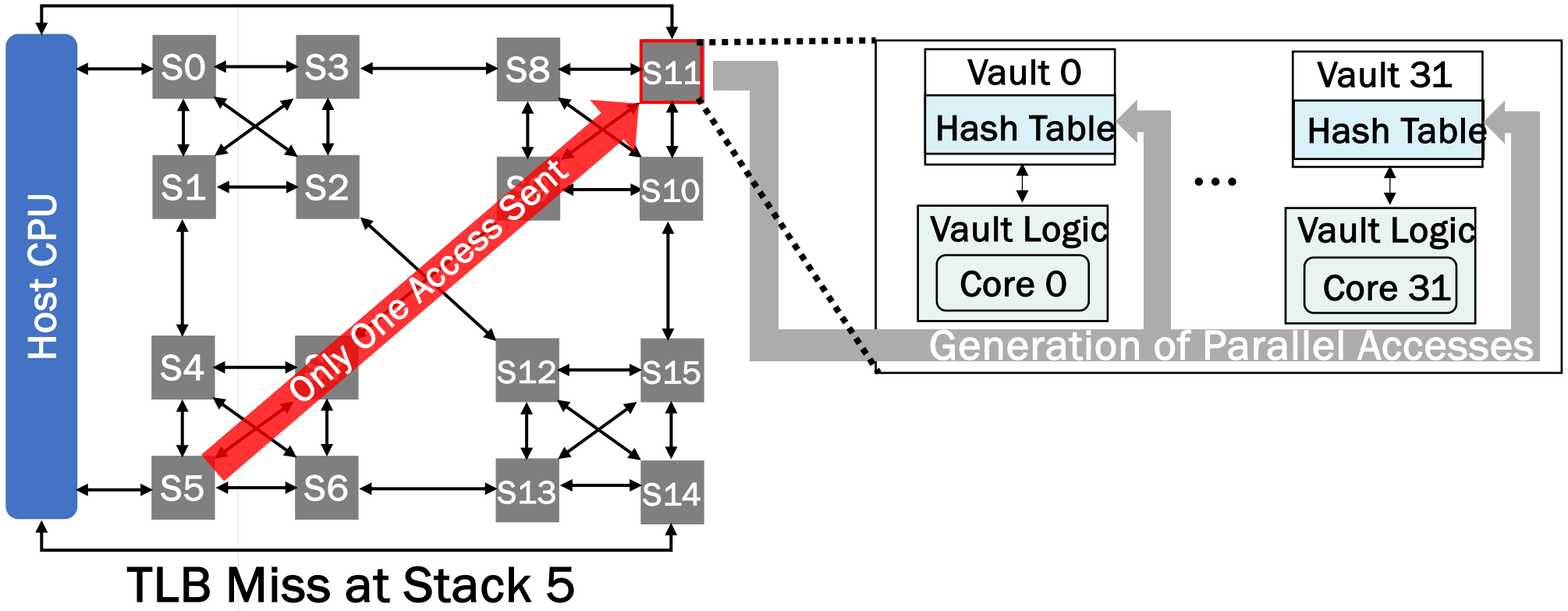

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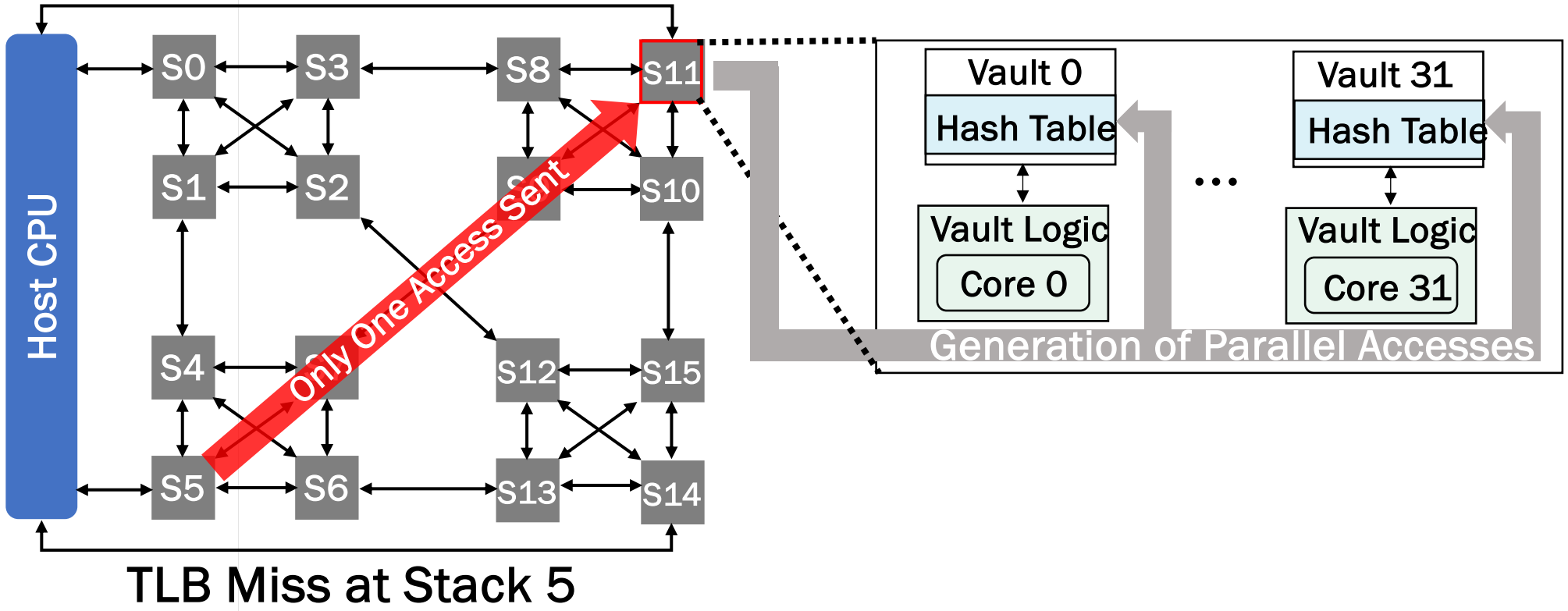
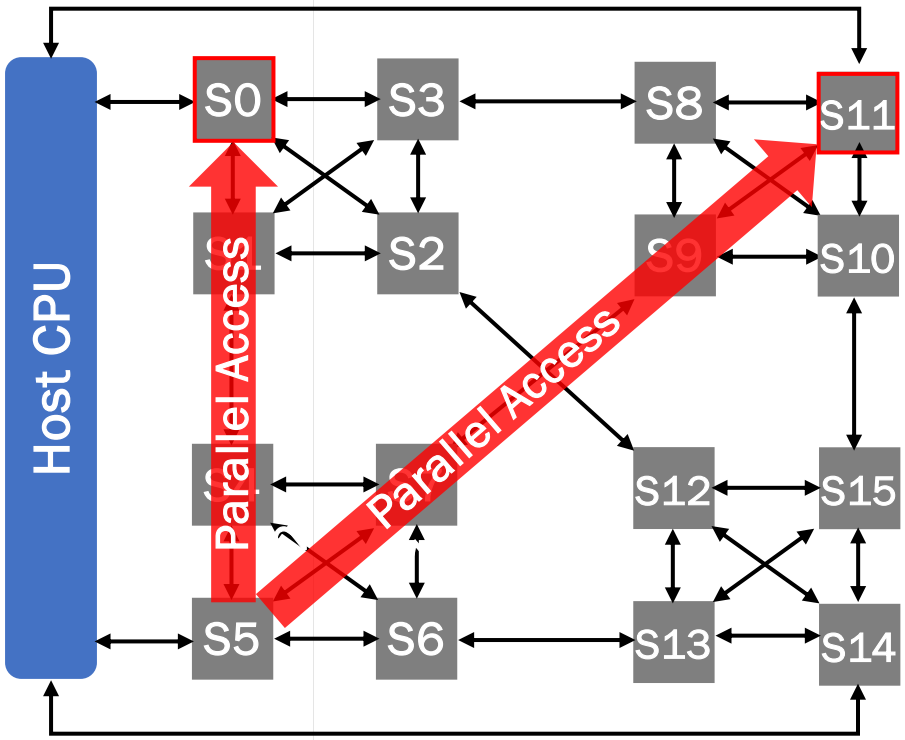


Network-contention-aware hash spawn parallel accesses within the same stack to avoid network traversal

Benefit and Opportunity



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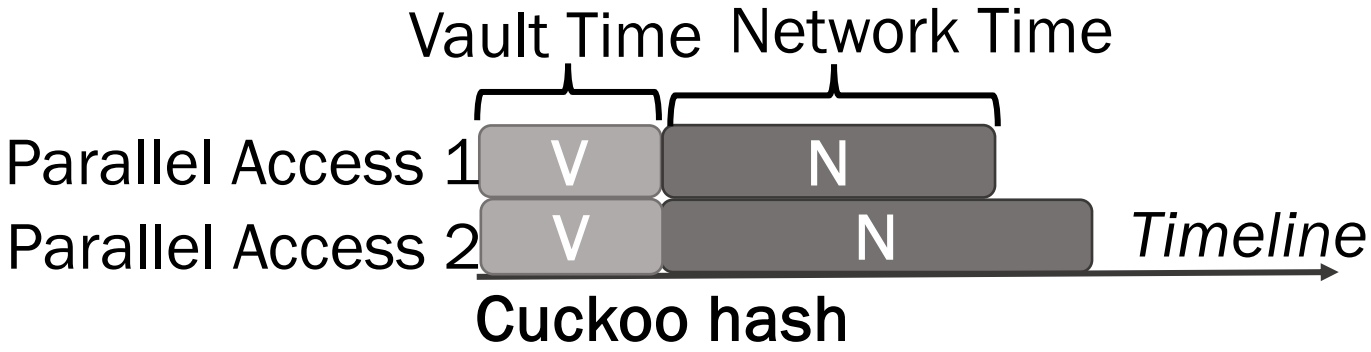
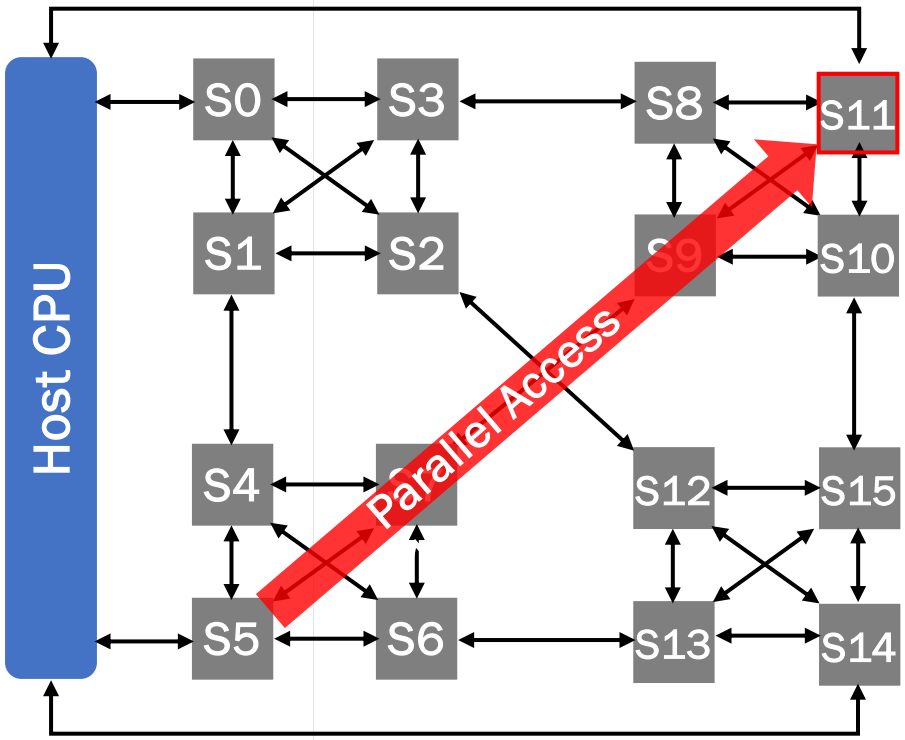


Cuckoo hash

Benefit and Opportunity



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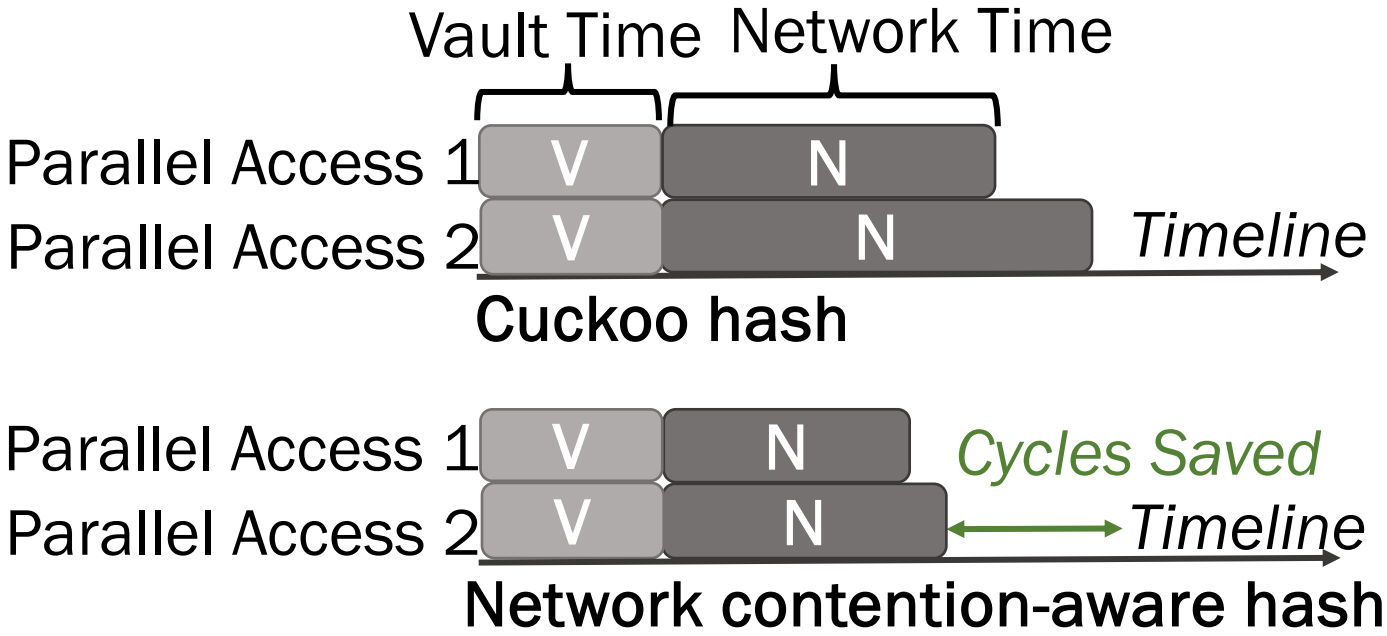

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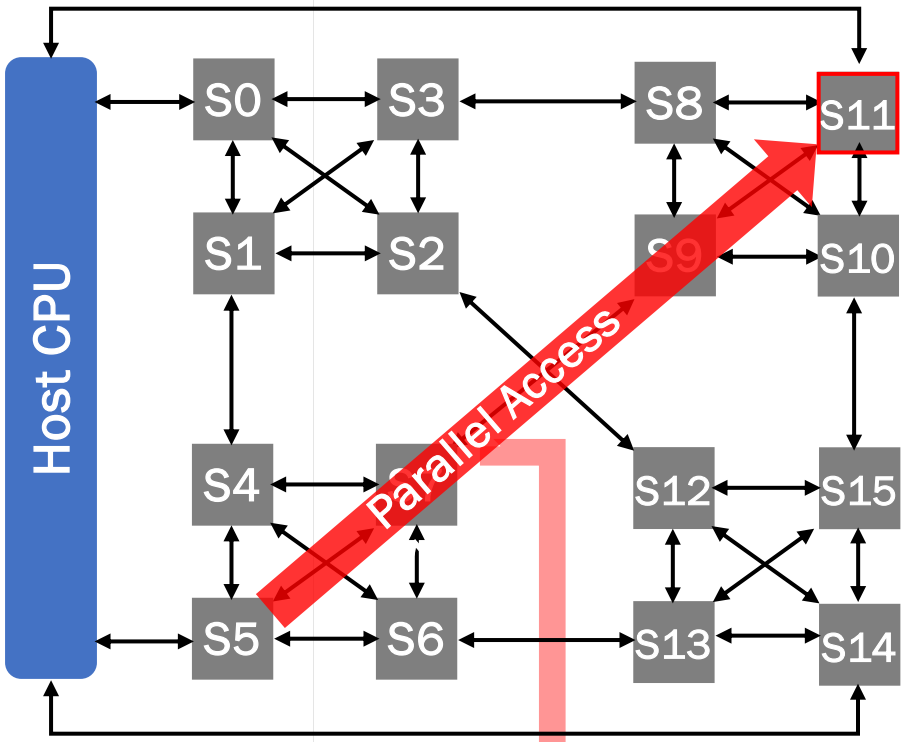
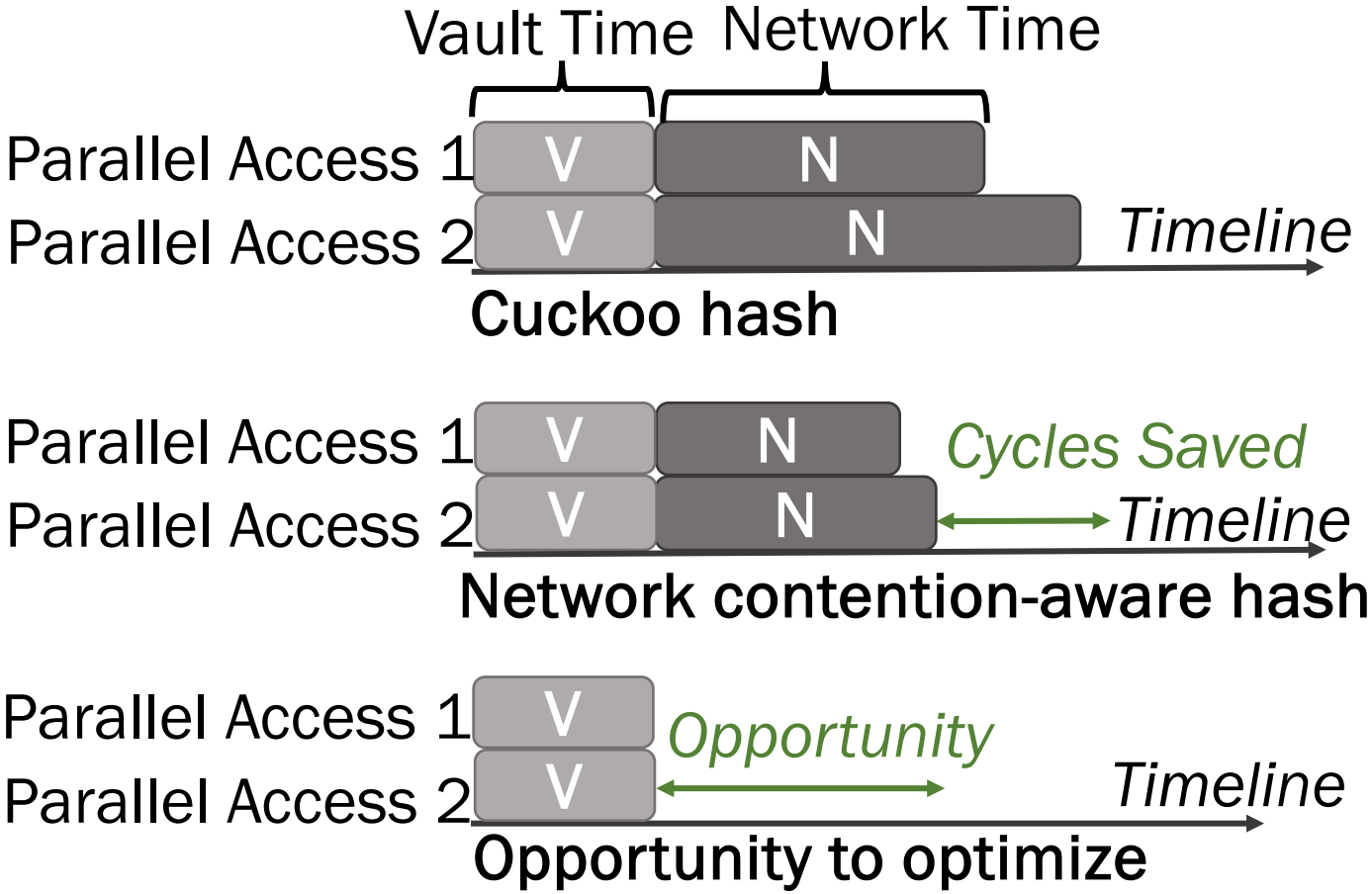


Can we get rid of this cross-stack access?



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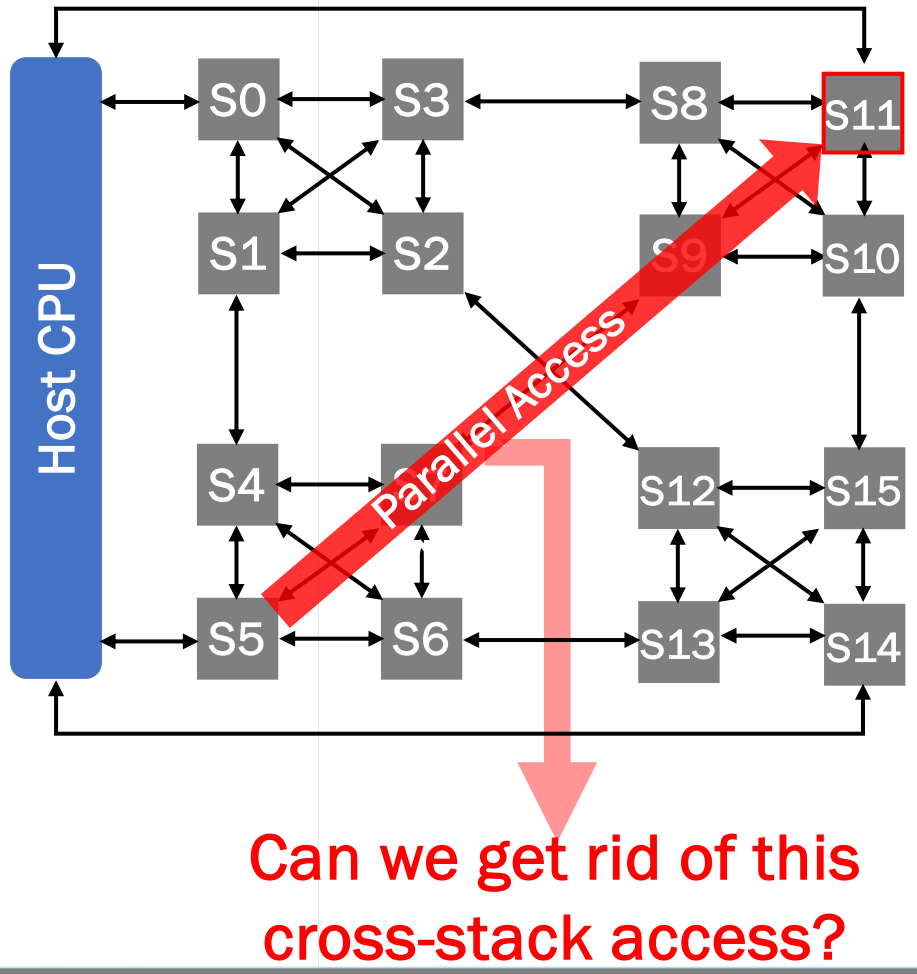
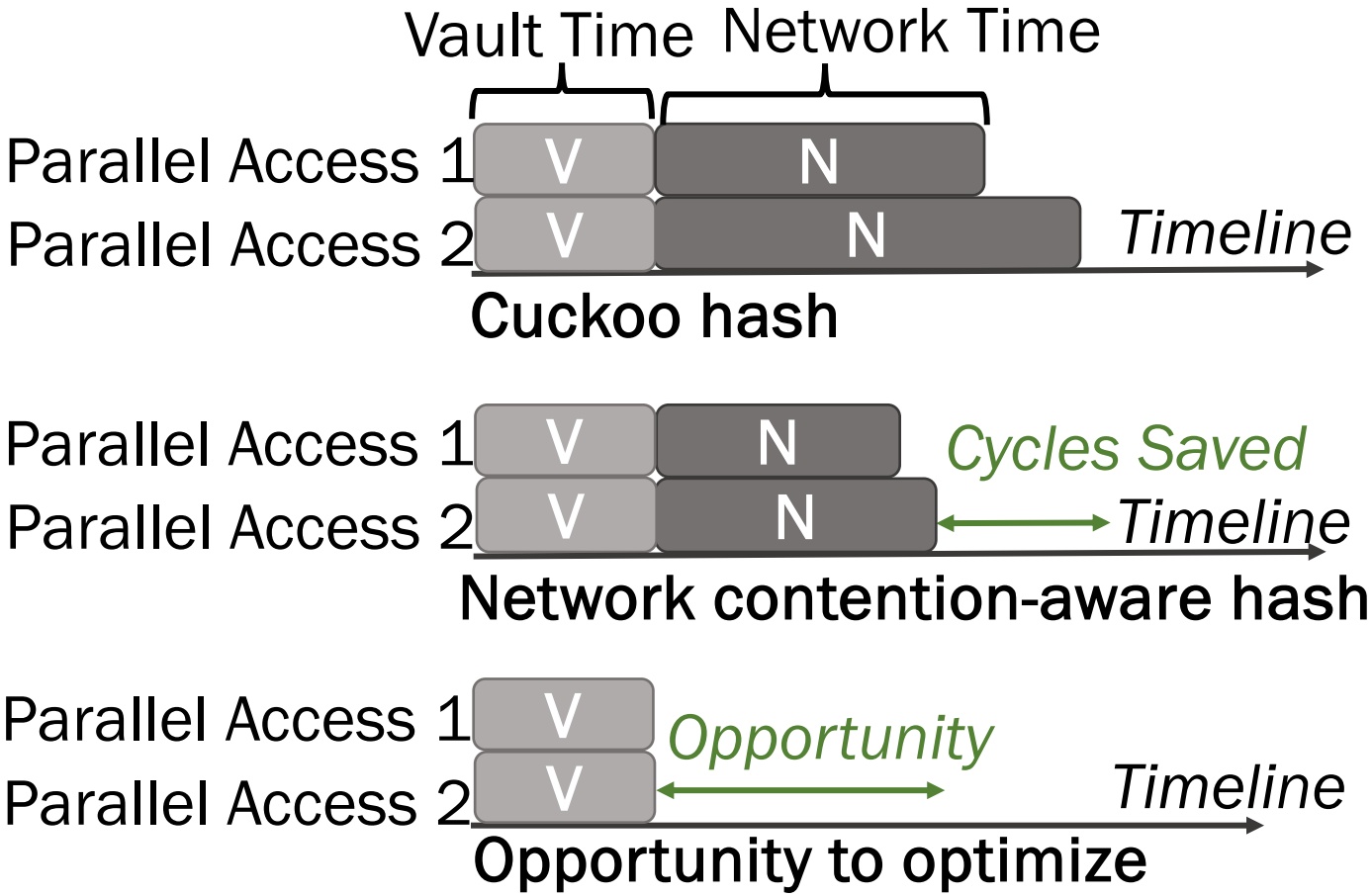




Is there any way to eliminate the overhead of cross-stack access?

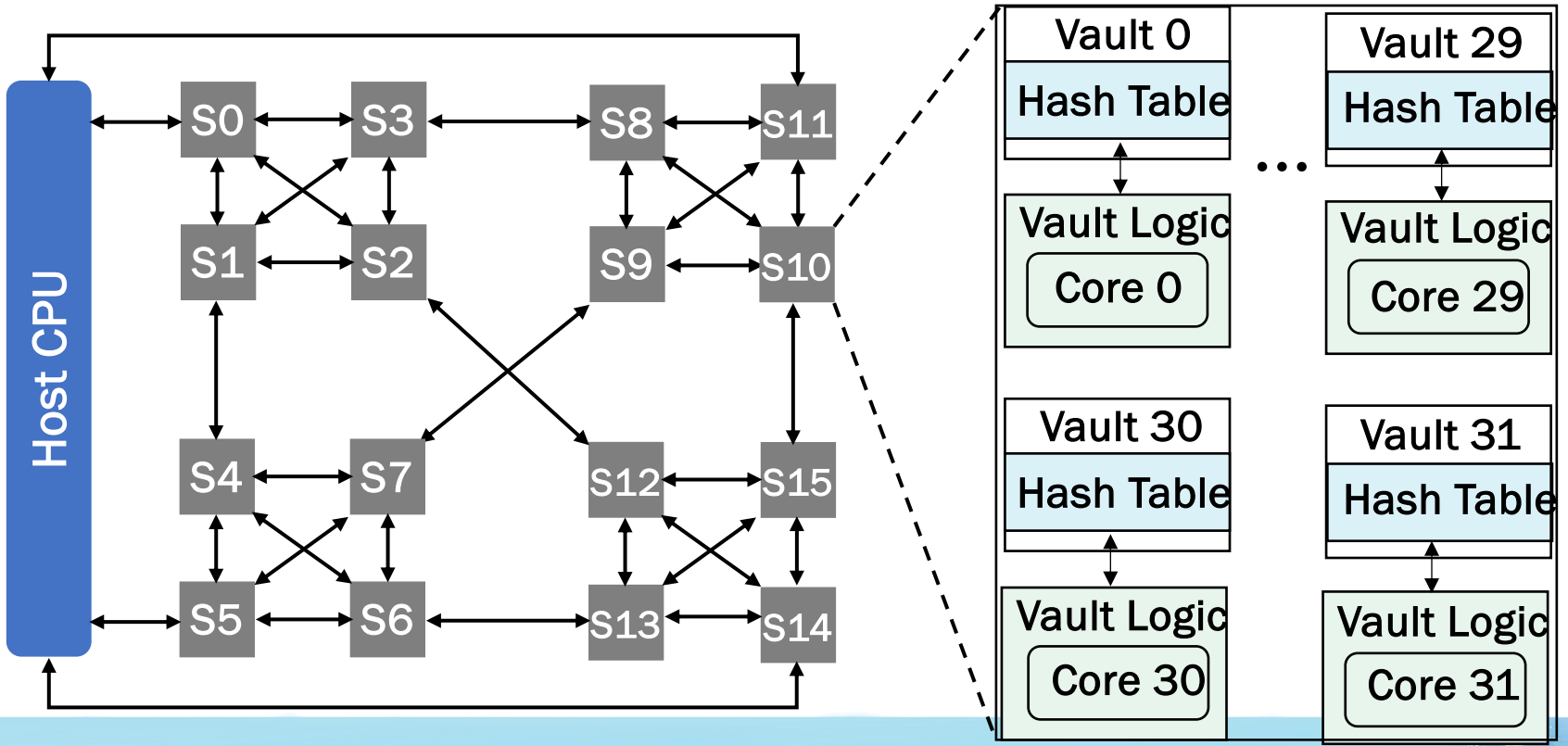
Observation: PIM programs feature high parallelism

- PIM suitable programs manifest as independent threads that can be assigned to different cores and execute in parallel

```
#pragma omp parallel for
for(...)
{

        ...

}
```



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Iterations are evenly distributed across the PIM stacks for computation

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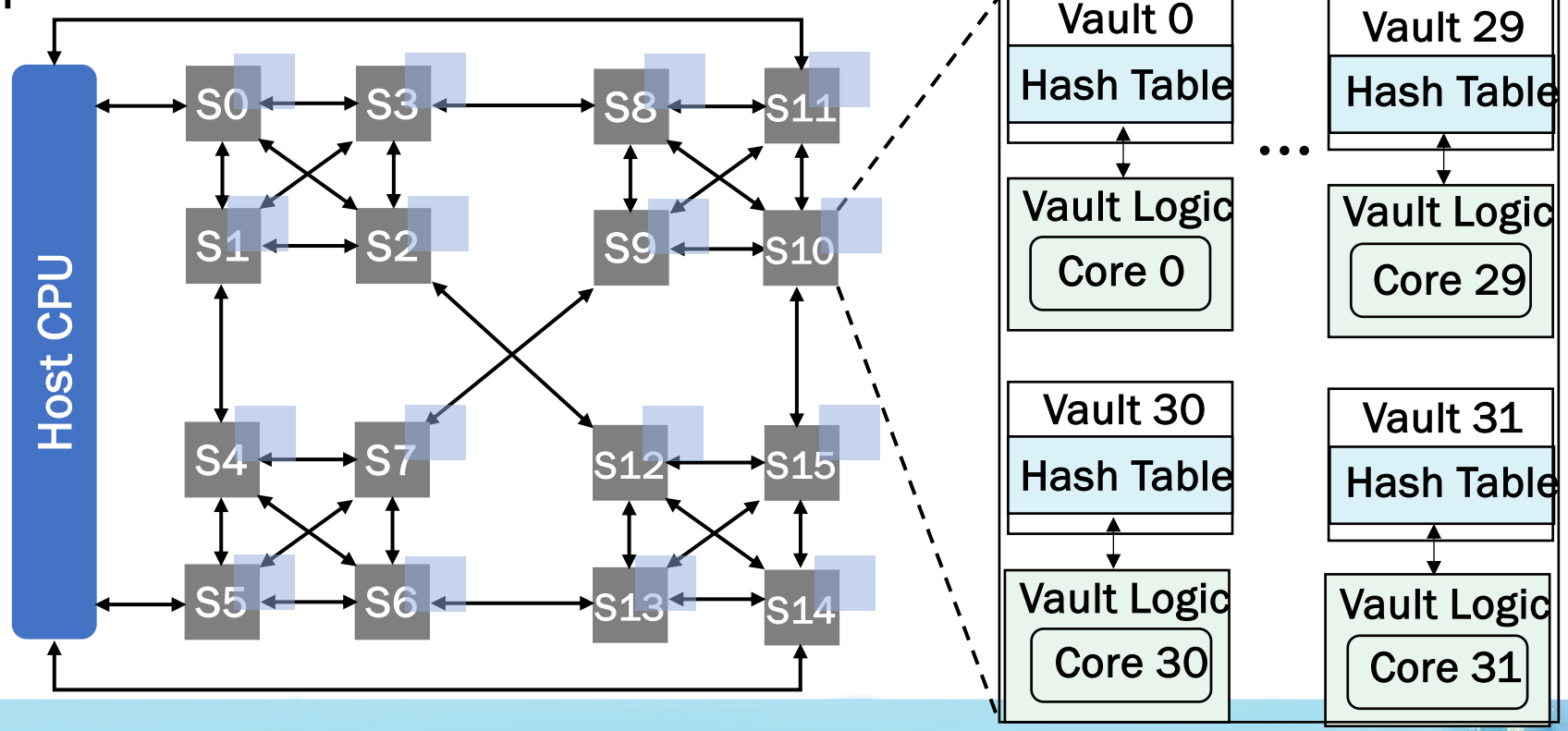

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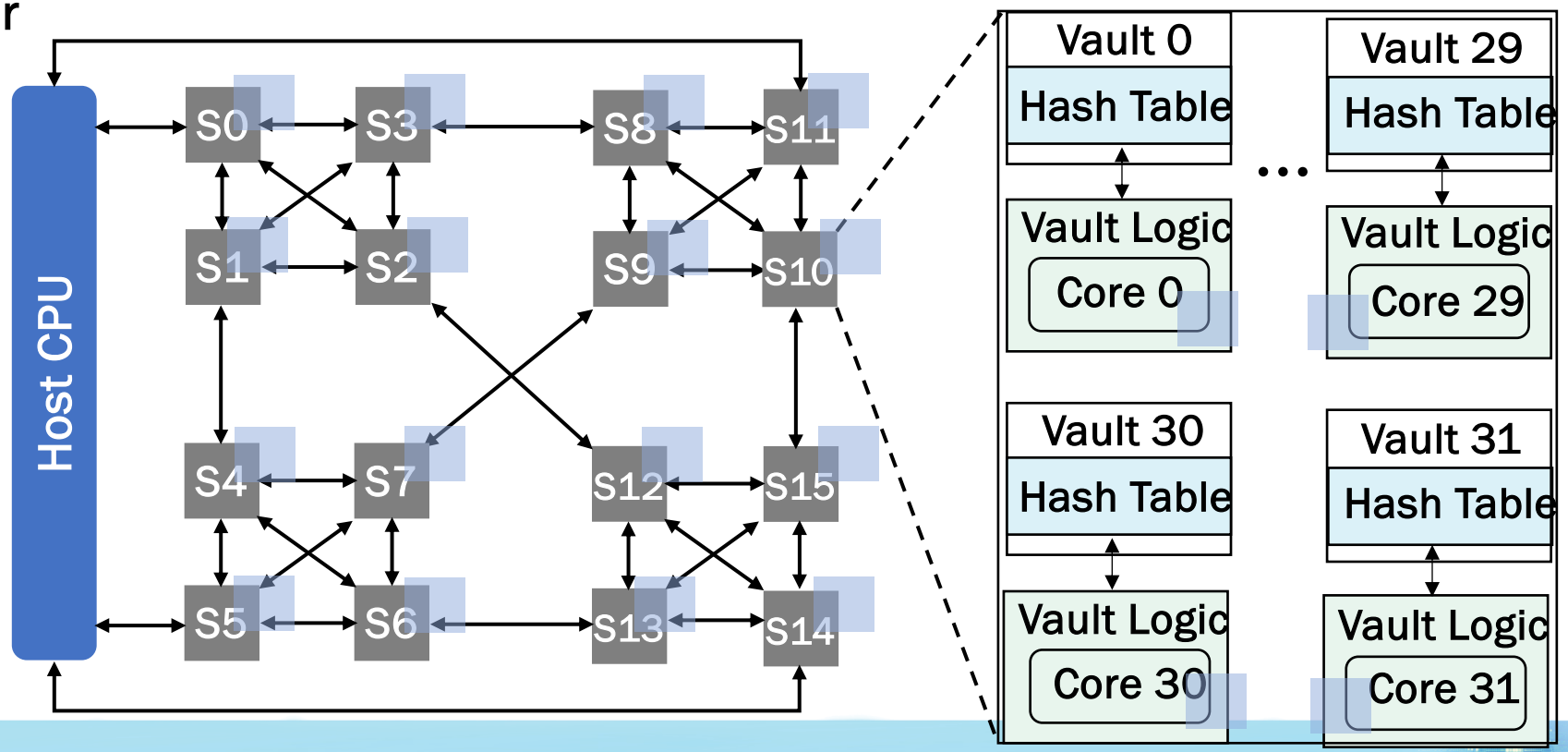
for(...)
{

    ...

}
```

Iterations are further distributed across the vaults within a stack



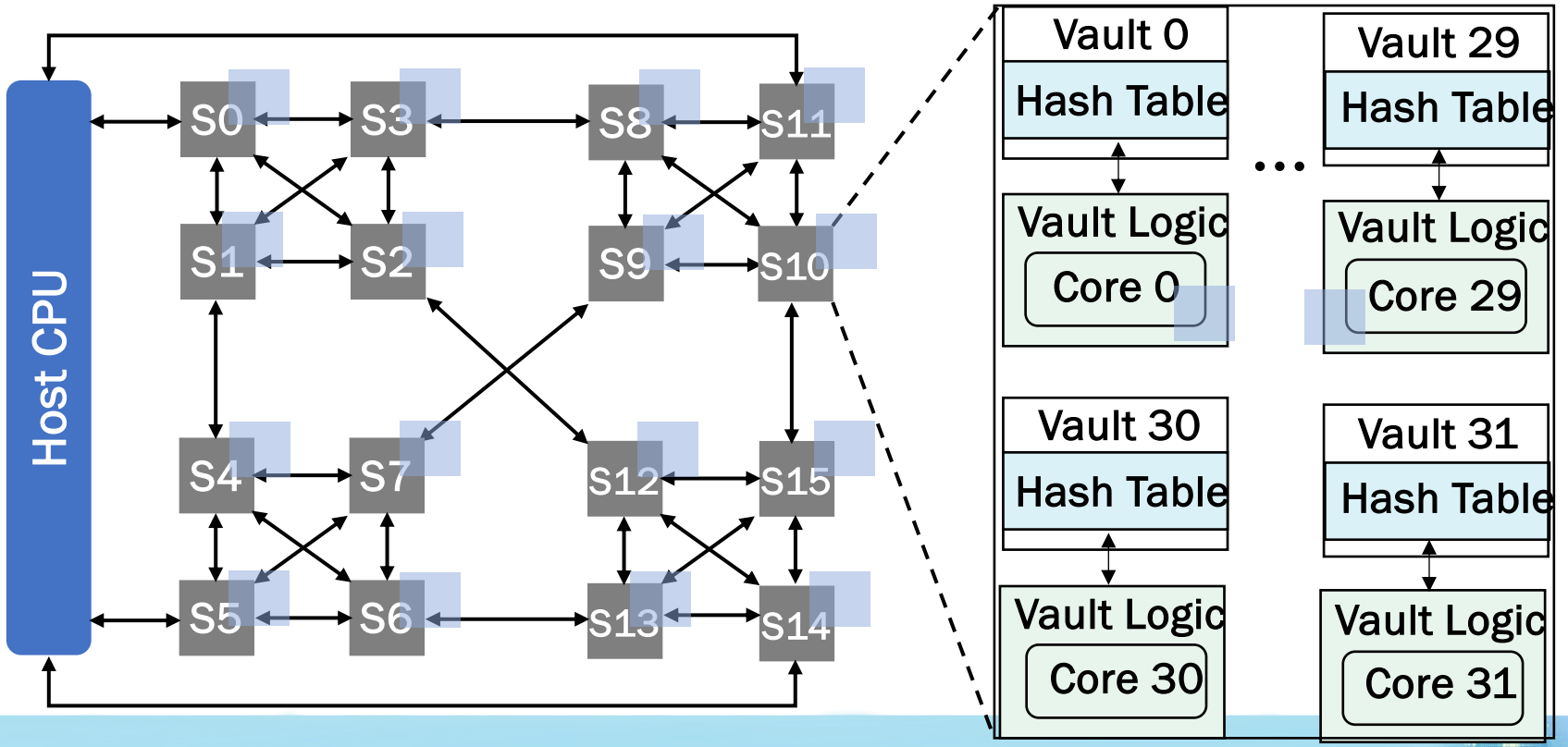
Observation: Fewer cores cause minimal slowdown

- Reduction in throughput has minimal impact on performance

```
#pragma omp parallel for
for(...)
{

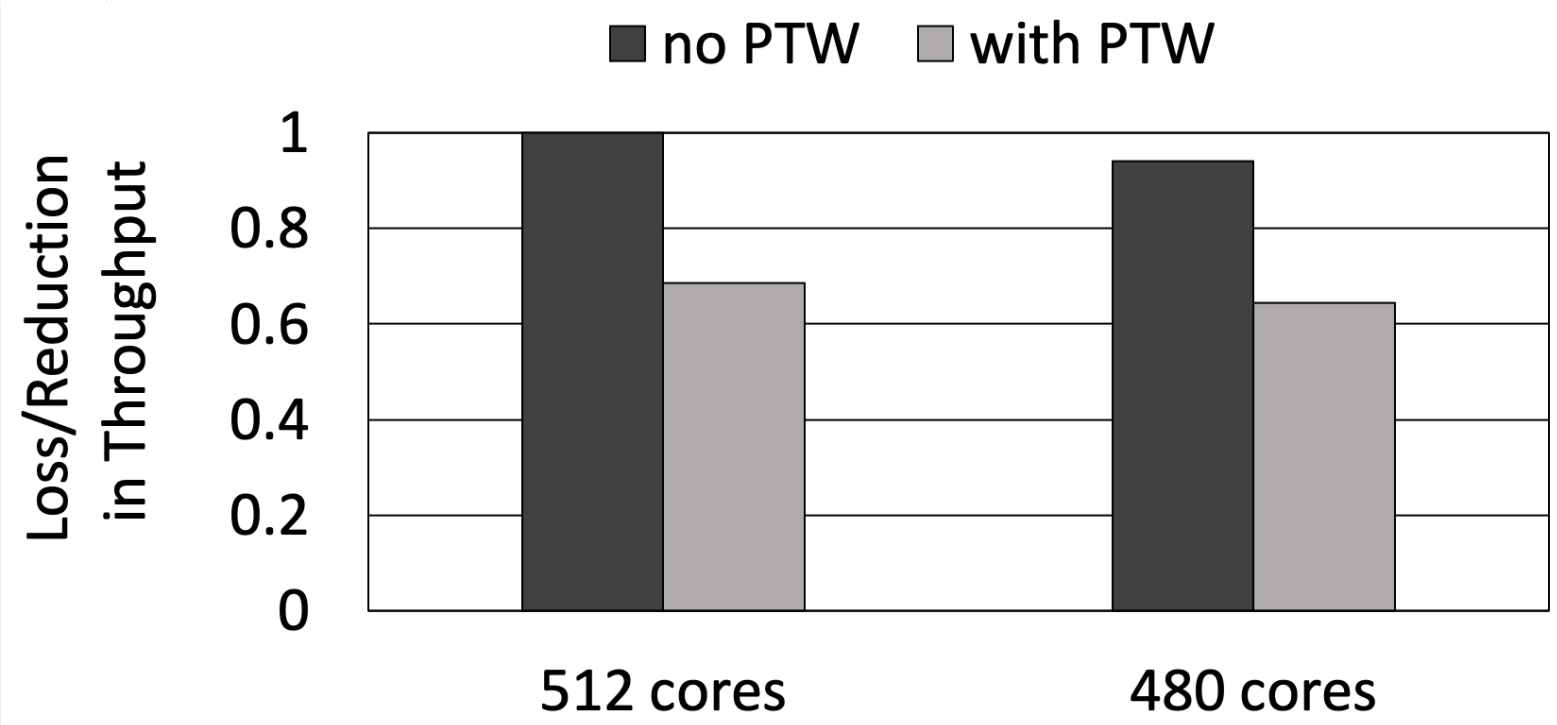
      ...

}
```



Page table walk overhead

- Observation: PIM suitable programs feature high parallelism and manifest as independent loops that can be assigned to different cores and be executed in parallel
- Observation: Reduction in throughput has minimal impact on performance



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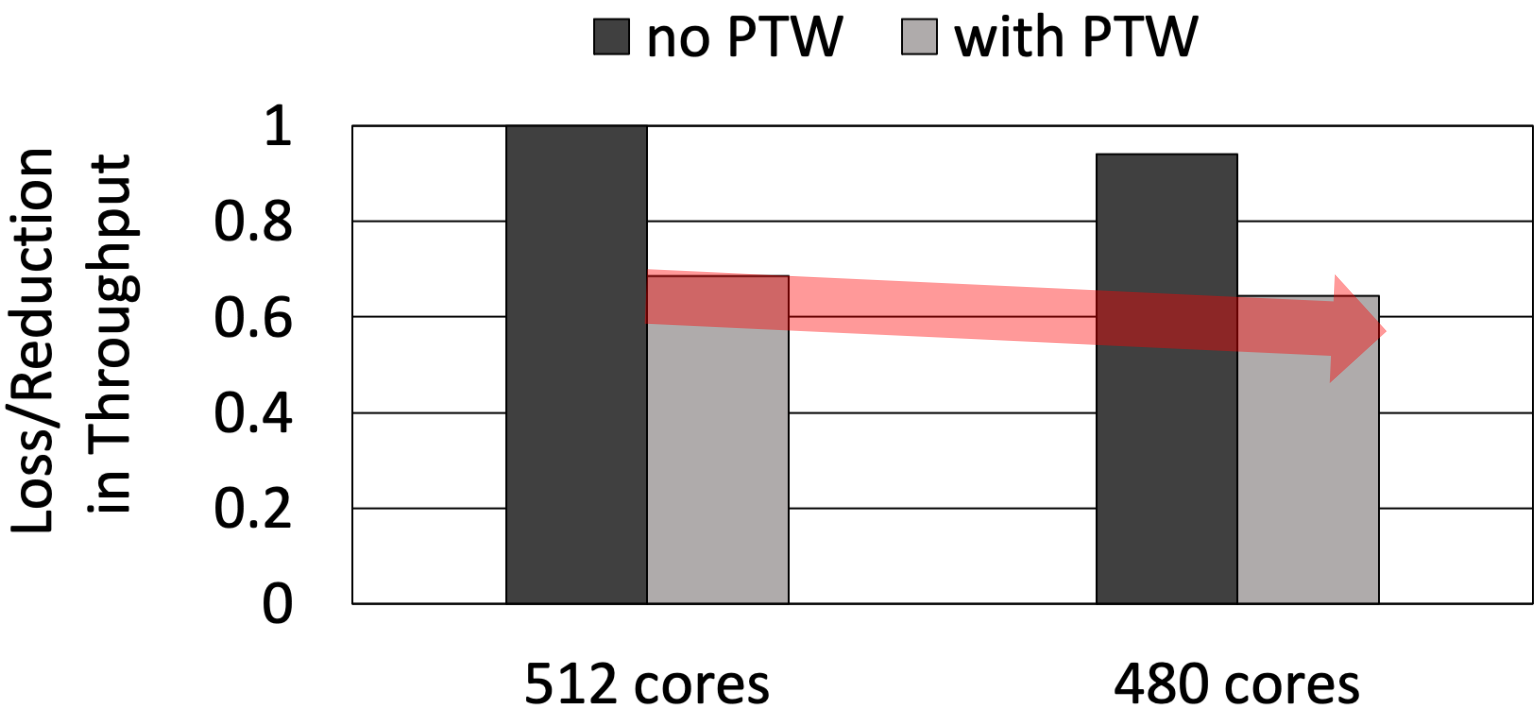

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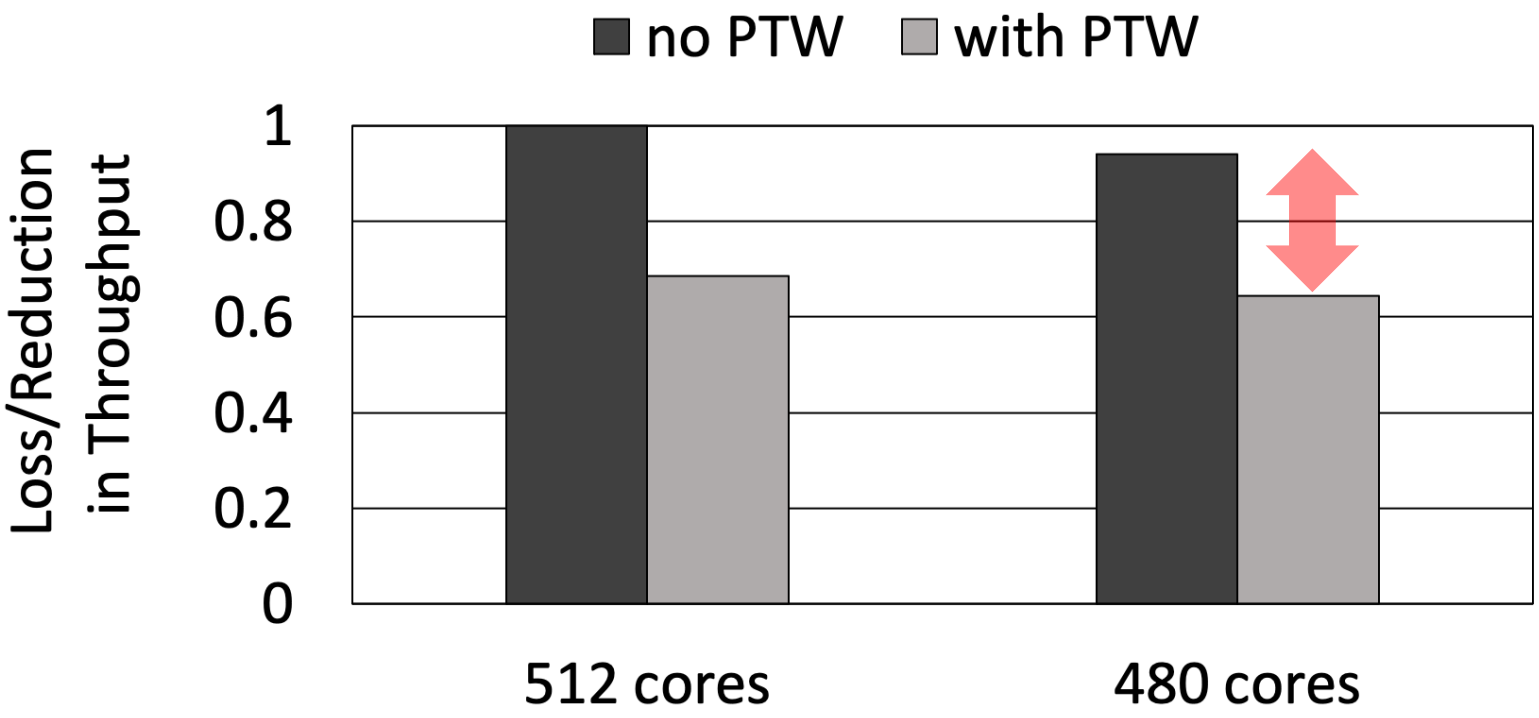


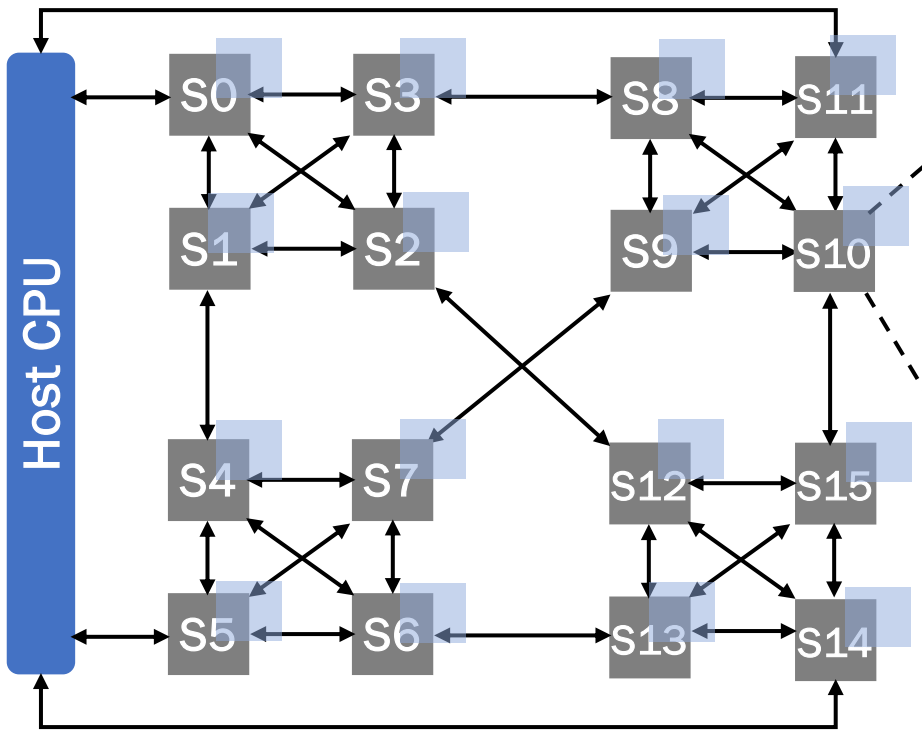
Performance is bottlenecked by the page table walk overhead

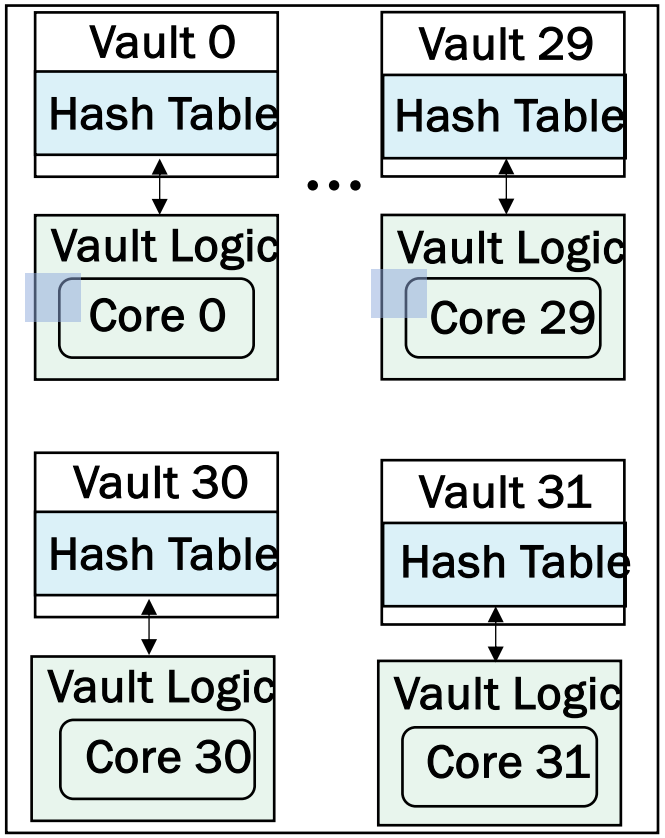
Key Idea: Pre-translation of page table walks

Utilize some throughput to pre-translate page table walks

```
#pragma omp parallel for
for(...)
{
    Code for main cores
    x=array1[i]
    sum+=x

}
for(...)
{
  Code for pre-translation cores
    x=array1[i]
    sum+=x
}
```

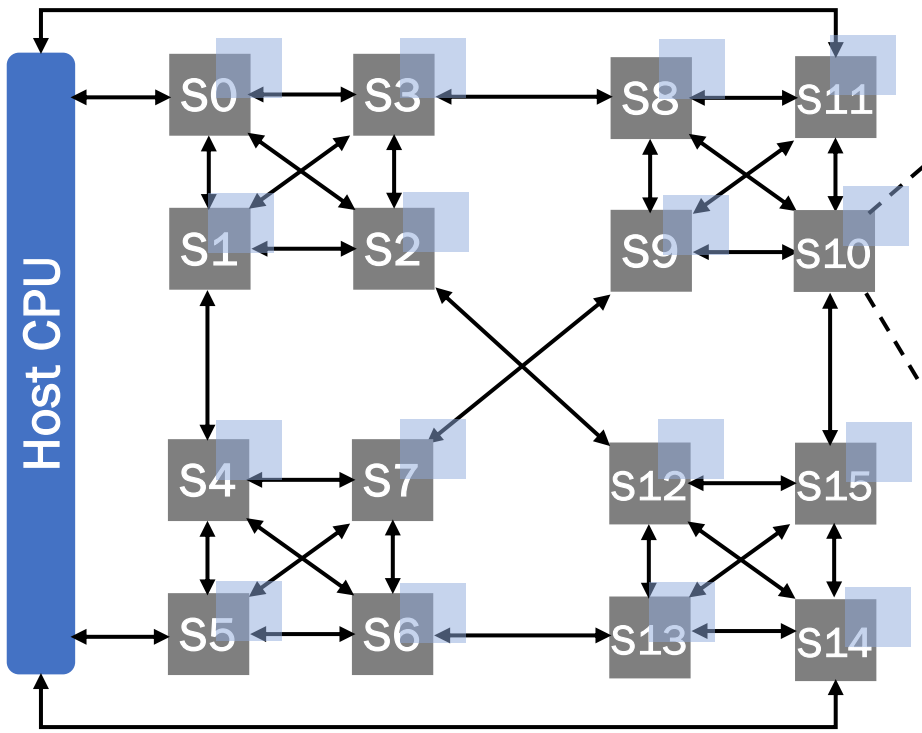


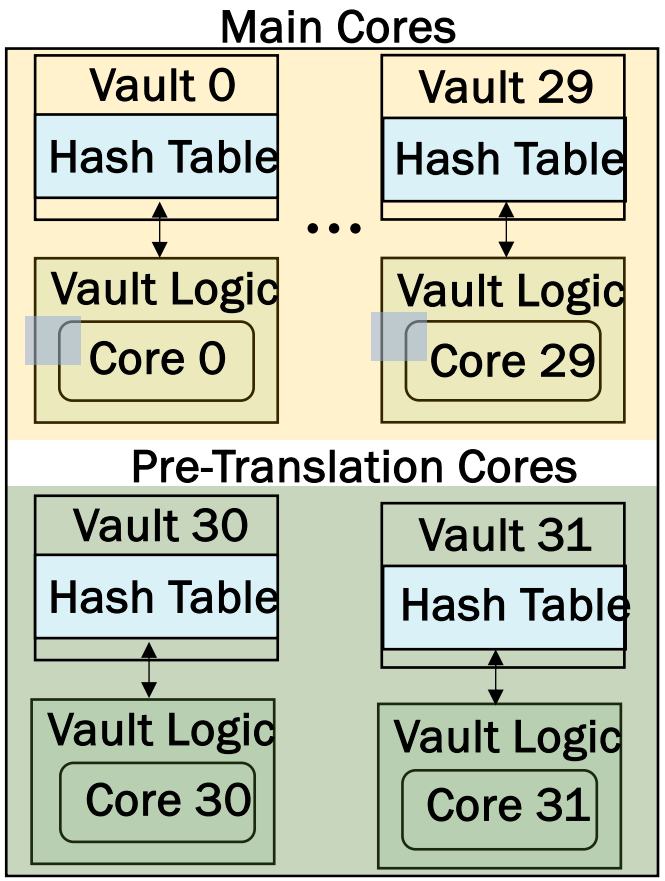


Key Idea: Pre-translation of page table walks

Utilize some throughput to pre-translate page table walks

```
#pragma omp parallel for
for(...)
{
    Code for main cores
    x=array1[i]
    sum+=x
}
for(...)
{
  Code for pre-translation cores
    x=array1[i]
    sum+=x
}
```

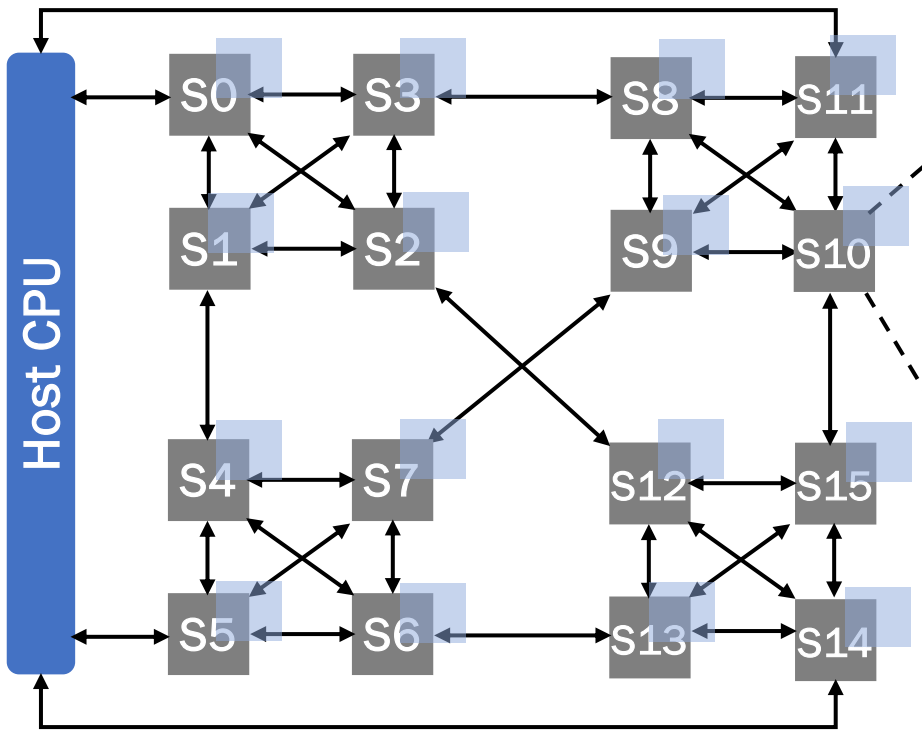


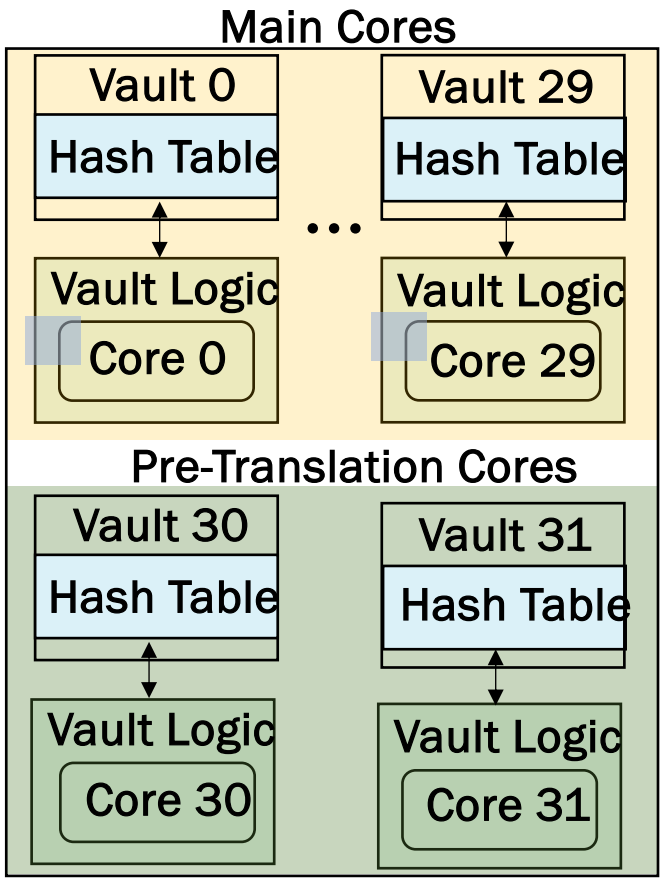


Key Idea: Pre-translation of page table walks

Utilize some throughput to pre-translate page table walks

```
#pragma omp parallel for
for(...)
{
    Code for main cores
    x=array1[i]
    sum+=x
}
for(...)
{
  Code for pre-translation cores
    x=array1[i]
    sum+=x
}
```



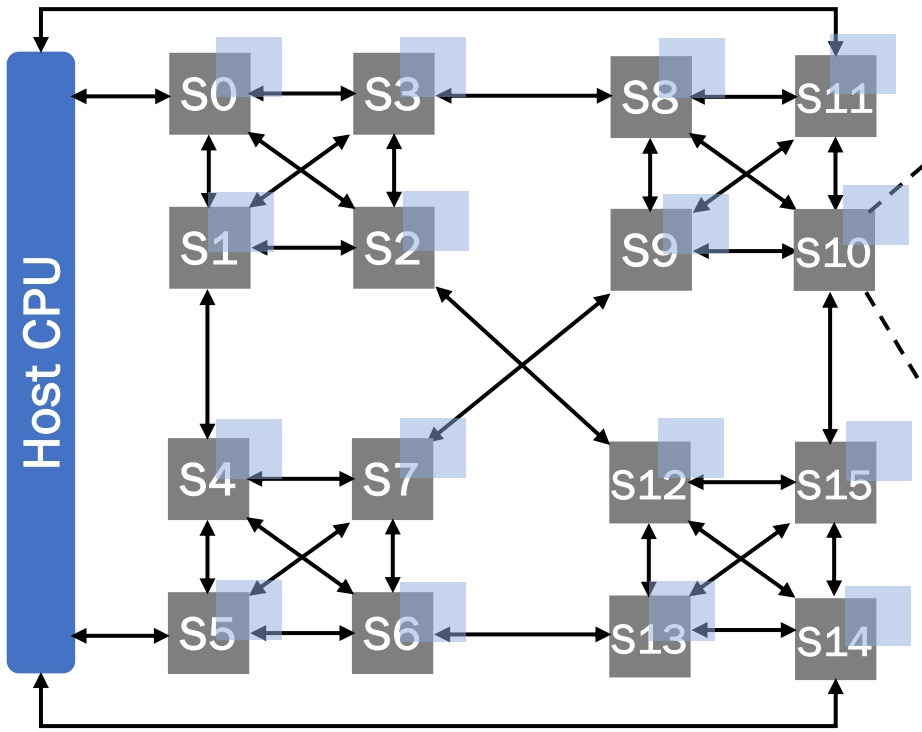


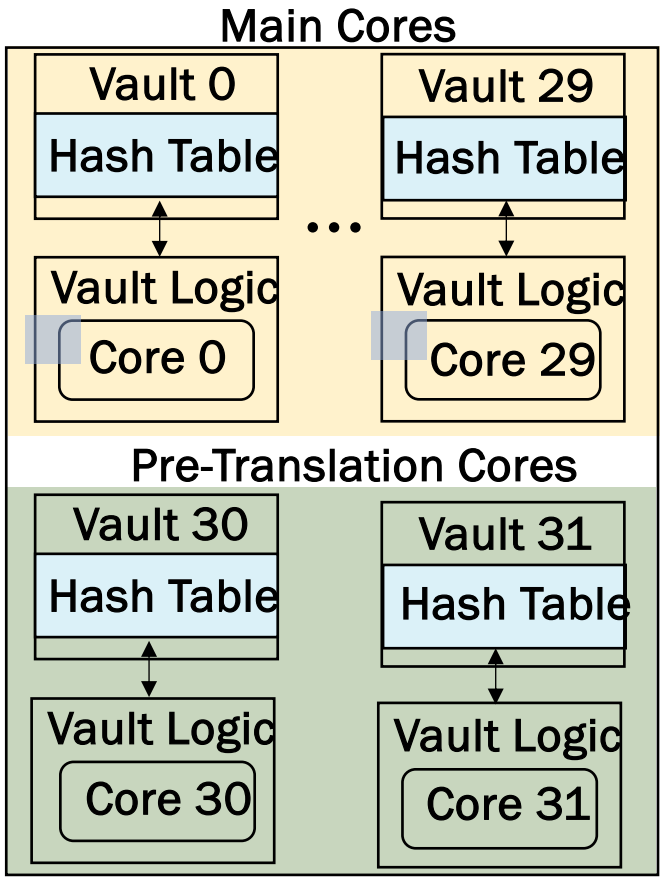
Pre-translation cores run ahead iterations for the main cores

Key Idea: Pre-translation of page table walks

Filter the pre-translation code to remove non-memory accesses and accesses to small data structures that are less likely to trigger PTW

```
#pragma omp parallel for
for(...)
{
    Code for main cores
    x=array1[i]
    sum+=x
}
for(...)
{
  Code for pre-translation cores
    x=array1[i]
    sum+=x
}
```

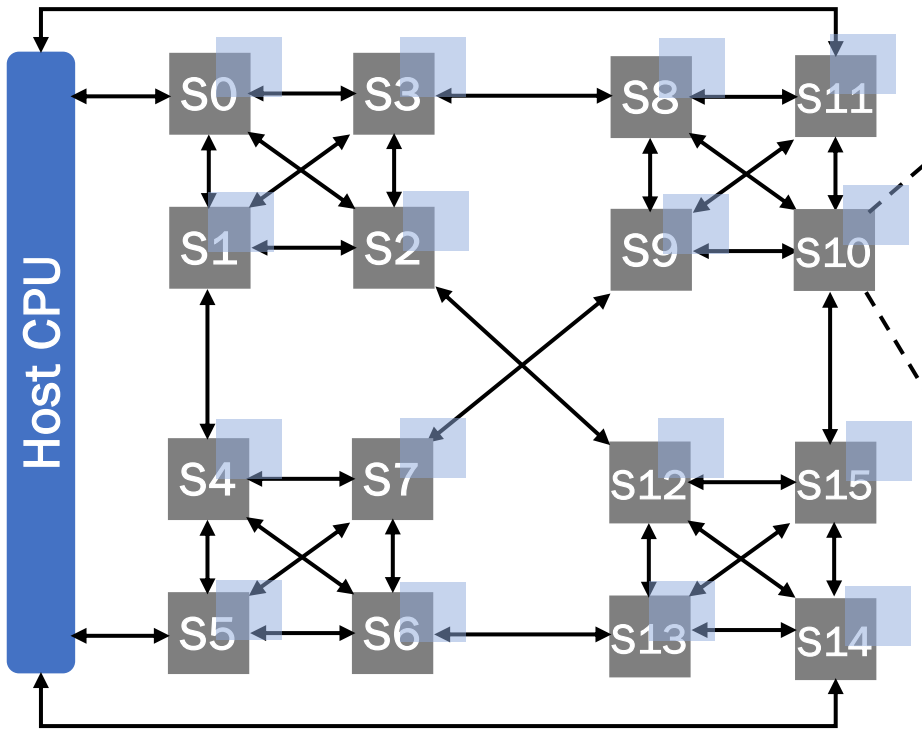


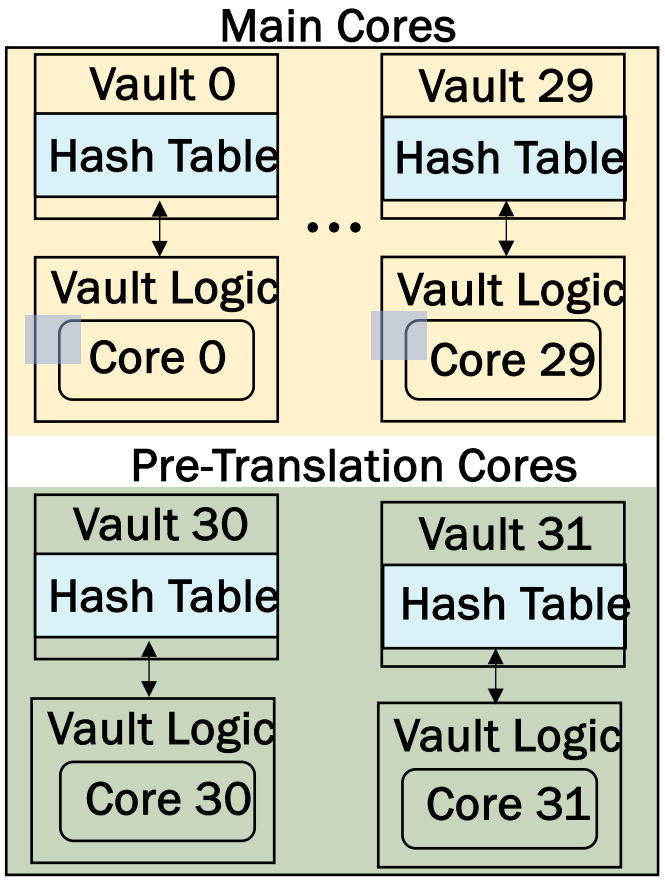


Key Idea: Pre-translation of page table walks

Filter the pre-translation code to remove non-memory accesses and accesses to small data structures that are less likely to trigger PTW

```
#pragma omp parallel for
for(...)
{
    Code for main cores
    x=array1[i]
    sum+=x
}
for(...)
{
  Code for pre-translation cores
    x=array1[i]
    [redacted]
}
```

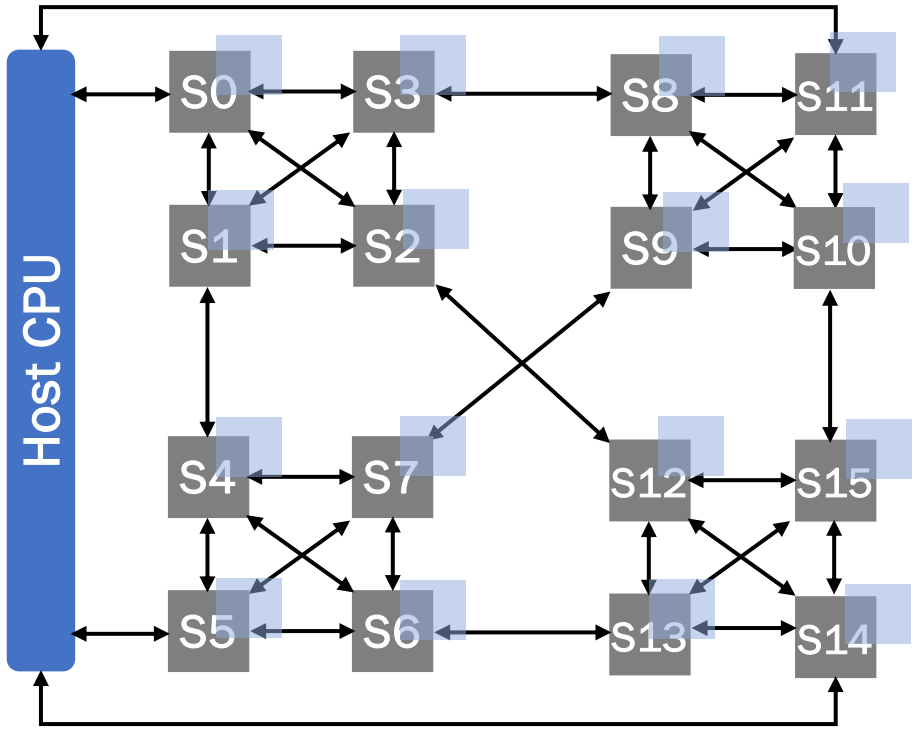


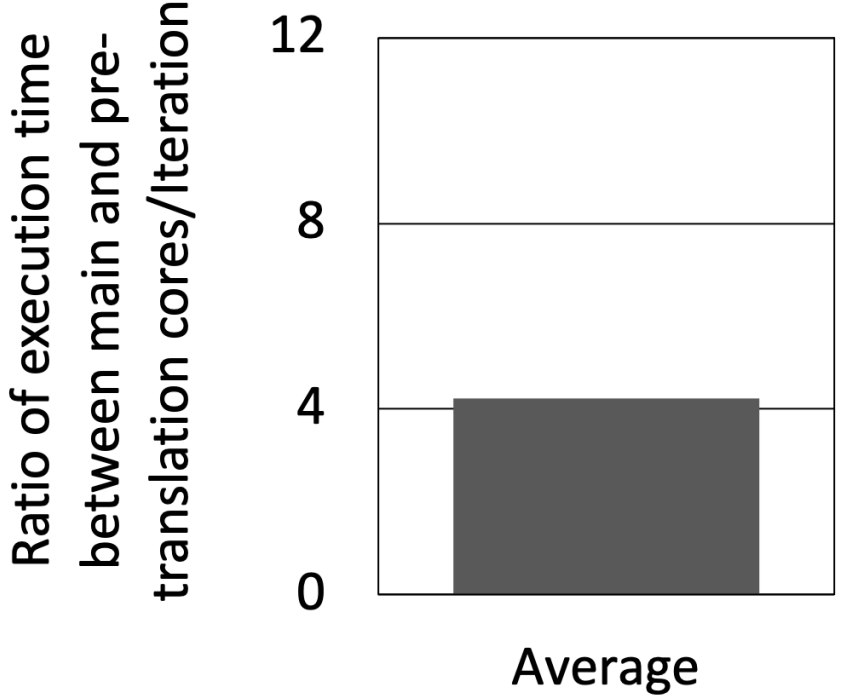


Key Idea: Pre-translation of page table walks

Filter the pre-translation code to remove non-memory accesses and accesses to small data structures that are less likely to trigger PTW

```
#pragma omp parallel for
for(...)
{
    Code for main cores
    x=array1[i]
    sum+=x
}
for(...)
{
  Code for pre-translation cores
    x=array1[i]
}
```





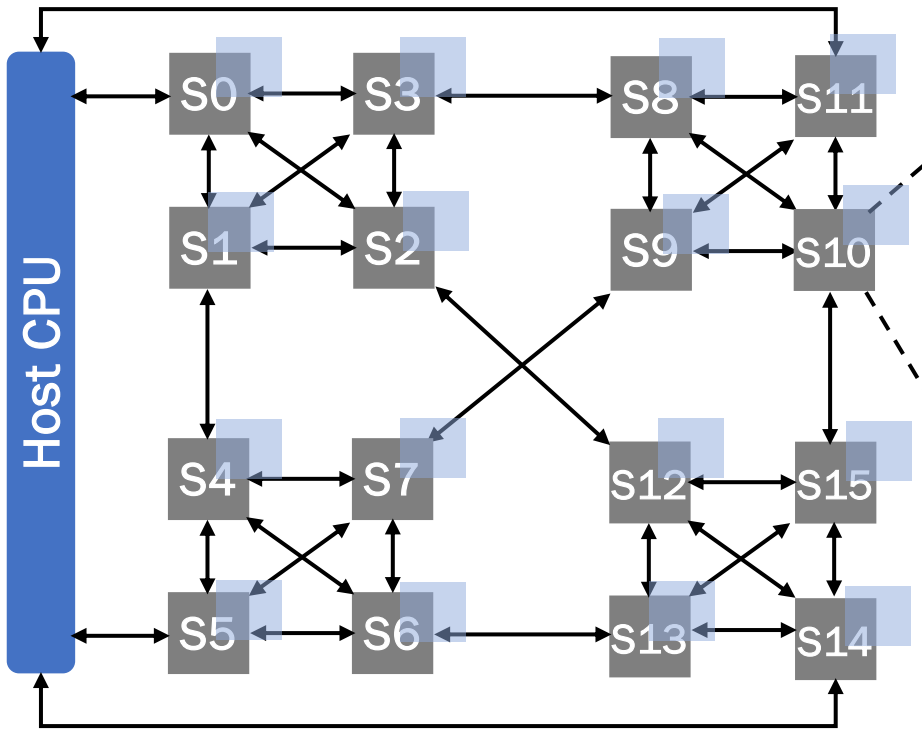
Pre-translation cores run faster than the main cores and are able to help a larger fraction of the main cores

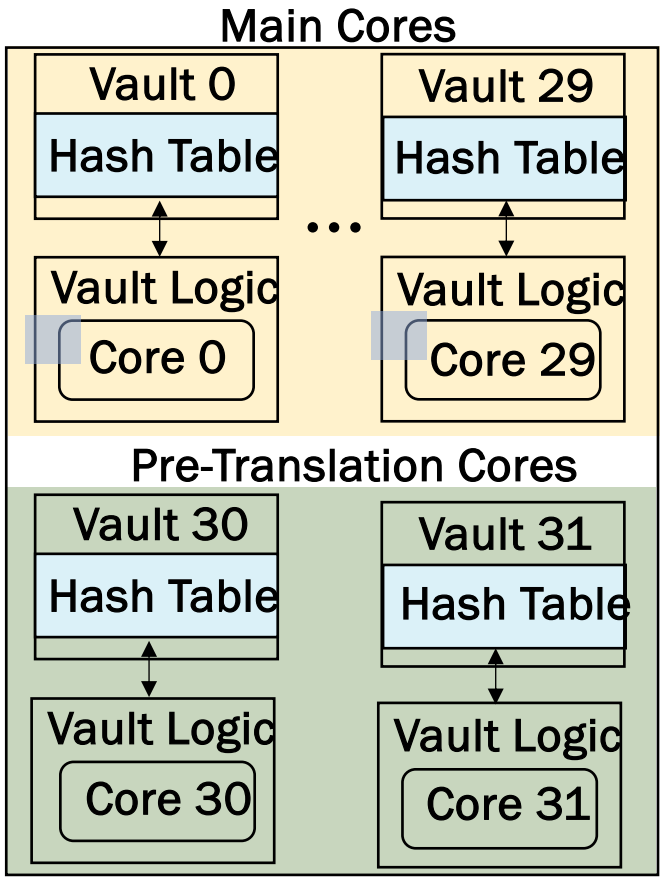
Key Idea: Pre-translation of page table walks

```
#pragma omp parallel for
for(...)
{
    Code for main cores
    x=array1[i]
    sum+=x
}

for(...)
{
  Code for pre-translation cores
    x=array1[i]

}
```





Key Idea: Pre-translation of page table walks

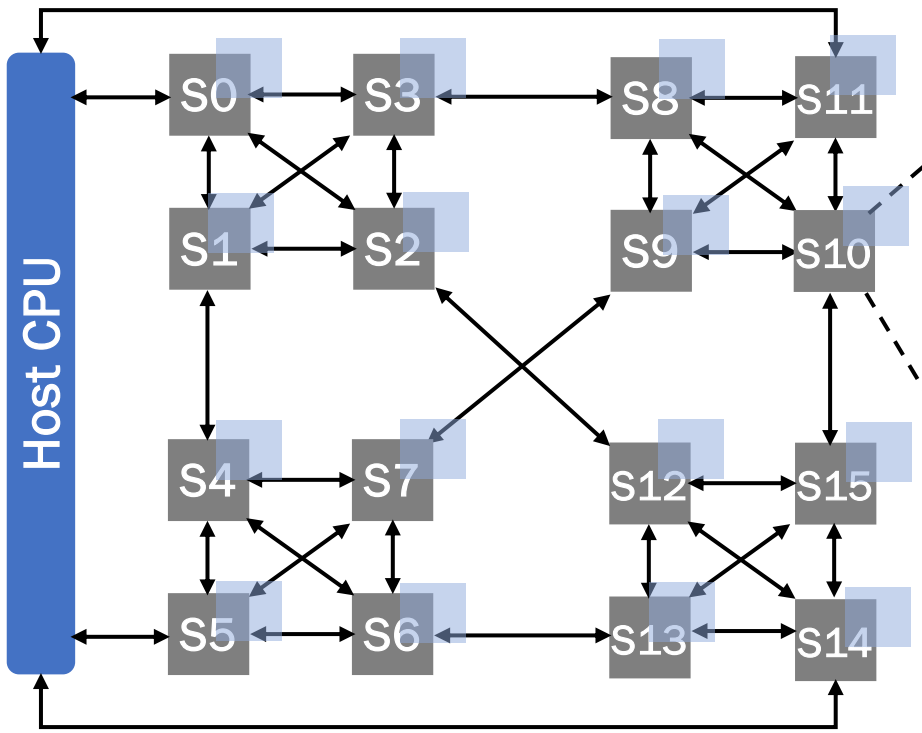
Step 1

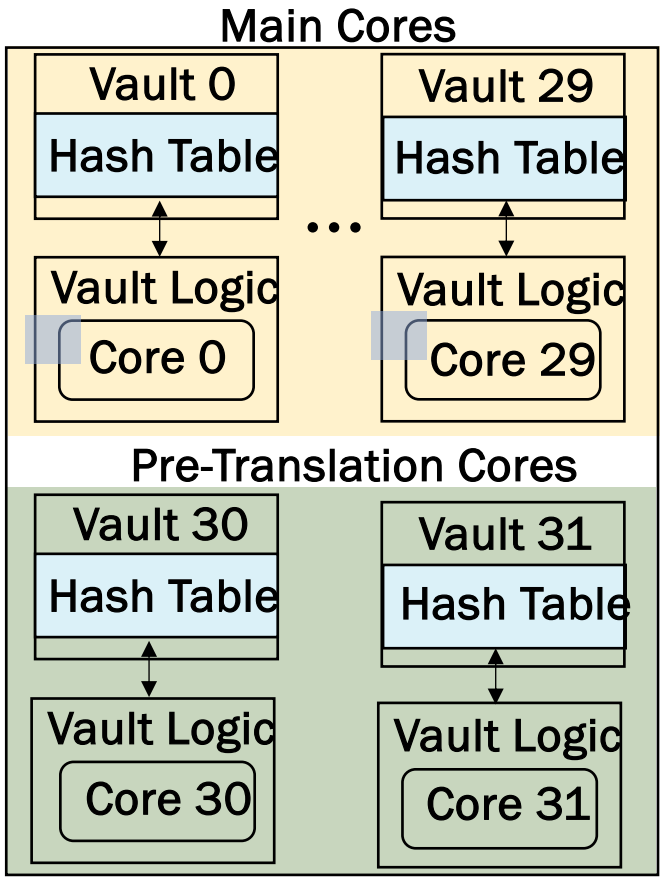
Timeline

```
#pragma omp parallel for
for(...)
{
    Code for main cores
    x=array1[i]
    sum+=x
}

for(...)
{
  Code for pre-translation cores
    x=array1[i]

}
```





Key Idea: Pre-translation of page table walks

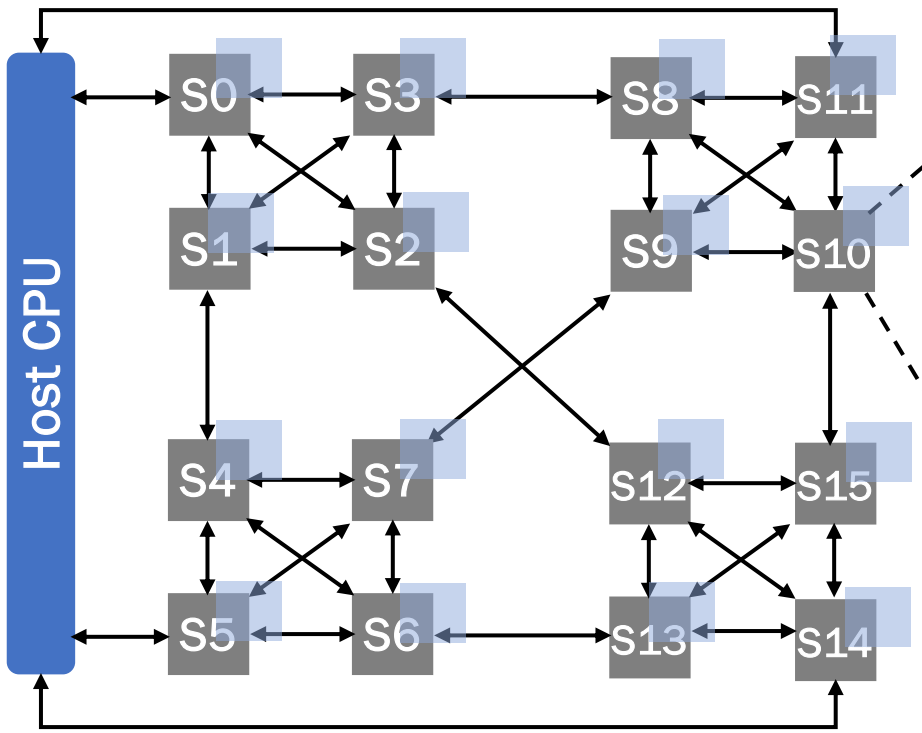
Step 1

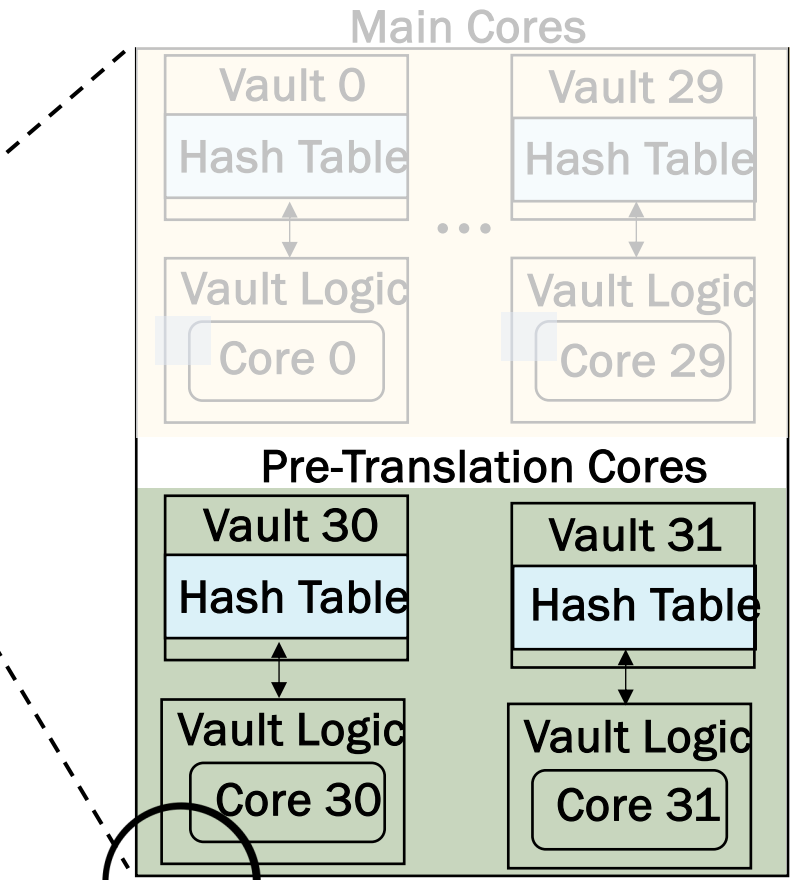
Timeline

```
#pragma omp parallel for
for(...) // ITERATION u =0
{
    Code for main cores
    x=array1[i]
    sum+=x
}

for(...) // ITERATION u=10
{
  Code for pre-translation cores
    x=array1[i]

}
```





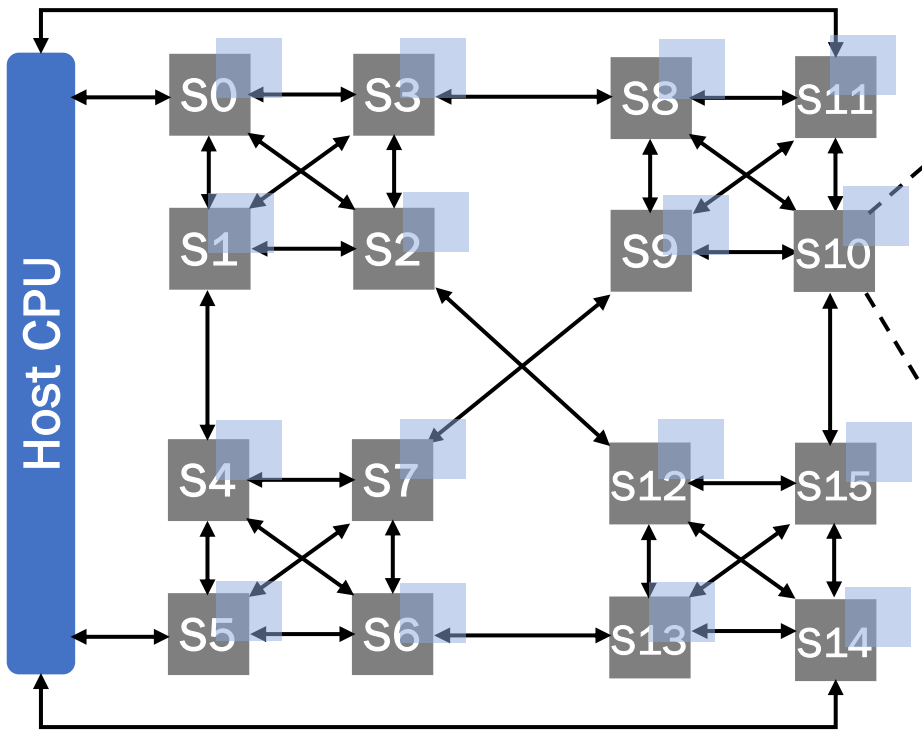
Key Idea: Pre-translation of page table walks

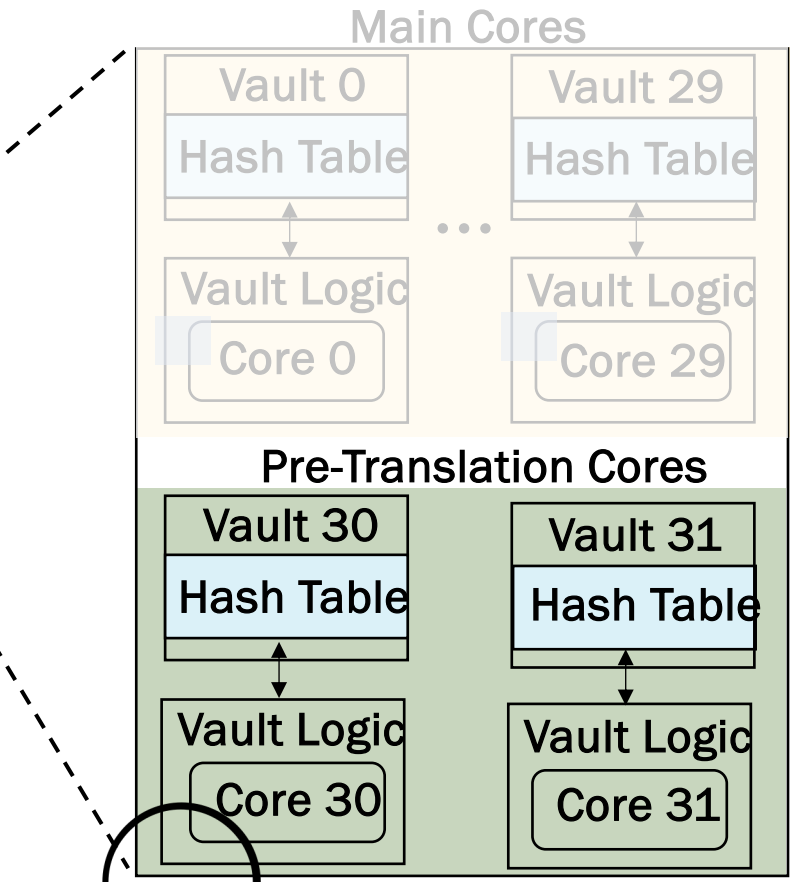
Step 1

Timeline

```
#pragma omp parallel for
for(...) // ITERATION u =0
{
    Code for main cores
    x=array1[i]
    sum+=x
}

for(...) // ITERATION u=10
{
  Code for pre-translation cores
    x=array1[i]   TLB Miss Generated
}
```





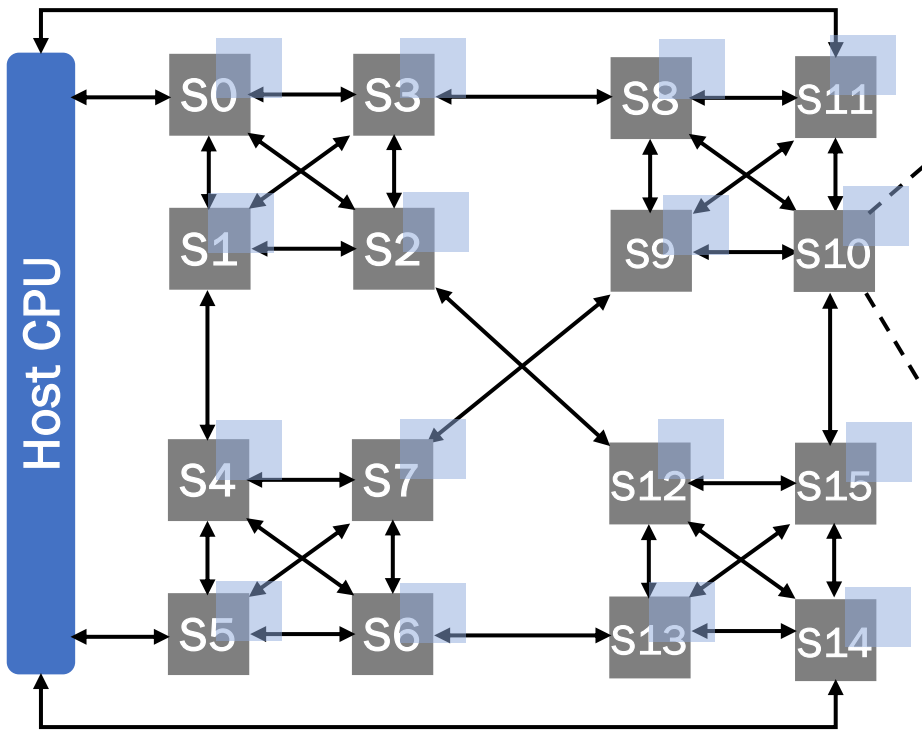
Key Idea: Pre-translation of page table walks

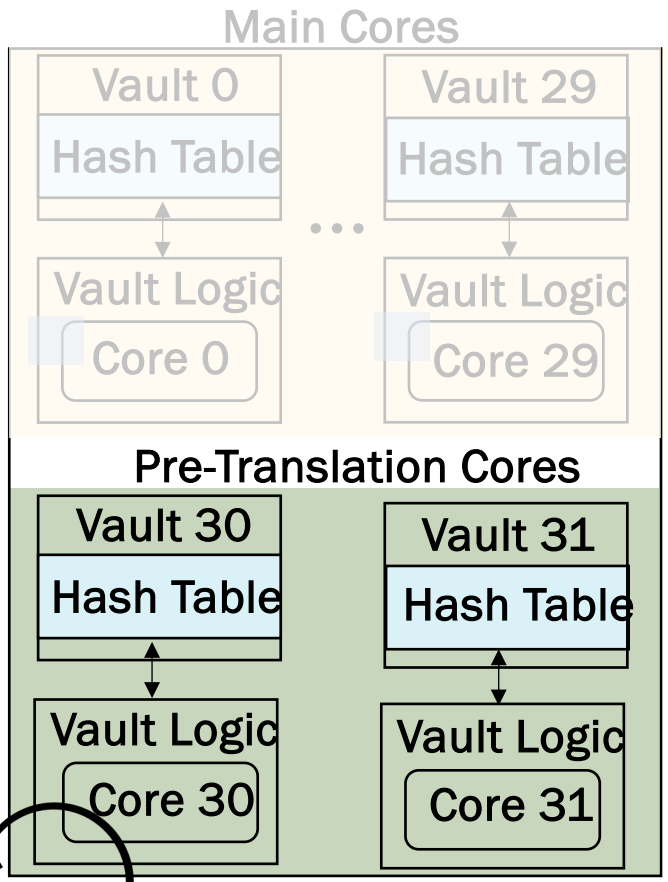
Step 1

Timeline

```
#pragma omp parallel for
for(...) // ITERATION u =0
{
    Code for main cores
    x=array1[i]
    sum+=x
}

for(...) // ITERATION u=10
{
  Code for pre-translation cores
    x=array1[i]   TLB Miss Generated
}
```





Perform PTW u=10

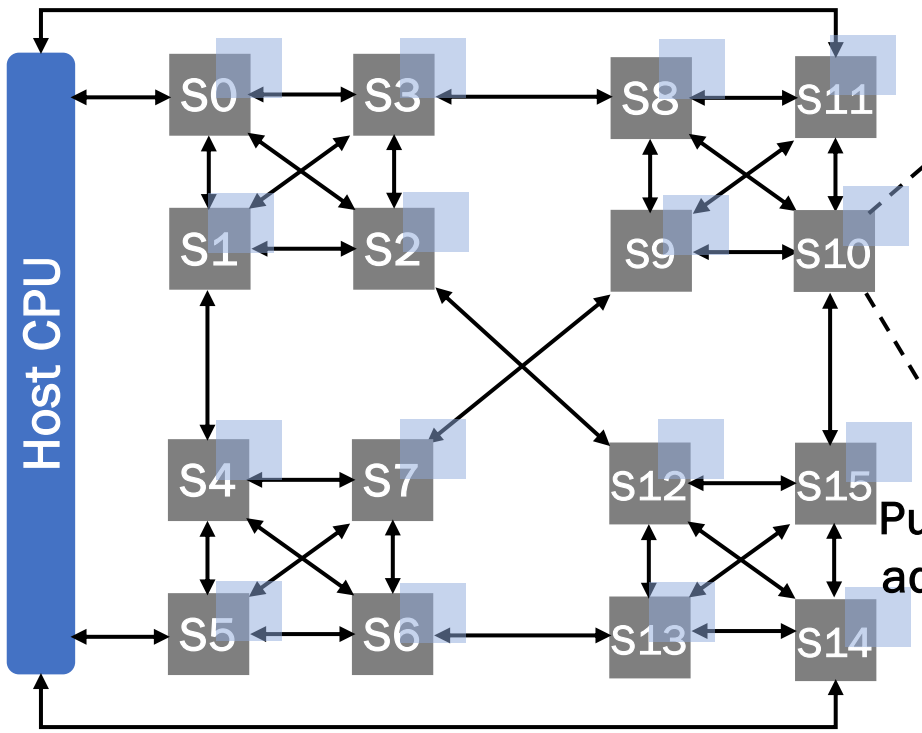
Key Idea: Pre-translation of page table walks

Step 1

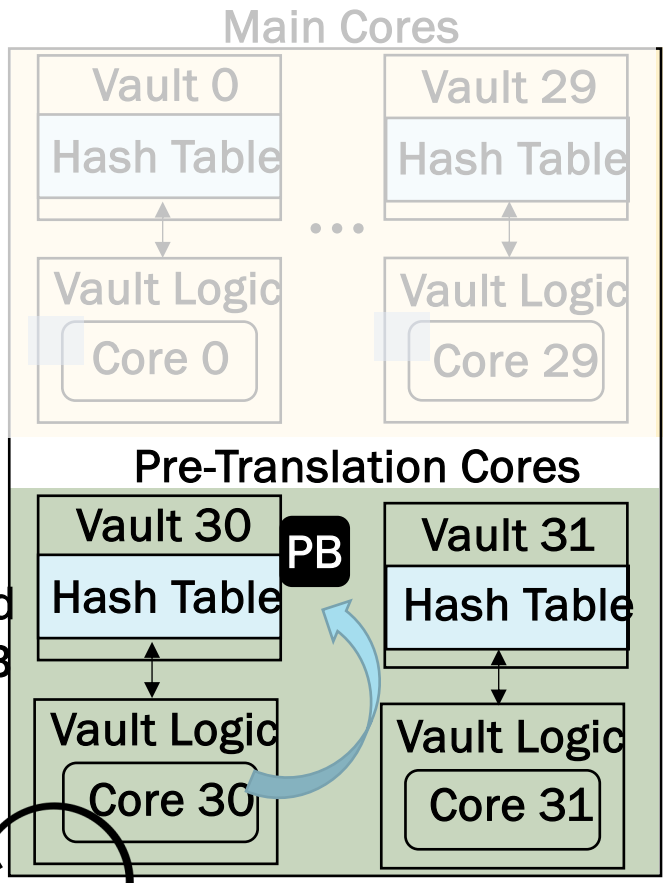
Timeline

```
#pragma omp parallel for
for(...) // ITERATION u =0
{
    Code for main cores
    x=array1[i]
    sum+=x
}

for(...) // ITERATION u=10
{
  Code for pre-translation cores
    x=array1[i]   TLB Miss Generated
}
```



Put translated address in PB



Perform PTW u=10

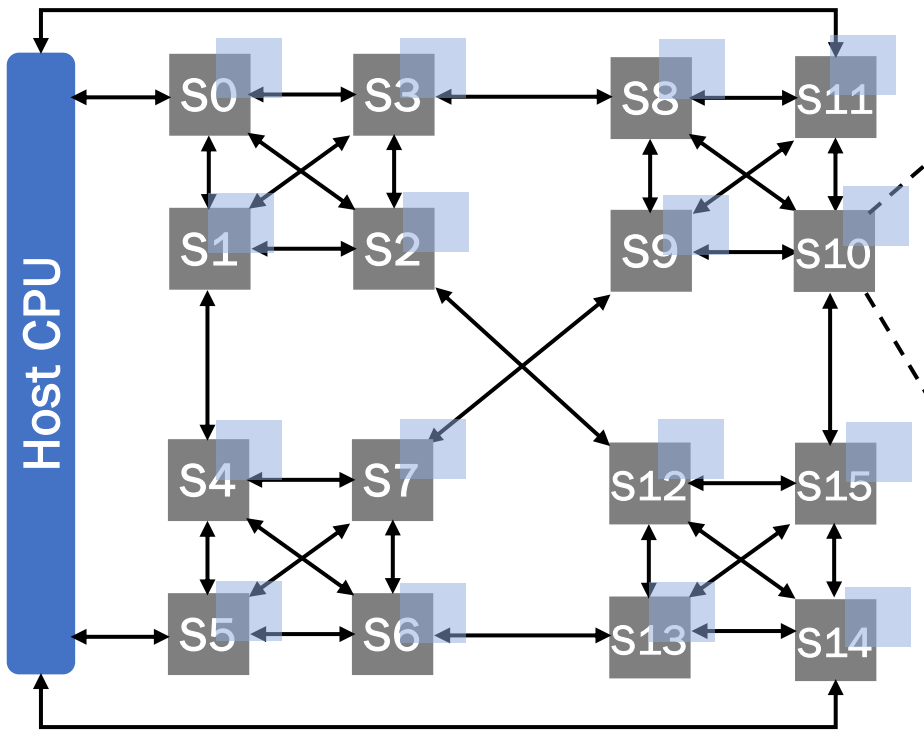
PB Pre-Translation Buffer

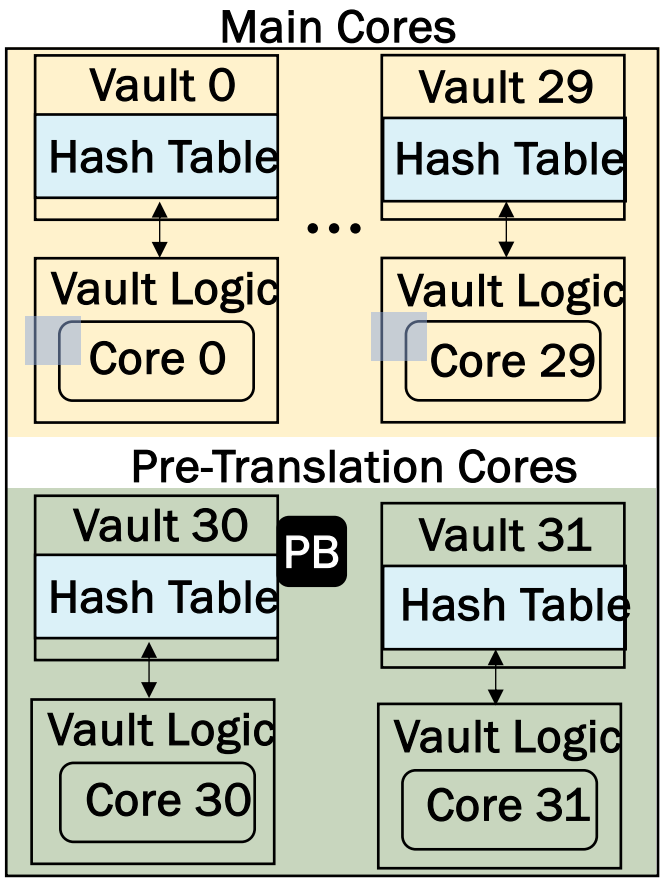
Key Idea: Pre-translation of page table walks

Step 1 | Step 2

Timeline

```
#pragma omp parallel for
for(...)
{
    Code for main cores
    x=array1[i]
    sum+=x
}
for(...)
{
    Code for pre-translation cores
    x=array1[i]
}
```





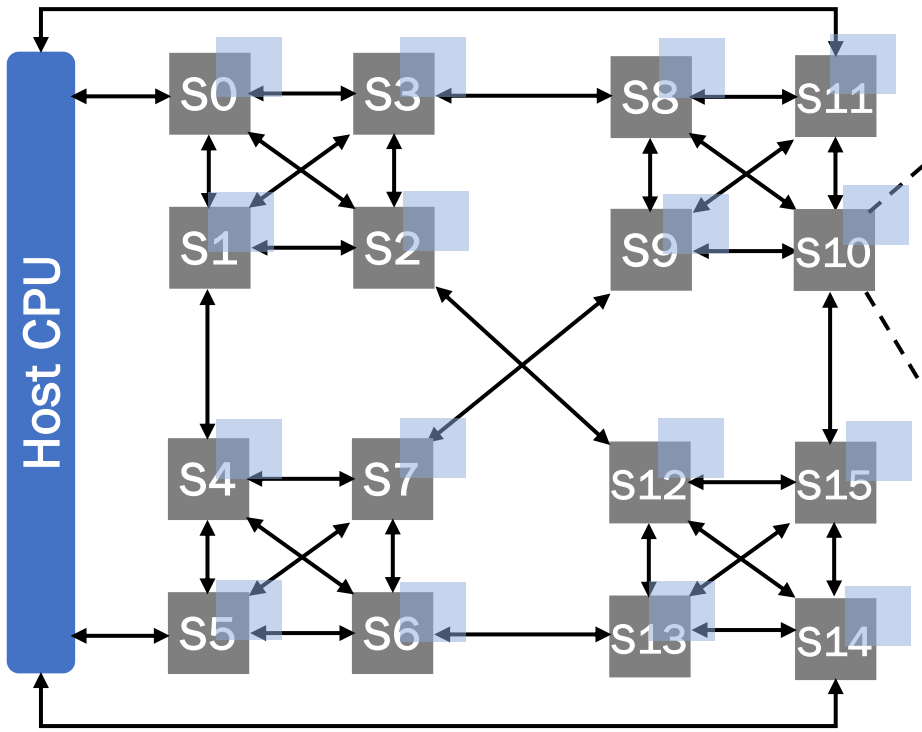
PB Pre-Translation Buffer

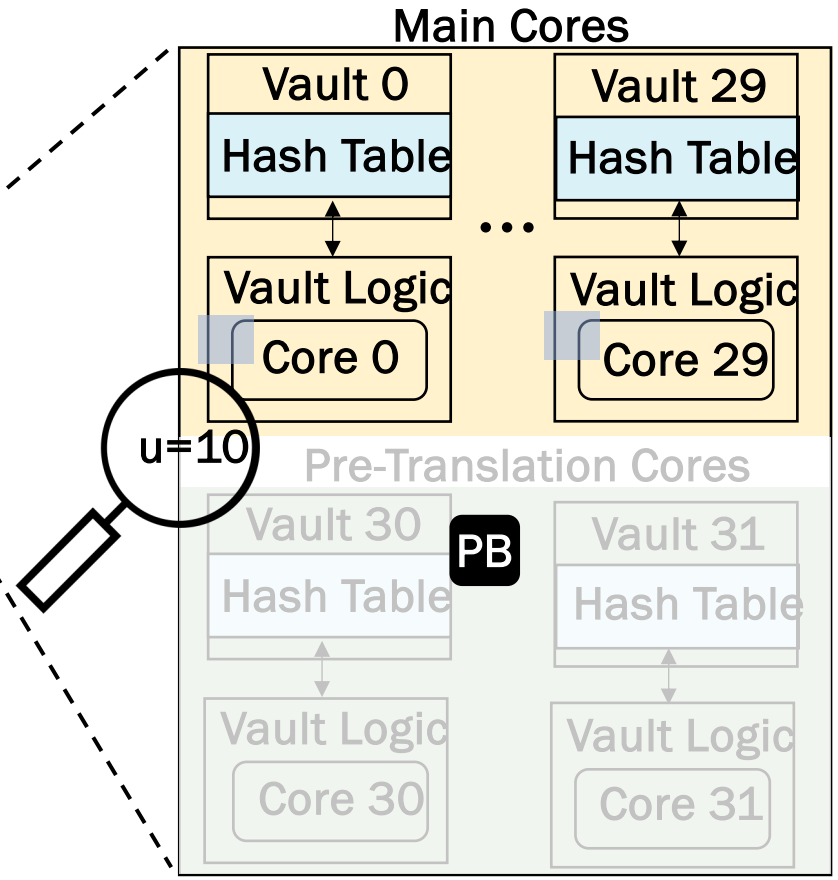
Key Idea: Pre-translation of page table walks

Step 1 | Step 2

Timeline

```
#pragma omp parallel for
for(...) // ITERATION u =10
{
    Code for main cores
    x=array1[i]
    sum+=x
}
for(...) // ITERATION u=20
{
    Code for pre-translation cores
    x=array1[i]
}
```





PB Pre-Translation Buffer

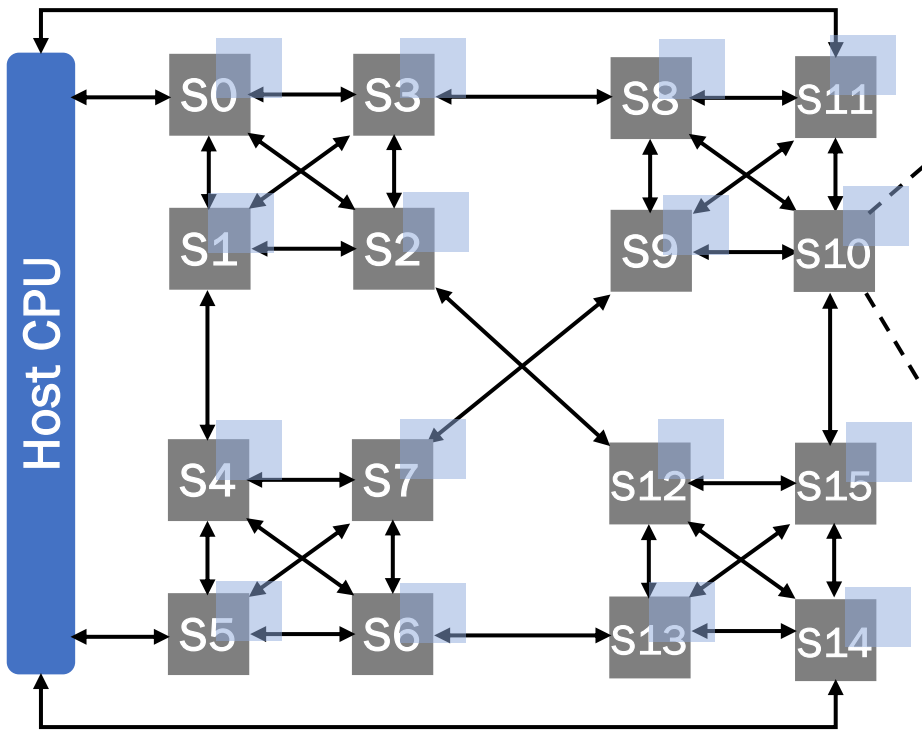
Key Idea: Pre-translation of page table walks

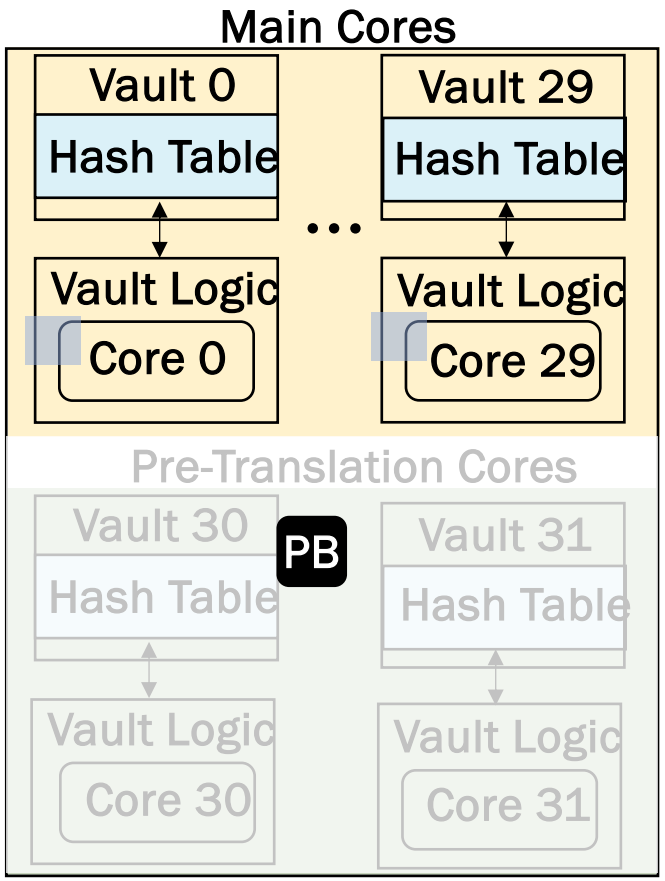
Step 1 | Step 2

Timeline

```
#pragma omp parallel for
for(...) // ITERATION u =10
{
    Code for main cores
    x=array1[i]
    sum+=x
}
for(...) // ITERATION u=20
{
    Code for pre-translation cores
    x=array1[i]
}
```

TLB Miss Generated





PB Pre-Translation Buffer

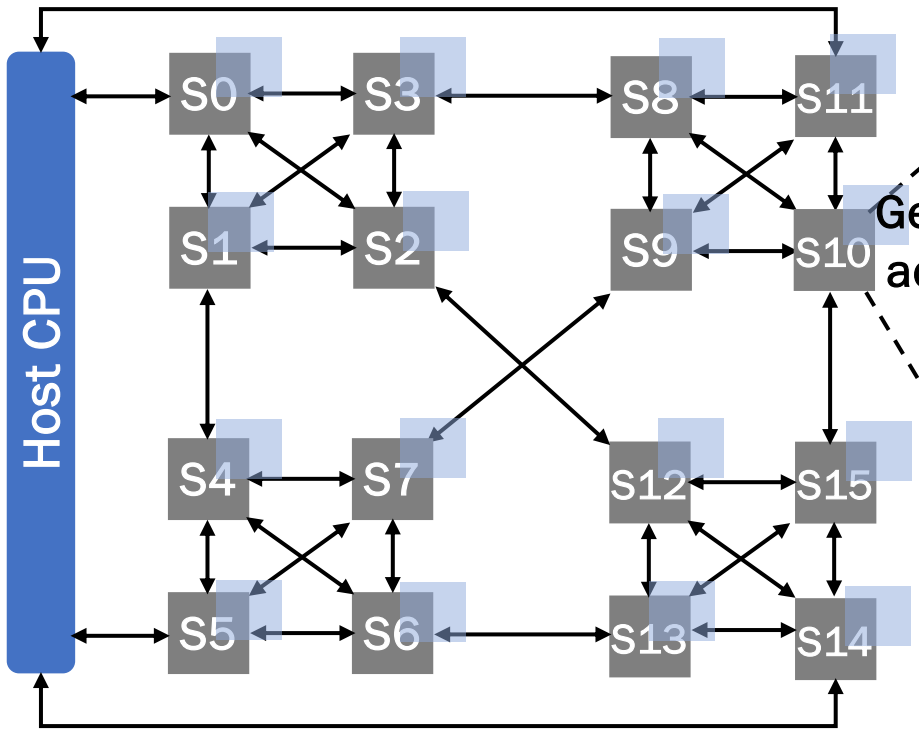
Key Idea: Pre-translation of page table walks

Step 1 | Step 2

Timeline

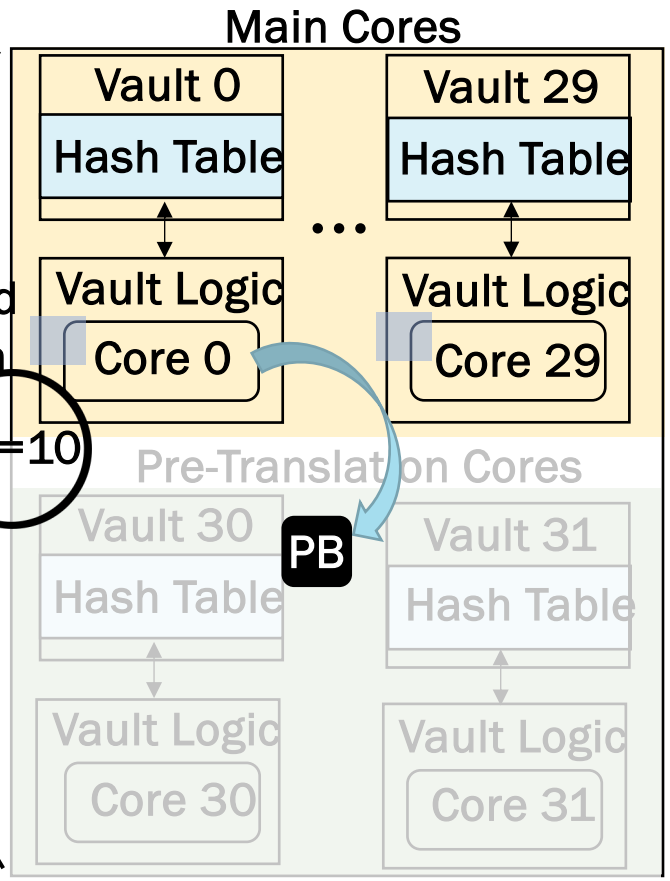
```
#pragma omp parallel for
for(...) // ITERATION u =10
{
    Code for main cores
    x=array1[i]
    sum+=x
}
for(...) // ITERATION u=20
{
    Code for pre-translation cores
    x=array1[i]
}
```

TLB Miss Generated



Get translated address from PB

u=10



PB Pre-Translation Buffer

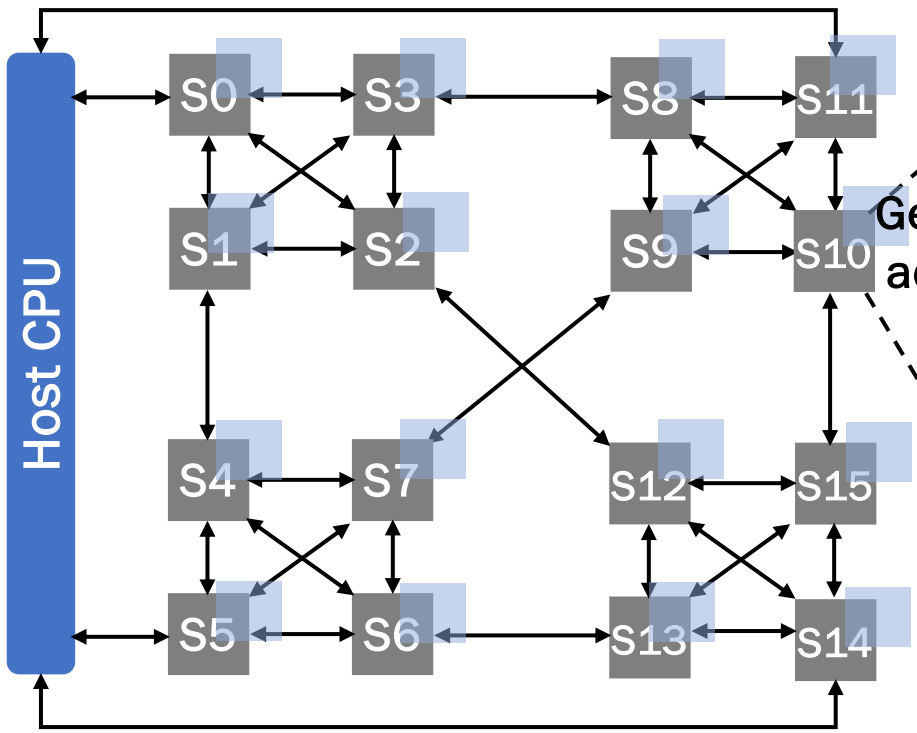
Key Idea: Pre-translation of page table walks

Step 1 | Step 2

Timeline

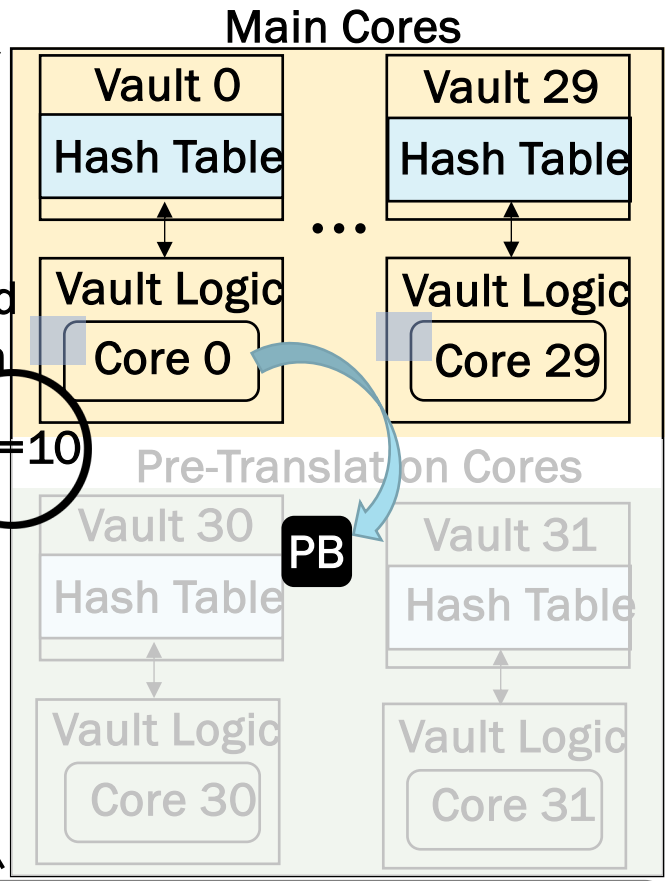
```
#pragma omp parallel for
for(...) // ITERATION u =10
{
    Code for main cores
    x=array1[i]
    sum+=x
}
for(...) // ITERATION u=20
{
    Code for pre-translation cores
    x=array1[i]
}
```

TLB Miss Generated



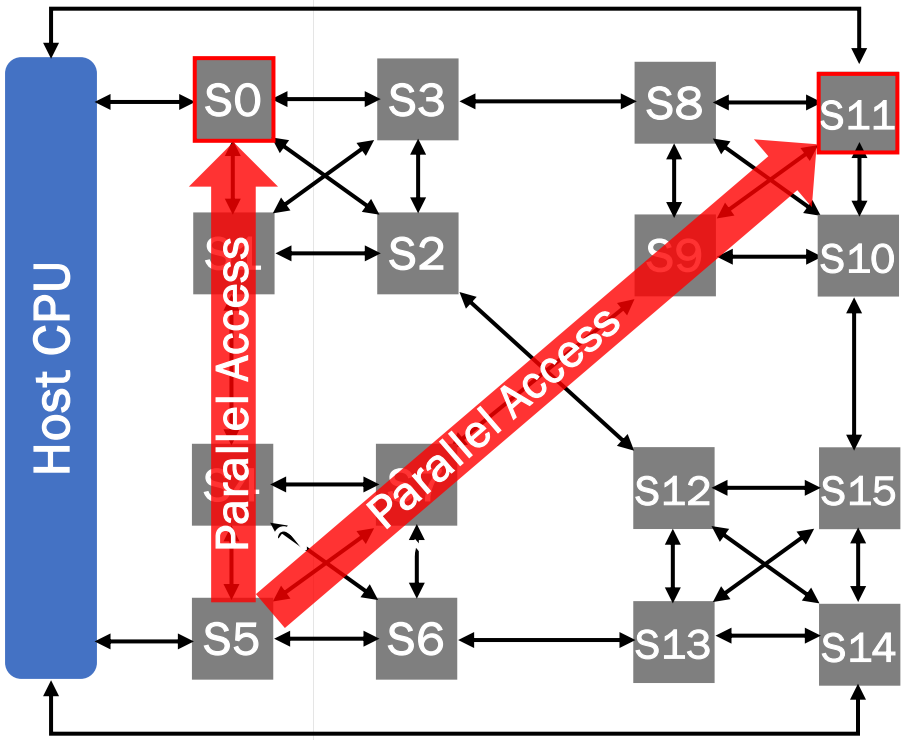
Get translated address from PB

u=10

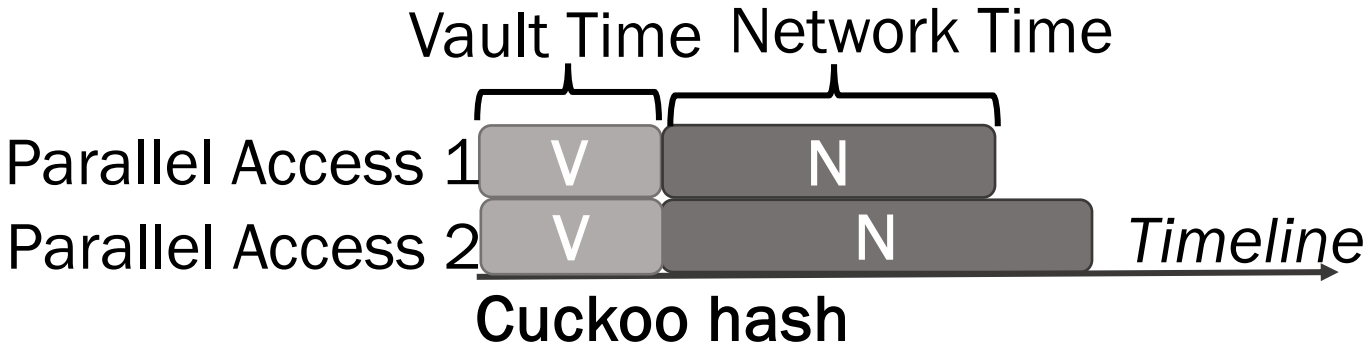


Pre-translation moves the page table walk latency off the critical path of execution

Summary of our approaches

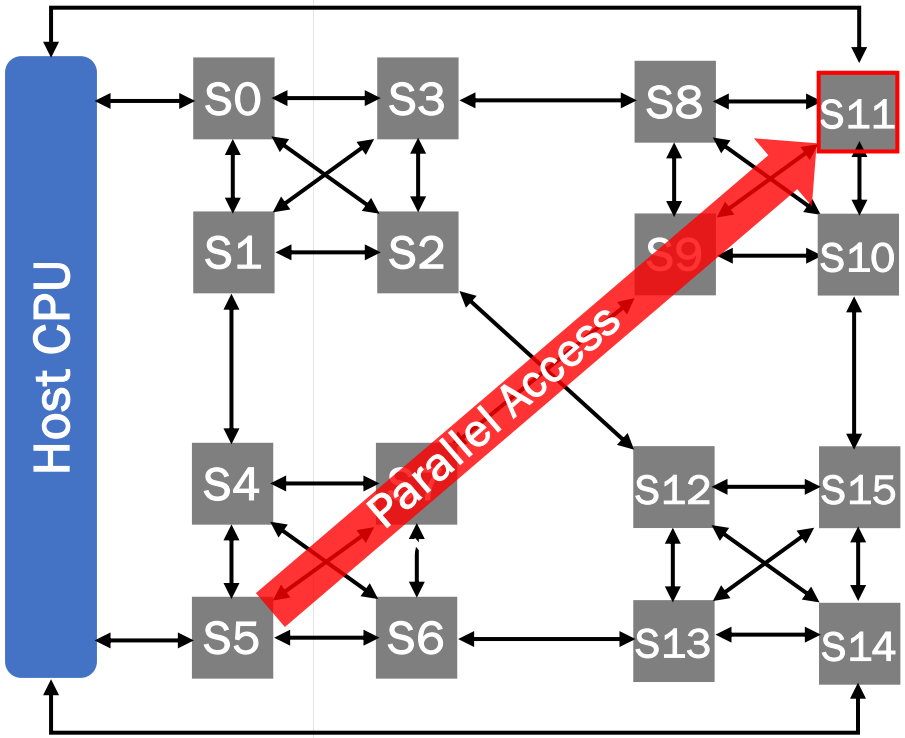


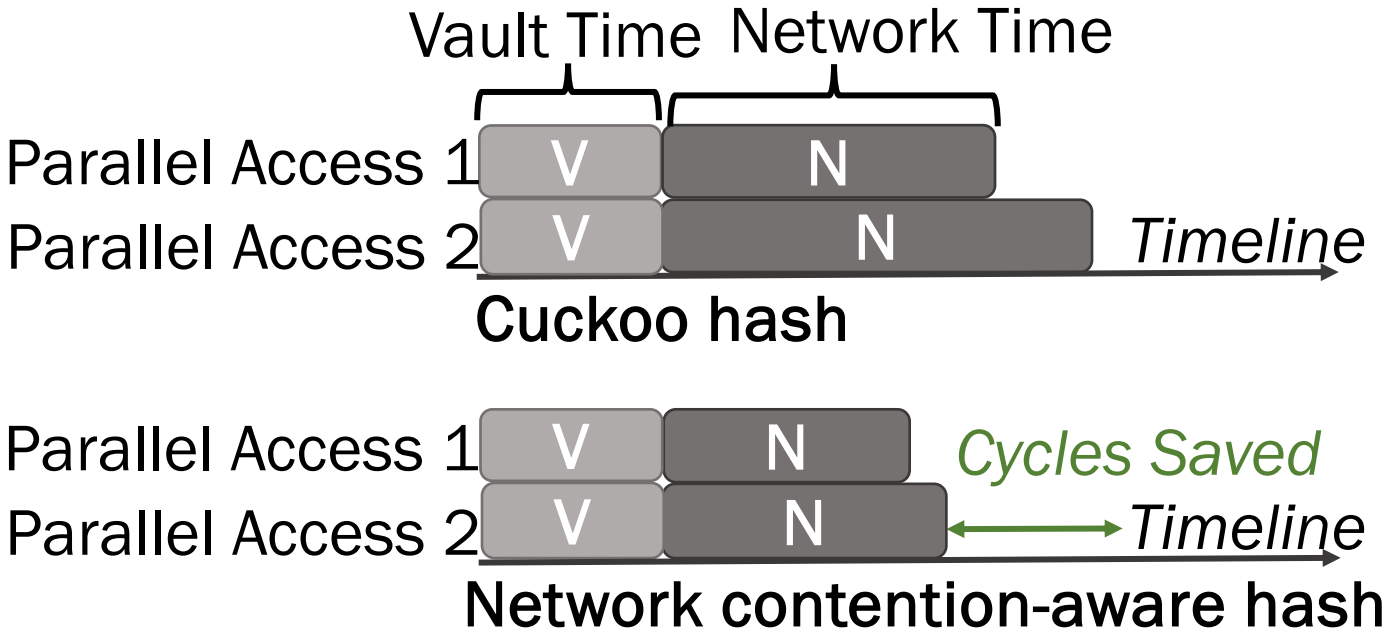
TLB Miss at Stack 5



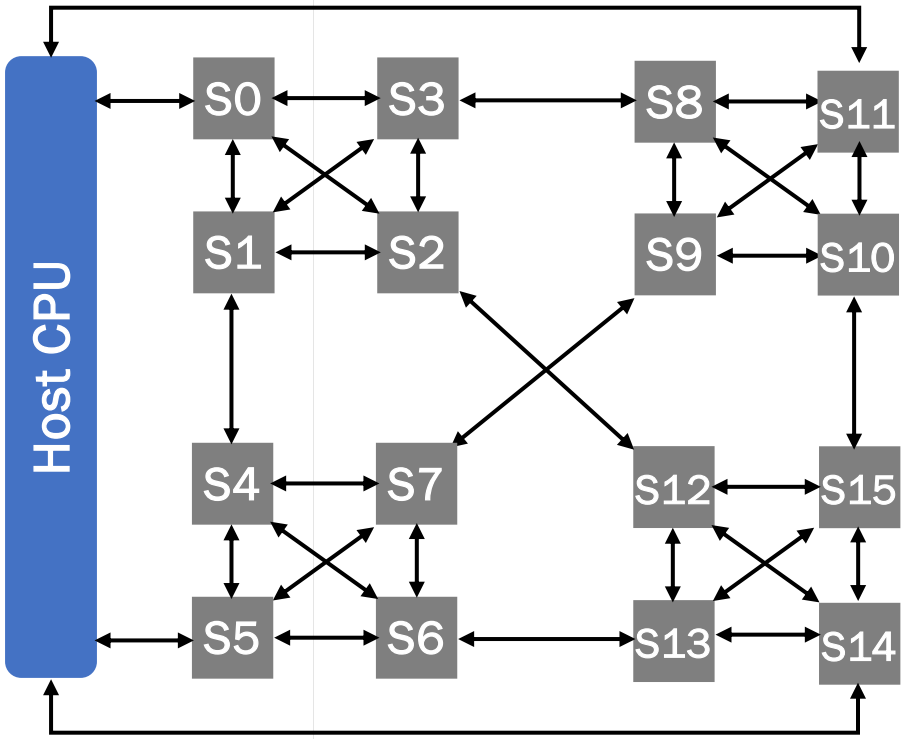
Cuckoo hash

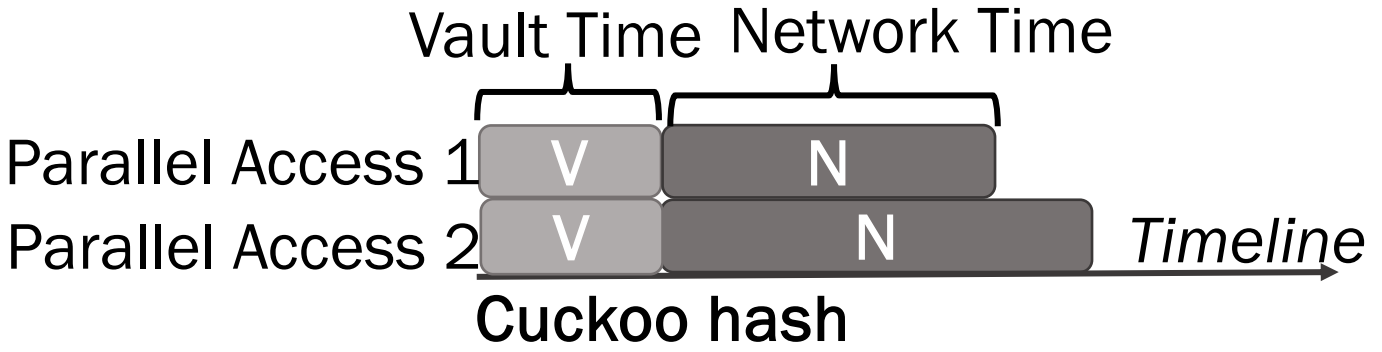
Summary of our approaches

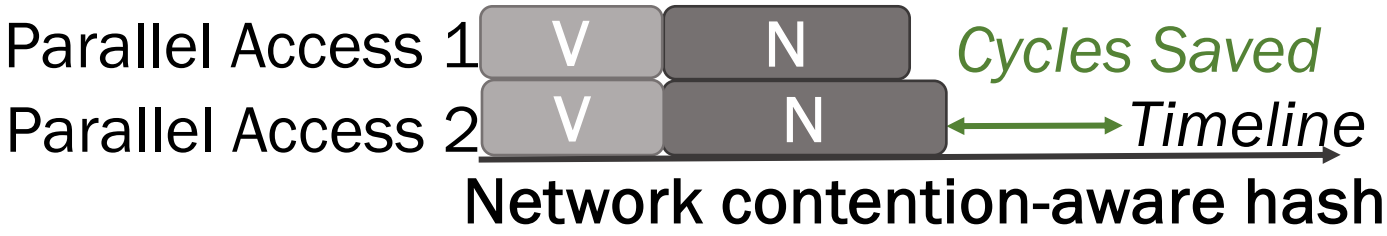


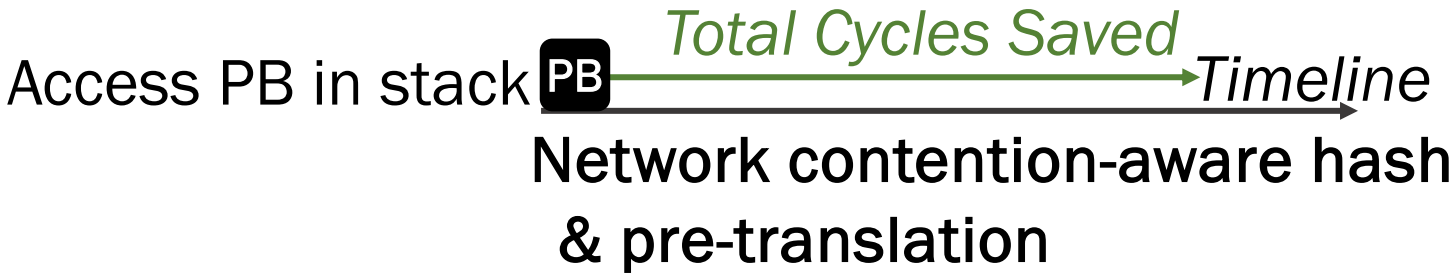


Summary of our approaches









Outline

- Processing-in-Memory Introduction
- Address Translation in PIM Architecture
- Challenges and Key Ideas
- Evaluation
- Conclusion

Methodology

Simulation Infrastructure (MultiPIM)

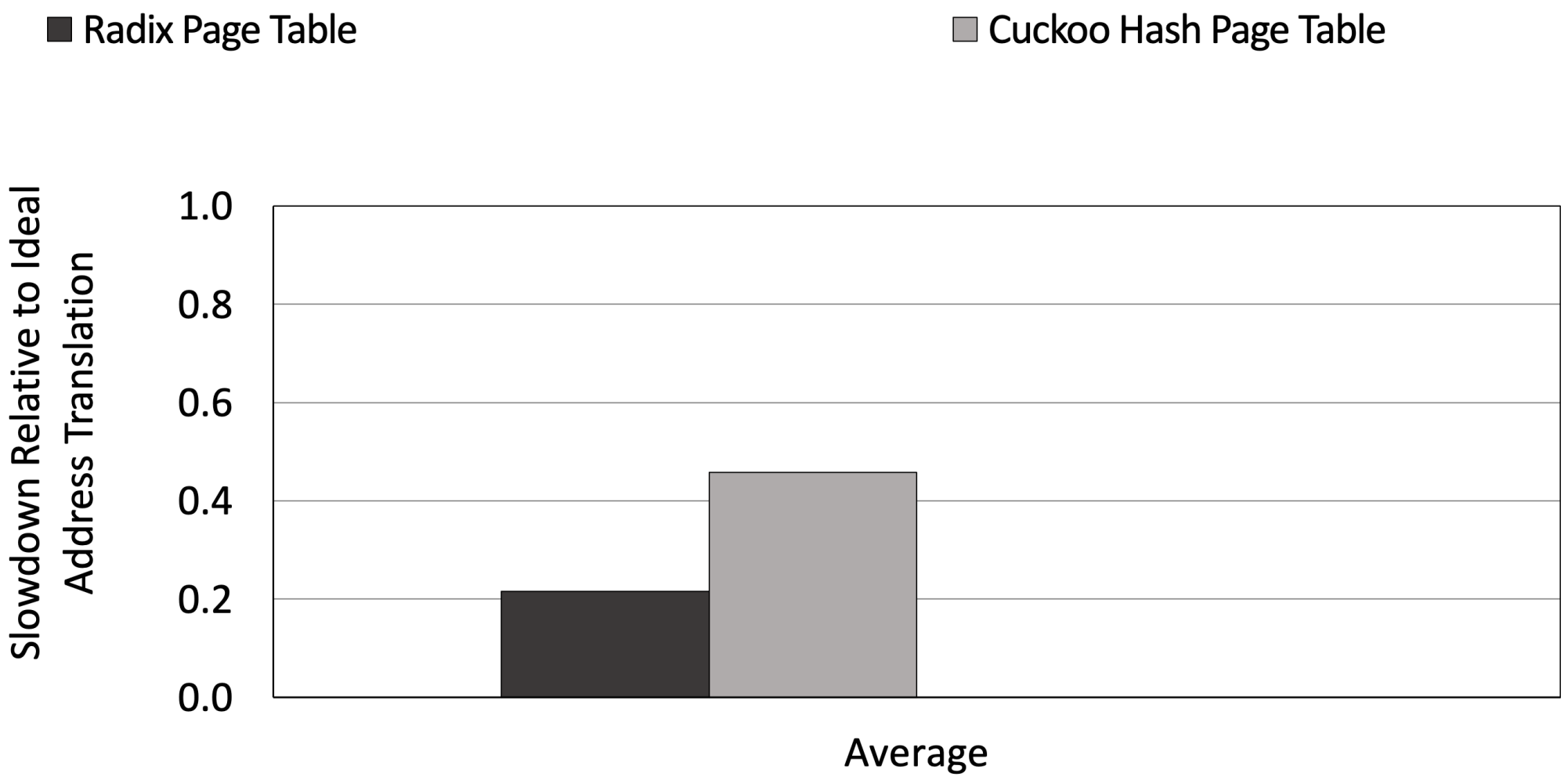
Configuration for Simulated PIM stacks		
Memory	Total number	16
	Memory interconnection	Dragonfly
	Capacity per memory	4GB, 4 layers, 8 banks per vault
	Vaults per memory	32, 32 TSV per vault
	DRAM	FR-FCFS, tCL=tRCD=tRP=17ns, tCWL=13ns
PIM Core	Type	In-order, 1 issue @ 2000MHZ
	L1I/D-Cache	Split 32KB, 4ways, 64B cacheline, LRU, write-back, MESI
	I/D-TLB	Split 64 entries, LRU
	Page table walker	1
	Pre-Translation Buffer Size	1024 entries per stack

Methodology

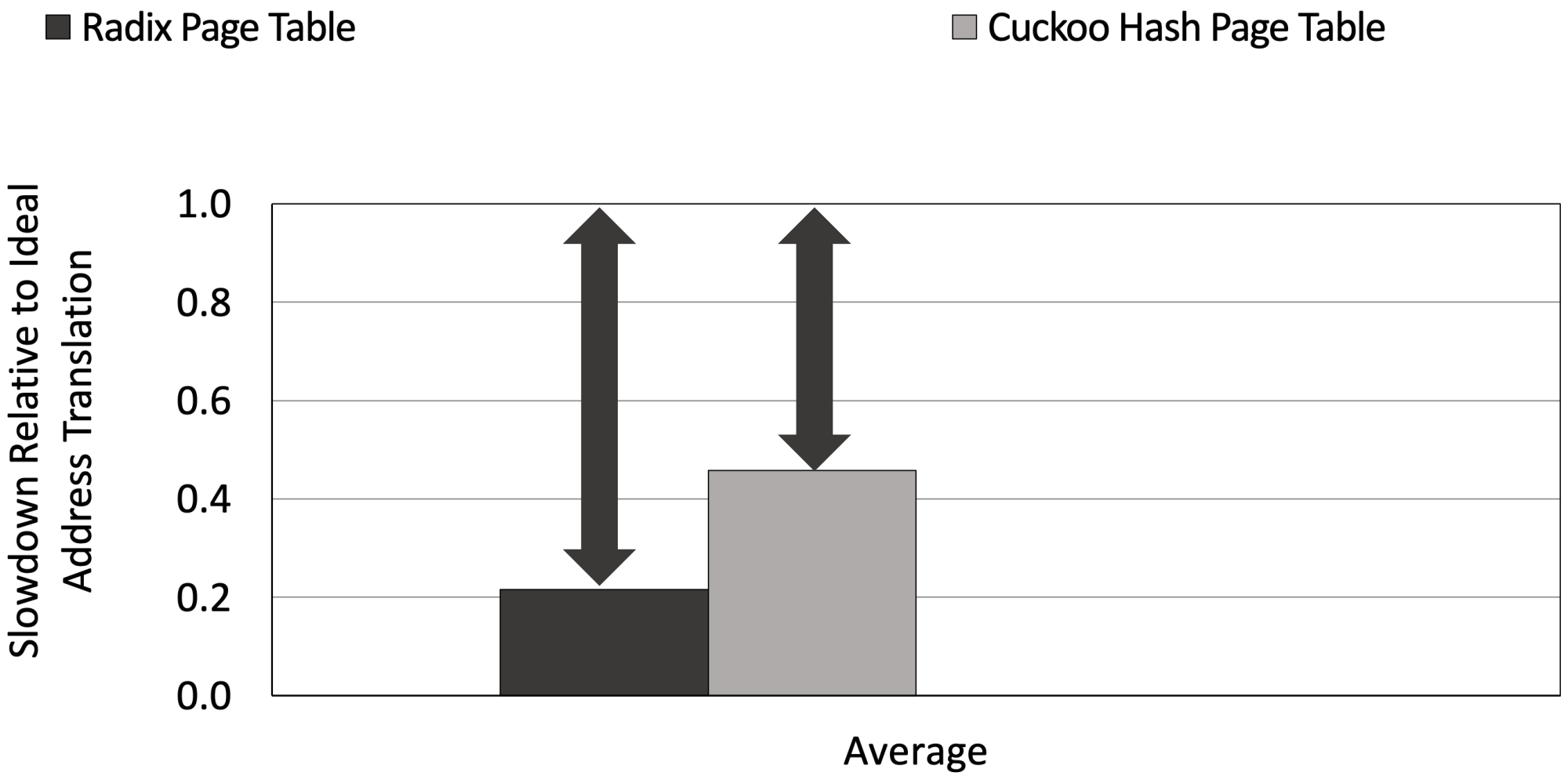
Workloads:

- Gapbs benchmark suite with workloads:
  - bfs
  - tc
  - cc
  - cc_sv
  - sssp
  - pr
- Parboil benchmark suite using the largest available dataset
  - spmv
  - sgemm
  - stencil
  - mri-grid
  - mri-q
  - histo
  - tpacf
  - cutcp
  - lbm

Performance Improvement

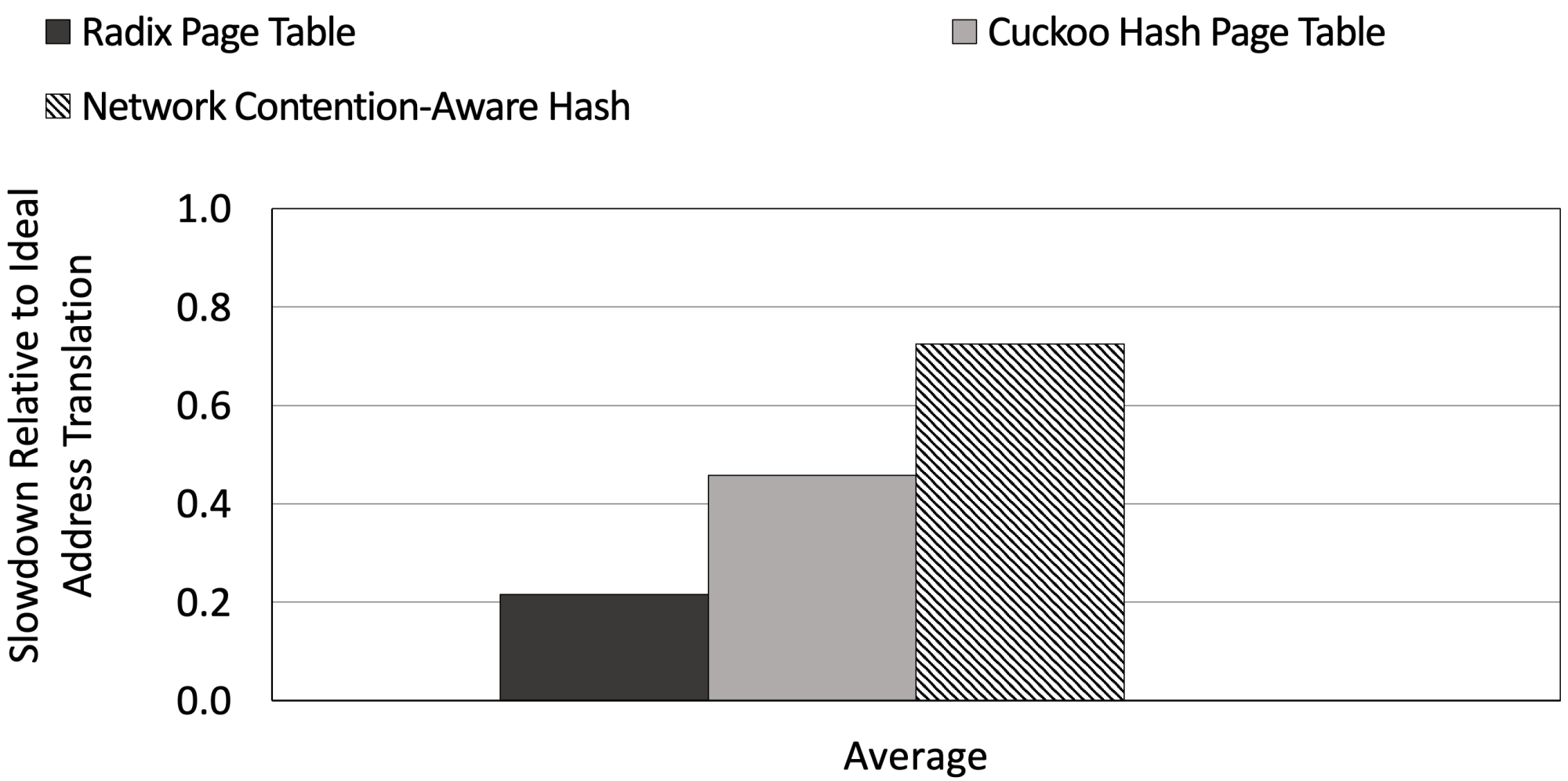


Performance Improvement

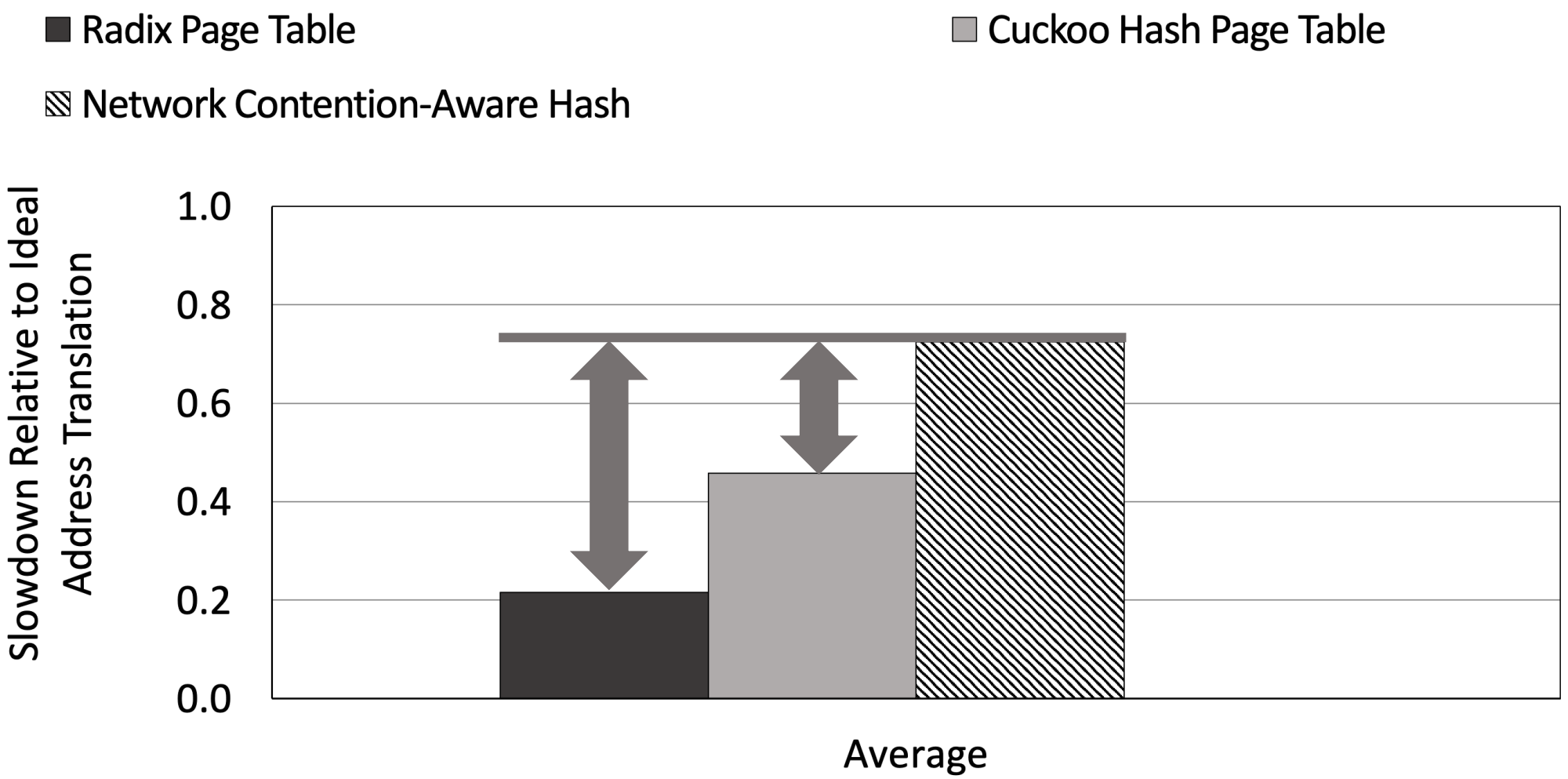


Huge performance overhead with radix and hash page table in PIM

Performance Improvement

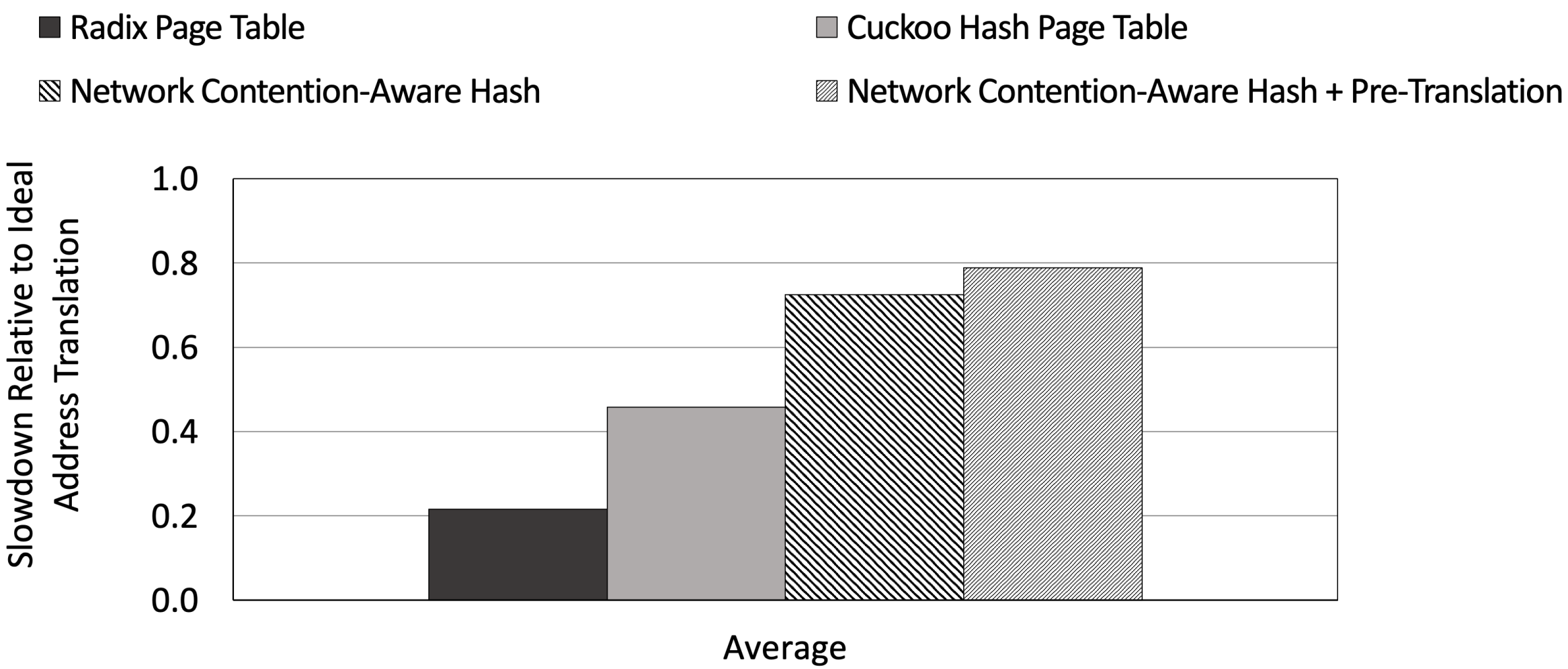


Performance Improvement

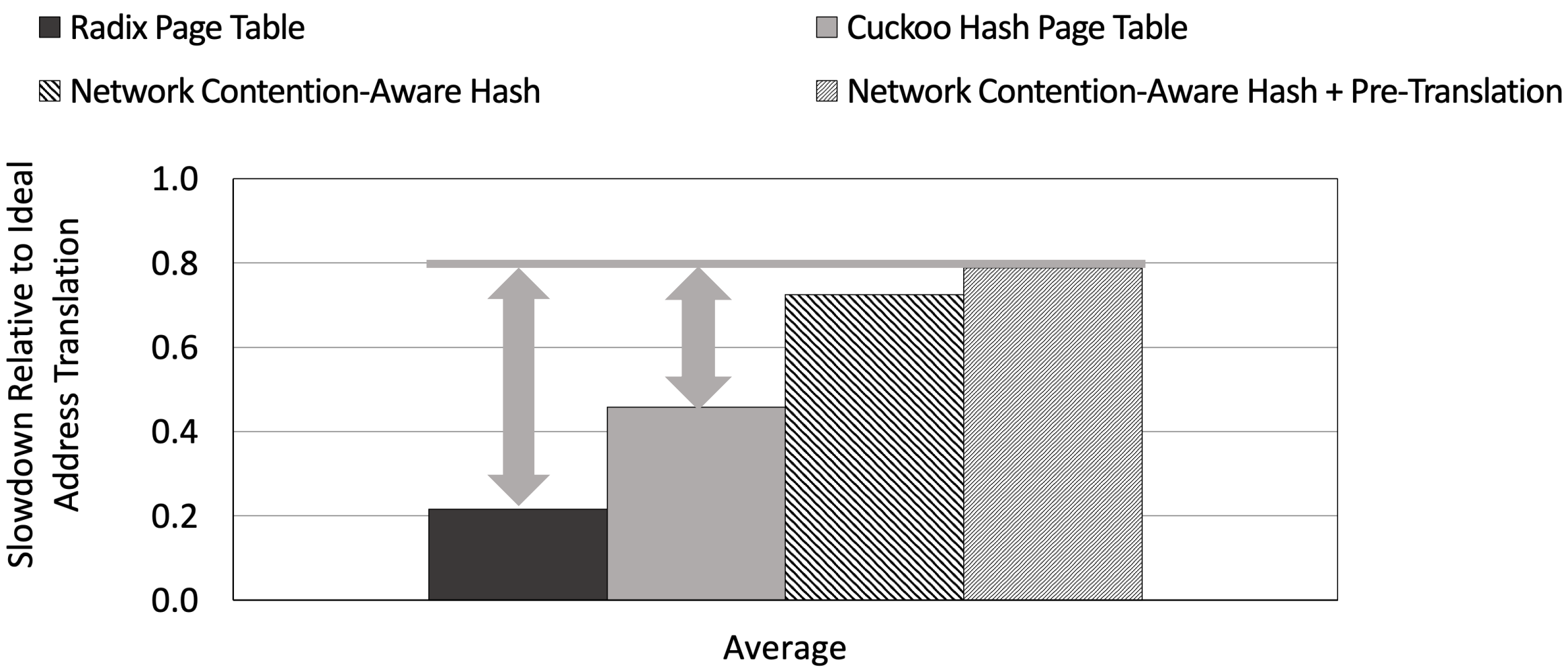


Network contention-aware hash achieves a speedup of 3.97× and 1.6× compared to radix and cuckoo hash page table

Performance Improvement

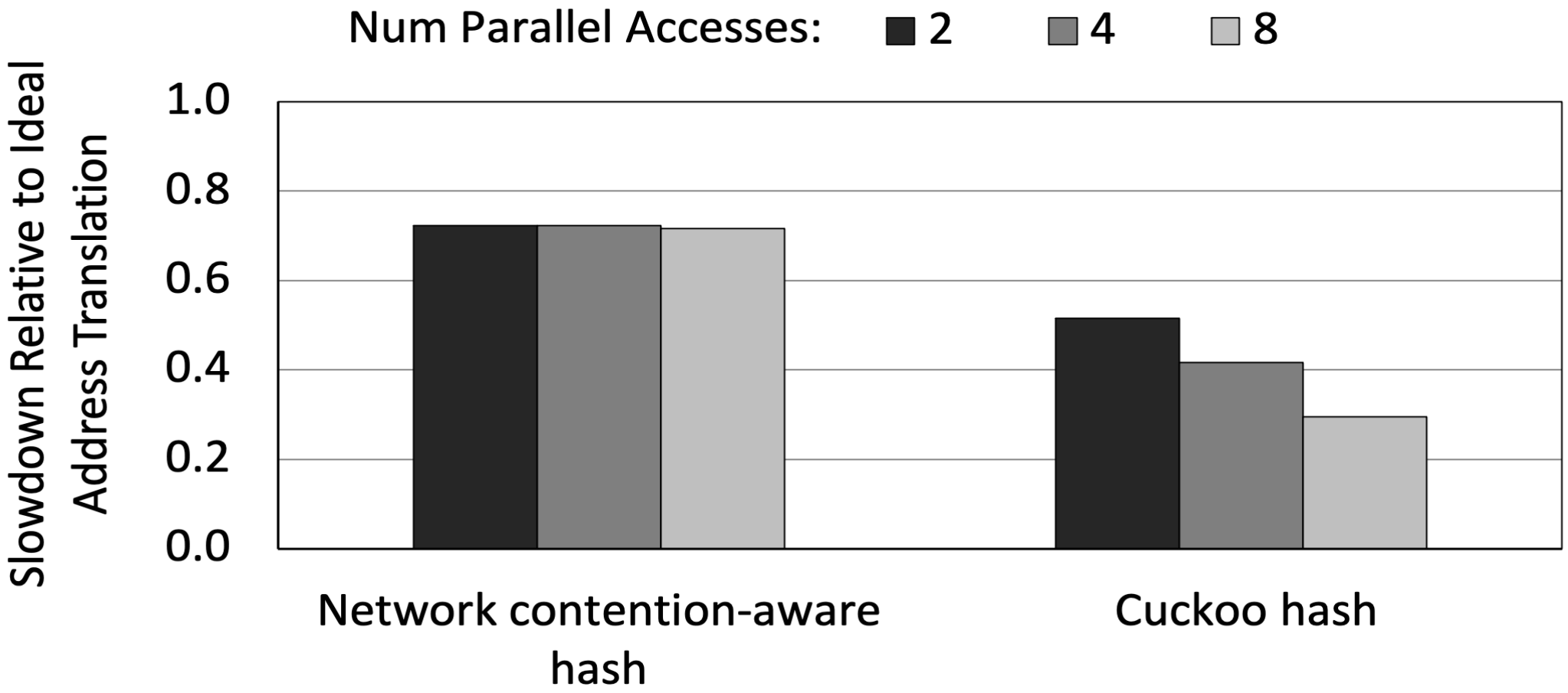


Performance Improvement

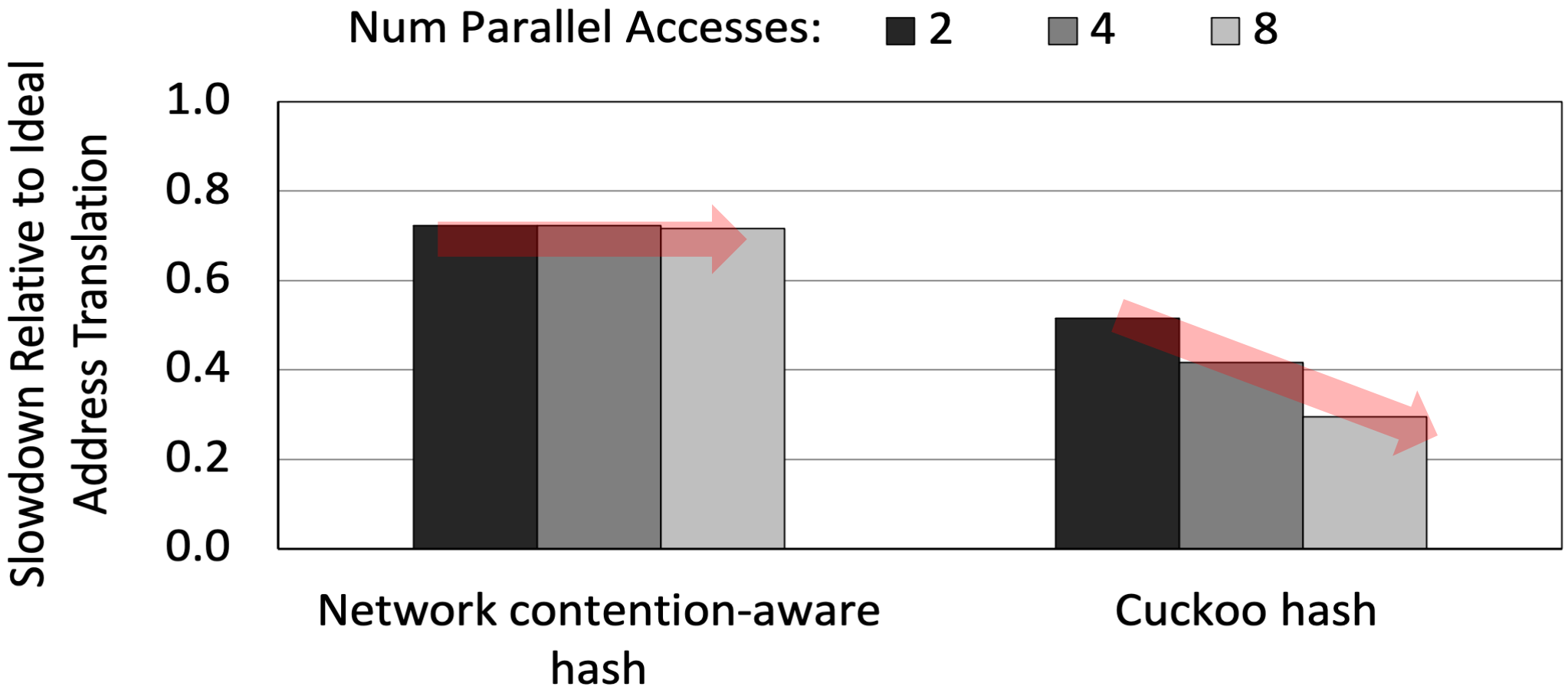


A total speedup of 4.4× and 1.7× is achieved compared to radix and cuckoo hash page table

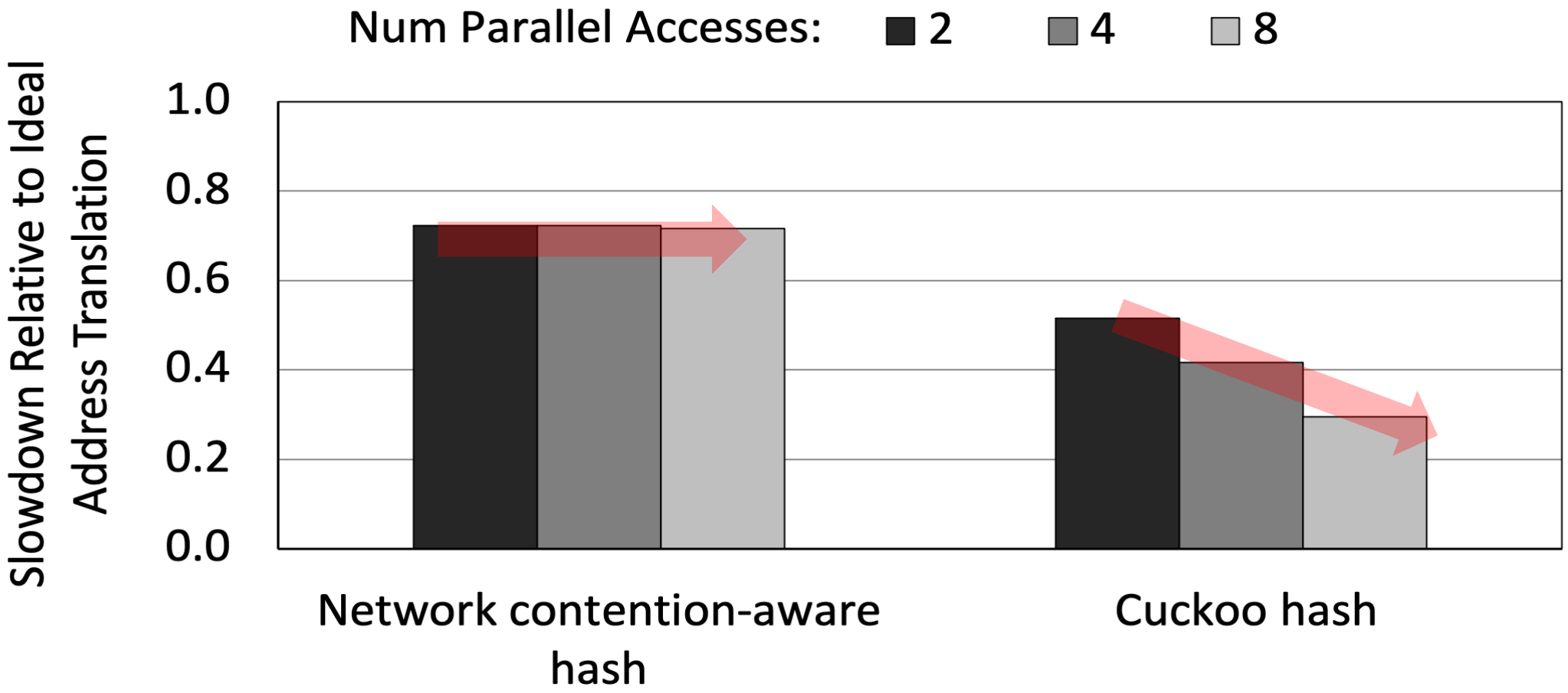
Sensitivity Results



Sensitivity Results

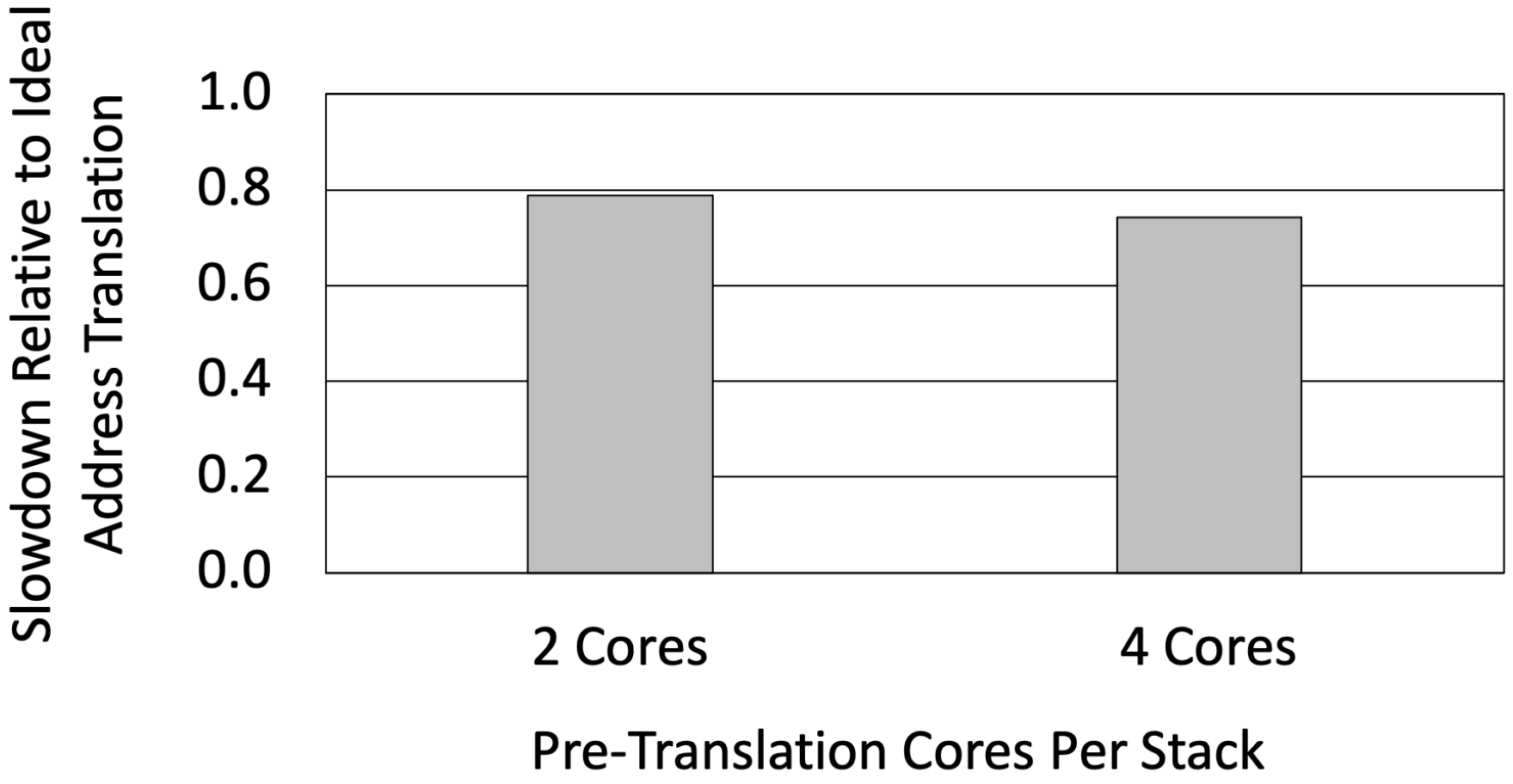


Sensitivity Results

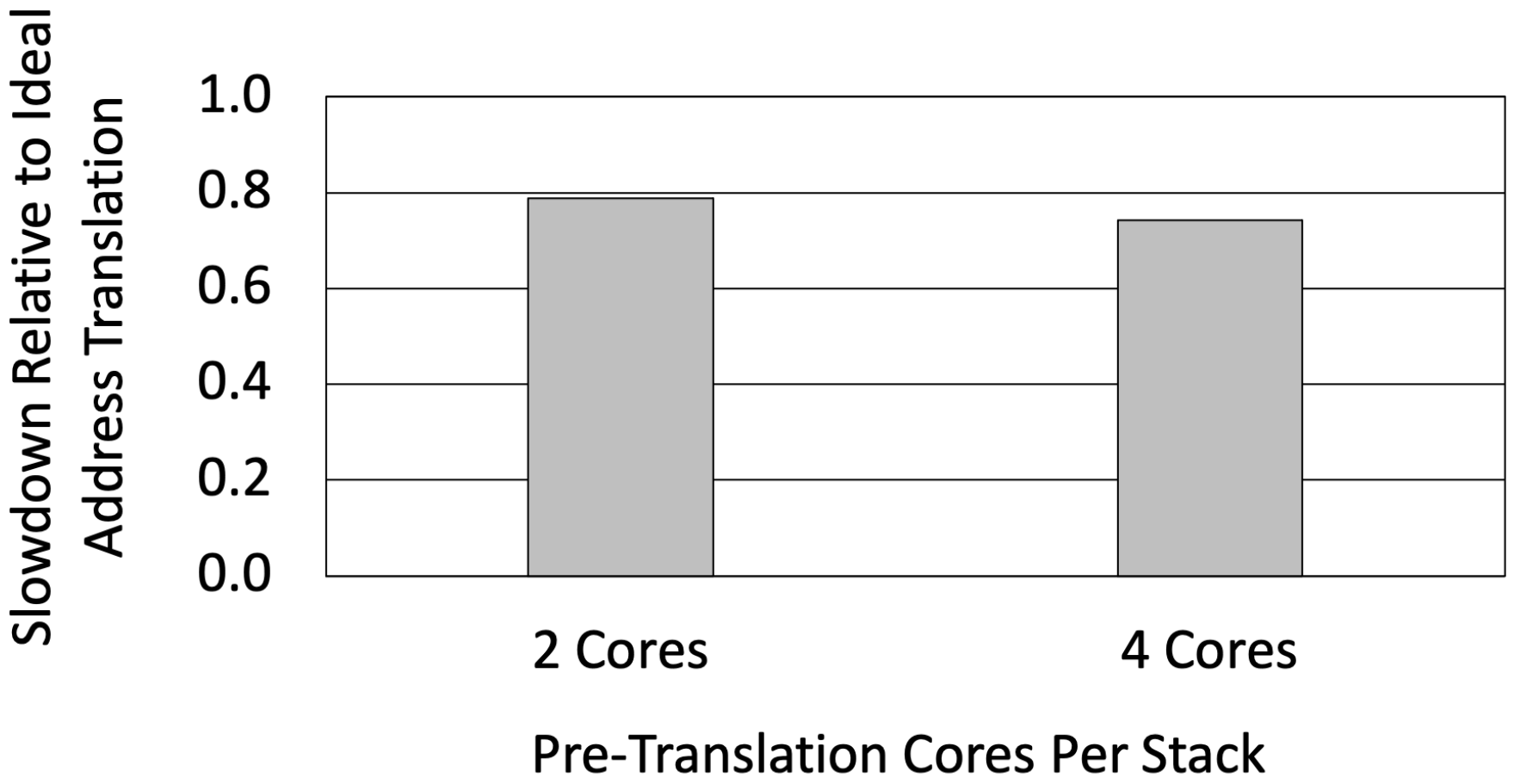


Network contention-aware hash scales well with minor performance degradation

Sensitivity Results



Sensitivity Results



2 cores is a good tradeoff between performance loss and pre-translation

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Conclusion

Multiple (PIM) stacks provide increased capacity for emerging data-intensive workloads

Running generalized applications divided between CPU and PIM is highly important

We propose address translation for multi-stack PIM running same application in CPU & PIM

Key Ideas:

- Network-contention-aware hash: Adapts cuckoo hash layout for multi-stack PIM system
- Pre-translation: Pre-translates addresses to avoid cross-stack page table walk accesses

Result: Provides 4.4x and 1.7x speedup compared to radix and cuckoo hash