Amel Fatima

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About me

I am a 3RD Year Ph.D. student pursuing my Ph.D. in Computer Engineering from the University of Virginia. I completed my masters as a Fulbright Scholar from the State University of New York at Buffalo. Currently, I am doing research targeting to solve the overhead of address translation in Processing in Memory (PIM) architectures.

Education

- **University of Virginia, Charlottesville, VA** August 2019

  Ph.D. in Computer Engineering, GPA 4.0/4.0 ***(Working as a Research Assistant in Shift Lab)***

  – Relevant Coursework: Computer Architecture.

- **State University of New York at Buffalo, NY** June 2019

  MS in Computer Science and Engineering, GPA 3.40/4.0 ***(Offered Tuition scholarship by the University and a Fulbright Scholar)***

  – Relevant Coursework: Intro to VLSI, Computer Architecture, Advanced Computer Architecture, Microelectronic Device Fabrication Lab and Theory, Computer Security, Algorithm for modern computing systems.

- **University of engineering and Technology Taxila, Pakistan** August 2016

  Bachelor of Engineering in Computer Engineering, GPA 3.43/4.0 ***(Gilgit Baltistan student scholarship for full tuition waiver)***

Technical Skills

- **Languages:** C, C++, Matlab, Python, Assembly Language (MIPS), Arduino IDE
- **HDL:** VHDL, Verilog
- **EDA and Simulation Tools:** Cadence Virtuoso-XL, Xilinx Vivado, Gem5 Simulator, Zsim, MATLAB, PIN instrumentation tool, Ramulator (DRAM simulator).
- **Skill Set:** Full-Custom and Semi-Custom IC Layout, Verification Checks involving Debugging DRC and LVS match, Placement and Routing of blocks, RTL Analysis, Static Timing Analysis,FPGA development with Basys 3 Board, Test bench creation, Architectural Simulation and benchmark of various computational Systems using Gem5 Simulator, Fabrication Lab skills (Photolithography, PECVD, Etching, E-Beam, Ellipsometer, Profilometer)

Academic Projects

- **Design of a 16-Bit RISC Processor** Spring 2018

  Technologies: VHDL, Vivado

  – Implemented a single cycle RISC Processor with 512Bytes Instruction and 512Bytes Data Memory
  – With 16 16-bit Registers
  – Designed my own 16 bit ISA of 24 instructions. Generated RTL and Timing Simulation using 100kHz clk.

- **Design of 8X8 Vedic Multiplier using Kogge Stone Adder** Fall 2017

  Technology: Cadence (TSMC 180nm Technology)

  – Implemented a very fast response-time 8-bit multiplier with low propagation delay, using Radix-2 Algorithm
  – Designed and Verified the Circuit layout with DRC LVS Check.

Various System Architecture simulations and Benchmarks using gem5 Fall 2018

– Computed the MPKI value of various cache levels with different parameters running ALPHA ISA in Gem5 simulator using Ruby Memory Module and spec2006 benchmark using various workloads like namd, leslie3d, bzip2, lmb

Fabrication lab projects Fall 2018

– Fabricated a design on Si surface with 5nm SiO_1 layer using PECVD and verifying the thickness using Ellipsometer
– Fabricated a design on Si surface with 75nm Ti layer using E-Beam, lift-off and verifying the thickness using Profilometer

- **Implementation of 8-Way Set Associative Cache** Fall 2018

  Technologies: Verilog, Vivado

  – Cache Size: 128KB, Address bits: 32, Cache Block Size: 64B. I am also implementing the Cache Controller

- **Implementation of Low Power 8X4 8T SRAM Cell with Dynamic Feedback Control using AVLG Technique** Fall 2018

  Technologies: Cadence

  – I am trying to simulate an 8T-SRAM cell using Adoptive Voltage Level Ground technique which will yield better performance, low power consumption and less leakage power.
  – It would lift the ground potential of the circuit to reduce the power consumption of the 8T SRAM Cell circuit.

Leadership Roles

Member Of GBSO (Gilgit Baltistan Student Organization)

– Helping students from rural areas like my hometown Gilgit Baltistan to adjust to the new city environment of my undergrad institute
– Counseling students for overcoming cultural shock and dealing with depression.

Co-Founder of ACM student chapter UET, Taxila

– I initiated a student chapter of ACM (international society for computer engineers) in UET, Taxila along with my 2 friends.

- I was also the Finance secretary of the society

Member Of Umeed-e-Subah

- I was a member of “Umeed-e-Subah” which helped underprivileged students with their basic educational needs.