# Chips-2.0 Demo for NEXYS3 Development Card

**Author:** Jonathan P Dawson

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email: chips@jondawson.org.uk Revised: Amer Al-Canaan, June 2014

email: amer c1@hotmail.com

This project is intended to demonstrate the capabilities of the Chips-2.0 development environment. The project is targets the Xilinx Spartan 6 device, and more specifically, the Digilent NEXYS3 development platform. The demo implements a TCP/IP socket interface, and a simple web application. This demonstration has been tested on a Debian Linux.

### **Dependencies**

- Xilinx ISE 12.0 or later (Webpack edition is free)
- Python 2.7 or later (but not Python 3)
- Chips-2.0 (Included)
- Digilent NEXYS3 Spartan 6 Development Kit.
- Digilent ADEPT2 utility
- git

#### Install

Clone the git the repository with git:

```
$ git clone https://github.com/amerc/phimii.git
$ cd Chips-Demo
$ git submodule init
$ git submodule update
```

# **Chips Compile**

To compile the c code in chips, issue the following command in the project folder:

```
$ scripts/nexys3.py compile
```

## **Build in ISE**

Edit the Xilinx variable in the *scripts/user\_settings* to point to the Xilinx ISE install directory. Then build the design using the following command:

```
$ scripts/nexys3.py build
```

# **Download to Nexys3**

Power up the Nexys3, and connect the JTAG USB cable to your PC. Run the download command:

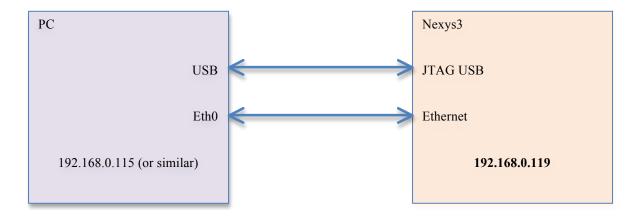
\$ scripts/atlys.py download

Or to do the 3 steps in a single command:

\$ scripts/nexys3.py all

## **Setup and Test**

Connect the Ethernet port to NEXYS3, using an Ethernet cable.



Using the following script, configure Ethernet port (eth0) with IP address 192.168.0.115 and subnet mask 255.255.255.0. Turn off TCP Window Scaling and TCP time stamps:

\$ scripts/configure\_network

Verify connection using ping command:

Connect to 192.168.1.1 using your favourite browser.

