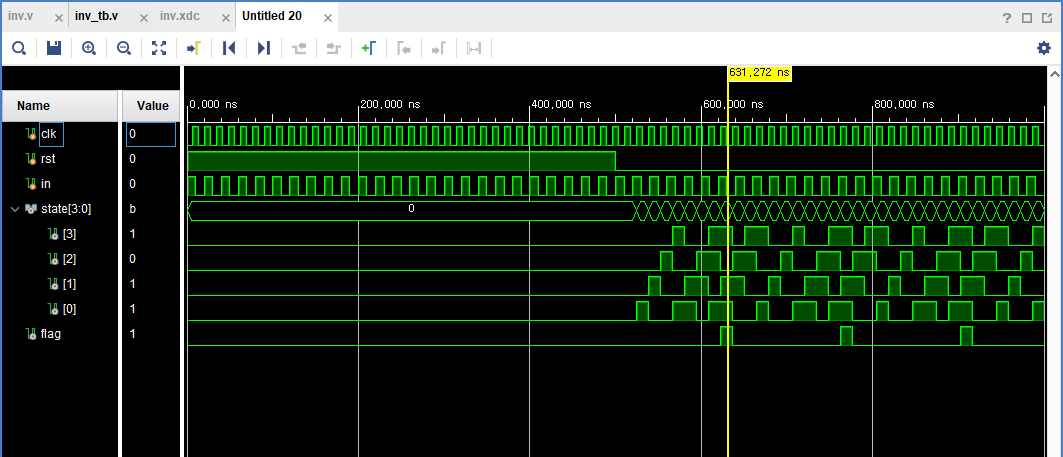
14주차 결과보고서

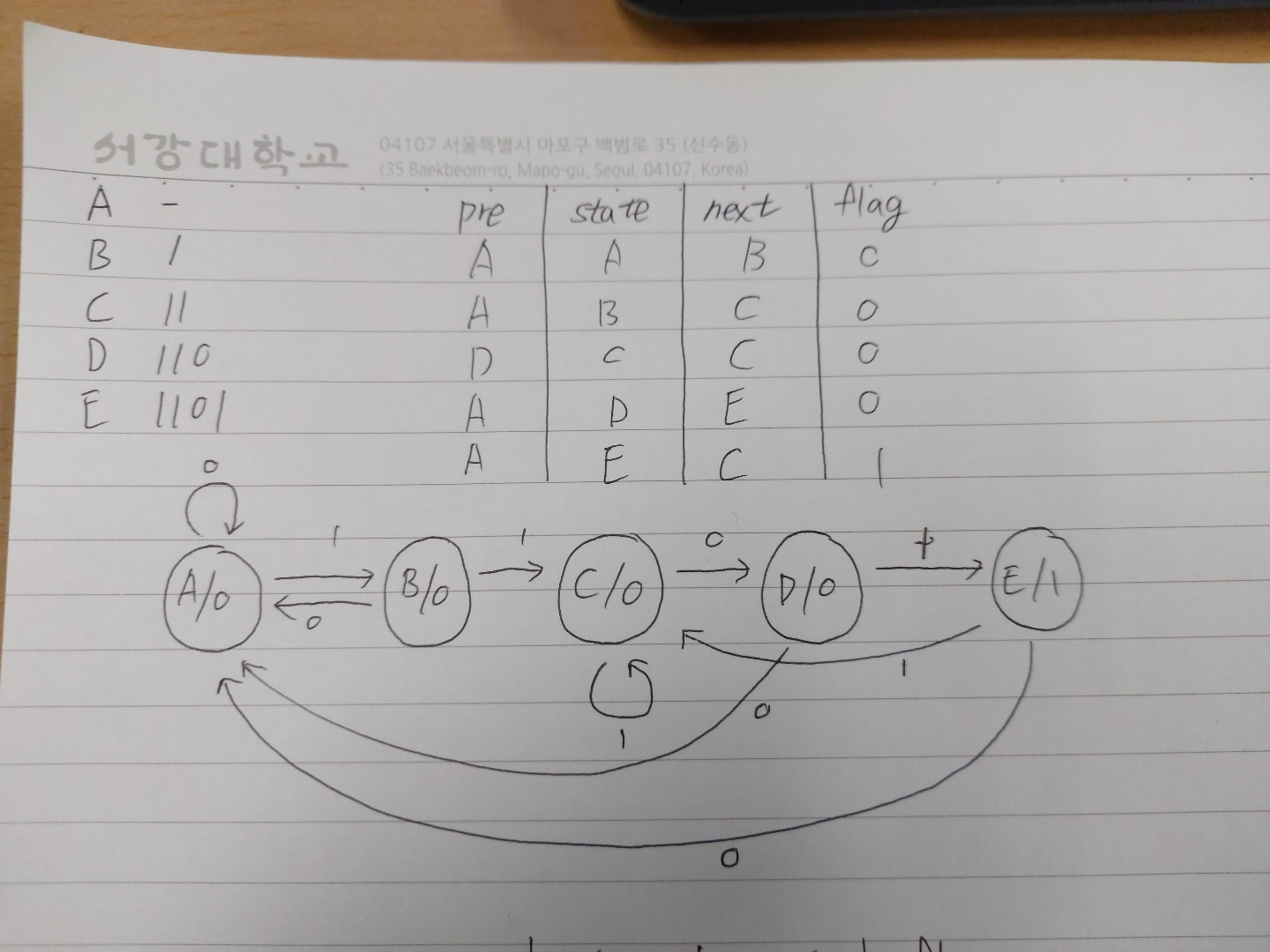
전공 : 컴퓨터공학과 학년 : 2학년 학번 : 20201597 이름 : 신동준

1. **Sequence Detector 1101 Moore machine 구현**

**(verilog source, simulation 결과(testbench 파일 작성시 output 제대로 나오도록 조정), 상태도, 상태표 작성)**

|  |
| --- |
| `timescale 1ns / 1ps  module inv(  clk,  rst,  state,  in,  flag  );  input clk,rst,in;  output state,flag;  reg[3:0] state = 4'b0000;  reg flag = 0;  parameter [3:0] s0=4'b0000;  parameter [3:0] s1=4'b0001;  parameter [3:0] s2=4'b0011;  parameter [3:0] s3=4'b0110;  parameter [3:0] s4=4'b1101;    always @(posedge clk)  begin  if (rst)  begin  state = s0;  flag <= 0;  end  else  begin  state <= state << 1;  state[0] <= in;  if(state == s4)  begin  flag <= 1;    end  else  begin  flag <= 0;  end  end    end    endmodule |





1. **Sequence Detector 10101을 구현(mealy, moore machine 모두)**

**상태도(State Table) 및 상태표(State Diagram) 작성.**

**Verliog Code 및 Simulation 결과 작성.**

**<moore>**

|  |
| --- |
| `timescale 1ns / 1ps  module inv(  clk,  rst,  state,  in,  flag  );  input clk,rst,in;  output state,flag;  reg[4:0] state = 5'b00000;  reg flag = 0;  parameter [4:0] s0=5'b00000;  parameter [4:0] s4=5'b10101;    always @(posedge clk)  begin  if (rst)  begin  state = s0;  flag <= 0;  end  else  begin  state <= state << 1;  state[0] <= in;  if(state == s4)  begin  flag <= 1;  end  else  begin  flag <= 0;  end  end    end    endmodule |

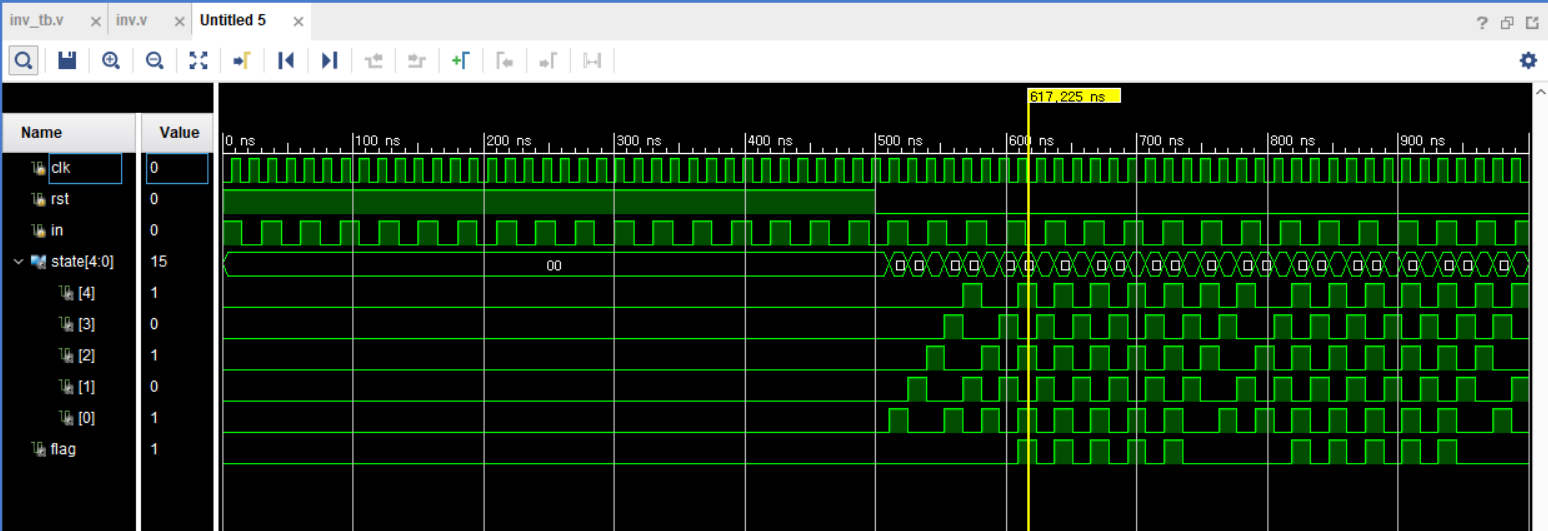


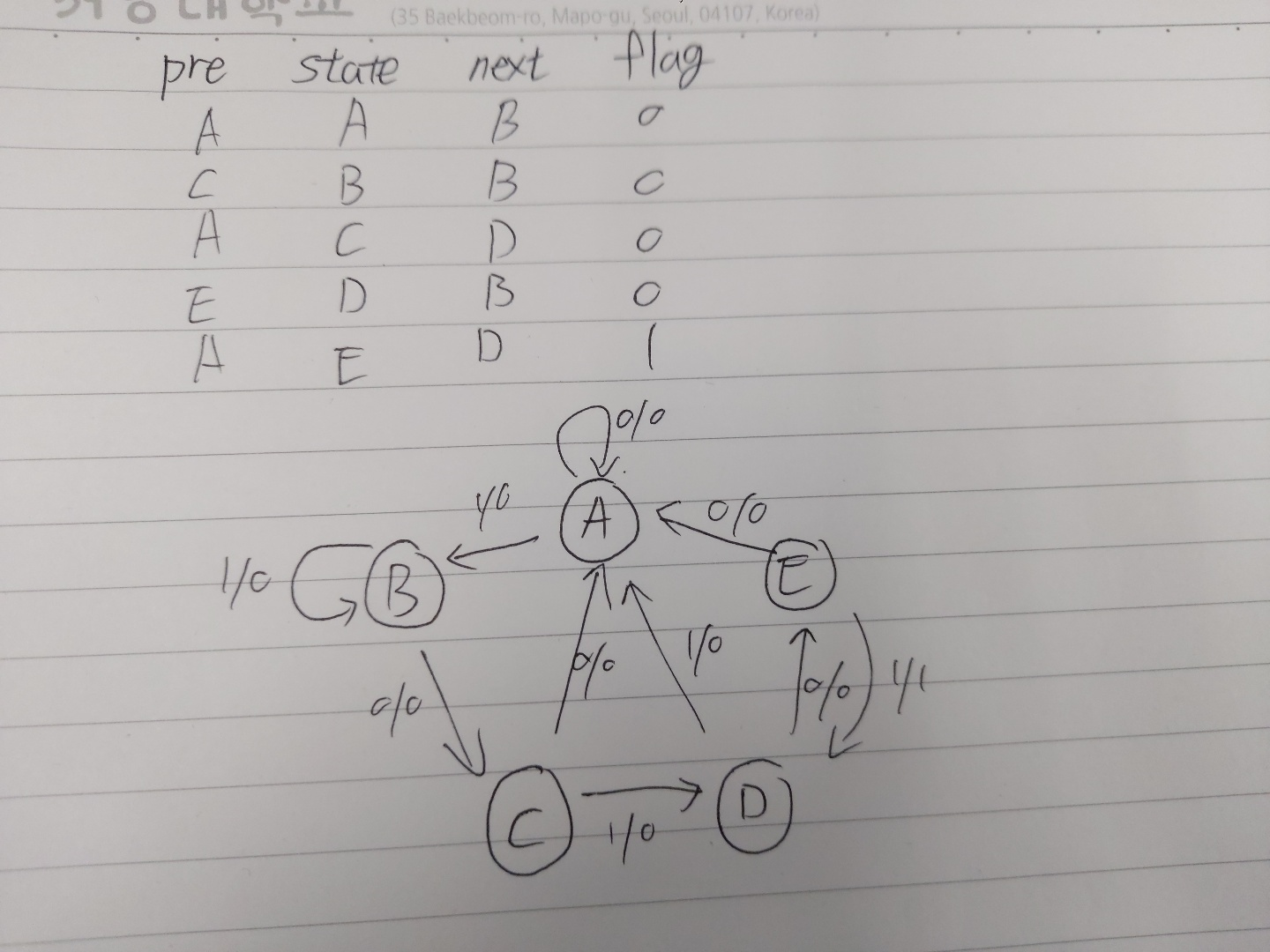
텍스트, 화이트보드이(가) 표시된 사진

자동 생성된 설명

**<mealy>**

|  |
| --- |
| `timescale 1ns / 1ps  module inv(  clk,  rst,  state,  in,  flag  );  input clk,rst,in;  output state,flag;  reg[4:0] state = 5'b00000;  reg flag = 0;  parameter [4:0] s0=5'b00000;  parameter [4:0] s4=5'b01010;    always @(posedge clk)  begin  if (rst)  begin  state = s0;  flag <= 0;  end  else  begin  state <= state << 1;  state[0] <= in;  if(state == s4 && in == 1)  begin  flag <= 1;  end  else  begin  flag <= 0;  end  end    end    endmodule |



****