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Data Sheet | October 2013

N-Channel Logic Level Power MOSFET 100 V, 12 A, 200 mΩ

These are N-Channel enhancement mode silicon gate power field effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V to 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

Formerly developmental type TA09526.

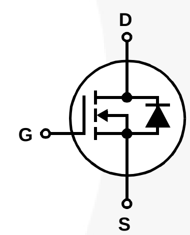
Ordering Information

PART NUMBER	PACKAGE	BRAND
RFP12N10L	TO-220AB	F12N10L

Features

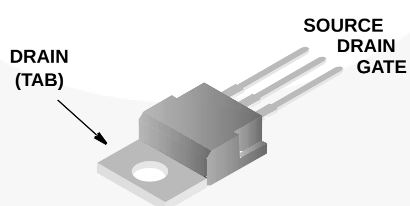
- 12A, 100V
- $r_{DS(ON)} = 0.200\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards

Symbol



Packaging

JEDEC TO-220AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFP12N10L	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	100	V
Drain to Gate Voltage (R_{GS} = 1MΩ) (Note 1)	V_{DGR}	100	V
Continuous Drain Current	I_D	12	A
Pulsed Drain Current (Note 3)	I_{DM}	30	A
Gate to Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation	P_D	60	W
Above $T_C = 25^oC$, Derate Linearly		0.48	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		100	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$ (Figure 7)		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80V$		-	-	1	µA
		$V_{GS} = 0V$	$T_C = 125^oC$	-	-	50	µA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = 10V$, $V_{DS} = 0V$		-	-	100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 12A$, $V_{GS} = 5V$ (Figures 5, 6)		-	-	0.200	Ω
Input Capacitance	C_{ISS}	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1MHz (Figure 8)		-	-	900	pF
Output Capacitance	C_{OSS}			-	-	325	pF
Reverse-Transfer Capacitance	C_{RSS}			-	-	170	pF
Turn-On Delay Time	$t_{d(ON)}$	$I_D = 6A$, $V_{DD} = 50V$, $R_G = 6.25\Omega$, $V_{GS} = 5V$ (Figures 9, 10, 11)		-	15	50	ns
Rise Time	t_r			-	70	150	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	100	130	ns
Fall Time	t_f			-	80	150	ns
Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-220				2.083	oC/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	$I_{SD} = 6A$	-	-	1.4	V
Diode Reverse Recovery Time	t_{rr}	$I_{SD} = 4A$, $dI_{SD}/dt = 50A/\mu s$	-	150	-	ns

NOTES:

2. Pulsed: pulse duration = 80µs max, duty cycle = 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

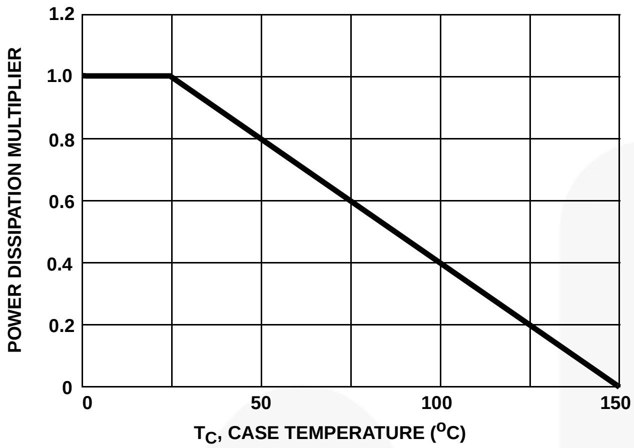


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

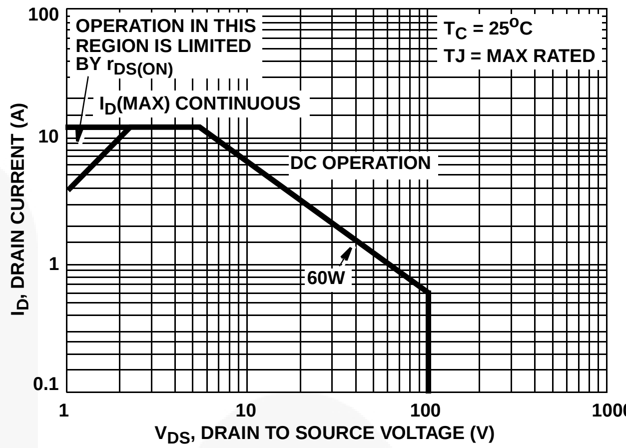


FIGURE 2. FORWARD BIAS OPERATING AREA

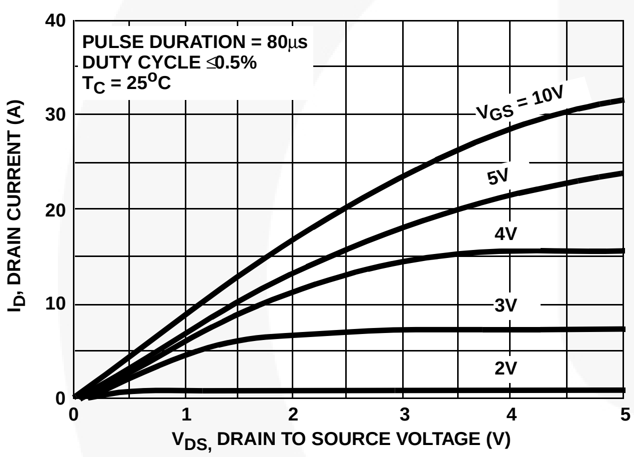


FIGURE 3. SATURATION CHARACTERISTICS

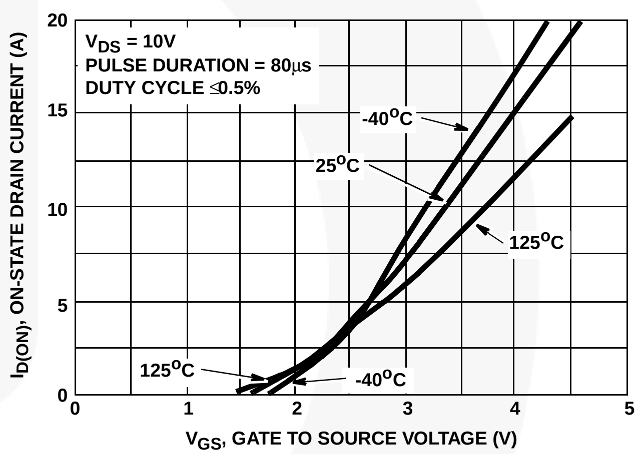


FIGURE 4. TRANSFER CHARACTERISTICS

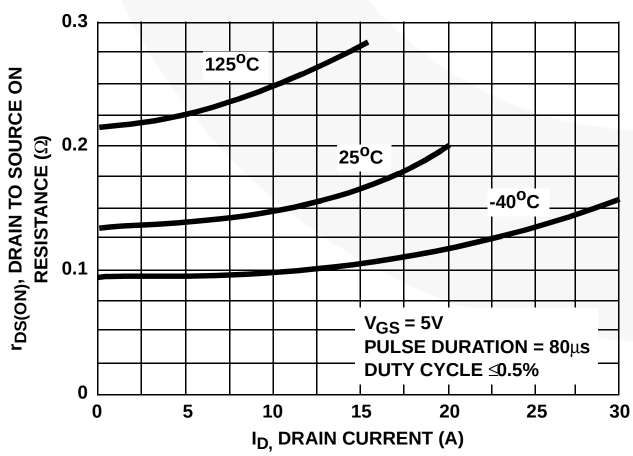


FIGURE 5. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

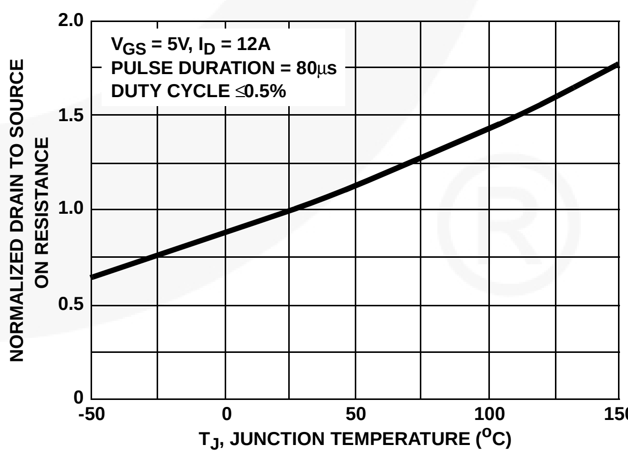


FIGURE 6. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

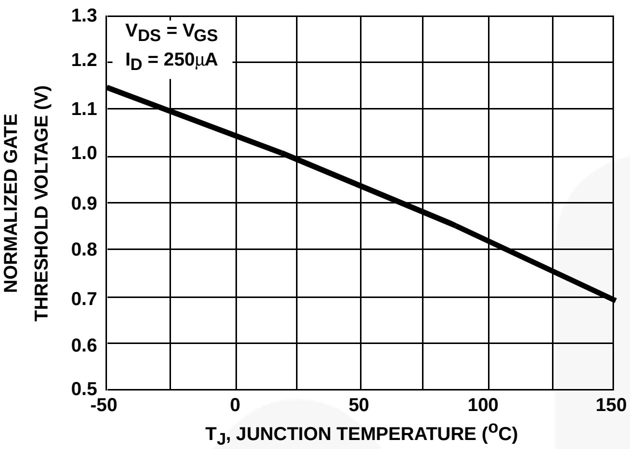


FIGURE 7. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

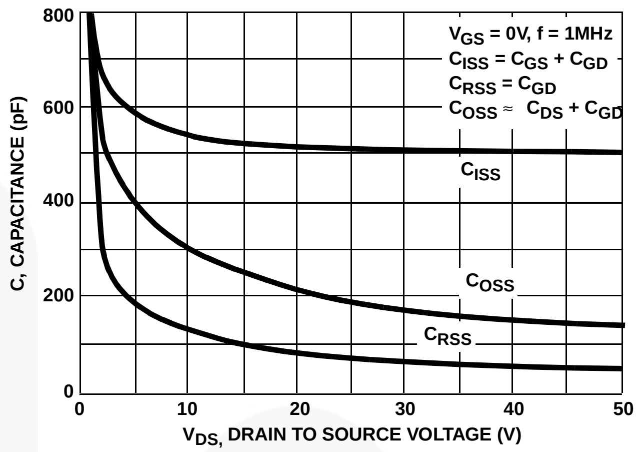
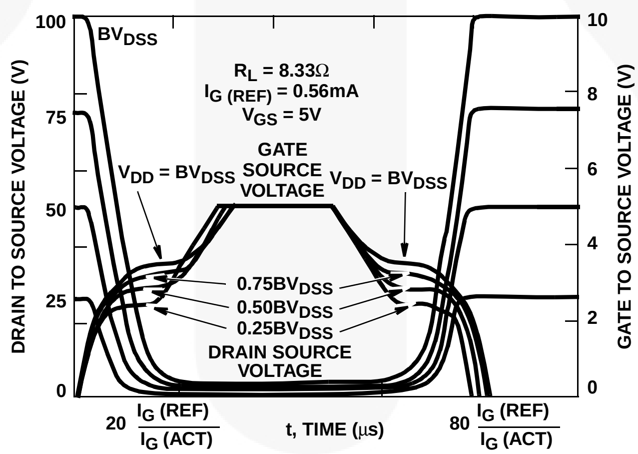


FIGURE 8. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Applications Notes AN7254 and AN7260

FIGURE 9. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

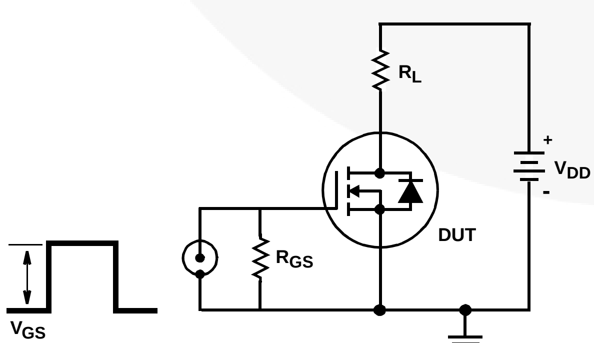


FIGURE 10. SWITCHING TIME TEST CIRCUIT

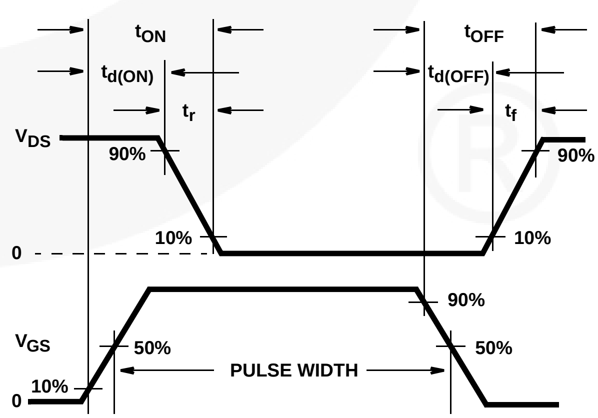


FIGURE 11. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

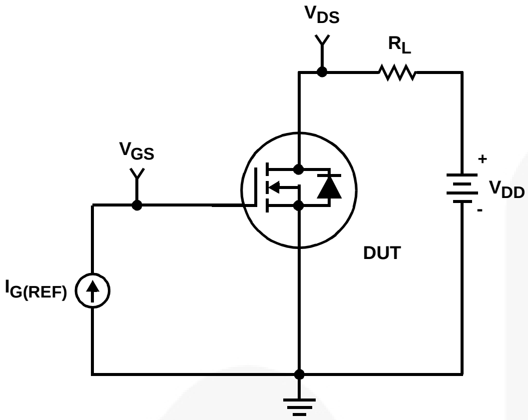


FIGURE 12. GATE CHARGE TEST CIRCUIT

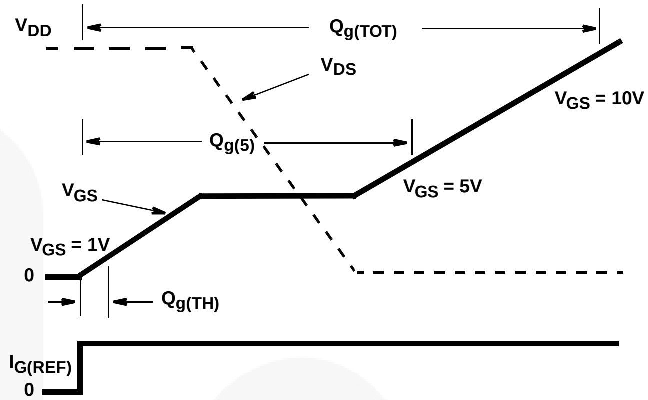


FIGURE 13. GATE CHARGE WAVEFORMS

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