Microprocessor
(Unit-2 :: Lectures – 3 & 4)

(BEI – I/II & BCT – II/II)

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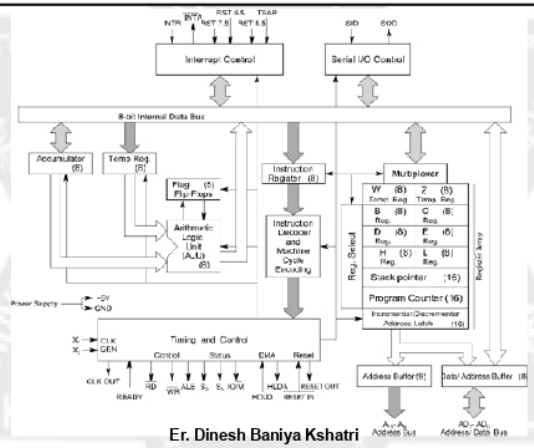
8085 Internal Architecture (Block Diagram)



8085 Internal Architecture (Arithmetic Logic Unit)

- ALU performs the actual arithmetic and logic operations
  - Operates on two 8-bit numbers
  - Examples of arithmetic operations: Addition, Subtraction
  - Examples of logic operations: AND, OR, XOR
- Uses data from memory or input ports and Accumulator to perform various operations
- It stores the result of an operation in the Accumulator

8085 Internal Architecture (General Purpose Registers)

- There are six general-purpose registers
  - Registers named as: B, C, D, E, H, L
  - Each register has a capacity of 8-bits
- Certain registers can be combined to form register pairs:
  - Valid register pairs are: BC, DE, HL
  - Can be used to hold 16-bit numbers

8085 Internal Architecture
(Accumulator)

- It is an 8-bit register
- Supplies data to ALU for computation
- Stores result generated by the ALU
- Is used to read data from input ports, and send data to output ports
- Is also called register A

8085 Internal Architecture
(Temporary Registers)

- There are two temporary 8-bit registers
  - Registers (W) and (Z)
- They are not accessible to programmers
- Used internally by the processor
  - To supply numbers to the ALU
  - To temporarily hold intermediate results

8085 Internal Architecture
(Flag Register) – [1]

- It consists of five flip-flops
- They are set or reset after an operation in the ALU and according to the conditions of the result

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	Z	X	AC	X	P	X	CY

8085 Internal Architecture
(Flag Register) – [2]

- **Carry Flag**:
  - If an ALU operation generates a carry, its status will be 1, otherwise 0
- **Zero Flag:**
  - If an ALU operation results in all zeros, its status will be 1, otherwise 0
- **Sign Flag:**
  - If an ALU operation results in the most significant bit (msb) of the result to be 1, then its status will be 1, otherwise 0

8085 Internal Architecture
(Flag Register) – [3]

- **Parity Flag:**
  - If an ALU operation generates a result having an even number of ones then its status will be 1, otherwise 0
- **Auxiliary Carry Flag:**
  - If an ALU operation causes a carry to be generated from the lower 4-bits to the upper 4-bits, its status will be 1, otherwise 0

8085 Internal Architecture
(Instruction Register & Instruction Decoder)

- Instruction register is an 8-bit register
- It receives operation codes (op-codes) of the current instruction from memory
- It passes the op-code to the instruction decoder
  - Allows the microprocessor to know about the operation to be performed

8085 Internal Architecture
(Stack Pointer - SP)

- It is a 16-bit register
- Used to point to a special location in memory called the stack
  - Stack follows the Last-in-First-out (LIFO) principle
- Start of the stack is defined by loading a 16-bit address into the stack pointer

8085 Internal Architecture
(Program Counter - PC)

- It is a 16-bit register
- It points to the memory location (holds the memory address) from which the next instruction is to be fetched
- Once an instruction has been fetched, the PC is incremented by one to point to the next instruction

8085 Internal Architecture
(Address & Data Bus)

- 8085 has 16 lines that are used as the address bus
- 8085 has 8 lines that are used as the data bus

- The 16 lines are split into two segments:
  - A_{15} - A_8 (High-order Address Bus, Unidirectional)
  - AD_7 - AD_0 (Low-order Address Bus & Data Bus, Bidirectional)

- Low-order Address / Data bus is time-multiplexed
  - Carries address bits or data bits at different instants of time

8085 Timing and Control Unit
(Clock Signals)

- **X1, X2 (Inputs):**
  - Are connections for external crystal oscillator
  - External frequency is divided by 2 to give the internal operating frequency

- **CLK OUT (Output):**
  - Is used to output a periodic signal
  - Can be used as a clock signal for peripheral devices

8085 Timing and Control Unit
(Control and Status Signals) – [1]

- $\overline{RD}$ **(Output):**
  - It represents the Read signal
  - Used when obtaining data from selected memory locations or input devices

- $\overline{WR}$ **(Output):**
  - It represents the Write signal
  - Used while sending data to selected memory locations or output devices

8085 Timing and Control Unit
(Control and Status Signals) – [2]

- **IO/** $\overline{M}$ **(Output):**
  - Differentiates between I/O and memory operations
  - When it is high, it indicates an I/O operation
  - When it is low, it indicates a memory operation

- **ALE (Output):**
  - Stands for Address Latch Enable
  - Used to activate an address latch
  - The latch stores the address bits ($A_7 – A_0$) from the lower half of the multiplexed address / data bus ($AD_7 – AD_0$)

8085 Timing and Control Unit
(Control and Status Signals) – [3]

- **S_1 and S_0 (Outputs):**
  - They represent status signals
  - Informs about internal operations of the processor
  - The truth table for the status signals is given below:

S1	S0	
0	0	HALT
0	1	WRITE
1	0	READ
1	1	FETCH

8085 Timing and Control Unit
(Peripheral Initiated Signals)

- **HOLD (Input):**
  - Indicates that a peripheral is requesting the use of the system bus of the processor
- **HLDA (Output):**
  - It stands for Hold Acknowledge
  - Processor informs peripherals regarding the reception of a hold request
- **READY (Input):**
  - Is used by a slow-responding peripheral device to inform the microprocessor when it is ready to send or accept data

8085 Timing and Control Unit
(Reset Signals)

- **$\overline{\text{RESET IN}}$ (Input):**
  - The program counter is set to zero
  - Buses are tri-stated (kept in high-impedance state)
- **RESET OUT (Output):**
  - Is used to inform peripheral devices that the processor is being reset

8085 Interrupt Control Unit – [1]

- **INTR (Input):**
  - It stands for interrupt request
  - It has the lowest priority amongst all interrupts
  - It can be enabled / disabled via software
- **$\overline{INTA}$ (Output):**
  - It stands for Interrupt Acknowledge
  - Is used by the processor to inform an interrupting peripheral regarding the reception of its interrupt request

8085 Interrupt Control Unit – [2]

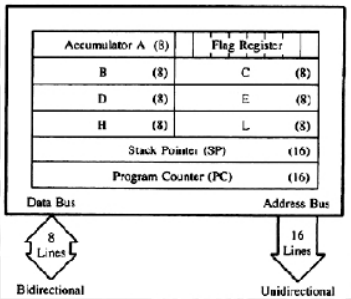
- **RST 7.5, RST 6.5, RST 5.5 (Inputs):**
  - They represent restart Interrupts
  - Activate subroutines from predefined memory locations
  - Priority hierarchy is: RST7.5 > RST6.5 > RST 5.5
  - These interrupts have higher priority than the INTR
  - They can be masked / unmasked via software
- **TRAP (Input):**
  - Activates a subroutine from a predefined memory location
  - It is non-maskable (cannot be enabled / disabled by software)
  - It has the highest priority amongst all interrupts

8085 Serial I/O Control Unit

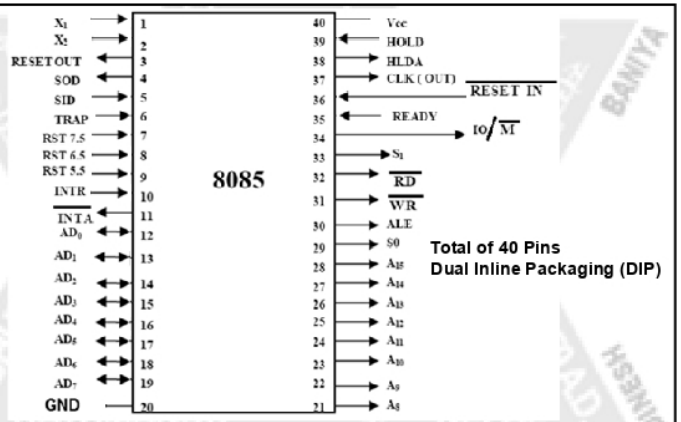
- **SID (Input):**
  - Stands for serial input data
  - Used by microprocessor to obtain data bit-by-bit from peripheral devices
- **SOD (Output):**
  - Stands for serial output data
  - Used by microprocessor to send data bit-by-bit to peripheral devices

8085 Programmer's Model

- Includes the registers required for programming the 8085:
  - Six general purpose 8-bit registers (B, C, D, E, H, L)
  - One 8-bit accumulator (A)
  - One 8-bit flag register (F)
  - One 16-bit Stack Pointer (SP)
  - One 16-bit Program counter (PC)

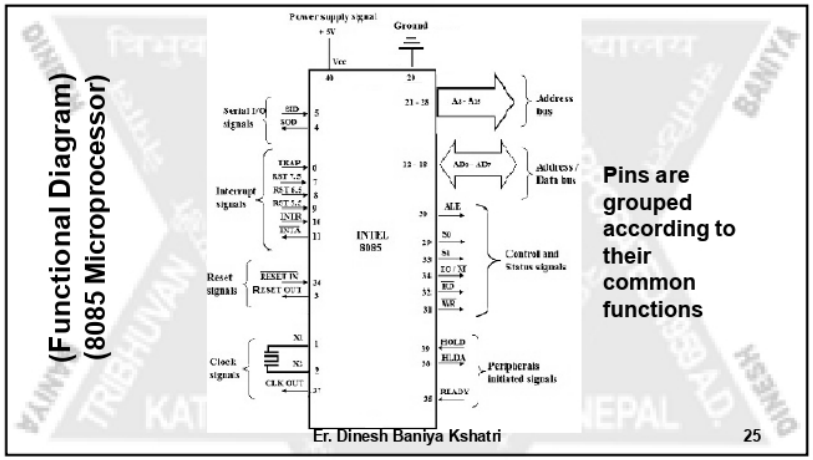


(Pin Diagram) (8085 Microprocessor)



Total of 40 Pins
Dual Inline Packaging (DIP)

(Functional Diagram) (8085 Microprocessor)



Pins are grouped according to their common functions