TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
THAPATHALI CAMPUS

Instrumentation I

BEX, BCT, BEL

Chapter 5: Analog to Digital and Digital to Analog Conversion

Er. Umesh Kanta Ghimire

Department of Electronics & Computer Engineering

IOE ,Thapathali Campus

ukg@tcioe.edu.np

+977-9843082840

13 November , 2020

ANALOG TO DIGITAL & DIGITAL TO ANALOG CONVERSIONS [6 hrs./10 Marks]

5.1 Analog signal and Digital signal

5.2 Digital to Analog convertors - weighted resistor type, R-2R ladder type, DAC Errors

5.3 Analog to Digital convertors - successive approximation type, ramp type, dual ramp type, flash type, ADC errors

Analog signal and Digital signal

Analog Signals

- Signals that vary continuously throughout a defined range.
- Representative of many physical quantities, such as temperature and velocity.
- Usually a voltage or current level.

Digital Signals

- Signals that take on specific values only.
- Required for operation with digital logic.
- A representative of physical quantities by a series of binary numbers.

Most physical quantities are analog in nature. Almost all sensors have analog outputs. Due to advancements of digital signal processing, most of data processing is accomplished by digit computers. The data processed by digital computers are again required to be connected to analog form.

- Generally, following steps are followed in digital processing:
  a. Convert real world analog inputs to digital forms
  b. Process digital information
  c. Convert digital output back to real world analog form
- The process of changing analog input to equivalent digital form is accomplished using analog to digital converter (ADC).
- The process of changing digital signal to equivalent analog form is accomplished using digital to analog converter (DAC).

Digital to Analog Conversion

- It is defined as the process of conversion of digital to its equivalent analog signal
- It is an important interface process for make application
- The device which performs digital to analog is known as Digital to Analog Converter or DAC
- It is a decoding device
- Analog output is dependent upon reference voltage V_{Ref} as well as soon a particular digital combination connected as input to the given DAC
- If we connect a low pass filter at the DAC output then step changes can be smoothed out
- A DAC is used to control the device like motor, furnace, robot, electromechanical devices, CRO, X/Y strip chart recorder etc
- In fact DAC has endless range of application
- There are two types of DAC
    1) Weighted Resistor Network (WRN) DAC
    2) R-2R ladder Network DAC

A decimal equivalent of a binary number in an n bit system can be represented by:

$$N = d_{n-1}2^{n-1} + d_{n-2}2^{n-2} + d_{n-3}2^{n-3} + \cdots + d_1 2^1 + d_0 2^0$$

Consider a four bit system having full range E_R ,then weight of $MSB = \frac{E_R}{2}$ and weight of $LSB = \frac{E_R}{2^4}$,for another value of digital input, the possible analog output is given by

Digital Input	Analog Output
1000	$\frac{E_R}{2^1}$
0100	$\frac{E_R}{2^2}$
0010	$\frac{E_R}{2^3}$
0001	$\frac{E_R}{2^4}$

The weight of LSB is $\frac{E_R}{2^4}$ and weight of MSB is $\frac{E_R}{2^1}$

i.e. weight of MSB is $\frac{E_R}{2}$ and weight of LSB is $\frac{E_R}{2^4}$ for generalized case.

Consider the above table for a 4-bit converter. If all the bits of the input are high , then the analog output (or exact range of the converter) is given by superposition theorem as follows:

$$E_o = \frac{E_R}{2^1} + \frac{E_R}{2^2} + \frac{E_R}{2^3} + \frac{E_R}{2^4}$$

$$E_o = E_R(1 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3} + 1 \times 2^{-4})$$

$$E_o = \frac{E_R}{2^4}(d_3.2^3 + d_2.2^2 + d_1.2^1 + d_0.2^0)$$

For the n-bit system, the output is given by,

$$E_o = \frac{E_R}{2^n}[d_{n-1}2^{n-1} + d_{n-2}2^{n-2} + d_{n-3}2^{n-3} + \cdots + d_1 2^1 + d_0 2^0]$$

and range is $\frac{E_R}{2^n}$

What will be the analog output for the digital input of 1010, if the full range of converter is 8 volt

Here digital input = 1010

No. of input bits = 4

Full range of converter = E_R = 8 volt

We have,

$$E_o = \frac{E_R}{2^4}(d_3.2^3 + d_2.2^2 + d_1.2^1 + d_0.2^0)$$

$$E_o = \frac{8}{16}[(1 \times 8) + (0 \times 4) + (1 \times 2) + (0 \times 1)]$$

$$E_o = \frac{1}{2}[8 + 2]$$

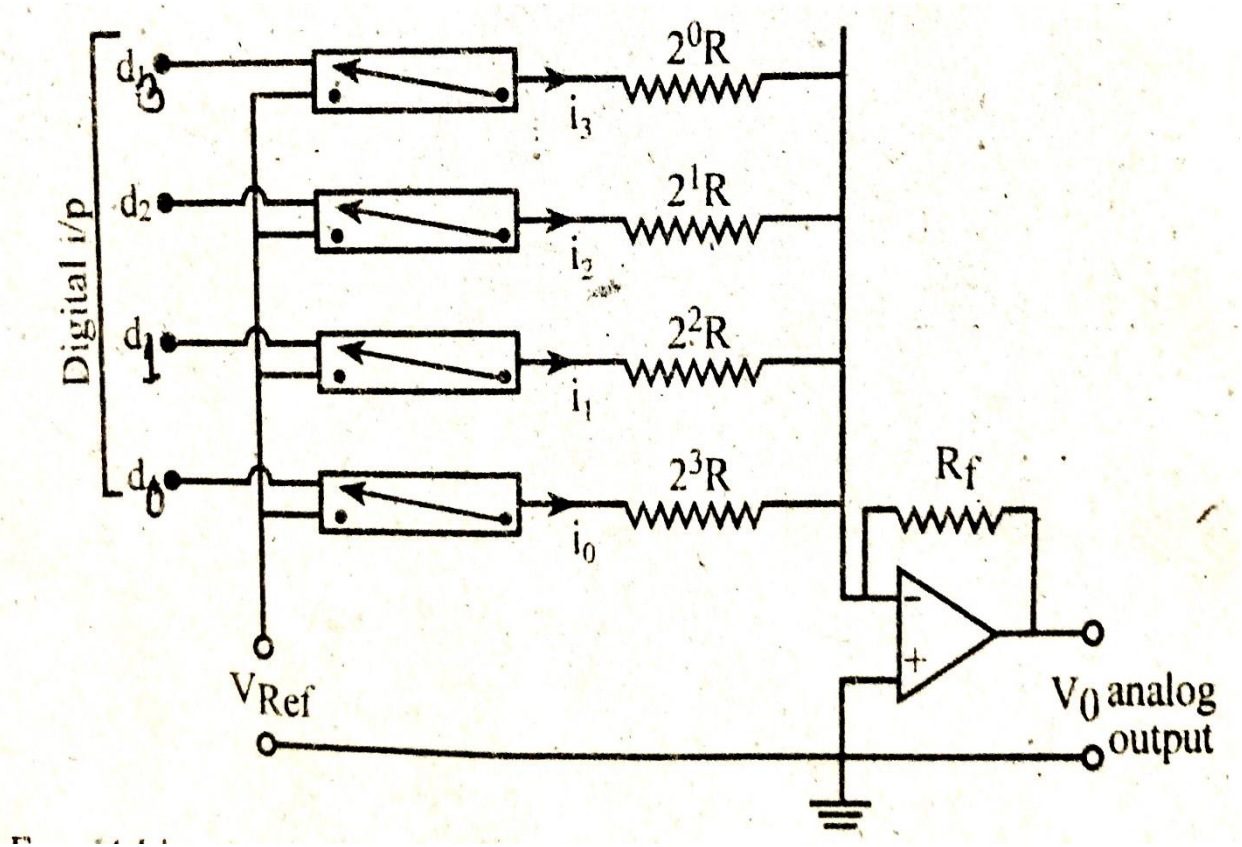
$$\therefore \boxed{E_o = 5 \text{ Volts}}$$

Weighted Resistor Network (WRN) DAC

- In this converter, the resistance associated with the digital binary input has the value reversed of the binary system i.e. resistance associated with MSB has the least value and the resistance value increase by the factor value-2 if we moved from MSB to LSB.
- Hence, if 2^0R is the resistance associated with the MSB, then the resistance associated with LSB is $2^{n-1}R$
- The figure shows a four bit Digital to Analog Converter

Switch

- When input bit is 1, switch is connected to V_{Ref}
- When input bit is 0, switch is connected to ground.



- In this converter, the reference voltage is connected to the resistor by means of switch which respond to binary one '1', each such switch having an input from one of the bit from the digital input. Thus an input of 1001 would close the switches attached to the LSB & MSB. The table below shows different combination of input and output for a 4-bit converter
- Here for shake of simplicity the four bit converter is used.

Digital Input	Analog Output
1000	$i_3 = \frac{V_{Ref}}{2^0 R}$
0100	$i_2 = \frac{V_{Ref}}{2^1 R}$
0010	$i_1 = \frac{V_{Ref}}{2^2 R}$
0001	$i_0 = \frac{V_{Ref}}{2^3 R}$

	Bits	Resistance Value
MSB	d_3	$2^0 R$
	d_2	$2^1 R$
	d_1	$2^2 R$
LSB	d_0	$2^3 R$

If all the inputs are high i.e. 1111 then the total current can be obtained by superposition theorem and given by,

$$i = i_3 + i_2 + i_1 + i_0$$

$$i = \frac{V_{Ref}}{2^0 R} + \frac{V_{Ref}}{2^1 R} + \frac{V_{Ref}}{2^2 R} + \frac{V_{Ref}}{2^3 R}$$

$$i = \frac{V_{Ref}}{R}\left[\frac{1}{2^0} + \frac{1}{2^1} + \frac{1}{2^2} + \frac{1}{2^3}\right]$$

$$i = \frac{V_{Ref}}{R}\left[d_3.2^0 + d_2.2^{-1} + d_1.2^{-2} + d_0.2^{-3}\right]$$

$$\boxed{i = \frac{V_{Ref}}{2^3 R}\left[d_3.2^3 + d_2.2^2 + d_1.2^1 + d_0.2^0\right]}$$

Hence the analog output voltage is given by,

$$V_0 = -i.R_f$$

$$\boxed{V_0 = -\frac{V_{Ref}.R_f}{2^3 R}\left[d_3.2^3 + d_2.2^2 + d_1.2^1 + d_0.2^0\right]}$$

Hence for n-bit converter the analog output is,

$$\boxed{V_0 = -\frac{V_{Ref}.R_f}{2^{n-1} R}\left[d_{n-1}2^{n-1} + d_{n-2}2^{n-2} + d_{n-3}2^{n-3} + \cdots + d_1 2^1 + d_0 2^0\right]}$$

Drawbacks of WRN DAC

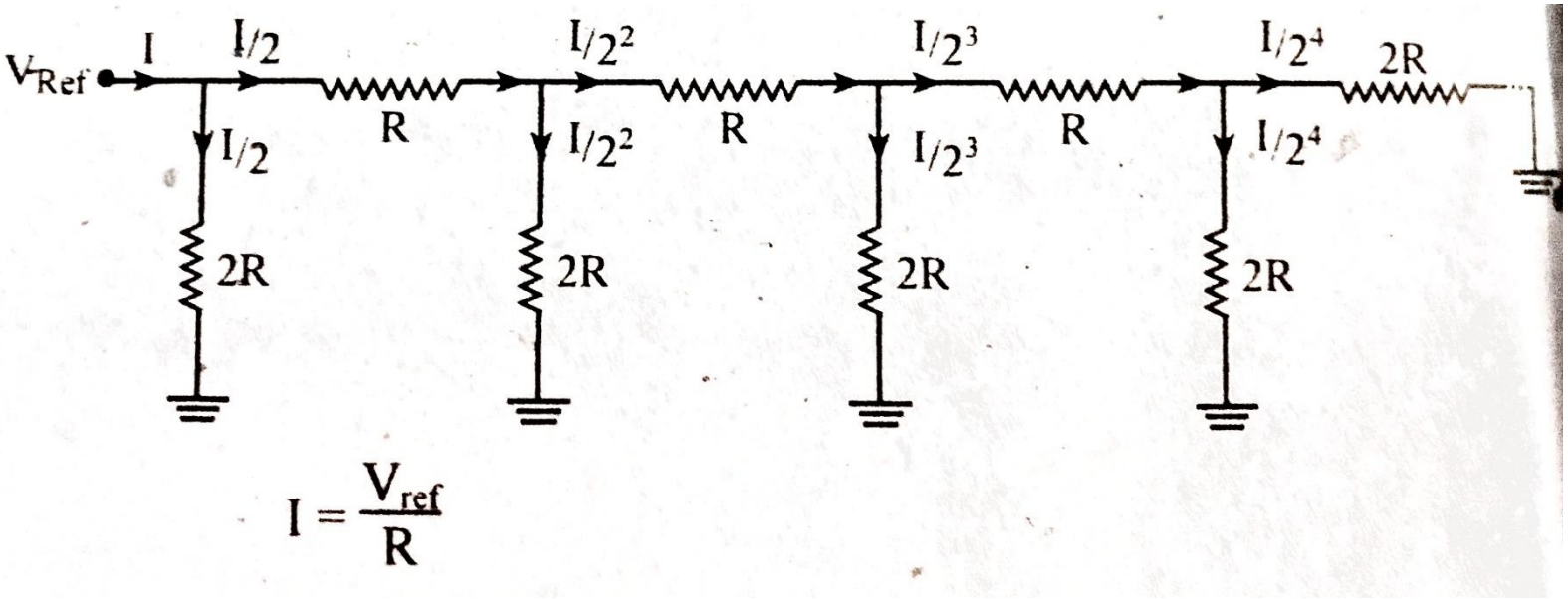
There are mainly two drawbacks of WRN DAC.

1. As the bit goes on increasing, the value of the resistance increases i.e. there will be a wide range of variation in the value of resistance used in DAC, which is not suitable for modern IC manufacturing technology.
2. If the bit goes on increasing then the tolerance value of LSB resistance may exceed the resistance value of the MSB.

To avoid these drawbacks R-2R- Ladder DAC is used.

R-2R- Ladder DAC

All the drawbacks of WRN DAC are overcome in R-2R networks. In this method only two values of resistances (always the ratio being 1:2) are used as shown in below:



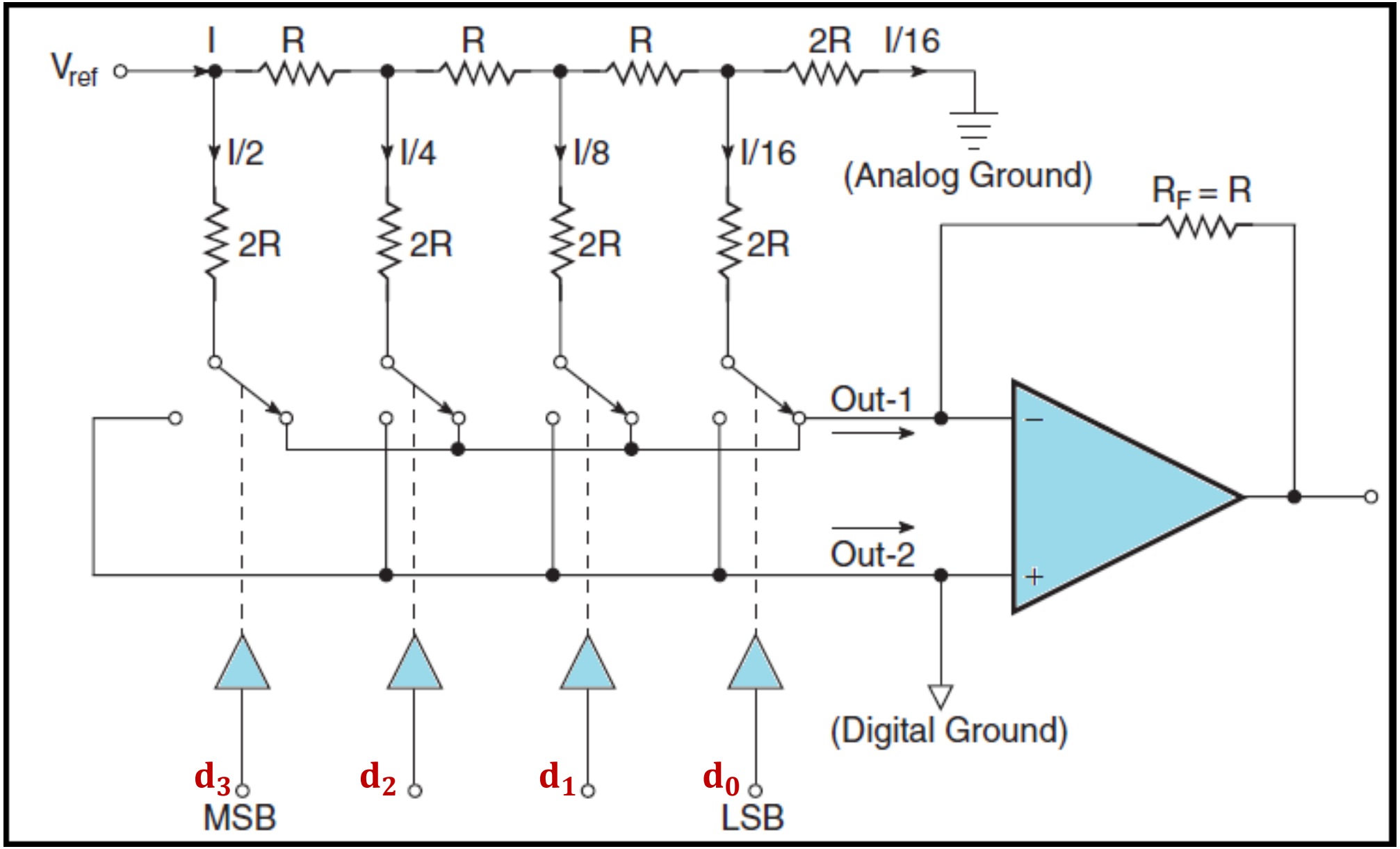


Figure: R-2R Network

If all the inputs are high i.e. 1111 then the total current can be obtained by superposition theorem and given by,

$$i = \frac{i}{2} + \frac{i}{2^2} + \frac{i}{2^3} + \frac{i}{2^4}$$

$$i = \frac{V_{Ref}}{R}\left[\frac{1}{2} + \frac{1}{2^2} + \frac{1}{2^3} + \frac{1}{2^4}\right]$$

$$i = \frac{V_{Ref}}{R}\left[1 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3} + 1 \times 2^{-4}\right]$$

$$i = \frac{V_{Ref}}{2^4 R}\left[1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0\right]$$

$$\boxed{i = \frac{V_{Ref}}{2^4 R}\left[d_3.2^3 + d_2.2^2 + d_1.2^1 + d_0.2^0\right]}$$

Hence the analog output voltage is given by,

$$V_0 = -i.R_f$$

$$\boxed{V_0 = -\frac{V_{Ref}.R_f}{2^4 R}\left[d_3.2^3 + d_2.2^2 + d_1.2^1 + d_0.2^0\right]}$$

Hence for n-bit converter the analog output is,

$$\boxed{V_0 = -\frac{V_{Ref}.R_f}{2^n R}\left[d_{n-1}2^{n-1} + d_{n-2}2^{n-2} + d_{n-3}2^{n-3} + \cdots + d_1 2^1 + d_0 2^0\right]}$$

Advantages of R-2R ladder

- Only 2 resistor values
- Easier implementation
- Easier to manufacture
- Faster response time

Disadvantages

- More confusing analysis
- May result in non-monotonic behavior at major crossings, such as from 01111_2 to 10000_2

An 8-bit DAC has a reference voltage of 12V. It uses a R-2R ladder network. Find the minimum value of resistance R such that the output current of the ladder does not exists above 10 mA. Also find the smallest value of quantized current.

No. of bits (n) = 8

Reference voltage (V_{Ref}) = 12 Volts

Maximum value of current (I_{Max}) = 10 mA = 0.01 A

We know,

$$V_0 = -\frac{V_{Ref}.R_f}{2^n R}[d_{n-1}2^{n-1} + d_{n-2}2^{n-2} + \cdots + d_1 2^1 + d_0 2^0]$$

$$\frac{V_0}{R_f} = -\frac{V_{Ref}}{2^n R}[d_{n-1}2^{n-1} + d_{n-2}2^{n-2} + \cdots + d_1 2^1 + d_0 2^0]$$

$$I_{Max} = \frac{V_0}{R_f} = -\frac{V_{Ref}}{2^n R}[d_{n-1}2^{n-1} + d_{n-2}2^{n-2} + \cdots + d_1 2^1 + d_0 2^0]$$

$$0.01 = -\frac{12}{2^8 R}[(1\times 2^7) + (1\times 2^6) + (1\times 2^5) + (1\times 2^4) + (1\times 2^3) + (1\times 2^2) + (1\times 2^1) + (1\times 2^0)]$$

$$R = -\frac{12}{256\times 0.01}[128 + 64 + 32 + 16 + 8 + 4 + 2 + 1]$$

$$R = -\frac{12}{2.56}\times 255 = 1195.3125\ \Omega$$

The smallest value of quantized current is equal to the current associated with LSB

$$I_{Min} = \frac{V_{Ref}}{2^n R} = \frac{12}{256\times 1195.3125} = 39.216\mu A$$

Performance characteristics of DAC/ADC specifications

1. Resolution
2. Settling Time
3. Linearity
4. Speed
5. Errors

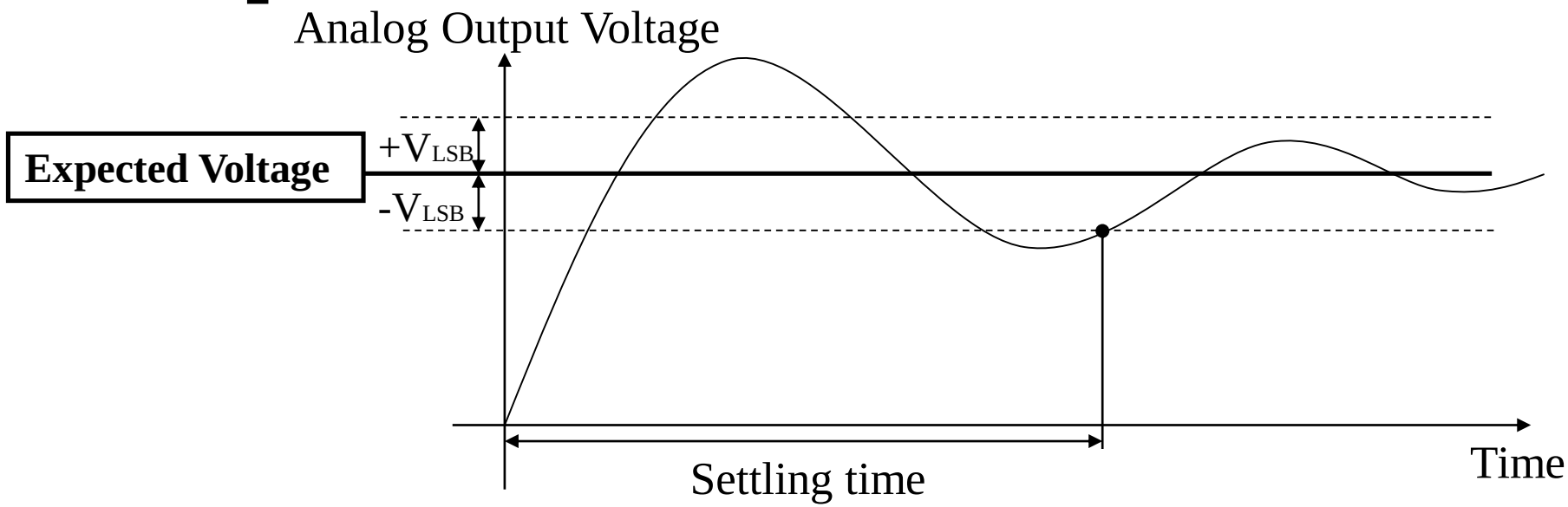
Resolution:

- Resolution is the amount of variance in output voltage for every change of the LSB in the digital input.
- Resolution defines how closely we can approximate the desired output signal (Higher Resolution means finer detail i.e. smaller Voltage divisions)

$$\text{Resolution} = V_{LSB} = \frac{V_{\text{Ref}}}{2^N}$$

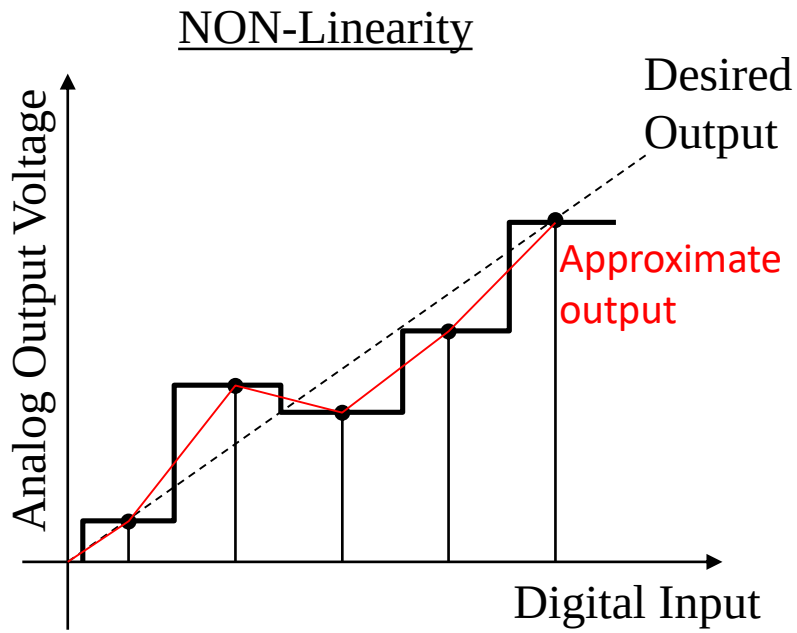
Settling Time:

- The time required for the input signal voltage to settle to the expected output voltage (within $\pm V_{LSB}$) is called settling time.
- Any change in the input state will not be reflected in the output state immediately. This time lag between the two events is settling time.



Linearity:

- Linearity is the difference between the desired analog output and the actual output over the full range of expected values.
- Ideally, a DAC should produce a linear relationship between a digital input and the analog output; this is not always the case



Speed:

- Speed means rate of conversion of a single digital input to its analog equivalent.
- Conversion Rate
  - ✓Depends on clock speed of input signal
  - ✓Depends on settling time of converter

Error:

- Error is the difference between expected ideal output and actual obtained output.

Errors in DAC+ADC

Error is the difference between expected ideal output and actual obtained output.

Following are common errors associated with DAC

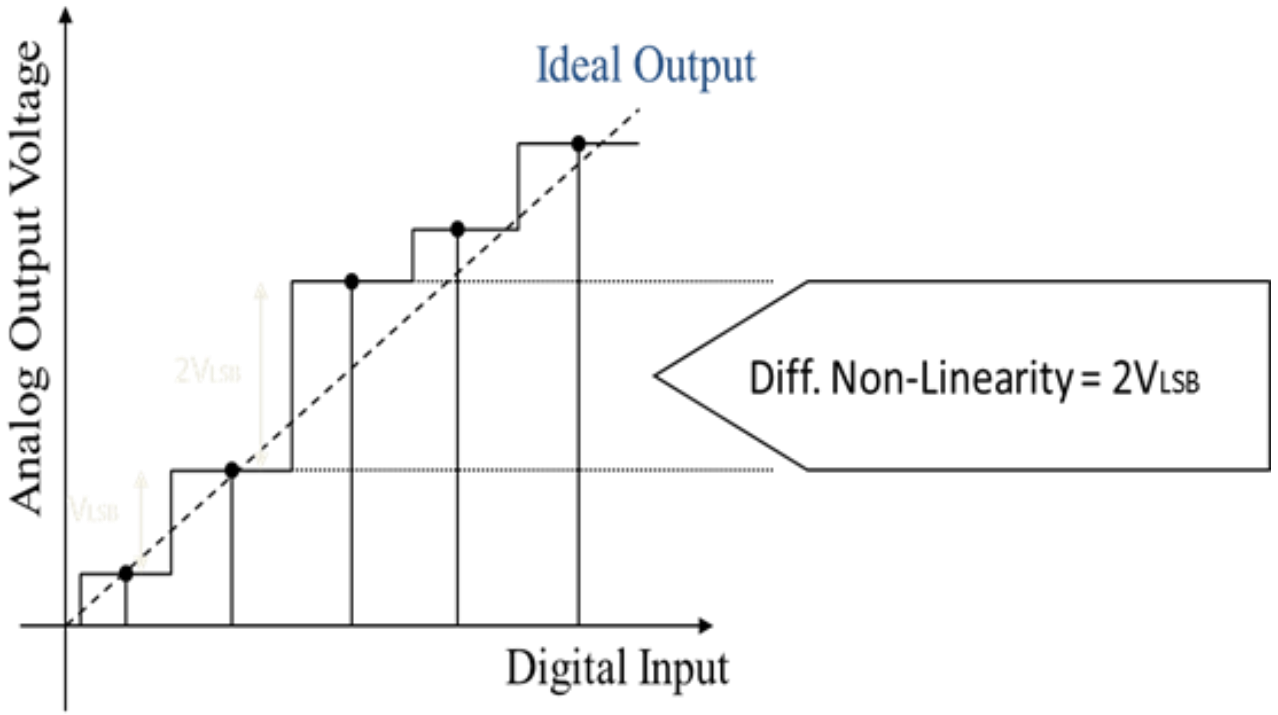
1. Non-linearity
   a) Differential Non-linearity
   b) Integral Non-linearity
2. Gain Error
3. Offset Error
4. Non-monotonicity

1. Non Linearity

- It refers to the deviation of output of DAC from ideal linear characteristics.
- There are two types of non-linearity.
  a) Differential non-linearity
  b) Integral non-linearity

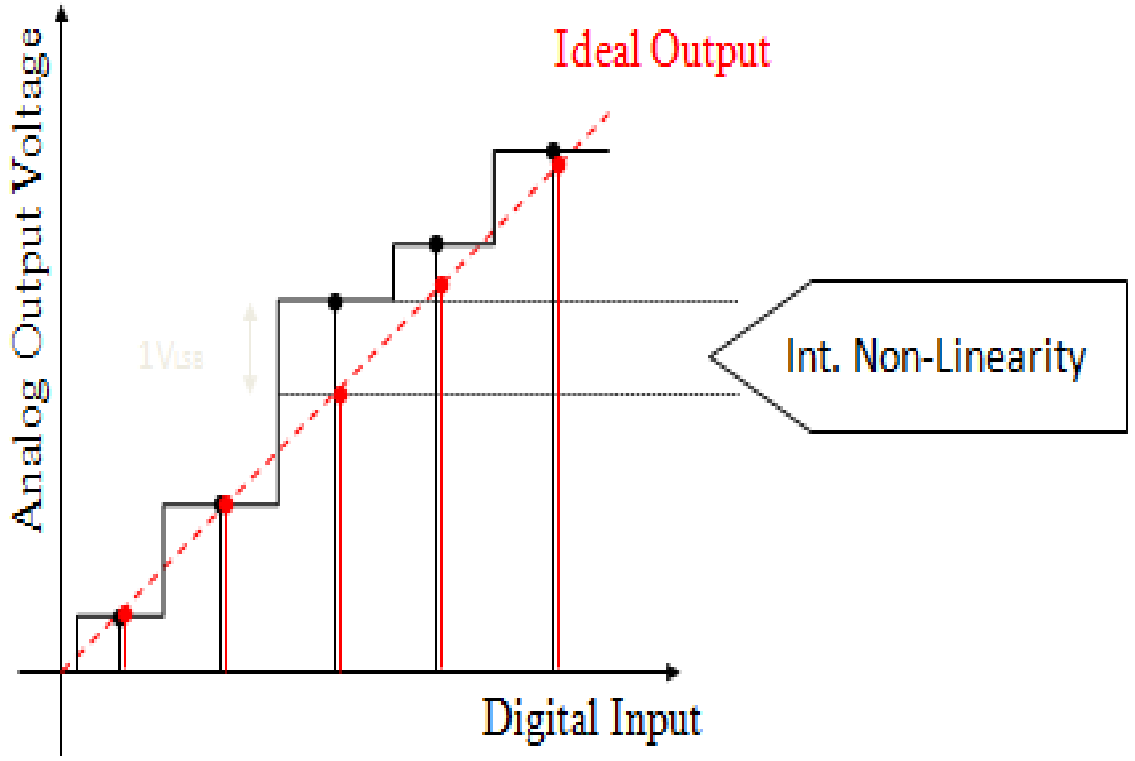
a) Differential Non-Linearity

- Differential non-linearity is the difference between an actual stepsize and ideal value (which is $1V_{LSB}$)



b) Integral Non-Linearity

- Integral non-linearity is the deviation of the values on the actual transfer function from a straight line.
- It is the maximum deviation of the output of a DAC for any given input code from its ideal straight line characteristics curve.



2. Gain Error

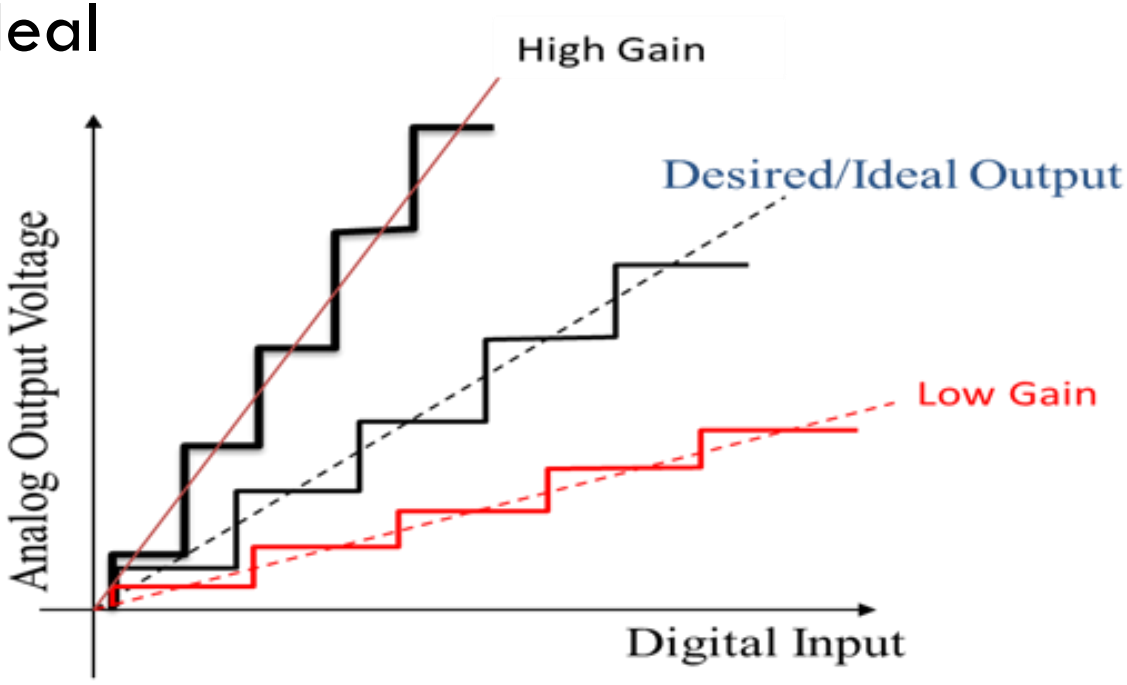
It is difference in slope of the ideal curve and the actual DAC output

High Gain Error:

- Actual slope greater than ideal

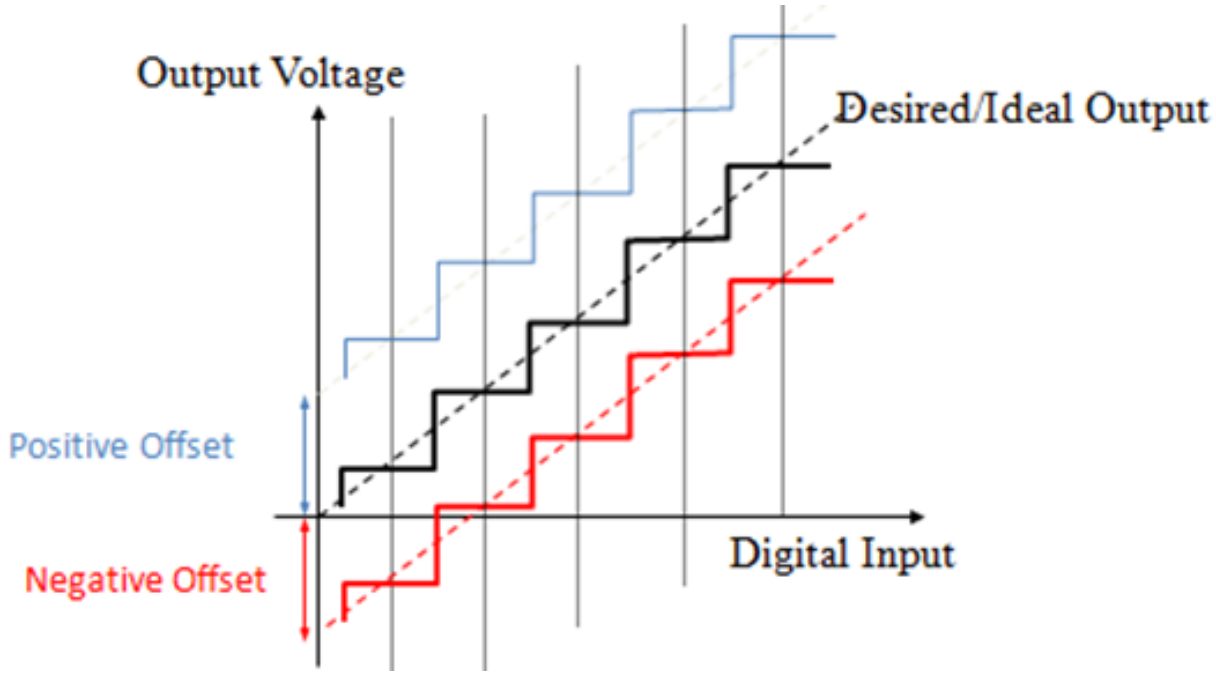
Low Gain Error:

- Actual slope less than ideal



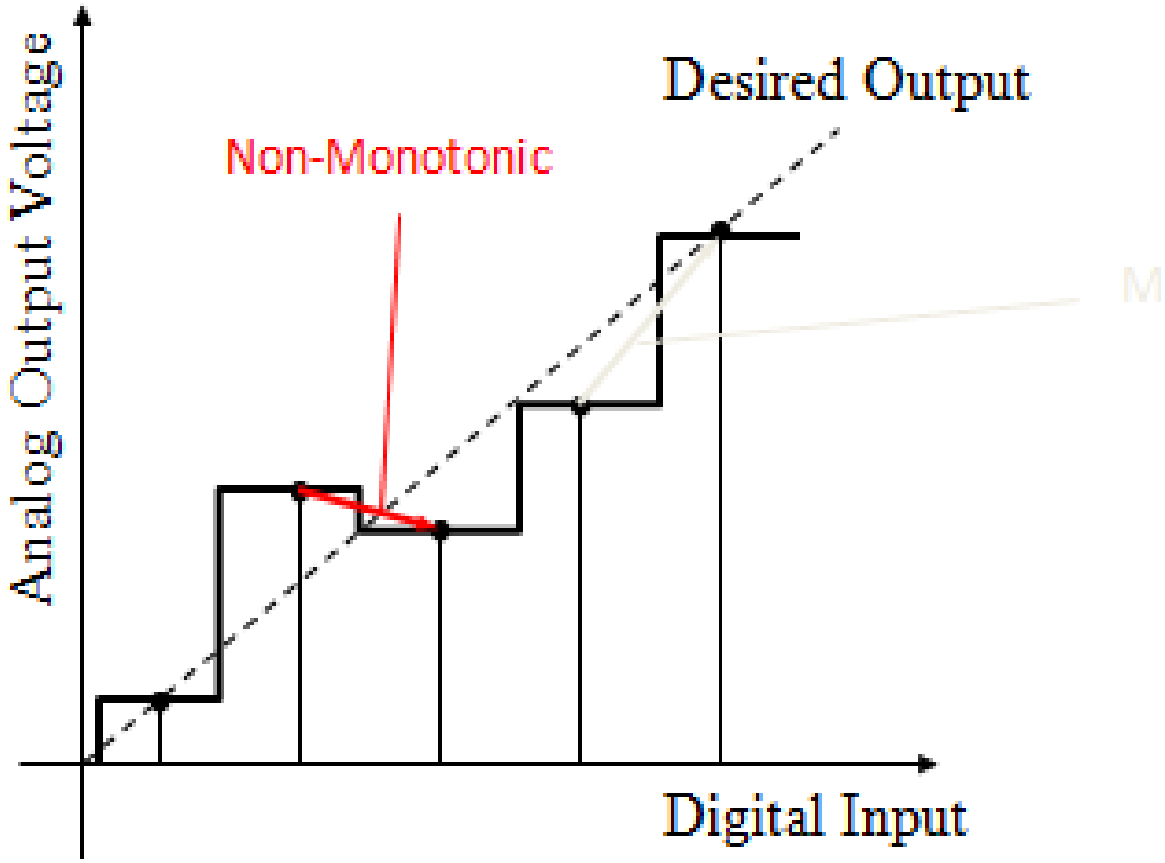
3. Offset Error

- It is a constant voltage difference between ideal DAC output and actual output.
- This is the error caused on entering a digital code which is supposed to produce zero volt.



4. Non-Monotonicity

- It is the decrease of analog output voltage with an increase in digital input.

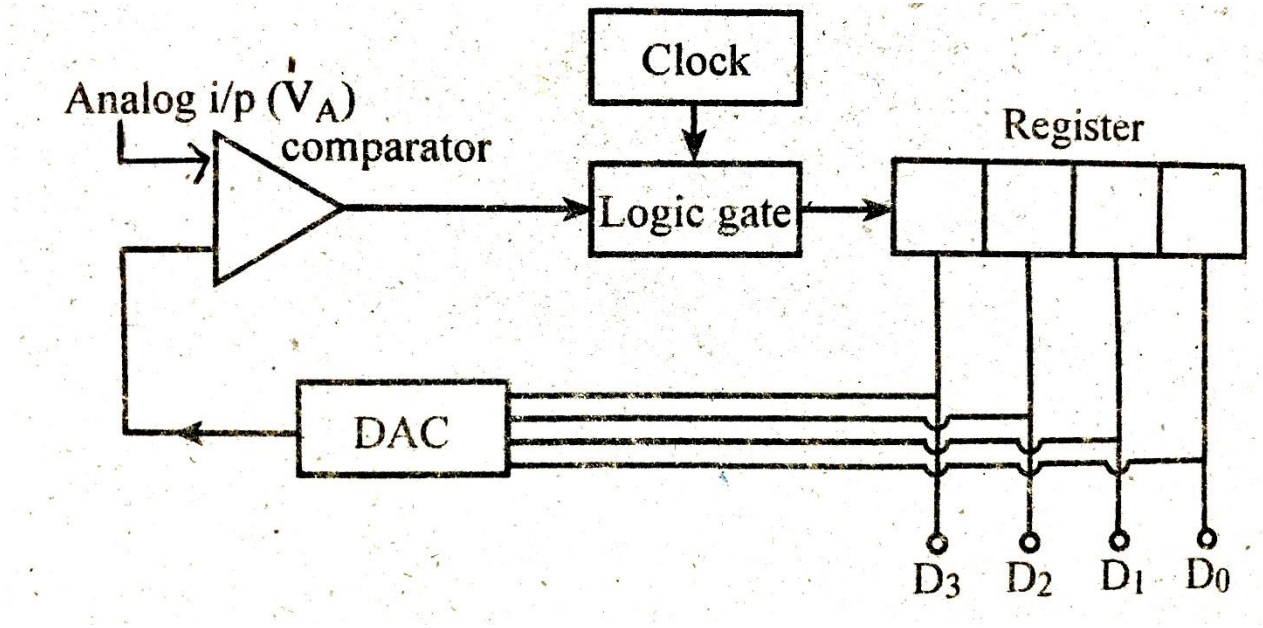


Analog to Digital Conversion

- These circuits converts the analog input signal to the binary equivalent of it.
- There are following types of ADC
  1) Successive Approximation ADC
  2) Ramp ADC
  3) Dual-Ramp type ADC &
  4) Flash (or Parallel) type ADC

Successive Approximation ADC

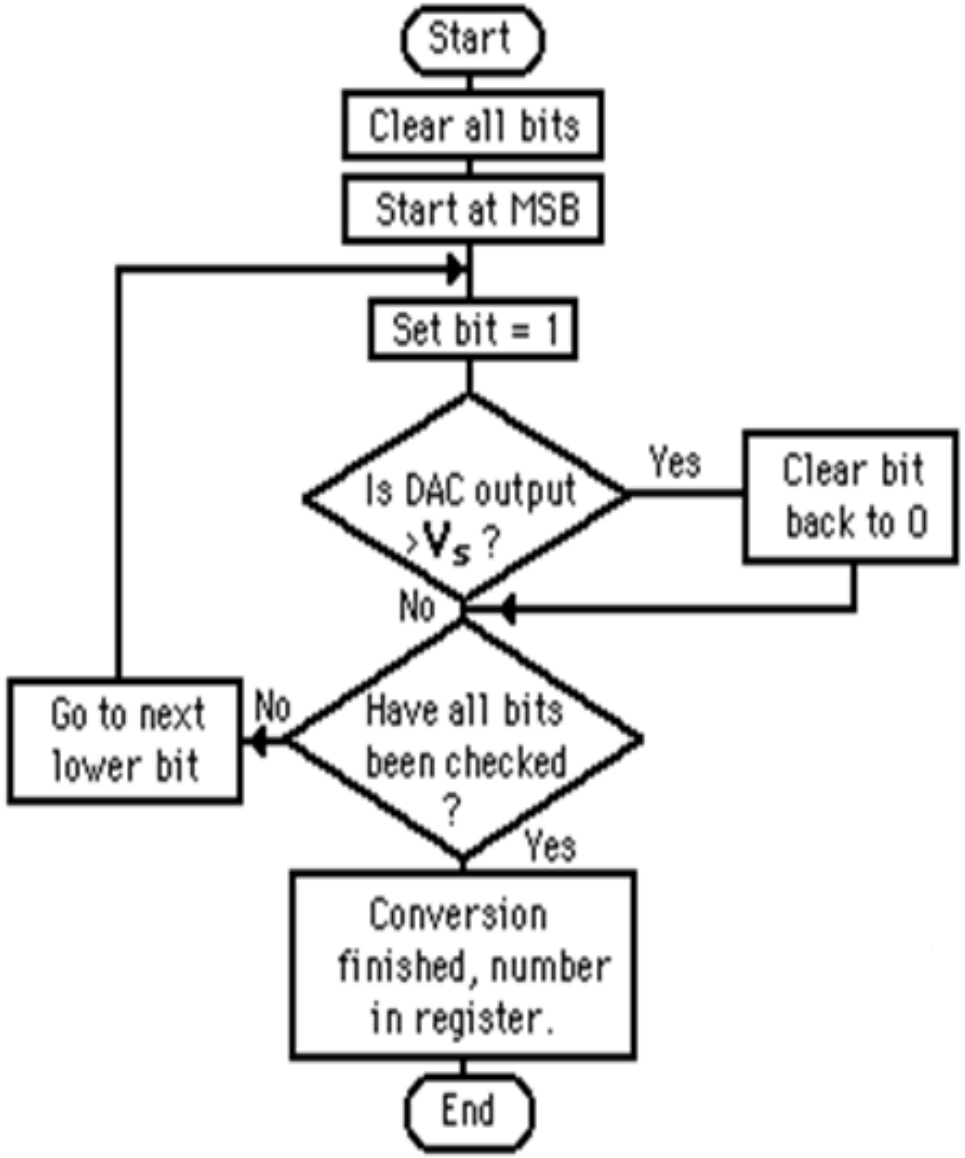
- Successive approximation type ADC is probably the most commonly used analog to digital conversion method.
- This method is based on comparing the input analog voltage (V_A) with another analog Voltage (E_o) until the two voltages are equal or as close as it is possible to set them
- Figure below shows the circuit diagram of Successive approximation ADC



- As shown above a clock is used to emit a regular sequence of pulses i.e. 0 & 1 bits, which are stored in a register and becomes input to Digital to Analog converter (DAC)
- At the start of the conversion process, the input to the DAC is set with MSB at 1 and other bits 0
- For a 4-bit converter ,this would mean 1000.
- Since this represent the mid point of digital range, it gives an analog output voltage from the DAC of $(\frac{8}{16}\mathrm{V_{ref}})$ i.e. $(\frac{8}{16})$ of the full scale analog voltage.
- This first approximation is then compared with the input analog voltage $\mathrm{V_A}$.
- If it is smaller than the input voltage $\mathrm{V_A}$, a second approximation is made and the next bit is turned ON, to give an input to the DAC of 1100 i.e. an analog voltage $\mathrm{E_o}$ from the DAC of $(\frac{12}{16})$ of the full scale analog voltage

- If this results in a voltage which is larger than the input analog voltage (V_A), the bit turned OFF and the next bit is tried i.e. an input of 1010 to the DAC.
- And so $(\frac{10}{16})$ of the full scale analog voltage
- If this is too low then next bit is added to give to 1011 i.e. $(\frac{11}{16})$ of the full scale analog voltage.
- If this is too high then the bit is turned OFF ,and the nearest digital equivalent to the input analog voltage given as 1010.
- Because each of the bits in the word is tried in sequence with an n-bit word it only takes n-steps to make the comparison.
- Thus, if the clock has the frequency 'f' , the time between pulses is $(\frac{1}{f})$
- Hence the conversion time is $(\frac{n}{f})$

Flow chart of Successive Approximation ADC



Find the successive approximation in an analog to digital output for a 4-bit converter to a 3.271 volt. If the reference voltage is 5V.

Given

Reference voltage (V_{ref}) = 5V

Input analog voltage (V_A) = 3.271V

1st approximation:

Input to DAC =1000 [MSB or 1st bit of 4-bit register to be high]

Output from DAC (E_o) = $\frac{8}{16} V_{ref} = \frac{8}{16} \times 5 = 2.5V$

Now $V_A > E_o$, so the first bit (MSB) remains at 1 and the next bit is turned ON

2nd approximation:

Input to DAC =1100

Output from DAC (E_o) = $\frac{12}{16} V_{ref} = \frac{12}{16} \times 5 = 3.75V$

Now $V_A < E_o$, so the bit is reset to 0 and the next bit is set to 1 or turned ON

3rd approximation:

Input to DAC =1010

Output from DAC $(E_o) = \frac{10}{16} V_{ref} = \frac{10}{16} \times 5 = 3.125V$

Now $V_A > E_o$, so the bit remains at 1 and the next bit is turned ON

4th approximation:

Input to DAC =1011

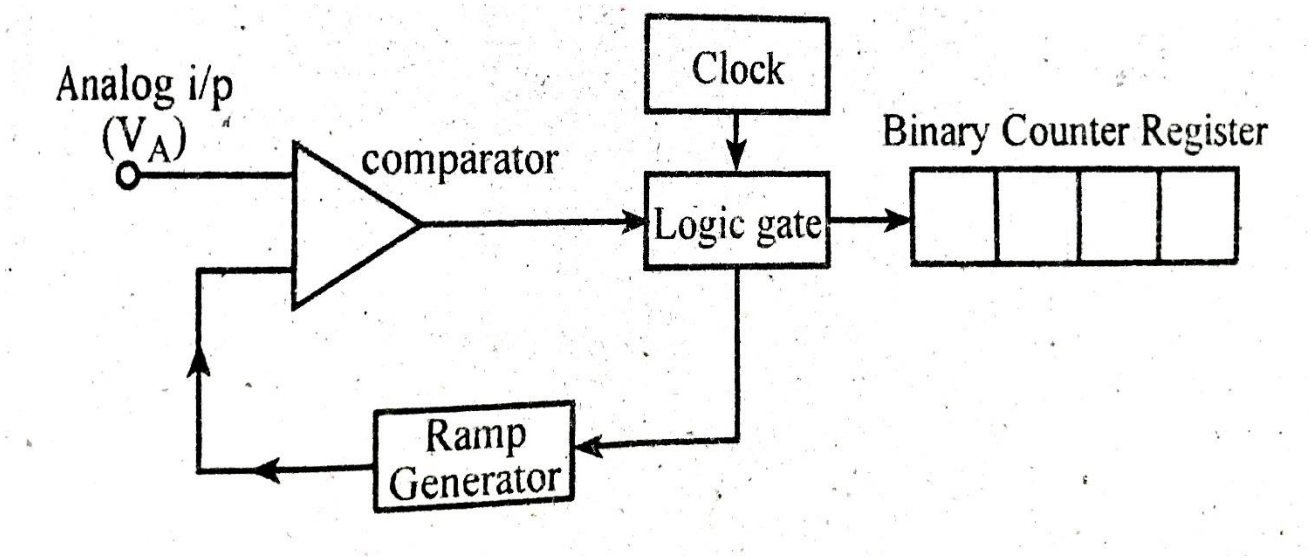
Output from DAC $(E_o) = \frac{11}{16} V_{ref} = \frac{11}{16} \times 5 = 3.4375V$

Now $V_A < E_o$, so the bit is reset to 0

and the digital equivalent of 3.271V analog voltage is 1010

Ramp type ADC

- The ramp form of ADC involves an analog voltage which is increased at a constant rate so called ramp voltage.
- This ramp voltage is generated by a capacitor being charged from a constant current source as shown below and the ramp signal is also shown



- The charge Q on the capacitor is Q = It
- Where, I = constant current
- And t = time for which the current changes in the capacitor
- Since the potential difference (P.d) across the capacitor is $V_C = \frac{Q}{C} = \frac{It}{C}$ then the P.d is proportional to the time for which the charging occurs. And so a ramp voltage is produced.

  i.e. $V_C \propto t$
- A ramp voltage is applied to a capacitor where it is compared to the analog input voltage V_A

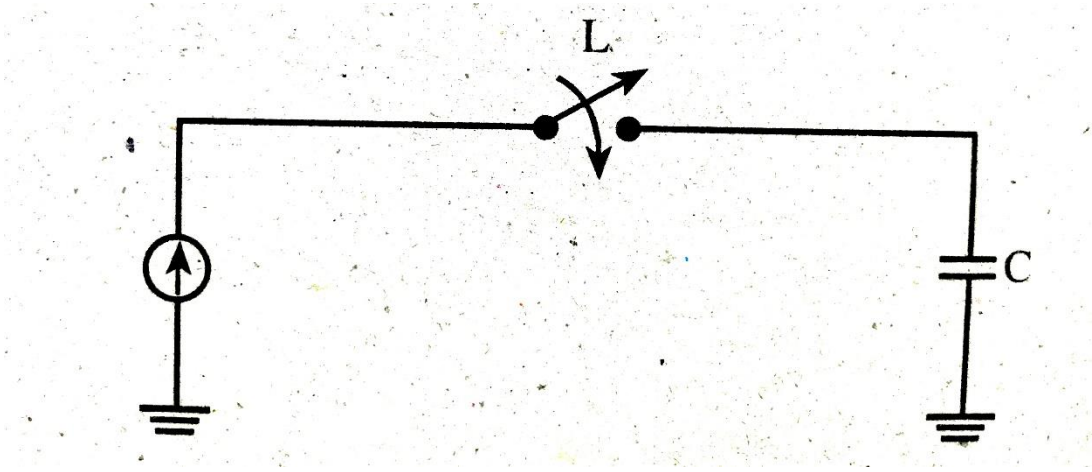
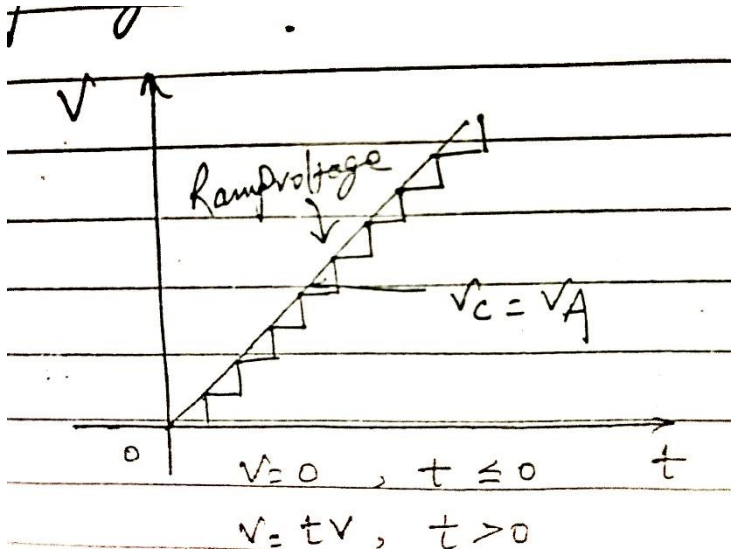


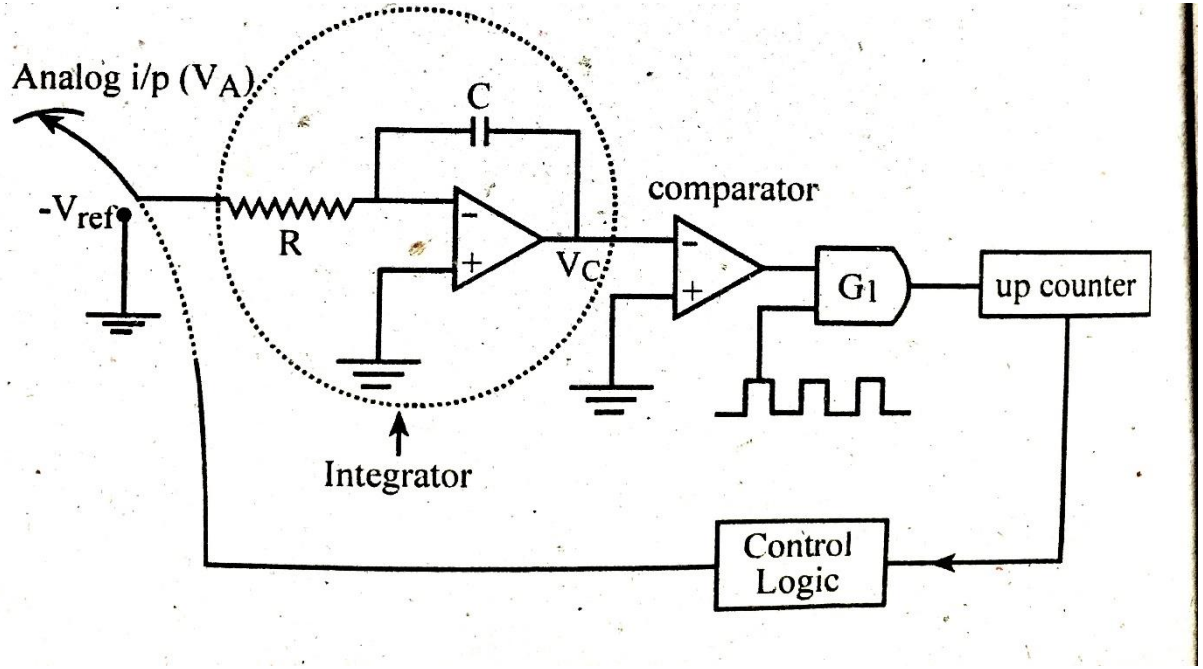
Fig: Ramp generator



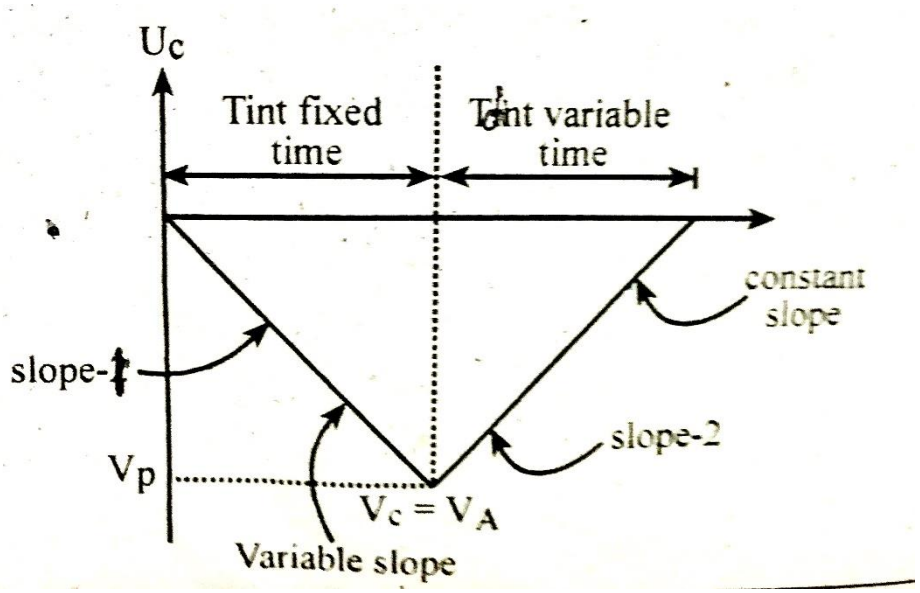
- The time taken for the ramp voltage to increase the value of the input analog voltage will depend on the magnitude of the input analog voltage.
- When the ramp voltage starts, a gate is opened which starts a binary counter, counting the regular pulse from the clock
- When the two voltages are equal, the gate closes and the word indicated by the counter is the digital representation of the sample analog input voltage
- Fig above shows the sub- systems involved in the ramp form (type) of ADC
- Ramp converters are cheap but relatively slow in Conversion i.e. (time delaying type)

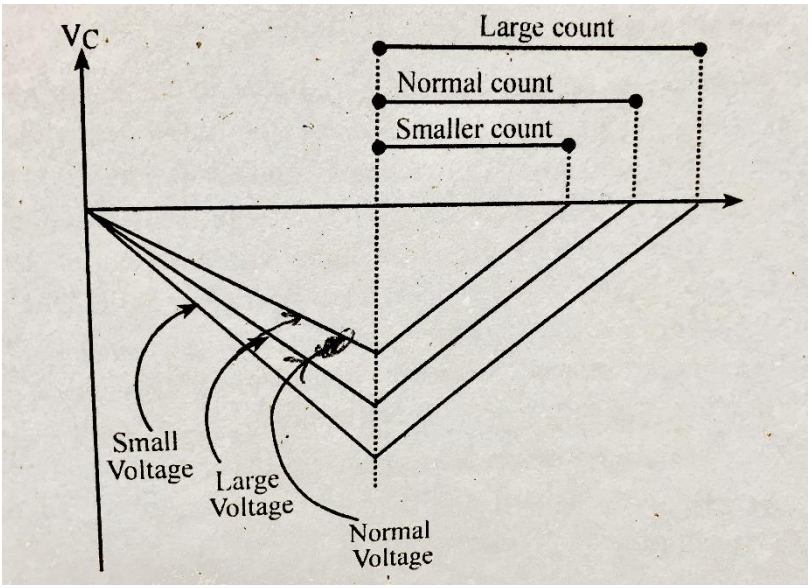
Dual Ramp ADC

- Dual slope ADC is used in digital voltmeter and other type of measuring instrument. A ramp generator is used to produce dual slope characteristics.
- A ramp generator is an integrator circuit.
- The conversion begins with the switch connected to input signal. If analog input is positive, output of integrator (Ramp generator) will be a ramp with negative slope.



- Output of integrator (v) = $\frac{-1}{RC}\int V_{in}.dt$
- The ramp is then allowed to run for fixed time so voltage it reaches is proportional to analog input. When the counter reaches a specific count, the counter is reset and control circuit causes switch to be connected to a reference voltage of opposite polarity. This time output of integrator is a positive going ramp with fixed slope.
- When the positive going ramp reaches zero Volts, it causes comparator to switch output thereby stopping the counter. The binary count stored in the counter register is proportional to analog voltage.





- It has an integrator which produces a ramp signal from constant input analog voltage V_{in}.
- Then there is a comparator to drive the AND gate whose another input is clock pulse of certain frequency.
- The gate drives an up-counter which on certain conditions sends the signal to control logic.
- The control logic then switches the input from $+V_{in}$ to $-V_{ref}$
- When V_{in} is fed or applied into the integrator, it produces a ramp signal where slope is equal to $\frac{-V_{in}}{RC}$
- The gate will open in this case. So, the up-counter will count up to its full scale (i.e. up to 111 for 3-bit) and then resets.
- As it resets, it sends the signal to the conditional logic to switch the input known voltage $(-V_{ref})$
- Now, the voltage will increase with the slope of $\frac{+V_{ref}}{RC}$
- When this negative voltage reaches zero, then the gate will be closed and up-counter will stop counting. The digital code or word seen in the counter will be equivalent to the input analog voltage V_{in}

❖ When V_{in} is fed to the input, the voltage V_C rises to certain level at fixed time (when up-counter counting is full-scale) say this voltage up
Now when the voltage $-V_{ref}$ is connected to the input V_C starts increasing with constant slope of $\frac{V_{ref}}{RC}$
Higher the value of V_{in} , higher will be the peak V_P during first phase of fixed time T_{int}, then longer will be the time for V_P to reach zero level and higher will be the up-counter count

From the figure,

$$\frac{V_{in}}{RC} = \frac{V_P}{T_{int}}$$

Similarly for the 2nd slope,

$$\frac{V_{ref}}{RC} = \frac{V_P}{T_{dint}}$$

Dividing equation (i) by (ii)

$$\frac{V_{in}}{V_{ref}} = \frac{T_{dint}}{T_{int}}$$

$$T_{dint} = \frac{V_{in}}{V_{ref}} \times T_{int}$$

Now total conversion time is given by,

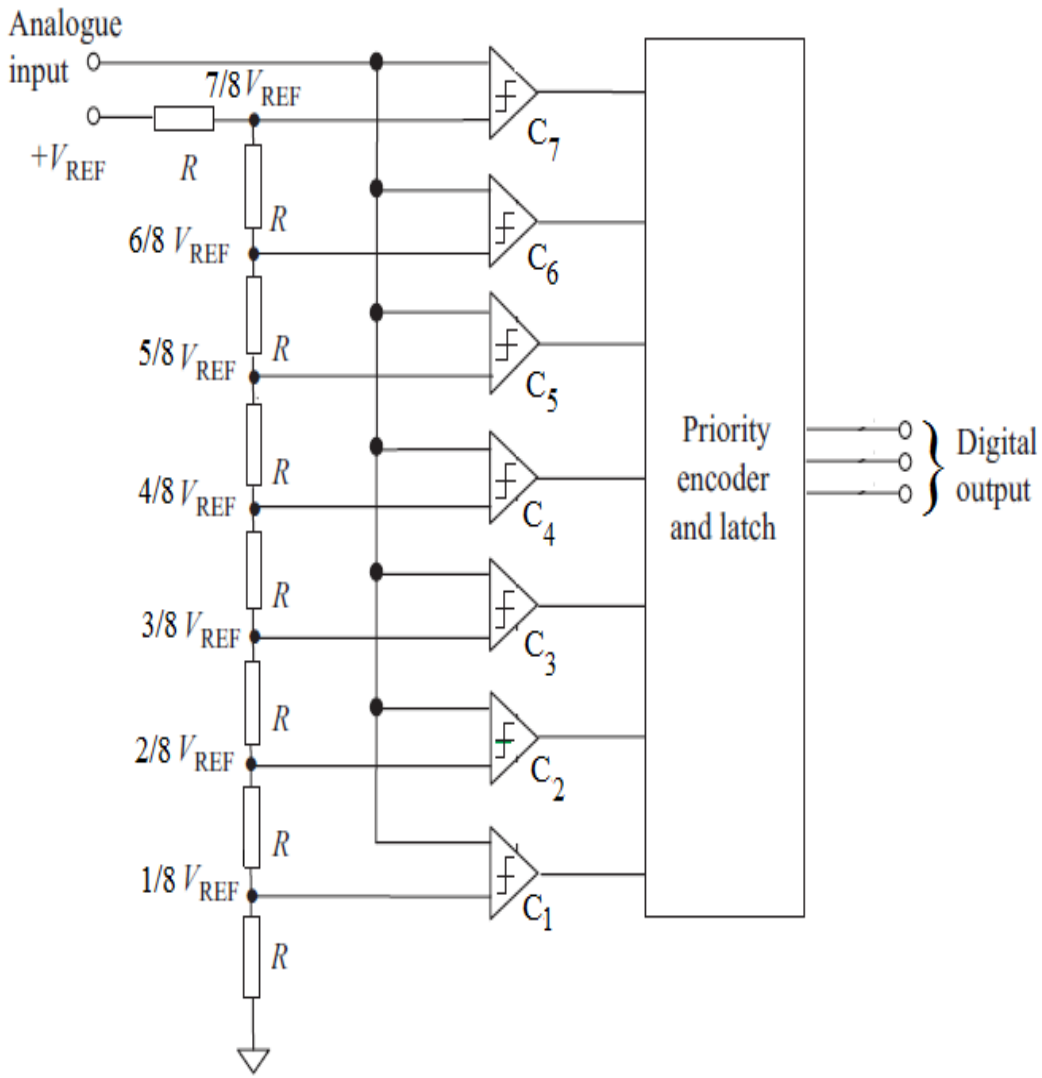
$$T_C = T_{int} + T_{dint}$$

$$T_C = T_{int} + \frac{V_{in}}{V_{ref}} \times T_{int}$$

$$\therefore \boxed{T_C = \left[1 + \frac{V_{in}}{V_{ref}}\right] \times T_{int}}$$

Flash Type/ Comparator Type/ Parallel ADC/Simultaneous ADC

- The parallel ADC is very fast but more costly form of ADC.
- for an n-bit converter, $2^n - 1$ separate voltage comparators are used in parallel.
- Each Comparator has the input analog voltage as one of its analog input.
- A reference Voltage is applied to a ladder of resistors so that the reference voltage applied to each comparator is one bit-higher in size than the reference voltage applied do the lower previous Comparator.
- When the analog input voltage (V_A) is applied all those comparators for which the analog voltage is greater than the reference voltage element will go high and those for which the analog voltage is less than the reference voltage, the element will go low.
- The resulting output of the comparator are fed in parallel to encode which translates them into the digital equivalent output.
- Because all the bits of the output digital word are simultaneously produced, this converter is very fast.



Analog input	C_1	C_2	C_3	C_4	C_5	C_6	C_7	output
$0 - \frac{1}{8}$ of V_{REF}	0	0	0	0	0	0	0	000
$\frac{1}{8} - \frac{2}{8}$ of V_{REF}	1	0	0	0	0	0	0	001
$\frac{2}{8} - \frac{3}{8}$ of V_{REF}	1	1	0	0	0	0	0	010
$\frac{3}{8} - \frac{4}{8}$ of V_{REF}	1	1	1	0	0	0	0	011
$\frac{4}{8} - \frac{5}{8}$ of V_{REF}	1	1	1	1	0	0	0	100
$\frac{5}{8} - \frac{6}{8}$ of V_{REF}	1	1	1	1	1	0	0	101
$\frac{6}{8} - \frac{7}{8}$ of V_{REF}	1	1	1	1	1	1	0	110
$\frac{7}{8} - \frac{8}{8}$ of V_{REF}	1	1	1	1	1	1	1	111

Advantages & Disadvantages of Flash ADC

Advantage:

- It is very fast
- Simplest in concept
- Clock is not required
- Its conversion time is less and can even digitize video signals

Disadvantage:

- Requires $(2^n - 1)$ comparator for n-bit
- Expensive and high power consumption

End of chapter 5