Spirit Level Reaction Time Tester

Hardware Design

Group 25

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A High-Level Block Diagram for the system

8284 Clock Generator

15MHz Crystal

X1
X2

+5V

RDY1
RDY2
F/C

CSYNC
AEN1
AEN2

8284

CLK — 5 MHz → To 8086
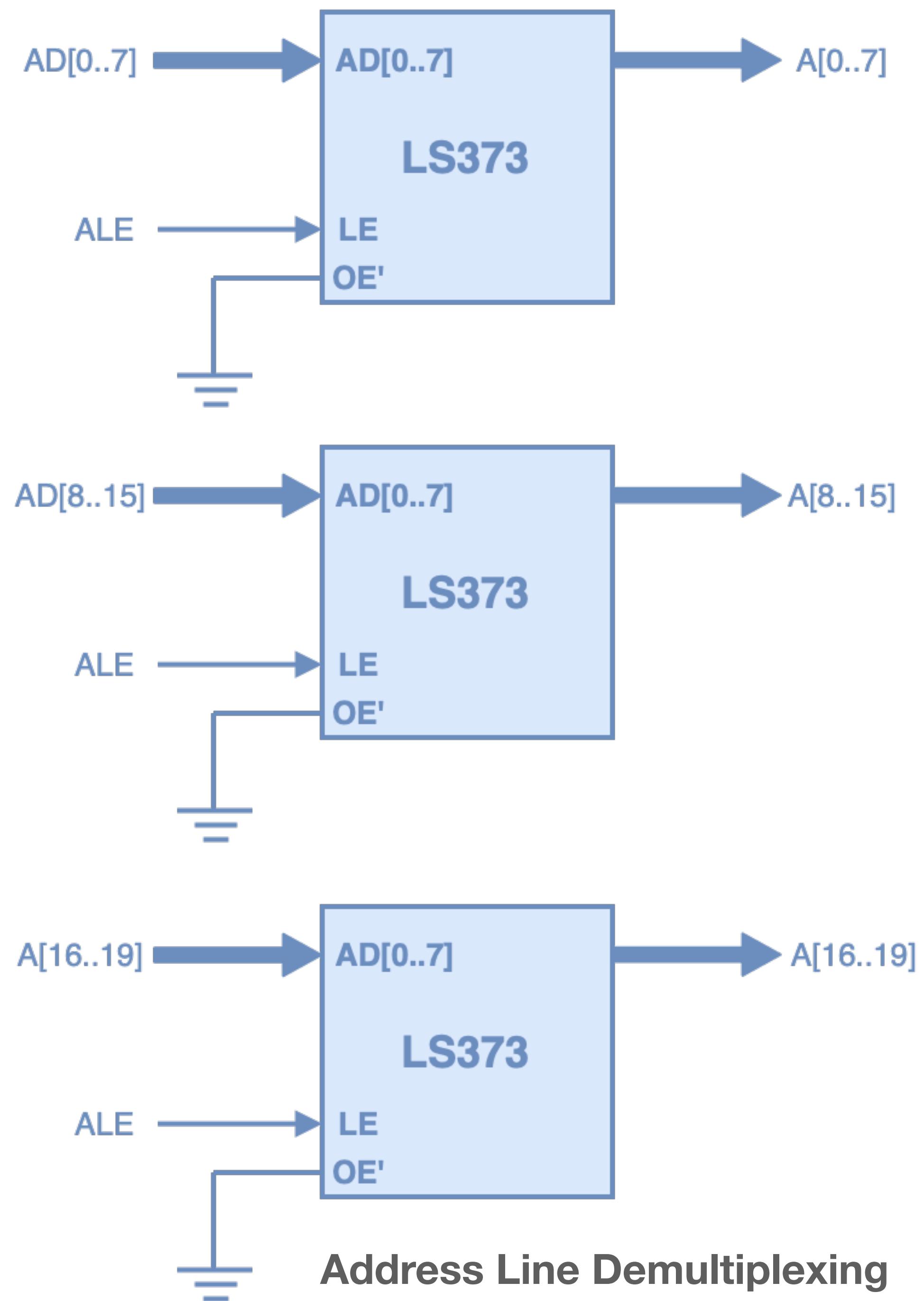PCLK — 2.5 MHz → To 8254
READY → To 8086
RESET → To 8086
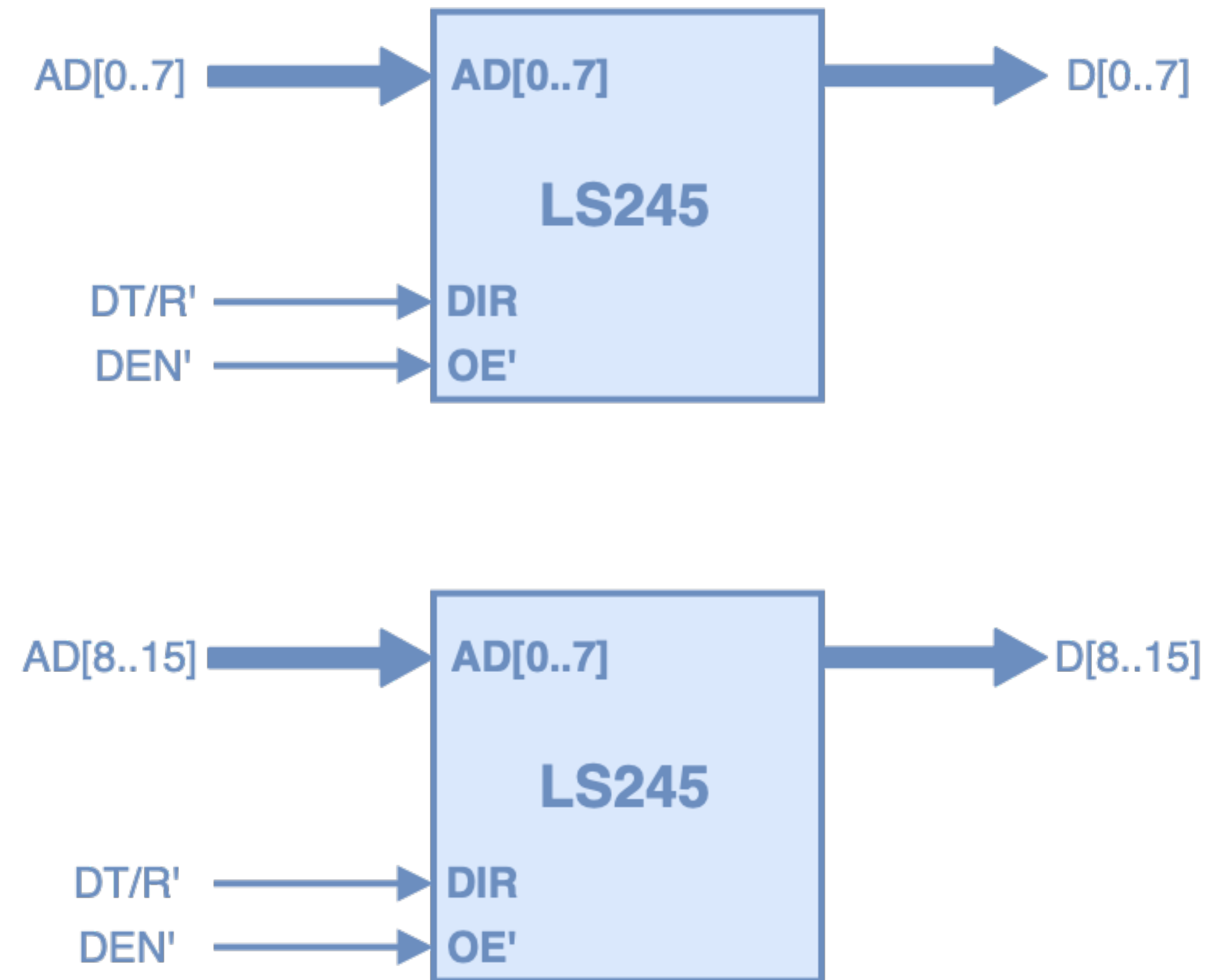
Vcc

RES
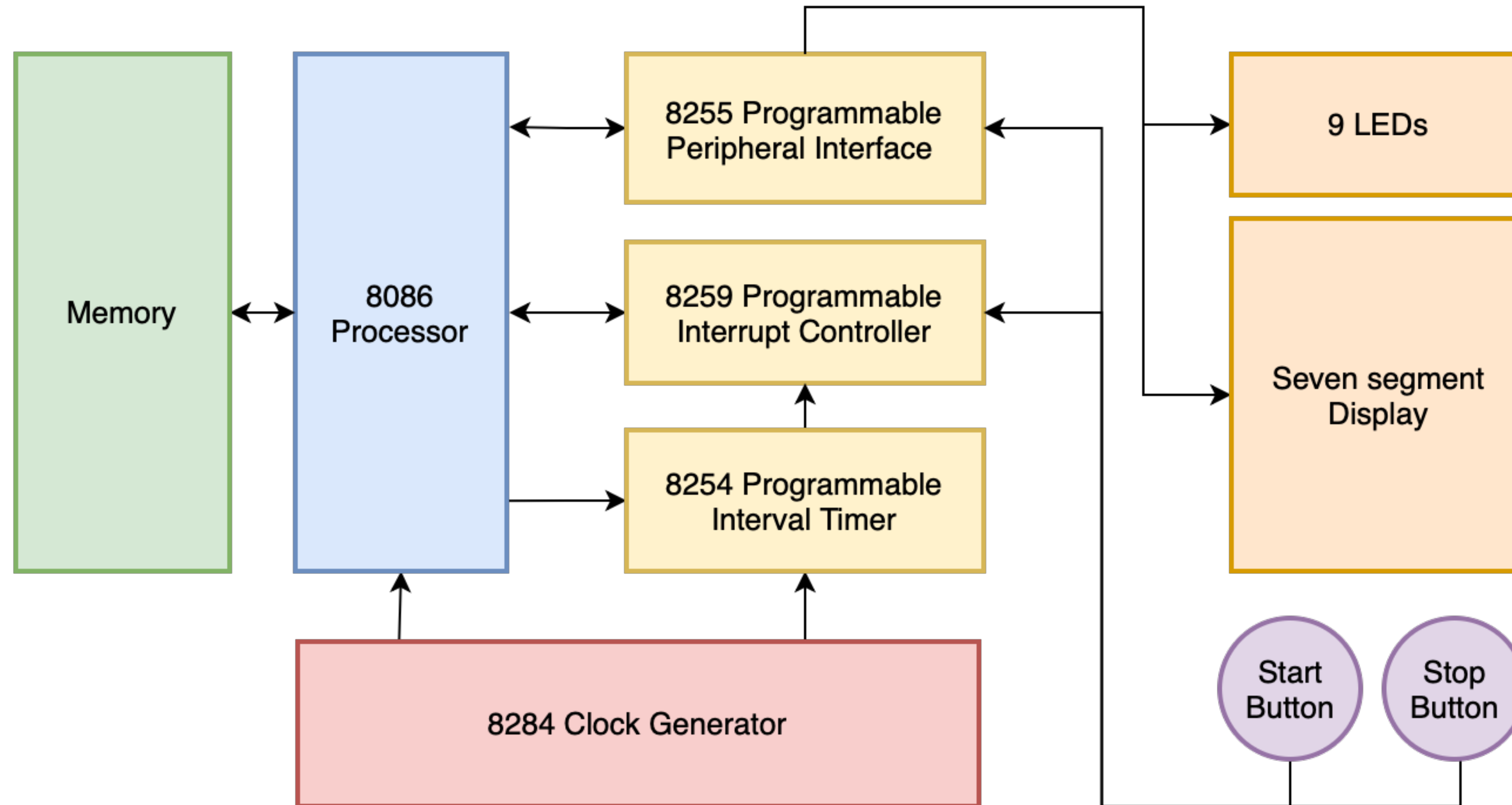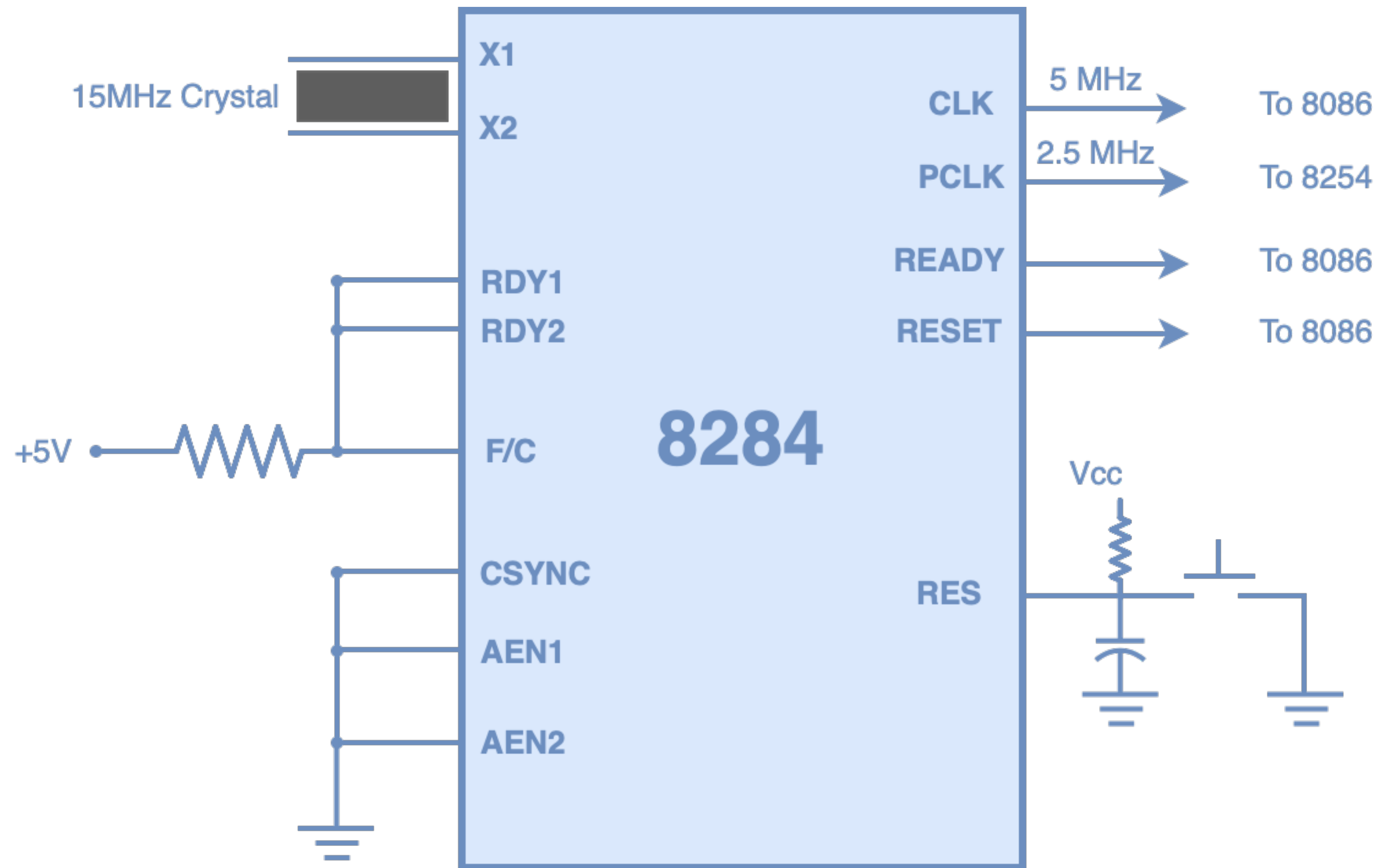
Signals Generated
• CLK at 5MHz
• PCLK at 2.5 MHz
• RESET
• READY

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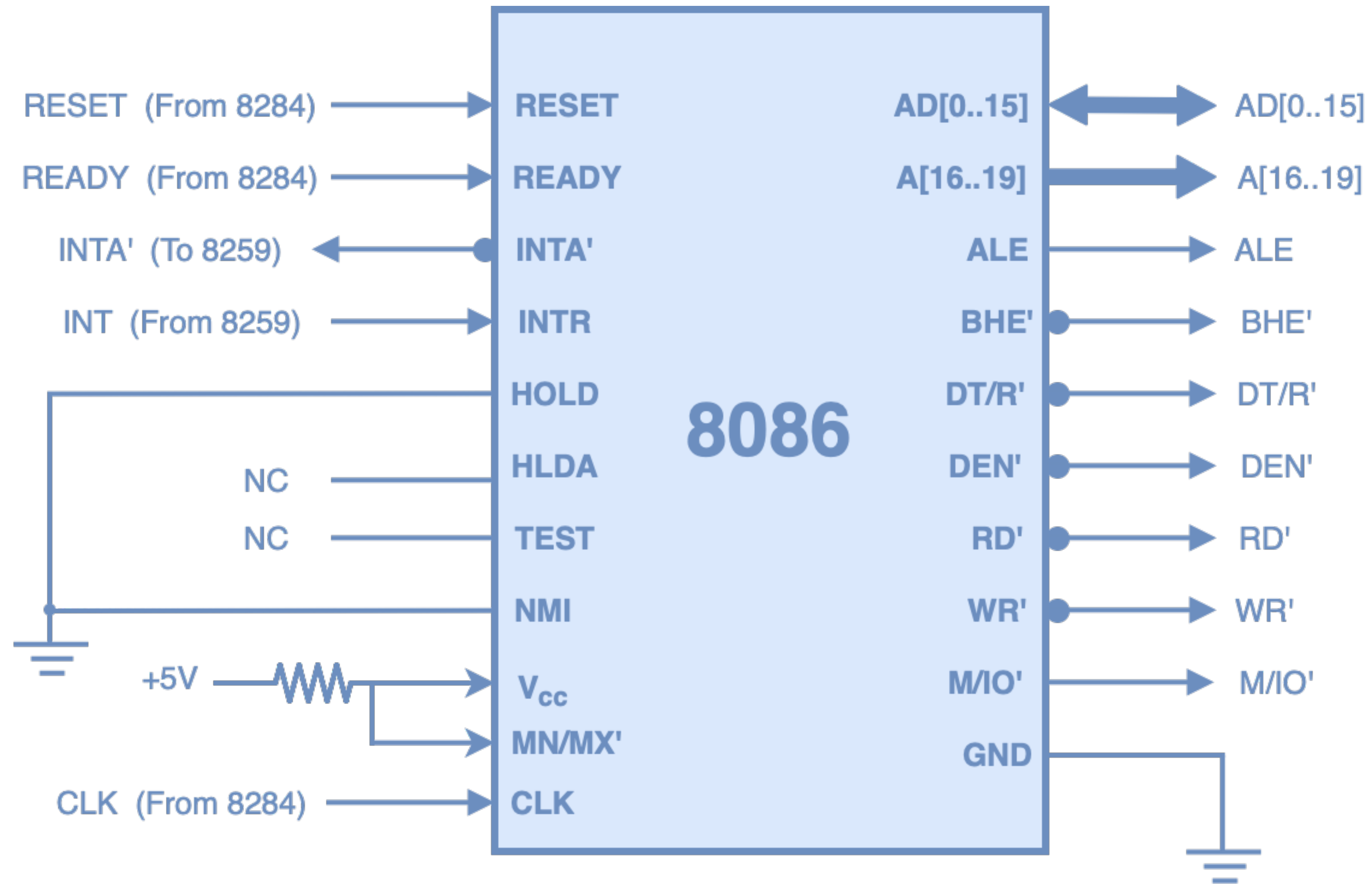
Intel 8086
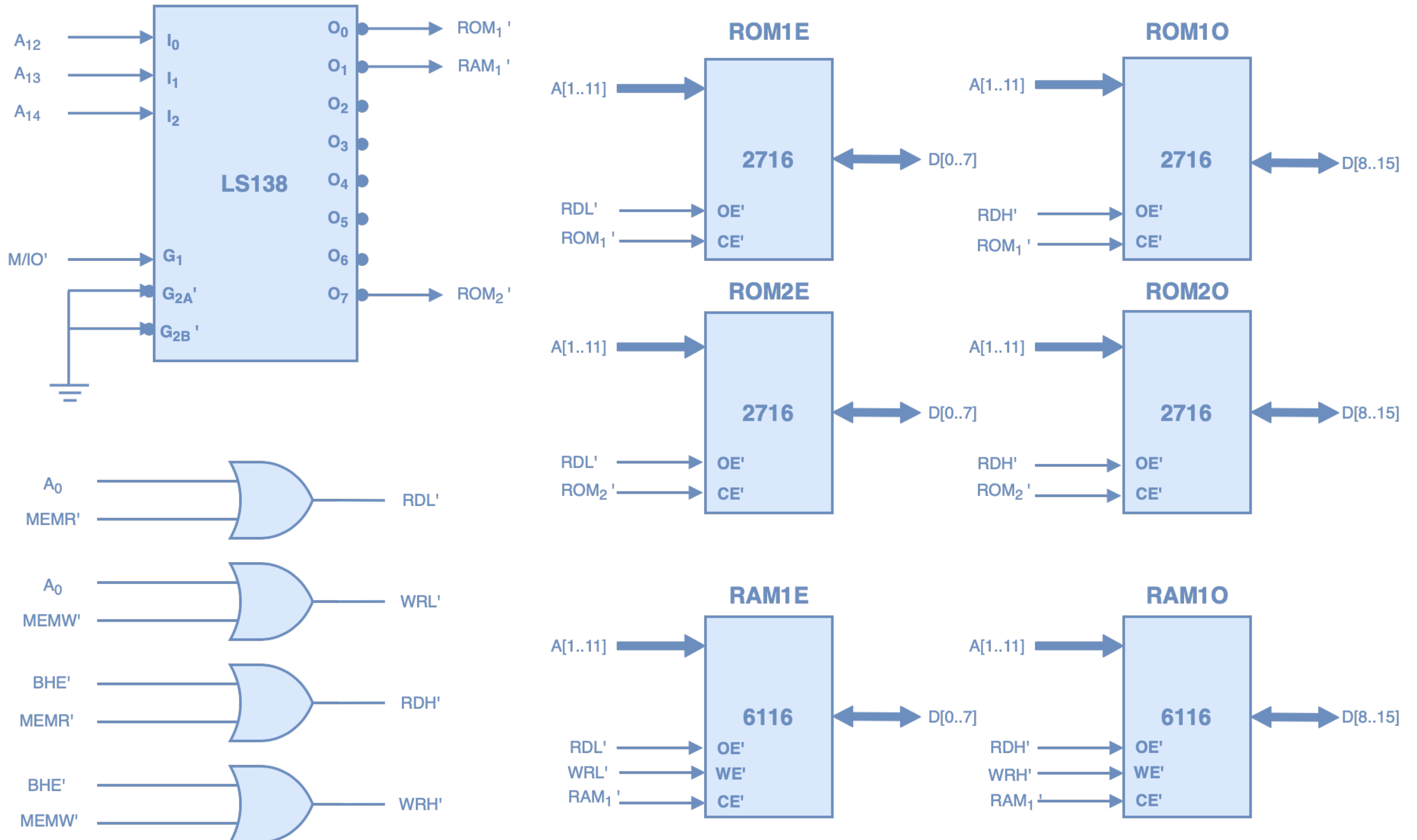
System Bus of 8086 (Address and Data)

Address Line Demultiplexing

Data Line Demultiplexing

System Bus of 8086 (Control)

LS244

M/IO'
RD'
WR'
OE'

M/IO'
RD'
WR'

IOR'
IOW'
MEMR'
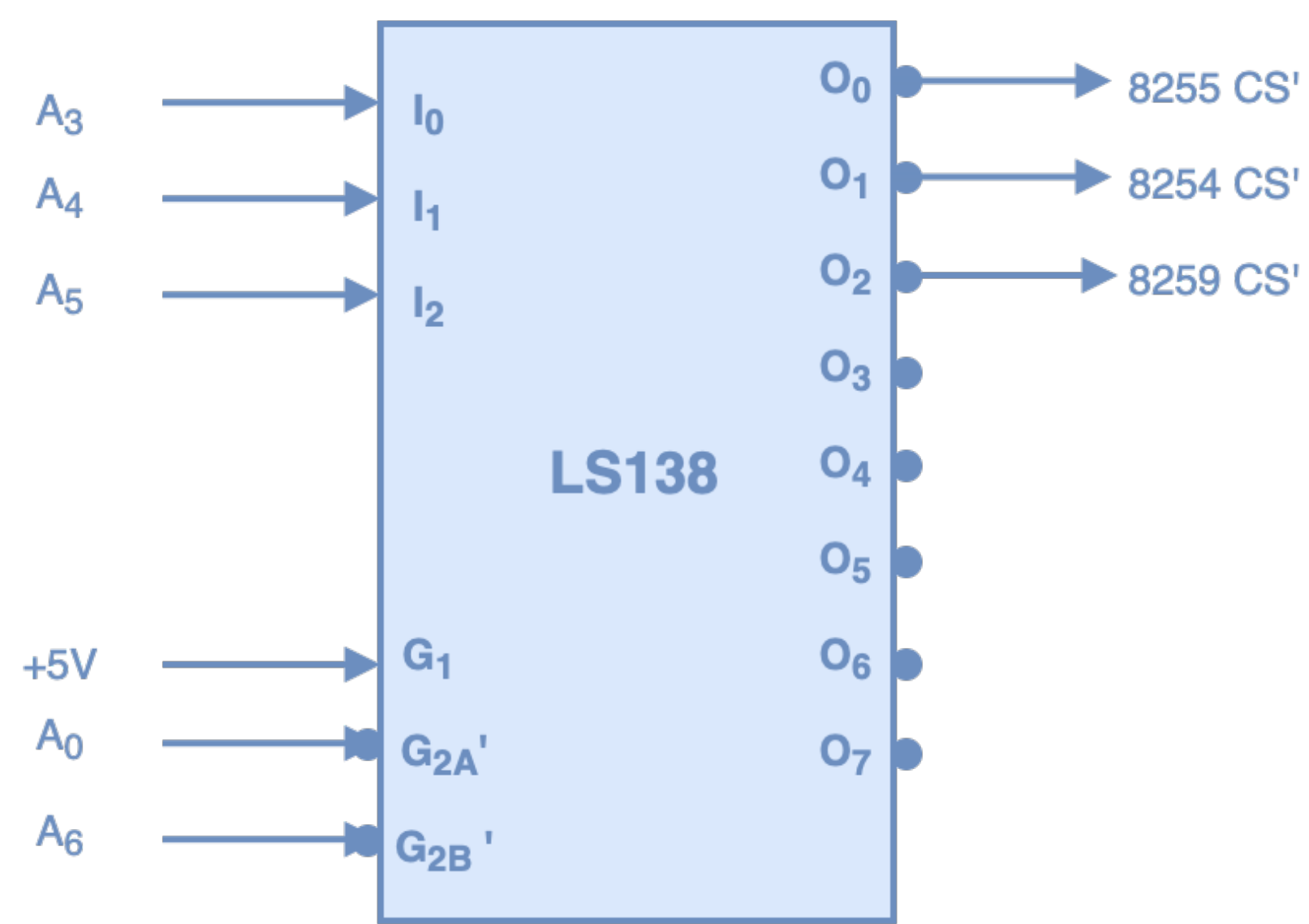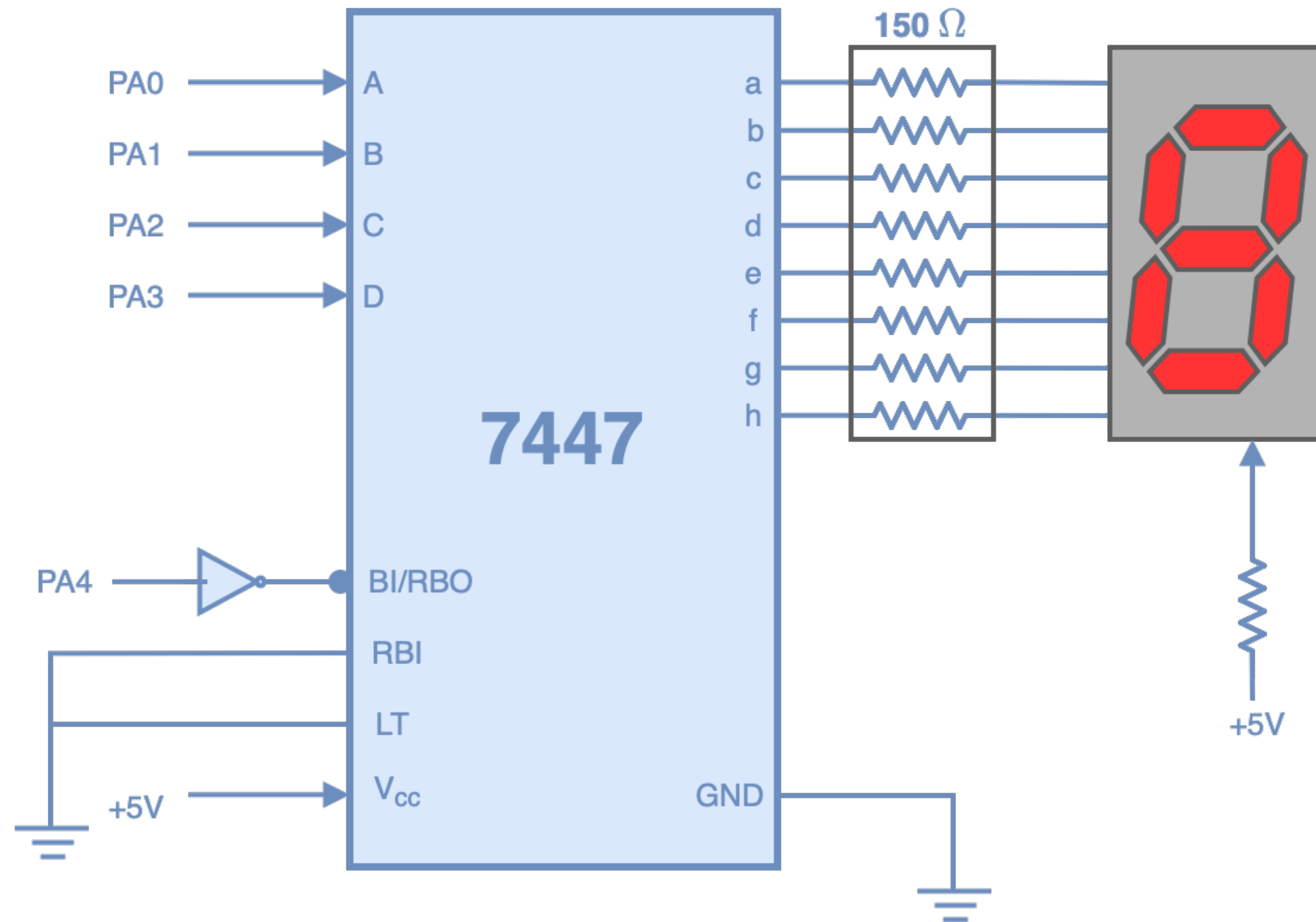MEMW'
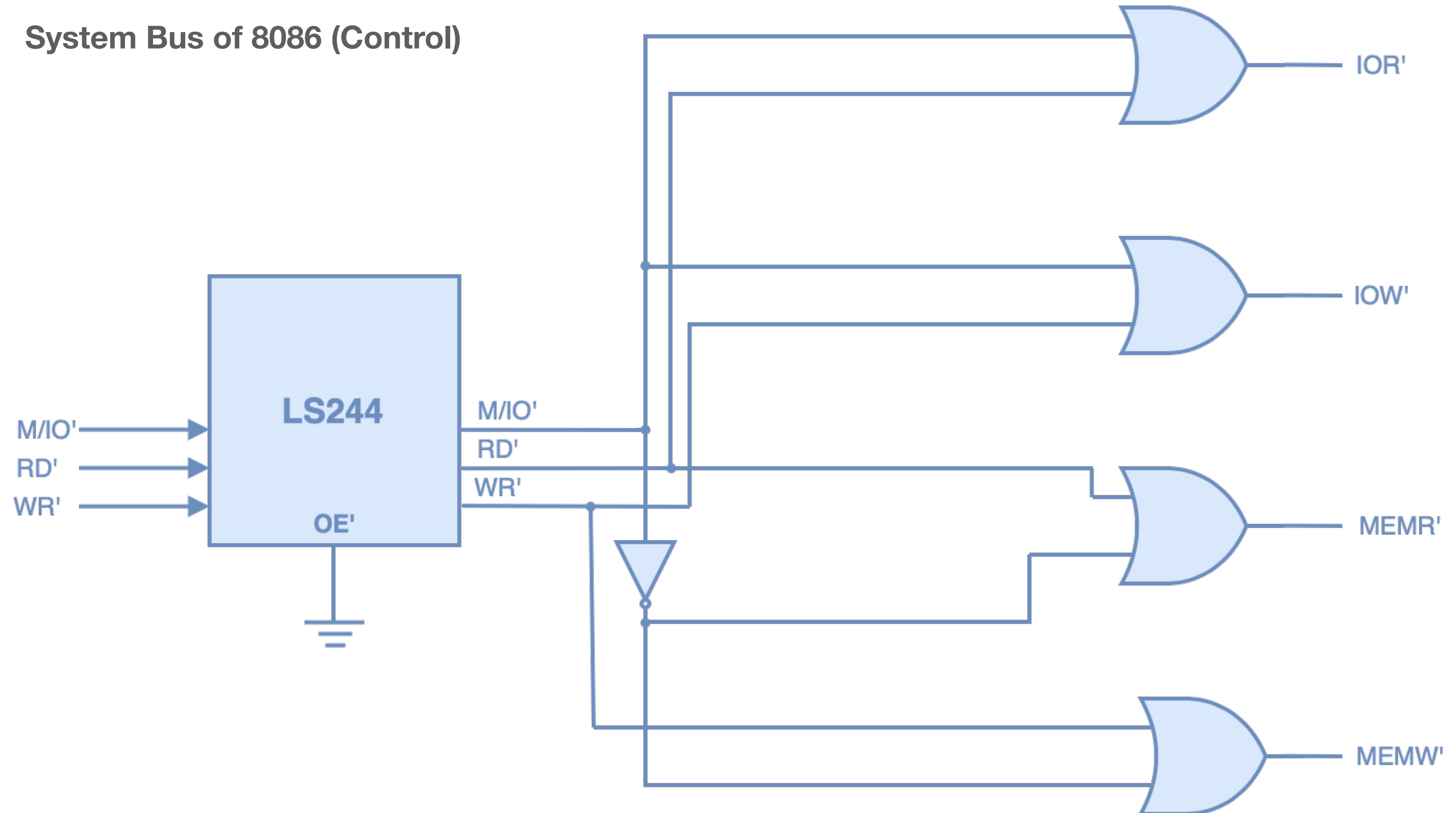
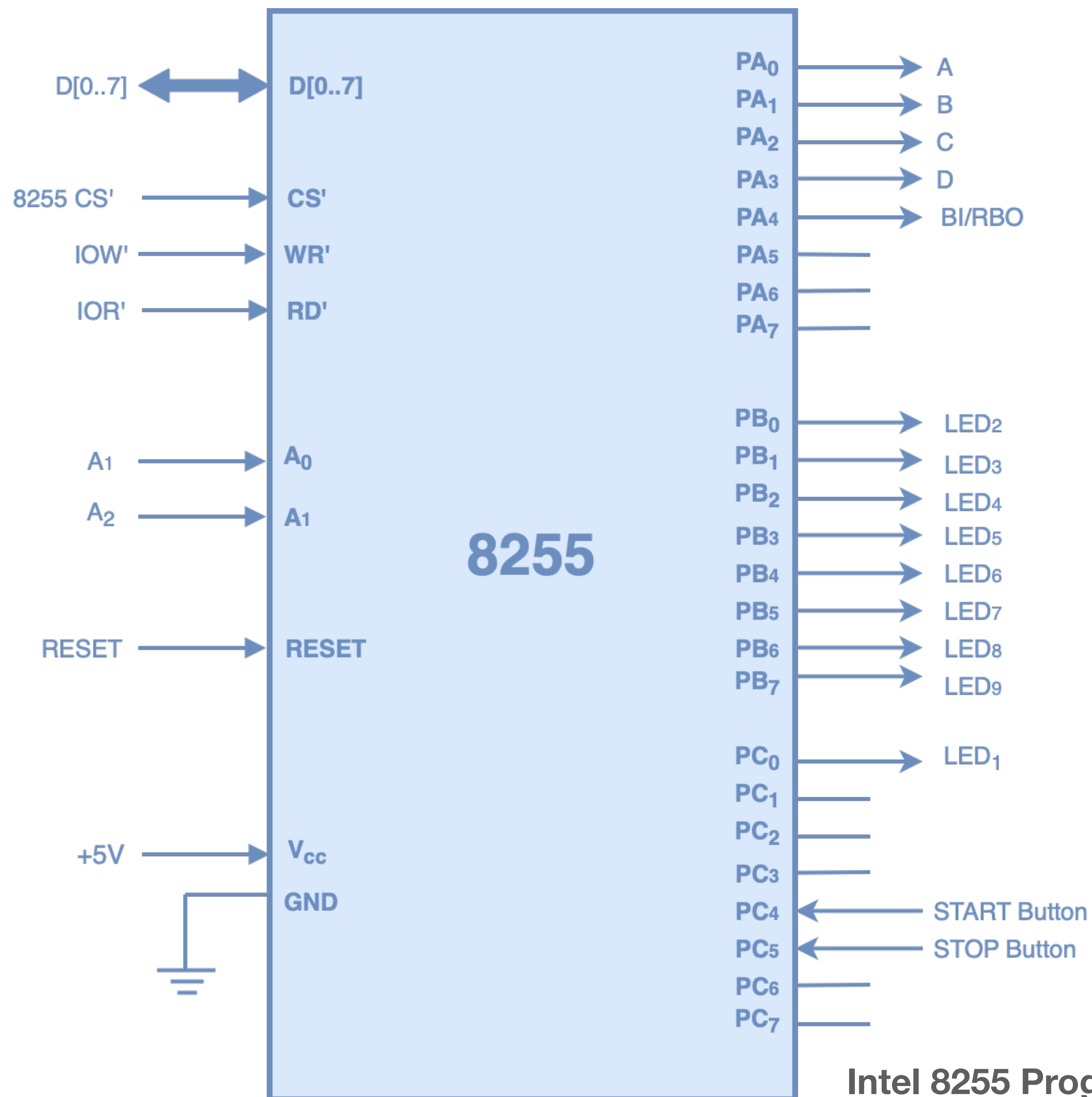Control Signal Generation

Memory Decoder and Memory Chip Connections

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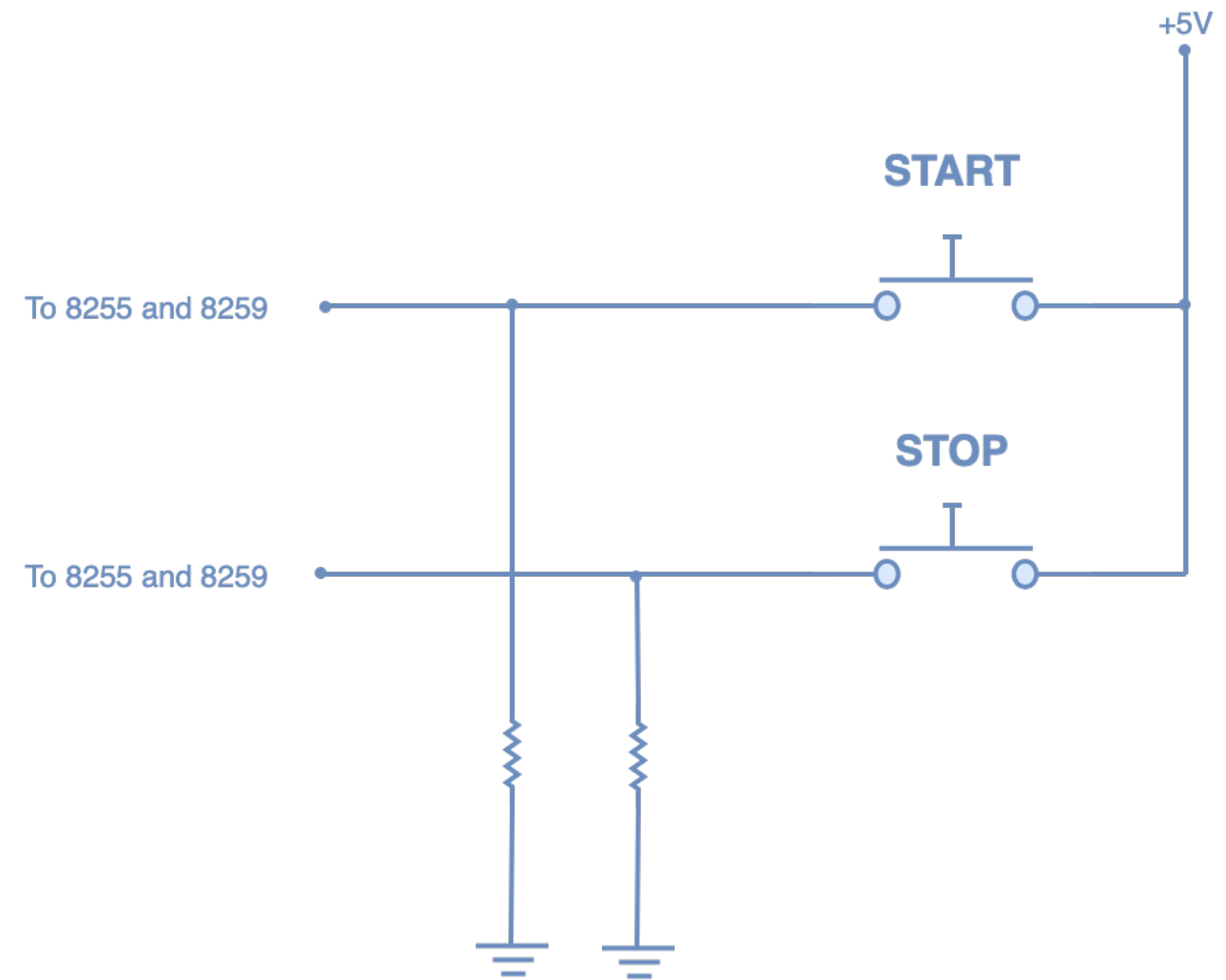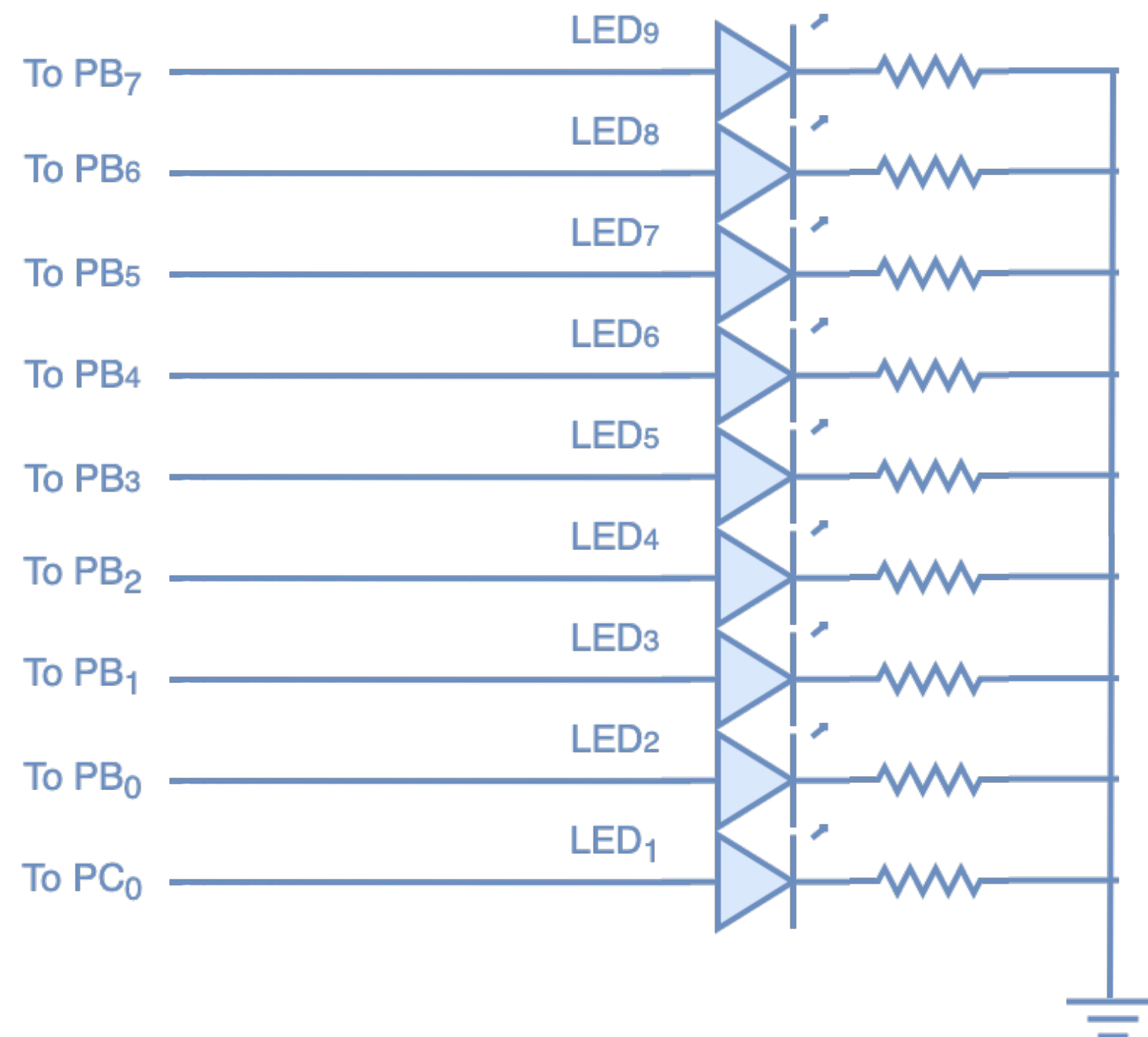
I/O Decoder and I/O Devices

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BCD-to-seven-segment Decoder Connections

Addresses
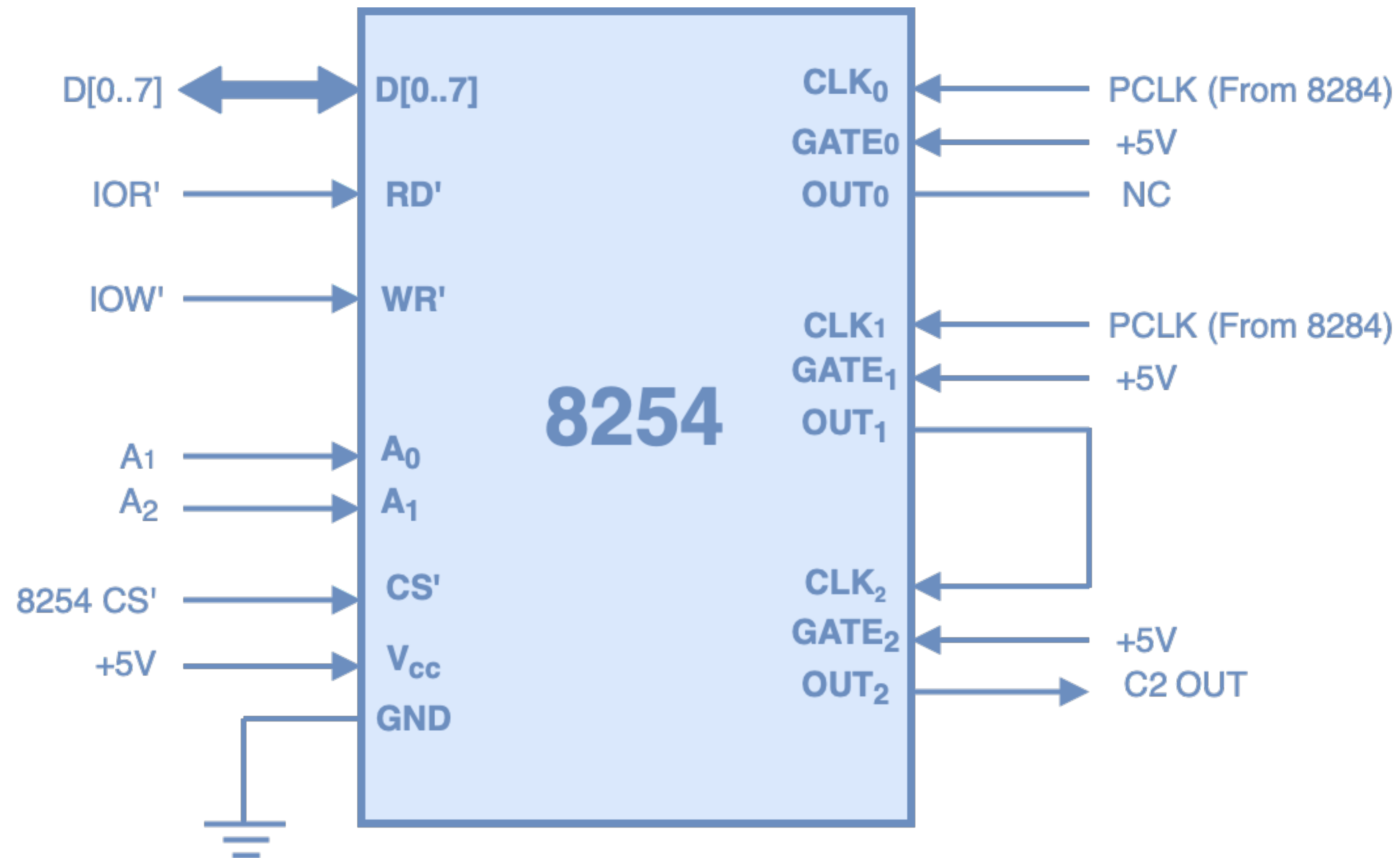- Port A: 00h
- Port B: 02h
- Port C: 04h
- Control Register: 06h

I/O Devices Connected
- Port A (Output)
    - PA_0 - PA_3: BCD inputs of IC 7447
    - PA_4: BI/RBO of IC 7447
- Port B (Output): LED_2 - LED_9
- Port C (Upper: Input, Lower: Output)
    - PC_0: LED_1
    - PC_4: START button
    - PC_5: STOP button

Intel 8255 Programmable Peripheral Interface   11

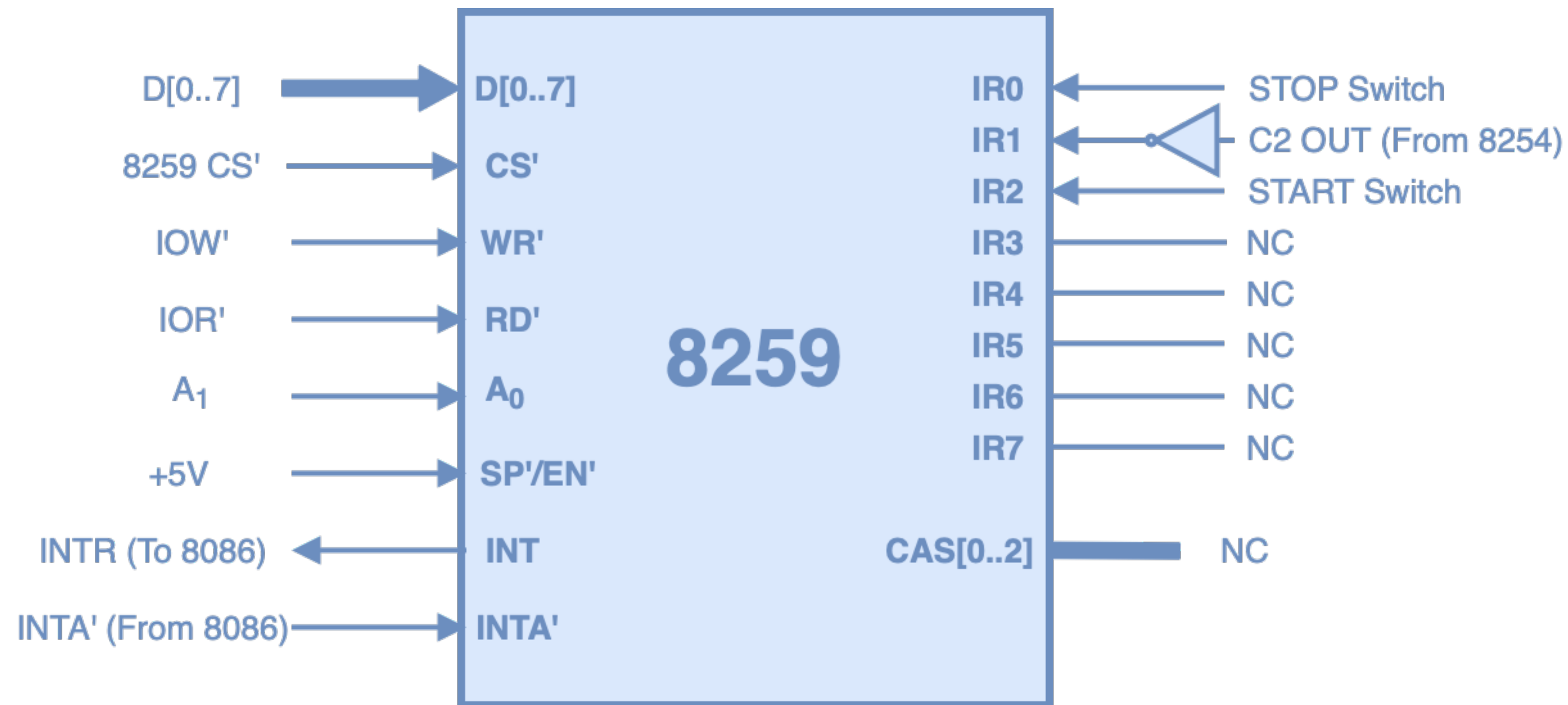**Intel 8254 Programmable Interval Timer**

Addresses
- Counter 0: 08h
- Counter 1: 0Ah
- Counter 2: 0Ch
- Control Register: 0Eh

Configuration
- Counter 0: Mode 2 (Value: 160d)
- Counter 1: Mode 2 (Value: 62500d)
- Counter 2: Mode 2
    1. Value: 160d + readout from C0 (Random delay)
    2. Value: 1d for 50ms interrupt

Outputs
- OUT_0 not used
- OUT_1 at 40 Hz
- OUT_2 at
    1. 0.25Hz - 0.125Hz (random delay) (Time period: 4 - 8 seconds)
    2. 20 Hz (for lighting every successive LED) (Time period: 50ms)

Intel 8259 Programmable Interrupt Controller

Inputs
- IR0: STOP Switch
- IR1: C2 OUT (OUT from counter 2)
- IR2: START Switch

Addresses
10h - 12h