

Spirit Level Reaction Time Tester

Hardware Design

Group 25

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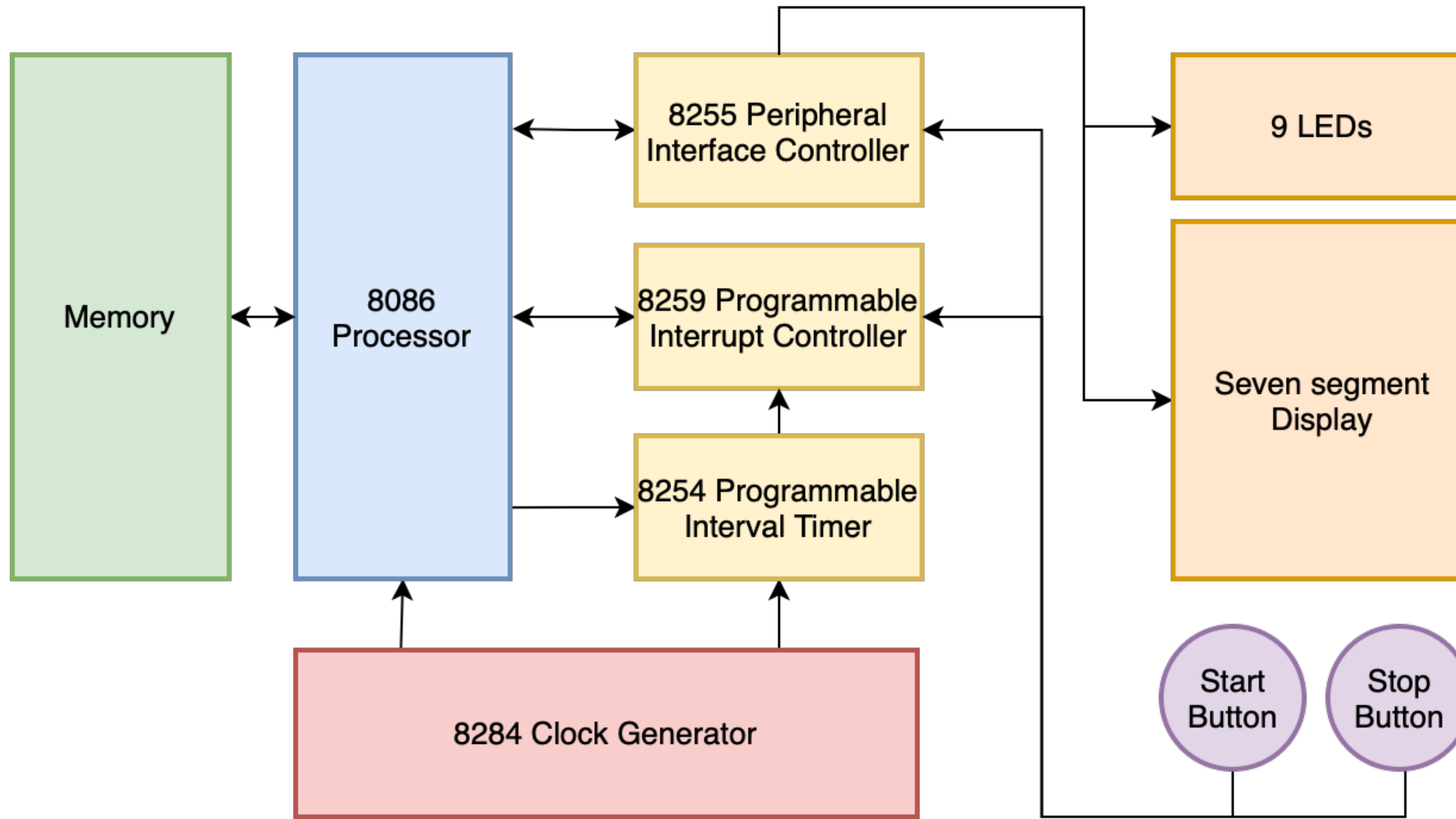
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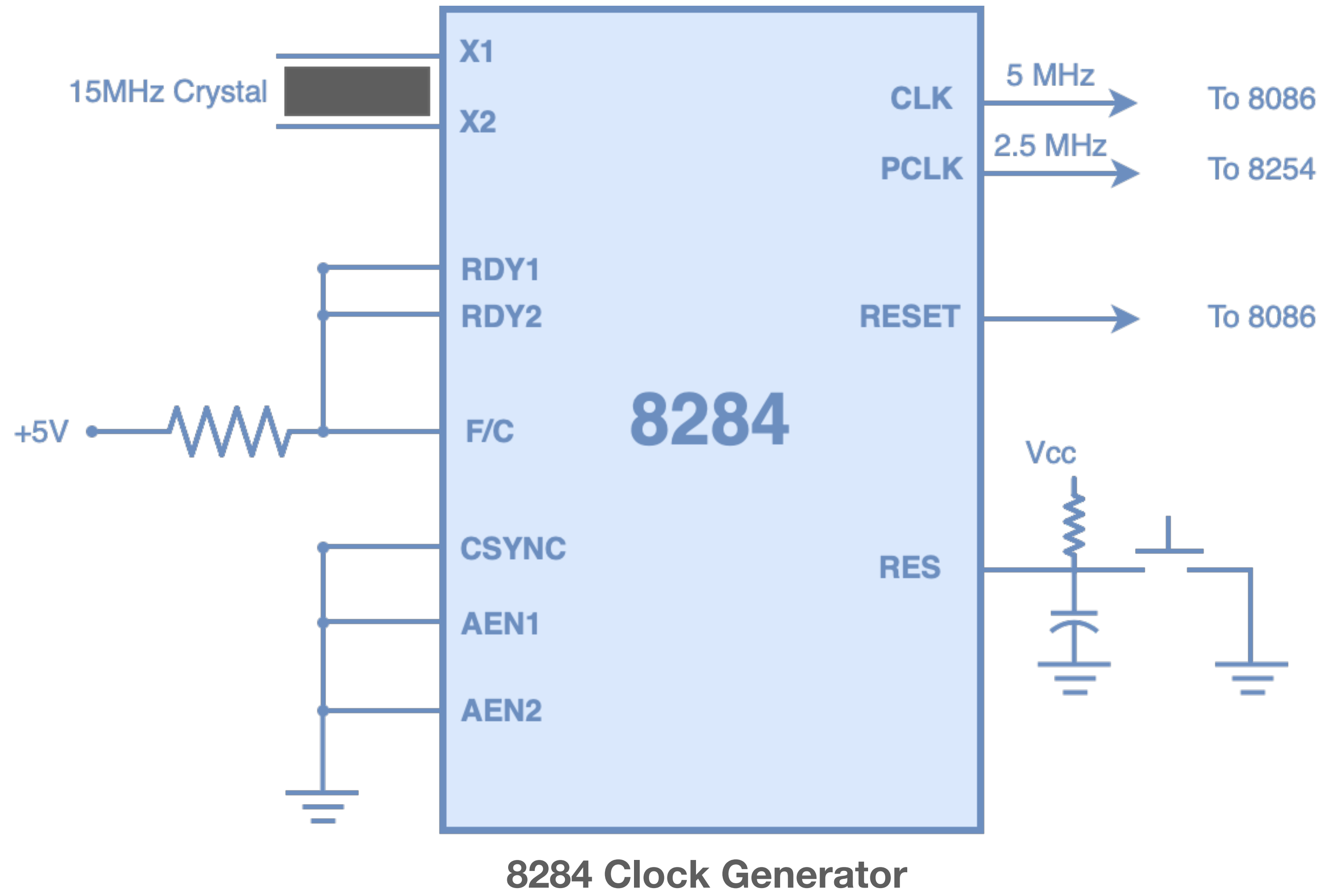
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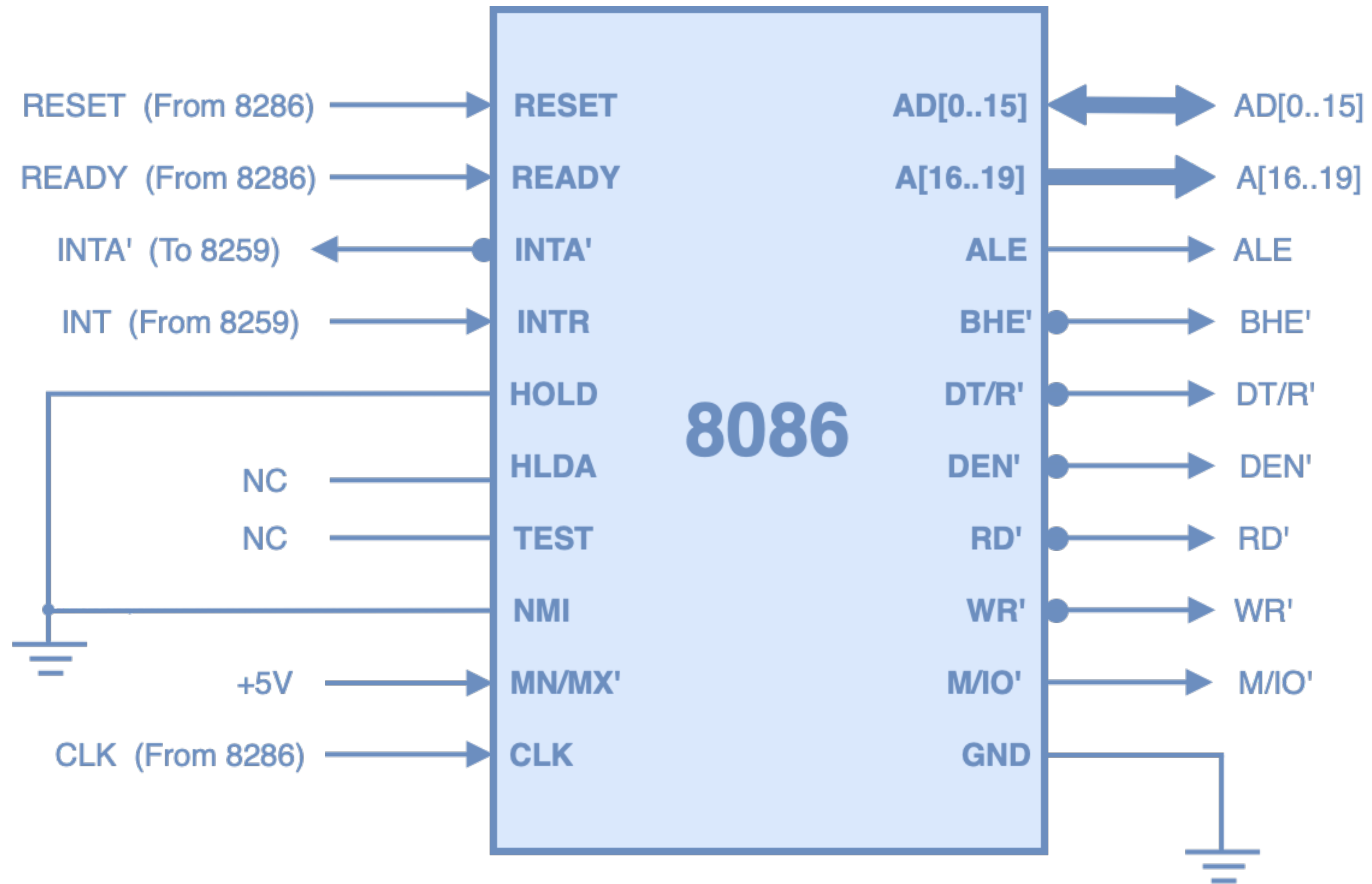
A High-Level Block Diagram for the system



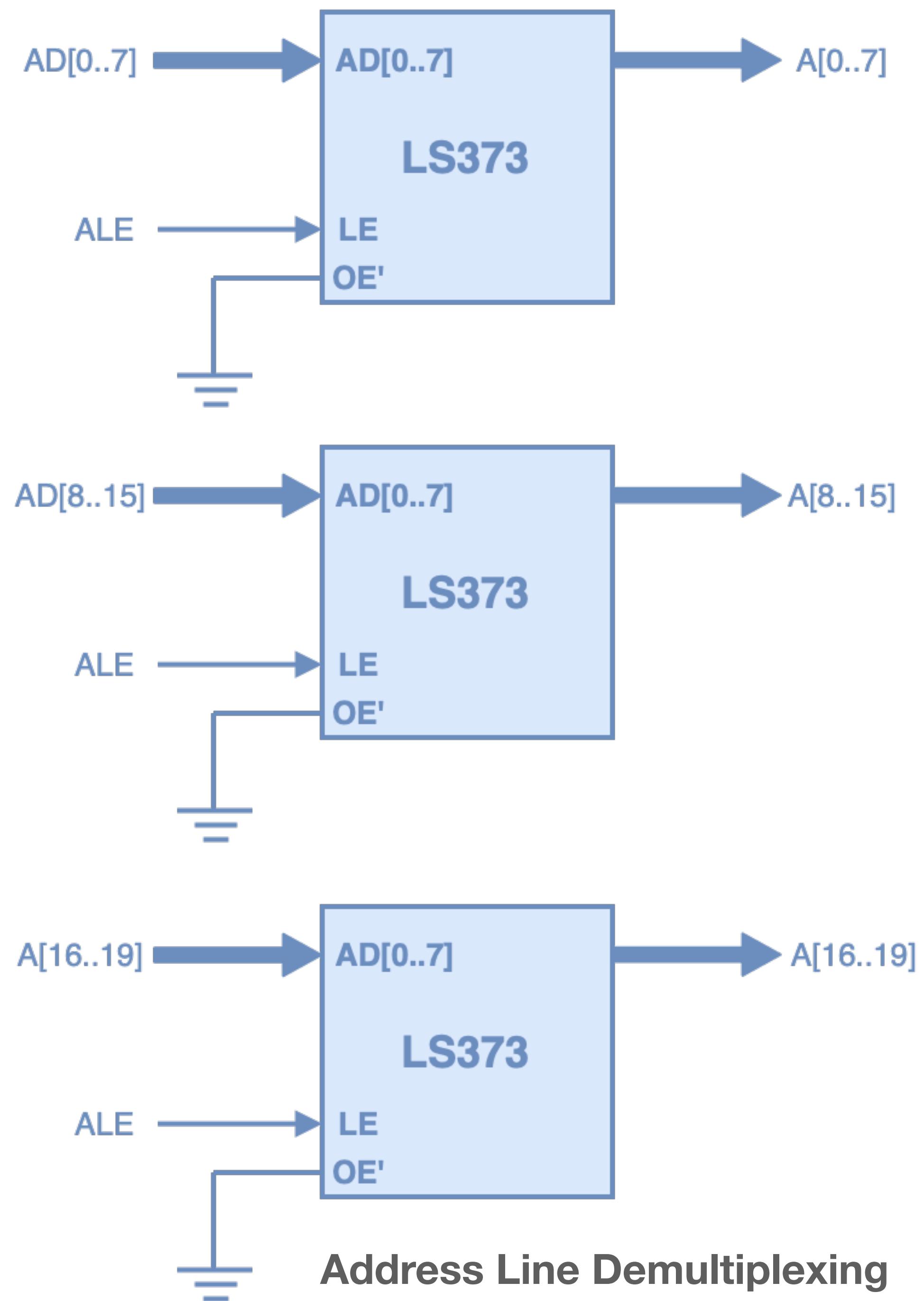


Signals Generated

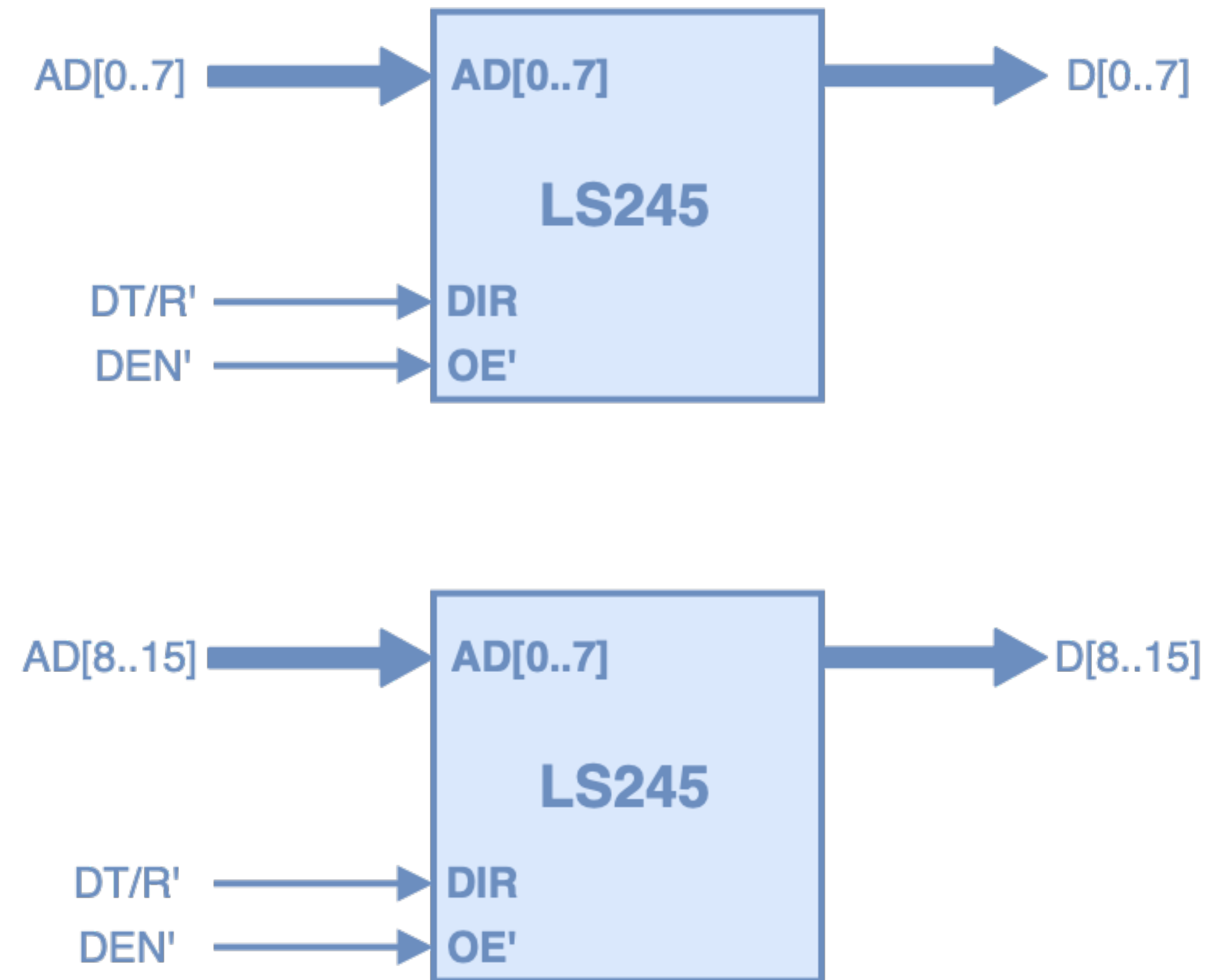
- CLK at 5MHz
- PCLK at 2.5 MHz
- RESET



Intel 8086

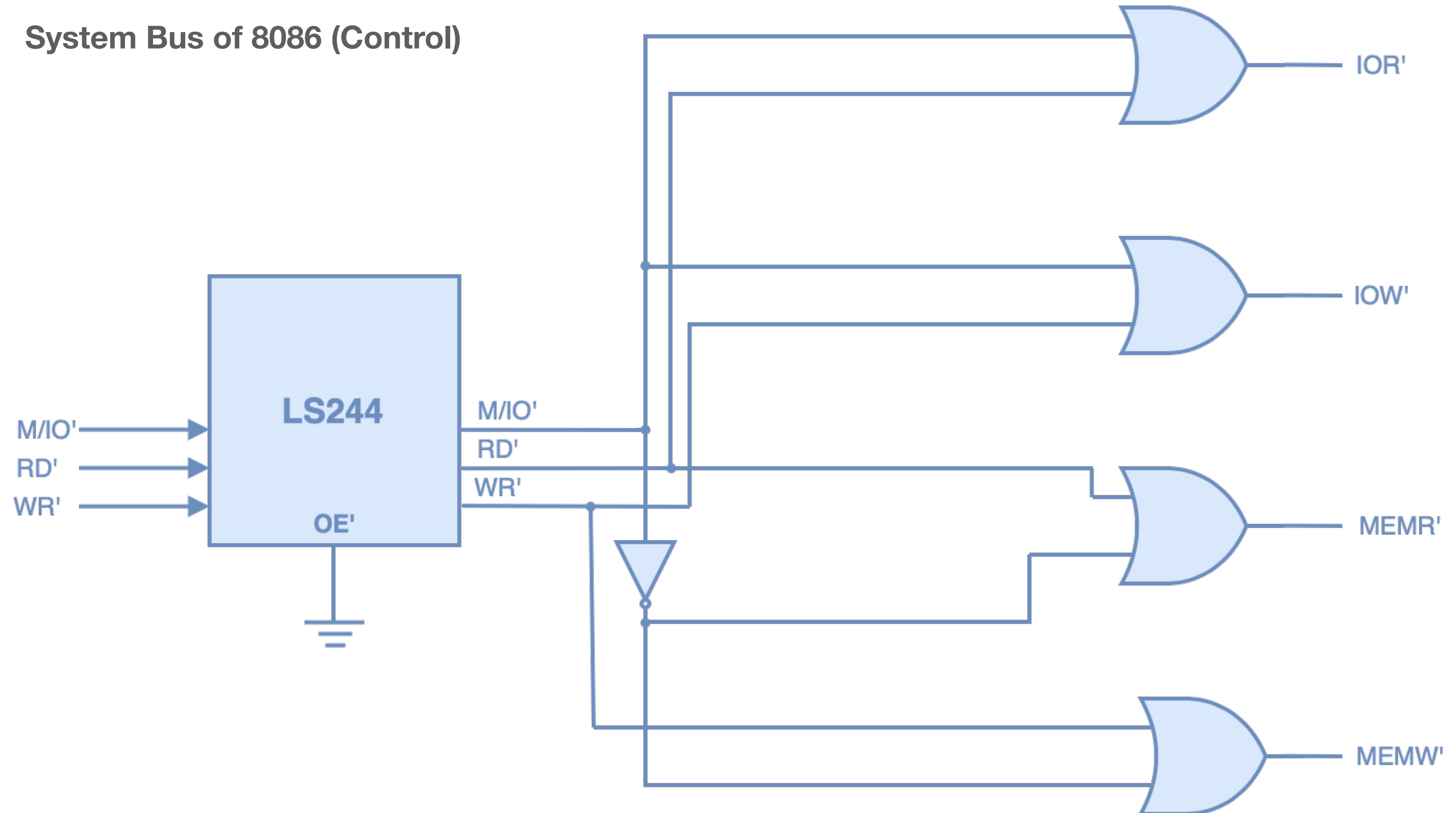


System Bus of 8086 (Address and Data)

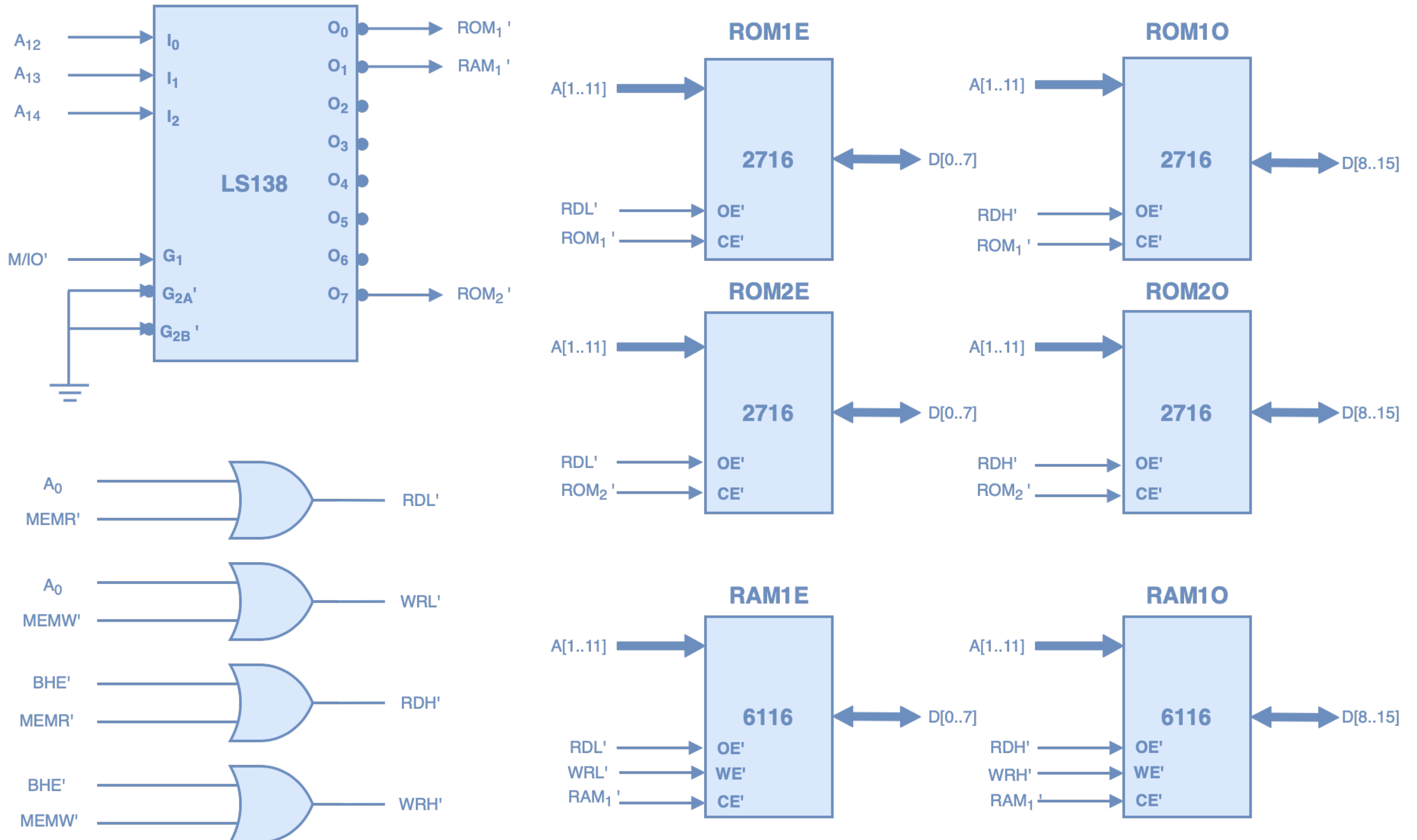


Data Line Demultiplexing

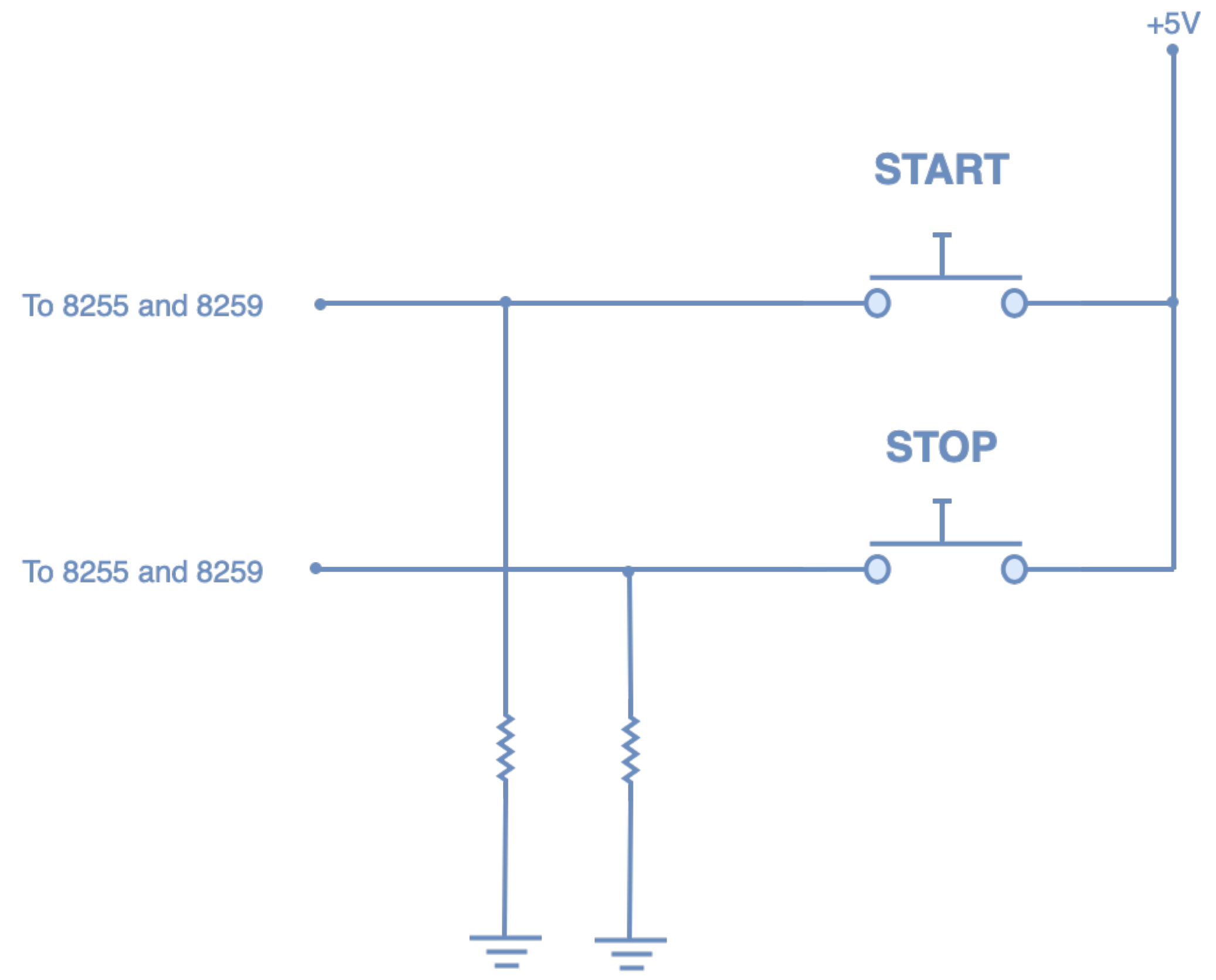
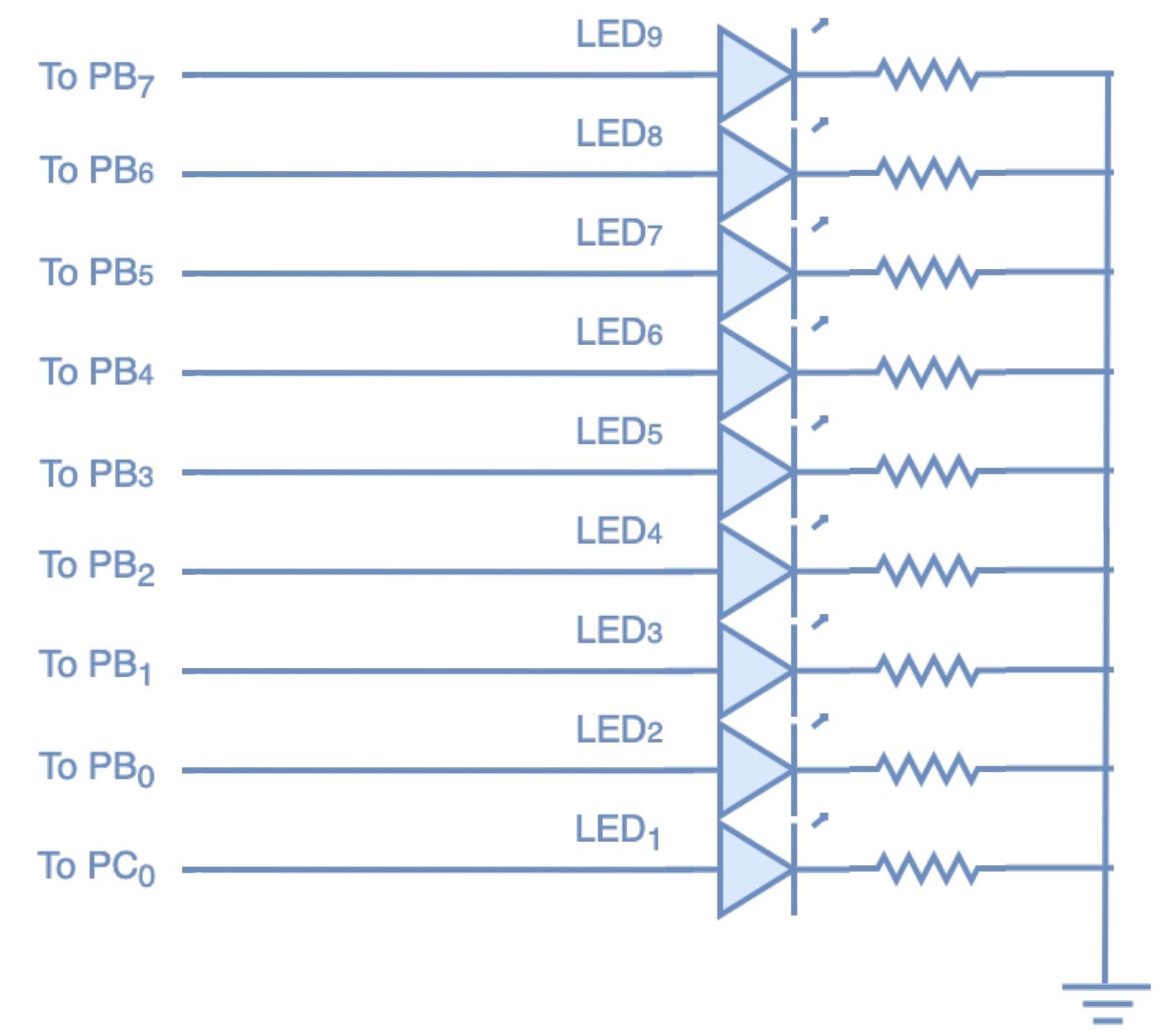
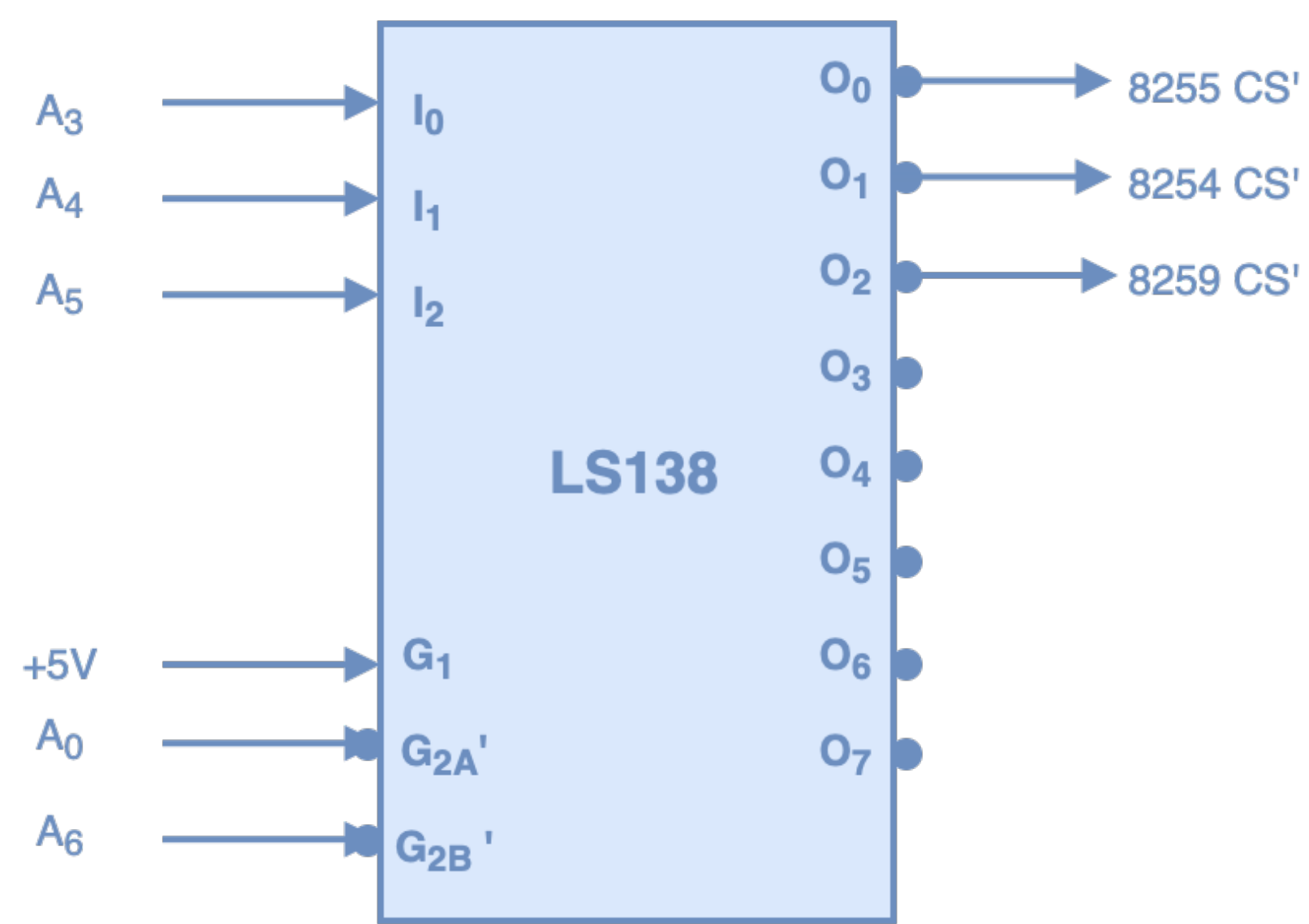
System Bus of 8086 (Control)



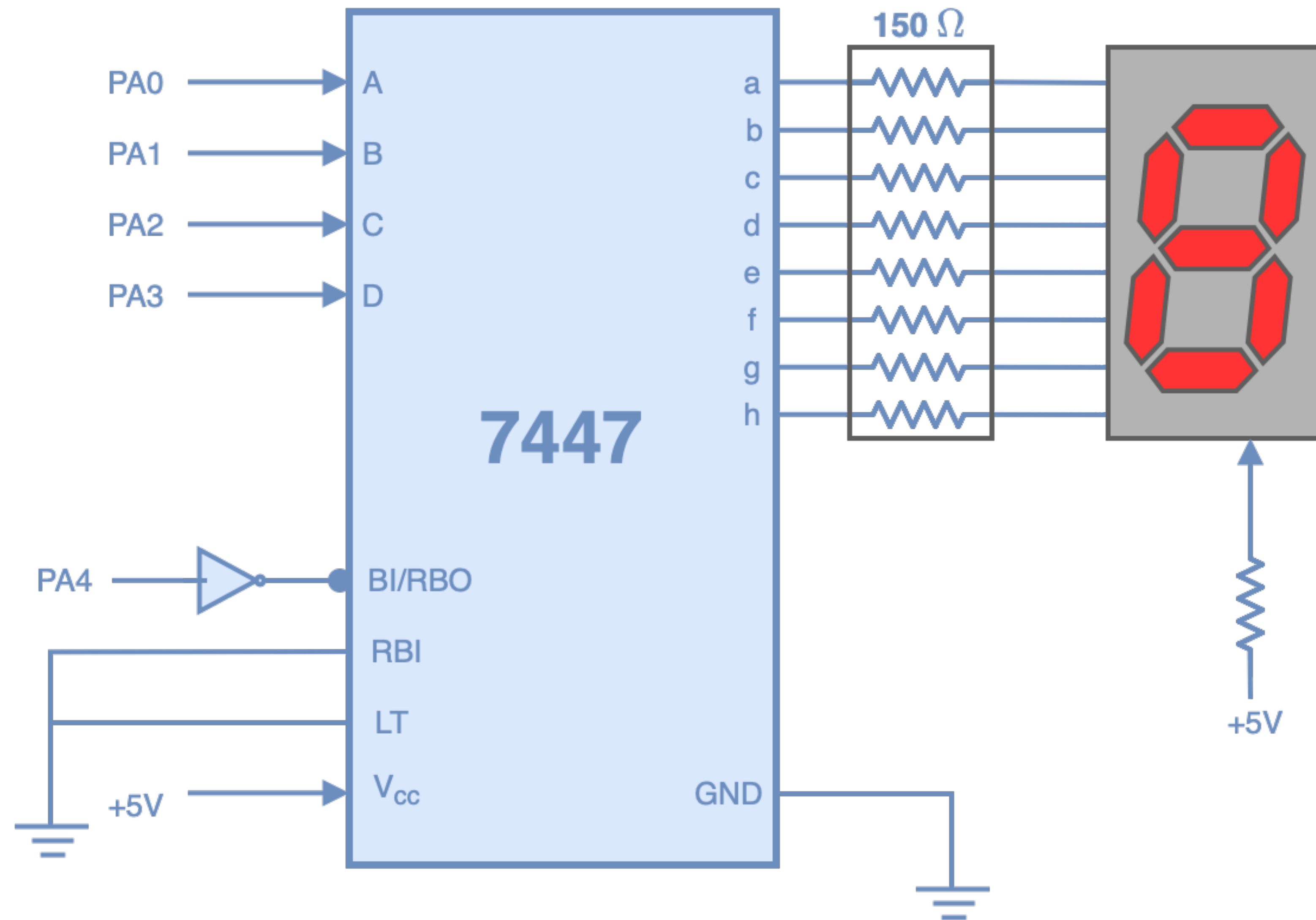
Control Signal Generation



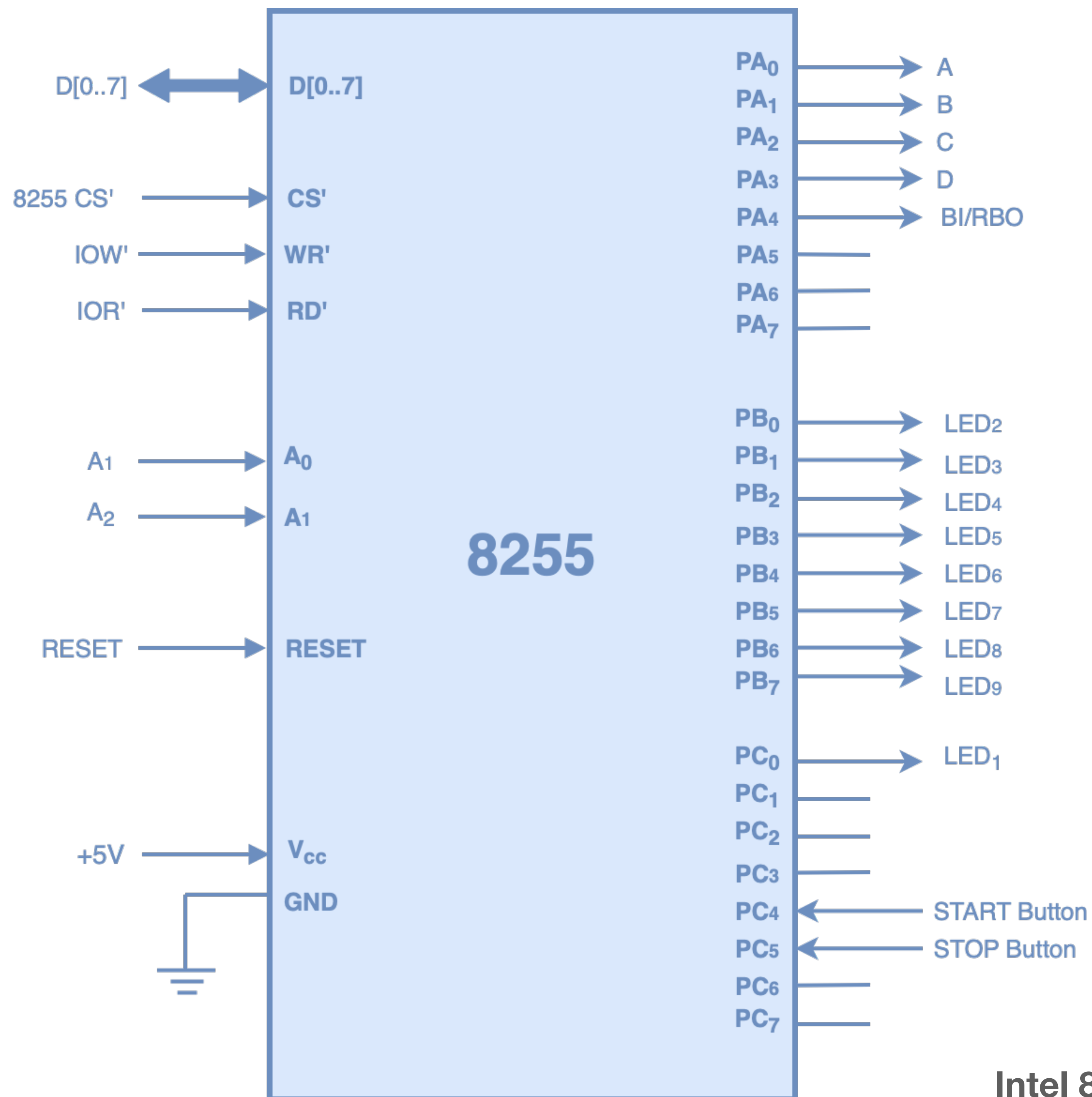
Memory Decoder and Memory Chip Connections



I/O Decoder and I/O Devices



BCD-to-seven-segment Decoder Connections

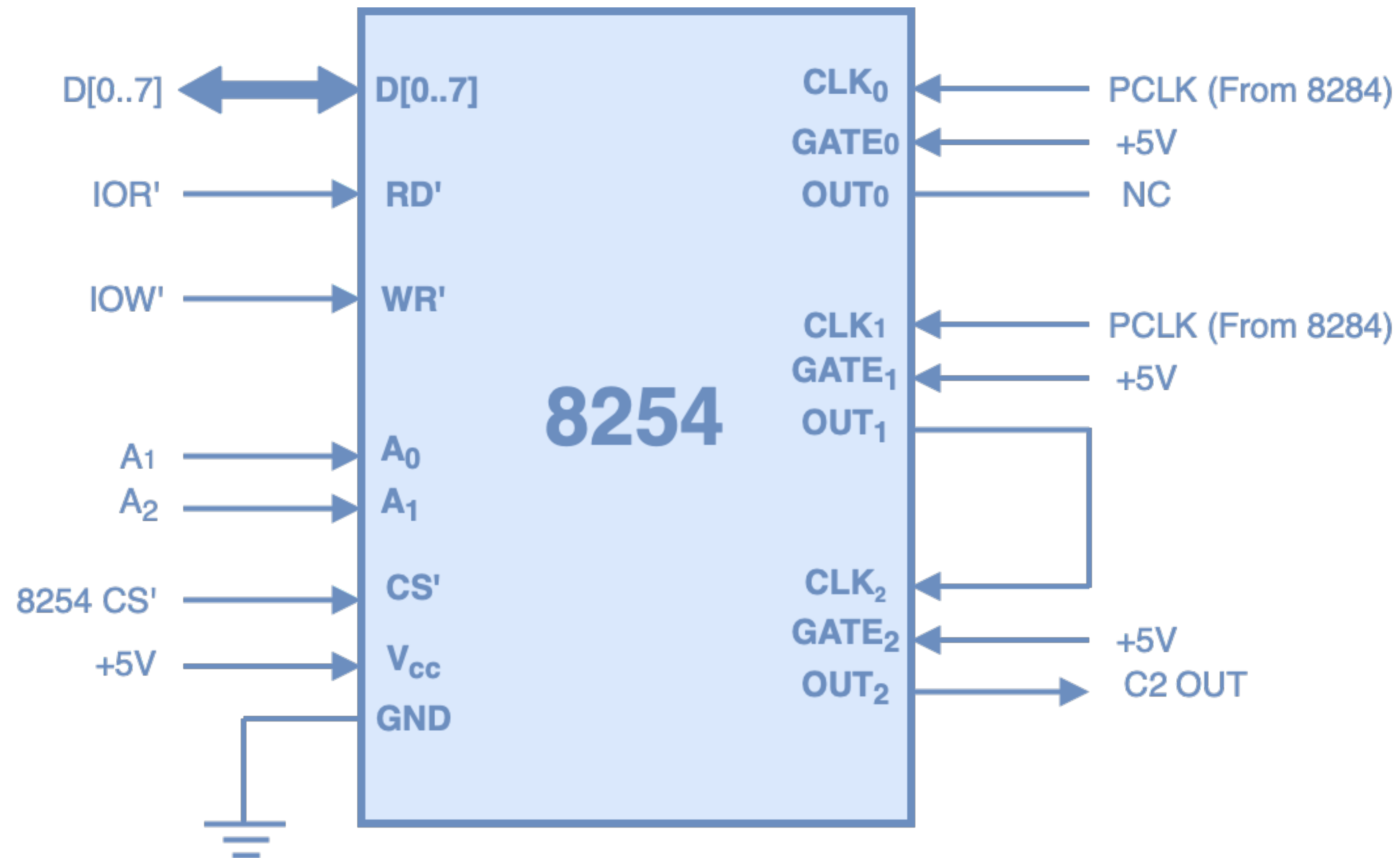


Addresses

- Port A: 00h
- Port B: 02h
- Port C: 04h
- Control Register: 06h

I/O Devices Connected

- Port A (Output)
 - PA₀ - PA₃: BCD inputs of IC 7447
 - PA₄: BI/RBO of IC 7447
- Port B (Output): LED₂ - LED₉
- Port C (Upper: Input, Lower: Output)
 - PC₀: LED₁
 - PC₄: START button
 - PC₅: STOP button



Intel 8254 Programmable Interval Counter

Addresses

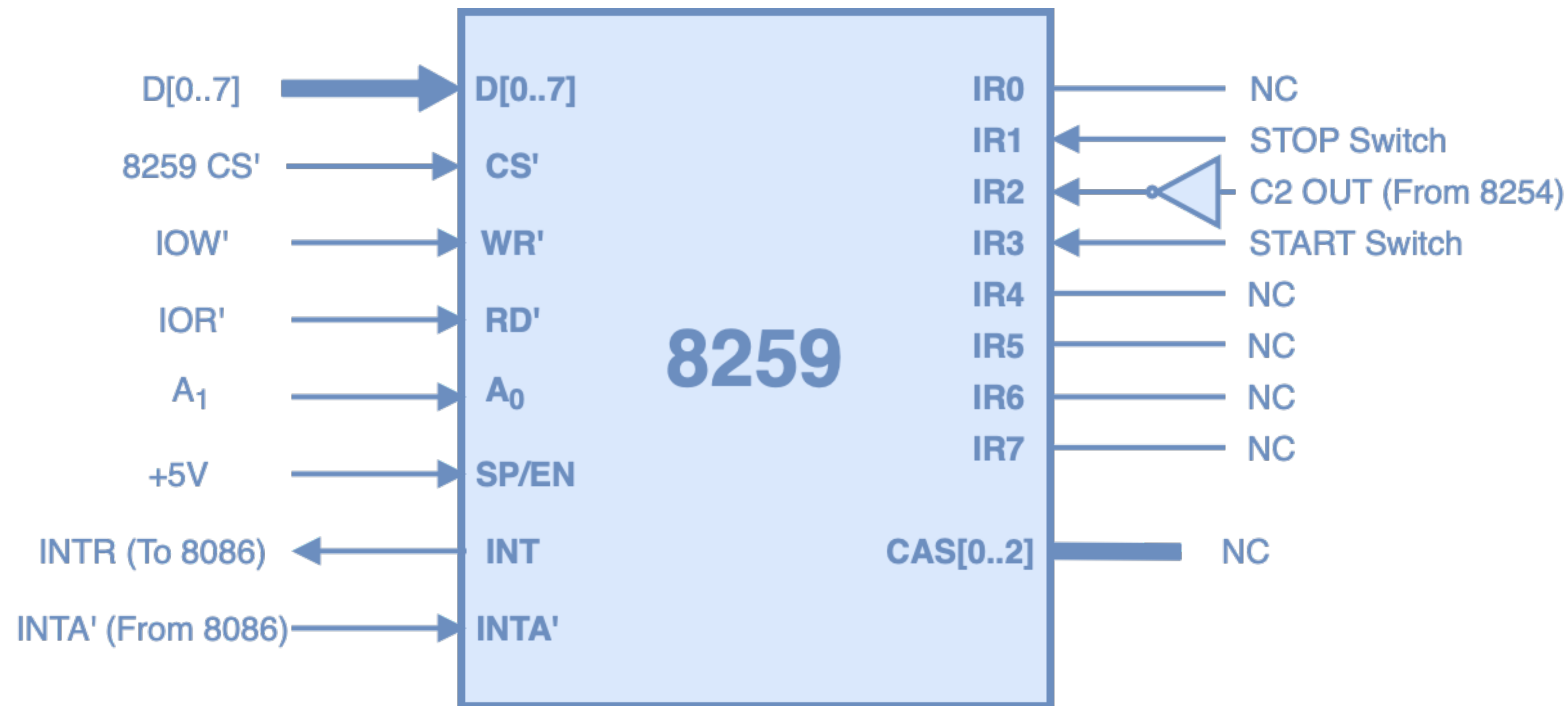
- Counter 0: 08h
- Counter 1: 0Ah
- Counter 2: 0Ch
- Control Register: 0Eh

Configuration

- Counter 0: Mode 2 (Seed: 161d)
- Counter 1: Mode 2 (Seed: 62500d)
- Counter 2: Mode 2
 1. Seed: 160d + readout from C0 (Random delay)
 2. Seed: 2d for 50ms interrupt

Outputs

- OUT₀ not used
- OUT₁ at 40 Hz
- OUT₂ at
 1. 0.25Hz - 0.125Hz (random delay)
 2. 20 Hz (for lighting every successive LED)



Intel 8259 Programmable Interrupt Controller

Inputs

- IR1: STOP Switch
- IR2: C2 OUT (OUT from counter 2)
- IR3: START Switch

Addresses

10h - 12h