Spirit Level Reaction Time Tester

Hardware Design

Group 25

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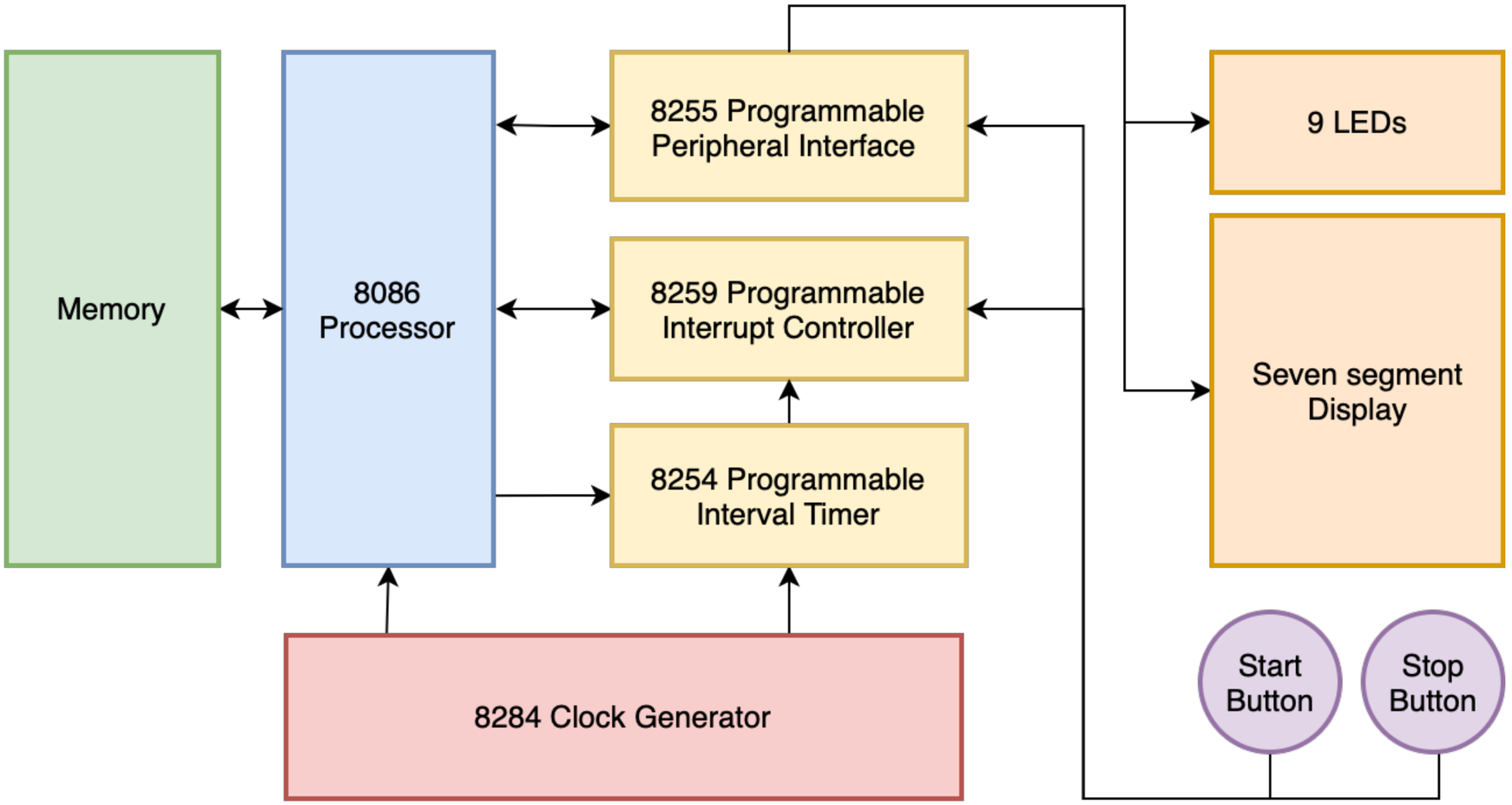
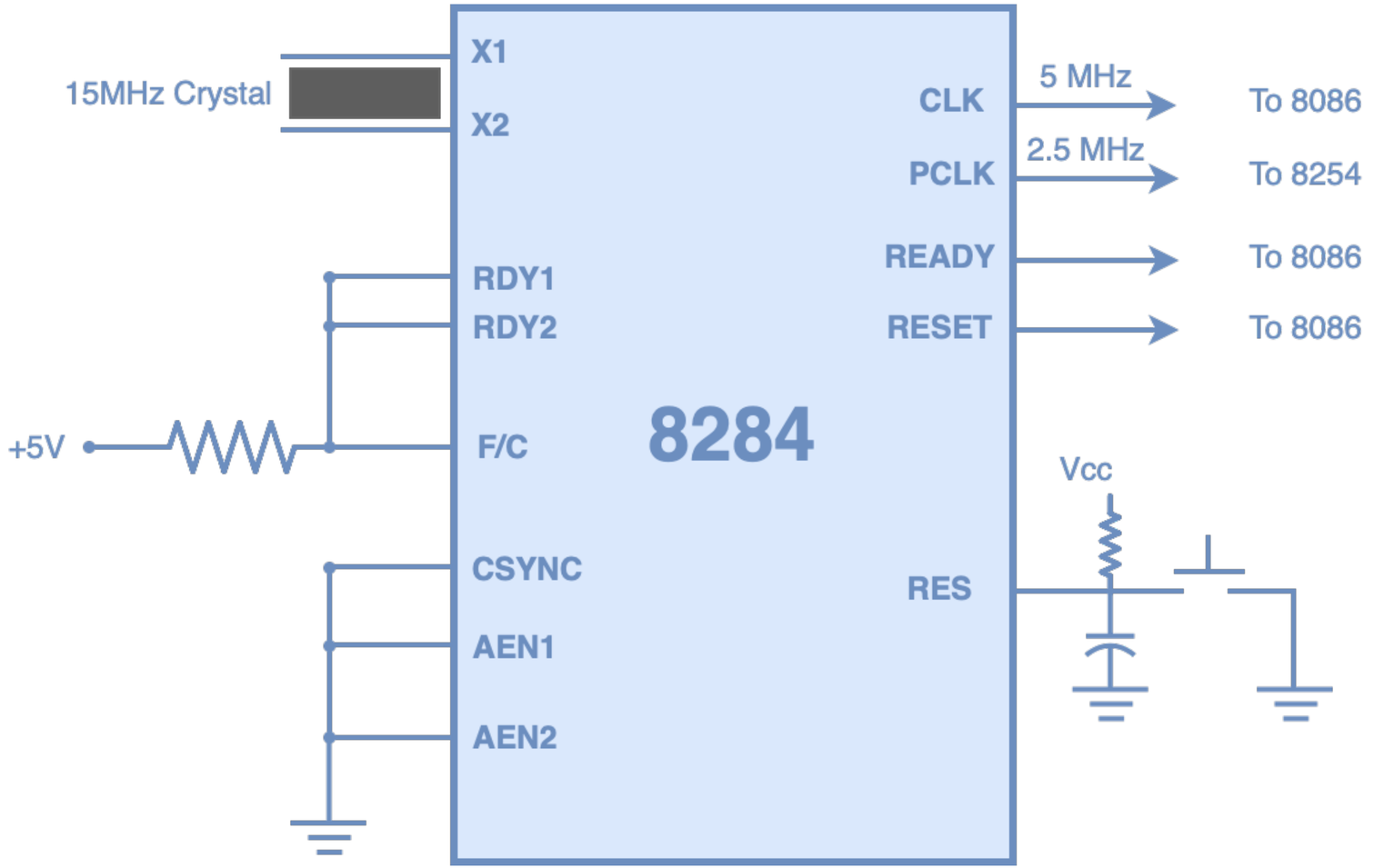
A High-Level Block Diagram for the system

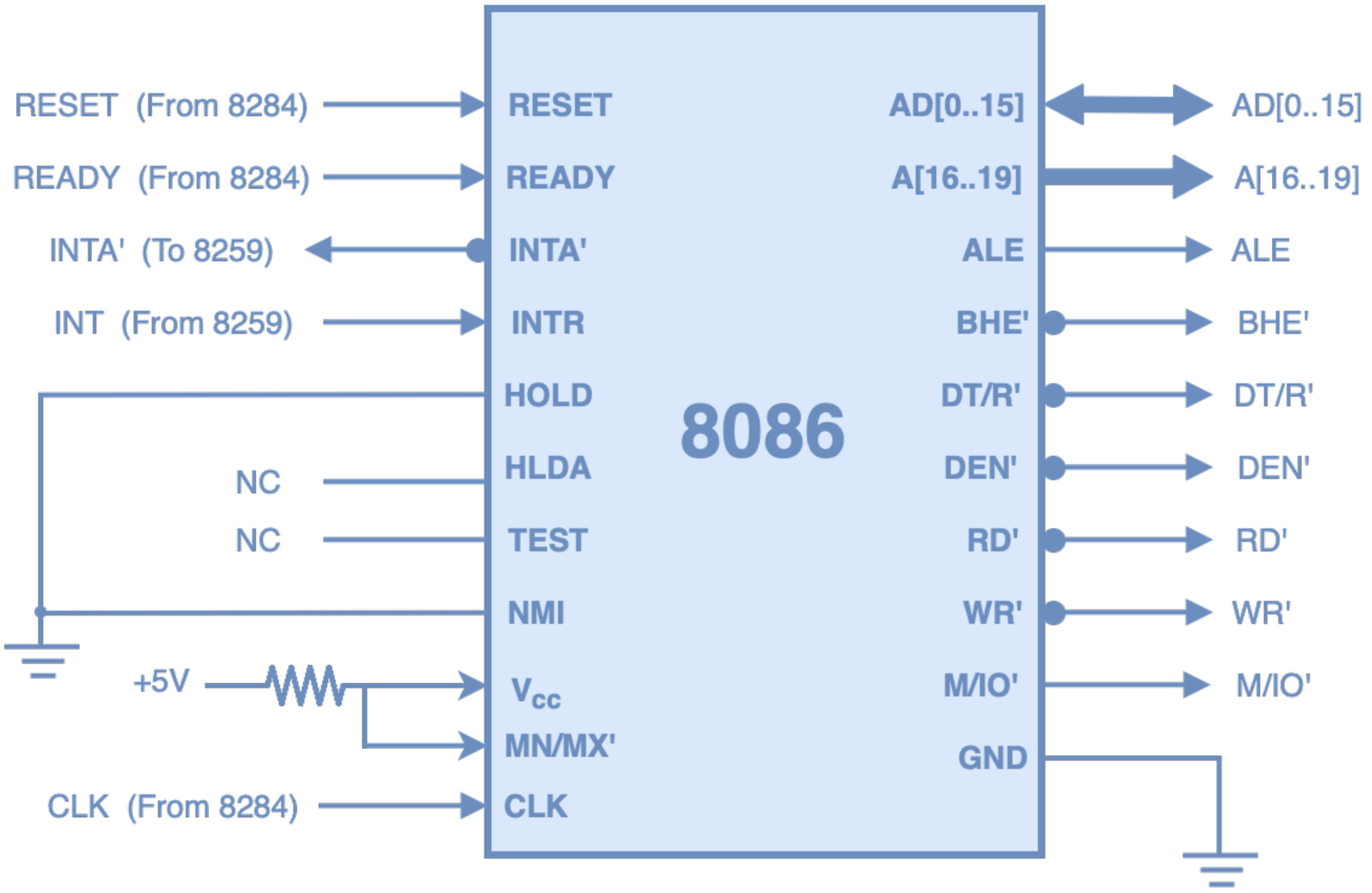




8284 Clock Generator

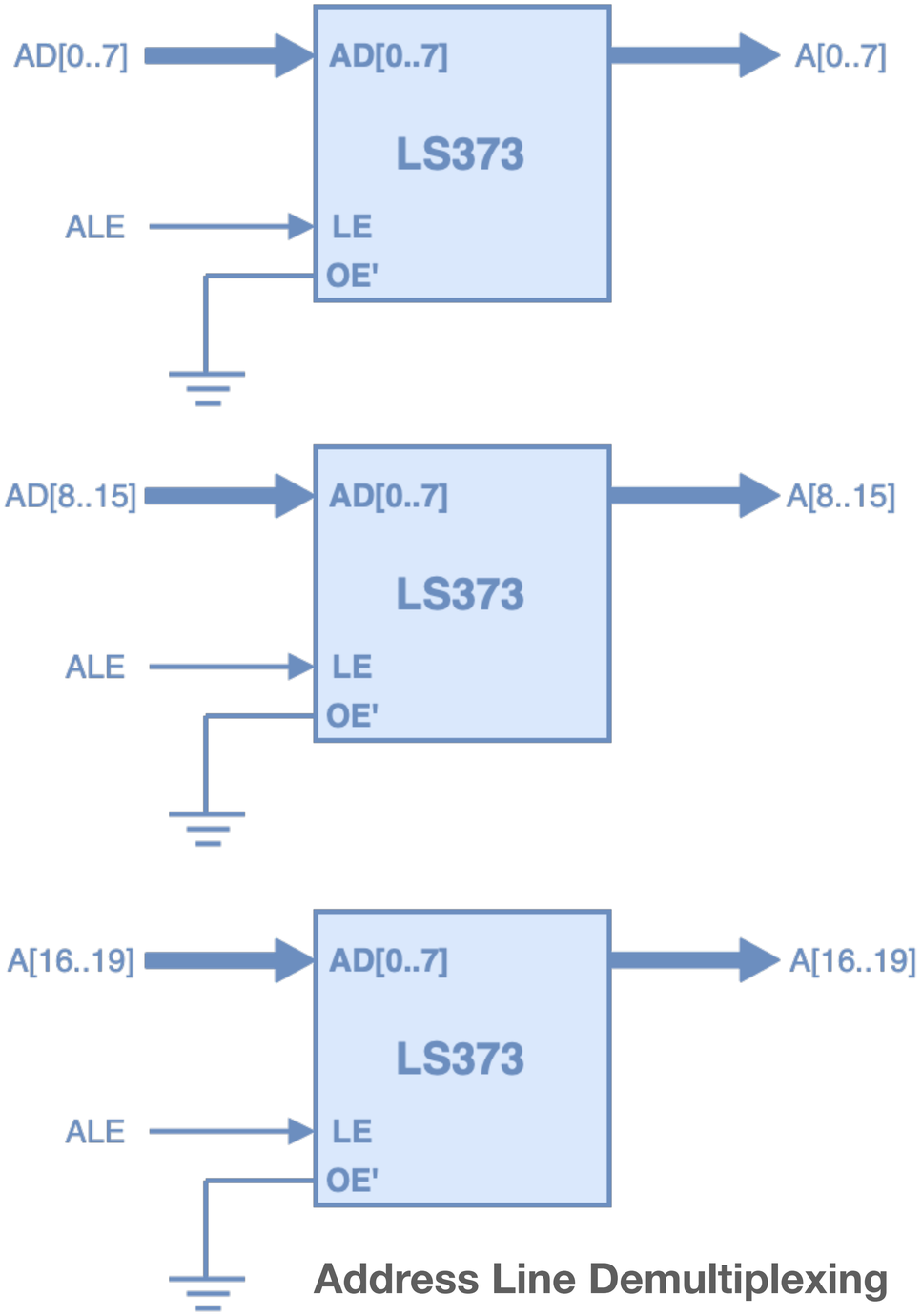
Signals Generated

- CLK at 5MHz
- PCLK at 2.5 MHz
- RESET
- READY

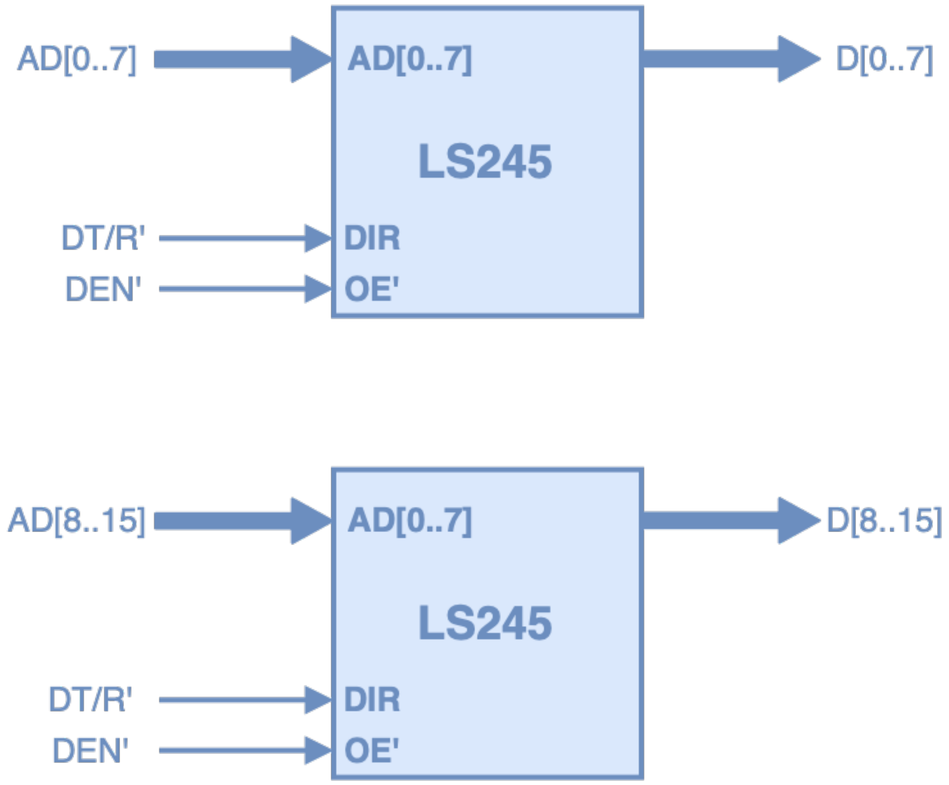

RESET (From 8284)
READY (From 8284)
INTA' (To 8259)
INT (From 8259)
NC
NC
+5V
CLK (From 8284)
RESET
READY
INTA'
INTR
HOLD
HLDA
TEST
NMI
Vcc
MN/MX'
CLK
8086
AD[0..15]
A[16..19]
ALE
BHE'
DT/R'
DEN'
RD'
WR'
M/IO'
GND
AD[0..15]
A[16..19]
ALE
BHE'
DT/R'
DEN'
RD'
WR'
M/IO'

Intel 8086

System Bus of 8086 (Address and Data)

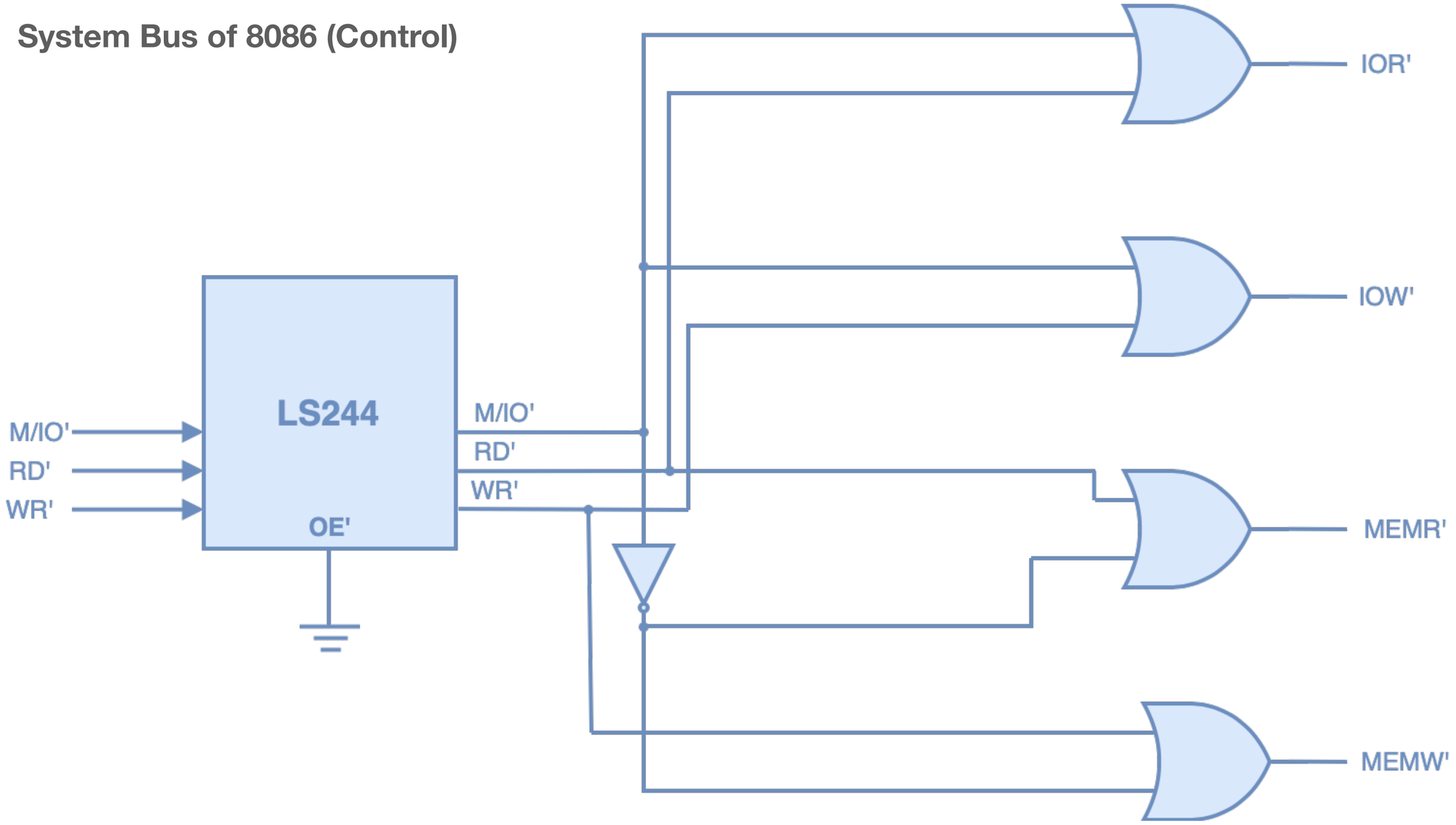


Address Line Demultiplexing

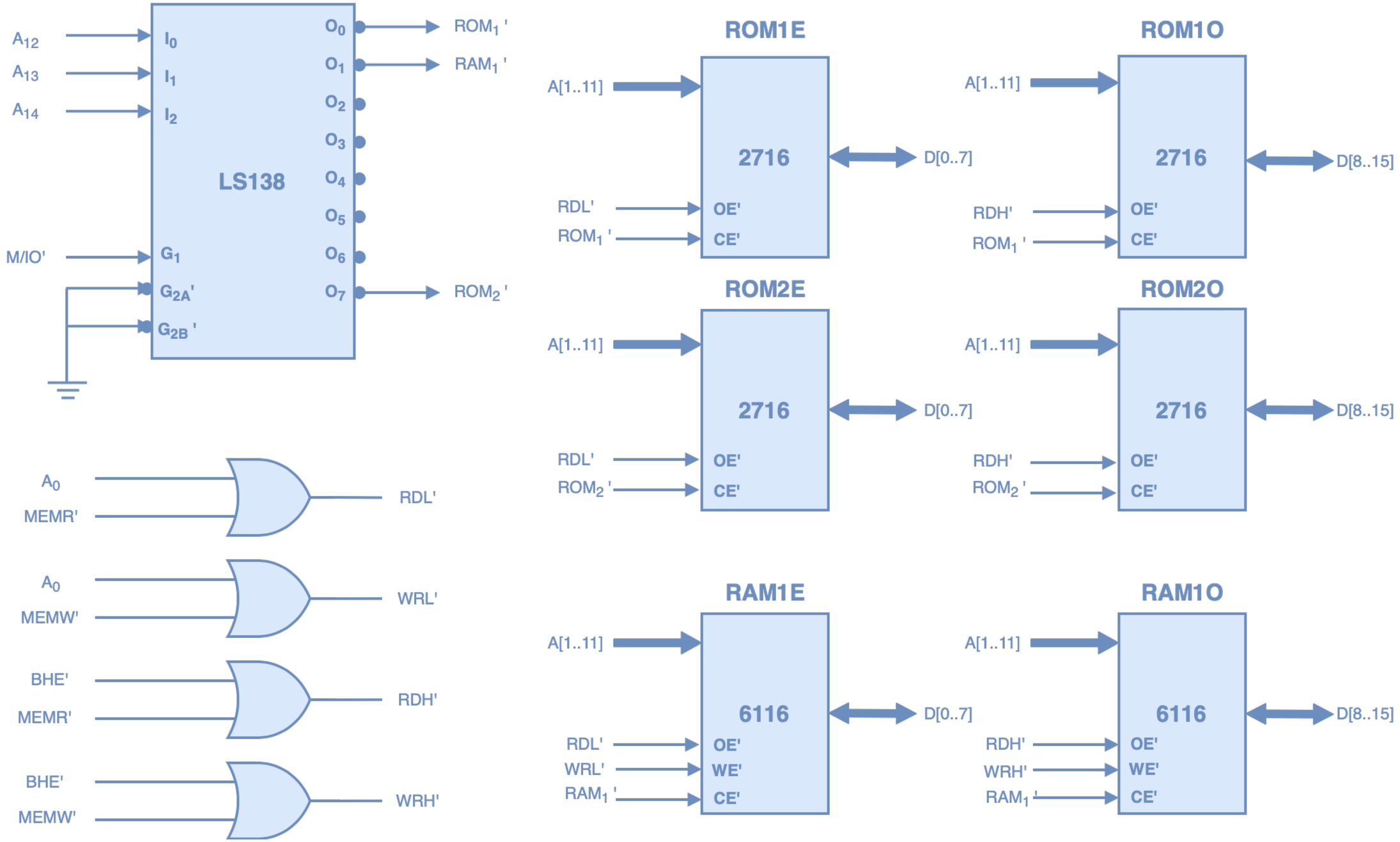


Data Line Demultiplexing

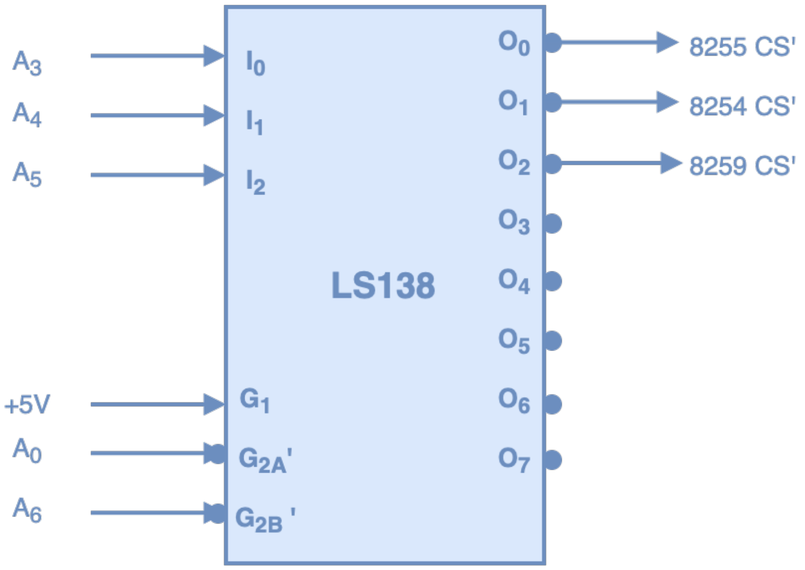
System Bus of 8086 (Control)

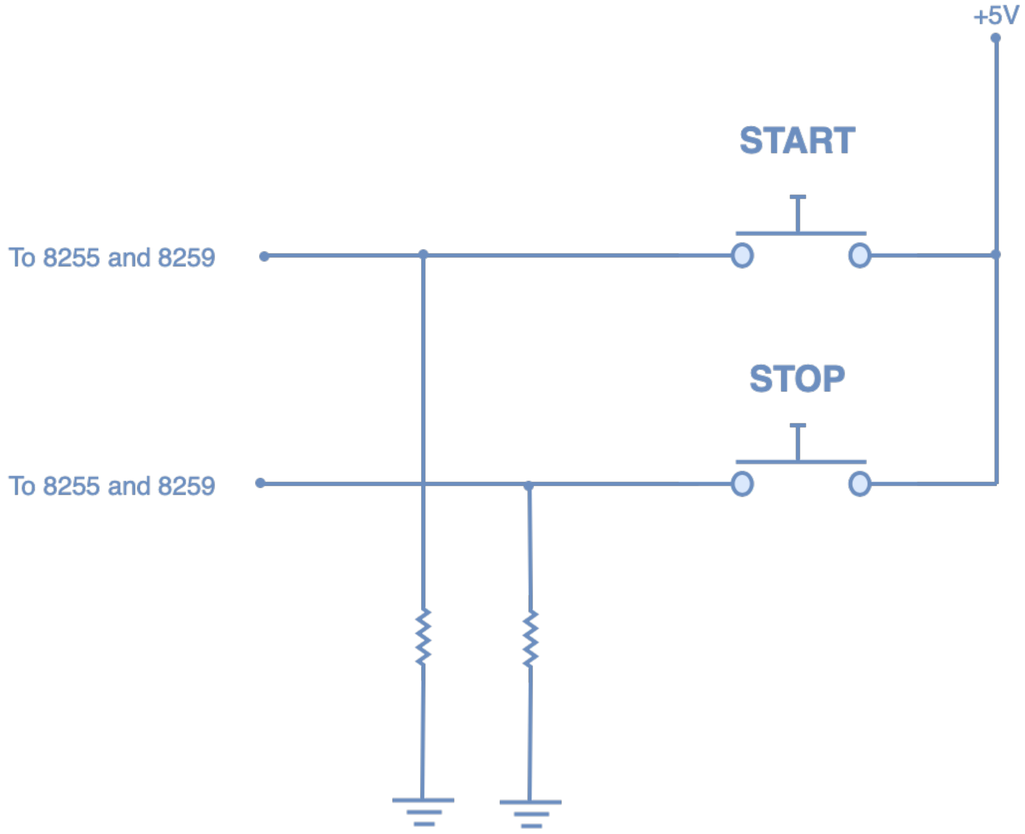


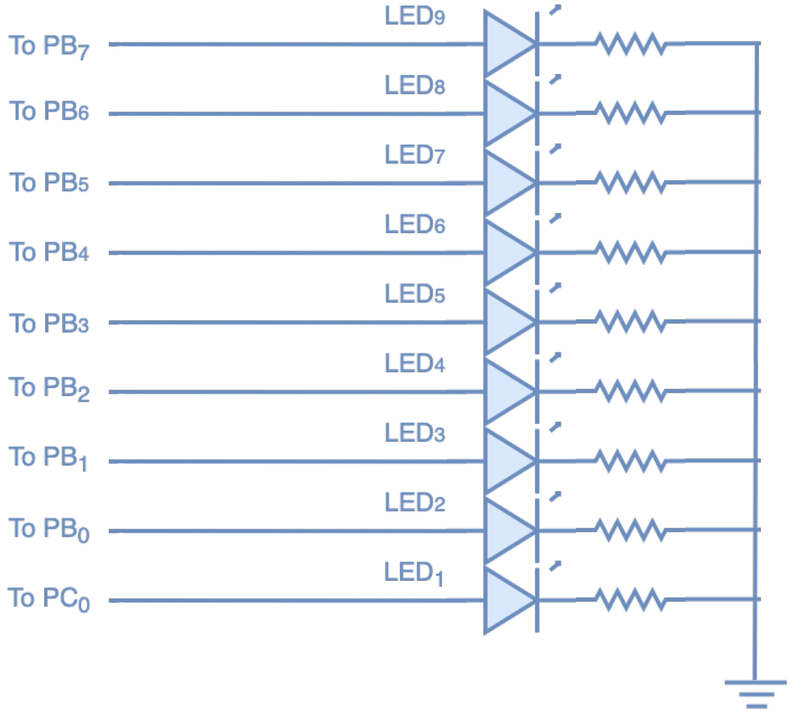
Control Signal Generation



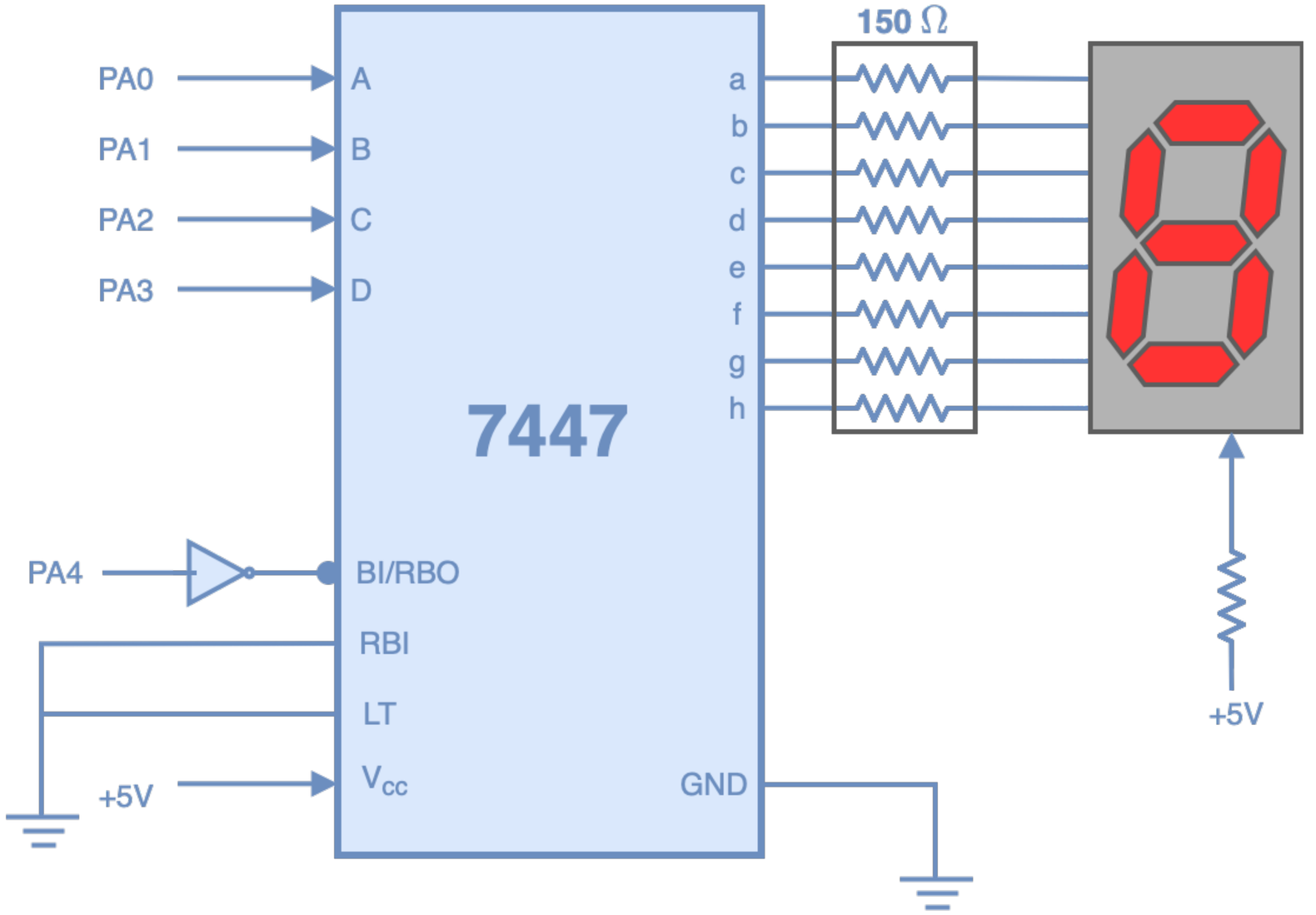
Memory Decoder and Memory Chip Connections



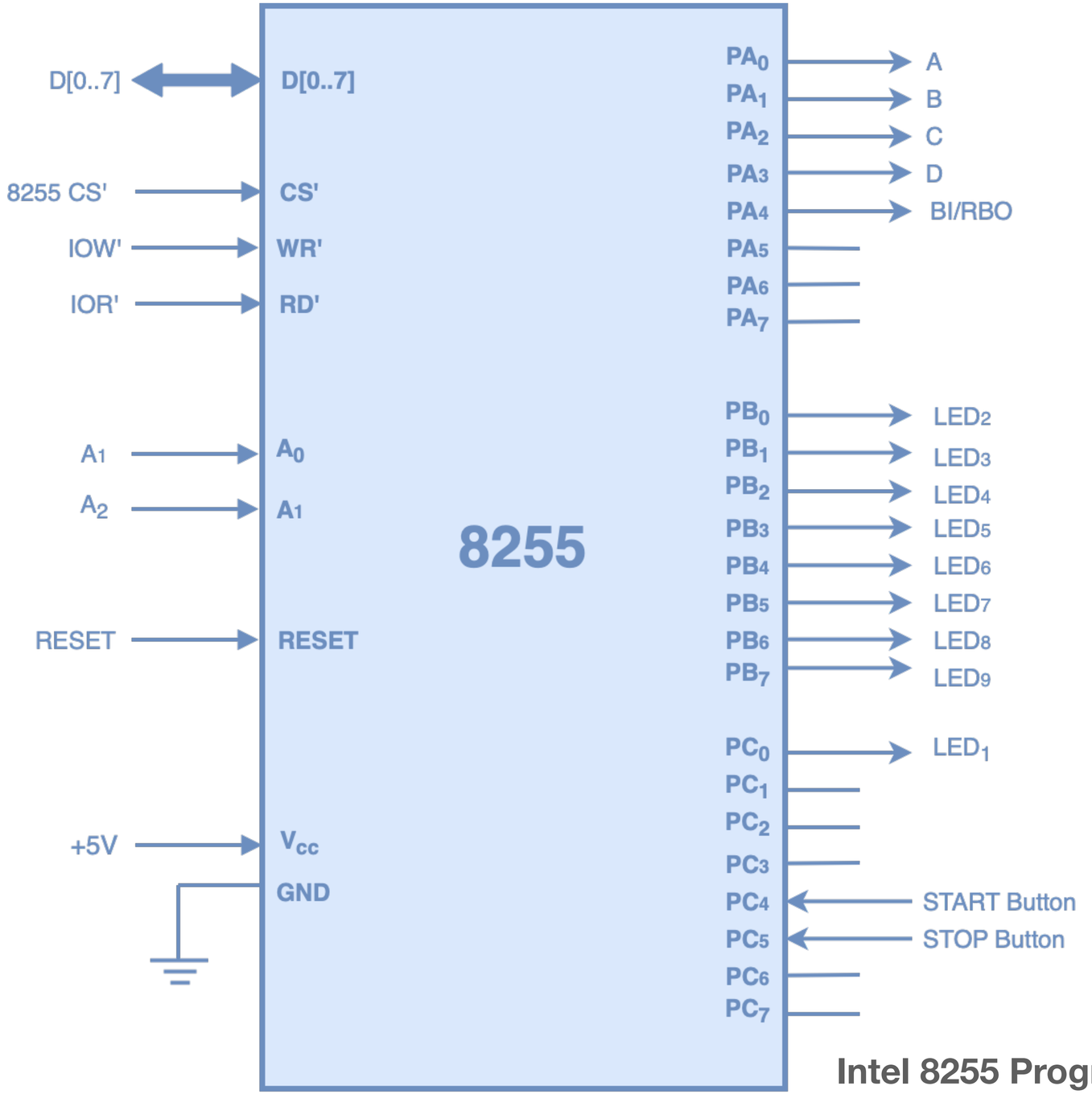




I/O Decoder and I/O Devices



BCD-to-seven-segment Decoder Connections

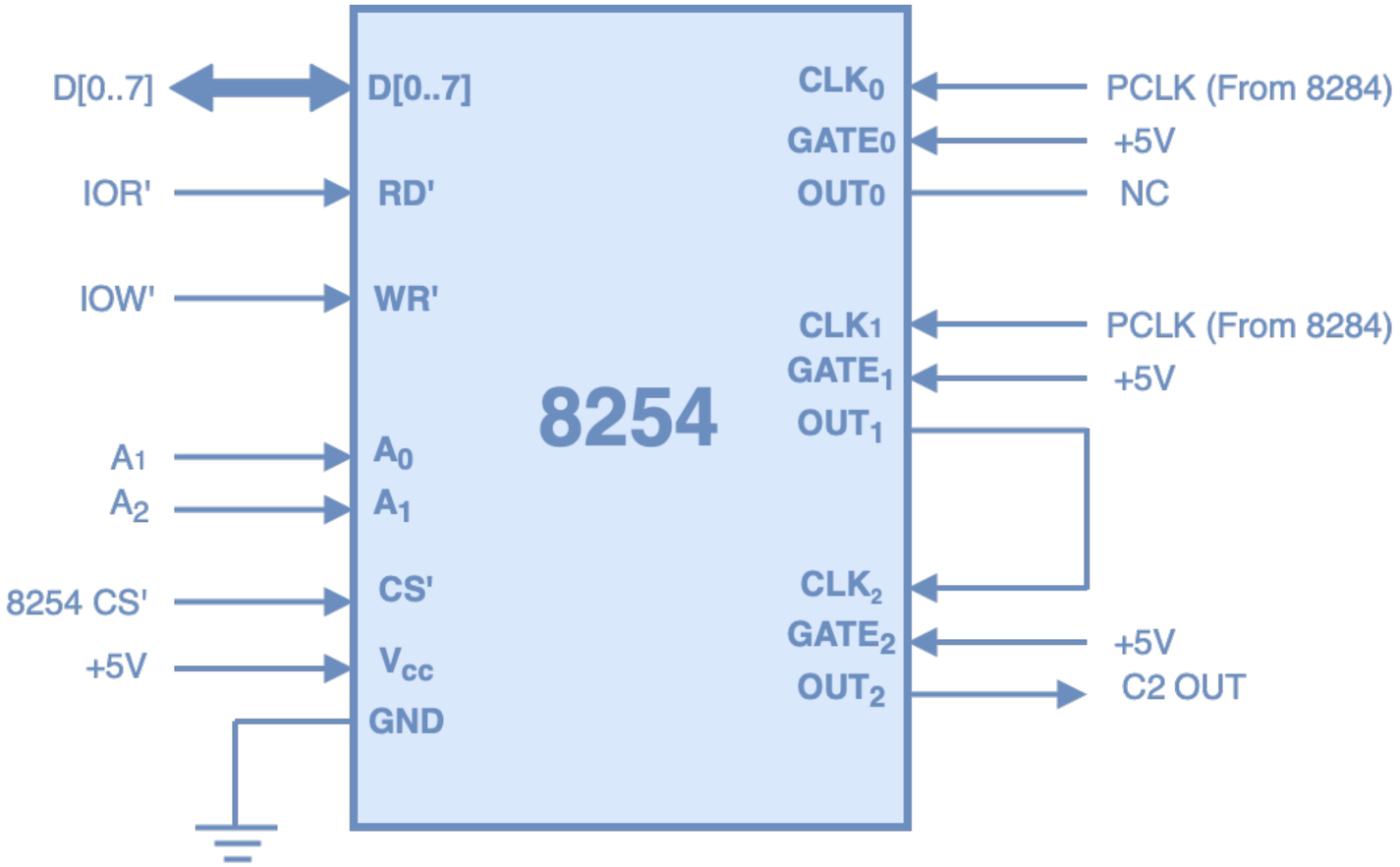


Addresses

- Port A: 00h
- Port B: 02h
- Port C: 04h
- Control Register: 06h

I/O Devices Connected

- Port A (Output)
  - PA_0 - PA_3: BCD inputs of IC 7447
  - PA_4: BI/RBO of IC 7447
- Port B (Output): LED_2 - LED_9
- Port C (Upper: Input, Lower: Output)
  - PC_0: LED_1
  - PC_4: START button
  - PC_5: STOP button



Intel 8254 Programmable Interval Timer

Addresses

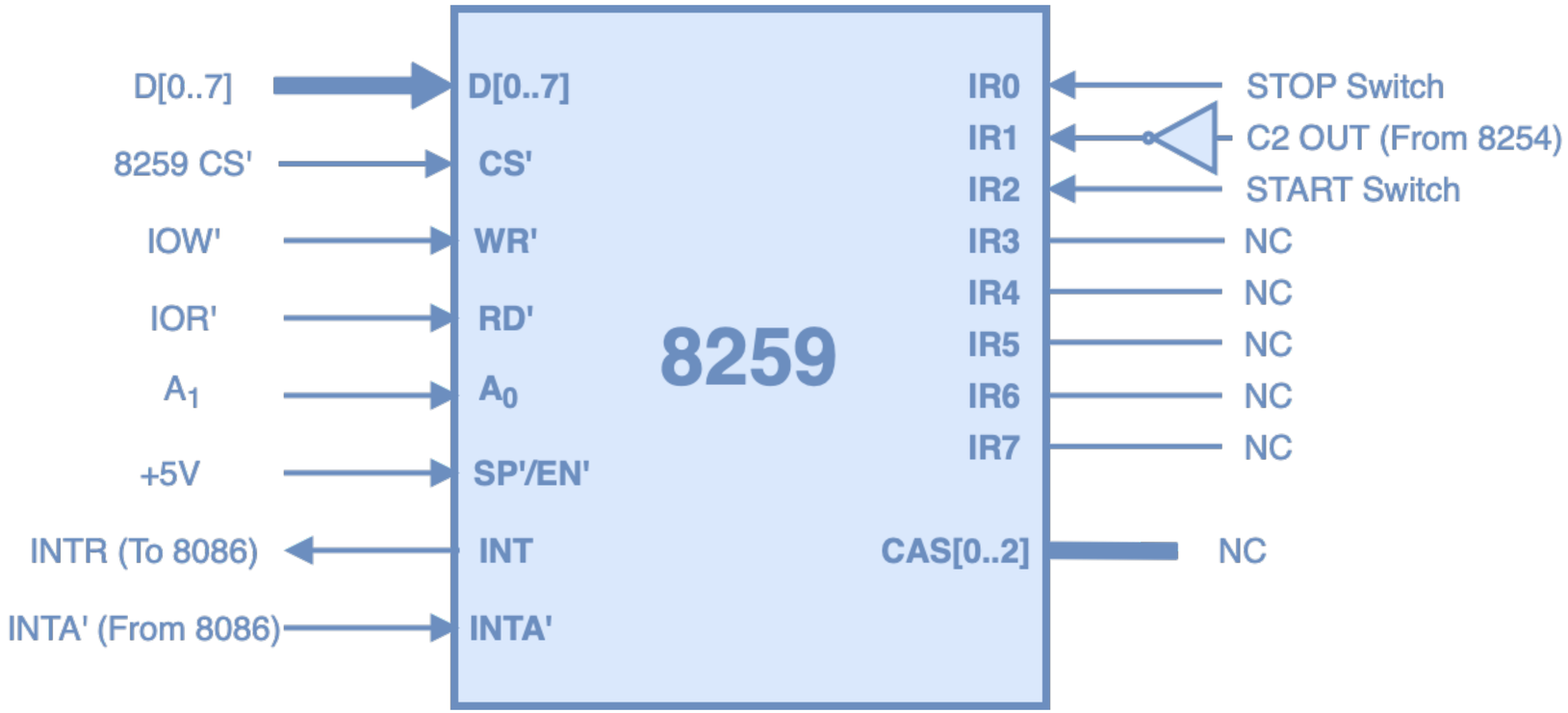
- Counter 0: 08h
- Counter 1: 0Ah
- Counter 2: 0Ch
- Control Register: 0Eh

Configuration

- Counter 0: Mode 2 (Value: 161d)
- Counter 1: Mode 2 (Value: 62500d)
- Counter 2: Mode 2
    1. Value: 159d + readout from C0 (Random delay)
    2. Value: 2d for 50ms interrupt

Outputs

- OUT_0 not used
- OUT_1 at 40 Hz
- OUT_2 at
    1. 0.25Hz - 0.125Hz (random delay)
    2. 20 Hz (for lighting every successive LED)



Intel 8259 Programmable Interrupt Controller

Inputs

- IR0: STOP Switch
- IR1: C2 OUT (OUT from counter 2)
- IR2: START Switch

Addresses

10h - 12h