

Analysis of Memristor Models and Implementation of Memristor based circuits

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by

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Declaration

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Abstract

RRAM has recently demonstrated outstanding characteristics such as high scalability, high speed, high density, and low energy operation. When using RRAM devices at the circuit level, a simple and accurate model is critical for rapid design and verification. The proper model selection provides insight into RRAM's behaviour as well as the efficient use of its unique properties. This work aims to assist circuit designers in selecting the best RRAM model for their applications. Here we have included simulations of some of the RRAM models. Also we have implemented some basic memristor-based circuits using one of these models.

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Chapter 1

Introduction

The existence of memristor as a device characterized by the relation between Charge q_t and flux linkage ϕ_t was discovered by Chua in [1]. This element is also being regarded as the fourth fundamental element linking flux linkages and charge. In 2008, the existence of the memristor was proved by the team at Hewlett Packard(HP). [1]

There were four circuit components for a long time: the resistor (1827), capacitor (1745), and inductor (1831). The equations governing the resistor, capacitor, and inductor are symmetric, therefore Dr. Chua proposed that a fourth passive device holding a relationship between magnetic flux and charge should exist. The connection between current and voltage is held by the resistor, the connection between current and flux is held by the inductor, and therefore the relationship between voltage and charge is held by the capacitor. Memristor is able to complete the circle. Dr. Chua demonstrated that none of the three passive components could match the memristor's capabilities, which an active circuit needed around 25 transistors to work similarly to the theoretical device. [1]

There are different RRAM models like Non-Linear Ion Drift Model [6], Simmons Tunnel Barrier Model [3], TEAM Model [4], VTEAM model [5]

RRAM devices can act as a memory element by storing the data as two or more resistance states. The RRAM devices have a HRS(high resistance state and a LRS(low resistance state)). Based on the voltage applied across the device or the current flowing through it, the RRAM device can shift from the LRA to HRS or vice versa. The resistance change is based on the formation and dissolution of a Conductive filament consisting of oxygen vacancies. When

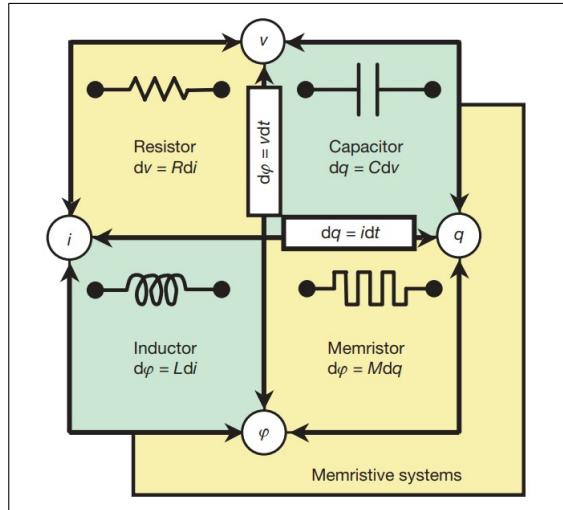


Figure 1.1: Fundamental two-terminal circuit elements [2]

a conductive filament is formed ,the device exhibits low resistance and when the filaments is broken ,it exhibits a high resistance state.

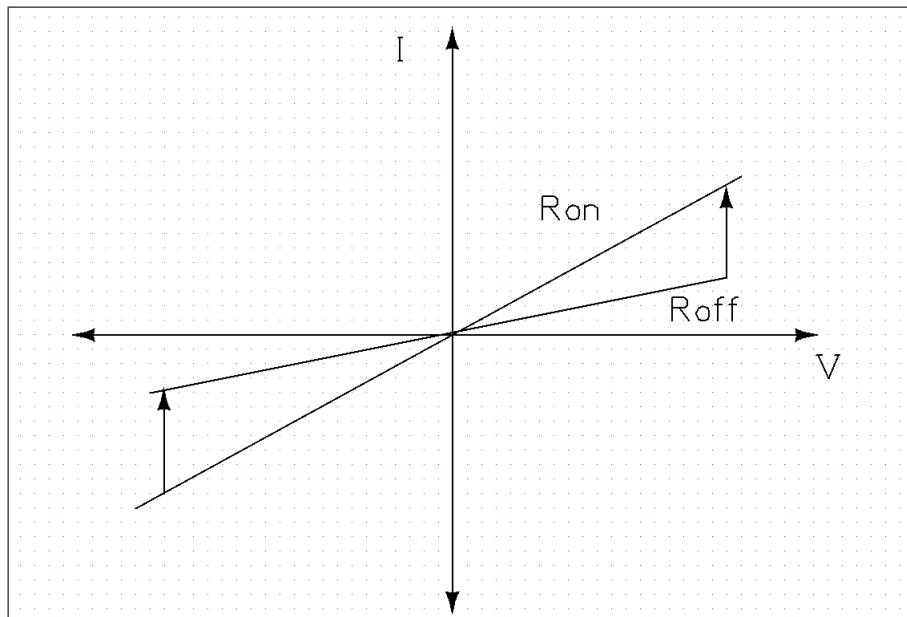


Figure 1.2: Ideal I-V characteristics of the memristor

Several other parameters, such as the maximum current during switching, are important at the design level (namely I_{off} and I_{on}).

R_{on} - Set resistance (typically low)

R_{off} -Reset resistance (typically high)

I_{on} - Maximum current during when changing states from HRS to LRS (set)

I_{off} - Maximum current during when changing states from LRS to HRS (reset)

$V_{set_{th}}$ - Set voltage threshold

$V_{reset_{th}}$ - Reset voltage threshold

Although RRAM-based devices have shown promising properties, there are still some challenges, the most significant of which is device variability (or reproducibility). As a result, the design and modelling communities are focusing more on the effect of variability on RRAM cell parameters.

Resistance change mechanisms are used in RRAM models to assess the effect of voltage,current and frequency changes on the cell parameters during set or reset operations. Researchers are working to make RRAM device emulators simple sothat they can be used to access the performance of memristive circuits at circuit level.

Chapter 2

Literature survey

RRAM has demonstrated outstanding characteristics such as high density as compared to CMOS technology and lower operating energy. A simple and error-free model is needed for an easier design and verification process using memristors. The paper [6], gives an analysis and validation of the reviewed RRAM models within the same simulation environment. Their research aims to help circuit designers choose the best RRAM model for their applications. Their work summarises the main characteristics as well as the flaws of each of the models mentioned. The authors also provide a Verilog-A code for the simulation of the memristor models.

Numerous physical experiments have shown that some physical memristors have a threshold voltage. Furthermore, as demonstrated in this paper, some physical memristors have a threshold voltage. Furthermore, as demonstrated in this paper, voltage-controlled memristors are required for some applications to function properly. The Voltage ThrEshold Adaptive Memristor (VTEAM) model is proposed in this paper [7] to describe the behaviour of voltage-controlled memristors. The previously proposed TEAM model, which describes current-controlled memristors, is extended by the VTEAM model. The VTEAM model is similar to the TEAM model in that it is simple, general, and flexible, and it can characterise various voltage-controlled memristors. A memristor model that exhibits a threshold voltage is required to accurately characterize physical behaviour and to apply to several memory and logic circuits. In this paper, the The VTEAM model, which has a threshold, is presented. voltage.

A memristor-based digital-to-analog converter (DAC) was proposed in this work [8] because a memristor has a low area, low power, and a lower threshold voltage when compared to CMOS circuits. Memristive circuits can also be used in in-memory computing applications. The proposed memristor DAC is based on the basic DAC cell, which is made up of two memristors connected in opposite directions. This basic DAC cell was used to build and simulate both a 4-bit and an 8-bit DAC. A sneak path problem was also depicted, and a solution was provided. The paper's proposed design aimed to reduce the area of traditional DAC's by implementing a memristor-based DAC that takes up to 40 percent lesser space.

Chapter 3

Memristor Spice modelling

In this chapter, a survey of many different memristor modelling techniques is given. The memristor models used for this chapter's discussion were chosen to demonstrate a wide range of various modelling methodologies while reducing redundancy. Some models try to recreate the functionality of a wider range of devices in a more generalised way, while other models have been developed to represent a specific device very closely.

In this chapter, the model's output I-V characteristics and how well they mimic the I-V properties of practical devices are discussed. Either sinusoidal or triangular pulses serve as the voltage inputs under investigation. To examine how each model transitions to intermediate levels between the maximum and least resistance, sinusoidal input pulses are applied at different amplitudes and frequencies. The subcircuit code is provided for each model, and the SPICE simulations were carried out in Spice-based simulator. This made it possible to compare the benefits and drawbacks of numerous different memristor models on an individual basis.

3.1 Linear Ion Drift Model (using Verilog-A code)

This was the first physical model of a memristor in HP Labs, created by R.S.Williams [1].

While one area is undoped, the other is doped (usually with positive oxygen ions, TiO₂), has low resistance, and is hence more conductive. Memristors are believed to have a uniform field, ohmic conductance, and average ion mobility. Thus, the equation for the state variable is as follows: [6]

$$\begin{aligned} \frac{dw}{dt} &= \frac{\mu_{v \cdot R_{ON}}}{D} i(t) \\ v(t) &= \left(R_{ON} \frac{w(t)}{D} + R_{OFF} \left(1 - \frac{w(t)}{D} \right) \right) \cdot i(t) \end{aligned} \quad (3.1)$$

Table 3.1: Model Parameters used for the simulation (Linear ion drift model) [6]

R_{on}	100 Ω	D	10 nm
R_{off}	2e5 Ω	$V_{threshold}$	0 V
u_v	$10 * 10^{-14} m^2 / V.s$	p_{coeff}	2

R_{off} is the off-state device resistance and R_{on} is the on-state at $w(d)=0$ device resistance at $w(t)=d$. In this instance, the state variable $w(t)$ is constrained to the boundaries of the intervals $[0, D]$.

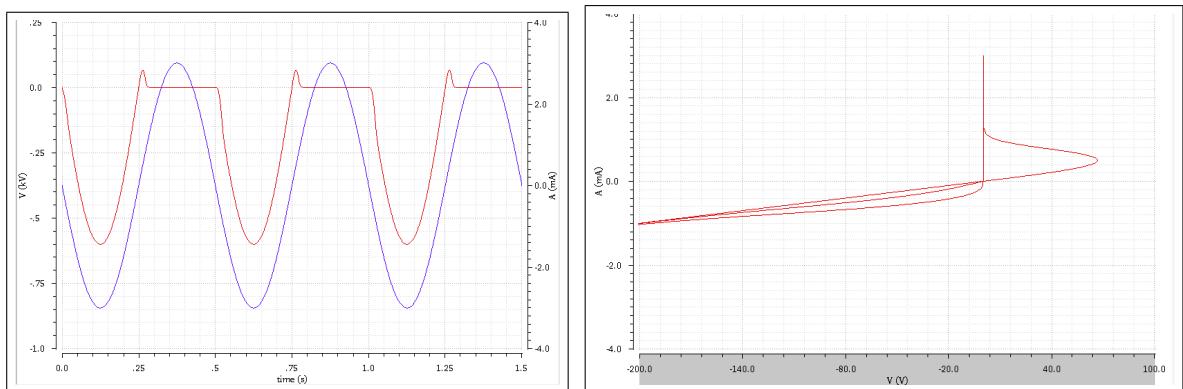


Figure 3.1: Simulation results for Linear Ion Drift Model

3.2 Linear Ion Drift Model (LTSpice Model)

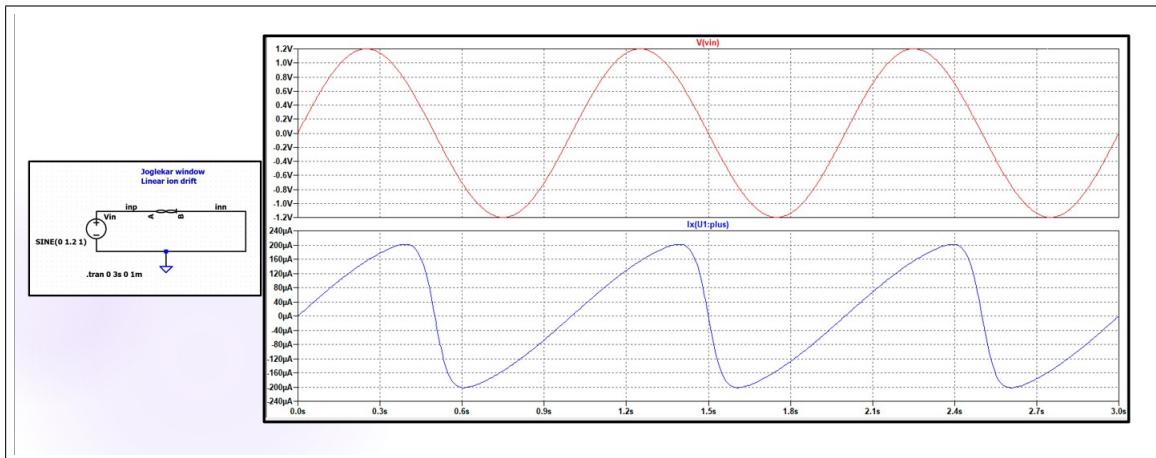


Figure 3.2: Transient Simulation results for Linear Ion Drift Model , Amplitude=1 V , Frequency =1 Hz , p=2

```
.SUBCKT memristor plus minus PARAMS:
+ Ron=100 Roff=16K Rinit=11K D=10N uv=10F p=2s
Gx 0 x value={I(Emem)*uv*Ron/D**2*f(V(x),p)}
Cx x 0 1 IC={(Roff-Rinit)/(Roff-Ron)}
Raux x 0 1000000
Emem plus aux value={-I(Emem)*V(x)*(Roff-Ron)}
Roff aux minus {Roff}
Eflux flux 0 value={SDT(V(plus,minus)) }
Echarge charge 0 value={SDT(I(Emem)) }
.func f(x,p)={1-(2*x-1)**(2*p)}
.ENDS memristor
```

Figure 3.3: Ngspice code for Linear ion drift model with joglekar window function

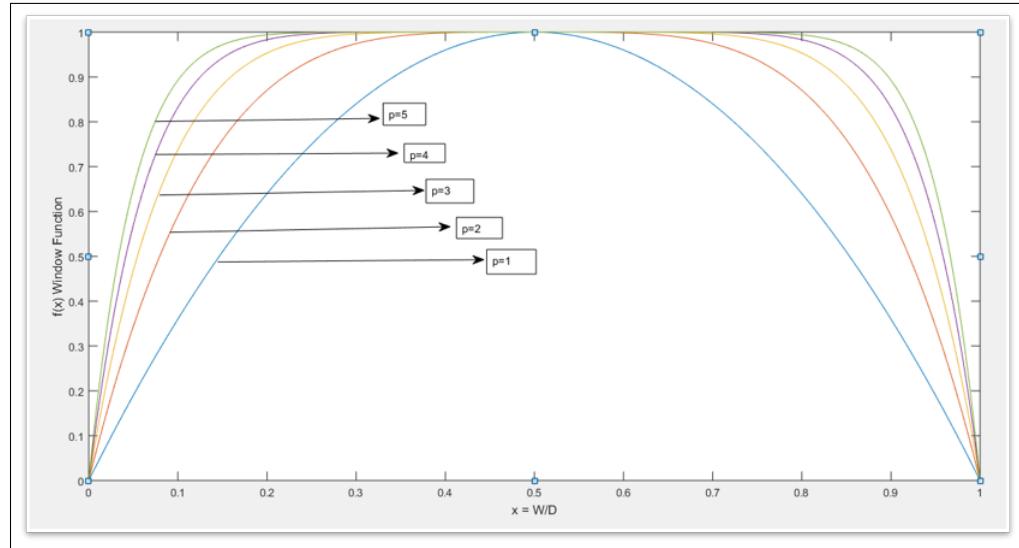


Figure 3.4: Joglekar window function for different "p" values

The Joglekar function is given as: [9]

$$f(x, p) = 1 - (2 \times x - 1)^{2 \times p}$$

Effect of variation of p coefficient

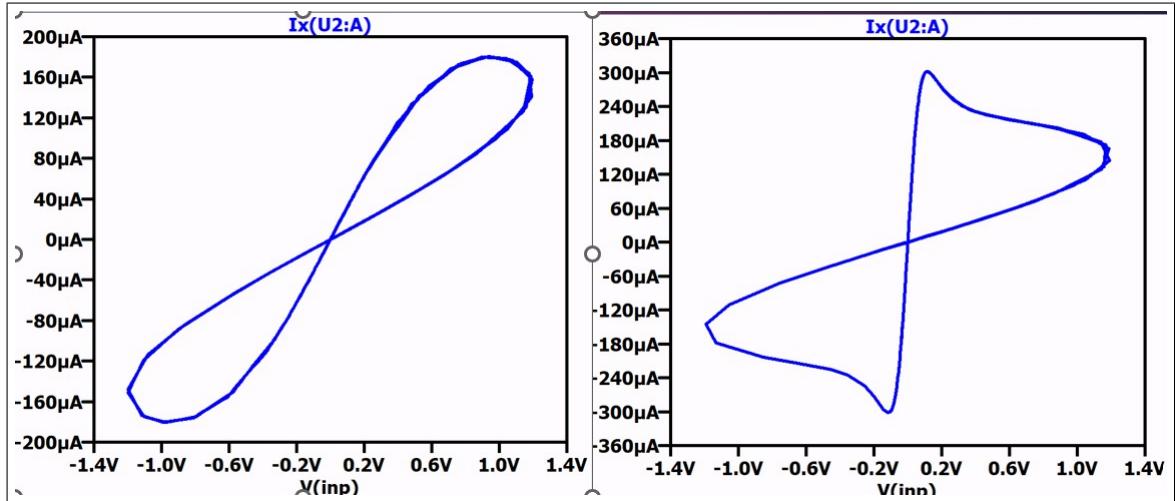


Figure 3.5: Effect of p coefficient in joglekar function (a) $A=1.2$ V $f=1$ Hz $p=1$, (b) $A=1.2$ V $f=1$ Hz $p=10$

Fig. 3.5 shows the effect of the "p" in the Joglekar window function on the I-V characteristics of the memristor. As the value of p in the Joglekar function increases, the I-V characteristics become more and more ideal as the slope becomes constant, the curvature decreases, and the change in resistance is less.

Effect of variation of Amplitude

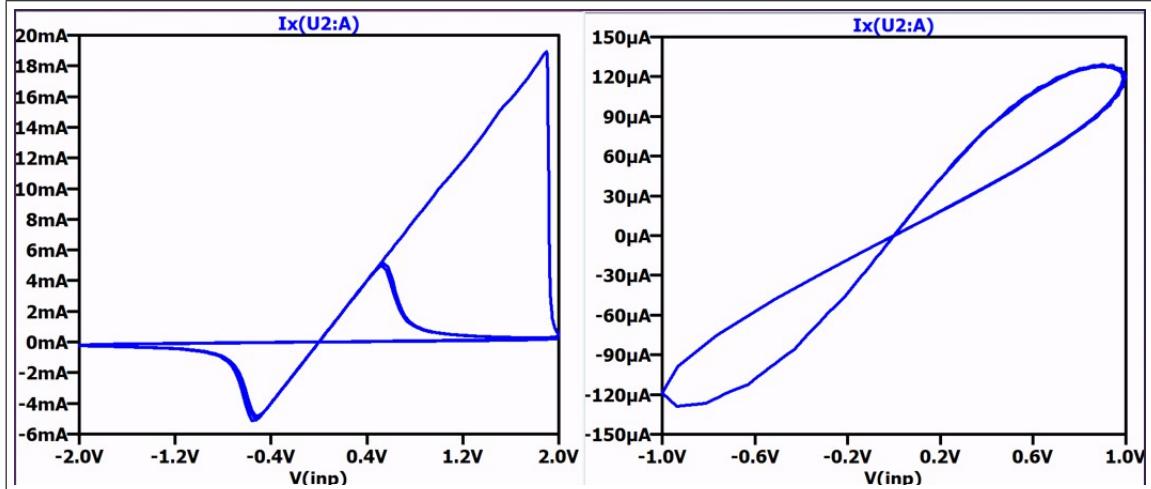


Figure 3.6: Effect of Amplitude (a) $A=2$ V $f=1$ Hz $p=2$, (b) $A=1$ V $f=1$ Hz $p=2$

As seen in figure 3.6, as the amplitude of the voltage across the memristor increases, the I-V characteristics deviates from the ideal characteristics as the curve becomes narrower. Also the memristor current decreases as the voltage across memristor increases.

Effect of variation of frequency

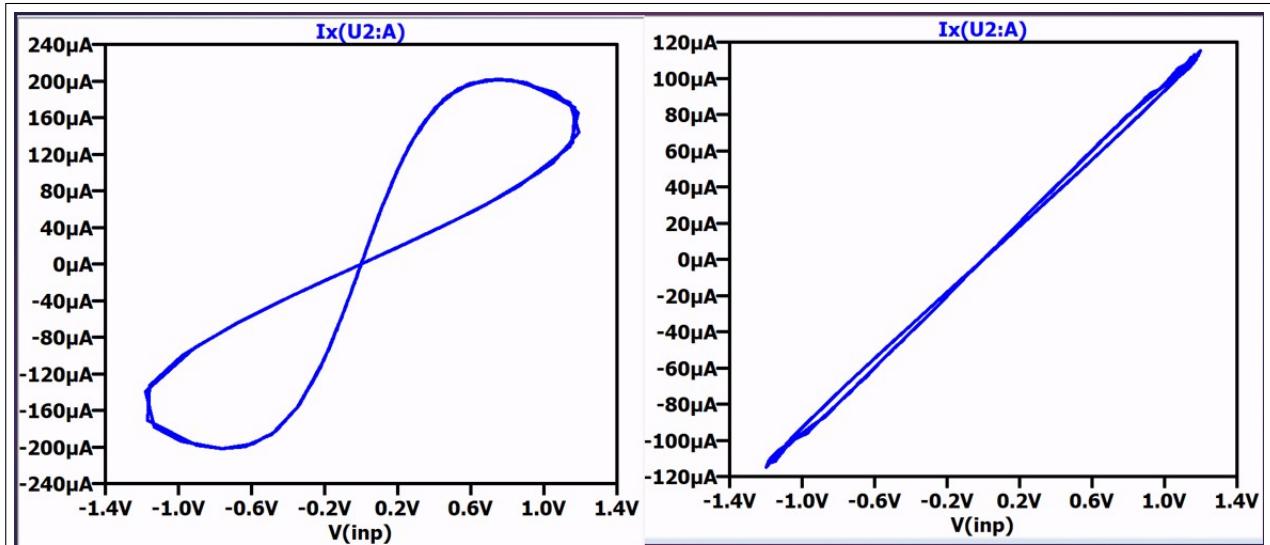


Figure 3.7: Effect of frequency (a) $A=1.2$ V $f=1$ Hz $p=2$, (b) $A=1.2$ V $f=5$ Hz $p=2$

As the frequency of the input voltage increases, it is seen that the I-V characteristic curve becomes narrower. With an increase in input frequency, the I-V characteristics deviate from the ideal memristor. Also, it is seen that the current also reduces when the input voltage frequency increases.

3.3 Non-Linear Ion Drift Model

Even though the linear ion drift model is straightforward and satisfies the fundamental memristor equations, it assumes a linear relation between the memristor current and voltage. In this model the memristor current assumes a non-linear dependence on the input voltage.

A manufactured memristor device exhibits unusual behaviour and exhibits high levels of non-linearity. This results in the creation of the non linear ion drift model of memristors, another memristor model. For this model, the current voltage relationship is written as; [10]

$$i(t) = w(t)^n \beta \sinh(\alpha v(t)) + \chi[\exp(\gamma v(t)) - 1] \quad (3.2)$$

The fitting parameters in equation (5) are denoted by the letters,, and; the parameters n specify the form of the w state variable over the currents. The state variables have a standard deviation of [0, 1]. The state variable differential equation is: [10]

$$\frac{dw}{dt} = a \cdot f(w) \cdot v(t)^m \quad (3.3)$$

Where m is an odd integer, f(w) is a window function, and an is a constant. The device's non-linearity is voltage-dependent. Logic gates are where this memristor model is most commonly used.

Table 3.2: Model Parameters used for the simulation (Non-Linear ion drift model) [3]

p_{coeff}	1	init	0.5
alpha	2	beta	9
C	0.01	g	4
n	13	q	13
a	3	model	3

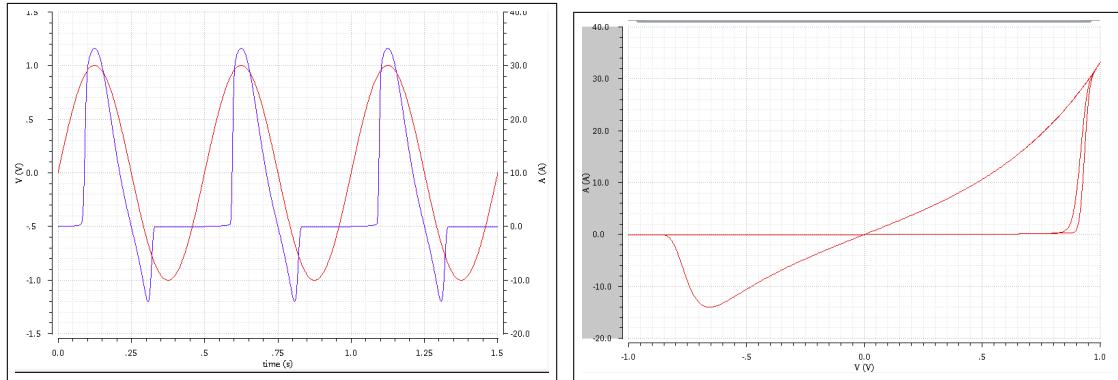


Figure 3.8: Simulation results for Non-Linear Ion Drift Model

3.4 VTEAM Model

Here, we will be using the VTEAM model of the memristor to test the characteristics of the device. Figure “n” shows the setup to test the memristor characteristics. The parameters of the VTEAM model used here are $R_{on}=50$, $R_{off}=1000$, $V_{on}=-0.2$ V, $V_{off}=0.02$ V. The time step dt is set at 10^{-14} for simulation. The input provided is a sine wave of frequency 1 MHz and Amplitude of 1 V is been used to simulate the Verilog-A model of VTEAM form acquired from [3].

Table 3.3: Model Parameters used for the simulation (VTEAM model) [7]

R_{on}	1000Ω	a_{on}	$2*10^{-9}m$
R_{off}	50Ω	a_{off}	$1.2*10^{-9}m$
v_{on}	-0.2 V	k_{on}	-10
v_{off}	0.02 V	k_{off}	$5*10^{-5}$
α_{on}	3	x_{on}	0 m
α_{off}	1	x_{off}	$3*10^{-9}m$

The mathematical model of the VTEAM model is expressed as follows [6]:

$$v(t) = \left[R_{on} \times \frac{W(t)}{D} + R_{off} \times \left(1 - \frac{W(t)}{D}\right) \right] \times i(t)$$

$$\frac{dw(t)}{dt} = \begin{cases} k_{off} \left(\frac{v(t)}{V_{off}} - 1\right)^{\alpha_{off}} f_{off}(w), & 0 < V_{off} < v \\ 0, & V_{on} < v < V_{off} \\ k_{on} \left(\frac{v(t)}{V_{on}} - 1\right)^{\alpha_{on}} f_{on}(w), & v < V_{on} < 0 \end{cases} \quad (3.4)$$

$V(t)$ is the voltage applied across memristor

$i(t)$ is the current through the memristor.

α_{off} , α_{on} , k_{off} , k_{on} are fitting parameters.

V_{on} and V_{off} are the threshold voltages.

f_{on} and f_{off} are window functions used to limit w to have a value between 0 and 1. [5]

$V(t)$ can be expressed as time varying resistance $R_m(t)$ as : [5]

$$V(t) = R_m(t) * i(t)$$

$$R_m(t) = R_{on} * \frac{W(t)}{D} + R_{off} * \left(1 - \frac{W(t)}{D}\right)$$

R_{on} is the Set resistance (typically low)

R_{off} is the Reset resistance (typically high)

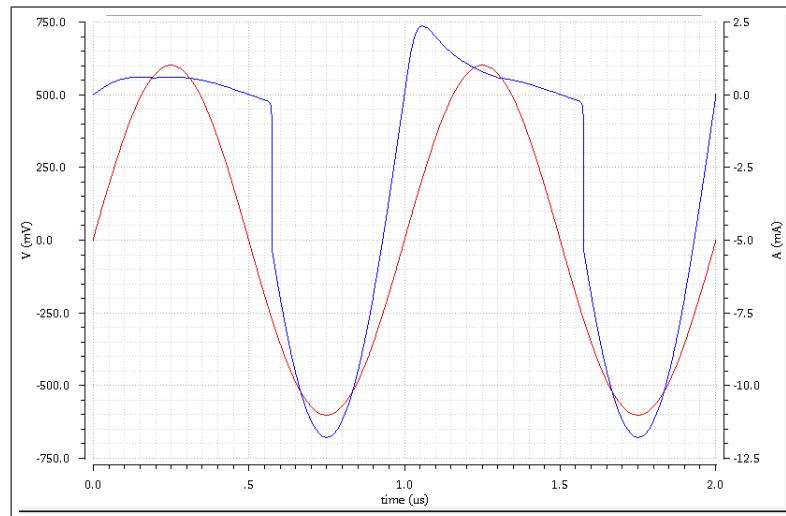


Figure 3.9: V and I graphs for the VTEAM model (Red- voltage,Blue-Current)

From the I-v graphs we can see that the current change is lesser when the applied voltage is positive as the memristor offer high resistance while the current change increases when the applied voltage is negative as the memristor offers lower resistance.

Also the current doesn't change much till the +ve voltage applied crosses a the threshold V_{th1} .

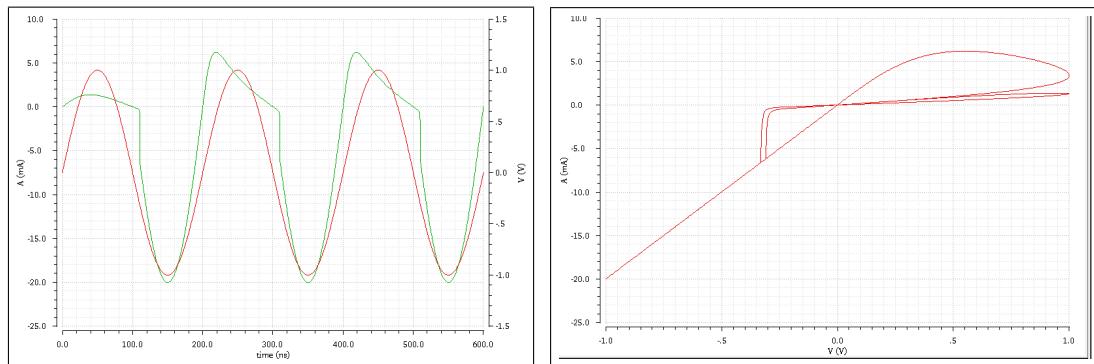


Figure 3.10: Simulation results for VTEAM Model

3.5 Simmons tunnel barrier model

A more accurate physical model of the memristor was suggested by Pickett in [3]. It depicts the memristor as an electron tunnel barrier connected in series with a resistor, as seen in Figure 3.14. It is also expected that the memristor switches asymmetrically and non linearly. The state variable is the Simmons tunnel barrier width. x is the breadth of the oxide region. As a result, the state variable derivative can be used to determine the oxygen vacancy drift velocity.

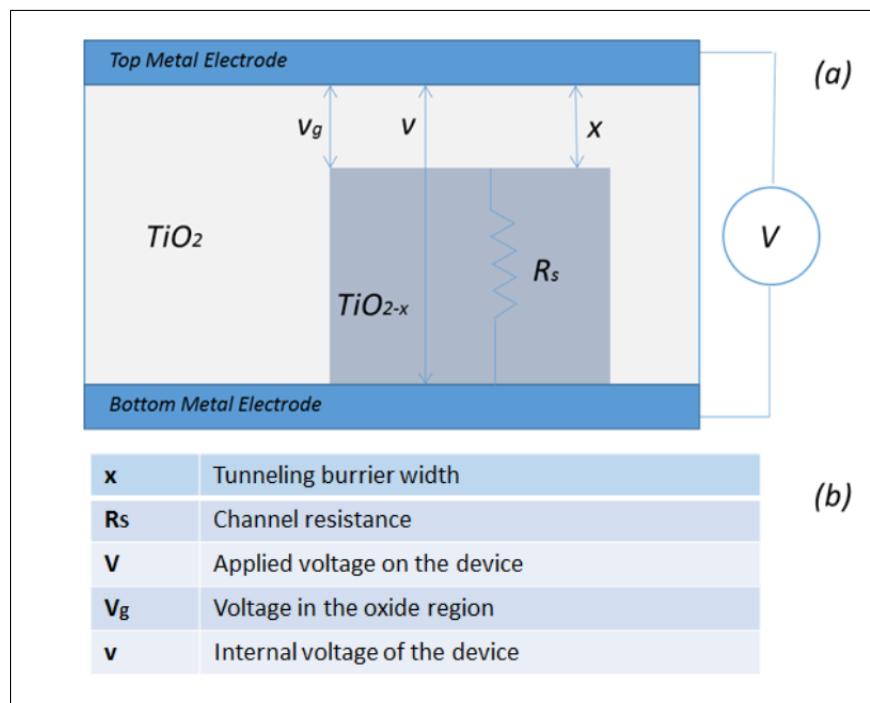


Figure 3.11: Simmons Tunnel barrier model

[6]

Table 3.4: Model Parameters used for the simulation (Simmons tunnel barrier model) [6]

R_{on}	1000Ω	a_{on}	$2*10^{-9} m$
R_{off}	50Ω	a_{off}	$1.2*10^{-9} m$
i_{on}	$8.9e-06 A$	i_{off}	$115e-06 A$
c_{on}	$40e-06 m/s$	c_{off}	$3.5e-06 m/s$
b	$500e-06 A$	x_c	$107e-11 m$

For this model ,we use the same test setup as figure 3.1. where the input current is 3 mA (p-p) and has frequency of 2 MHz.

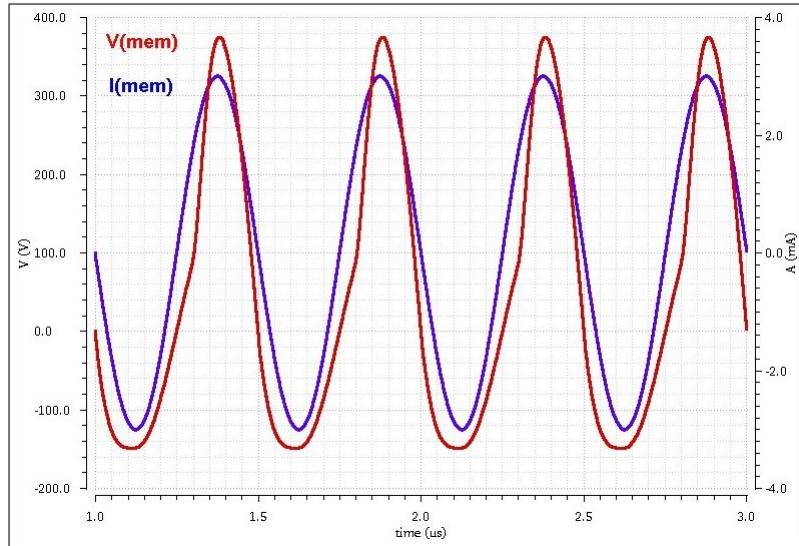


Figure 3.12: Simmons Tunnel barrier model current (blue) and voltage (red) graphs

The simmons tunnel model assumes an exponential dependence of current on the state variable.So, the voltage change is lesser for a positive current and is more for a negative current.

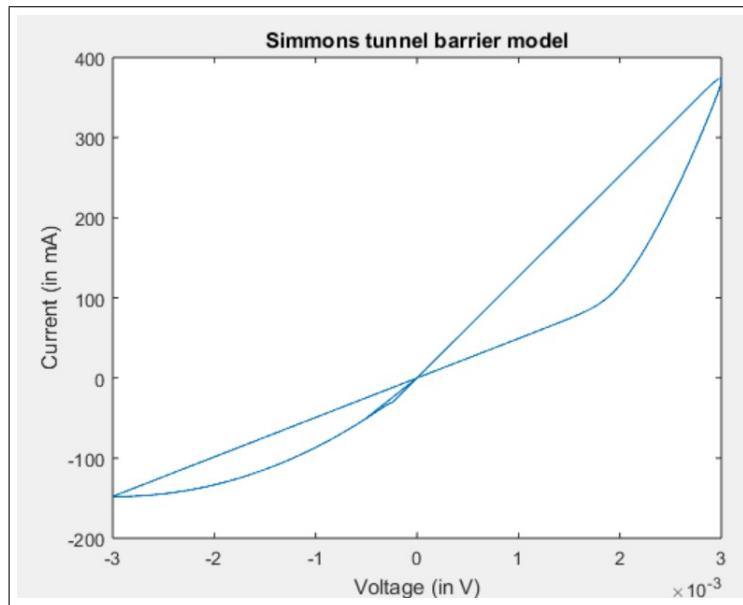


Figure 3.13: Simmons Tunnel barrier model I-V Characteristics

Chapter 4

Memristor -based circuits

The number of transistors on a chip has been steadily increasing over the past decades. However, there are signs that Moore's law, which states that the number of transistors on a chip roughly doubles every two years, is slowing. In order to catch up with the Moore's law ,research suggests using components having smaller footprint than the MOSFET. With the introduction of memristors, research into memristors and their applications has become a hot topic. Among these, memristor-based logic circuits have gotten a lot of attention. One of the major reasons for this is that the memristor based circuits have comparatively less area than the traditional CMOS circuits.

Also one of the other application of the memristive circuits is in the In-memory compute which does not follow the traditional Von-neumann architecture. The technique of running computer calculations entirely in computer memory is known as in-memory computation (or in-memory computing). These circuits aim to manage basic ALU operations in the memory itself instead of juggling between memory and ALU unit.These will save clock cycles and time and hence effectively increase the speed of the RAM(Random access memory) .

This chapter implements some basic circuits using the VTEAM Memristor model.

4.1 DAC metrics and terminologies

4.1.1 Input dynamic range

Input dynamic range is defines the ratio of the largest to smallest possible signal value that can be resolved by the ADC.

For a n-bit ADC,

$$DR = 20 * \log(2^n - 1)db$$

4.1.2 DNL (Differential non-linearity)

Digital-to-analog (DAC) and analog-to-digital (ADC) converters frequently use the performance indicator known as differential non-linearity (abbreviated DNL). It's a phrase used to describe the difference between two analogue values that match to neighbouring digital input values. This specification is crucial for assessing inaccuracy in a digital-to-analog converter (DAC); it mostly determines how accurate a DAC will be. Any two consecutive digital codes should, in theory, translate into output analogue voltages that are separated by exactly one Least Significant Bit (LSB). A measurement of the worst-case departure from the ideal 1 LSB step is differential non-linearity. For instance, a DAC that shows 12 LSB differential non-linearity has an output change of 1.5 LSB for a change in digital code of 1 LSB. In bits or fractions, differential nonlinearity can be stated..

Differential non-linearity is defined as the difference between the step size with respect to the standard step size.

$$DNL = \left| \frac{V_{out}(i+1) - V_{out}(i)}{Step} - 1 \right|$$

Step - Step width of the ADC.

- Missing codes, or codes for which there is no input voltage to obtain the at the ADC output, appear in the transfer function if the DNL of an ADC is less than -1.
- A DAC's transfer function becomes non-monotonic if the DNL of the DAC exceeds 1. In closed-loop control applications, a non-monotonic DAC is especially undesirable since it may result in stability issues, i.e. oscillations.

4.1.3 INL (Integral non-linearity)

A typical performance metric in digital-to-analog (DAC) and analog-to-digital (ADC) converters is integral nonlinearity, abbreviated as INL. It is a measurement of the difference between the actual measured output value for a specific input code and the desired output value in DACs. It is the difference between the actual threshold level of an output code and the desired input threshold value in ADCs. After offset and gain errors have been eliminated, this measurement is done. [1]

The ideal transfer function for a DAC or ADC is a straight line. The ideal line that is chosen determines the INL measurement. A common option is the line joining the endpoints of the transfer function or the line connecting the smallest and largest. Utilizing a best fit line as an alternative involves minimising the average (or alternatively, the mean squared) INL.

Integral non-linearity measures the maximum deviation of the ADC characteristics from the best-fit line. For a best straight line approach INL is given by:

$$INL = |V_{o_{ideal}} - V_{o_{real}}|$$

Vo - Output voltage of the ADC

4.2 Memristor Ratioed logic

Many different logic have been defined to construct digital and analog circuits using the memristor. Some of the major types are MAGIC (memristor aided logic), Hybrid memristor logic, Imply logic, etc.

In this section we will briefly discuss the Memristor ratioed logic also known as MAGIC.

In many ways, solely memristor elements are employed to create logic gate circuits, whereas in other approaches, hybrid memristor elements and CMOS structures are used . fundamental logic gates such as AND gate and Or gate can be implemented with the memristor ratioed logic.

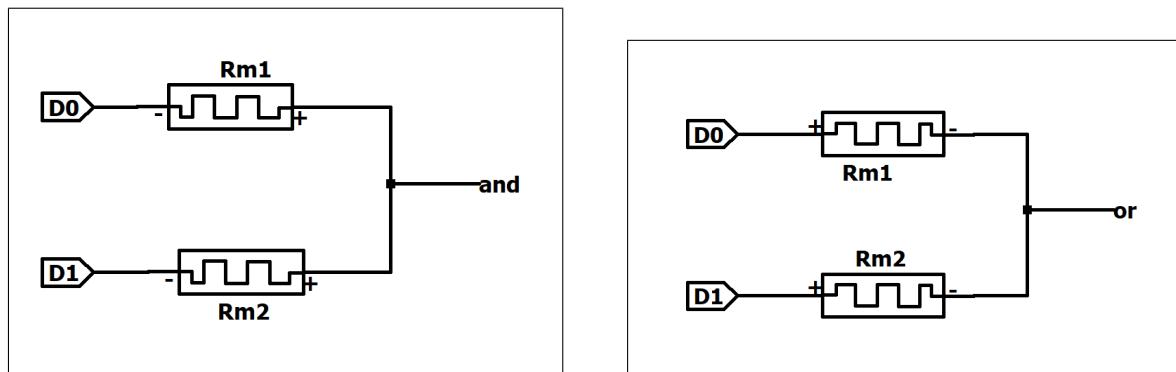


Figure 4.1: (a) AND gate schematic (b) OR gate schematic

D0	D1	Rm2	Rm1	output
1	1	R_{off}	R_{off}	high
1	0	R_{on}	R_{off}	low
0	1	R_{off}	R_{on}	low
0	0	R_{off}	R_{off}	low

Table 4.1: Different states for AND gate

D0	D1	Rm2	Rm1	output
1	1	R_{off}	R_{off}	high
1	0	R_{on}	R_{off}	high
0	1	R_{off}	R_{on}	high
0	0	R_{off}	R_{off}	low

Table 4.2: Different states for OR gate

Two memristors paired with the proper polarities have been used to create AND and OR gates . In order to fully comprehend the link between two memristors and how it operates, this method has been simulated and illustrated as follows: Figure 4.1(a) depicts an AND-gate in

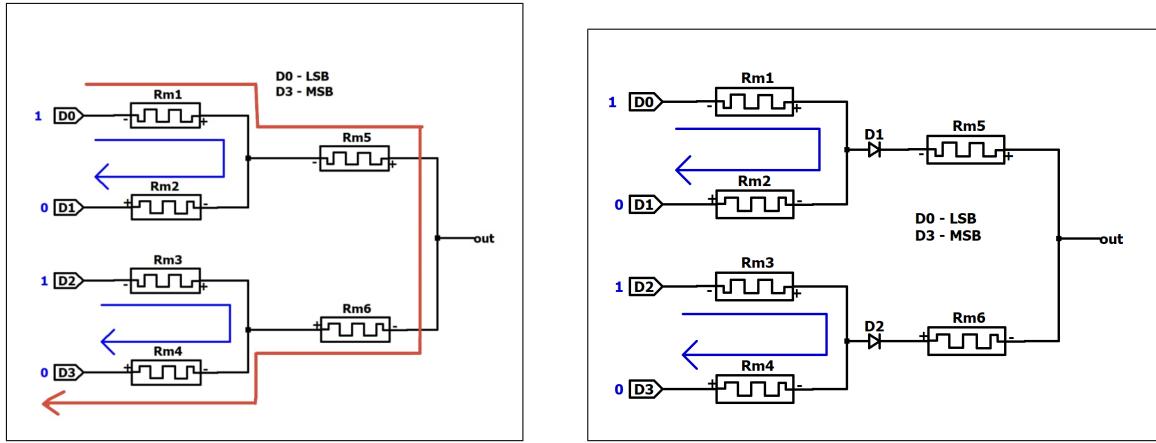


Figure 4.2: (a)Sneak path problem in a 4-bit DAC , (b) Solution for the sneak path problem

which the input voltages 'D0' and 'D1' are connected to a negative memristor sign, and the output voltage 'and' is gathered by the positive memristor sign. The 'out' is expressed as:

$$V_{and} = \frac{R_{m1} * V_{D0} + R_{m2} * V_{D1}}{R_{m1} + R_{m2}}$$

Here, R_{m1} and R_{m2} are the memristor resistances.They can be R_{on} or R_{off} depending on the voltage applied across them.

One of the major problems encountered in the Memristive DAC's is the "Sneak path problem".Several types of research has been published to solve the problem including the 1T1M(1 transistor 1 memristor) model,1D1M(1 diode 1 memristor) model and the 1S1M(1 selector 1 memristor) model [6].In our approach for the DAC , the sneak path problem will occur when the two stages are connected with each other as there is a possibility of a alternative current path leading to a division of the current.

4.3 4-bit thermometer code DAC

Here we will construct the thermometer code 4-bit DAC with 4 output levels with a Digital input of 1 V and LSB of 250 mV.

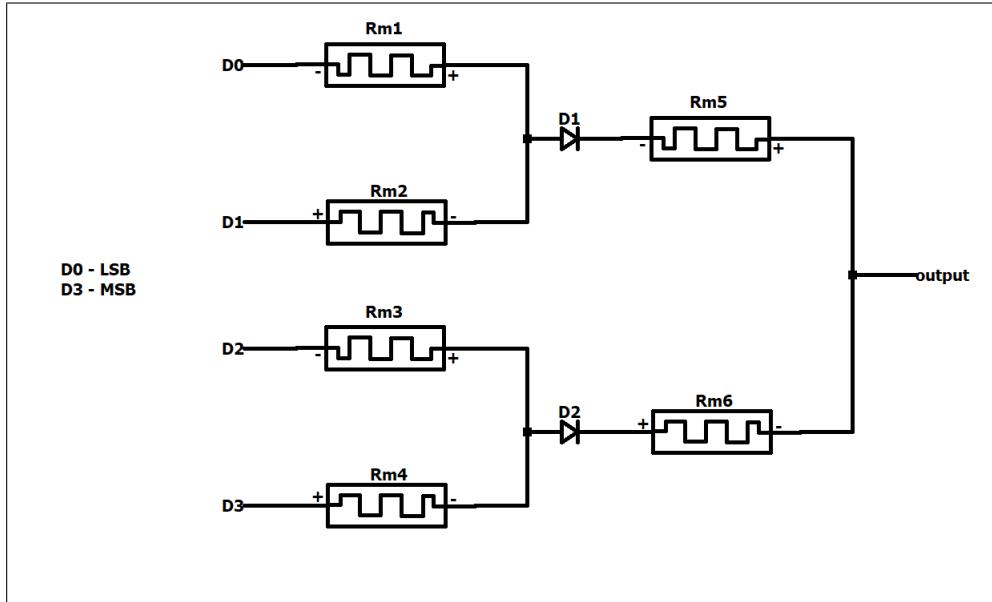


Figure 4.3: 4-bit DAC cell Schematic (Thermometer code)

Here resistances of all the memristors is taken to be the same having values according to the VTEAM model.



Figure 4.4: 4-bit DAC cell (thermometer code) transient results (Red - output ,Yellow - Expected ideal output)

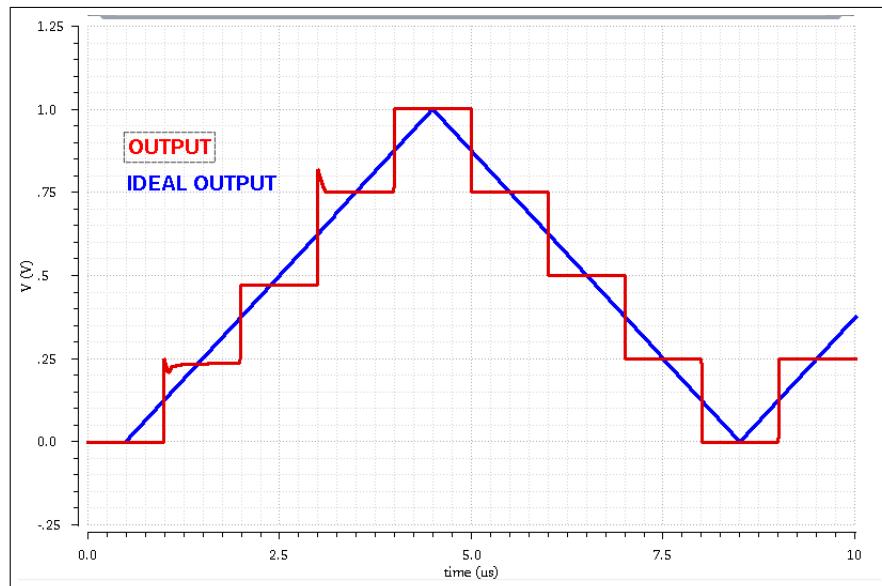


Figure 4.5: Ideal output and actual output of 4-bit thermometer code DAC (Red - output ,Blue - Expected ideal output)

Figures 4.5 shows the ideal and the actual outputs of the 4-bit DAC. Ideally we expect a ADC output to be a straight continuous line but the actual output has more like a staircase structure.

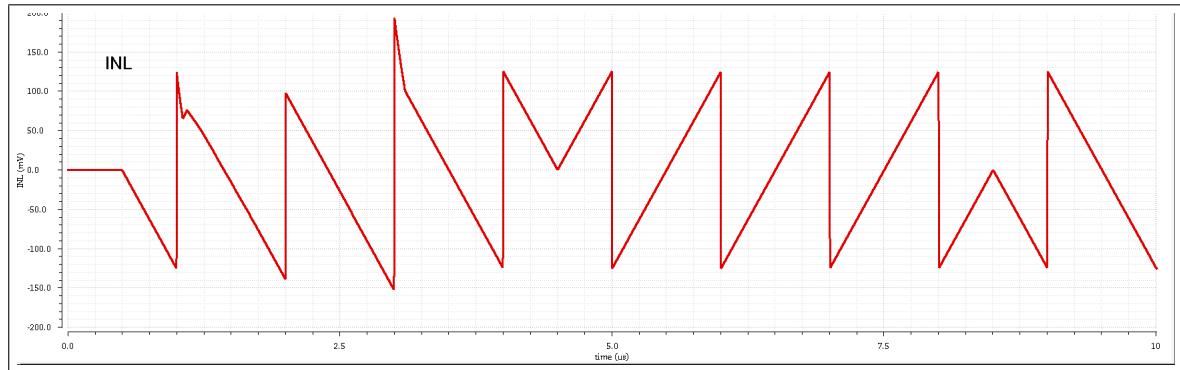


Figure 4.6: INL of 4-bit thermometer code DAC

The maximum magnitude of the INL is 190 mV which is lesser than the LSB size which is 250 mV.

4.4 8-bit thermometer code DAC

Here we will construct the thermometer code 8-bit DAC with 8 output levels with a Digital input of 1 V and LSB of 125 mV.

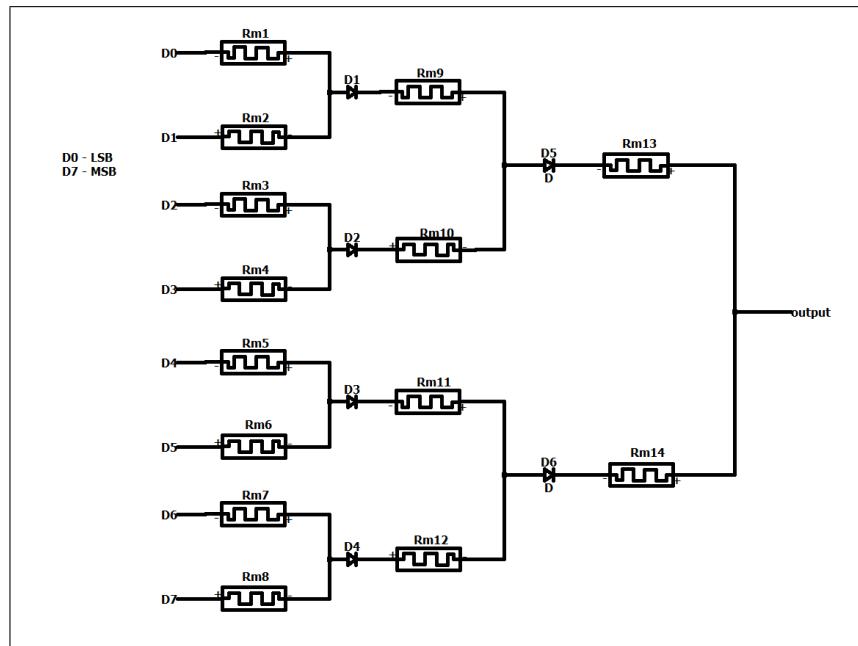


Figure 4.7: 8-bit DAC cell(thermometer code) schematic



Figure 4.8: 8-bit DAC cell(thermometer code) transient results (Red - output ,Yellow - Expected ideal output)

There are 8 levels in the output with the LSB of 125 mV.

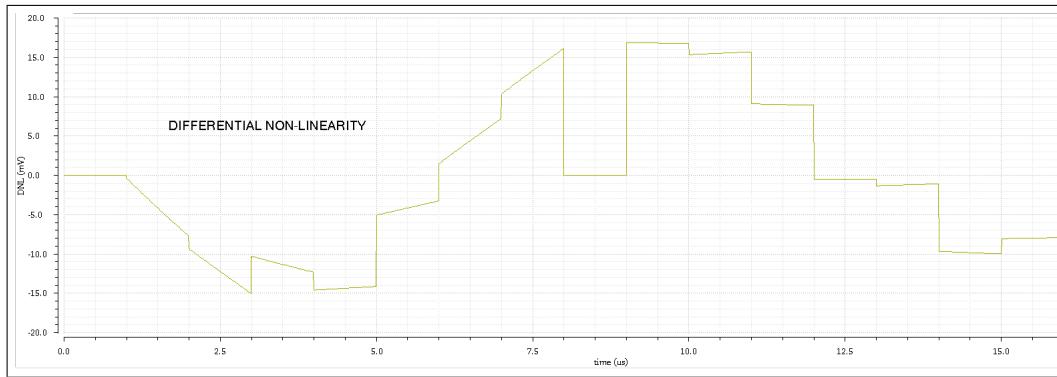


Figure 4.9: INL of 8-bit thermometer code DAC

The maximum magnitude of the INL is 80 mV which is lesser than the LSB size which is 125 mV.

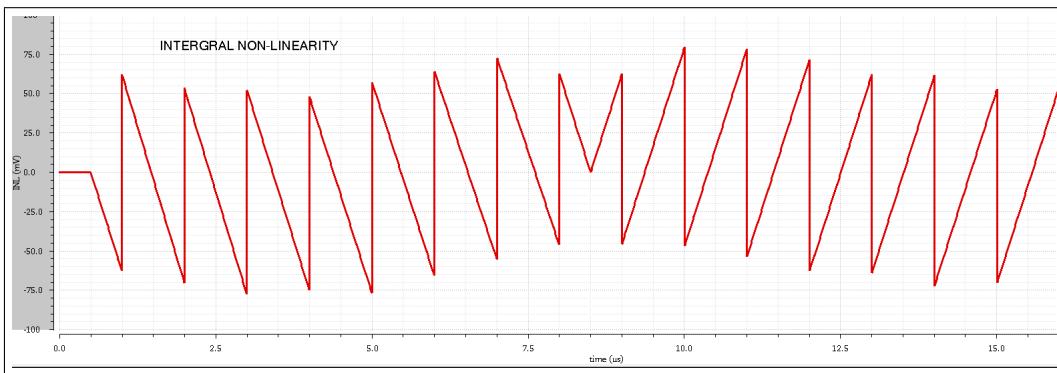


Figure 4.10: DNL of 8-bit thermometer code DAC

The maximum magnitude of the DNL is 17 mV which is much lesser than the LSB size which is 125 mV thus ensuring that there are no missing codes.

4.5 4-Bit Binary weighted DAC

Here we will construct the 4-bit DAC with the 2-bit binary weighted cell mentioned in the earlier subsection.

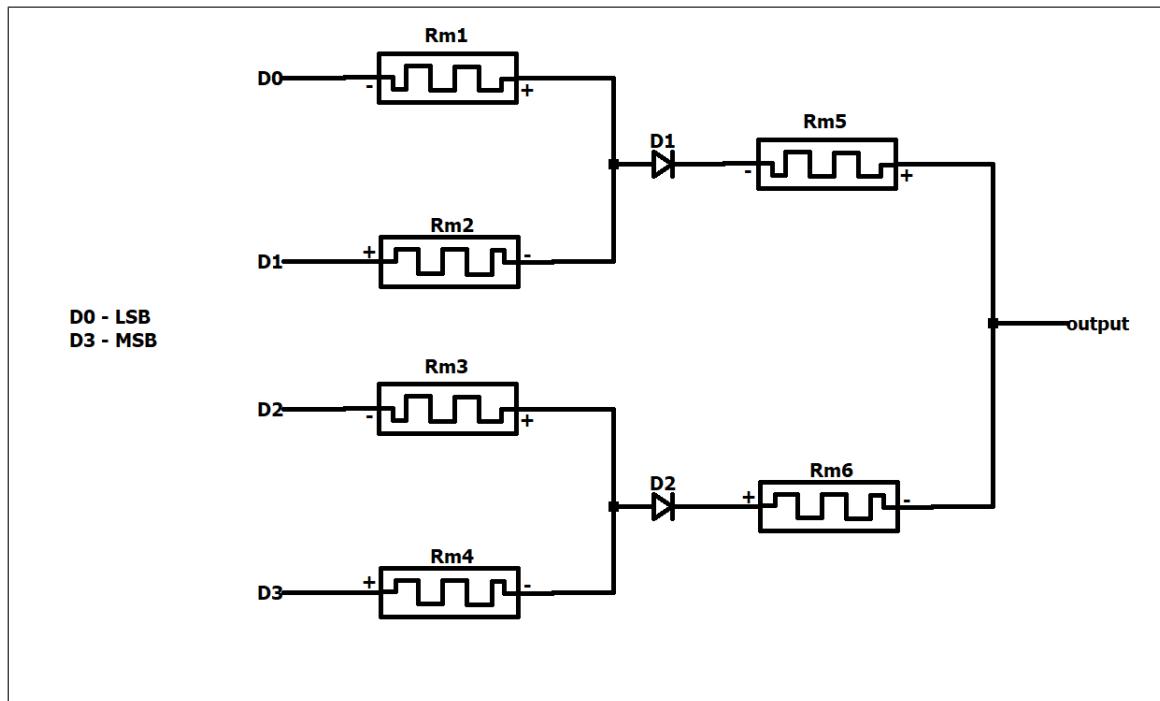


Figure 4.11: 4-bit DAC cell circuit

The input voltage levels for the digital inputs (D0-D3) are taken as 1 volt. According to the binary weighted configuration described earlier, R_m1 , R_m3 , and R_m5 are doubles of R_m2 , R_m4 , and R_m6 . The voltage step for the 4-bit DAC is 66.667 mV.

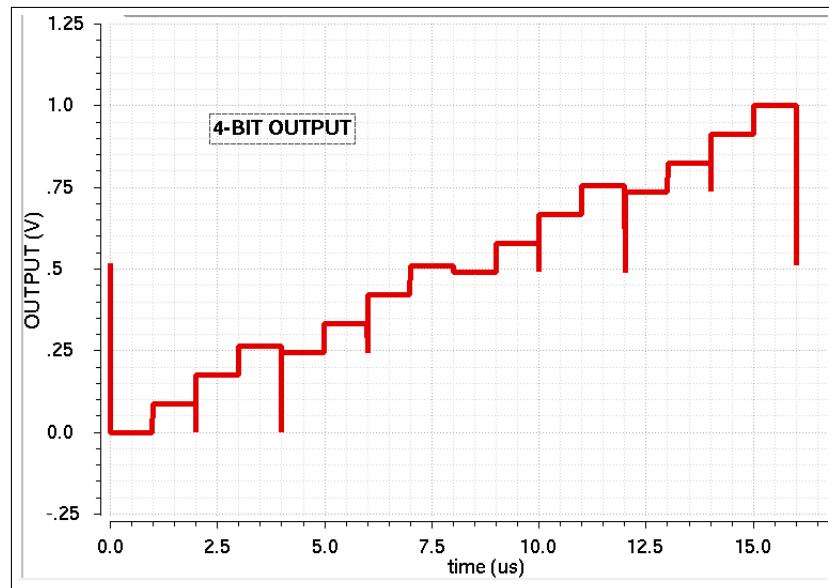


Figure 4.12: Transient simulation of 4-bit DAC cell

The 4-bit cell output is seen to have a bit of spikes which can be resolved with the appropriate use of filters. These spikes are due to sudden change in resistance.

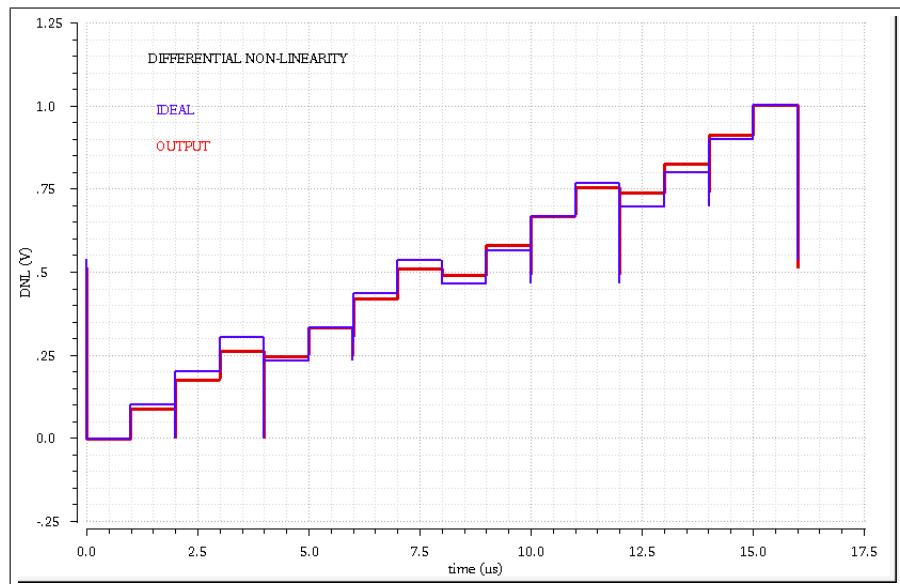


Figure 4.13: Output vs ideal output

Figures 4.13 compares output of the 4-bit to the ideal expected output.

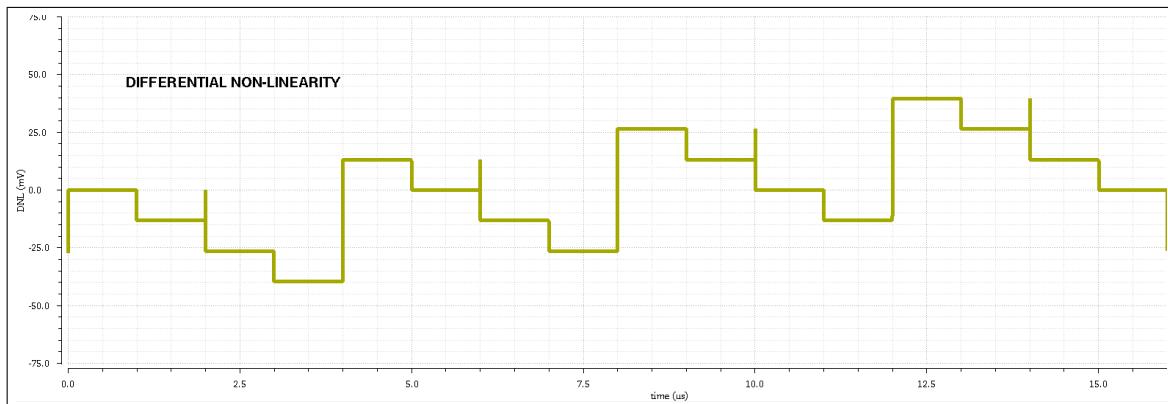


Figure 4.14: DNL of 4-bit binary weighted DAC cell

The maximum magnitude of DNL seen is 40 mV range is well within the LSB of 66.667 mV. This implies that there are no missing codes.

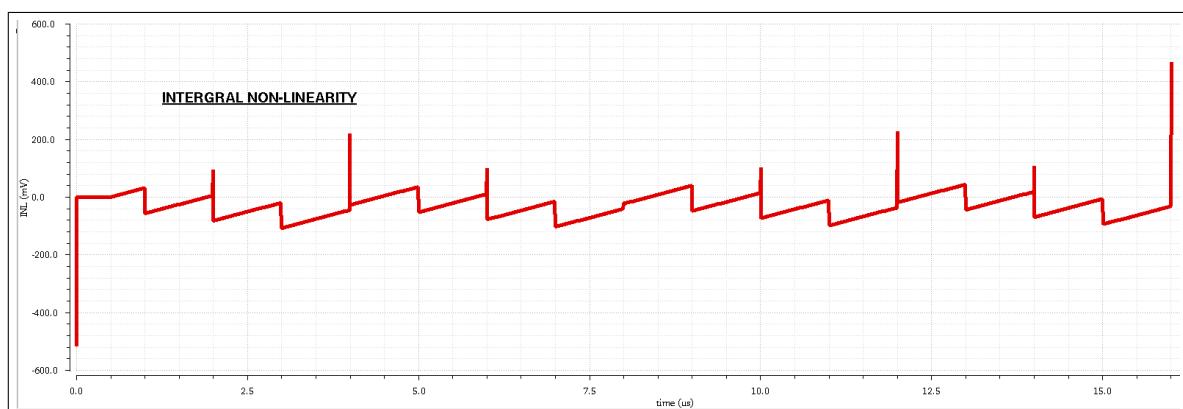


Figure 4.15: INL of 4-bit binary weighted DAC cell

The maximum magnitude of INL is 480 mV which is way above the LSB of 66.667 mV. This is due to the voltage spikes seen in the circuit and needs to be resolved. Higher resolution DAC's can be made using this 4-bit DAC as a building block.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

Different models of RRAM devices are simulated in this report. The models are simulated according to the ideal test conditions and Verilog-A specifications in [6].Also, some basic memristor-based circuits are simulated using some of the models. 4-bit and 8-bit thermometer code DAC's were simulated using the VTEAM model of the memristor. The sneak path problem was resolved by using a diode between the connecting stages of the DAC. Also, a 4-bit binary weighted DAC was simulated, and the INL and DNL parameters were measured.

5.2 Future work

Further work includes adding some more memristor models and creating a common test bench to evaluate the models for different applications. For the 4-bit DAC, the output has some spikes due to sudden changes in resistance, which affect the INL and DNL values and need to be resolved.

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