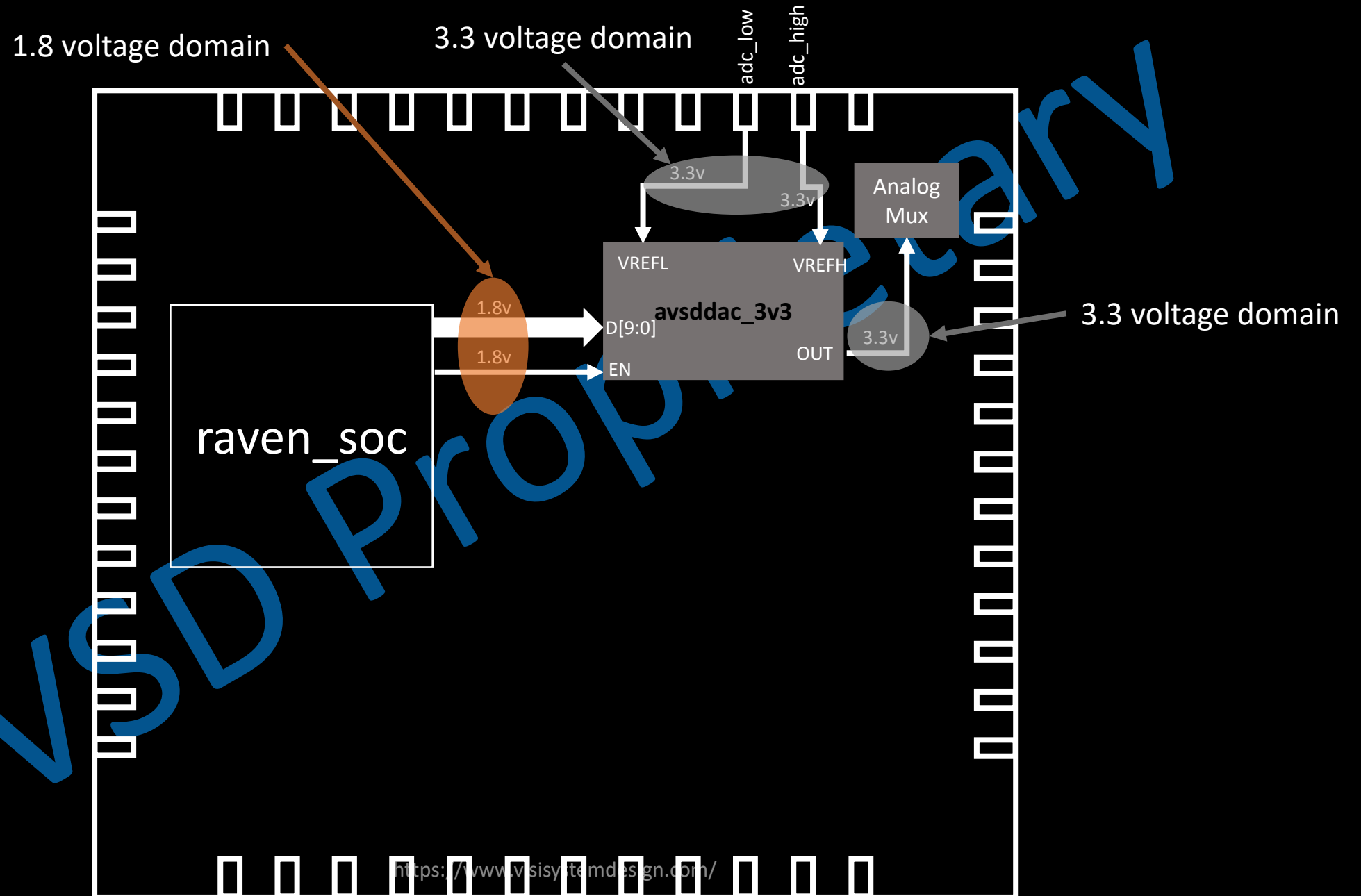


DISCLAIMER by VSD Corp. Pvt. Ltd.

- DAC (avsddac_3v3) spec sheet for 180nm tech node
- Original Specs from XFAB and Recreated by VSD Corp. Pvt. Ltd.
- To be used only for Educational purposes
- Please contact Kunal at kunalpghosh@gmail.com in case of any doubts

Application Note for dac (avsddac_3v3)



avsdac_3v3 preferred dimensions, pin locations and metal layers



 VDD, VSS pins (metal2) – 1.5 μm x 0.8 μm

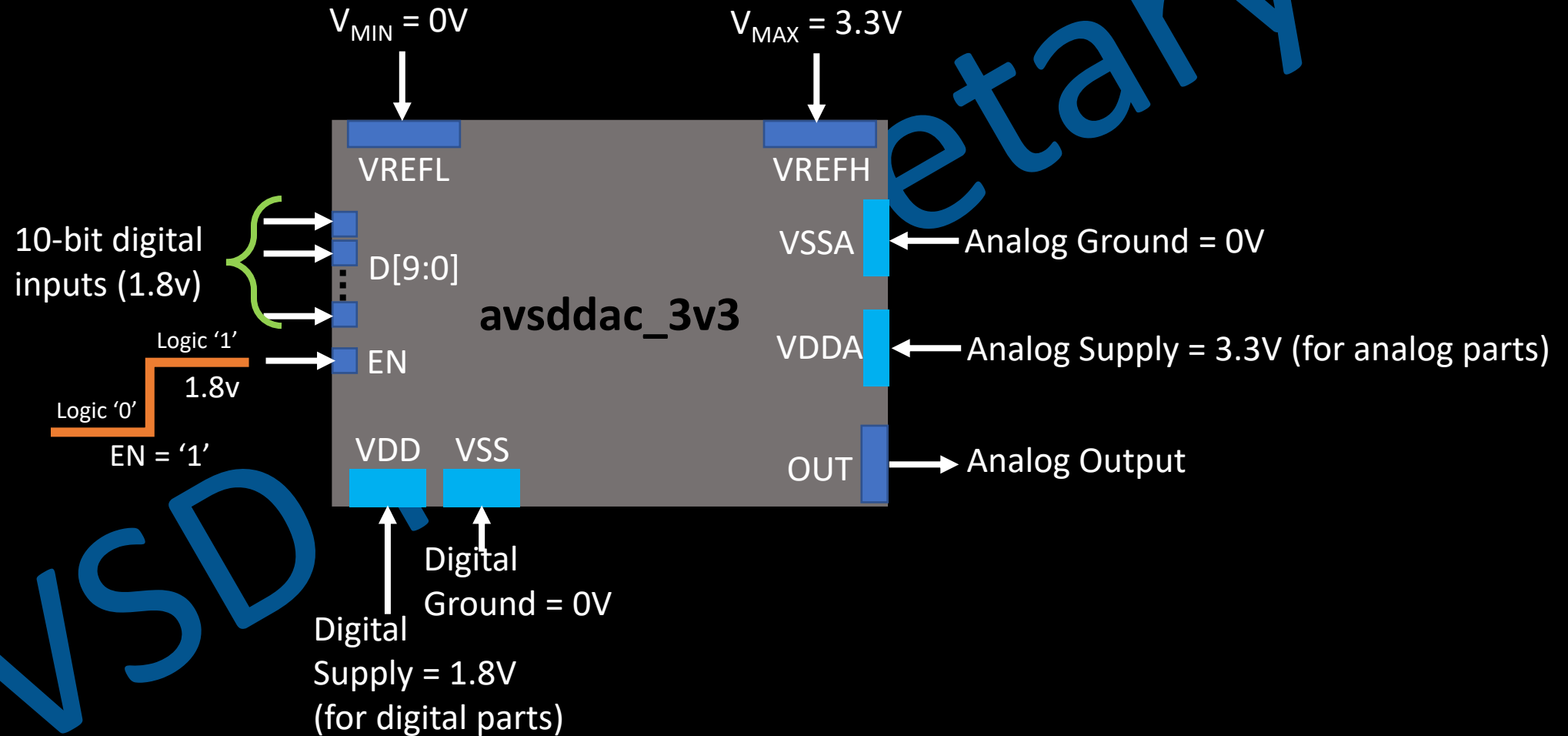
 D[9-0], EN pins (metal3) – 0.28 μm x 0.28 μm

 VREFL, VREFH pins (metal2) – 9.48 μm x 0.8 μm

 OUT pin (metal3) – 0.8 μm x 1.6 μm

 VDDA, VSSA pins (metal3) – 0.8 μm x 3 μm

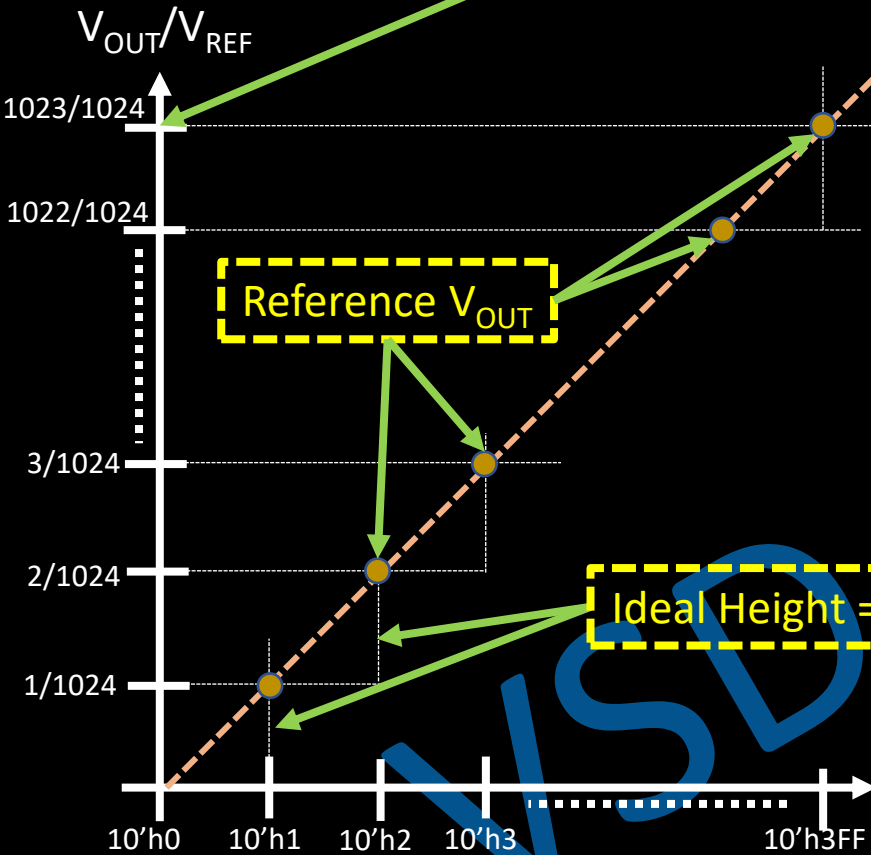
avsdac_3v3 operating modes



avsdac_3v3 operating modes

Full scale voltage
 $V_{FS} = 0V \text{ to } 3.297V$

Accuracy = 0.09%

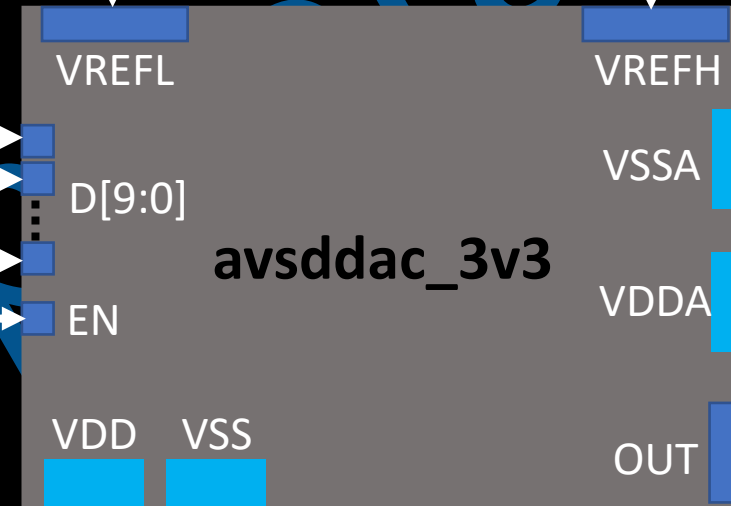


10-bit digital
inputs (1.8v)

Logic '1'
1.8v
Logic '0'
EN = '1'

$V_{MIN} = 0V$

$V_{MAX} = 3.3V$



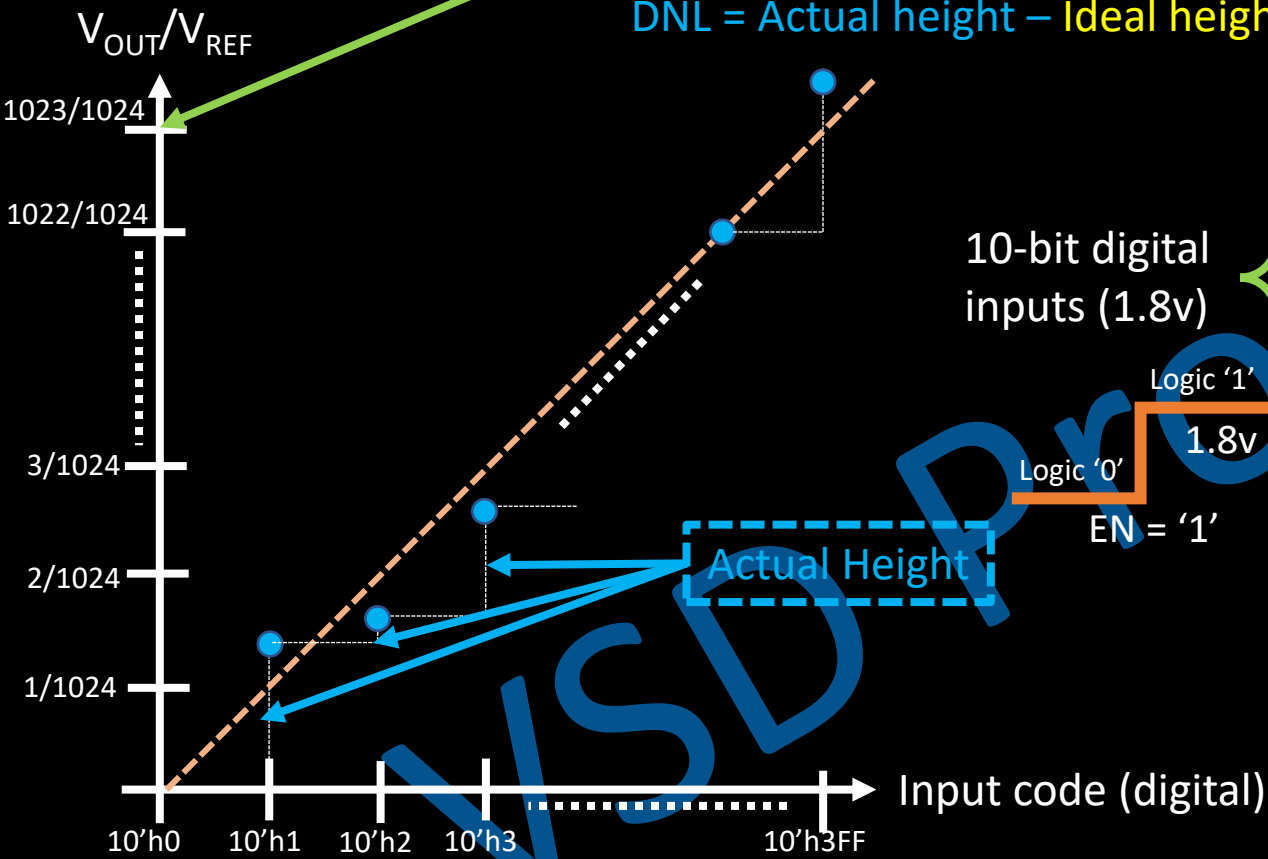
1LSB = 0.00322V or 3.2mV ($1LSB = V_{REF}/2^N$)
Resolution = 10bits (For $V_{REF}=3.3V$)

avsdac_3v3 operating modes

Full scale voltage
 $V_{FS} = 0V \text{ to } 3.297V$

Differential nonlinearity
(DNL) = 0.2LSB

DNL = Actual height – Ideal height



10-bit digital
inputs (1.8v)

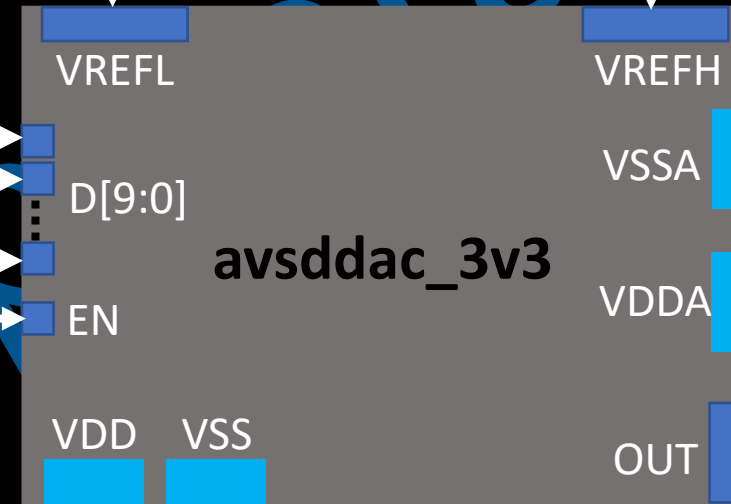
Logic '1'

Logic '0'

EN = '1'

$V_{MIN} = 0V$

$V_{MAX} = 3.3V$



DNL (LSBs)

0.2

10'h0

-0.05

10'h3FF

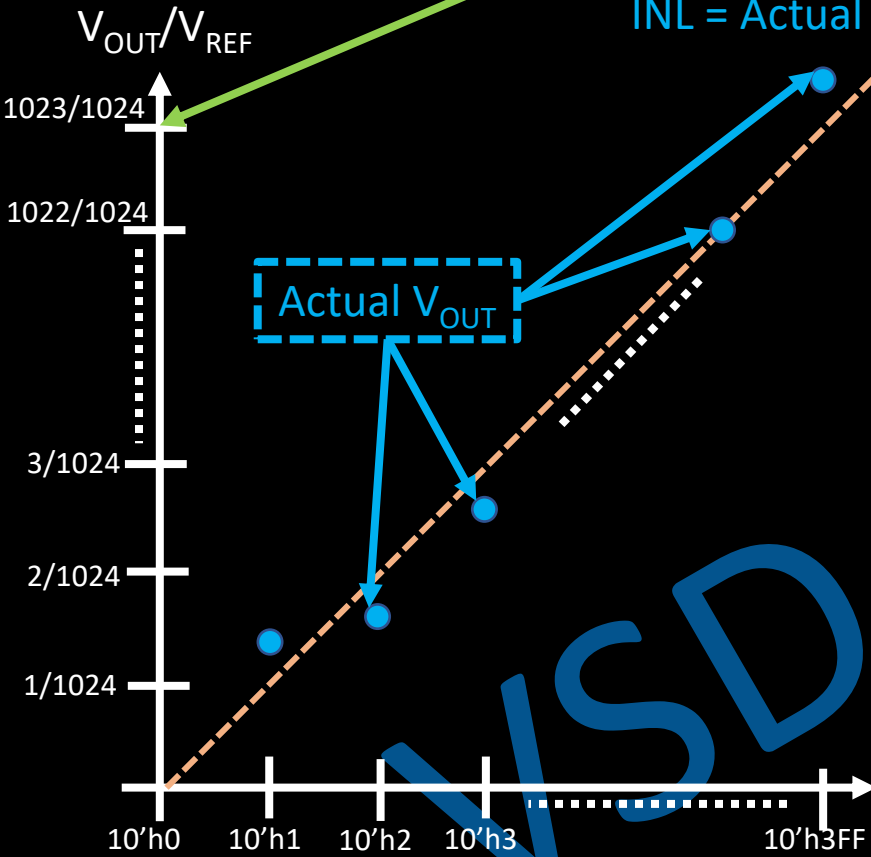
Input code (digital)

avsdac_3v3 operating modes

Full scale voltage
 $V_{FS} = 0V \text{ to } 3.297V$

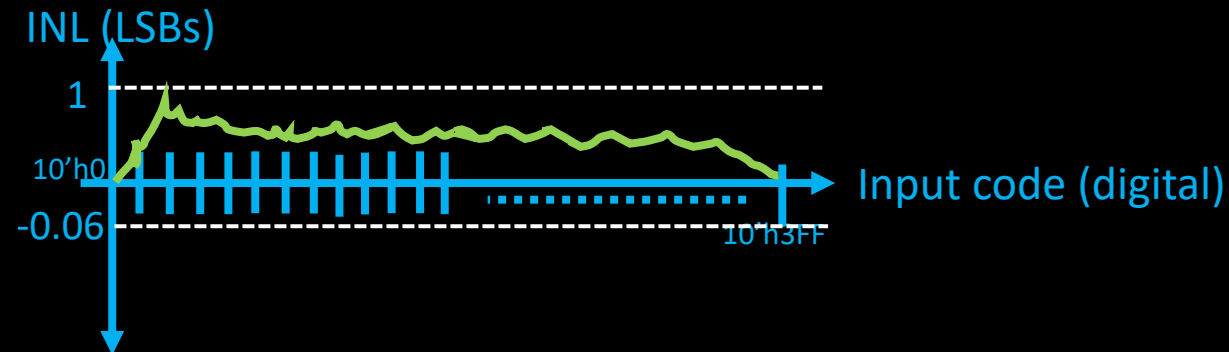
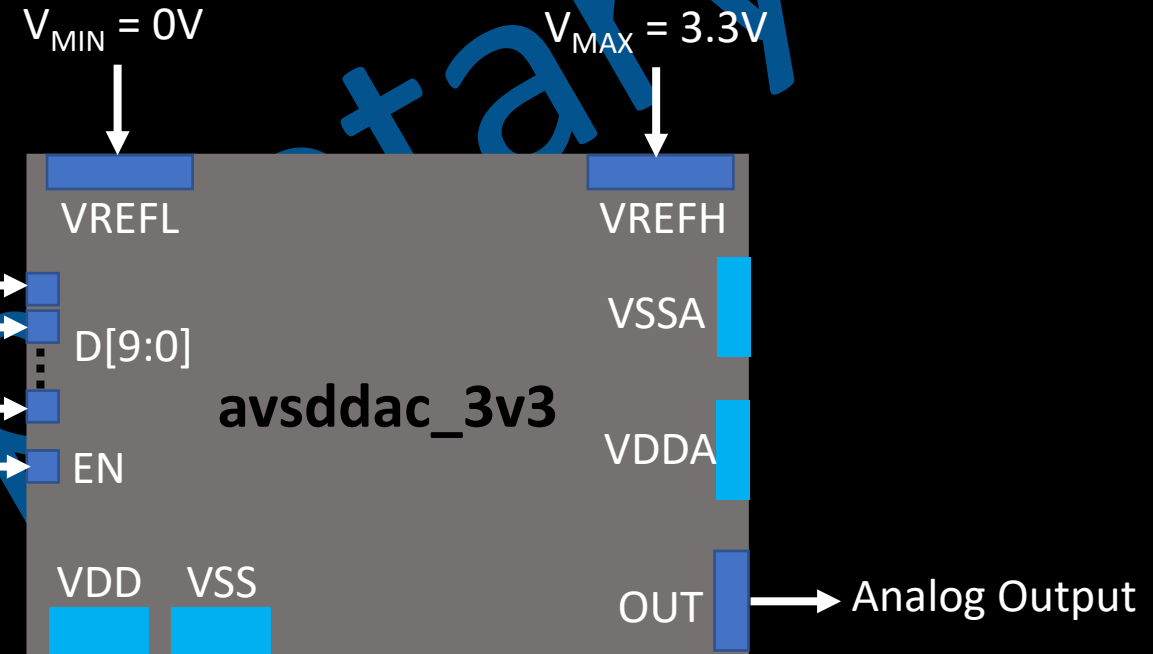
Integral nonlinearity
(INL) = 1LSB

$INL = \text{Actual } V_{OUT} - \text{Reference } V_{OUT}$

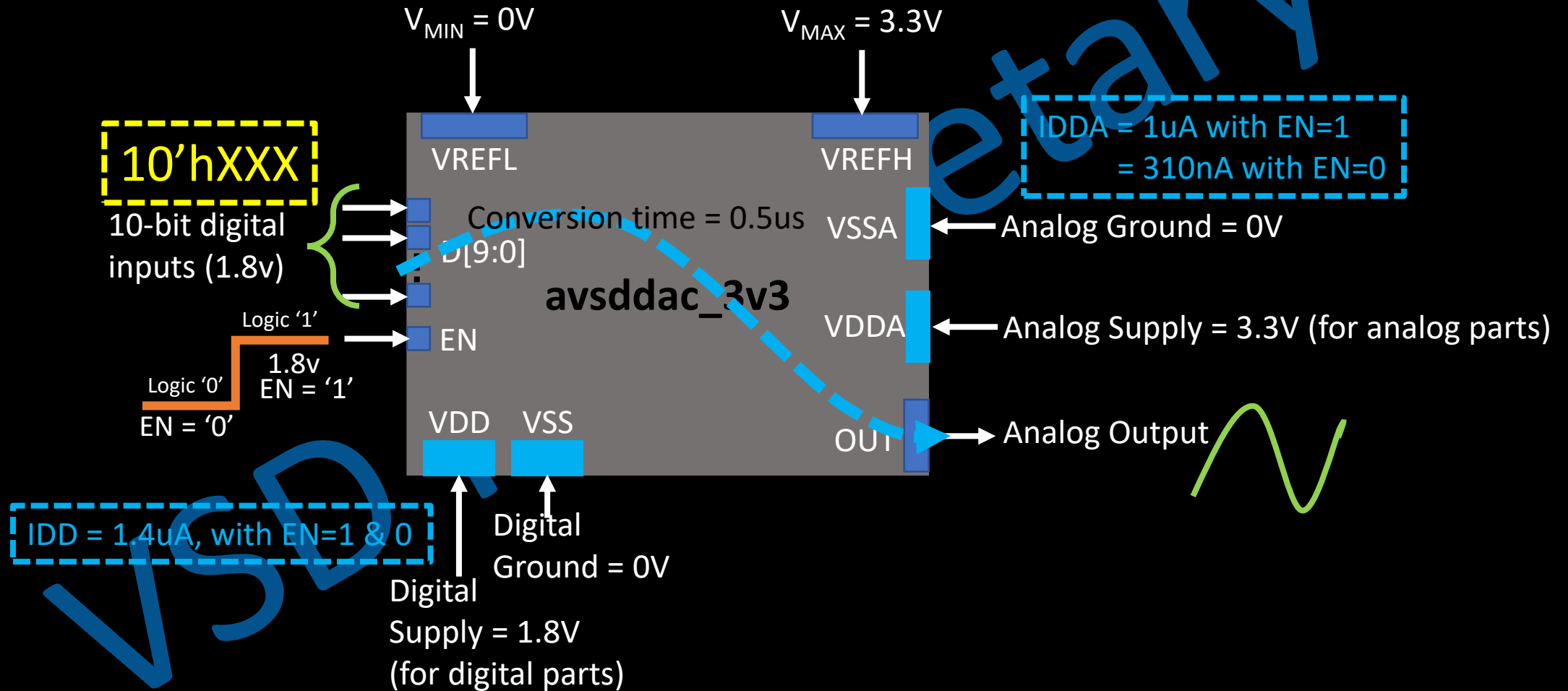


10-bit digital
inputs (1.8v)

Logic '1' 1.8v
Logic '0'
EN = '1'



avsdac_3v3 operating modes



avsdac_3v3 plots and values needed

- 1) DNL vs Digital code at $V_{REF}=V_{DD}=3.3V$ and $T=20C$ & $85C$
- 2) INL vs Digital code at $V_{REF}=V_{DD}=3.3V$ and $T=20C$ & $85C$
- 3) DNL vs Digital code at $V_{REF}=1.25V$, $V_{DD}=3.3V$ and $T=20C$ & $85C$
- 4) INL vs Digital code at $V_{REF}=1.25V$, $V_{DD}=3.3V$ and $T=20C$ & $85C$