ECE 485/585
Microprocessor System Design

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Chipsets and High Speed Interconnect

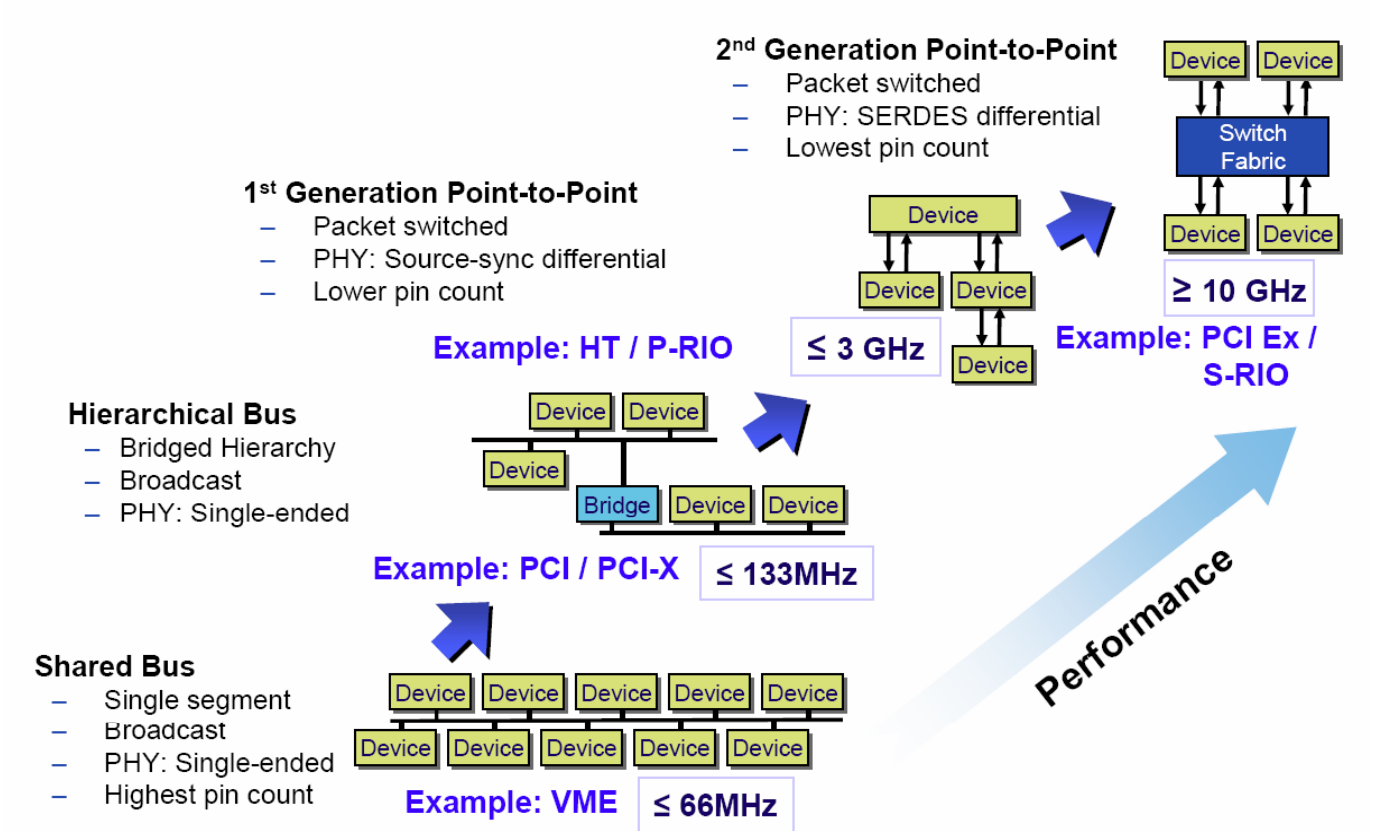
ECE 485/585

Mark G. Faust

Chipsets and High Speed Interconnect

- System Architecture Evolution
- Chipsets
- PCI Express
- QuickPath

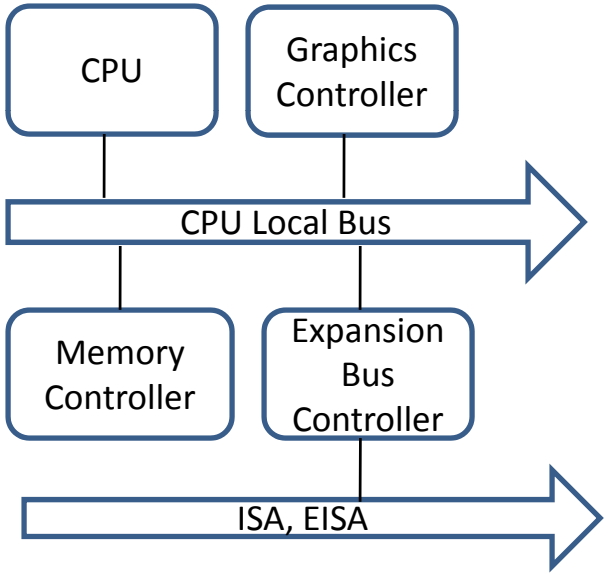
Interconnect Trends



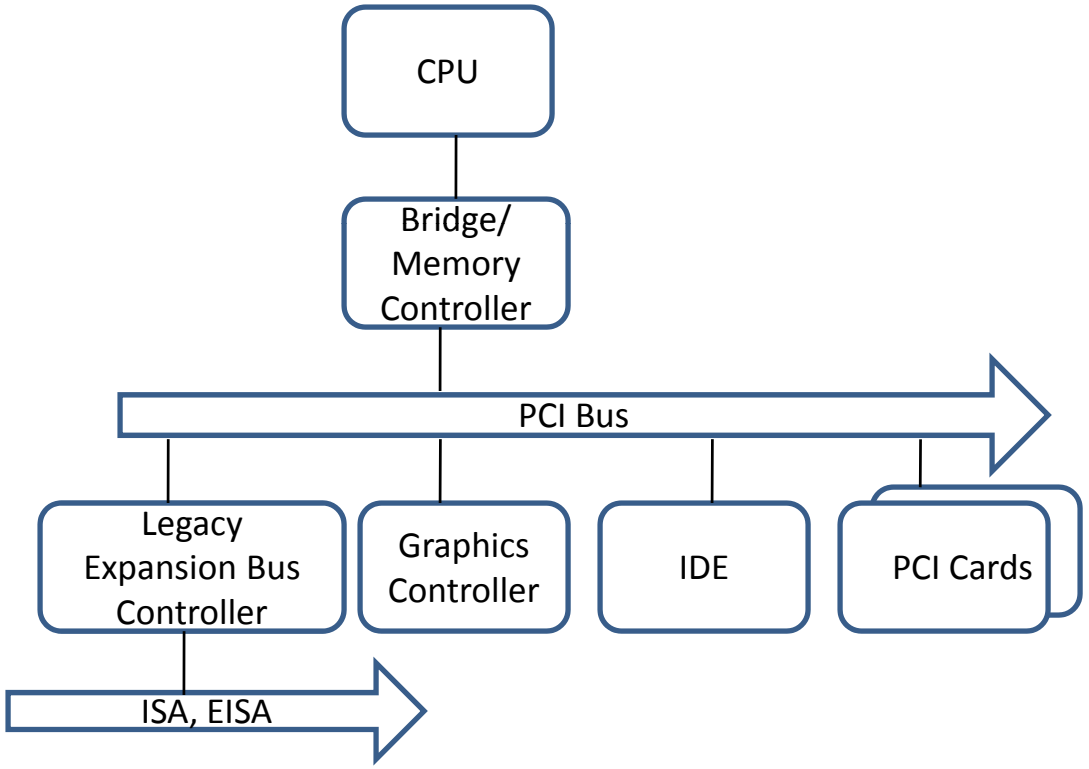
From: RapidIO Trade Association

Chipsets and PC Bus Architecture Evolution

PC Bus Evolution

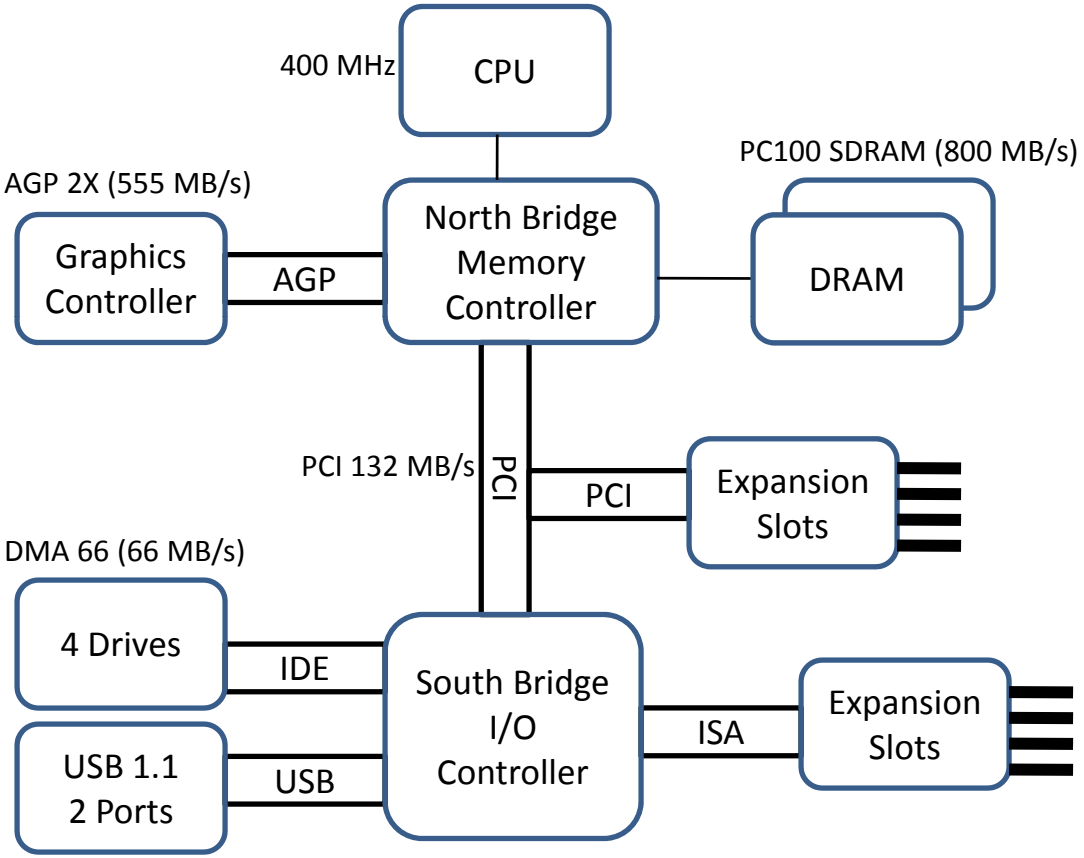


CPU Local Bus Architecture



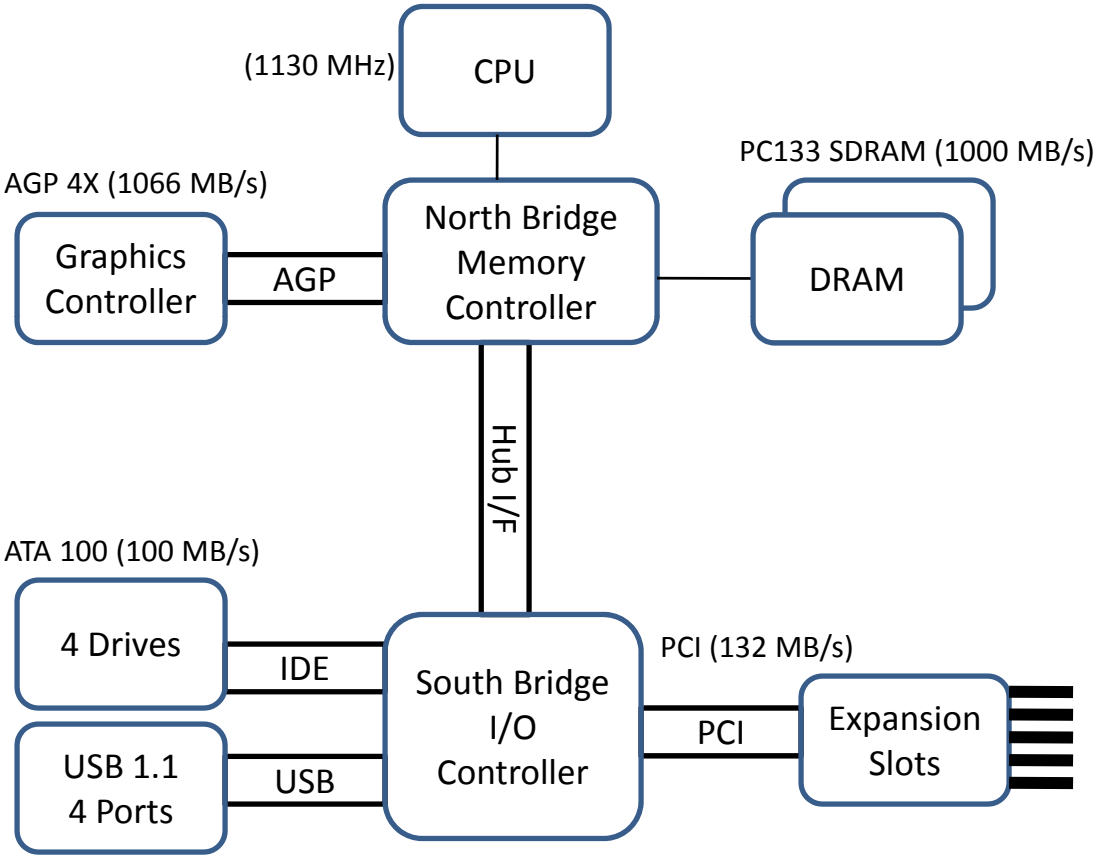
PCI Bus Architecture

PC Bus Evolution



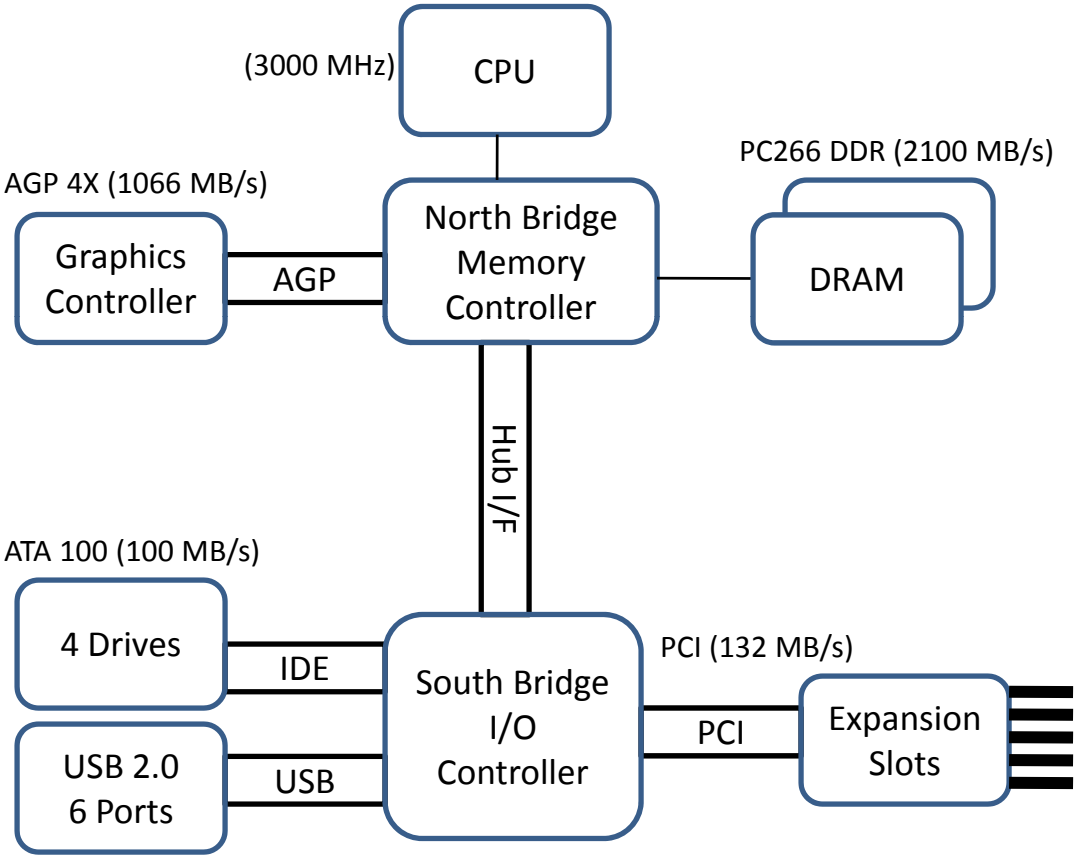
PC Architecture ~1998 (440 BX Chipset)

PC Bus Evolution

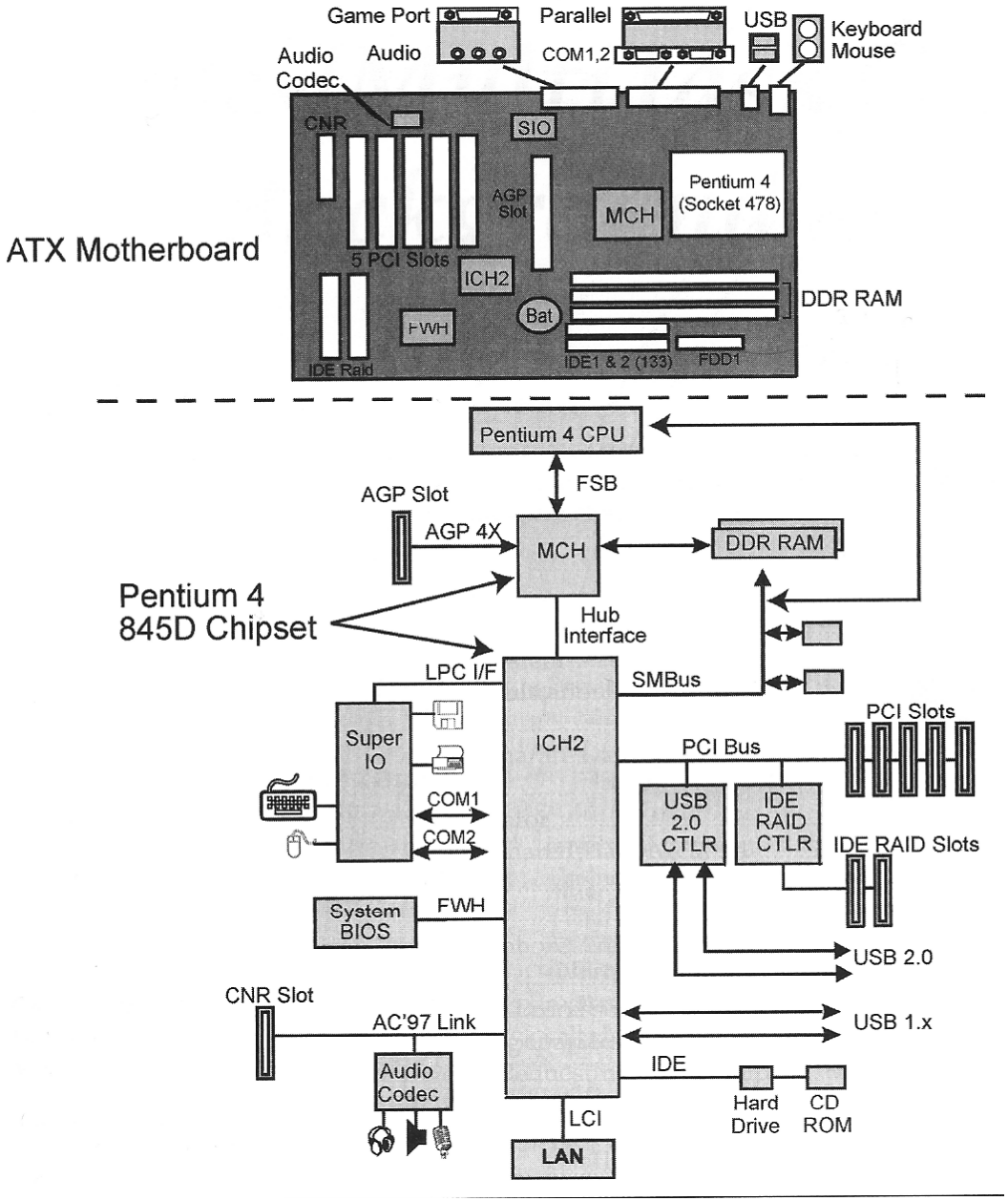


PC Architecture ~2000 (815E Chipset)

PC Bus Evolution

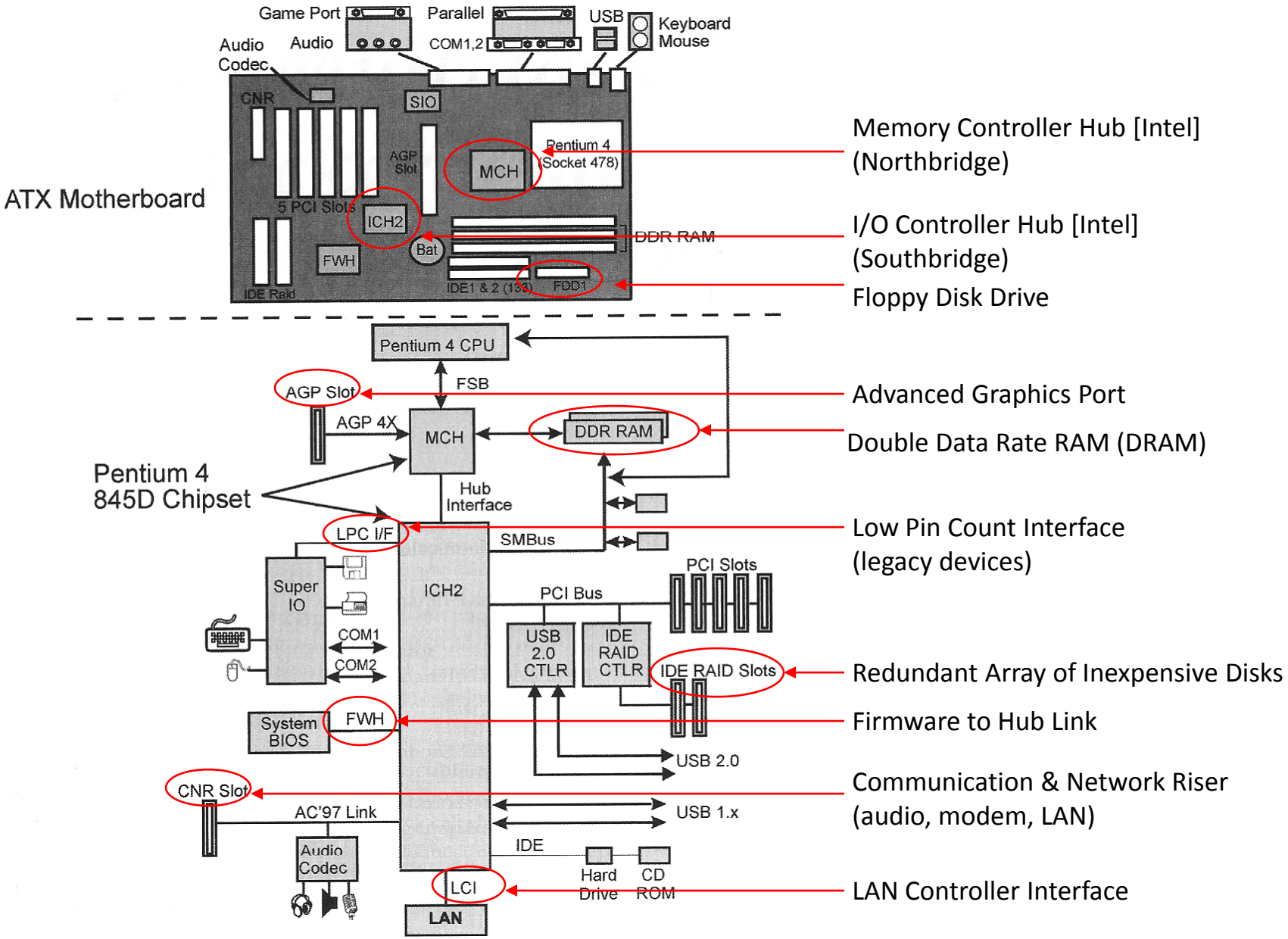


PC Architecture ~2002 (845G Chipset)



- ICH Incorporates
  - IO APIC
    (Advanced Programmable Interrupt Controller) for multiprocessor environments
  - Dual 8259a Interrupt Controllers

- MCH
  - Essentially DMA/memory controller
  - Interface
    - CPU (via FSB)
    - Graphics (AGP 8x)
    - DDR RAM
    - I/O Hub (ICH)
    - Gigabit Ethernet (bandwidth)
  - Some Intel MCH hubs incorporate graphics controller

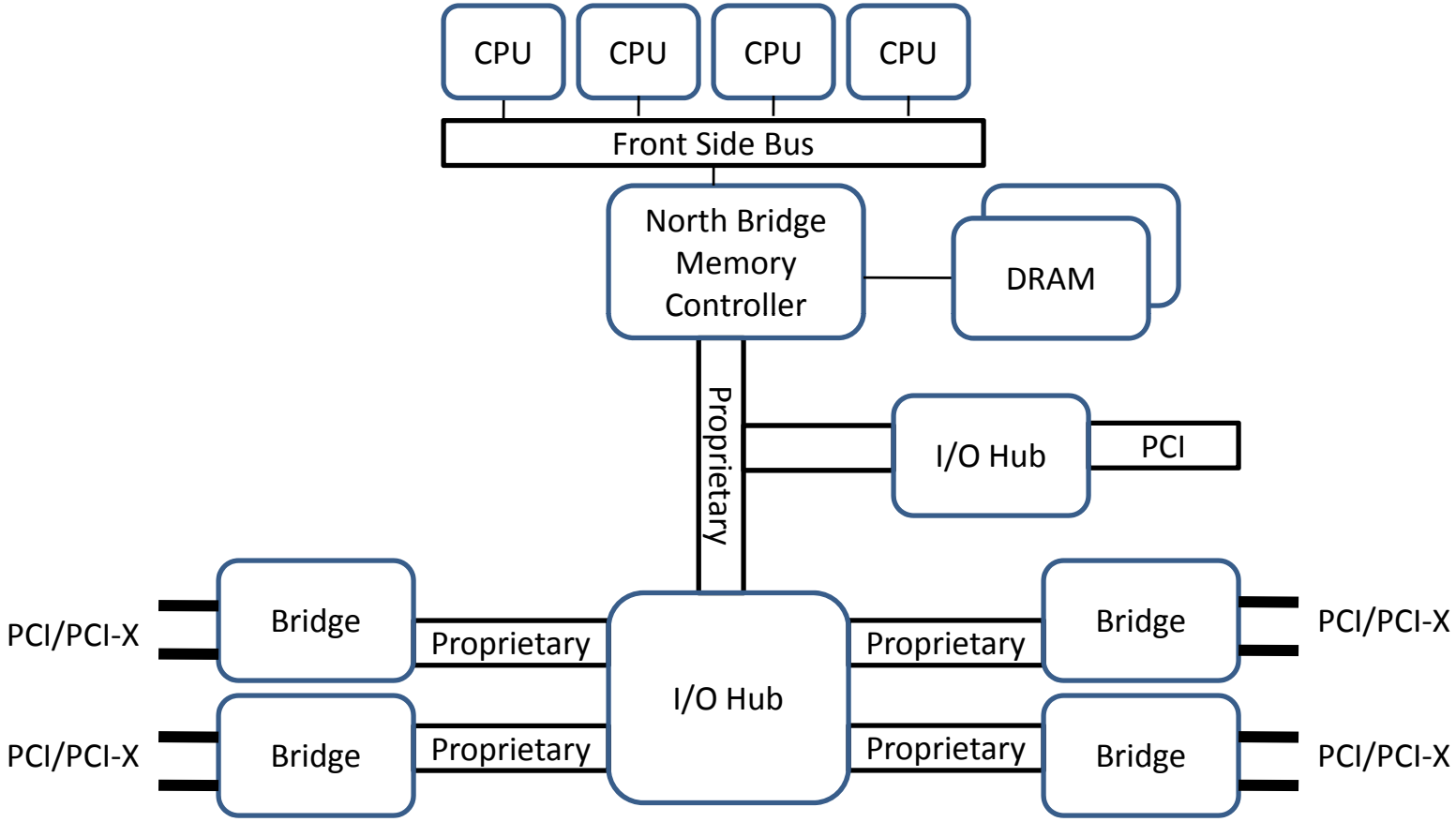

ATX Motherboard
Game Port
Parallel
USB
Keyboard
Mouse
Audio
Codec
Audio
COM1,2
CNR
SIO
AGP
Slot
MCH
Pentium 4
(Socket 478)
5 PCI Slots
ICH2
DDR RAM
FWH
Bat
IDE Raid
IDE1 & 2 (133)
FDD1
Memory Controller Hub [Intel]
(Northbridge)
I/O Controller Hub [Intel]
(Southbridge)
Floppy Disk Drive
Pentium 4 CPU
FSB
AGP Slot
AGP 4X
MCH
DDR RAM
Advanced Graphics Port
Double Data Rate RAM (DRAM)
Pentium 4
845D Chipset
Hub
Interface
LPC I/F
SMBus
Low Pin Count Interface
(legacy devices)
Super
IO
ICH2
PCI Slots
PCI Bus
COM1
COM2
USB
2.0
CTLR
IDE
RAID
CTLR
IDE RAID Slots
Redundant Array of Inexpensive Disks
System
BIOS
FWH
Firmware to Hub Link
USB 2.0
CNR Slot
AC'97 Link
USB 1.x
Communication & Network Riser
(audio, modem, LAN)
IDE
Audio
Codec
Hard
Drive
CD
ROM
LCI
LAN
LAN Controller Interface

Pentium 4 Chipset Comparison

	875P chip set	845GL chip set
Target segment	Performance PC	Value PC
System bus (64 bit)	800/533 MHz	400 MHz
Memory controller hub ("north bridge")		
Package size, pins	42.5 × 42.5 mm, 1005	37.5 × 37.5 mm, 760
Memory speed	DDR 400/333/266 SDRAM	DDR 266/200, PC133 SDRAM
Memory buses, widths	2 × 72	1 × 64
Number of DIMMs, DRAM Mbit support	4, 128/256/512 Mbits	2, 128/256/512 MBits
Maximum memory capacity	4 GB	2 GB
Memory error correction available?	yes	no
AGP graphics bus, speed	yes, 8X or 4X	no
Graphics controller	external	Internal (Extreme Graphics)
CSA Gigabit Ethernet interface	yes	no
South bridge interface speed (8 bit)	266 MHz	266 MHz
I/O controller hub ("south bridge")		
Package size, pins	31 × 31 mm, 460	31 × 31 mm, 421
PCI bus: width, speed, masters	32-bit, 33 MHz, 6 masters	32-bit, 33 MHz, 6 masters
Ethernet MAC controller, interface	100/10 Mbit	100/10 Mbit
USB 2.0 ports, controllers	8, 4	6, 3
ATA 100 ports	2	2
Serial ATA 150 controller, ports	yes, 2	no
RAID 0 controller	yes	no
AC-97 audio controller, interface	yes	yes
I/O management	SMbus 2.0, GPIO	SMbus 2.0, GPIO

FIGURE 8.12 Two Pentium 4 I/O chip sets from Intel. The 845GL north bridge uses many fewer pins than the 875 by having just one memory bus and by omitting the AGP bus and the Gigabit Ethernet interface. Note that the serial nature of USB and Serial ATA means that two more USB ports and two more Serial ATA ports need just 39 more pins in the south bridge of the 875 versus the 845GL chip sets.

Server Architecture



PC Bus Evolution

PCI

$$33.3\ MHz \times 4\ bytes = 133\ MB/s$$

$$\frac{133\ MB/s}{74\ pins} = 1.8\frac{MB}{s}/pin$$

PCI-X 2.0

$$533\ MHz \times 8\ bytes = 4264\ MB/s$$

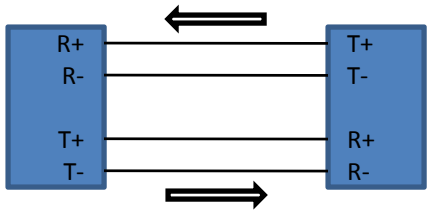
$$\frac{4264\ MB/s}{150\ pins} = 28.4\frac{MB}{s}/pin$$

PCI Express (PCI-e)

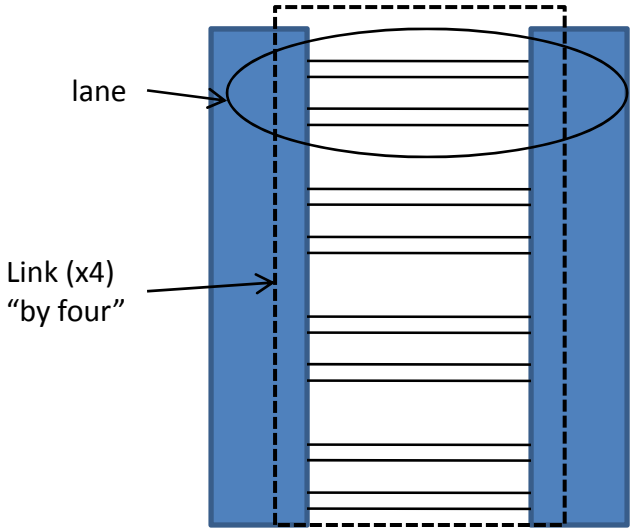
$$2500\ MHz \times 1\ bit \times \frac{1\ byte}{10\ bits} = 250\ MB/s\ (TX)$$

$$2500\ MHz \times 1\ bit \times \frac{1\ byte}{10\ bits} = 250\ MB/s\ (RX)$$

$$\frac{500\ MB/s}{8\ pins} = 62.5\frac{MB}{s}/pin$$

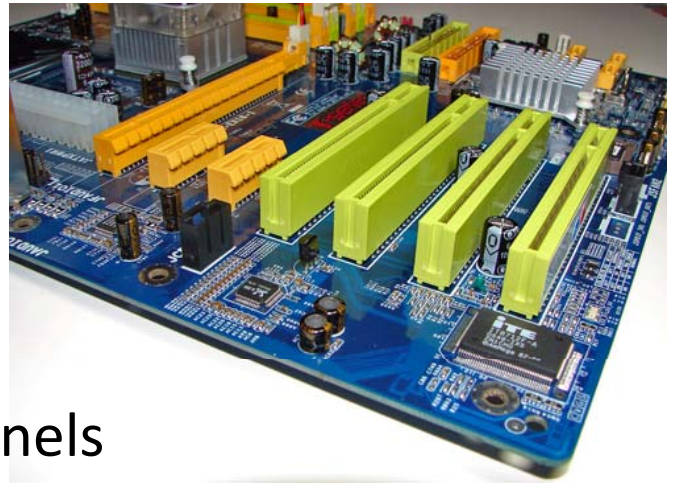


A "lane" – a point-to-point connection between two PCI-e devices



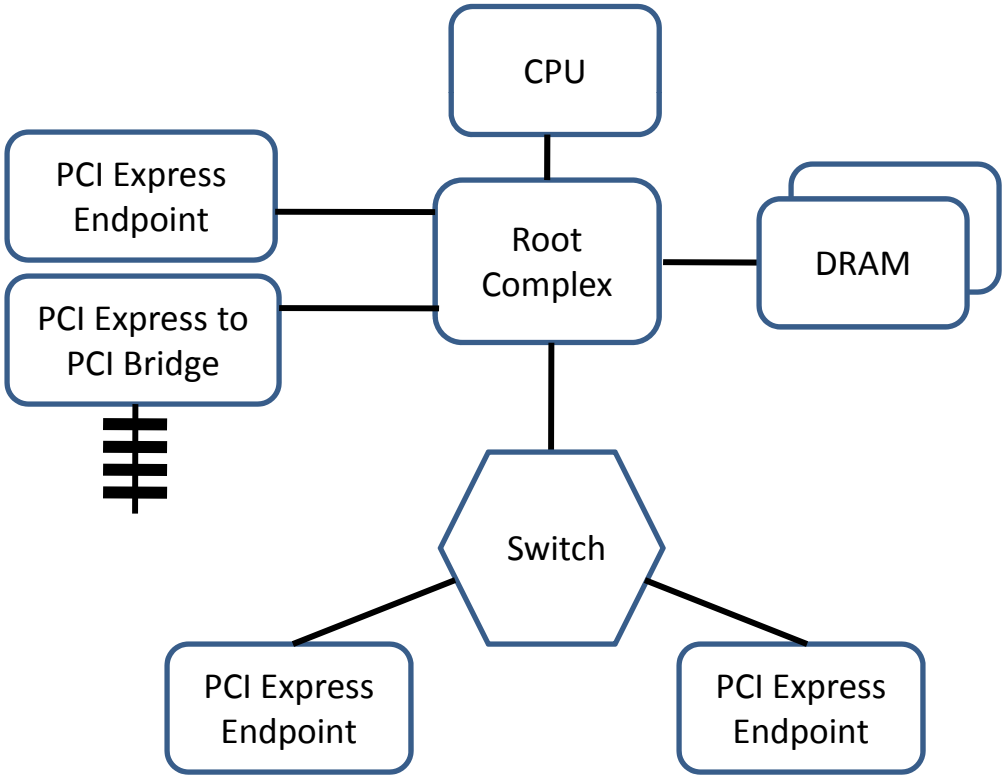
PCI Express

- Benefits
  - Smaller physical interface
  - Scalability (not shared bus architecture)
    - Additional point-to-point links
    - Flexible point-to-point links
      - x1, x2, x4, x8, x12, x16, x32
  - Support for quality of service
    - Isochronous transfers
    - Traffic “classes” and virtual channels
  - S/W compatibility with PCI

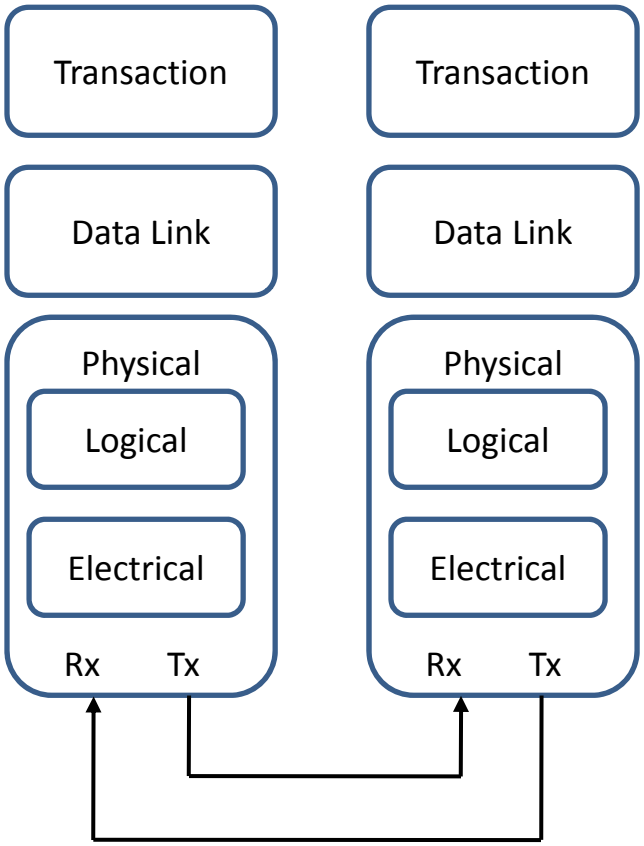


PCI Express

- Device types
  - Root complex, PCIe to PCI bridge, endpoint, switch

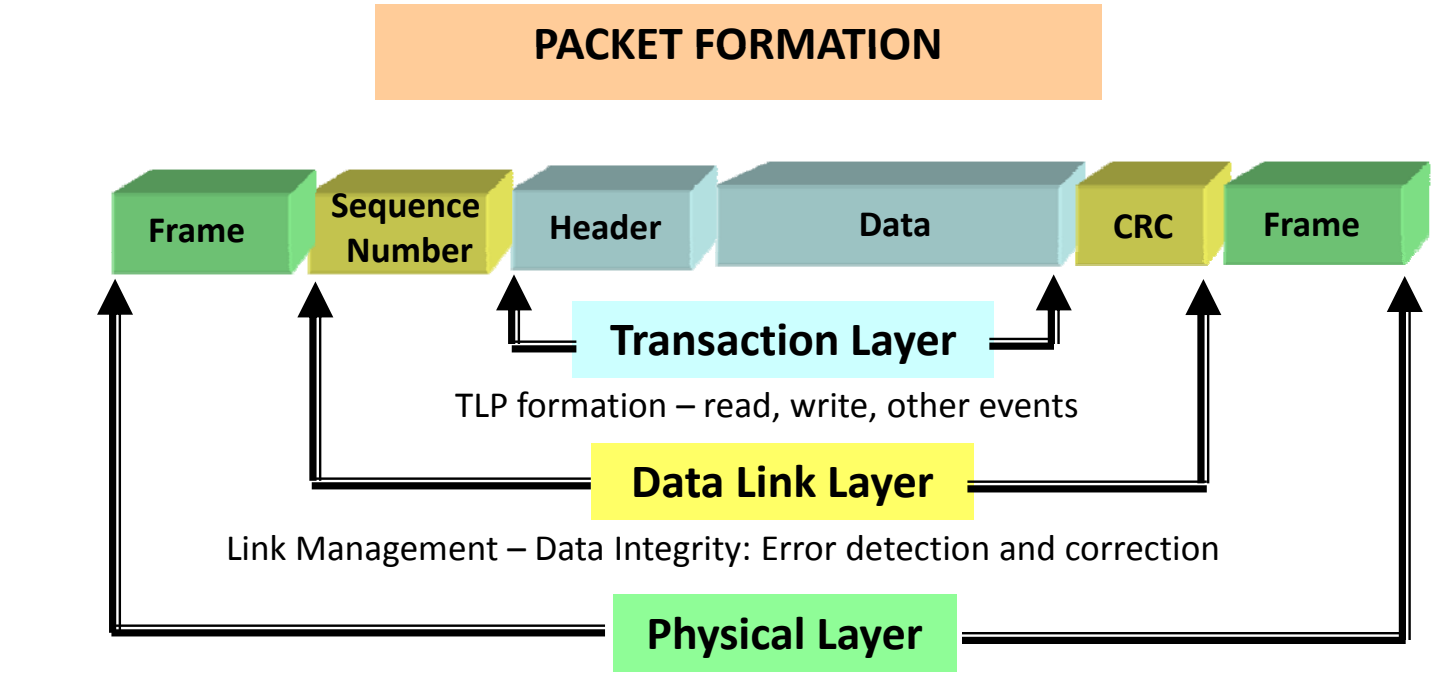


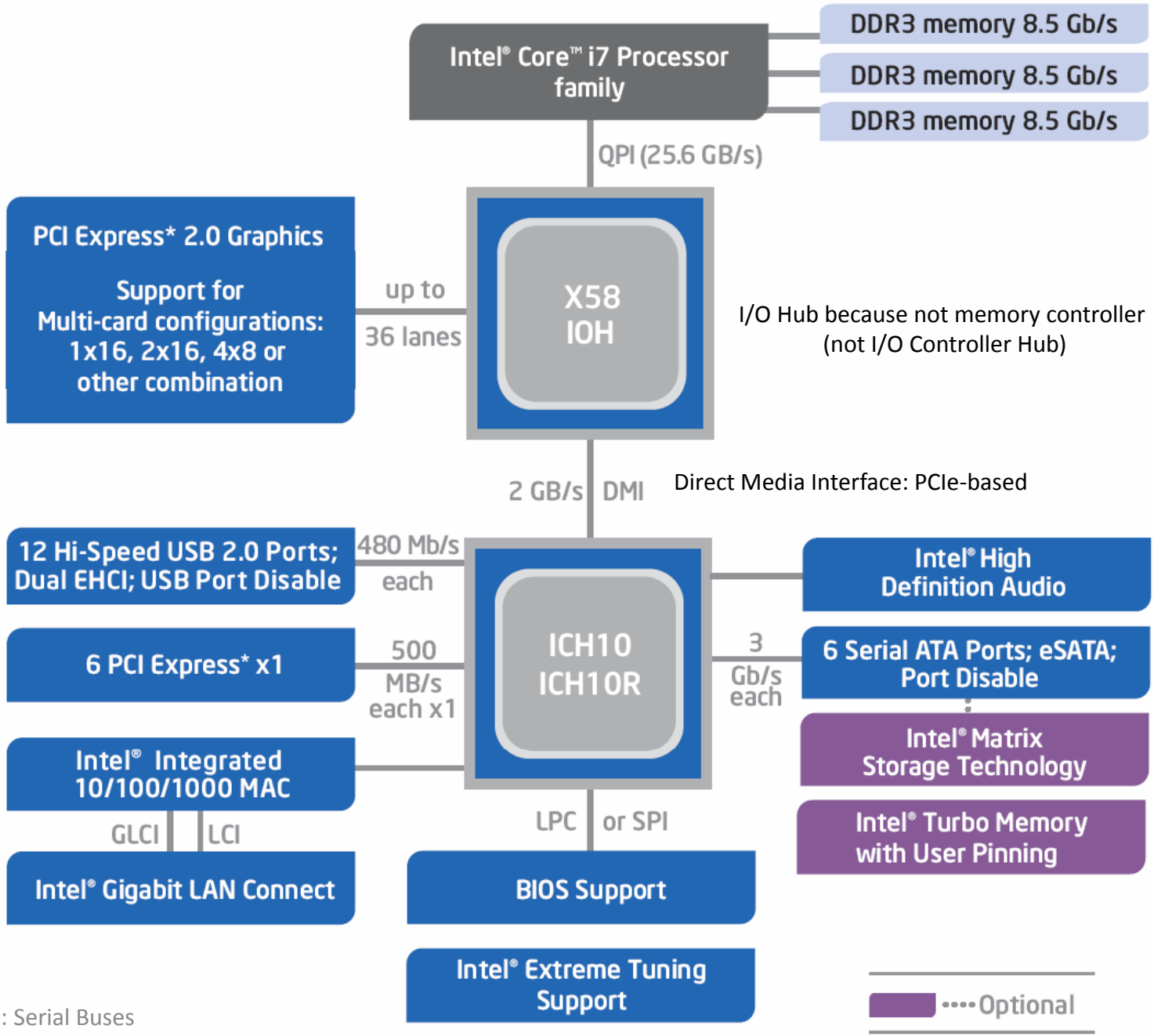
PCI Express Layers



- The transaction layer assembles and disassembles transaction layer packets
- The data link layer primarily handles link management and error detection/correction
- The physical (PHY) layer provides logic and circuitry needed to serialize/deserialize data, drive transmitted bits or buffer received bits on each lane.

PCI Express – Layered Architecture




Intel® Core™ i7 Processor family
DDR3 memory 8.5 Gb/s
DDR3 memory 8.5 Gb/s
DDR3 memory 8.5 Gb/s
QPI (25.6 GB/s)
PCI Express* 2.0 Graphics
Support for Multi-card configurations: 1x16, 2x16, 4x8 or other combination
up to
36 lanes
X58 IOH
I/O Hub because not memory controller (not I/O Controller Hub)
2 GB/s
DMI
Direct Media Interface: PCIe-based
12 Hi-Speed USB 2.0 Ports; Dual EHCI; USB Port Disable
480 Mb/s each
6 PCI Express* x1
500 MB/s each x1
Intel® Integrated 10/100/1000 MAC
GLCI
LCI
Intel® Gigabit LAN Connect
ICH10 ICH10R
3 Gb/s each
Intel® High Definition Audio
6 Serial ATA Ports; eSATA; Port Disable
Intel® Matrix Storage Technology
Intel® Turbo Memory with User Pinning
LPC
or SPI
BIOS Support
Intel® Extreme Tuning Support
Optional

QuickPath Interconnect

Transfer Speeds

Technology	Bit Rate (GT/s)
Intel front-side bus	1.6[1]
Intel® QuickPath Interconnect	6.4/4.8
Fully-Buffered DIMM	4.0[2]
PCI Express* Gen1[3]	2.5
PCI Express* Gen2[3]	5.0
PCI Express* Gen3[3]	8.0