**I updated Project files on Github :**

**Date : 24th November (Thursday), Hours: 5**

Understanding given paper “R. Gutierrez, V. Torres and J. Valls, "Hardware Architecture of a Gaussian Noise Generator Based on the Inversion Method," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 59, no. 8, pp. 501-505, Aug. 2012.”

I read 4 different papers to understand different aspects of the paper.

1. D. U. Lee, W. Luk, J. Villasenor and P. Y. K. Cheung, "Hierarchical segmentation schemes for function evaluation," Proceedings. 2003 IEEE International Conference on Field-Programmable Technology (FPT) (IEEE Cat. No.03EX798), 2003, pp. 92-99

To understand How to calculate Chebyshev Polynomials and Generate Coefficients in terms Coef0-2

1. Pierre L'Ecuyer. 1996. Maximally equidistributed combined Tausworthe generators. Math. Comput. 65, 213 (January 1996), 203-213. DOI=http://dx.doi.org/10.1090/S0025-5718-96-00696-5

To understand Combined Taussworthe used for Generating URNG in given paper

1. R. C. C. Cheung, D. U. Lee, W. Luk and J. D. Villasenor, "Hardware Generation of Arbitrary Random Number Distributions From Uniform Distributions Via the Inversion Method," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 15, no. 8, pp. 952-962, Aug. 2007

To understand Segmentation and mask block scheme, and understand mask to zero

1. D. U. Lee, J. D. Villasenor, W. Luk and P. H. W. Leong, "A hardware Gaussian noise generator using the Box-Muller method and its error analysis," in IEEE Transactions on Computers, vol. 55, no. 6, pp. 659-671, June 2006.

To understand normalization procedure

1. V. G. Oklobdzija, "An algorithmic and novel design of a leading zero detector circuit: comparison with logic synthesis," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 2, no. 1, pp. 124-128, March 1994.

Leading Zero Detector Circuit

**Date : 26th November (Saturday) , Hours:4**

* Worked on Matlab Code
* Generating Chebyshev Polynomial 2nd Degree Coefficients (ROM\_coef)
* Tausworthe Generator, Leading Zero Detection, Masking to Zero Functions
* Completed matlab code for GNG using ICDF as in the paper

**Date: 27th November (Sunday), Hours: 5**

* Worked on Verilog Code
* Tausworthe Generator, Leading Zero Detection, Masking to Zero modules and testbench for each module
* Writing ROM\_coef module and its matlab file writing for binary conversion
* Completed top level module for GNG using ICDF in verilog.

**Date: 9th December (Friday), Hours: 1**

* Worked on Matlab code and commenting on it.

**What is remaining? How many more hours needed ?**

* Testbench for top module, Testing Matlab Code, Cross-simulation between matlab and RTL code (3-4 Hours)
* Constraint File and complete analysis in terms of Power, Clock frequency, and slice count of hardware on Xilinx Virtex-5 FPGA (1 Hour)
* Project report writing (1-2 Hours)