THE UNIVERSITY OF THE WEST INDIES

EXAMINATIONS OF DECEMBER 2009

Code and Name of Course: **ECNG3006 Microprocessor Systems** Paper:

Date and Time: **Dec 10th 2009 9 AM** Duration: **Three Hours**

INSTRUCTIONS TO CANDIDATES: This paper has 7 pages and 5 questions

Attempt ALL questions.
Each question is worth 20 marks.
Maximum 100 marks.

This exam contributes 50% of the final course grade.
You must pass this exam in order to pass the course.

The following reference information is provided for Q3.b

- **Function Information – C18 library - page 6.**
- **Electrical Information – PIC18F452 - page 6.**
- **Electrical Information – 3951 motor driver - page 7.**

The graph paper on page 5 should be used to answer Q4.b. Please detach the page from this exam paper, write your ID number at the top of the page, and attach the page to your exam booklet at the end of the exam.

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Case Information for use in Q1.a, Q3, Q4, and Q5

An embedded motor controller must meet the following requirements:

- three tasks A,B,C, must run while sharing global resources R and P:
  - Task C is responsible for updating the command to the motor outputs
  - Task B is responsible for sampling the input signal.
  - Task A is responsible for executing a motor control algorithm based on a Finite State Machine.
- jobs should be scheduled using a pre-emptive priority-based scheduling algorithm
- global resources (R and P) are protected using mutexes (one per resource):
  - all acquisition attempts should time-out after 5ms
  - mutexes should employ a priority inheritance protocol
- inter-task messaging facilities:
  - attempt to send/recieve messages in a non-blocking manner
  - have a maximum message queue length of 4
  - discard **old** messages on overflow

Task Name	Parameters (ϕ, p, e, D) (units: milliseconds)	Resources Used	Operation and Estimated Times
A	(0, - , 8, 60)	R, P	job released on message receipt if message from Task B (1 ms) lock P with timeout (1-5 ms) if P locked (1 ms) lock R with timeout (1-5 ms) if R locked (1 ms) trigger FSM w/ALL TaskB msgs (1 ms) release R (1 ms) release P (1 ms) else if message from Task C (1 ms) remove message from queue (1 ms) resume Task C (1 ms) else (1 ms) clear ALL messages (1 ms)
B	(0, 15, 5, 15)	P	job released periodically lock P with timeout (1-5 ms) if P locked (1 ms) sample signal (1 ms) release P (1 ms) send message to Task A (1 ms)
C	(0, 120, 5, 60)	R	job released periodically iff task not suspended do lock R with timeout (1-5 ms) if R not locked (1 ms) send message to Task A (1 ms) suspend task C (1 ms) while R not locked (1 ms) update motor current command (1 ms) release R (1 ms)

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Q1. Both mutexes and message queues can be used for **inter-task communication**.

(a) Compare and contrast the use of mutexes and message queues as described on page 2. *6 marks*

(b) i. Under what circumstances does the use of mutexes cause deadlock in pre-emptive priority-based systems? *4 marks*

ii. How does the Original Ceiling priority inheritance protocol "correct" priority inversion? *4 marks*

(c) Describe how each of the three features (mutexes, message queues, and priority inheritance protocols) could be used/implemented using the μCOS-II kernel. *6 marks*

Q2. Kernels are used to facilitate **task management**.

(a) i. Draw a diagram to illustrate task states, and the functions that cause tasks to change state under a typical kernel. *4 marks*

ii. Highlight/annotate areas of your diagram to indicate functions specific to real-time (as opposed to general purpose) kernel functions. *4 marks*

(b) Differentiate between task scheduling, and context switching. *6 marks*

(c) Describe the role of the Task Control Block structure within the task scheduling and context switching functions of the μCOS-II kernel. *6 marks*

Q3. The platform used with a kernel should possess certain **hardware features**.

(a) If the μCOS-II kernel is used for the motor controller (as described on page 2), it would require a platform processor had both, a user-addressable stack and hardware timer interrupts. Explain why this is so. *4 marks*

(b) Task C (as described on page 2) is responsible for updating and sending an appropriate command to the motor interface circuitry to control motor current. The DC motor to be controlled is rated at 9V, 0.37Amps, 6420 rpm.

i. Design a hardware interface to allow the PIC18F452 to perform analogue control of DC motor current, using the PWM peripheral output CCP1, and the 3951 Full-Bridge Motor Driver. *8 marks*

ii. Describe, and create, appropriate software interface routines for the interface designed in Q3(b)i using the C programming language, or C-like pseudo-code. You may presume appropriate μCOS-II kernel and C18 compiler library functions are available. *8 marks*

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Q4. System behavior can be predicted using standard **performance metrics and tools**. For the motor controller(as described on page 2):

(a) i. Calculate the hyper-period of the system *1 mark*

ii. Calculate the system utilization *2 marks*

iii. Identify the job parameters $J_{Q,n} : e_{Q,n}(r_{Q,n}, d_{Q,n}]$ for all job instances n belonging to individual tasks during the hyper-period. *4 marks*

iv. Draw the job precedence graph - use this graph to explain how you would determine effective deadlines and release times. *3 marks*

(b) Using the Graph Paper on page 5, draw the task timelines where: *4 marks*

- Job priorities are determined using pre-emptive Least Slack Time scheduling,
- Original Ceiling Priority inheritance protocol is in effect, and
- Job execution times are adjusted based on branch executed, and time spent acquiring mutexes

(c) Critically assess motor controller performance based on these analyses. Your answer should make reference to, and make observations about, results from Q4.a, and Q4.b. *6 marks*

Q5. Performance analysis presumes, and system testing ensures, that all **timing** requirements are met, and that **resources** are not exhausted.

(a) For each of the following items, identify ONE feature which could influence either timing resolution, precision, or accuracy, and explain how it affects timing:

i. Least Slack Time scheduling algorithm *2 marks*

ii. C programming language *2 marks*

iii. MCC18 build tools for PIC18F452 (including linker, libraries, and compiler) *2 marks*

(b) Task A implements a motor control algorithm using a Finite State Machine.

i. Identify and explain two strategies for implementing an FSM using the C language. *4 marks*

ii. Contrast strategies from Q5(b)i, in terms of their resource requirements, and impacts on timing. *4 marks*

(c) You are the leader of an engineering team responsible for developing a motor controller(as described on page 2). Your team has completed the design, but has not yet done any system-wide time and resource-based tests.

The general manager is convinced that system testing is not needed, as your team ran extensive performance analyses on the initial design, and each interface has been individually tested. He has threatened to withhold Christmas bonuses from all team members, unless the product is immediately cleared for production.

What would you say to the general manager, and to the team members who feel cheated out of their bonus? *6 marks*

END OF QUESTIONS

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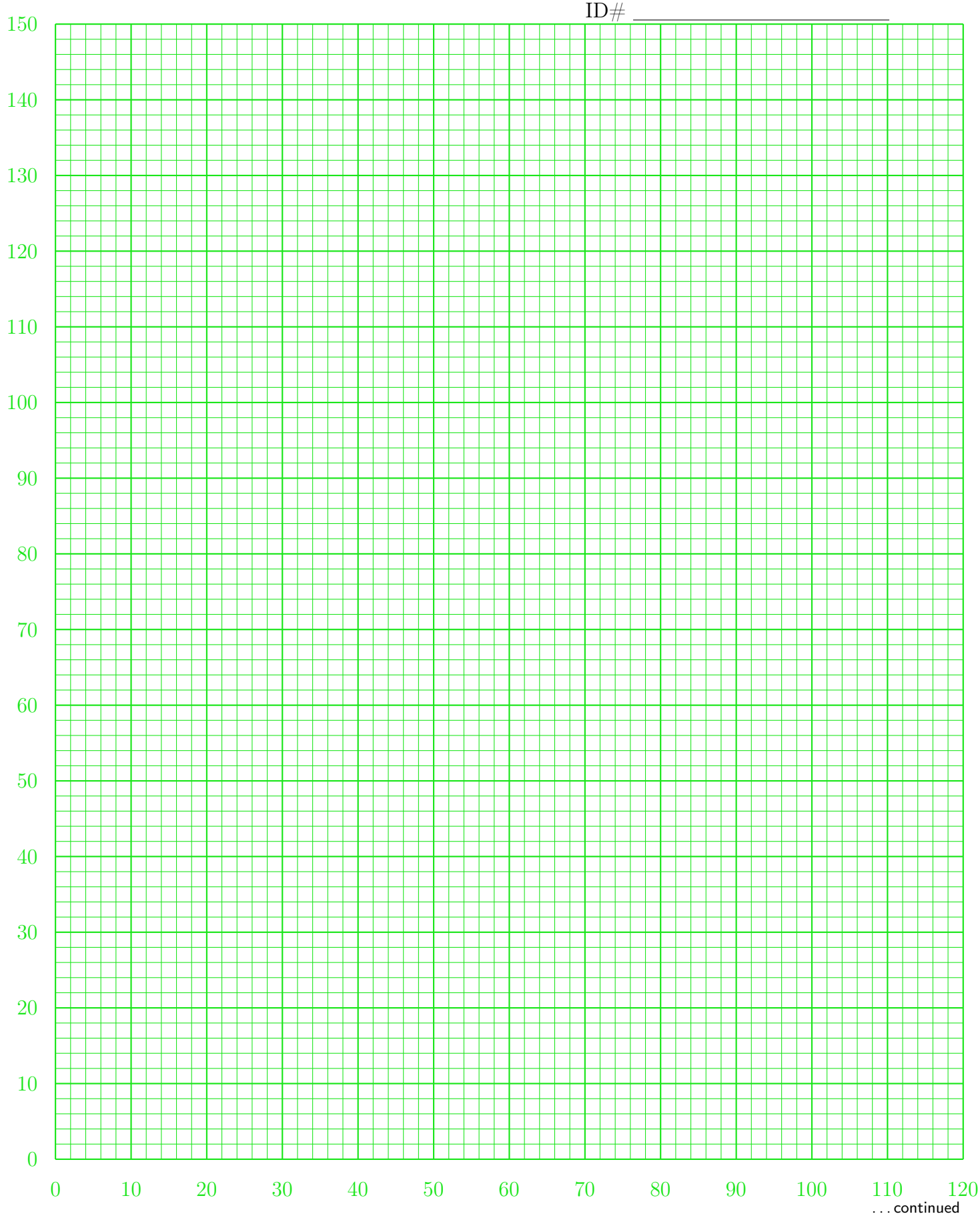

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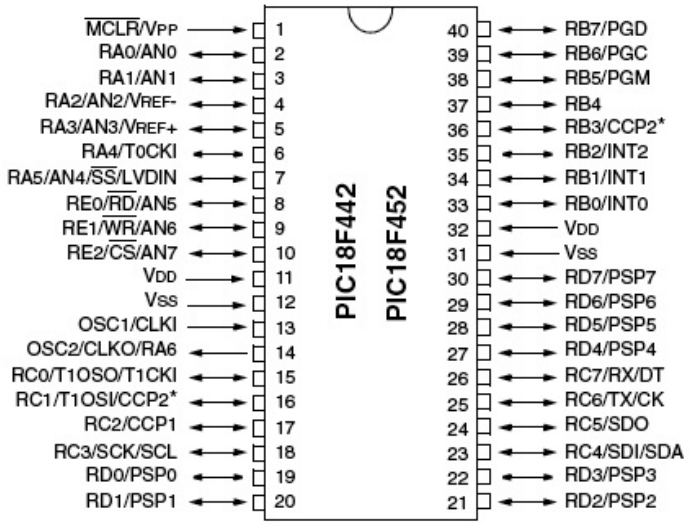
C18 Library functions for PWM peripheral and Timers.

`void ClosePWMx(void)`	Disable PWM channel x.
`void OpenPWMx (char period)`	Configure PWM channel x with given period
`void SetDCPWMx(unsigned int d)`	Write a new duty cycle value to PWM channel x.
`void CloseTimerx(void)`	Disable timer x.
`void OpenTimerx( unsigned char cfg )`	Configure and enable timer x.
`unsigned int ReadTimerx (void)`	Read the value of timer x.
`void WriteTimerx (unsigned int t)`	Write a value into timer x.

PIC18F452 description



Output Pin Load resistance	R_L	464Ω
Output Pin Load capacitance	C_L	50 pF
Input Pin capacitance	C_{in}	5 pF
Max. Port output rise/fall time	T_{io}	40ns
Max. Delay port output	$T_{os}H2_{io}$	255ns
Min. Input Hold time	$T_{os}H2_{io}I$	100 ns
Max. current sunk/sourced by output (ignoring totals)		20mA
Max. input leakage current	I_{IL}	$\pm 1\mu$A
Output Low Voltage	V_{OL}	0.6V
Output High Voltage	V_{OH}	$V_{DD} - 0.7$ Volts
Max. Input Low Voltage (TTL)	V_{IL}	$0.15V_{DD}$ Volts
Min. Input High Voltage (TTL)	V_{IH}	$0.25V_{DD} + 0.8$ Volts
Max. Input Low Voltage (ST)	V_{IL}	$0.2V_{DD}$ Volts
Min. Input High Voltage (ST)	V_{IH}	$0.8V_{DD}$ Volts

All voltages must lie between V_{dd} and V_{ss}. All ratings taken at 25°. Pins on ports C,D and E are normally Schmitt Trigger inputs, push-pull outputs. Port A pin 4 is a Schmitt Trigger input, open-drain output. All other pins are normally TTL level inputs, push-pull outputs. Input circuitry on some pins changes depending on the pin function selected.

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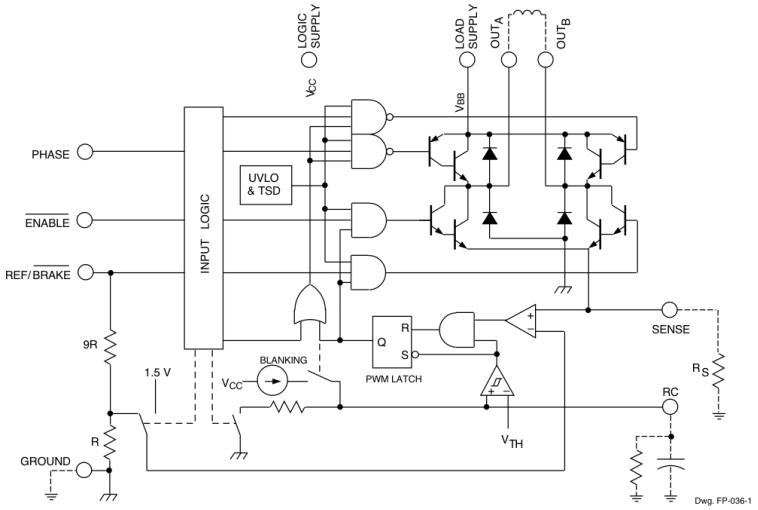
Information for 3951 motor controller



BRAKE	ENABLE	PHASE	OUT$_A$	OUT$_B$	DESCRIPTION
H	H	X	Z	Z	Outputs Disabled
H	L	H	H	L	Forward
H	L	L	L	H	Reverse
L	X	X	L	L	Brake, See Note

X = Irrelevant Z = High Impedance (source and sink both OFF)

LOAD CURRENT REGULATION WITH EXTERNAL PWM OF THE PHASE INPUT

The PHASE input can be pulse-width modulated to regulate load current. Typical propagation delays from the PHASE inputs to transitions of the power outputs are specified in the electrical characteristics table. Toggling the PHASE terminal determines/controls which sink/source pair is enabled, producing a load current that varies with the duty cycle and remains continuous at all times. If the internal current-control circuitry is not used; the REF terminal should be connected to VCC, the SENSE terminal should be connected to ground, and the RC terminal should be left floating (no connection).

ELECTRICAL CHARACTERISTICS	Symbol	Min.	Typ.	Max.	Units
Load Supply Voltage Range	V_{BB}	V_{CC}	–	50	V
Load Supply Current	$I_{BB(ON)}$	–	2.9	6.0	mA
(No Load)	$I_{BB(OFF)}$	–	3.1	6.5	mA
	$I_{BB(BRAKE)}$	–	3.1	6.5	mA
Logic Supply Voltage Range	V_{CC}	4.5	5.0	5.5	V
Logic Input Voltage	$V_{IN(1)}$	2.0	–	–	V
	$V_{IN(0)}$	–	–	0.8	V
Logic Input Current	$I_{IN(1)}$	–	<1.0	20	μA
	$I_{IN(0)}$	–	<-2.0	-200	μA
Propagation Delay Time	t_{pd}				
PHASE Change to Source ON		–	2.9	–	μs
PHASE Change to Source OFF		–	0.7	–	μs
PHASE Change to Sink ON		–	2.4	–	μs
PHASE Change to Sink OFF		–	0.7	–	μs
Logic Supply Current	$I_{CC(ON)}$	–	20	30	mA
(No Load)	$I_{CC(OFF)}$	–	12	18	mA
	$I_{CC(BRAKE)}$	–	26	40	mA

END OF QUESTION PAPER