JFK-10

THE UNIVERSITY OF THE WEST INDIES
ST. AUGUSTINE

EXAMINATIONS OF DECEMBER 2012

Code and Name of Course: **ECNG3006 Microprocessor Systems: Design and Appl'n**

Date and Time: FRIDAY 14 DECEMBER 2012 @ 9 AM Duration: **Three hours**

INSTRUCTIONS TO CANDIDATES: This paper has 6 pages and 4 questions. Max. Marks: **100**

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Attempt ALL questions.
Questions 1-3 are each worth 20 marks.
Question 4 is worth 40 marks.

This exam contributes 50% of the final course grade.
You must pass this exam in order to pass the course.

The following reference information is provided:

- I2C Timing Diagrams
- Case Study

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Q1. Kernels are used to facilitate **task management**.

(a) Abstract models can be used to describe kernel **structure**, **workload**, **resources**, and task management **algorithms**. State parameters that define **each** model. *4 marks*

(b) Will a context-switch based kernel **always** provide better response-time performance than a foreground-background system? Justify your response and identify at least one other reason why a context-switch based kernel might be preferred. *6 marks*

(c) Draw a diagram to illustrate task states and the functions that cause tasks to change state under a typical context-switch based kernel. *4 marks*

(d) Identify, and assess the validity of, **one** guideline that appears in the MISRA C/C++ standards which may impact the implementation of a kernel. Your answer should examine the assumptions underlying the guideline/feature, and refer to a specific kernel. *6 marks*

Q2. The application platform used should possess certain **hardware features**.

(a) Processor X does not support interrupts. Should it be used to develop a solutions for a real-time application? Support your answer by referring to the needs of realtime applications, and the different roles that interrupts may play in real-time applications. *6 marks*

(b) Identify, and briefly describe the operation of **two** assembly-language instructions of the PIC18 that facilitate use of context switch based kernels. *4 marks*

(c) Explain how direct interfacing can be used to "read" an impedance-based sensor connected to the PIC18. Your answer should identify the information about the sensor and/or PIC18 that is required. *4 marks*

(d) A system must sample a 32-bit reading, at 100 milli-second intervals for up to 2 hours. Readings should be stored on a 4Mbit I2C EEPROM. The EEPROM operates with I2C clock frequency of 100 kHz, and supports both single byte and 128-byte page write operations.Develop an appropriate storage strategy. Show reasoning. *6 marks*

Refer to Q3 on Pg3

Q3. System behavior can be predicted, monitored and analyzed using standard **performance metrics, analytical methods, techniques, and tools.**

(a) Are traceability table(s) more **effectively** used as tools to:

- debug programs following the detection of run-time errors? OR
- identify, control, and track requirements changes?

You should support your answer with examples from project implementation(s). *6 marks*

(b) Describe the concept of the **idle task**, and explain technique(s) by which the kernel may use the idle task to track actual **system utilization**. *4 marks*

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FIGURE 6-1: BYTE WRITE

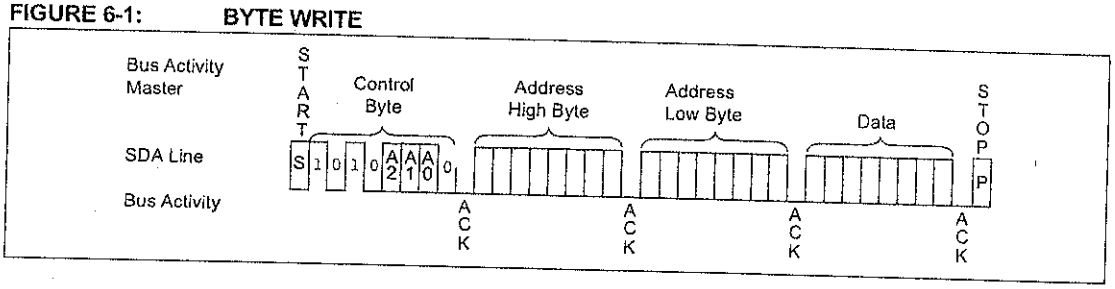

FIGURE 6-2: PAGE WRITE

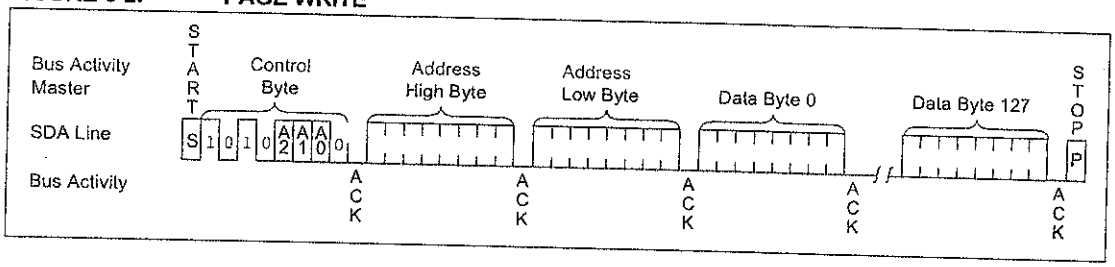

Figure Q2.d: Timing diagrams for I2C Byte and Page write operations

(c) Four periodic tasks have execution times of 1, 2, 2 and 1 respectively. The tasks have periods of 10, 15, 30 and 15 respectively. Pre-emptive EDF scheduling is utilised, where Task D is dependent on outputs of Tasks A and B, and Tasks A and C share a resource.

i. Complete the precedence graph (on page 6), and determine the effective release times, and deadlines, for jobs representing the first iteration of each task.

4 marks

ii. Construct a timeline for the system, using the grid (on page 6), and indicate all instances where tasks have been pre-empted, or kept waiting. State any assumptions.

6 marks

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Q4. For the **Case Study**[1] shown in Figure Q3:

(a) Select, and justify your choice of, appropriate inter-task communication mechanisms for

i. managing access to the samples used by all three tasks, *4 marks*

ii. preventing **Calculate** and **Acquire** tasks from running while the other is active *4 marks*

(b) "Interrupt overload is not necessarily caused by high interrupt loads but rather by unexpectedly high interrupt loads." Explain this statement in the context of RS232 interrupts being used for communication between the system, the stepper motor controller, and the Torque measurement controller. *6 marks*

(c) Determine the minimum resolution of the D/A converter to be used for i_{ph}, and the error associated with attempting to output 3A at that resolution. Explain your reasoning. *4 marks*

(d) An engineer is having difficulty choosing between two methods of implementing the Acquire task in C, and wishes to flip a coin to decide between:

- a series of nested loops
- an FSM based switch-case implementation

What opinion/advice would **you** offer to the engineer? *10 marks*

(e) Run-time and Jitter for the **Acquire** task can be measured. How will running **Acquire** as one task on a multitasking system vs. alone on bare hardware affect these values? *6 marks*

(f) Based on the preceding analyses, critically assess system design suitability. Your answer should identify potential system hazards, and consider whether a preemptive priority based scheduler is suitable for the application. *6 marks*

END OF QUESTIONS

[1]Based on Rasmussen, Peter Omand; Andersen, Gert Karmisholt; Helle, Lars; Pedersen, John Kim; Blaabjerg, Frede / Fully Automatic Characterization System for Switched Reluctance Motors. In: Proceedings of International Conference on Electrical Machines, ICEM'98, Istanbul, Turkey, Sept. 1998. Faculty of Engineering : Middel East Technical University, 1998. `http://www.dee.hcmut.edu.vn/vn/bomon/bmthietbi/dongco_tutro/srm/35.pdf`

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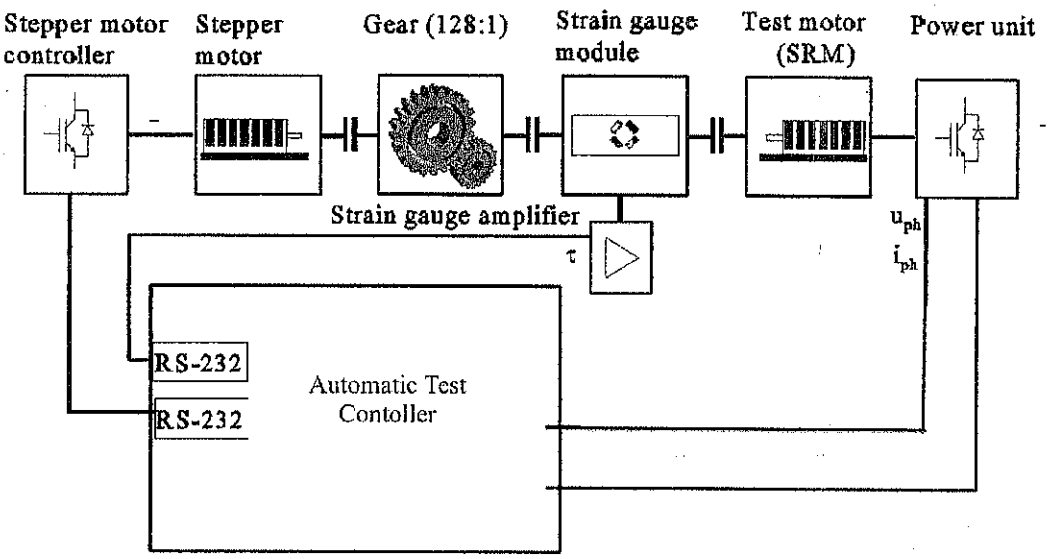

Figure Q4 Block diagram for SRM Automatic Characterization System

An automatic test system for the characterization of Switched Reluctance Motors (SRM) uses a pre-emptive priority-based scheduler for three tasks:

T_1 **Display** - which plots current results as a graph on a GUI

T_2 **Calculate** - which determines the torque characteristic **after** all readings have been acquired

T_3 **Acquire** - which operates when the system starts, and not if the Calculate task is active

- For rotor angles between 0 and 180 degrees in 1 degree steps

  J_{31} Turn/lock SRM rotor position using stepper motor (send 1 byte @1200baud 8N1, step resolution 1.8 mechanical degrees)

  * For fixed voltage u_{ph} and dc current i_{ph} between 0 and 15A in 1.5A increments

  J_{32} Set appropriate dc current i_{ph} on a single motor phase (D/A output)

  J_{33} Wait for torque reading to settle (send 1 byte - receive 1 byte @9600 baud 8N1 at 1s intervals max. 4 s)

  J_{34} Record 32-bit torque reading (after settling send 1 byte - recieve 4 bytes @9600 baud 8N1)

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Figure 3(c)i Precedence graph for Job set $J_1 ... J_4$

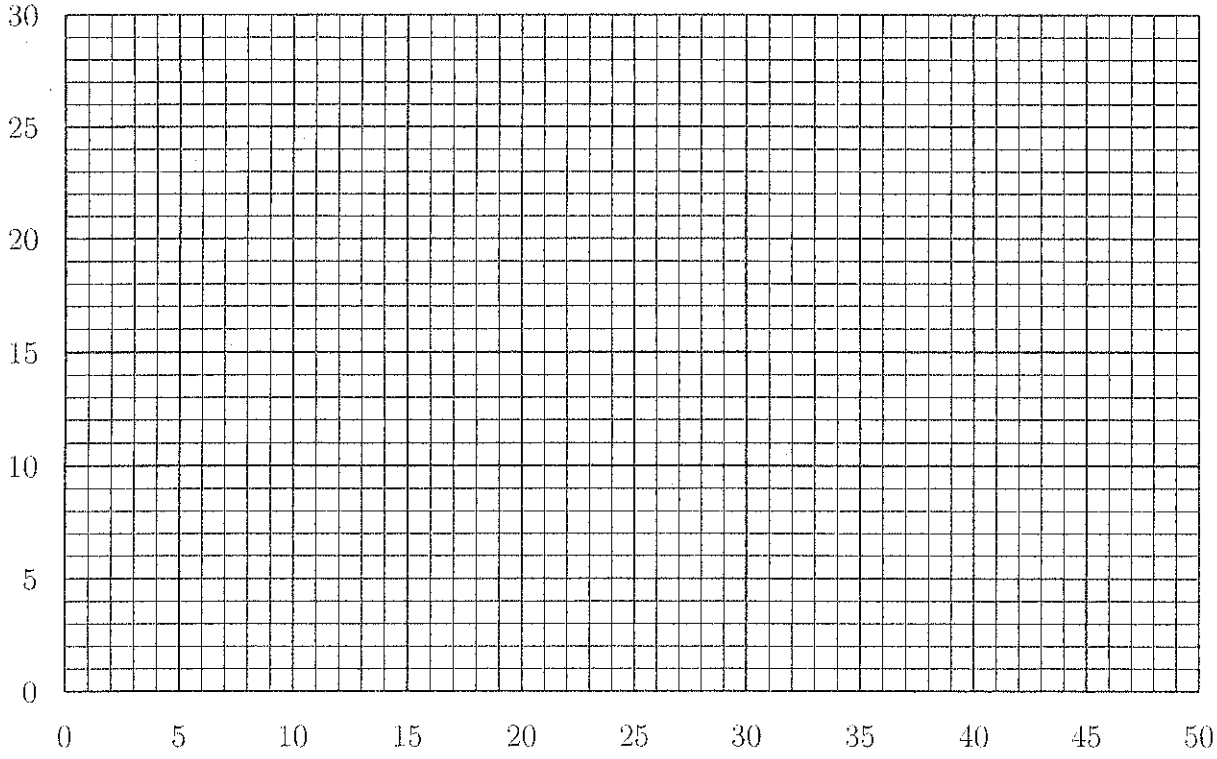

Figure 3(c)ii Grid for Timeline for Job set $J_1 ... J_4$