THE UNIVERSITY OF THE WEST INDIES
ST. AUGUSTINE

EXAMINATIONS OF DECEMBER 2013

Code and Name of Course: **ECNG3006 Microprocessor Systems: Design and Appl'n**

Date and Time: Duration: **Three hours**

INSTRUCTIONS TO CANDIDATES: This paper has 7 pages and 3 questions. Max. Marks: **100**

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Attempt ALL questions.
Questions 1-2 are each worth 25 marks.
Question 3 is worth 50 marks.

This exam contributes 50% of the final course grade.

Questions Q3.a and Q3.b should be answered on pages 6-7
and the script returned with your exam booklet.

The following reference information is provided:

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Q1. μCOS-II is an example of a real-time operating system (RTOS) kernel which supports multi-tasking.

(a) Differentiate between task scheduling, and context switching. *5 marks*

(b) Describe the concept of the **idle task**, and explain it's role in allowing the kernel to track actual **system utilization**. *5 marks*

(c) Describe the role of the Task Control Block structure within the task scheduling and context switching functions of the μCOS-II kernel. *5 marks*

(d) Identify **one** task-management function that is supported by μCOS-II, and appears in an RTOS-related standard. Your answer should name the standard, and examine the rationale for including the task management function in the standard. *5 marks*

(e) *"Multi-tasking provides better average task performance (reduced response-time) than cyclic executives."*

Discuss the validity of the statement. If **true**, why do embedded system designers sometimes prefer cyclic executives? If **false**, why do embedded system designers sometimes prefer multi-tasking solutions? *5 marks*

Q2. Figure Q2 describes an ultrasonic receiver in an automotive system which alerts driver when they are too close to an object. It consists of analogue signal acquisition circuitry, an A-D converter, and digital algorithms implemented on a microprocessor.

(a) Use the equation and values provided to quantify the effect of the amplifier parameters on the the **effective** number of bits available from the A-D converter. *5 marks*

(b) Illustrate **two** strategies for implementing a finite state machine (FSM) using C-like pseudo-code. Contrast your chosen strategies for a system with only two states. *5 marks*

(c) Describe one technique for determining an **appropriate** stack size for the task which implements the digital filter. Is your chosen technique more likely to under-size or over-size the task stack? *5 marks*

(d) Explain the rationale for performing initialisation tests each time a system starts. Support your answer by recommending a test for the receiver system. *5 marks*

(e) *"The PIC16F877 micro-controller is unsuited for real-time systems".*

Discuss the validity of the statement. Support your answer by considering whether the PIC16F877 can be used for the system described in Figure Q2. *5 marks*

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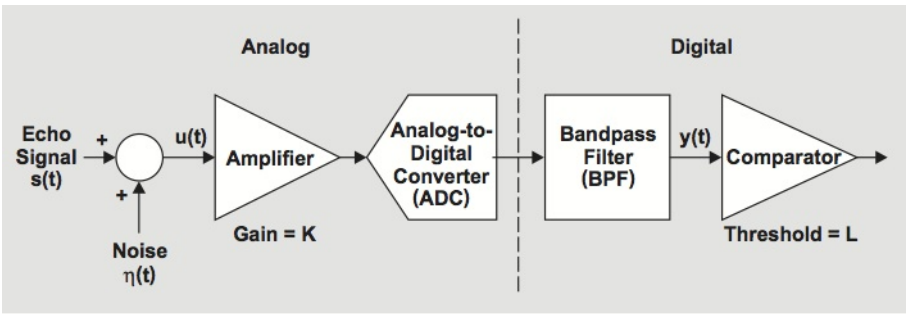
Figure Q2 Extract from Analog Applications Journal 3Q 2012
"Using a fixed threshold in ultrasonic distance-ranging automotive applications" by Arun T. Vemuri

"The echo signal, $s(t)$, received by the ultrasonic receiver is corrupted with noise. The input-referred noise, $h(t)$, ...is the sum of noise from the external environment and all signal-chain components as a function of time (t). This corrupted signal, $u(t)$, is amplified by an amplifier with gain, K, and is digitized with an analog-to-digital converter (ADC). The digitized AM signal is routed through a bandpass filter (BPF), which is primarily used to improve the signals signal-to-noise ratio. The filtered signal, $y(t)$, is compared against a threshold, L, to detect the presence of an object."



Speed of sound: 340m/s
A/D Converter Resolution: 10 bits
Configurable Amplifier Gains, K=10
Amplifier Gain Bandwidth: 1MHz
Ultrasonic Signal Carrier Frequency, f: 40 kHz

Maximal frequency constraint for observed error ε:

$$f < f_a \frac{\sqrt{2\varepsilon}}{1-\varepsilon} \tag{1}$$

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Q3. An Automotive Electronic Throttle Control System is an example of an embedded system with real time requirements. Jobs and tasks for such a system are described on page 5.

(a) i. Fill in the missing job parameters and precedence arrows on the precedence graph on page 6. *5 marks*

ii. Use the precedence graph on page 6 to determine the effective release times and deadlines for jobs J23 and J33. Show your reasoning. *5 marks*

iii. Use the graph paper on page 7 to construct a **cyclic schedule** for the execution of these jobs where the minor cycle is 10ms. *5 marks*

(b) Use the graph paper on page 7 to construct appropriate **task and resource timelines** for the execution of these jobs presuming that they are scheduled using a pre-emptive priority based scheduler, with a 10ms tick, where Task 3 has the highest priority, and Task 1 has the lowest priority. *10 marks*

(c) Compare the task performance achieved using the cyclic executive, and the pre-emptive priority based scheduler. Your answer should clearly identify at least **two** criteria you could use for comparison, and explain which system you would prefer to implement and what adjustments (if any) you would make. *10 marks*

(d) In order to reduce system costs, you have been asked to implement the cyclic schedule using a processor which can support a minimum clock tick of 20ms, and an in-house kernel that supports mutexes but not semaphores.

Assess whether the suggested scheme is feasible. Your answer should identify all resources and procedures you would require to detect and/or address any subsequent issues. *15 marks*

END OF QUESTIONS

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Figure Q3 Description of Electronic Throttle Control System controller

System Inputs:	• Accelerator Pedal Sensor, • Throttle Position Sensor
System Outputs:	• Throttle Motor Signal, • Throttle Clutch Signal
System Resources:	**R1** Semaphore - maximum count 1
Task 1: Throttle Clutch Control	connects/disconnects the clutch upon receiving the appropriate semaphore from Task 2; runs at 100 ms intervals but must finish within 50ms of being released. **J11, e=10ms** upon receiving semaphore R1, toggle clutch
Task 2: Throttle Motor Control	updates the PWM duty cycle and period and releases clutch semaphores at 100 ms intervals. **J21, e=10ms** retrieve most recent readings **J22, e=20ms** after J21, perform update calculations **J23, e=5ms** after J22, output new PWM values; if needed release semaphore R1 for clutch
Task 3: Sensing	reads the Throttle and Accelerator Pedal sensors at 100ms intervals. **J31, e=5ms** read Accelerator Sensor **J32, e=5ms** read Throttle sensor; released 20 ms after J31 due to shared hardware **J33, e=10ms** after J31 and J32, update stored readings

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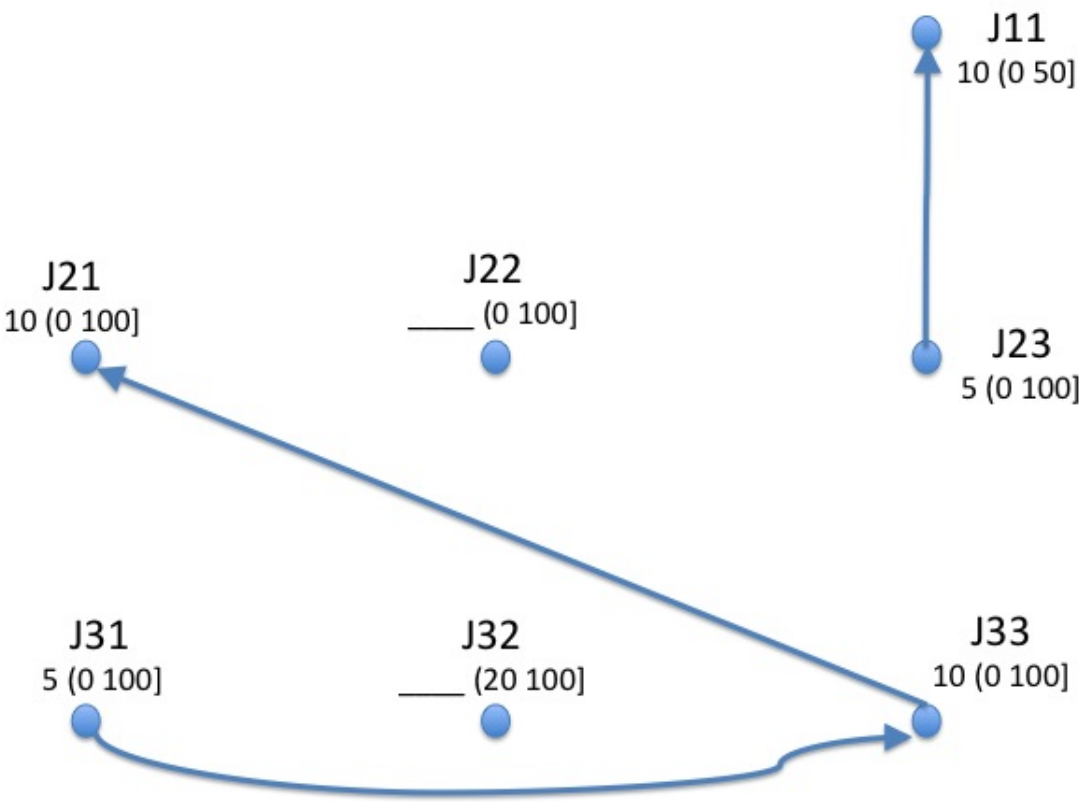

Figure Q3.a Precedence graph for Job set $J11...J33$

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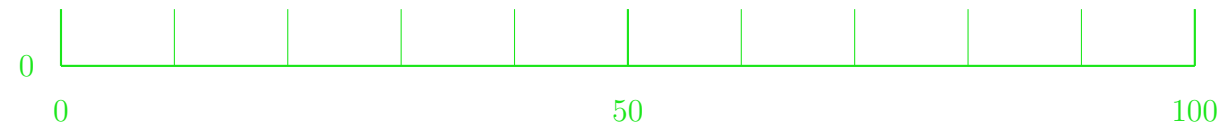

Figure Q3(a)iii Grid for Cyclic Schedule for Job set $J11...J33$

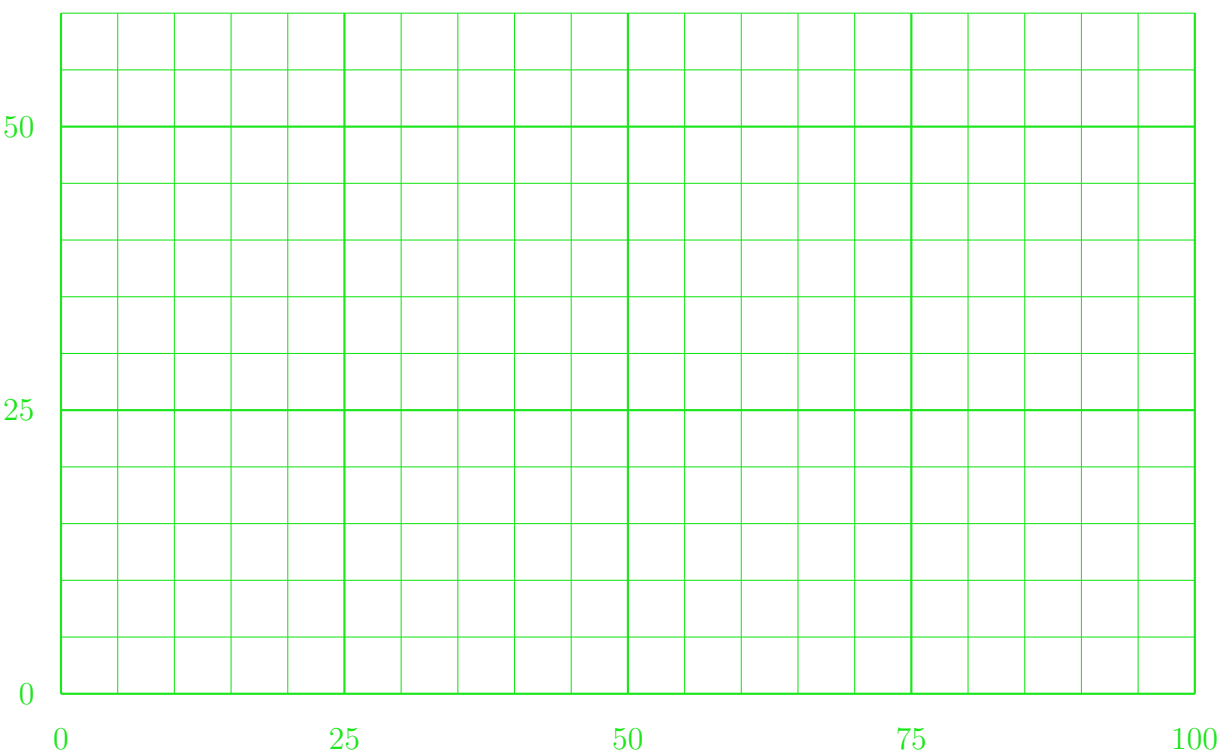

Figure Q3.b Grid for EDF Timeline(s) for Job set $J11...J33$

END OF EXAM PAPER