THE UNIVERSITY OF THE WEST INDIES
ST. AUGUSTINE

EXAMINATIONS OF December 2014

Code and Name of Course: **ECNG3006 Microprocessor Systems** Paper: **Final**

Date and Time: Duration: **Three (3) hours**

INSTRUCTIONS TO CANDIDATES: This paper has 7 pages and 3 questions. Max. Marks: **100**

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Attempt ALL questions.
Questions 1-2 are each worth 25 marks.
Question 3 is worth 50 marks.

Questions Q3.a and Q3.b should be answered on pages 6-7
and the script returned with your exam booklet.

The following reference information is provided:

- Description of Ultrasonic Receiver on page 3
- Task Information for Process Control System on page 5

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Q1. μCOS-II is an example of a commercial real-time operating system (RTOS) kernel which supports multi-tasking, and pre-emptive priority based systems.

(a) Do real-time application developers necessarily benefit from using a commercial RTOS? Support your answer by identifying at least **two** reasons why developers choose to use or not use commercial RTOS. *5 marks*

(b) Differentiate between the roles of the kernel and the scheduler within μCOS-II; which is more important? *5 marks*

(c) μCOS-II is used to create a periodic task A ($p_A = 10$) and a sporadic task B, where Task B has higher priority than Task A. Determine the maximum response time of Task A in terms of the nominal task execution times (e_A=5 , e_B=1) given that the minimum inter-arrival time of Task B is 3 time units. Explain your reasoning. *5 marks*

(d) Explain how the μCOS-II task stack is manipulated during a context switch. Your response should differentiate between the processor stack, the C Run-time stack, and the task stack. *5 marks*

(e) μCOS-II is 99% compliant with the Motor Industry Software Reliability Association (MISRA-C:1998) C Coding Standards. One of the rules μCOS-II violates is MISRA-C Rule 15.2 which states that "an unconditional break statement shall terminate every non-empty switch clause".

i. Use a fragment of C-code to illustrate a violation of MISRA-C Rule 15.2. *2 marks*

ii. Violation of MISRA-C rules does not always lead to increased observation of embedded system malfunction. Explain why this is so, using a historical example of embedded system failure to support your answer. *3 marks*

Q2. Figure Q2 describes an algorithm for the use of an ultrasonic receiver in an automotive system which alerts driver when they are too close to an object. It consists of analogue signal acquisition circuitry, an A-D converter, and a digital filtering algorithm described using a finite state machine, and implemented in a single task.

(a) Use the equation and values provided to quantify the effect of the amplifier parameters on the the **effective** number of bits available from the A-D converter. *5 marks*

(b) Illustrate **two** strategies for implementing a finite state machine (FSM) using C-like pseudo-code. Contrast your chosen strategies for a system with only two states. *5 marks*

(c) Describe one technique for determining an **appropriate** stack size for the task which implements the digital filter. Is your chosen technique more likely to undersize or over-size the task stack? *5 marks*

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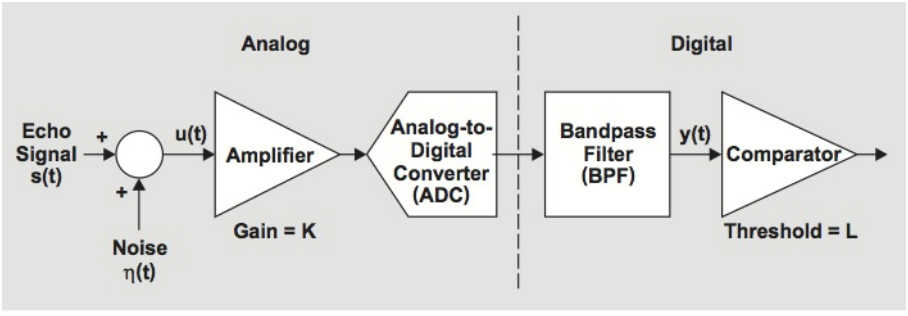
Figure Q2 Extract from Analog Applications Journal 3Q 2012
"Using a fixed threshold in ultrasonic distance-ranging automotive applications" by Arun T. Vemuri

"The echo signal, $s(t)$, received by the ultrasonic receiver is corrupted with noise. The input-referred noise, $h(t)$, ...is the sum of noise from the external environment and all signal-chain components as a function of time (t). This corrupted signal, $u(t)$, is amplified by an amplifier with gain, K, and is digitized with an analog-to-digital converter (ADC). The digitized AM signal is routed through a bandpass filter (BPF), which is primarily used to improve the signals signal-to-noise ratio. The filtered signal, $y(t)$, is compared against a threshold, L, to detect the presence of an object."



Speed of sound: 340m/s
A/D Converter Resolution: 10 bits
Configurable Amplifier Gains, K=10
Amplifier Gain Bandwidth: 1MHz
Ultrasonic Signal Carrier Frequency, f: 40 kHz

Maximal frequency constraint for observed error ε:

$$f < f_a \frac{\sqrt{2\varepsilon}}{1-\varepsilon} \tag{1}$$

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(d) Using a sample C-like code, identify the key function calls in the C18 libraries for accessing the A/D converter on the PIC18F452. Your answer(s) do not need to be syntactically correct. *5 marks*

(e) Identify two or more concerns associated with the use of interrupts in critical systems, where failures may endanger life. Where interrupt use is required in a critical system, how can these concerns be addressed ? *5 marks*

Q3. A Process Control System is an example of an embedded system with real time requirements. Jobs and tasks for such a system are described on page 5.

(a) i. Fill in the missing job parameters and precedence arrows on the precedence graph on page 6. *5 marks*

ii. Use the precedence graph on page 6 to determine the effective release times and deadlines for jobs J22 and J32. Show your reasoning. *5 marks*

iii. Use the graph paper on page 7 to construct a **cyclic schedule** for the execution of these jobs where the minor cycle is 10ms. *5 marks*

(b) Use the graph paper on page 7 to construct appropriate **task and resource timelines** for the execution of these jobs presuming that they are scheduled using a pre-emptive priority based scheduler, with a 10ms tick, where Task 3 has the highest priority, and Task 1 has the lowest priority. *10 marks*

(c) Compare the task performance achieved using the cyclic executive, and the pre-emptive priority based scheduler. Your answer should clearly identify at least **two** criteria you could use for comparison, and explain which system you would prefer to implement and what adjustments (if any) you would make. *10 marks*

(d) In order to reduce system costs, you have been asked to implement the pre-emptive priority based system using a processor with limited stack space; thus all task variables are static, and communication is achieved through the use of shared global variables.

Assess whether the suggested scheme is feasible. Your answer should identify all resources and procedures you would require to detect and/or address any subsequent issues. *15 marks*

END OF QUESTIONS

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Figure Q3 Description of Process Control System based on Presentation on Selective Catalytic reduction by Kyle Hunte, November 2014

Selective Cataytic Reduction is a process by which exhaust containing nitrous oxides (dangerous emissions) is reacted with ammonia to form nitrogen and water(safe to emit). In this process ammonia is pumped from feed tanks, heated, and combined with exhaust.

System Inputs:	• Ammonia Tank Level Sensor • Temperature Sensor
System Outputs:	• Pump (On/Off) • Heater (On/Off)
System Resources:	**R1** Semaphore - maximum count 1 **R2** Semaphore - maximum count 1
Task 1: Ammonia Tank Level Monitoring	Sends signal to Pump Control Task; Runs at 50 ms intervals. **J11, e=5ms** read and store current Tank level reading **J12, e=5ms** after J11, if level low then release semaphore R1 else release semaphore R2
Task 2: Pump Control	Toggles state of pump at 100% based on semaphore received; deadline 30 ms after semaphore release. **J21, e=10ms** on receiving R1, turn pump on **J22, e=10ms** on receiving R2, turn pump off
Task 3: Temperature Control	Reads the Temperature Sensor, filters data, and turns the Heater on and off appropriately. Runs at 100 ms intervals, but the heater must be triggered within 50ms of the temperature reading. **J31, e=10ms** read and store Current Temperature and filter Reading (average current and stored readings) **J32, e=5 or 10ms** after J31, if Reading is $> T_{upper}$ then release J34; else if temperature is $< T_{lower}$ then release J33 **J33, e=5ms** after J32, turn on Heater **J34, e=5ms** after J32, turn off Heater

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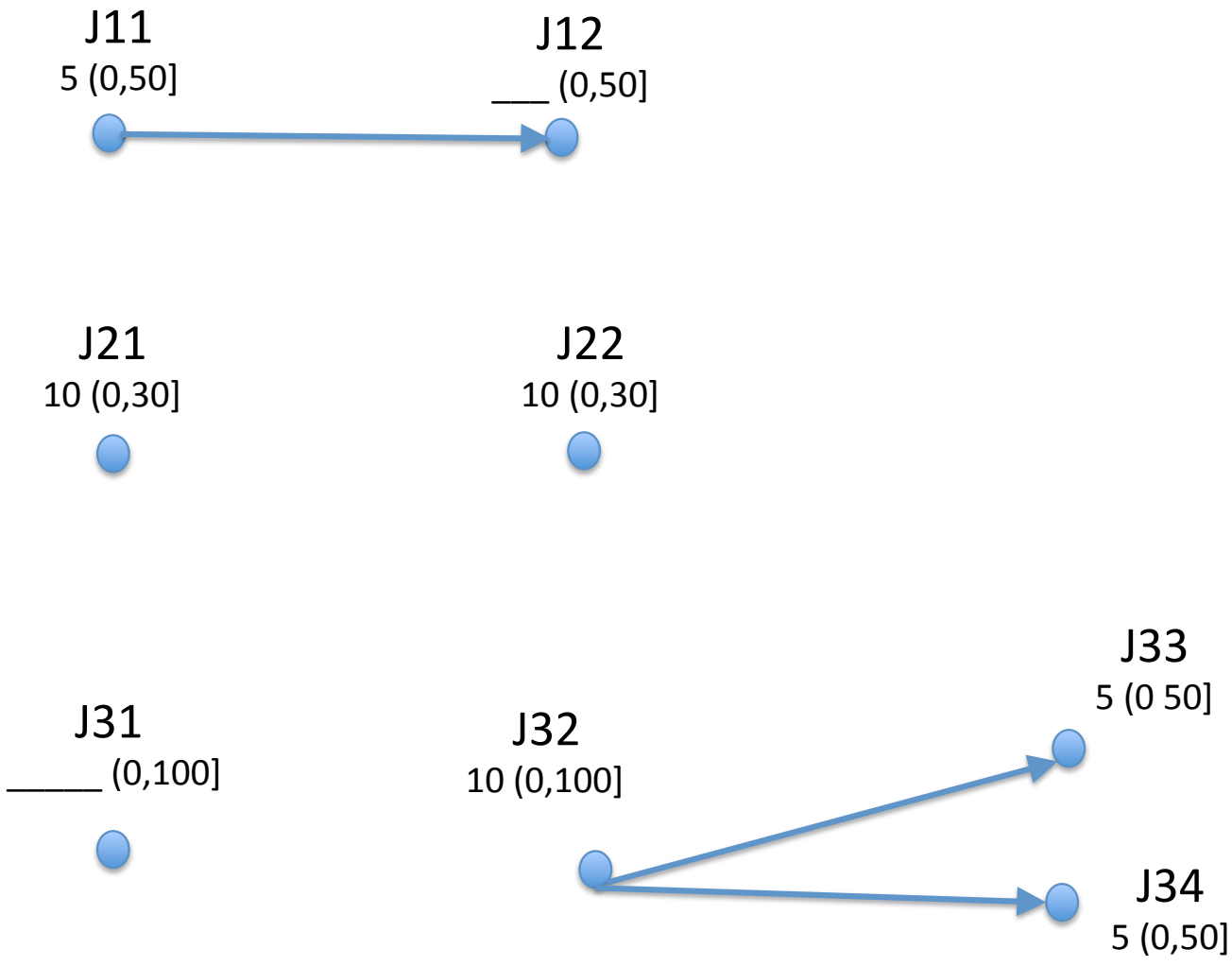

Figure Q3.a Precedence graph for Job set $J11...J34$

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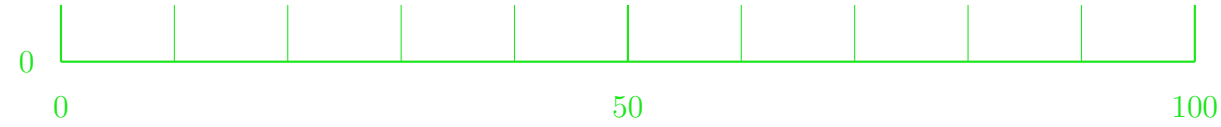

Figure Q3(a)iii Grid for Cyclic Schedule for Job set $J11...J34$

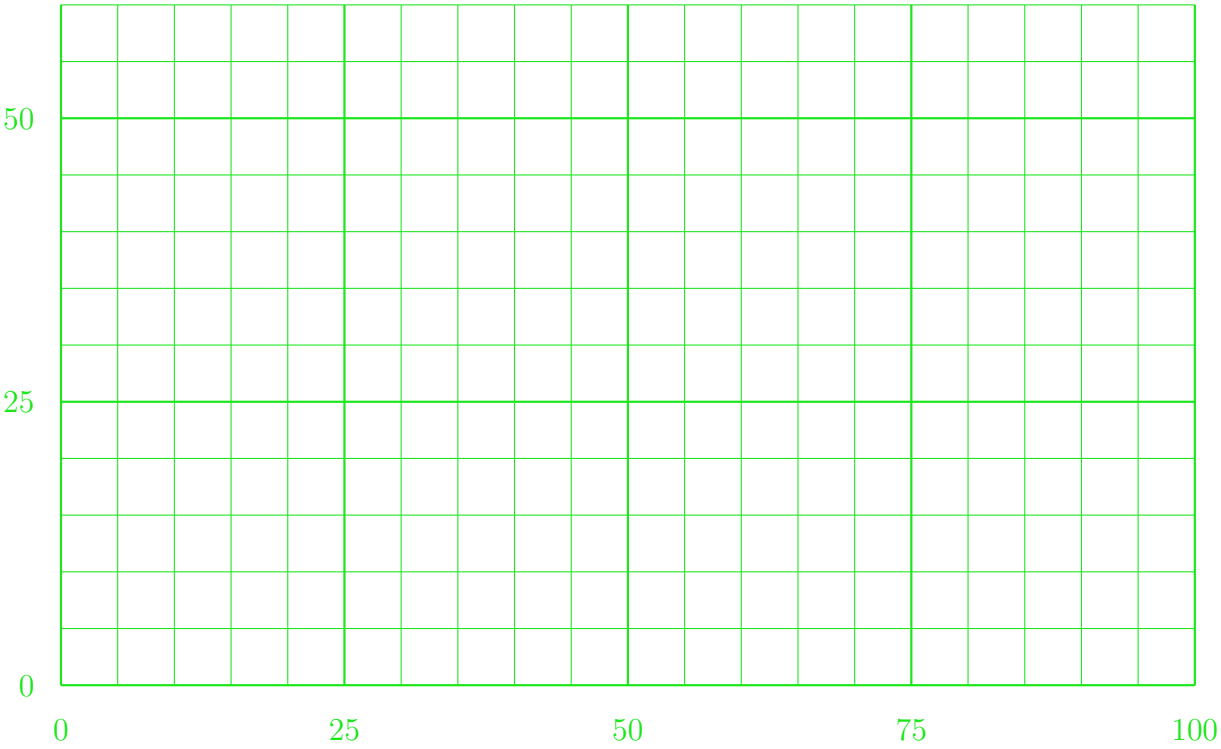

Figure Q3.b Grid for Pre-emptive Priority Timeline(s) for Job set $J11...J34$

END OF EXAM PAPER