THE UNIVERSITY OF THE WEST INDIES
ST. AUGUSTINE

EXAMINATIONS OF DECEMBER 2011

Code and Name of Course: **ECNG3006 Microprocessor Systems: Design and Appl'n**

Date and Time: **Wednesday 14th December - JFK 9 AM** Duration: **Three hours**

INSTRUCTIONS TO CANDIDATES: This paper has 7 pages and 4 questions. Max. Marks: **90**

ID# _____

Attempt ALL questions.
Questions 1-3 are each worth 20 marks.
Question 4 is worth 30 marks.

This exam contributes 50% of the final course grade.
You must pass this exam in order to pass the course.

The following reference information is provided:

- Requirements for OverTemperature Shutdown System (OTSS)[1] - page 4
- Proposed solution: Block Diagram, Kernel Requirement, Task Division- pages 4, 5
- Functional description of Dallas 1822[2] - page 6
- Electrical Information for Dallas 1822 and MicroChip PIC18F452[3] - page 7

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Q1. Kernels are used to facilitate **task management**.

(a) Draw a diagram to illustrate task states and the functions that cause tasks to change state under a typical kernel. *4 marks*

(b) Critically appraise the roles of the kernel and the scheduler within a real-time operating system. Which is more important and why? *6 marks*

(c) Mutexes, semaphores, and messages are **mechanisms** used by kernels. These mechanims can be used to achieve resource management, synchronization and inter-task communication **functions** within jobs.
Identify the mechanism **best** suited for **each** function; justify your choices. *6 marks*

(d) Identify, and assess the validity of, **one** task-management guideline/feature that appears in an RTOS-related standard. Your answer should examine the assumptions underlying the guideline/feature and make specific reference to at least one of the following standards: POSIX 1b, MISRA C/C++, μITRON 4.0, OSEK/VDK 2.2.3. *4 marks*

Q2. The application platform used should possess certain **hardware features**.

(a) The μCOS-II kernel requires a processor that provides a user-accessible processor stack and an internal hardware timer that can generate interrupts.
Explain how the μCOS-II kernel makes use of these two processor features. *4 marks*

(b) "The PIC 16F877 micro-controller is unsuited for real-time systems". Rebut this statement by showing how, under certain restrictions, the PIC16F877 can be used for real-time systems. Your answer should identify the restrictions, as well as the needs/requirements of real-time systems. *6 marks*

(c) An engineer, working on a mission-critical embedded system, must retrieve a 12-bit temperature reading, with $\pm 0.1^\circ$ Celsius accuracy, at 5 second intervals, for a room in which eight Dallas 1822 temperature sensors are distributed. The sensors are all connected to a PIC18F452 via a single Dallas 1-wire bus.
(S)he wants to flip a coin to decide between two strategies:

i. reading a single randomly chosen sensor at 12 bit accuracy, *4 marks*

ii. reading all 8 sensors at 9 bit accuracy, and averaging to get a 12-bit result. *4 marks*

For each strategy, determine the accuracy of 12 bit value(s), and estimate the time required to initiate temperature conversion, read the relevant sensor(s), and provide the 12-bit result. State all assumptions/considerations.

iii. What verbal advice would **you** offer to the engineer? *2 marks*

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Q3. System behavior can be predicted, monitored and analyzed using standard **performance metrics, analytical methods, techniques, and tools**.

(a) Describe the concept of the **idle task**, and explain it's role in allowing the kernel to track actual **system utilization**. *4 marks*

(b) "**Testing** interrupt-rich code has always been recognized as difficult. This is due in large part to the unpredictability, and unreproducibility, of real-world events". Do you agree with the statement? Justify your opinion by critically reviewing the relevant testing methodology. *6 marks*

(c) Identify and describe one technique for determining an **appropriate** task stack size. Is your chosen technique more likely to under-size or over-size the task stack? What are the potential ramifications of using a "bad" task stack size generated using this technique? *6 marks*

(d) Timelines and precedence graphs are visual tools that illustrate the behavior of real-time jobs. **Contrast** the two tools in terms of the system constraints that can be observed. *4 marks*

Q4. For the Over-Temperature Shutdown System (OTSS) (as described on pages 4 and 5):

(a) Identify appropriate task parameters (ϕ, p, e, D) for each Task P, S, R. *4 marks*

(b) Appropriately subdivide tasks into jobs, and identify the job parameters:

$$J_{Q,n} : e_{Q,n}(r_{Q,n}, d_{Q,n}]$$

for all job instances n belonging to individual tasks during the first hyper-period. *6 marks*

(c) Draw the job precedence graph - use this graph to determine effective deadlines and release times, and identify potential sources of jitter. Show your reasoning. *10 marks*

(d) Calculate the system utilization. How will the kernel tick size and overhead affect your calculation? Show your reasoning. *4 marks*

(e) Based on the preceding analyses, critically assess system performance. Your answer should identify potential system hazards, and consider whether a pre-emptive priority based scheduler is suitable for the application. *6 marks*

END OF QUESTIONS

1 2 3

[1]Case Information is taken from/based on Data Center Over-Temperature Shutdown System Overview `http://uscms-docdb.fnal.gov/cgi-bin/ShowDocument?docid=3211` and Requirements `http://uscms-docdb.fnal.gov/cgi-bin/ShowDocument?docid=3018`

[2]Datasheet for DS1822 Econo 1-Wire Digital Thermometer - Dallas Semiconductor - `http://www.maxim-ic.com`

[3]PIC18FXX2 Data Sheet, High Performance, Enhanced FLASH Microcontrollers with 10-Bit A/D, MicroChip Document DS39564B `http://www.microchip.com`

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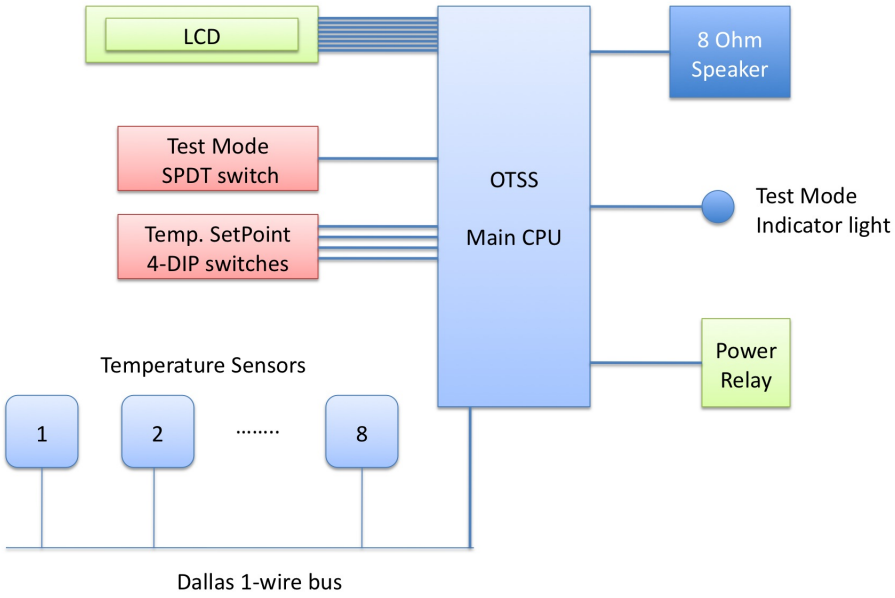
Requirements for ...Data Center Over-Temperature Shutdown System (OTSS)[1]

"This system ...protect[s] equipment in ...data centers from activation of fire sprinklers due to high temperature caused by insufficient cooling conditions [as opposed to fire conditions]. When triggered ..., the Over-Temperature Shutdown System [OTSS] will cause a main power disconnect for all non-safety related systems in the data centers. Emergency lighting, fire, and security systems are not connected to the [OTSS]."

- "[There is] an array of eight temperature sensors mounted in the ceiling area of the computer room."
- "[the main breaker] feeding power to [the] computer room ...is equipped with a shunt-trip coil that is designed to trip the breaker when powered from ...the OTSS ...through power relays"
- "The OTSS must turn off all major power ...when the temperature in the room reaches a preset limit. This limit is to be adjustable within the range of 30°C and 70°C. The OTSS must generate a power off trip within 15 seconds of the measured room temperature exceeding the trip set point. The system must be designed to minimize nuisance trips to every extent possible."
- "[The OTSS will] fail in the power-on mode to minimize data center down time"
- "[The OTSS will have" disconnect switches and indicators to allow periodic testing of the system without powering off the computer room"
- "[The OTSS will have] a local temperature display"

Proposed solution for OTSS - Block diagram



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Proposed solution - Kernel Requirements + Task Division

The embedded kernel selected for the OTSS must meet the following requirements:

- kernel tick resolution of 100 milli-seconds (ms), with nominal kernel overhead of 10 ms per tick
- pre-emptive priority based scheduler with support for the Shortest Job First scheduling algorithm
- support for 3 distinct tasks:
  - Task P is responsible for serially polling each of the temperature sensors, and determining the "correct" temperature.
  - Task S is responsible for updating the LCD display within 1 second of a temperature reading.
  - Task R is responsible for comparing the temperature reading with the set-point (set using switches), updating the test mode indicator LED, and triggering the relay (in run mode) or the speaker (in test mode).
- support for mutexes and semaphores:
  - Task S is released by a semaphore generated by Task P
  - All tasks must access the final temperature reading using a mutex
  - Blocking is resolved via priority inheritance using the Immediate Ceiling Priority Protocol

Task Name	Operation
P	job(s) released periodically every 5 seconds reset all sensors (1 ms) initiate 12-bit temperature read on all sensors (971 ms) for i = 1 to 8 (1 ms) read sensor i (10 ms) calculate average of all sensor readings (1 ms) update final temperature (1 ms + mutex wait time)
S	job(s) released on temperature update (semaphore available) retrieve final temperature (1 ms + mutex wait time) convert temperature reading to ASCII string (max 16 chars) (1 ms) place cursor on LCD (1 ms) while there are characters left (1 ms) transmit next character to LCD (1 ms)
R	job(s) released periodically every 5 seconds read DIP switches and update setpoint (1 ms) read test-mode switch and turn test-mode LED on/off (1 ms) retrieve final temperature (1 ms + mutex wait time) if final temperature is greater than setpoint (1 ms) if test-mode (1 ms) turn on speaker (1 ms) else activate relay (1 ms) else turn off speaker (1 ms) deactivate relay (1 ms)

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Dallas 1822 Functional Description[2]

"The DS1822 communicates over a 1-Wire bus that by definition requires only one data line (and ground) for communication with a central microprocessor. It has an operating temperature range of 55C to +125C and is accurate to 2.0C over the range of 10C to +85C. ...
The DS1822 uses Dallas exclusive 1-Wire bus protocol that implements bus communication using one control signal. The control line requires a weak pullup resistor since all devices are linked to the bus via a 3-state or open-drain port (the DQ pin in the case of the DS1822). In this bus system, the microprocessor (the master device) identifies and addresses devices on the bus using each devices unique 64-bit code. ...
The core functionality of the DS1822 is its direct-to-digital temperature sensor. The resolution of the temperature sensor is user-configurable to 9, ...or 12 bits, corresponding to increments of 0.5C, ...and 0.0625C, respectively. ...
to initiate a temperature measurement and A-to-D conversion, the master must issue a Convert T [44h] command. Following the conversion, the resulting thermal data is stored ...in the scratchpad memory ...
The DS1822 output temperature data is calibrated in degrees centigrade; ...The temperature data is stored as a 16-bit sign-extended twos complement number .... The sign bits (S) indicate if the temperature is positive or negative: for positive numbers S = 0 and for negative numbers S = 1. If the DS1822 is configured for 12-bit resolution, all bits in the temperature register will contain valid data ..., and for 9-bit resolution bits 2, 1 and 0 are undefined. ...
[At the start of each communication sequence] the bus master transmits (TX) the reset pulse by pulling the 1-Wire bus low for a minimum of 480μs. The bus master then releases the bus and goes into receive mode (RX). When the bus is released, the 5k pullup resistor pulls the 1-Wire bus high. When the DS1822 detects this rising edge, it waits 15μs to 60μs and then transmits a presence pulse by pulling the 1-Wire bus low for 60μs to 240μs.
The bus master writes data to the DS1822 during write time slots and reads data from the DS1822 during read time slots. One bit of data is transmitted over the 1-Wire bus per time slot. ...time slots must be a minimum of 60μs in duration with a minimum of a 1μs recovery time between individual ...slots.
[ROM] commands operate on the unique 64bit ROM codes of each slave device and allow the master to single out a specific device if many are present on the 1-Wire bus. .... each command is 8 bits long. The master device must issue an appropriate ROM command before issuing a DS1822 function command.

- MATCH ROM [55h] The match ROM command followed by a 64-bit ROM code sequence allows the bus master to address a specific slave device ...only the slave that exactly matches the 64-bit ROM code sequence will respond to the function command issued by the master ...
- SKIP ROM [CCh] The master can use this command to address all devices on the bus simultaneously without sending out any ROM code information. For example, the master can make all DS1822s on the bus perform simultaneous temperature conversions by issuing a Skip ROM command followed by a Convert T [44h] command.

After the bus master has used a ROM command to address the DS1822 with which it wishes to communicate, the master can issue one of the DS1822 function commands. These commands allow the master to ...read from the DS1822s scratchpad memory, [and] initiate temperature conversions.

- CONVERT T [44h] This command initiates a single temperature conversion. Following the conversion, the resulting thermal data is stored ...in the scratchpad memory
- READ SCRATCHPAD [BEh] This command allows the master to read the contents of the scratchpad. The data transfer starts with the least significant bit of byte 0 and continues through the scratchpad until the 9th byte (byte 8 - CRC) is read.

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Dallas 1822 Electrical Characteristics[2]

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	Local Power	+3.0		+5.5	V
Pullup Supply Voltage	V_{PU}	Local Power	+3.0		V_{DD}	V
Thermometer Error	t_{ERR}	-10C to +85C			±2	° C
Input Logic Low	V_{IL}		-0.3		+0.8	V
Input Logic High	V_{IH}	Local Power	+2.2		V_{DD} + 0.3 (max 5.5)	V
Sink Current	I_L	$V_{I/O} = 0.4V$	4.0			mA
Standby Current	I_{DDS}			750	1000	nA
Active Current	I_{DD}	$V_{DD} = 5V$		1	1.5	mA
DQ Input Current	I_{DQ}			5		μA
Drift				±0.2		°C
Capacitance	$C_{IN/OUT}$				25	pF

PIC18F452 Electrical Characteristics[3]

Output Pin Load resistance	R_L	464Ω
Output Pin Load capacitance	C_L	50 pF
Input Pin capacitance	C_{in}	5 pF
Max. Port output rise/fall time	T_{io}	40ns
Max. Delay port output	$T_{os}H2_{io}$	255ns
Min. Input Hold time	$T_{os}H2_{io}I$	100 ns
Max. current sunk/sourced by output (ignoring totals)		20mA
Max. input leakage current	I_{IL}	±1μA
Output Low Voltage	V_{OL}	0.6V
Output High Voltage	V_{OH}	$V_{DD} - 0.7$ Volts
Max. Input Low Voltage (TTL)	V_{IL}	$0.15V_{DD}$ Volts
Min. Input High Voltage (TTL)	V_{IH}	$0.25V_{DD} + 0.8$ Volts
Max. Input Low Voltage (ST)	V_{IL}	$0.2V_{DD}$ Volts
Min. Input High Voltage (ST)	V_{IH}	$0.8V_{DD}$ Volts

All voltages must lie between V_{dd} and V_{ss}. All ratings taken at 25°. Pins on ports C,D and E are normally Schmitt Trigger inputs, push-pull outputs. Port A pin 4 is a Schmitt Trigger input, open-drain output. All other pins are normally TTL level inputs, push-pull outputs. Input circuitry on some pins changes depending on the pin function selected.

END OF QUESTION PAPER