THE UNIVERSITY OF THE WEST INDIES
ST. AUGUSTINE

EXAMINATIONS OF December 2016

Code and Name of Course: **ECNG3006 Microprocessor Systems** Paper: **Final**

Date and Time: **9 Dec 2016 9AM** Duration: **Three (3) hours**

INSTRUCTIONS TO CANDIDATES: This paper has 5 pages and 3 questions. Max. Marks: **100**

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Attempt ALL questions.
Questions 1-2 are each worth 25 marks.
Question 3 is worth 50 marks.

Questions Q3.a and Q3.b should be answered on page 5
and the script returned with your exam booklet.

The following reference information is provided:

- Simplified Description of Aircraft Braking System on page 4

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Q1. μCOS-II is an example of a commercial real-time operating system (RTOS) kernel which supports both mutexes and semaphores, as well as both co-operative, and pre-emptive, priority based multi-tasking systems.

(a) Describe the role of the Task Control Block structure within the task scheduling and context switching functions of the μCOS-II kernel. *5 marks*

(b) Compare and contrast the creation and usage of a mutex and a binary semaphore for resource access in μCOS-II. *5 marks*

(c) Compare the performance goal(s) of co-operative priority-based schedulers and pre-emptive priority-based schedulers. Support your answer by identifying at least **one** reason why developers choose to use or not use co-operative scheduling. *5 marks*

(d) Define the term "jitter", and explain how jitter can be observed and quantified for a system designed around μCOS-II. Support your answer by identifying two possible causes of jitter. *5 marks*

(e) *"Multi-tasking provides better average task performance (reduced response-time) than cyclic executives."*

Discuss the validity of the statement. If **true**, why do embedded system designers sometimes prefer cyclic executives? If **false**, why do embedded system designers sometimes prefer multi-tasking solutions? *5 marks*

[Q1 Total 25 marks]

Q2. An embedded real-time system consists of a PIC18 micro-controller connected to a 4x16 LCD display via an 8-bit interface, as well as a digital temperature sensor which can be configured for 8 to 12 bits of resolution.

(a) Differentiate between sensor linearization and sensor calibration. Explain how each can be used in the temperature sensor in either hardware or software. *5 marks*

(b) Determine the maximum rate at which parallel 8-bit data can be clocked out from a microprocessor whose output pin rise/fall time is $t\mu s$. You should presume a separate clock line is in use. State any assumptions and explain your reasoning. *5 marks*

(c) "If the noise effect rather than quantization predominates, the resolution can be increased by averaging several readings." Explain this statement. Why does averaging not "work" if quantization rather than noise predominates? *5 marks*

(d) "The PIC 16F877 micro-controller is unsuited for real-time systems". Discuss this statement. Show how, under certain restrictions, the PIC can be used for these systems. *5 marks*

(e) Using a sample C-like code, identify the key function calls in the C18 libraries for accessing the LCD. Your answer(s) do not need to be syntactically correct. *5 marks*

[Q2 Total 25 marks]

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Q3. These questions will be based on an embedded system scenario with real time requirements: "Simplified Description of Aircraft Braking System". Jobs and tasks for such a system are described on page 4.

(a) Use the graph paper on page 5 to construct a **cyclic schedule** for the execution of these jobs where the minor cycle is 10ms. *5 marks*

(b) Use the graph paper on page 5 to construct appropriate **task timelines** for the execution of these jobs assuming that they are scheduled using a pre-emptive priority based scheduler, with a 2ms tick, where Task 1 has the highest priority, followed by Task 2, then Task 3, and Task 4 has the lowest priority. *10 marks*

(c) Compare the task performance achieved using the cyclic executive, and the pre-emptive priority based scheduler. Your answer should clearly identify at least **two** criteria you could use for comparison, and explain which system you would prefer to implement and what adjustments (if any) you would make. *10 marks*

(d) Contrast the Rate Monotonic and Least Slack Time Scheduling algorithms. Support your answer by determining the relative priorities of the 4 Tasks for each scheduling algorithm. *10 marks*

(e) You have been asked to modify the implementation so that a foreground-background system may be used. To do so, the Brake Pedals will deliver an interrupt-on-change signal when the Brake Position changes, and a timer will be configured to interrupt at 10ms intervals.

In the revised system, Tasks 3 and 4 runs in the background, Task 1 is called in the interrupt handler for the timer, and Task 2 is called in the interrupt handler (foreground) for the interrupt on change. Assess whether the suggested scheme is feasible, and if it offers any benefits. Your answer should identify all resources and procedures you would require to detect and/or address any subsequent issues. *15 marks*

[Q3 Total 50 marks]

END OF QUESTIONS

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Figure Q3 – Simplified Description of Aircraft Braking System

Based on: Smartcockpit.com - BOEING 767 SYSTEMS REVIEW
`http://www.smartcockpit.com/download.php?path=docs/&file=B767_Brakes.pdf`
and Landing Gear `http://www.smartcockpit.com/docs/Boeing_767-300-Landing_Gear.pdf`

The airplane has two main landing gear. Each main gear has four wheels in tandem pairs. Each wheel is fitted with a hydraulically powered disc brake. The left and right brake pedals provide independent control of the hydraulic pressure applied to the left and right sets of brakes. Pushing a brake pedal opens the respective brake valve. The parking brake is set by fully depressing both brake pedals, pulling the parking brake handle up, then releasing the pedals. The parking brake is released by depressing the pedals until the parking brake handle releases. Brake temperature values range from 0 to 9. Temperature values are not instantaneous and tend to build for 10 to 15 minutes after the brakes are applied. A brake temperature monitor system will illuminate the BRAKE TEMP light for temperature values of 5 and above.

System Input:	• Parking Brake Handle Position (Up/Down) • Left/Right Brake Pedals (Fully Depressed(31)/Not Depressed(0)) • Left/Right Brake Temperature Sensor (continuous value 0 - 9) • Hydraulic Pump Pressure Sensor (continuous value 0 - 255)
System Output:	• Left/Right Hydraulic Valve (continuous value 0 - 31); response time 10 ms • Handle State (Released/Locked) • Parking Hydraulic Valve (On/Off); response time 10 ms • Hydraulic Pump Command (continuous value 0 - 63) • Brake Temperature Light (On/Off)
Task 1: Hydraulic Pump Control	Feedback control of Hydraulic Pump Pressure; Runs at 10 ms intervals. **J11, e=1ms** read Pressure Sensor **J12, e=2ms** after J11, calculate new Pressure Command **J13, e=1ms** after J12, output new Pressure Command
Task 2: Brake Pedal Update	Read status of Brake Pedals and controls valves accordingly; Runs at 10ms intervals. Phase Delay 5ms. **J21, e=1ms** read Left Brake Pedal - output value to Left Valve **J22, e=1ms** after J21, read Right Brake Pedal - output value to Right Valve
Task 3: Parking Brake	Engages and disengages Parking Brake; Runs at 50ms intervals. **J31, e=2ms** read Left Brake Pedal and Right Brake Pedal **J32, e=1ms** after J31, if both pedal readings are 31 then Lock Parking Handle **J33, e=1ms** after J32, if both pedals readings are 0 then Release Parking Handle **J34, e=1ms** after J33, if Parking Handle Position is Up and Parking Handle is Locked then turn Parking Valve On **J35, e=1ms** after J34, if Parking Handle is Released then turn Parking Valve Off
Task 4: Brake Temperature Monitor	Reads the Temperature Sensors, and controls the BRAKE TEMP Light. Runs at 50 ms intervals. **J41, e=3ms** read Temperature Sensors; store the maximum value retrieved **J42, e=1ms** after J41, if temperature is > 5 then turn on BRAKE TEMP; else turn off BRAKE TEMP

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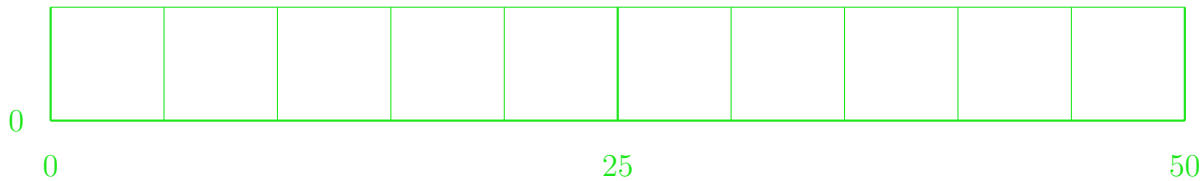

Figure Q3.a Grid for Cyclic Schedule for Job set $J11...J42$

Figure Q3.b Grid for Pre-emptive Priority Timeline(s) for Job set $J11...J32$

END OF EXAM PAPER